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Passlack

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(54) **FIELD EFFECT TRANSISTOR WITH CONDUCTION BAND ELECTRON CHANNEL AND UNI-TERMINAL RESPONSE**

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H01L 27/092	(2006.01)
B82Y 10/00	(2011.01)
H01L 29/12	(2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ***H01L 27/092*** (2013.01); ***B82Y 10/00*** (2013.01); ***H01L 29/122*** (2013.01); ***H01L 29/20*** (2013.01); ***H01L 29/205*** (2013.01); ***H01L 29/432*** (2013.01); ***H01L 29/7783*** (2013.01); *H01L 29/201* (2013.01); *H01L 29/517* (2013.01); *H01L 31/03046* (2013.01); *H01L 31/035236* (2013.01); *H01L 31/1844* (2013.01)

(58) **Field of Classification Search**
CPC H01L 31/035236; H01L 31/03046; H01L 31/1844
USPC 257/12, 14, 15, 20, 27, 183, 220, 241, 257/287
See application file for complete search history.

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Assistant Examiner — John M Parker
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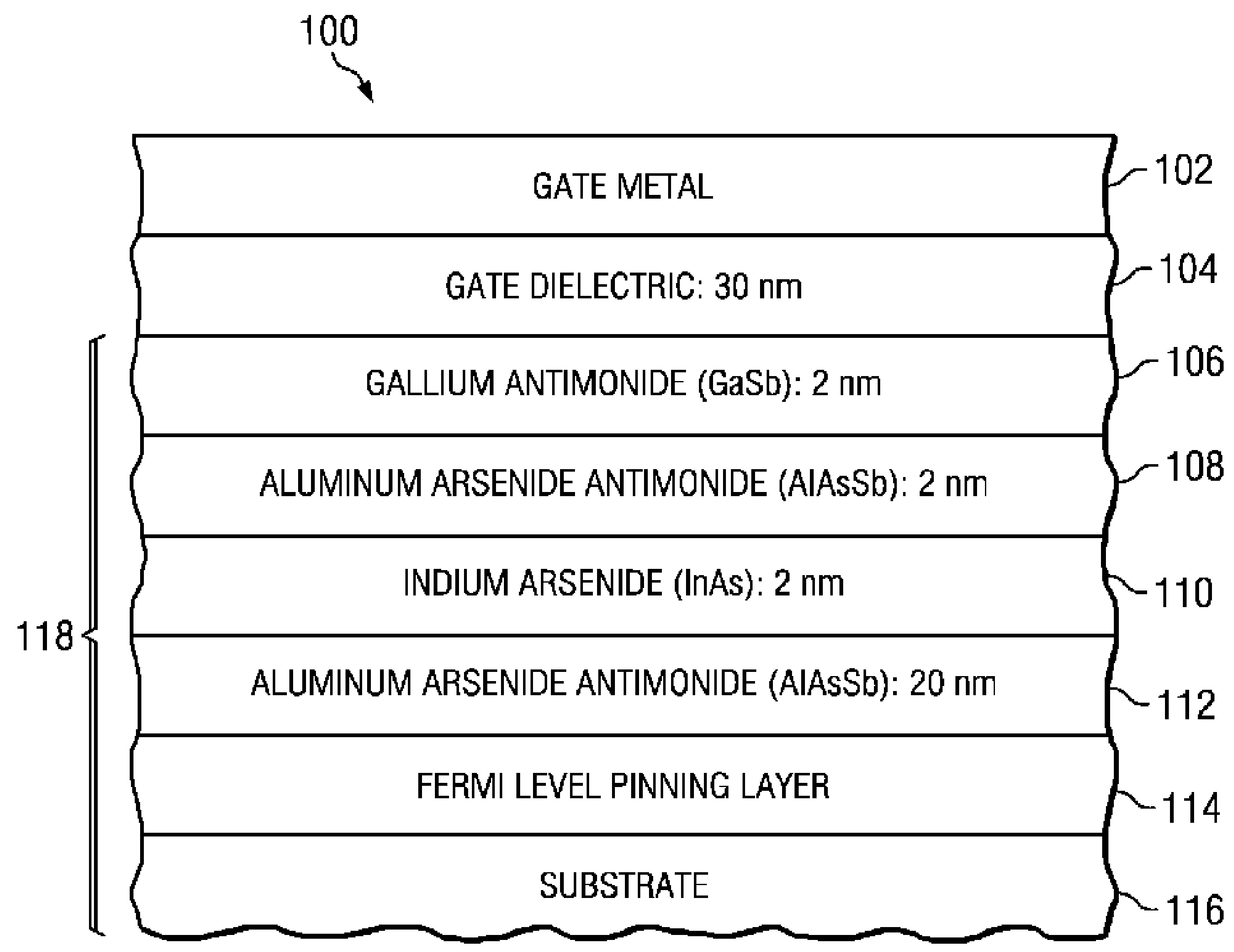
(57) **ABSTRACT**

A uni-terminal transistor device is described. In one embodiment, an n-channel transistor comprises a first semiconductor layer having a discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; a gate dielectric layer disposed above the first semiconductor layer; and a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

41 Claims, 5 Drawing Sheets



(51) **Int. Cl.**

H01L 29/205	(2006.01)
H01L 29/43	(2006.01)
H01L 29/778	(2006.01)
H01L 29/20	(2006.01)
H01L 31/18	(2006.01)
H01L 31/0352	(2006.01)
H01L 31/0304	(2006.01)
H01L 29/201	(2006.01)
H01L 29/51	(2006.01)

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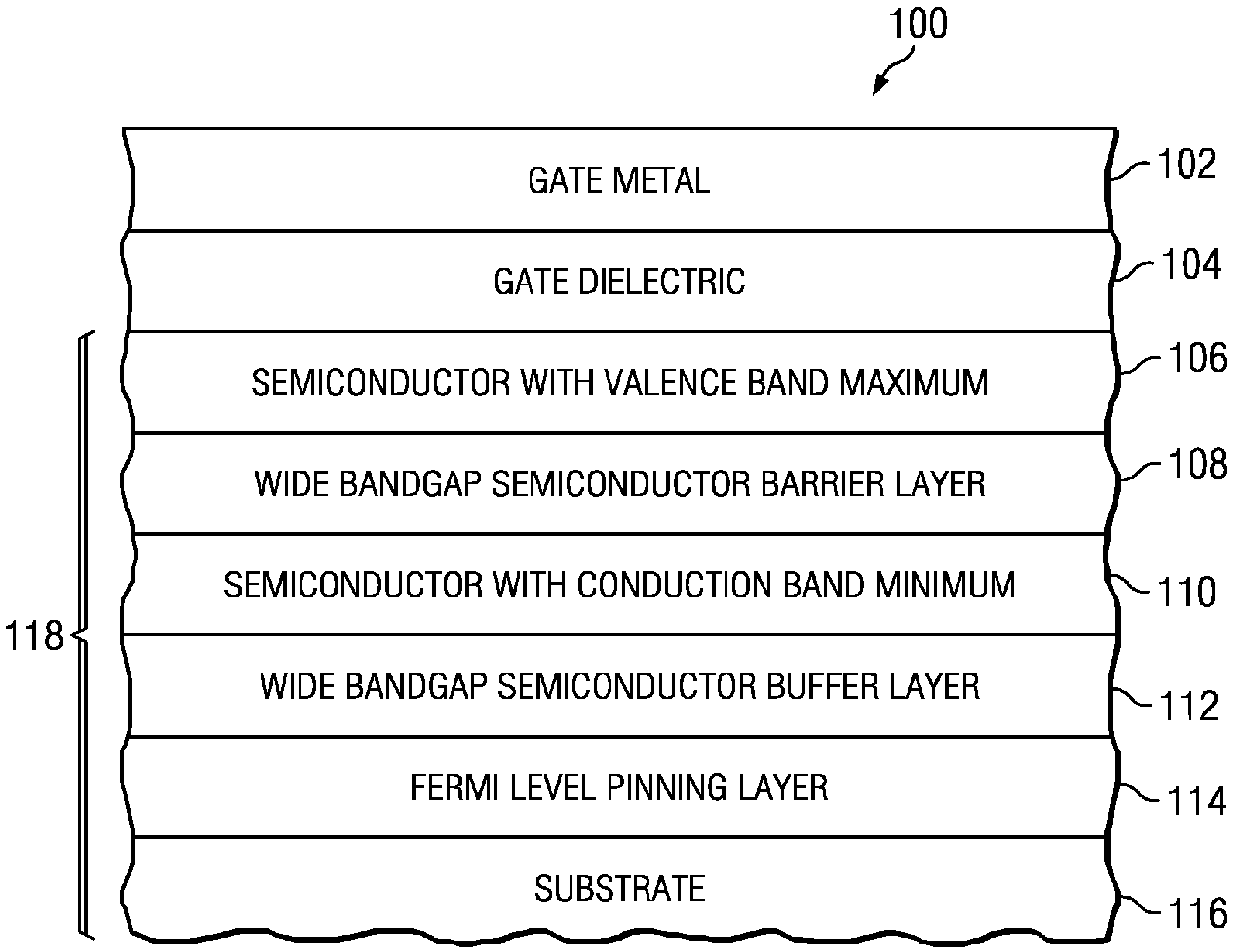

100
GATE METAL
102
GATE DIELECTRIC
104
SEMICONDUCTOR WITH VALENCE BAND MAXIMUM
106
WIDE BANDGAP SEMICONDUCTOR BARRIER LAYER
108
SEMICONDUCTOR WITH CONDUCTION BAND MINIMUM
110
118
WIDE BANDGAP SEMICONDUCTOR BUFFER LAYER
112
FERMI LEVEL PINNING LAYER
114
SUBSTRATE
116

Fig. 1

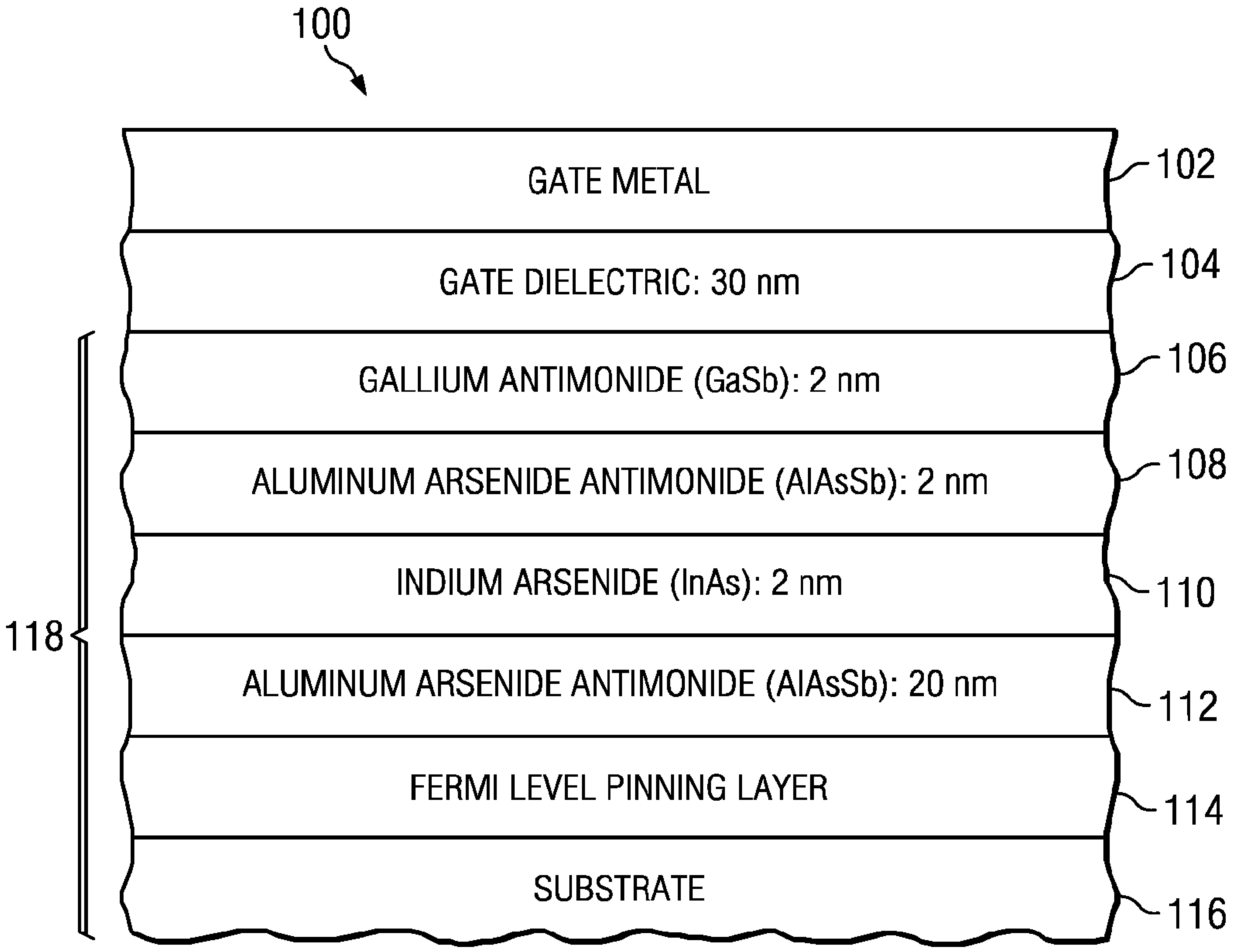
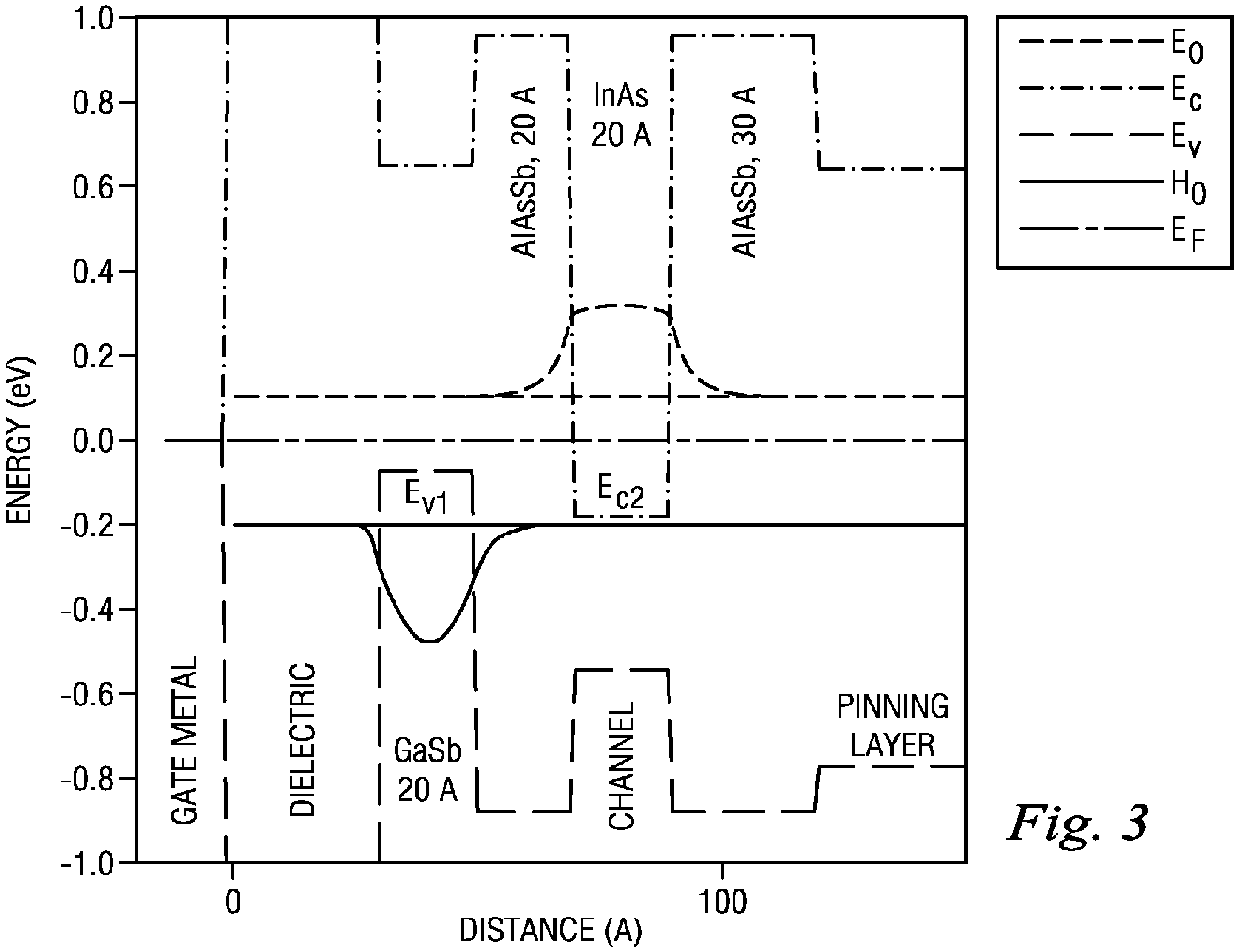

100
GATE METAL
102
GATE DIELECTRIC: 30 nm
104
GALLIUM ANTIMONIDE (GaSb): 2 nm
106
ALUMINUM ARSENIDE ANTIMONIDE (AlAsSb): 2 nm
108
INDIUM ARSENIDE (InAs): 2 nm
110
118
ALUMINUM ARSENIDE ANTIMONIDE (AlAsSb): 20 nm
112
FERMI LEVEL PINNING LAYER
114
SUBSTRATE
116

Fig. 2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0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
ENERGY (eV)
0
100
DISTANCE (A)
E_0
E_c
E_v
H_0
E_F
AlAsSb, 20 A
InAs
20 A
AlAsSb, 30 A
E_{v1}
E_{c2}
GATE METAL
DIELECTRIC
GaSb
20 A
CHANNEL
PINNING
LAYER

Fig. 3

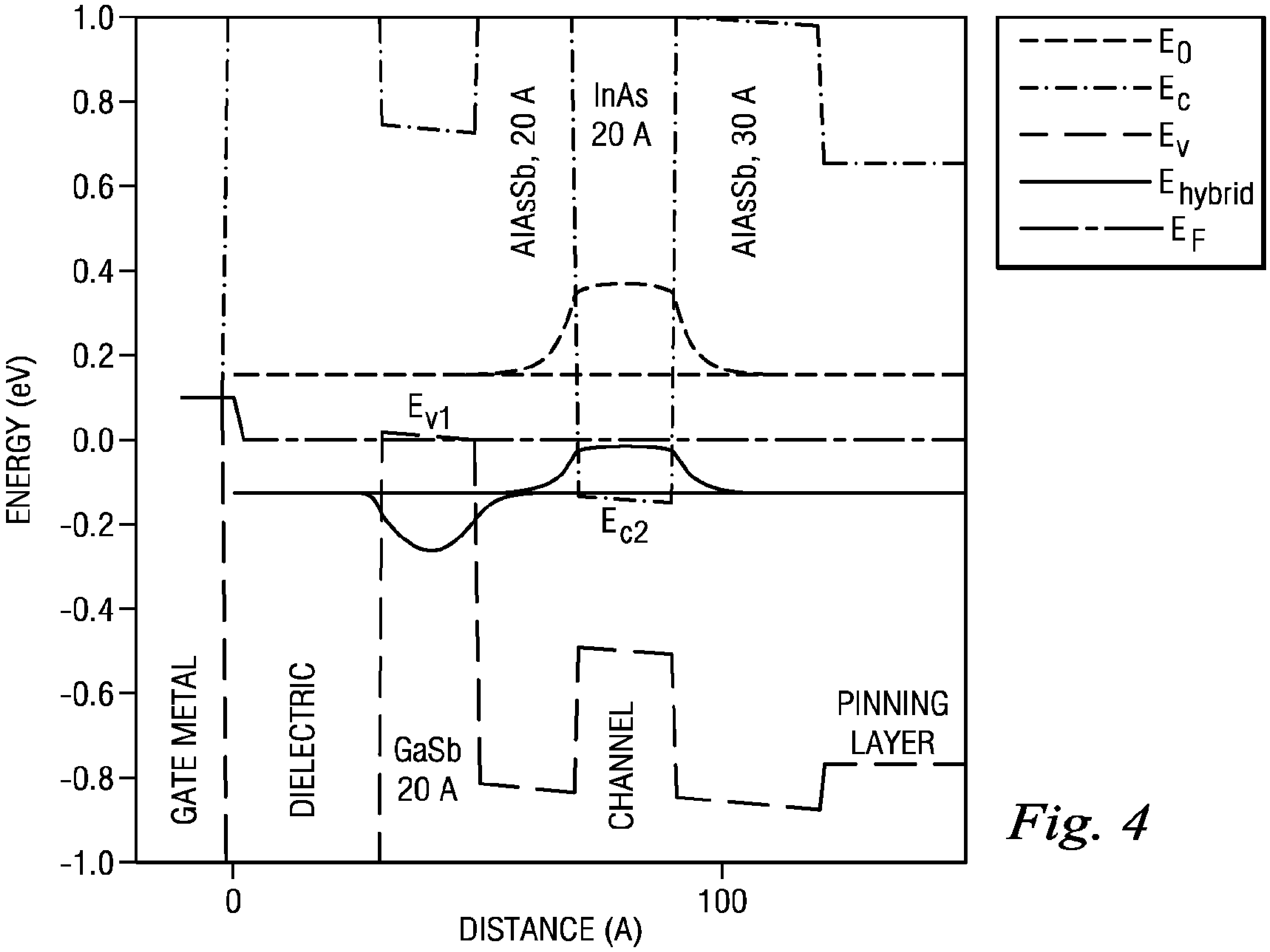
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
ENERGY (eV)
0
100
DISTANCE (A)
E_0
E_c
E_v
E_{hybrid}
E_F
AlAsSb, 20 A
InAs
20 A
AlAsSb, 30 A
E_{v1}
E_{c2}
GATE METAL
DIELECTRIC
GaSb
20 A
CHANNEL
PINNING
LAYER

Fig. 4

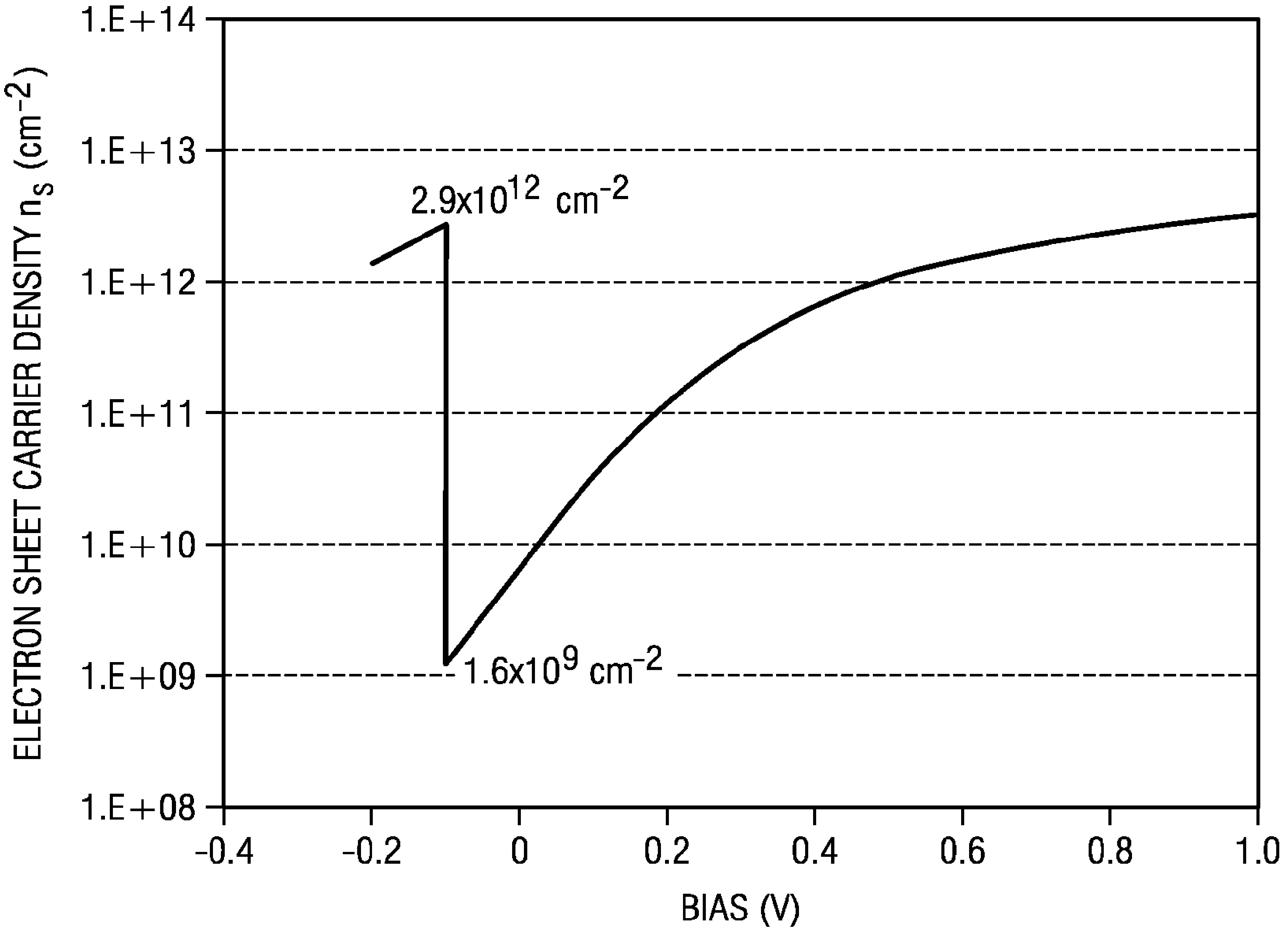
ELECTRON SHEET CARRIER DENSITY n_S (cm^{-2})
1.E+14
1.E+13
1.E+12
1.E+11
1.E+10
1.E+09
1.E+08
$2.9x10^{12}$ cm^{-2}
$1.6x10^{9}$ cm^{-2}
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1.0
BIAS (V)

Fig. 5

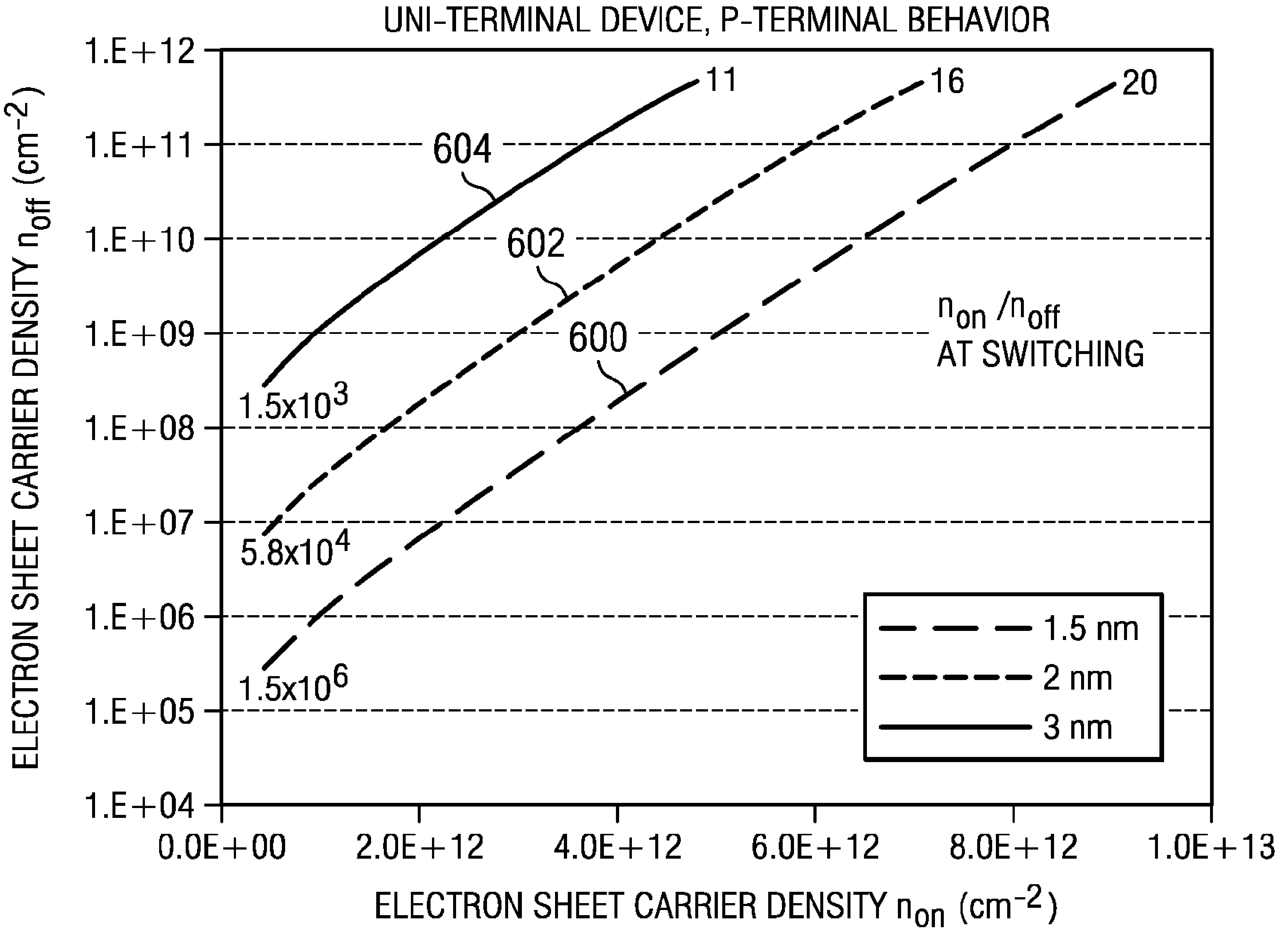
UNI-TERMINAL DEVICE, P-TERMINAL BEHAVIOR
ELECTRON SHEET CARRIER DENSITY n_{off} (cm^{-2})
1.E+12
1.E+11
1.E+10
1.E+09
1.E+08
1.E+07
1.E+06
1.E+05
1.E+04
11
16
20
604
602
600
n_{on}/n_{off}
AT SWITCHING
$1.5x10^3$
$5.8x10^4$
$1.5x10^6$
1.5 nm
2 nm
3 nm
0.0E+00
2.0E+12
4.0E+12
6.0E+12
8.0E+12
1.0E+13
ELECTRON SHEET CARRIER DENSITY n_{on} (cm^{-2})

Fig. 6

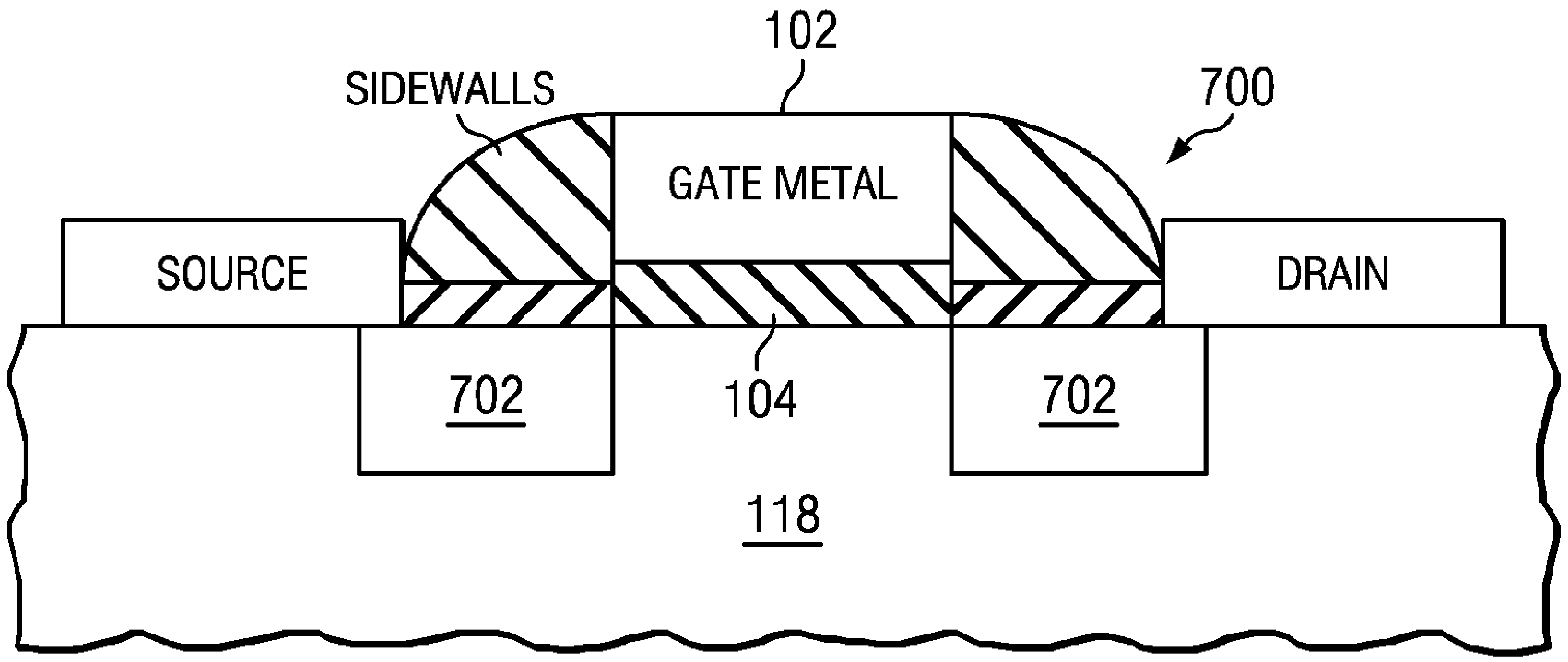
102
SIDEWALLS
700
GATE METAL
SOURCE
DRAIN
702
104
702
118

Fig. 7

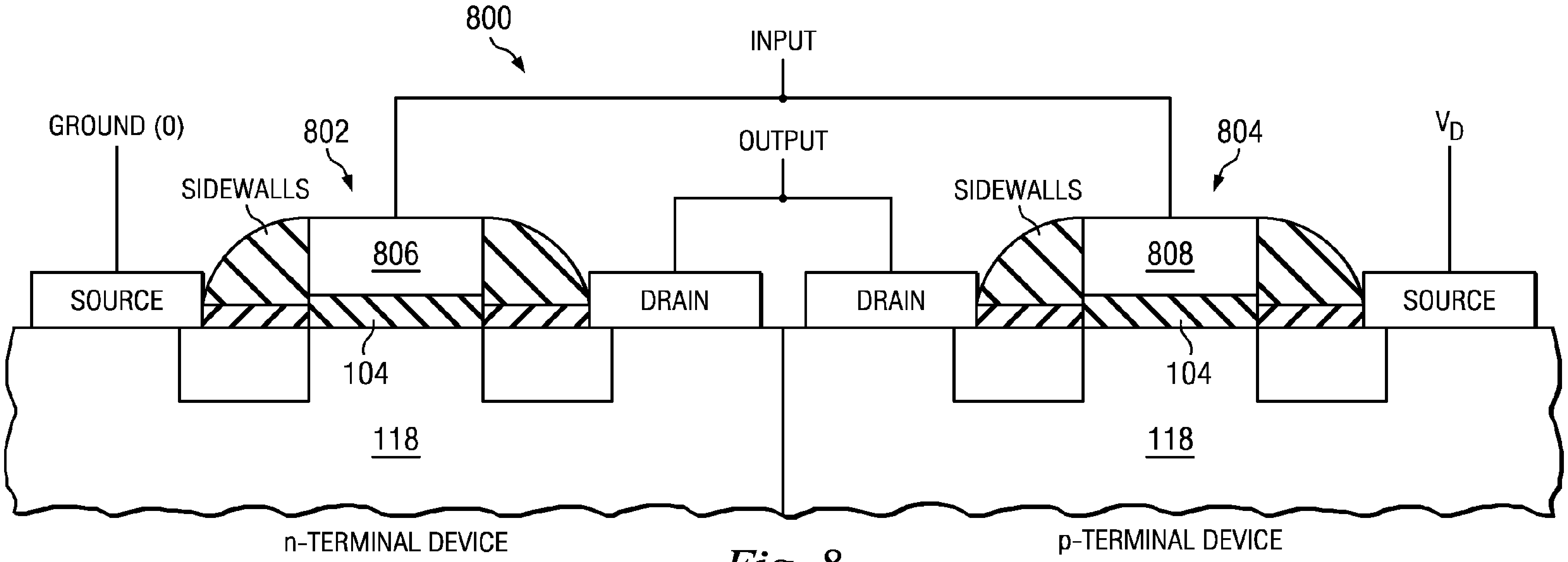
800
INPUT
GROUND (0)
802
OUTPUT
804
V_D
SIDEWALLS
SIDEWALLS
806
808
SOURCE
DRAIN
DRAIN
SOURCE
104
104
118
118
n-TERMINAL DEVICE
p-TERMINAL DEVICE

Fig. 8

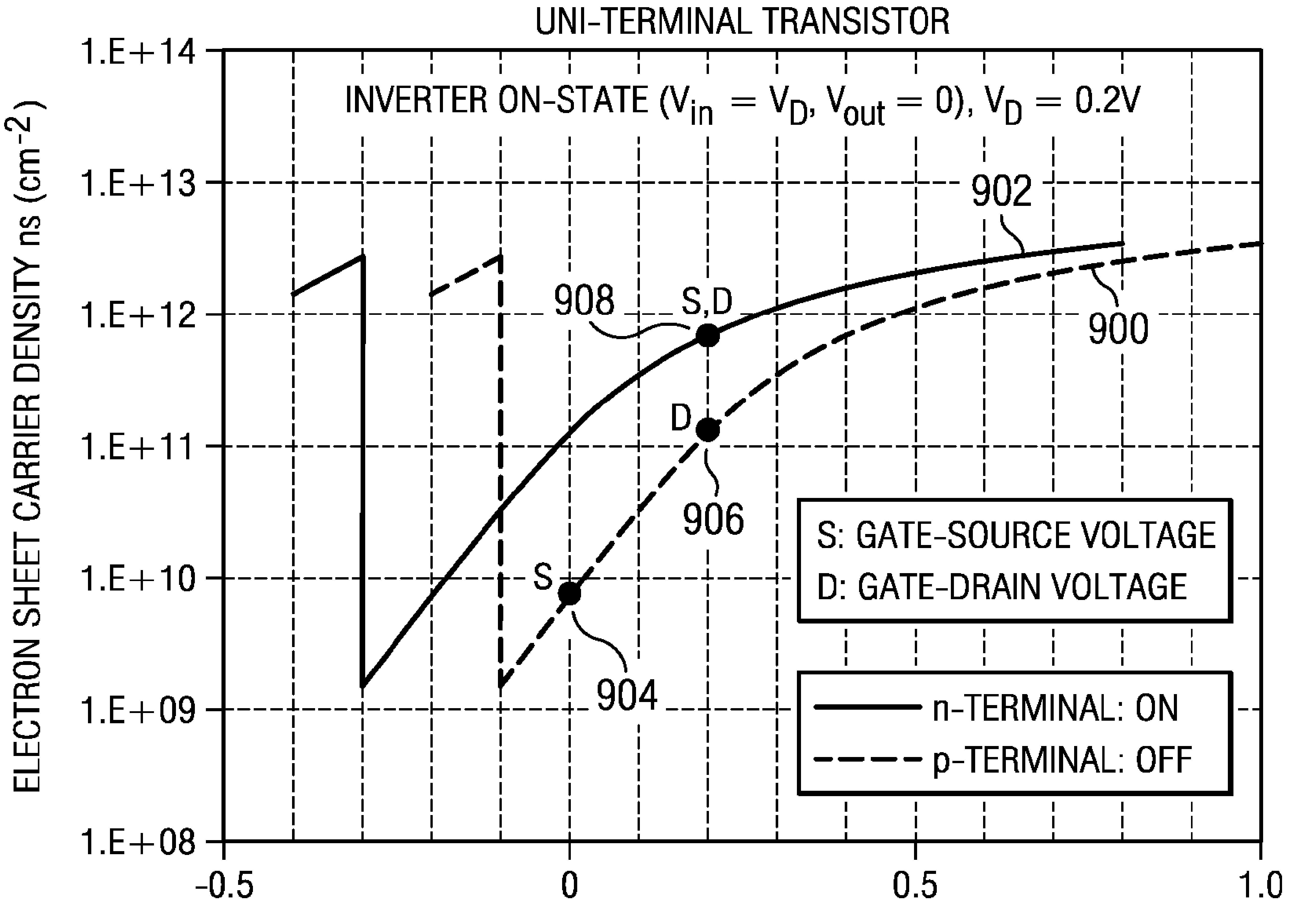

Fig. 9

INVERTER ON-STATE (V_{in}=V_D, V_{out}=0), V_D=0.2V

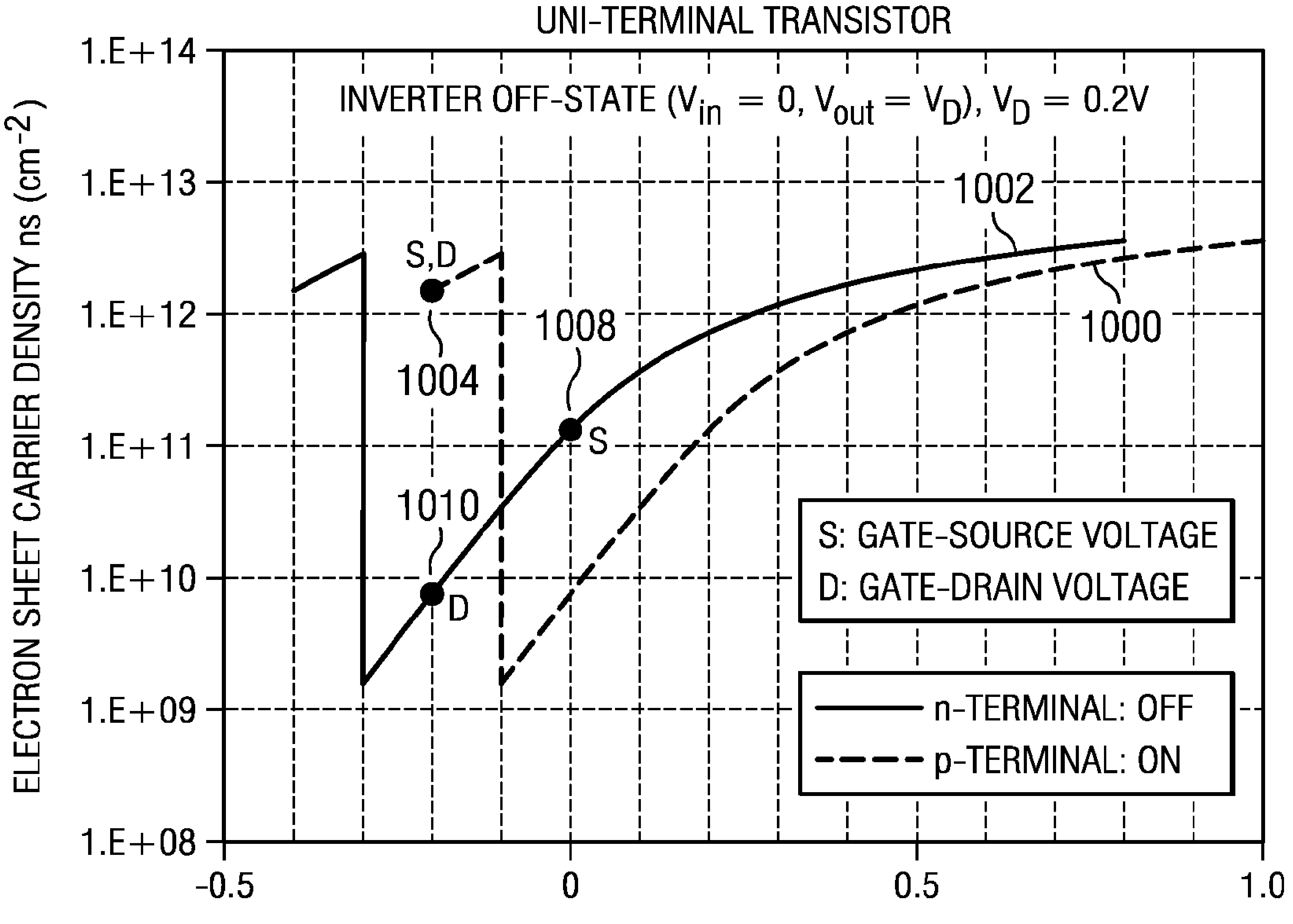

Fig. 10

INVERTER OFF-STATE (V_{in}=0, V_{out}=V_D), V_D=0.2V

FIELD EFFECT TRANSISTOR WITH CONDUCTION BAND ELECTRON CHANNEL AND UNI-TERMINAL RESPONSE

This patent claims the benefit of U.S. Ser. No. 61/303,025 filed Feb. 10, 2010, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

The present disclosure relates to field effect transistors ("FETs") with uni-terminal response, and more specifically to a common epitaxial layer structure that forms channels comprising conduction band electrons for both positive and negative gate bias for use in FETs with both n- and p-terminal characteristics.

Traditional complementary metal-oxide semiconductor ("CMOS") technology utilizes conduction band electrons to form the conducting channel in devices with n-terminal characteristics and valence band electrons (holes) in devices with p-terminal characteristics. The terminal characteristics of n-channel and p-channel devices are referred to as "complementary". When such complementary devices are connected in series, they form a basic logic gate, or an inverter. This basic complementary design has dominated digital electronics for decades because of its simplicity and low power dissipation; however, the performance of devices with p-channel characteristics is inferior to devices with n-channel characteristics because valence band electrons, or holes, exhibit substantially less mobility than conduction band electrons. This limits the performance of CMOS inverters.

Prior art has described the formation of a conducting channel utilizing conduction band electrons for both devices with p- and n-terminal characteristics (see, e.g., U.S. Pat. No. 5,355,005). However, each type of device uses its own epitaxial layer structure, which complicates manufacture and increases costs.

SUMMARY

One embodiment is an n-channel transistor comprising a first semiconductor layer having a discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; a gate dielectric layer disposed above the first semiconductor layer; and a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

Another embodiment is an n-channel transistor comprising a first semiconductor layer having a discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; a gate dielectric layer disposed above the first semiconductor layer; and a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain p-terminal characteristics.

Yet another embodiment is an inverter circuit comprising an n-channel transistor with n-terminal characteristics comprising a first semiconductor layer having a first discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; a first wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; a first gate dielectric layer disposed above the first semiconductor layer; and a first gate metal layer disposed above the first gate dielectric layer and having a first effective workfunction selected to position the first discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the first gate metal layer and to obtain n-terminal characteristics. The n-channel transistor with n-terminal characteristics further comprises a first set of extensions having n-type conductivity. The inverter circuit further comprises an n-channel transistor with p-terminal characteristics comprising a third semiconductor layer having a second discrete hole level H_0; a fourth semiconductor layer having a second conduction band minimum E_{C2}; a second wide bandgap semiconductor barrier layer disposed between the third and fourth semiconductor layers; a second gate dielectric layer disposed above the third semiconductor layer; and a second gate metal layer disposed above the second gate dielectric layer and having a second effective workfunction selected to position the second discrete hole level H_0 below the second conduction band minimum E_{c2} for zero bias applied to the second gate metal layer and to obtain p-terminal characteristics. The n-channel transistor with p-terminal characteristics further comprises a second set of extensions having n-type conductivity.

Another embodiment is an inverter circuit comprising a first semiconductor layer having a first discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; and a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers. The inverter circuit further comprises a first gate dielectric layer disposed above the first semiconductor layer; a first gate metal layer disposed above the first gate dielectric layer and having a first effective workfunction selected to position the first discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the first gate metal layer and to obtain n-terminal characteristics; a second gate dielectric layer disposed above the first semiconductor layer; and a second gate metal layer disposed above the second gate dielectric layer and having a second effective workfunction selected to position the second discrete hole level H_0 below the second conduction band minimum E_{c2} for zero bias applied to the second gate metal layer and to obtain p-terminal characteristics.

Yet another embodiment comprises an n-channel transistor having n-terminal characteristics. The n-channel transistor comprises means for providing a layer having a discrete hole level H_0; means for providing a layer having a conduction band minimum E_{C2}; and means for providing a wide bandgap barrier between the layer having a discrete hole level H_0 and the layer having a conduction band minimum E_{C2}. The n-channel transistor further comprises means for providing a dielectric layer above the layer having a discrete hole level H_0; and means disposed above the dielectric layer for implementing a gate having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

Yet another embodiment is an n-channel transistor having p-terminal characteristics. The n-channel transistor comprises means for providing a layer having a discrete hole level H_0; means for providing a layer having a conduction band minimum E_{C2}; and means for providing a wide bandgap barrier between the layer having a discrete hole level H_0 and the layer having a conduction band minimum E_{C2}. The n-channel transistor further comprises means for providing a dielectric layer above the layer having a discrete hole level

H_0; and means disposed above the dielectric layer for implementing a gate having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain p-terminal characteristics.

Yet another embodiment is an inverter circuit comprising means for implementing a layer having a discrete hole level H_0; means for implementing a layer having a conduction band minimum E_{C2}; and means for implementing a wide bandgap barrier between the layer having a first discrete hole level H_0 and the layer having a conduction band minimum E_{C2}. The inverter circuit further comprises means for implementing a first dielectric layer above the layer having a discrete hole level H_0; means for implementing a first gate above the first dielectric layer having a first effective workfunction selected to position the first discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the first gate and to obtain n-terminal characteristics; means for implementing a second dielectric layer above the layer having a discrete hole level H_0; and means for implementing a second gate above the second gate dielectric layer having a second effective workfunction selected to position the second discrete hole level H_0 below the second conduction band minimum E_{c2} for zero bias applied to the second gate and to obtain p-terminal characteristics.

Still another embodiment is a device including an n-channel transistor comprising a first semiconductor layer having a discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; and a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; the n-channel transistor further comprises a gate dielectric layer disposed above the first semiconductor layer; and a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

Still another embodiment is a device including an n-channel transistor comprising a first semiconductor layer having a discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; and a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers; the n-channel transistor further comprises a gate dielectric layer disposed above the first semiconductor layer; and a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the gate metal layer and to obtain p-terminal characteristics.

Still another embodiment is a device including an inverter circuit comprising a first semiconductor layer having a first discrete hole level H_0; a second semiconductor layer having a conduction band minimum E_{C2}; and a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers. The inverter circuit further comprises a first gate dielectric layer disposed above the first semiconductor layer; a first gate metal layer disposed above the first gate dielectric layer and having a first effective workfunction selected to position the first discrete hole level H_0 below the conduction band minimum E_{c2} for zero bias applied to the first gate metal layer and to obtain n-terminal characteristics; a second gate dielectric layer disposed above the first semiconductor layer; and a second gate metal layer disposed above the second gate dielectric layer and having a second effective workfunction selected to position the second discrete hole level H_0 below the second conduction band minimum E_{c2} for zero bias applied to the second gate metal layer and to obtain p-terminal characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a layer structure used in a uni-terminal transistor in accordance with one embodiment.

FIG. **2** is a more detailed illustration of the layer structure shown in FIG. **1**.

FIG. **3** is a calculated band diagram illustrating the relative energy levels of the layer structure shown in FIG. **2** in thermal equilibrium (bias=0 V).

FIG. **4** is a calculated energy band diagram of the layer structure shown in FIG. **2** under a bias of −0.1 V applied to a gate electrode thereof.

FIG. **5** illustrates the calculated electron sheet carrier density in the InAs layer n_s as a function of gate bias V for the layer structure shown in FIG. **2**.

FIG. **6** illustrates the calculated InAs sheet electron concentration in off-state vs. on-state for different InAs layer thickness for p-terminal operation of the layer structure shown in FIG. **2** with $SR=n_{on}/n_{off}$ as a parameter.

FIG. **7** illustrates a MOSFET fabricated using the layer structure of FIG. **2**.

FIG. **8** illustrates a complementary inverter circuit comprising two uni-terminal devices connected in series fabricated using the layer structure of FIG. **2**.

FIG. **9** illustrates channel electron charge vs. input voltage of the p- and n-terminal devices for the on-state of the inverter circuit of FIG. **8**.

FIG. **10** illustrates channel electron charge vs. input voltage of the p- and n-terminal devices for the off-state of the inverter circuit of FIG. **8**.

DETAILED DESCRIPTION

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Furthermore, the following description shows two or more layers in contact with each other. Such contact can be direct physical contact, or there may be an intervening layer and the contact is indirect, such as through indirect coupling.

The embodiments described herein provide a transistor in which the conducting channel is formed with conduction band electrons for both devices with p- and n-terminal characteristics using a common and simple semiconductor layer structure; that is, a uni-terminal device.

A layer structure used in a uni-terminal transistor according to one embodiment is shown in FIG. **1** and designated by a reference numeral **100**. The layer structure **100** comprises a gate metal layer **102**, a gate dielectric layer **104**, a first semiconductor layer with a valence band maximum **106**, a wide bandgap semiconductor barrier layer **108**, a second semiconductor channel layer with a conduction band minimum **110**, a wide bandgap semiconductor buffer layer **112**, a Fermi level pinning layer **114**, and a substrate **116**. The gate metal layer **102** comprises a metal having an appropriate effective workfunction, as will be described in greater detail below. The material comprising the first semiconductor layer with the valence band maximum **106** is selected such that the valence band maximum E_{v1} is located in the vicinity of the conduction band minimum E_{c2} of the material comprising the second semiconductor layer with the conduction band minimum **110**.

The Fermi level pinning layer **114** pins the Fermi level at the backside of the structure **100** at an appropriate energy position, as will be described in greater detail below. Layers **106-116** are collectively designated by a reference numeral **118**.

FIG. **2** is a more detailed illustration of the layer structure **100**. As shown in FIG. **2**, the wide bandgap barrier and buffer layers **108** and **112** comprise AlAsSb, the first semiconductor layer **106** comprises GaSb, the second semiconductor channel layer **110** comprises InAs. For the selected materials, $E_{V1}=-4.79$ eV and $E_{C2}=-4.9$ eV. The Fermi level pinning layer **114** can comprise a wide bandgap semiconductor layer with a discrete energy level inside its bandgap, an interface of high defectivity, or a Schottky contact with appropriate barrier height.

In one embodiment, the gate dielectric layer **104** may comprise hafnium oxide (HfO_2) having a thickness of approximately 30 nm. In the same or another embodiment, the gate metal layer **102** may comprise one of tantalum nitride (TaN), titanium nitride (TiN), tungsten (W), tantalum (Ta), molybdenum (Mo), and ruthenium (Ru), among others. It will be recognized that regulation of the effective workfunctions of the foregoing metals may be may be accomplished via adjustment of process conditions to achieve the desired effective workfunction for the intended purpose, as described below.

FIG. **3** is a calculated band diagram illustrating the relative energy levels of the uni-terminal device layer structure depicted in FIG. **2** in thermal equilibrium (bias=0 V). The Fermi level E_F is positioned at an absolute energy of −4.72 eV (relative energy 0 eV) using the Fermi level pinning layer **114**. Flatband condition is obtained by selecting a metal with an effective workfunction Φ_m of 4.72 eV, which equals the Fermi level pinning position. In equilibrium and at zero bias, the discrete GaSb energy level H_0 shown with its wavefunction ψ_{Ho} (heavy or light hole level) is positioned below the InAs conduction band minimum E_{c2}. Since the discrete InAs energy level E_0 shown with its wavefunction ψ_{Eo} (electron ground level) is located substantially above E_F, the transistor is off and the electron sheet carrier concentration n_s in the InAs channel layer is low. In the case shown in FIG. **3**, $n_s=7.3\times10^9\ \mathrm{cm}^{-2}$.

FIG. **4** is a calculated energy band diagram of the uni-terminal device layer structure depicted in FIG. **2** under a bias of −0.1 V applied to the gate electrode. The hybrid state E_{hybrid} (shown with its wavefunction ψ_{hybrid}) is formed, which is situated substantially below E_F and gives rise to an electron density $n_{on}=2.9\times10^{12}\ \mathrm{cm}^{-2}$ in the conduction band of the InAs channel layer. Switching is assumed to occur almost instantaneously at the switch voltage V_s when the hybrid state forms under appropriate gate bias. V_s is somewhat above −0.1 V and is set equal to −0.1 V here for purposes of simplicity. Immediately before the hybrid state forms, the layer structure is off with $n_{off}=1.6\times10^9\ \mathrm{cm}^{-2}$ in the InAs channel layer conduction band, resulting in a switching ratio $SR=n_{on}/n_{off}=1.84\times10^3$.

FIG. **5** illustrates the calculated electron sheet carrier density in the InAs channel layer n_s as a function of gate bias V for the uni-terminal device in accordance with the embodiment illustrated in FIG. **2**. As previously described with reference to FIGS. **3-4**, the electron channel in the InAs layer **110** turns on when the gate bias is lowered from 0 V to −0.1 V, resulting in p-terminal characteristics. The gate voltage at threshold (threshold voltage V_t) in p-terminal operation of the device is equal to the switch voltage $V_s=-0.1$ V. The formation of the hybrid state essentially acts as a dramatic electron density booster carrying the device almost immediately to high n_{on}. This is a desirable property for a "millivolt switch," as is the high SR for the uni-terminal layer structure shown in FIG. **2** in p-terminal operation. Switching may also not be as abrupt as indicated because of lateral inhomogeneities in layer thickness, composition, etc. Further, illustrated in FIG. **5**, the layer structure **100** (FIG. **2**) operates in standard n-terminal mode with a positive V_t when the gate bias is increased above 0 V. Consequently, the uni-terminal layer structure **100** (FIG. **2**) can operate with p- and n-terminal characteristics for negative and positive gate voltage, respectively. In both cases, the conducting channel is formed by conduction band electrons in the InAs channel layer **110**.

FIG. **6** illustrates the calculated InAs sheet electron concentration in off-state vs. on-state for different InAs layer thickness for p-terminal operation of the uni-terminal layer structure **100** (FIG. **2**) with $SR=n_{on}/n_{off}$ as a parameter. In particular, a line **600** corresponds to an InAs layer thickness of 1.5 nm ($SR=1.5\times10^6$), a line **602** corresponds to an InAs layer thickness of 2.0 nm ($SR=5.8\times10^4$), and a line **604** corresponds to an InAs layer thickness of 3.0 nm ($SR=1.5\times10^3$). Higher SR can be obtained with smaller InAs layer thickness. The lowest n_{on} shown for all curves is $4.3\times10^{11}\ \mathrm{cm}^{-2}$. SR falls with higher n_{on}. A correct calculation of the hybridized state is expected to lead to n_{on} values (and simultaneously n_{off} values) that are higher by a factor of up to 3 due to higher unified effective mass and nonparabolicity. On the other hand, the resulting electric field may substantially reduce n_{on} values and SR.

FIG. **7** illustrates a MOSFET **700** fabricated using the layer structure according to the embodiments shown in FIGS. **1** and **2**. The n-type extensions **702** can be implemented using standard means such as ion implantation or virtual channels.

FIG. **8** illustrates a complementary inverter circuit **800** comprising two uni-terminal devices **802**, **804**, connected in series. The n-terminal device utilizes a gate metal **806** having an effective workfunction Φ_{m1}, the p-terminal device employs a gate metal **808** having an effective workfunction Φ_{m2}. In one particular embodiment, $V_D=0.2$ V, $\Phi_{m1}=4.52$ eV and $\Phi_{m2}=4.72$ eV.

FIG. **9** illustrates channel electron charge vs. input voltage of the p-terminal device **804** (represented by a line **900**) and the n-terminal device **802** (represented by a line **902**) for the on-state of the inverter circuit **800** (FIG. **8**). The gate-source voltage (S) and gate-drain voltage (D) operating points **904**, **906**, for the p-terminal device, respectively, and gate-source voltage and gate-drain voltage operating point **908** (which is the same for both voltages), for the n-terminal device, respectively, are also shown.

FIG. **10** illustrates channel electron charge vs. input voltage of the p-terminal device **804** (represented by a line **1000**) and the n-terminal device **802** (represented by a line **1002**) for the off-state of the inverter circuit **800** (FIG. **8**). The gate-source voltage and gate-drain voltage operating point **1004** (which is the same for both voltages) for the p-terminal device and gate-source voltage and gate-drain voltage operating points **1008**, **1010**, for the n-terminal device, respectively, are also shown.

It will be noted that the embodiments described and illustrated herein may be advantageously employed in implementing high performance ("HP"), low operating power ("LOP"), and low standby power ("LSTP") devices. Moreover, all of the transistors described herein may be advantageously implemented in any electronic device and/or circuit that employs one or more transistors.

While the preceding shows and describes one or more embodiments, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the present disclosure. For example, various steps of the described methods may be executed in a different order or executed sequentially, combined, further divided, replaced with alternate steps, or removed entirely. In addition, various functions illustrated in the methods or described elsewhere in the disclosure may be combined to provide additional and/or alternate functions. Therefore, the claims should be interpreted in a broad manner, consistent with the present disclosure.

What is claimed is:

1. An n-channel transistor having n-terminal characteristics, the n-channel transistor comprising:

a first semiconductor layer having a discrete hole level H0;

a second semiconductor layer having a lower conduction band EC2 than the first semiconductor layer, wherein the first semiconductor layer has a higher valence band than the second semiconductor layer;

a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers;

a gate dielectric layer disposed above the first semiconductor layer; and

a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H0 below the conduction band EC2 for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

2. The n-channel transistor of claim **1** wherein EC2=−4.9 eV.

3. The n-channel transistor of claim **1** wherein the effective workfunction is 4.52 eV.

4. The n-channel transistor of claim **1** wherein the wide band gap semiconductor barrier layer comprises AlAsSb.

5. The n-channel transistor of claim **1** wherein the wide band gap semiconductor barrier layer has a thickness of approximately 2 nm.

6. The n-channel transistor of claim **1** wherein the first semiconductor layer comprises GaSb and has a thickness of approximately 2 nm.

7. The n-channel transistor of claim **1** wherein the second semiconductor layer comprises InAs and has a thickness of approximately 2 nm.

8. The n-channel transistor of claim **1** further comprising:

a substrate;

a Fermi level pinning layer disposed on the substrate;

extensions having n-type conductivity; and

a wide bandgap buffer layer disposed between the second semiconductor layer and the Fermi level pinning layer.

9. The n-channel transistor of claim **8** wherein the wide bandgap buffer layer comprises AlAsSb.

10. The n-channel transistor of claim **8** wherein a thickness of the wide bandgap buffer layer is approximately 20 nm.

11. The n-channel transistor of claim **8** wherein the Fermi level pinning layer comprises a wide bandgap semiconductor layer with a discrete energy level inside its bandgap.

12. The n-channel transistor of claim **8** wherein the Fermi level pinning layer comprises an interface of high defectivity.

13. The n-channel transistor of claim **8** wherein the Fermi level pinning layer comprises a Schottky contact having an appropriate barrier height.

14. The n-channel transistor of claim **1** wherein the gate metal layer comprises a metal selected from a group consisting of TaN, TiN, W, Ta, Mo, and Ru.

15. The n-channel transistor of claim **1** wherein the gate dielectric layer comprises HfO2.

16. The n-channel transistor of claim **1** wherein an electron density in the second semiconductor layer increases abruptly in response to a negative bias applied to the gate metal layer.

17. An n-channel transistor having n-terminal characteristics, the n-channel transistor comprising:

a first layer having a discrete hole level H0, the first layer having a higher valence band than each remaining semiconductor layer of the n-channel transistor;

a second layer having a conduction band EC2, the conduction band being lower than each remaining semiconductor layer of the n-channel transistor;

a wide bandgap barrier between the first layer and the second layer;

a dielectric layer above the first layer; and

a gate disposed above the dielectric layer, the gate having an effective workfunction selected to position the discrete hole level H0 below the conduction band EC2 for zero bias applied to the gate and to obtain n-terminal characteristics.

18. The n-channel transistor of claim **17** wherein EC2=−4.9 eV.

19. The n-channel transistor of claim **17** wherein the effective workfunction is 4.52 eV.

20. The n-channel transistor of claim **17** wherein the wide band gap barrier comprises AlAsSb having a thickness of approximately 2 nm.

21. The n-channel transistor of claim **17** wherein the first layer comprises GaSb and has a thickness of approximately 2 nm.

22. The n-channel transistor of claim **17** wherein the second layer comprises InAs and has a thickness of approximately 2 nm.

23. The n-channel transistor of claim **17** further comprising:

a substrate;

means for achieving Fermi level pinning disposed on the substrate; and

means for providing a wide bandgap buffer between the second layer and the means for achieving Fermi level pinning.

24. The n-channel transistor of claim **23** wherein the means for providing a wide bandgap buffer comprises AlAsSb having a thickness of approximately 20 nm.

25. The n-channel transistor of claim **23** wherein the means for achieving Fermi level pinning comprises one of a wide bandgap semiconductor layer with a discrete energy level inside its bandgap, an interface of high defectivity, and a Schottky contact having an appropriate barrier height.

26. The n-channel transistor of claim **17** wherein the gate comprises a material selected from a group consisting of TaN, TiN, W, Ta, Mo, and Ru.

27. The n-channel transistor of claim **17** wherein the dielectric layer comprises HfO2.

28. The n-channel transistor of claim **17** wherein an electron density in the second layer increases abruptly in response to a negative bias applied to the gate.

29. A device including an n-channel transistor comprising:

a first semiconductor layer having a discrete hole level H0, the first semiconductor layer having a higher valence band than each remaining semiconductor layer of the n-channel transistor;

a second semiconductor layer having a conduction band EC2 that is lower than conduction bands of each remaining semiconductor layer within the n-channel transistor;

a wide bandgap semiconductor barrier layer disposed between the first and the second semiconductor layers;

a gate dielectric layer disposed above the first semiconductor layer; and

a gate metal layer disposed above the gate dielectric layer and having an effective workfunction selected to position the discrete hole level H0 below the conduction band EC2 for zero bias applied to the gate metal layer and to obtain n-terminal characteristics.

30. The device of claim **29** wherein EC2=−4.9 eV.

31. The device of claim **29** wherein the effective workfunction is 4.52 eV.

32. The device of claim **29** wherein the wide band gap semiconductor barrier layer comprises AlAsSb having a thickness of approximately 2 nm.

33. The device of claim **29** wherein the first semiconductor layer comprises GaSb and has a thickness of approximately 2 nm.

34. The device of claim **29** wherein the second semiconductor layer comprises InAs and has a thickness of approximately 2 nm.

35. The device of claim **29** further comprising:

a substrate;

a Fermi level pinning layer disposed on the substrate;

extensions having n-type conductivity; and

a wide bandgap buffer layer disposed between the second semiconductor layer and the Fermi level pinning layer.

36. The device of claim **35** wherein the wide bandgap semiconductor buffer layer comprises AlAsSb having a thickness of approximately 20 nm.

37. The device of claim **35** wherein the Fermi level pinning layer comprises one of a wide bandgap semiconductor layer with a discrete energy level inside its bandgap, an interface of high defectivity, and a Schottky contact having an appropriate barrier height.

38. The device of claim **29** wherein the gate metal layer comprises a metal selected from a group consisting of TaN, TiN, W, Ta, Mo, and Ru.

39. The device of claim **29** wherein the gate dielectric layer comprises HfO2.

40. The device of claim **29** wherein an electron density in the second semiconductor layer increases abruptly in response to a negative bias applied to the gate metal layer.

41. The device of claim **29** wherein the device is at least one of a low operating power ("LOP") device, a high performance ("HP") device, and a low standby power ("LSTP") device.

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