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(54) **MICROFEATURE WORKPIECES HAVING INTERCONNECTS AND CONDUCTIVE BACKPLANES, AND ASSOCIATED SYSTEMS AND METHODS**

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See application file for complete search history.

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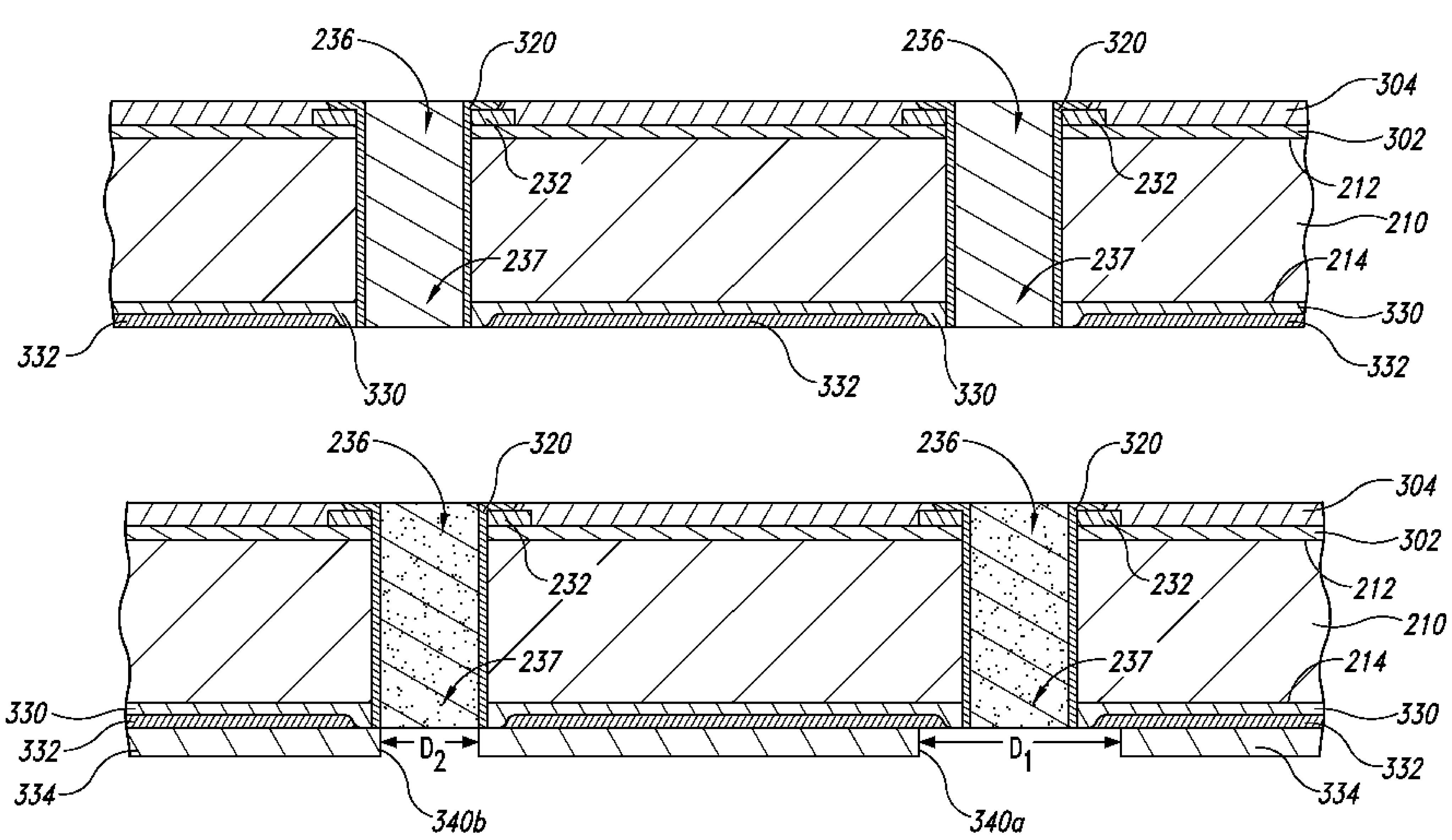
(57) **ABSTRACT**

Microfeature workpieces having interconnects and conductive backplanes and associated systems and methods are disclosed herein. One such device includes a semiconductor substrate having integrated circuitry and terminals electrically coupled to the integrated circuitry. The device also includes electrically conductive interconnects extending through at least a portion of the semiconductor substrate and electrically coupled to corresponding terminals. The device further includes a conductive backplane assembly having a conductive layer at a back side of the semiconductor substrate. One or more of the interconnects are electrically coupled to the conductive layer at the back side of the semiconductor substrate.

11 Claims, 10 Drawing Sheets



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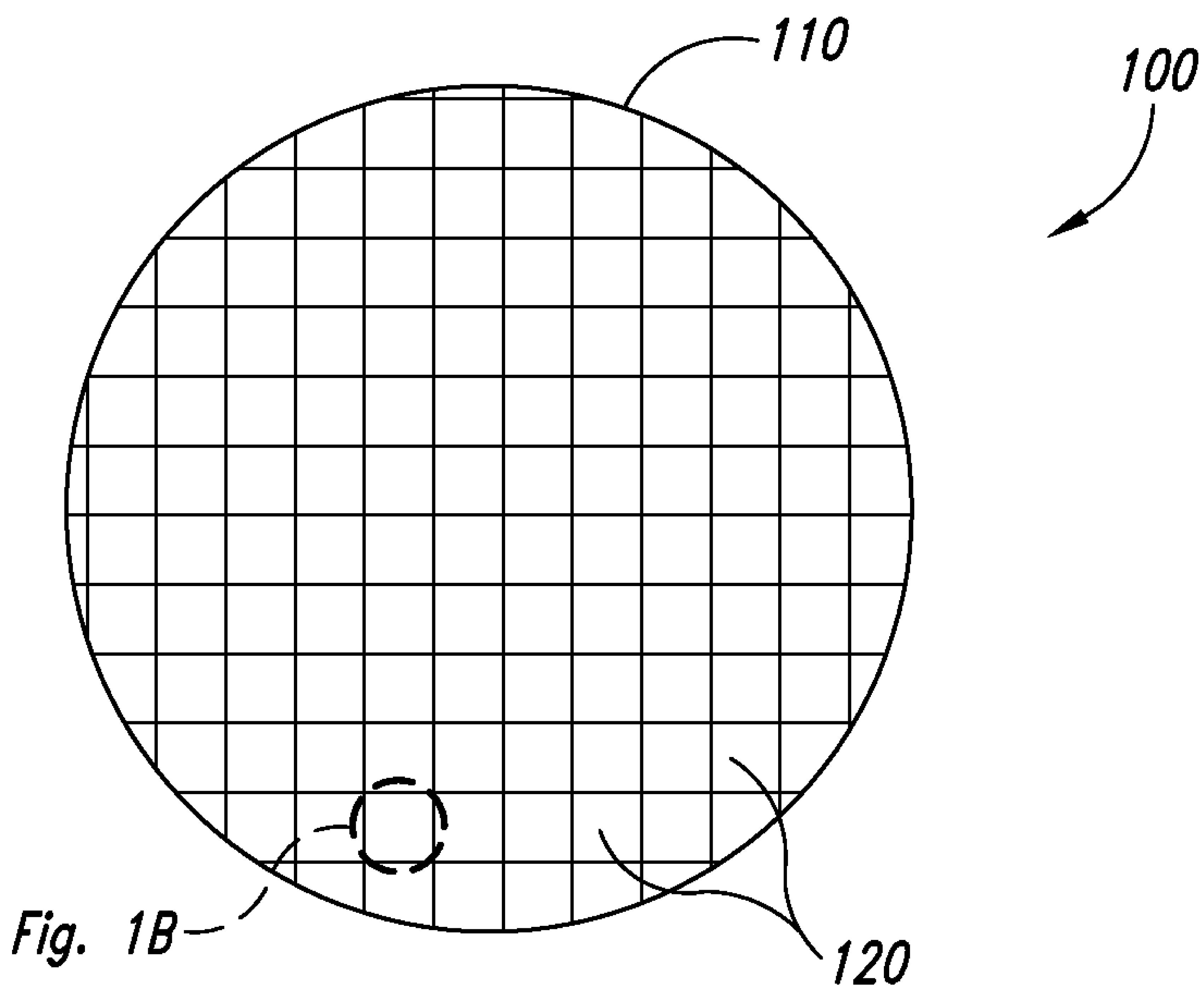

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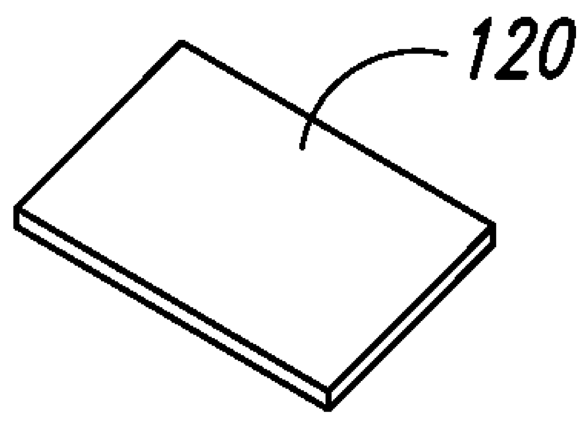

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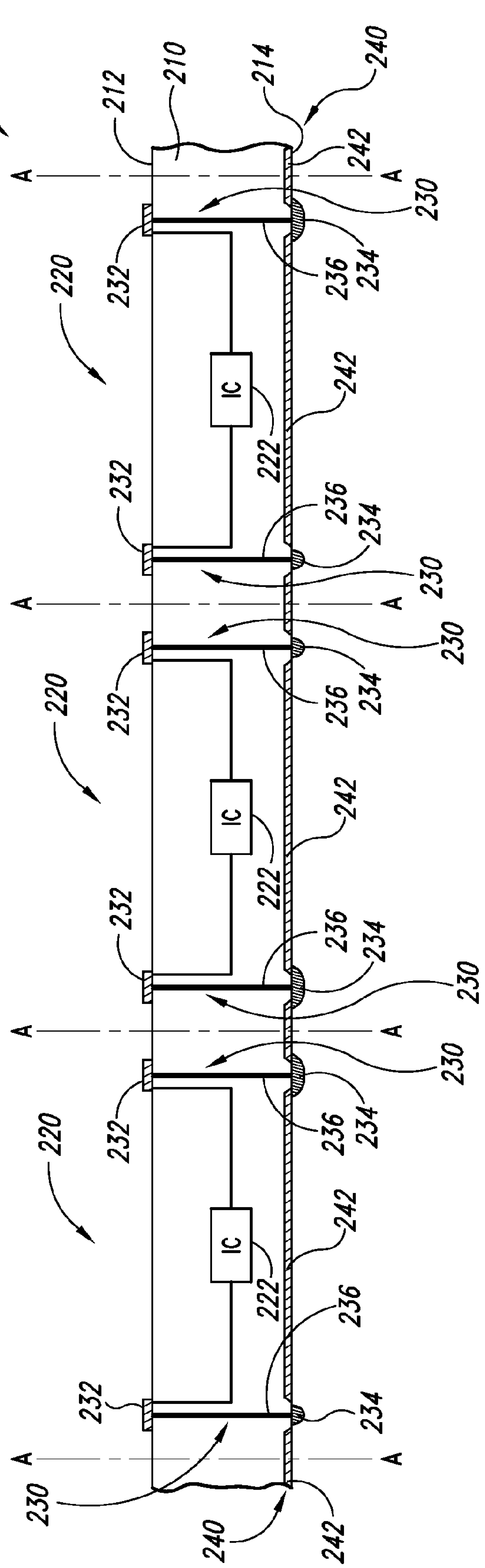

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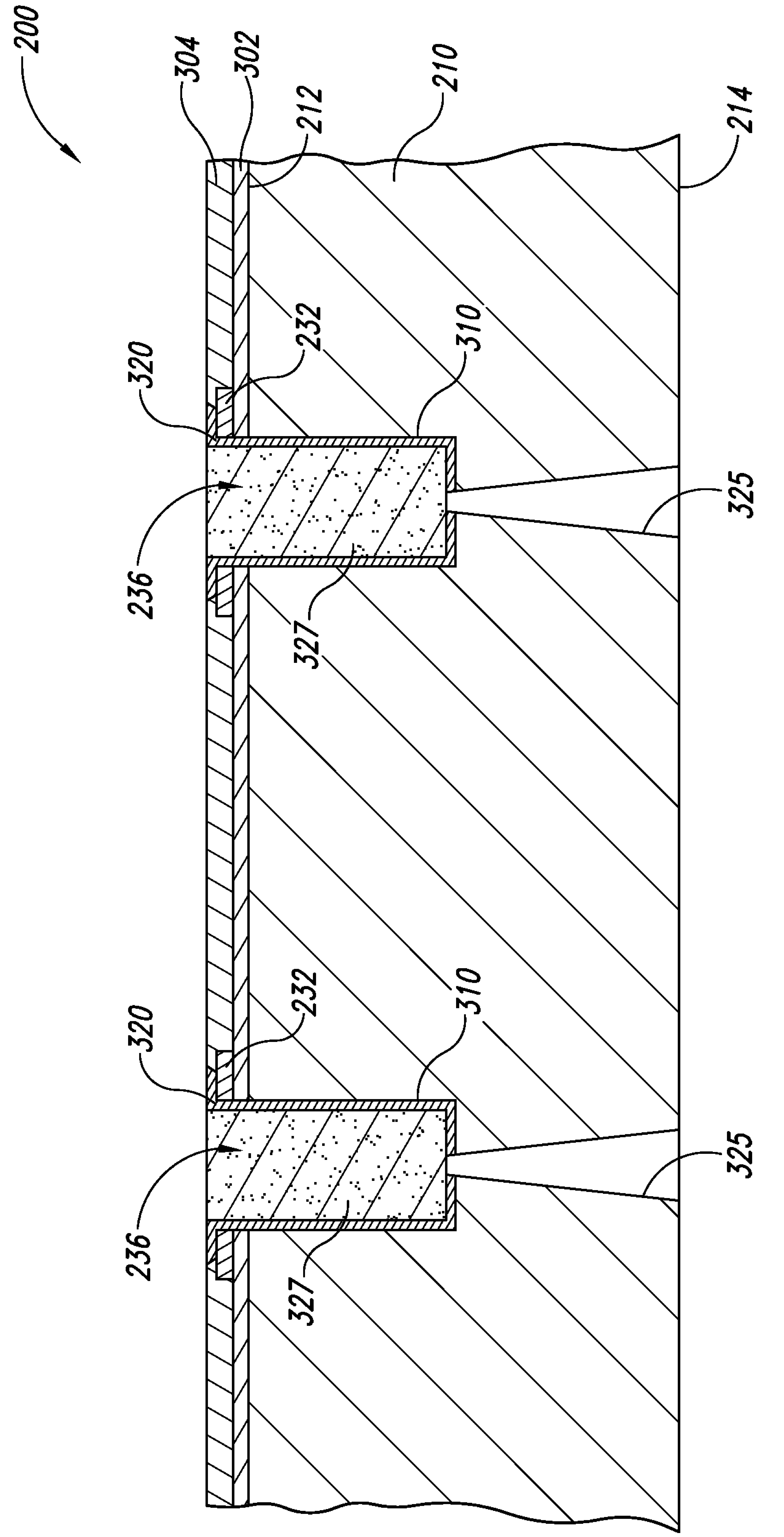
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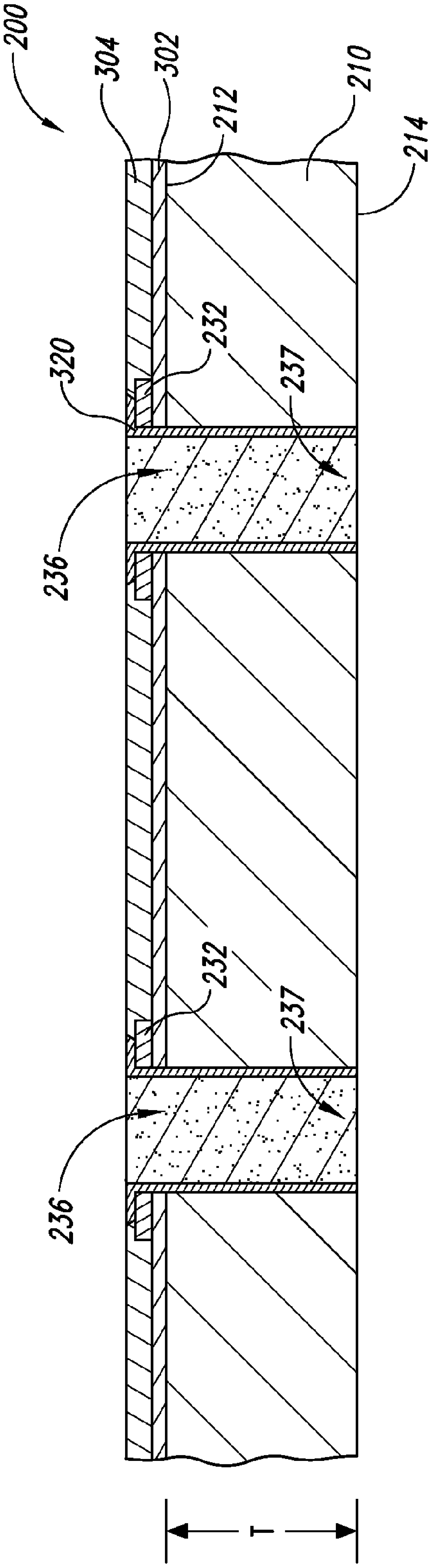
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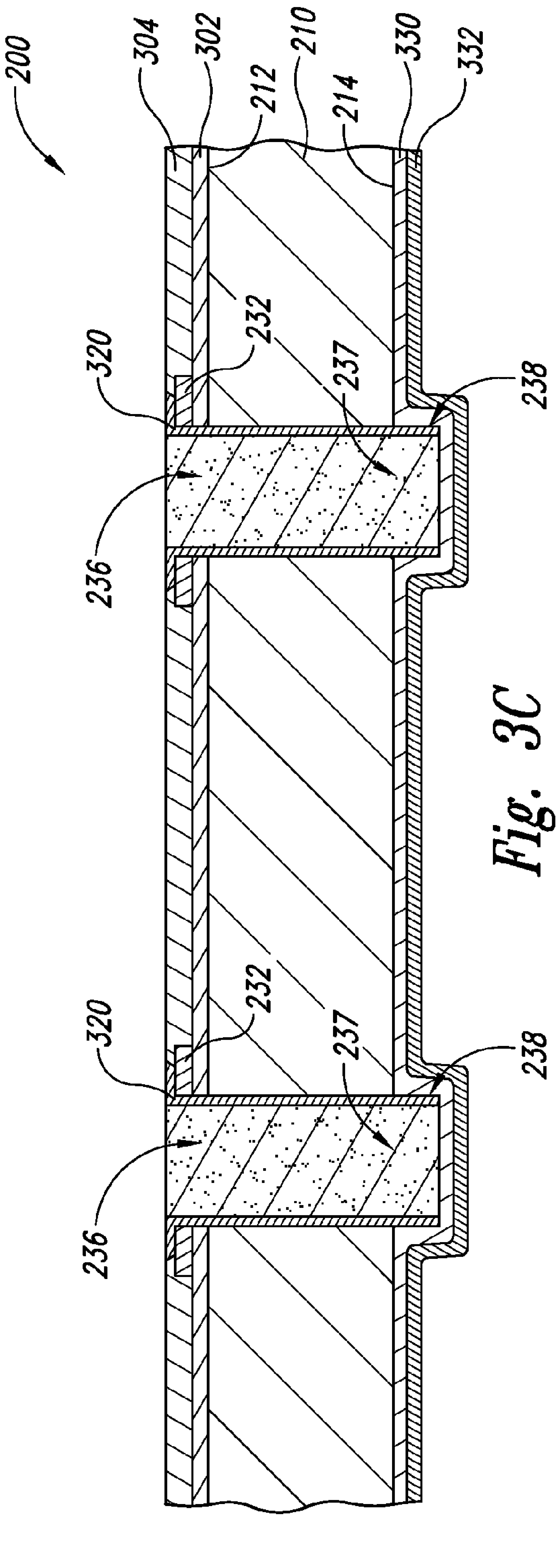
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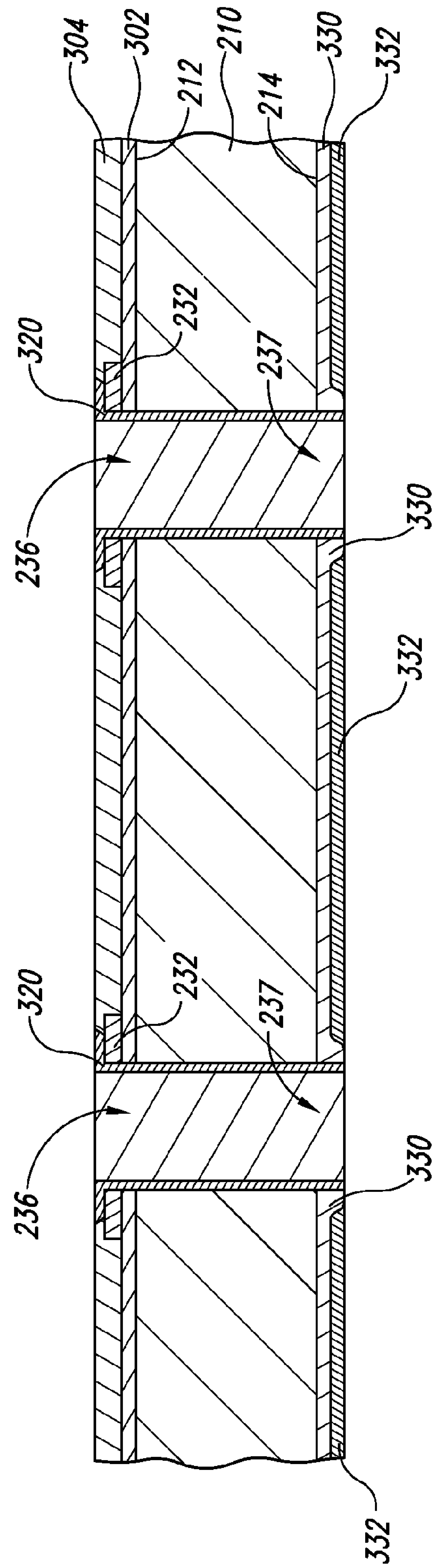
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Fig. 3D

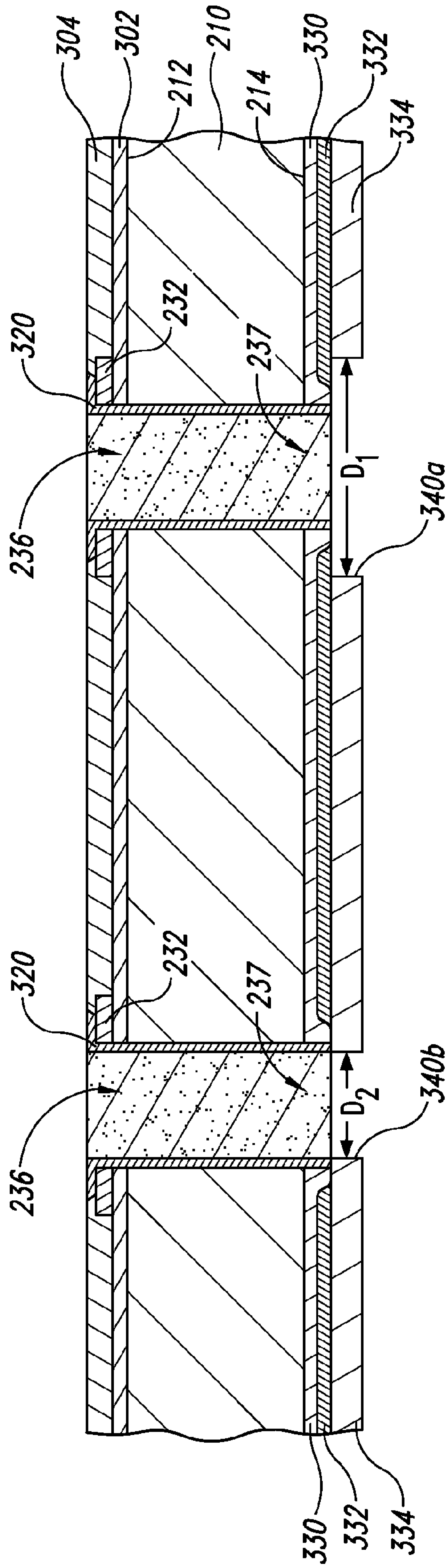
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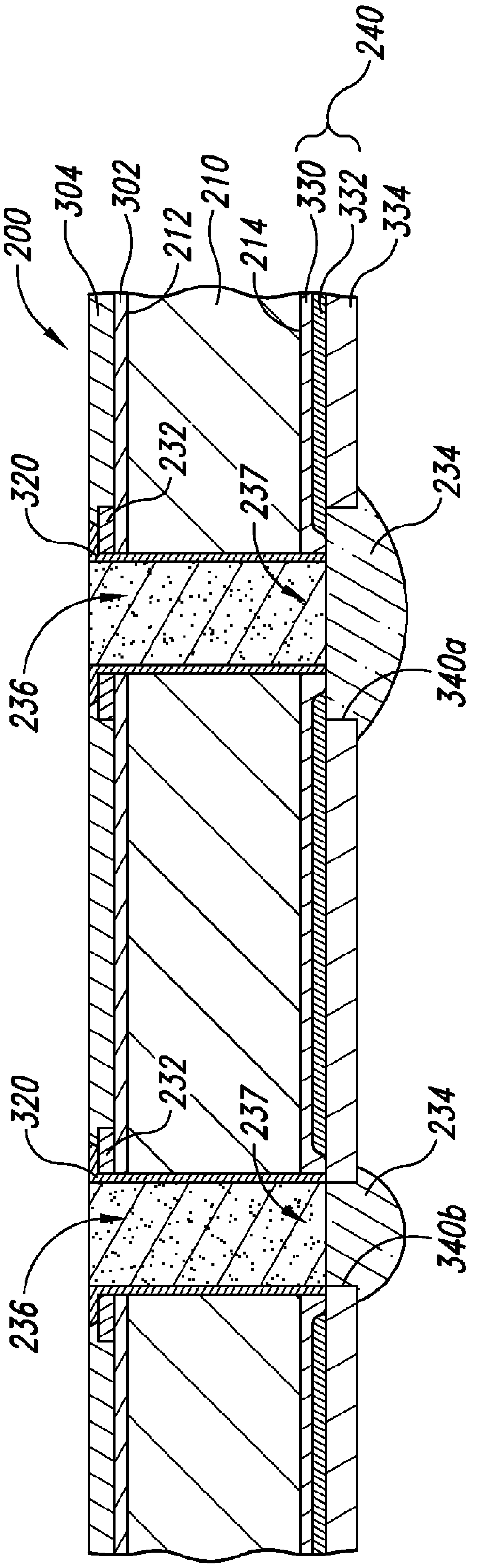
Fig. 3E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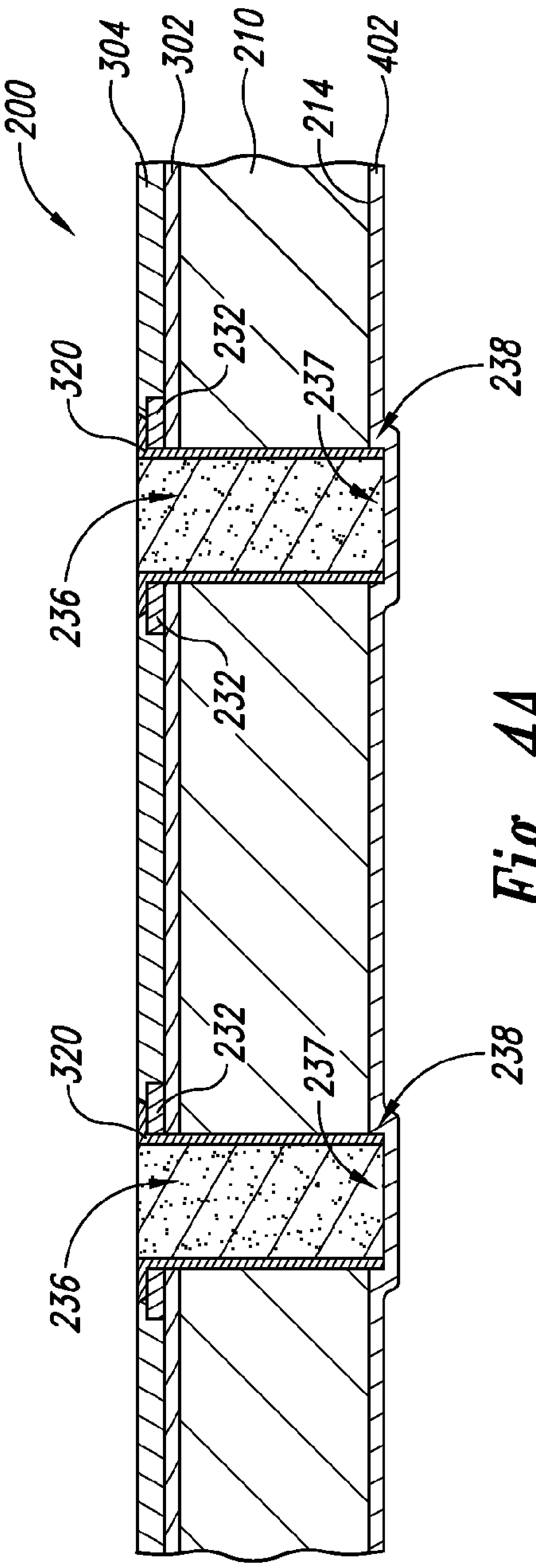
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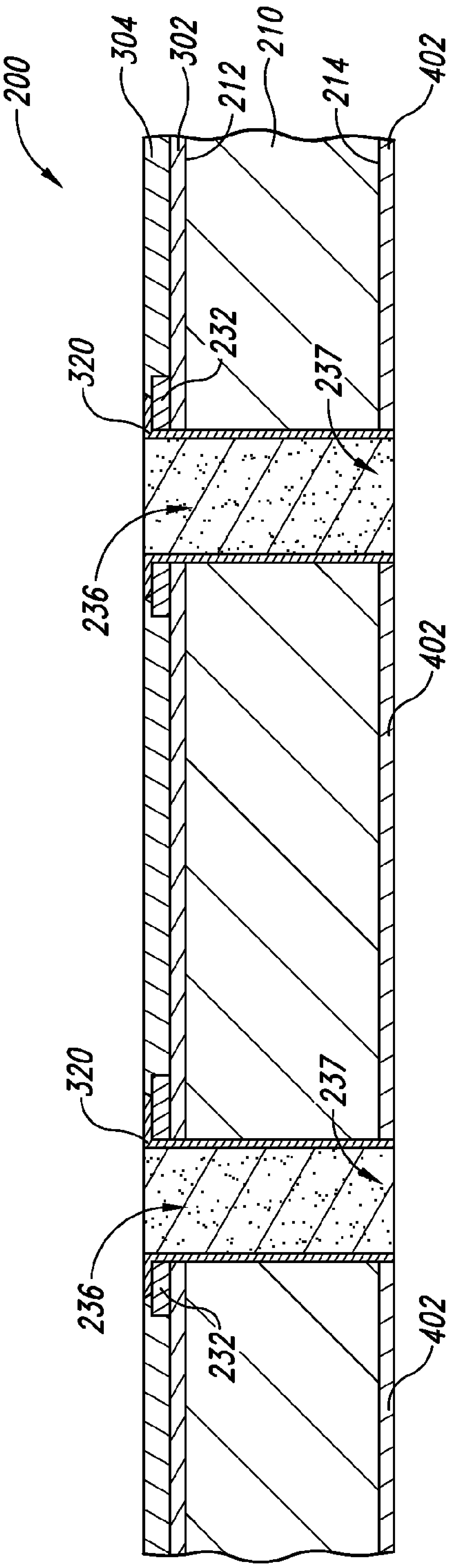
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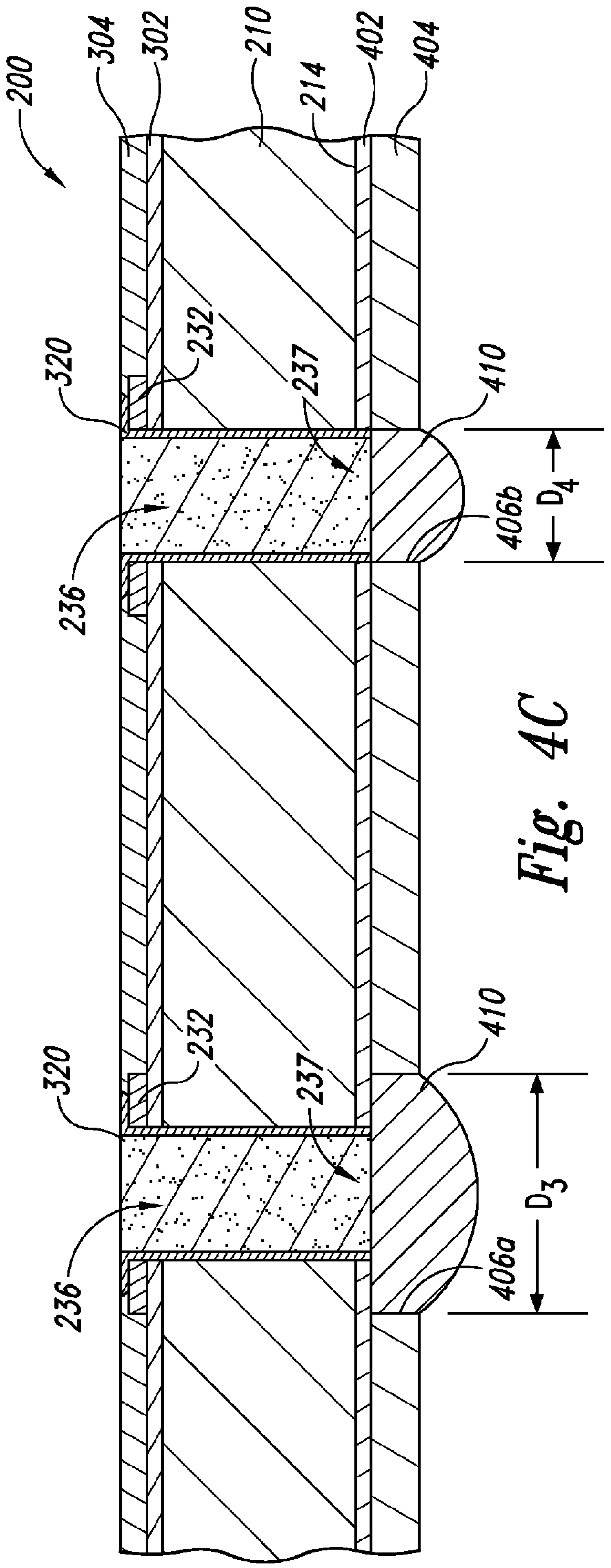
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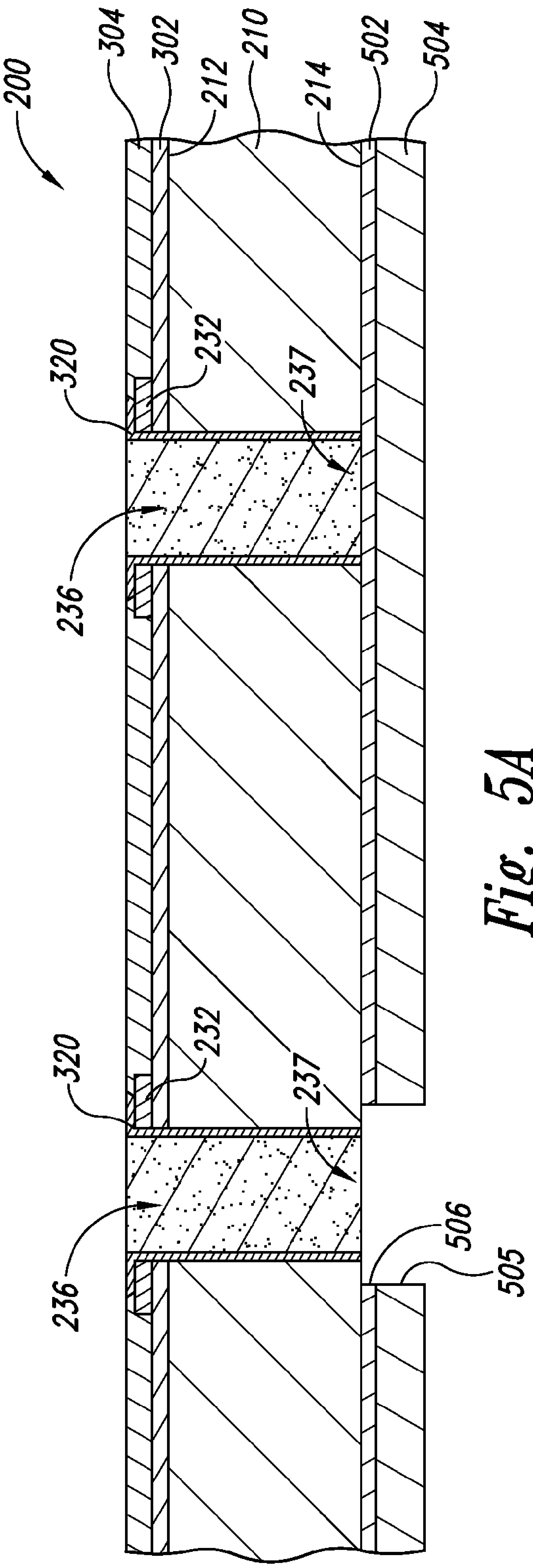
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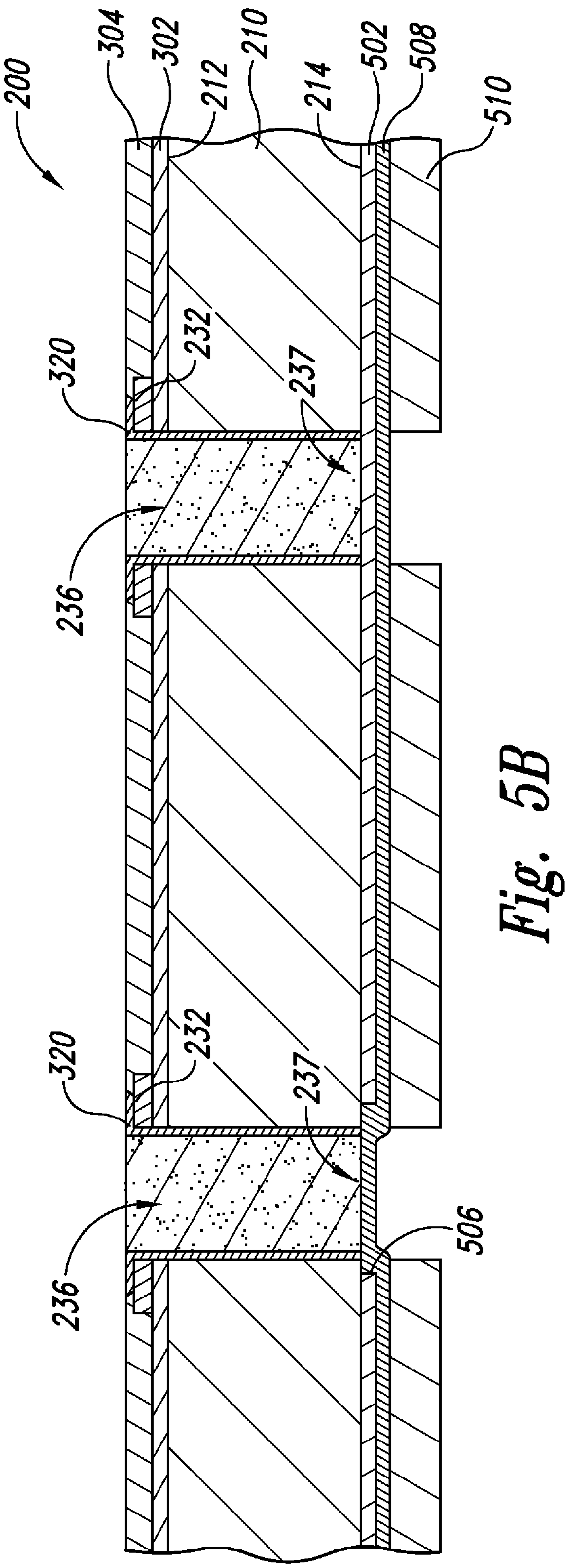
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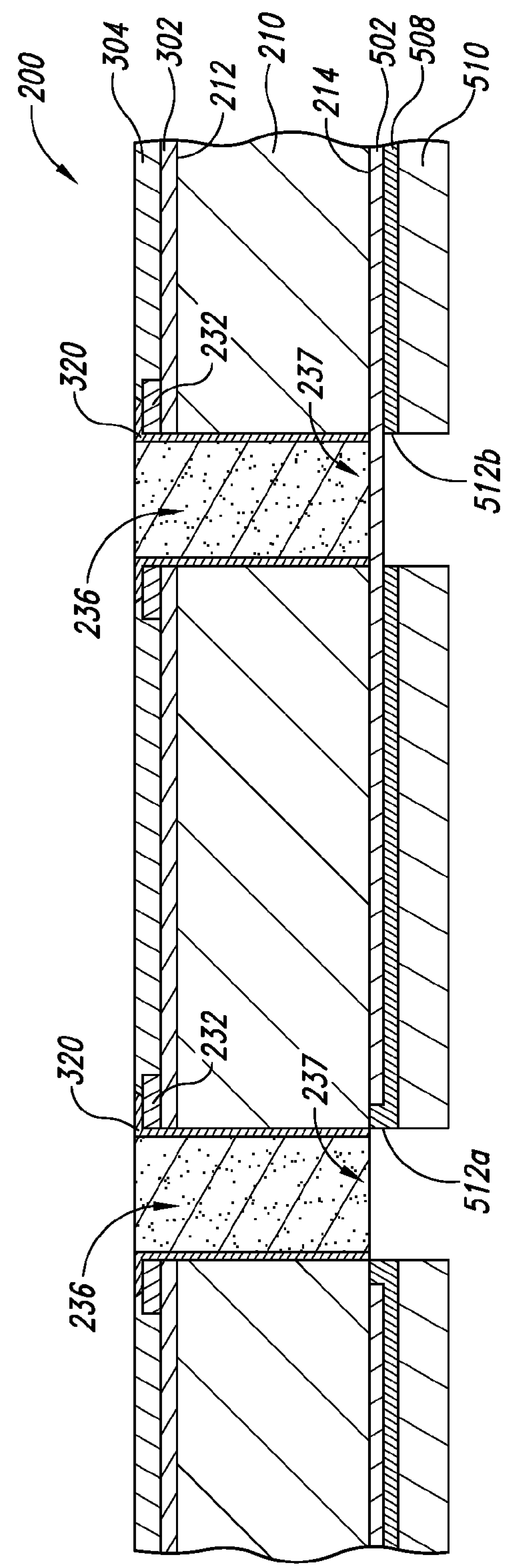
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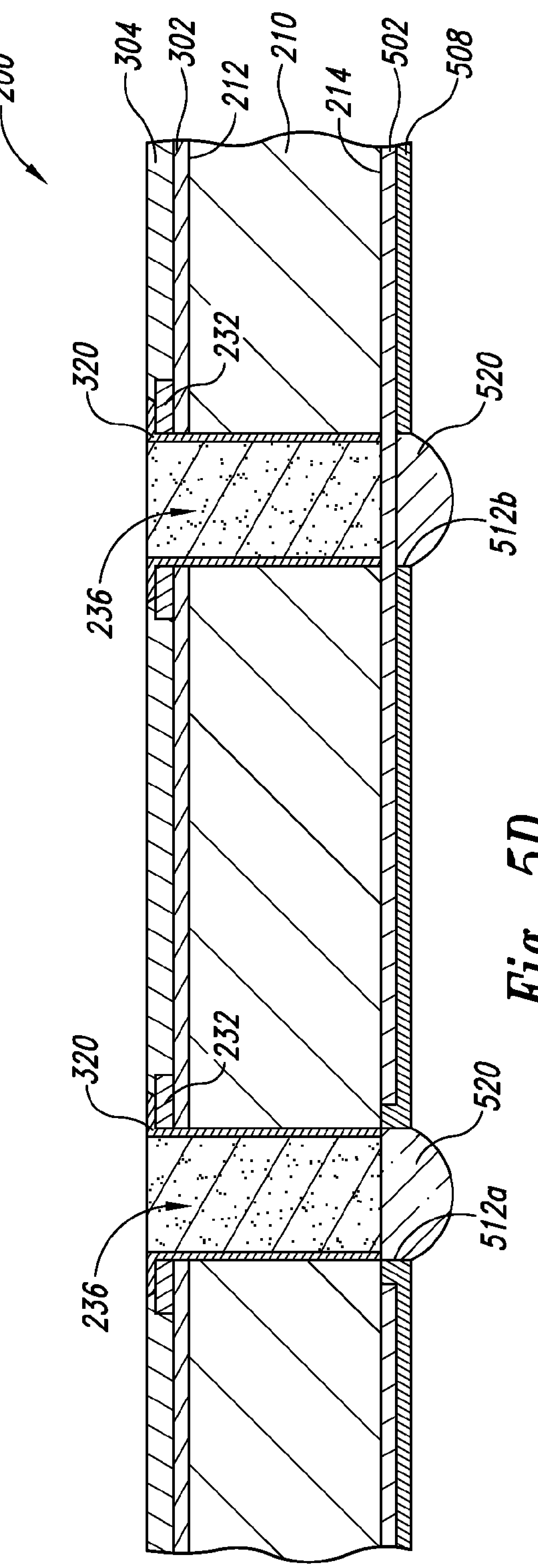
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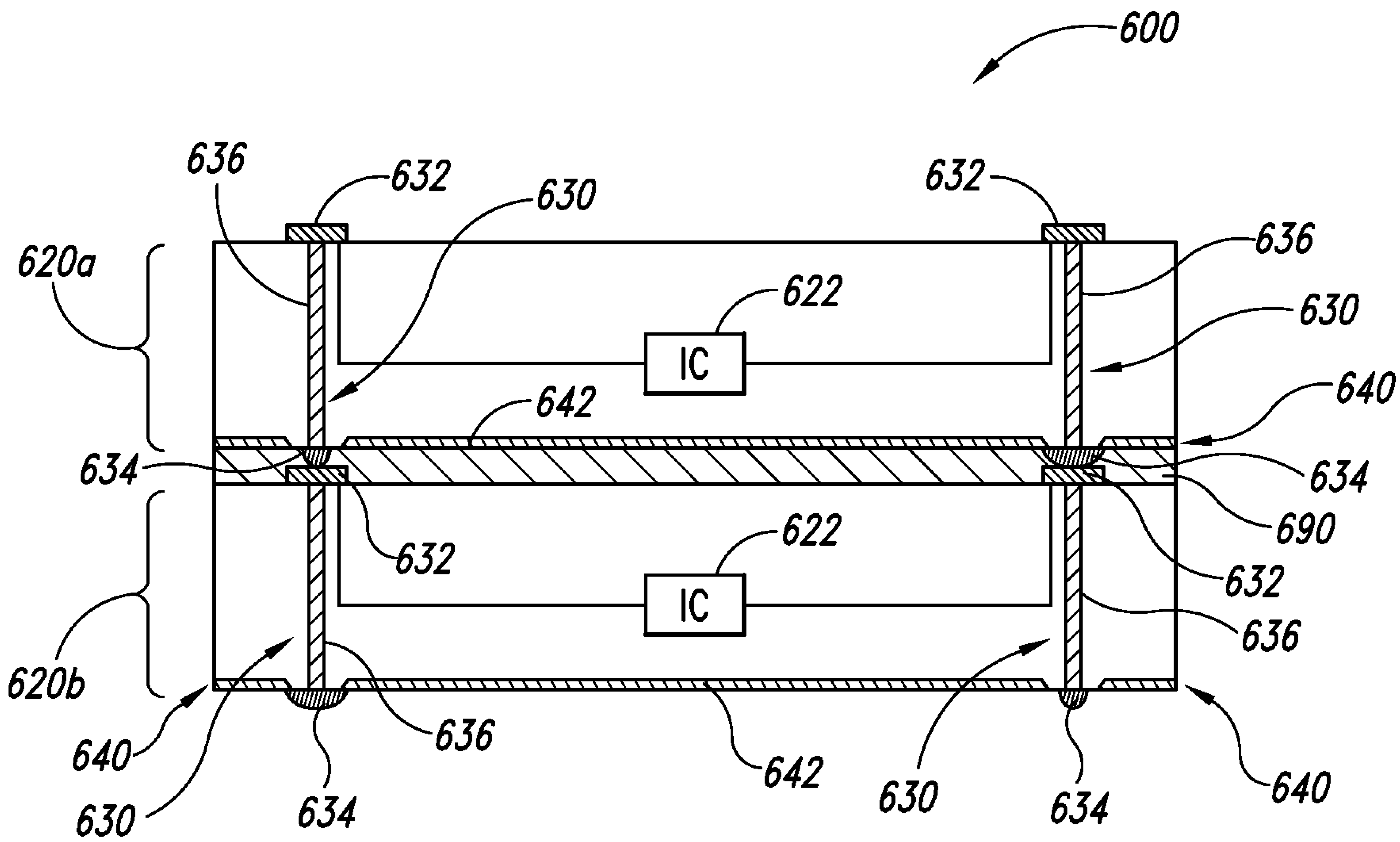
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Fig. 6

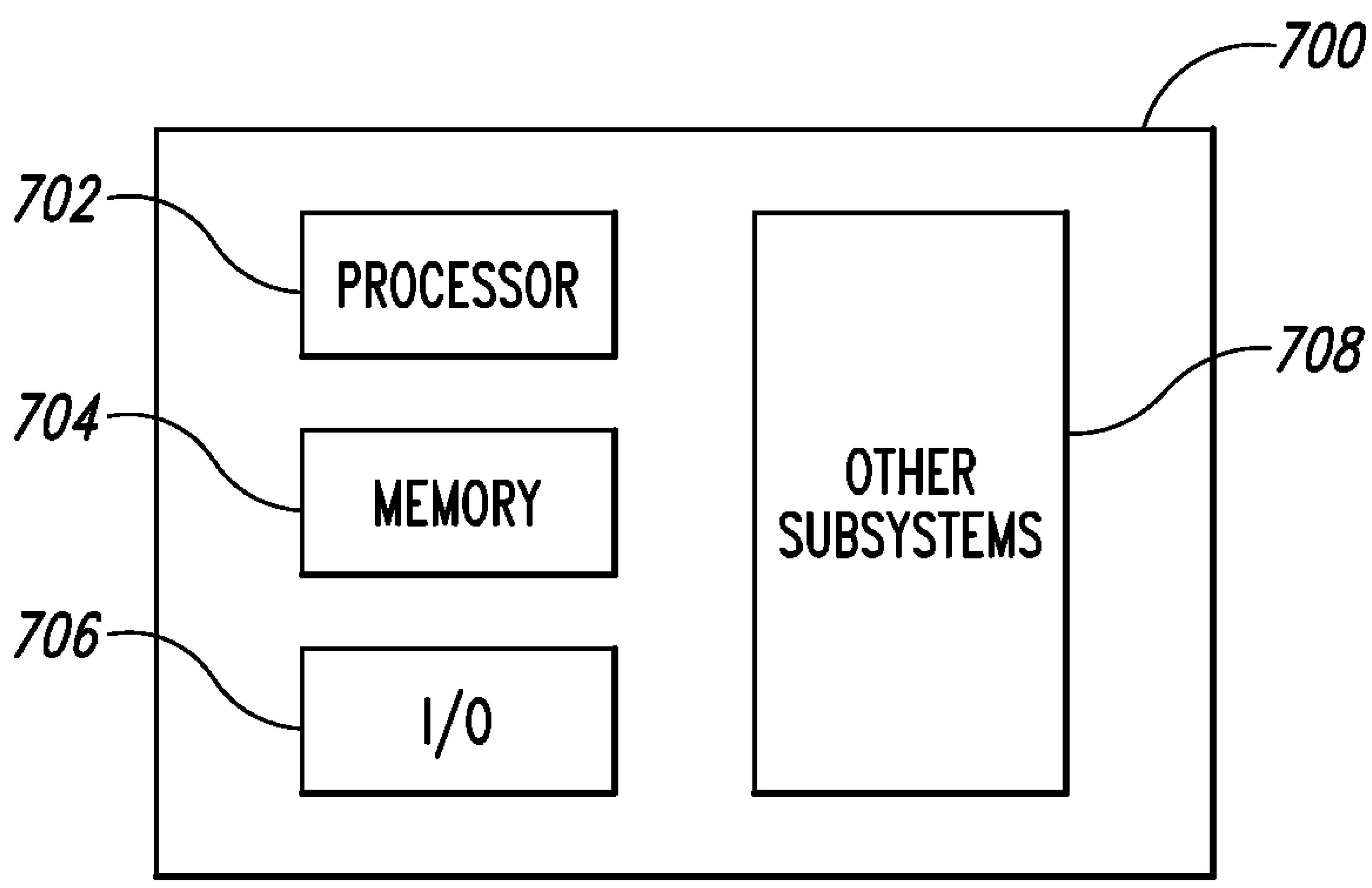
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Fig. 7

MICROFEATURE WORKPIECES HAVING INTERCONNECTS AND CONDUCTIVE BACKPLANES, AND ASSOCIATED SYSTEMS AND METHODS

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of U.S. application Ser. No. 11/514,568 filed Aug. 31, 2006, now U.S. Pat. No. 7,902,643, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

The present disclosure is directed generally toward microfeature workpieces having interconnects and conductive backplanes, and associated systems and methods.

BACKGROUND

Processors, memory devices, imagers and other types of microelectronic devices are often manufactured on semiconductor workpieces or other types of workpieces. In a typical application, several individual dies (e.g., devices) are fabricated on a single workpiece using sophisticated and expensive equipment and processes. Individual dies generally include an integrated circuit and a plurality of bond-pads coupled to the integrated circuit. The bond-pads provide external electrical contacts on the die through which supply voltage, signals, etc., are transmitted to and from the integrated circuit. The bond-pads are usually very small, and they are arranged in an array having a fine pitch between bond-pads. The dies can also be quite delicate. As a result, after fabrication, the dies are packaged to protect the dies and to connect the bond-pads to another array of larger terminals that is easier to connect to a printed circuit board. The dies can be packaged after cutting the workpiece to separate the dies (die-level packaging), or the dies can be packaged before cutting the workpiece (wafer-level packaging).

Conventional die-level packaged microelectronic devices include a microelectronic die, an interposer substrate or lead frame attached to the die, and a molded casing around the die. The bond-pads of the die are typically coupled to terminals on the interposer substrate or the lead frame. In addition to the terminals, the interposer substrate also includes ball-pads coupled to the terminals by conductive traces supported in a dielectric material. Solder balls can be attached to the ball-pads in one-to-one correspondence to form a "ball-grid array." Packaged microelectronic devices with ball-grid arrays are generally higher-grade packages having lower profiles and higher pin counts than conventional packages using lead frames.

Packaged microelectronic devices such as those described above are used in cellphones, pagers, personal digital assistants, computers, and many other electronic products. To meet the demand for smaller electronic products, there is a continuing drive to increase the performance of packaged microelectronic devices, while at the same time reducing the height and the surface area or "footprint" of such devices on printed circuit boards. Reducing the size of high performance devices, however, is difficult because the sophisticated integrated circuitry requires more bond-pads, which results in larger ball-grid arrays and thus larger footprints. One technique for increasing the component density of microelectronic devices within a given footprint is to stack one device on top of another.

One concern with many high-density packaged microelectronic devices is electromagnetic emissions or radiation generated by the devices during operation. Such electromagnetic disturbances are often referred to as electromagnetic interference ("EMI"). EMI within a particular system or device generally occurs as a result of the generation and/or transmission of electromagnetic radiation by integrated circuits, power supplies, or other radiation sources. Left unchecked, EMI can produce a number of undesirable effects. For example, EMI can interfere with or impair the operation and integrity of unshielded equipment and/or systems proximate to the source of the emissions. Furthermore, EMI can significantly degrade or otherwise negatively affect the performance of unshielded devices.

One approach to addressing the problems with EMI is to shield or ground the integrated circuitry within packaged microelectronic devices. A conventional method for shielding lead frame devices, for example, includes forming a conductive backplane on a back side of the wafer. Portions of the lead frame can then be electrically coupled to the backplane, and one or more bond-pads can be electrically coupled to the backplane via the corresponding portions of the lead frame to ground the device. One significant drawback with this approach, however, is that it is not suitable for devices with small arrays of back side contacts (e.g., ball-grid arrays) because (a) many of the ball-pads or back side contacts should not be grounded or otherwise connected in common, and (b) the remaining ball-pads or back side contacts cannot be connected to the backplane using wire-bonding or other conventional techniques. Accordingly, there is a need to provide the methods for packaging microelectronic devices having small arrays of back side contacts and conductive backplanes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a partially schematic illustration of a representative microfeature workpiece carrying microfeature dies configured in accordance with embodiments of the invention.

FIG. **1**B is a schematic illustration of a microfeature die singulated from the workpiece shown in FIG. **1**A.

FIG. **2** is a partially schematic, side cross-sectional view of a portion of a microfeature workpiece including one or more interconnects coupled to a conductive backplane structure in accordance with several embodiments of the invention.

FIGS. **3**A-**3**F are schematic, side cross-sectional views illustrating various stages in a method for forming a conductive backplane in accordance with an embodiment of the invention.

FIGS. **4**A-**4**C are schematic, side cross-sectional views illustrating various stages in a method for forming a conductive backplane in accordance with another embodiment of the invention.

FIGS. **5**A-**5**D are schematic, side cross-sectional views illustrating various stages in a method for forming a conductive backplane in accordance with still another embodiment of the invention.

FIG. **6** is a schematic, side cross-sectional view of a packaged microelectronic device in accordance with one embodiment of the invention.

FIG. **7** is a schematic illustration of a system that can include one or more microelectronic devices configured in accordance with embodiments of the invention.

DETAILED DESCRIPTION

The following disclosure describes several embodiments of methods for forming conductive backplanes on microfeature workpieces having interconnects, and devices formed using such methods. As used herein, the terms "microfeature workpiece" and "workpiece" refer to substrates on and/or in which microfeature electronic devices are integrally formed. A microfeature workpiece can include a wafer and/or individual dies or combinations of dies that make up the wafer. Typical electronic devices formed on and/or in microfeature workpieces include processors, memory, imagers, thin-film recording heads, data storage elements, and other products with integrated circuits. Micromachines, microfluidic devices and other micromechanical devices are included within this definition because they are manufactured using much of the same technology that is used in the fabrication of integrated circuits. The substrates can be semi-conductive pieces (e.g., doped silicon wafers, gallium arsenide wafers, or other semiconductor wafers), non-conductive pieces (e.g., various ceramic substrates), or conductive pieces. In some cases, the workpieces are generally round, and in other cases the workpieces can have other shapes, including rectilinear shapes. Several embodiments of methods for forming conductive backplanes in connection with microfeature workpiece fabrication are described below. A person skilled in the relevant art will understand, however, that the invention has additional embodiments, and that the invention may be practiced without several of the details of the embodiments described below with reference to FIGS. **1A-7**.

FIG. **1A** is a microfeature workpiece **100** in the form of a semiconductor wafer **110** that includes multiple microfeature dies **120**. At least some of the processes described below may be conducted on the microfeature workpiece **100** at the wafer level, and other processes may be conducted on the individual microfeature dies **120** of the microfeature workpiece **100** after the dies **120** have been singulated from the larger wafer **110**. Accordingly, unless otherwise noted, structures and methods described below in the context of a microfeature workpiece can apply to the wafer **110**, the dies **120** that are formed from the wafer **110**, and/or an assembly of one or more dies **120** in a stacked-die configuration or attached to a support member. FIG. **1B** is a schematic illustration of an individual die **120** after it has been singulated from the wafer **110** shown in FIG. **1A**. The die **120** can include operable microelectronic structures, optionally encased within a protective encapsulant. The die **120** can be electrically connected to external structural devices by pins, bond pads, solder balls, redistribution structures, and/or other conductive structures.

FIG. **2** is a partially schematic, side cross-sectional view of a portion of a microfeature workpiece **200** configured in accordance with several embodiments of the invention. More specifically, FIG. **2** illustrates the workpiece **200** after a plurality of interconnects have been formed in the workpiece **200** and one or more of the interconnects have been selectively coupled to a conductive backplane structure **240** to provide EMI shielding and/or grounding for the various components of the workpiece **200**. The microfeature workpiece **200** includes a semiconductor substrate **210** having a front or active side **212**, a back side **214**, and a plurality of microelectronic dies **220** formed on and/or in the substrate **210**. The workpiece **200** can include several features generally similar to the workpiece **100** described above with reference to FIG. **1A**. The substrate **210**, for example, can be a semiconductor wafer with the dies **220** arranged in a die pattern on the wafer. Individual dies **220** can include integrated circuitry **222** and electrical connectors **230** electrically coupled to the integrated circuitry **222**. Although the illustrated dies **220** have the same structure, in other embodiments the dies **220** can have different features to perform different functions.

The connectors **230** shown in FIG. **2** provide a small array of back side contacts within the footprint of each die **220**. Individual connectors **230**, for example, can include a terminal or bond site **232** (e.g., a bond-pad), a conductive coupler **234** (e.g., a solder ball or other external interconnect structure), and an interconnect **236** coupling the terminal **232** to the conductive coupler **234**. In the embodiment illustrated in FIG. **2**, the terminals **232** are at the front side **212** of the substrate **210**, the conductive couplers **234** are at the back side **214** of the substrate **210**, and the interconnects **236** are through-substrate or through-wafer interconnects that extend completely through the substrate **210** to couple the terminals **232** to corresponding conductive couplers **234**. In other embodiments, however, the terminals **232** can be internal features that are embedded at an intermediate depth within the substrate **210** and coupled to corresponding conductive couplers **234** with interconnects **236** that extend through only a portion of the substrate **210**. The conductive couplers **234** can be attached either before or after singulating the dies **220** from the workpiece **200**.

The workpiece **200** further includes the backplane structure **240** at the back side **214** of the substrate **210**. The backplane structure **240** can include, for example, a metal or conductive "shield" layer **242** on and/or in the substrate **210**. In several embodiments, the backplane structure **240** can also include one or more dielectric layers (not shown) and/or other structures. Various embodiments of the backplane structure **240** are described in detail below. As mentioned previously, one or more of the interconnects **236** can be selectively coupled to the backplane structure **240** to provide EMI shielding and/or grounding. More specifically, the backplane structure **240** can be configured such that (a) the individual conductive couplers **234** contact both the corresponding interconnect **236** and the portion of the conductive layer **242** adjacent to the associated interconnect **236** to electrically connect the interconnect to the backplane structure **240**, or (b) the individual conductive couplers **234** contact only the corresponding interconnect **236** and remain electrically isolated from the conductive layer **242**. After coupling selected interconnects **236** to the backplane structure **240**, the workpiece **200** can be cut along lines A-A to singulate the dies **220**. Various embodiments of the backplane structure **240** and processes for selectively coupling one or more of the interconnects **236** to the backplane structure **240** are discussed in greater detail below.

In contrast with conventional unshielded BGA devices described previously, several embodiments of the interconnects **236** and the backplane structure **240** enable devices having small arrays of back side contacts (e.g., ball-grid arrays) to use conductive backplanes. Electrically coupling one or more of the interconnects **236** to the backplane **240** can accordingly provide EMI shielding and grounding for such devices. The back side arrays of electrical connectors also allow the dies **220** to be stacked on other dies or directly attached to an interposer substrate without peripheral wire-bonds. The individual dies **220** accordingly have a significantly smaller footprint and profile than conventional stacked devices including wire-bonds or other conventional devices with backplanes. Thus, the dies **220** can be used in smaller electronic devices and the problems associated with EMI or other electromagnetic radiation in such high density packaged devices can be mitigated.

In the embodiment illustrated in FIG. **2**, formation of the interconnects **236** and the backplane structure **240** is complete. FIGS. **3**A-**5**D described below illustrate various embodiments of conductive backplane structures and methods for forming such structures. Although the following description illustrates only two interconnects adjacent to a portion of the backplane structure, it will be appreciated that (a) a plurality of interconnects are constructed simultaneously through a plurality of dies on a wafer, and (b) the backplane structure is fabricated across all or a substantial portion of the workpiece.

FIGS. **3**A-**3**F illustrate various stages of a method for forming one embodiment of the backplane structure **240** of FIG. **2**. FIG. **3**A, more specifically, is a schematic, side cross-sectional view of a portion of the workpiece **200** at an early stage of this process after constructing a substantial portion of an embodiment of the interconnect **236**, but before forming the backplane structure. More specifically, the workpiece **200** has dielectric layers **302** and **304** over at least a portion of the front side **212** of the substrate **210** to protect the substrate **210** and the terminals **232**. The dielectric layers **302** and **304** and/or one or more of the subsequent dielectric layers can be parylene, low temperature chemical vapor deposition (CVD) materials, such as tetraethylorthosilicate (TEOS), silicon nitride (Si_3Ni_4), silicon oxide (SiO_2), and/or other suitable dielectric materials. The foregoing list of dielectric materials is not exhaustive. The dielectric layers **302** and **304** are not generally composed of the same material as each other, but these layers may be composed of the same material. In addition, one or both of the dielectric layers **302** and **304** may be omitted and/or additional layers may be included.

The workpiece **200** also includes a plurality of vias or apertures **310** formed through at least part of the substrate **210** using etching, laser drilling, or other suitable techniques. The illustrated vias **310** are blind vias that extend only partially through the substrate **210** or are otherwise closed at one end. In other embodiments, however, the vias **310** can extend entirely through the workpiece **200** and/or the substrate **210**. Further details of representative methods for forming vias **310** are disclosed in pending U.S. patent application Ser. No. 11/027,443, filed Dec. 30, 2004, and incorporated herein by reference in its entirety.

The vias **310** are generally lined with another dielectric layer and one or more conductive layers (shown collectively as liner **320**). The embodiment of the liner **320** is shown schematically as a single layer, but in many embodiments the liner **320** has a number of different dielectric and conductive materials. The dielectric layer(s) of the liner **320** electrically insulate the components in the substrate **210** from the interconnects that are subsequently formed in each via **310**. The dielectric layer can include materials similar to those of the dielectric layers **302** and **304** described above. The conductive layer(s) of the liner **320** can include tantalum (Ta), tungsten (W), copper (Cu), nickel (Ni), and/or other suitable conductive materials.

After lining the vias **310**, vent holes **325** are formed in the substrate **210** to extend from a bottom portion of each via **310** to the back side **214** of the substrate **210**. After forming the vent holes **325**, a conductive fill material **327** is deposited into each via **310** to form the interconnects **236**. The fill material **327** can include Cu, Ni, silver (Ag), gold (Au), solder, conductive polymer, or other suitable materials or alloys of materials having the desired conductivity. The vent holes **325** allow trapped air, gases, or volatile solvents to escape from the larger vias **310** when filling the vias with the conductive fill material **327**. The vent holes **325** are an optional structure that can be omitted in several embodiments.

Referring next to FIG. **3**B, the substrate **210** is thinned to a desired thickness "T" by removing material from the back side **214** of the substrate **210**. In the illustrated embodiment, a back side portion **237** of each interconnect **236** is at least partially exposed after removing material from the back side **214**. In one embodiment, the initial thickness of the substrate **210** is approximately 750 μm, and the final thickness T is approximately 100-500 μm. The initial and final thicknesses can be different in other embodiments. The back side **214** of the substrate **210** can be thinned using chemical-mechanical planarization (CMP) processes, dry etching processes, chemical etching processes, chemical polishing, grinding procedures, or other suitable processes.

Referring to FIG. **3**C, the back side **214** of the substrate **210** is etched back to further expose the back side portions **237** of each interconnect **236**, thus forming conductive "posts" **238**. In other embodiments, other suitable processes in addition to, or in lieu of, the etching process can be used to offset the back side **214** of the substrate **210** from the ends of the interconnects **236** to form the posts **238**. After etching the back side **214**, a first dielectric layer **330** is deposited onto the back side **214** of the substrate **210** and over the posts **238**. The first dielectric layer **330** can be a low temperature CVD oxide or other suitable dielectric material, such as one of the materials described above with reference to FIG. **3**A. A conductive or metal layer **332** is then deposited over the first dielectric layer **330**. The conductive layer **332** is an embodiment of the metal or conductive layer **242** shown in FIG. **2**. The conductive layer **332** can be composed of aluminum (Al), Cu, Ni, W, a conductive polymer, or another suitable conductive material.

FIG. **3**D illustrates the workpiece **200** after the portions of the conductive layer **332** and the first dielectric layer **330** on the ends of the posts **238** (FIG. **3**C) have been removed to expose the back side portions **237** of each interconnect **236**. In this embodiment, for example, the overburden portions of the conductive layer **332** and the first dielectric layer **330** are removed from the workpiece **200** by pressing the workpiece **200** against a planarizing medium and moving the workpiece and/or the planarizing medium relative to each other in a CMP process. As a result, the conductive layer **332** has a planarized surface and the first dielectric layer **330** has a planarized portion proximate to and at least generally surrounding each interconnect **236** to electrically insulate the conductive layer **332** from the interconnects **236**. In other embodiments, the overburden portions of the conductive layer **332** and the first dielectric layer **330** can be removed using an etching process in lieu of, or in addition to, the CMP process.

Referring next to FIG. **3**E, a second dielectric layer or "cap" layer **334** is applied to the back side **214** of the substrate **210** over the remaining portions of the first dielectric layer **330**, the conductive layer **332**, and the exposed back side portions **237** of the interconnects **236**. The second dielectric layer **334** can include a low temperature CVD oxide (e.g., SiO_2), a photosensitive polyimide, or another suitable dielectric material. After depositing the second dielectric layer **334**, a plurality of openings **340** including a first opening **340***a* and a second opening **340***b* are formed in the second dielectric layer **334** to expose the back side portions **237** of the interconnects **236** and, in some cases, a portion of the conductive layer **332**. If the second dielectric layer **334** is a low temperature CVD oxide, the first and second openings **340***a* and **340***b* can be formed by patterning and etching the second dielectric layer **334** to form the openings. For example, the first and second openings **340***a* and **340***b* can be etched using one or more etching steps that selectively remove the material from the second dielectric layer **334** compared to the interconnects **236** and the conductive layer **332**. Alternatively, if the second dielectric layer **334** is a photosensitive polyimide material, a photolithographic procedure is used to selectively expose portions of the second dielectric layer **334**, and the exposed portions of the second dielectric layer **334** are developed to form the first and second openings **340***a* and **340***b*. In other embodiments, other suitable techniques and/or processes can be used to form the first and second openings **340***a* and **340***b*.

The dimensions and/or alignment of the first and second openings **340***a* and **340***b* can be used to selectively control which interconnects **236** will be electrically coupled to the conductive layer **332**. For example, the first opening **340***a* has a first diameter or cross-sectional dimension D_1 and the second opening **340***b* has a second diameter or cross-sectional dimension D_2 less than the first diameter D_1. The first diameter D_1 of the first opening **340***a* is sized such that both the back side portion **237** of the corresponding interconnect **236** and at least a portion of the conductive layer **332** adjacent to the interconnect **236** is exposed. Conversely, the second diameter D_2 of the second opening **340***b* is sized such that the portions of the conductive layer **332** adjacent to the second opening **340***b* are covered by the second dielectric layer **334** to ensure electrical isolation between the corresponding interconnect **236** and the conductive layer **332**. In one embodiment, the second opening **340***b* is configured so that only the backside portion **237** of the associated interconnect **236** is exposed.

Referring to FIG. **3**F, the conductive couplers **234** are attached to the back side portions **237** of each interconnect **236** to (a) selectively couple particular interconnects **236** to the conductive layer **332** of the backplane structure **240**, and (b) provide an external connection to other electronic devices at the back side **214** of the workpiece **200**. More specifically, the conductive coupler **234** in the first opening **340***a* is in electrical contact with both the interconnect **236** and the conductive layer **332** to electrically couple the corresponding interconnect **236** to the backplane **240**. In contrast, the conductive coupler **234** in the second opening **340***b* is electrically coupled to the corresponding interconnect **236**, but the size and/or alignment of the second opening **340***b* prevent the conductive coupler **234** from contacting the conductive layer **332**. This interconnect **236** accordingly remains electrically isolated from the backplane **240**. Any number of interconnects **236** within a particular die **220** (FIG. **2**) can be selectively coupled to the backplane **240** based on the particular specifications or operational requirements of the resulting device.

As discussed previously, electrically coupling one or more of the interconnects **236** to the backplane **240** can provide EMI shielding and/or grounding for devices having small arrays of back side contacts, such as the dies **220** (FIG. **2**) and the resulting packaged devices. Embodiments of the method described above with reference to FIGS. **3**A-**3**F are also expected to mitigate the problems associated with "floating" backplanes in which a conductive backplane is present in a particular device but is not electrically coupled to the circuitry in the device. As discussed above, for example, electrically and physically coupling one or more interconnects **236** to the backplane **240** with the conductive couplers **234** can provide a robust connection between the device's circuitry and the backplane **240**.

In one embodiment, a microfeature device comprises a semiconductor substrate having a front side, a back side, integrated circuitry and terminals electrically coupled to the integrated circuitry. The device also includes electrically conductive interconnects, electrically coupled to the terminals. The interconnects extend through at least a portion of the semiconductor substrate and have back side portions at the back side of the substrate. The device further includes a conductive backplane at the back side of the semiconductor substrate, and one or more of the interconnects are electrically coupled to the conductive layer at the back side of the semiconductor substrate.

In another embodiment, a microfeature workpiece comprises a semiconductor substrate having a front side, a back side, and a plurality of microelectronic dies on and/or in the substrate. The individual dies include integrated circuitry and bond-pads electrically coupled to the integrated circuitry. The workpiece also includes a plurality of electrically conductive through-substrate interconnects electrically coupled to corresponding bond-pads. The workpiece further includes a shield layer at the back side of the semiconductor substrate. First interconnects of individual dies are electrically coupled to the shield layer, and second interconnects of individual dies are electrically isolated from the shield layer.

In still another embodiment, a microelectronic device includes a semiconductor substrate having integrated circuitry and bond-pads electrically coupled to the integrated circuitry. The device also includes electrically conductive through-substrate interconnects in contact with corresponding bond-pads and having back side portions. The device further includes an EMI shield at a back side of the semiconductor substrate for EMI shielding. The back side portion of at least one interconnect is electrically coupled to the EMI shielding, and the back side portion of at least one other interconnect is electrically isolated from the EMI shield.

In yet another embodiment, a microfeature workpiece includes a semiconductor substrate having a front side, a back side, and a plurality of microelectronic dies on and/or in the semiconductor substrate. The individual dies include integrated circuitry, an array of bond-pads electrically coupled to the integrated circuitry, and a plurality of electrically conductive through-substrate interconnects electrically coupled to corresponding bond-pads. The dies also include a back side metal layer. One or more of the interconnects are electrically coupled to the metal layer. The workpiece further includes a plurality of scribe lines spacing apart the individual dies.

In still another embodiment, a microelectronic device includes a semiconductor substrate having a front side, a back side opposite the front side, integrated circuitry, and an array of bond-pads at the front side of the substrate electrically coupled to the integrated circuitry. The device also includes a plurality of electrically conductive interconnects extending through the substrate. The interconnects have front side portions electrically coupled with corresponding bond-pads and back side post portions at the back side of the substrate. The device further includes a conductive layer at the back side of the substrate. The conductive layer has an array of openings aligned with corresponding interconnects such that the back side post portions of the interconnects extend through the openings in the conductive layer. The device also includes dielectric spacers in the openings between the conductive layer and the back side post portions of the corresponding interconnects. The back side post portions of first interconnects are electrically coupled to the conductive layer, and the back side post portions of second interconnects are electrically isolated from the conductive layer.

Another embodiment is directed toward a method of processing a semiconductor substrate. The semiconductor substrate includes integrated circuitry and a plurality of terminals electrically coupled to the integrated circuitry. The method includes forming a plurality of electrically conductive interconnects extending at least partially through the substrate and in contact with corresponding terminals. The interconnects have back side portions at a back side of the semiconductor substrate. The method also includes constructing a conductive backplane at a back side of the semiconductor substrate. The method further includes electrically coupling at least one of the back side portions of the interconnects to the backplane, and electrically isolating at least one other interconnect from the backplane.

Another embodiment is directed toward yet another method of processing a semiconductor substrate having a plurality of microelectronic dies. The individual dies include an integrated circuit and bond-pads electrically coupled to the integrated circuit. The method includes constructing a plurality of electrically conductive through-substrate interconnects extending at least partially through the semiconductor substrate and in contact with corresponding bond-pads. The method also includes forming a metal layer at a back side of the semiconductor substrate. The method further includes selectively coupling a back side portion of first interconnects of individual dies to the metal layer, while keeping second interconnects of individual dies electrically isolated from the metal layer.

Still another embodiment is directed toward a method of fabricating a semiconductor substrate. The semiconductor substrate has integrated circuitry, a plurality of bond-pads electrically coupled to the integrated circuitry, and a plurality of electrically conductive through-substrate interconnects in contact with corresponding bond-pads. The method includes forming an EMI shield at a back side of the semiconductor substrate that does not directly contact the interconnects. The method further includes coupling an interconnect to the shield with a solder ball in direct physical contact with a back side portion of the interconnect and a corresponding portion of the shield.

FIGS. **4**A-**4**C are schematic, side cross-sectional views illustrating various stages of a method for forming another embodiment of the backplane structure **240** shown in FIG. **2**. The initial stages of this method are at least generally similar to the steps described above with reference to FIGS. **3**A-**3**C, and as such FIG. **4**A shows a workpiece configuration similar to that illustrated in FIG. **3**C. The subsequent stages of this method, however, differ from that described above with reference to FIGS. **3**A-**3**F in that a dielectric layer is not deposited over the back side **214** of the substrate **210**. Instead, a conductive or metal layer **402** is deposited directly onto the back side **214** and over the exposed back portions **237** of the interconnects **236**. The conductive layer **402** can include an argon (Ar) pre-sputter with TiAl, Ti-silicide, or another suitable conductive material that can bond directly to the silicon material of the substrate **210**.

FIG. **4**B illustrates the workpiece **200** after the overburden portions of the conductive layer **402** have been removed to expose the back side portions **237** of each interconnect **236**. The overburden portions of the conductive layer **402** can be removed from the workpiece **300** using a CMP process or etching process similar to those described above with reference to FIG. **3**D. In other embodiments, however, another suitable technique can be used to remove the desired portions of the conductive layer **402**.

Referring next to FIG. **4**C, a first dielectric layer **404** is applied to the back side **214** of the substrate **210** over the conductive layer **402** and the exposed back side portions **237** of the interconnects **236**. The first dielectric layer **404** can include a low temperature CVD oxide, a photosensitive polyimide, or another suitable dielectric material similar to those described previously. After depositing the first dielectric layer **404**, a plurality of openings **406** (two are shown as a first opening **406***a* and a second opening **406***b*) are formed in the first dielectric layer **404** to expose the back side portions **237** of the interconnects **236** and, in some cases, a portion of the conductive layer **402** adjacent to the interconnects **236**. The first and second openings **406***a* and **406***b* can be formed using processes or techniques similar to those described above with reference to FIG. **3**E. As discussed previously, the chosen technique depends largely on the composition of the first dielectric layer **404**.

Similar to the first and second openings **340***a* and **340***b* described above with reference to FIG. **3**E, the dimensions and/or alignment of the first and second openings **406***a* and **406***b* shown in FIG. **4**C can be used to selectively control which interconnects **236** will be electrically coupled to the conductive layer **402**. For example, the first opening **406***a* has a third diameter or cross-sectional dimension D_3 and the second opening **406***b* has a fourth diameter or cross-sectional dimension D_4 less than the third diameter D_3. The third diameter D_3 is sized such that both the interconnect **236** and a portion of the conductive layer **402** adjacent to the interconnect **236** are exposed. The fourth diameter D_4, however, is sized such that the conductive layer **402** covers the dielectric portions of the liner **320** at the second opening **406***b*. A conductive coupler **410** (e.g., a solder ball or other external interconnect structure) in the first opening **406***a* accordingly electrically couples the associated interconnect **236** to the conductive layer **402** of the backplane structure, but another conductive coupler **410** in the second opening **406***b* is electrically coupled only to the corresponding interconnect **236** and remains electrically isolated from the backplane structure.

The methods for forming the backplane structure described above with reference to FIGS. **3**A-**4**D include (a) a single CMP step to remove the overburden portions of the conductive layer and/or the dielectric layer, and (b) a single masking step to selectively form openings over the interconnects having the desired dimensions and alignment. Using only a single CMP step and a single masking step provides an efficient process to fabricate the backplane structure. Furthermore, reducing the amount of processing also mitigates the potential for damage to and/or contamination of the workpiece **200** that can result from CMP or other rigorous processes.

FIGS. **5**A-**5**D are schematic, side cross-sectional views illustrating various stages of a method for forming still another embodiment of the backplane structure **240** shown in FIG. **2**. Referring first to FIG. **5**A, the initial stages of this method are at least generally similar to the steps described above with reference to FIGS. **3**A and **3**B, but the back side **214** of the substrate **210** is not etched or otherwise recessed back to form the conductive posts **238** (FIG. **3**C). Instead, after thinning the substrate **210** to the desired thickness, a conductive layer **502** is deposited over the back side **214** of the substrate **210** and the exposed back side portions **237** of each interconnect **236** to provide the material for the conductive backplane. The conductive layer **502** can include conductive materials generally similar to those described above with reference to FIG. **3**C and FIG. **4**A.

After depositing the conductive layer **502**, a first mask **504** is applied over the conductive layer **502**. The first mask **504** can be a layer of resist that is patterned according to the arrangement of the interconnects **236** and the desired configuration of the resulting backplane structure. In the embodiment shown in FIG. **5**A, for example, the first mask **504** has an opening **505** over one of the interconnects **236**, and then an opening **506** is formed through the conductive layer **502** to expose the corresponding interconnect **236** and at least a portion of the back side **214** of the substrate **210**. The opening **506** can be formed using etching or another suitable process. The first mask **504** can be removed.

Referring to FIG. **5**B, a first dielectric layer **508** is deposited onto the workpiece **300** over the conductive layer **502** and into the opening **506** such that the first dielectric layer **508** covers the exposed back side portions of the interconnects **236** and the substrate **210**. The first dielectric layer **508** can include a low temperature CVD oxide or another suitable dielectric material. A second mask **510** is subsequently applied over the first dielectric layer **508** and patterned to form openings over the interconnects **236**.

Referring next to FIG. **5**C, a plurality of openings **512** (two are shown as a first opening **512***a* and a second opening **512***b*) are formed in the first dielectric layer **508** using an etching process or another suitable technique. The first opening **512***a* exposes the back side portion **237** of the corresponding interconnect **236**, and the second opening **512***b* exposes the conductive layer **508**. In one embodiment, the etching process selectively removes the material of the dielectric layer **508** faster than the material of the conductive layer **502** or the interconnect **236**. FIG. **5**D illustrates the workpiece **200** after conductive couplers **520** have been deposited into the respective first and second openings **512***a* and **512***b*. The conductive coupler **520** in the first opening **512***a* is electrically coupled to the corresponding interconnect **236**, but is electrically isolated from the conductive layer **502**. On the other hand, the conductive coupler **520** in the second opening **512***b* is directly electrically coupled to the conductive layer **502**, thus electrically coupling the corresponding interconnect **236** to the backplane structure.

FIG. **6** is a schematic, side cross-sectional view of a packaged microelectronic device **600** configured in accordance with an embodiment of the invention. The microelectronic device **600** includes a plurality of microelectronic dies **620** (individually identified as a first microelectronic die **620***a* and a second microelectronic die **620***b*) interconnected in a stacked-die arrangement. The first and second microelectronic dies **620***a* and **620***b* can have many components at least generally similar to the microelectronic dies **220** discussed above and illustrated in FIG. **2**. For example, the first and second dies **620***a* and **620***b* can each include integrated circuitry **622** and connectors **630** electrically coupled to the integrated circuitry **622**. Each connector **630** can include a terminal **632** (e.g., a bond-pad), a conductive coupler **634** (e.g., a solder ball or other external interconnect structure), and an interconnect **636** extending through the respective die coupling the terminal **632** to the conductive coupler **634**. The first and second dies **620***a* and **620***b* also include a conductive backplane structure **640** at a back side of the individual dies. The backplane structure **640** can include, for example, a conductive or metal layer **642** on the respective dies. The backplane structure **640** can be constructed using any of the methods described above with respect to FIGS. **3**A-**5**D.

In the illustrated embodiment, the conductive couplers **634** of the first upper die **620***a* are coupled to corresponding terminals **632** of the second lower die **620***b* to electrically connect the first die **620***a* to the second die **620***b*. A suitable underfill material **690** or other compound can optionally be used to structurally attach the first and second dies **620***a* and **620***b* together in the illustrated stacked-die configuration. Additionally, the conductive couplers **634** at the back side of the second die **620***b* can in turn be used to electrically connect the microelectronic device **600** to another external device or board.

In one embodiment, for example, a microelectronic assembly includes a first microelectronic device and a second microelectronic device coupled to the first device in a stacked configuration. The first device has a first microelectronic die with a first integrated circuit and an array of first bond-pads electrically coupled to the first integrated circuit. The first die also includes first electrically conductive interconnects extending at least partially through the first die and in contact with corresponding first bond-pads. The first die further includes a first conductive backplane assembly having a first conductive layer at a back side of the first die, with at least one first interconnect electrically coupled to the first conductive layer. The second device has a second microelectronic die with a second integrated circuit and an array of second bond-pads electrically coupled to the second integrated circuit. The second die also includes second electrically conductive interconnects extending at least partially through the second die and in contact with corresponding second bond-pads. The second die further includes a second conductive backplane assembly having a second conductive layer at a back side of the second die, with at least one second interconnect electrically coupled to the second conductive layer.

The stacked microelectronic device **600** or any one of the microelectronic devices formed using the methods described above with reference to FIGS. **1**A-**6** can be incorporated into any of a myriad of larger and/or more complex systems **700**, a representative one of which is shown schematically in FIG. **7**. The system **700** can include a processor **702**, a memory **704** (e.g., SRAM, DRAM, DDR-SDRAM, flash memory, such as NAND flash memory or other types of flash memory, and/or other suitable memory devices), input/output devices **706**, and/or other subsystems or components **708**. Microelectronic devices and/or microfeature workpieces (e.g., in the form of microfeature dies and/or combinations of microfeature dies) may be included in any of the components shown in FIG. **7**. The resulting system **700** can perform any of a wide variety of computing, processing, storage, sensor, imagers, and/or other functions. Accordingly, representative systems **700** include, without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants), multi-processor systems, processor-based or programmable consumer electronics, network computers, and mini-computers. Other representative systems **700** include cameras, light or other radiation sensors, servers and associated server subsystems, display devices, and/or memory devices. In such systems, individual dies can include imager arrays, such as a CMOS imager. Components of the system **700** may be housed in a single unit or distributed over multiple, interconnected units, e.g., through a communications network. Components can accordingly include local and/or remote memory storage devices and any of a wide variety of computer-readable media.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the invention. For example, structures and/or processes described in the context of particular embodiments may be combined or eliminated in other embodiments. In particular, the conductive backplane structures described above with reference to particular embodiments can include one or more additional dielectric or conductive layers, or one or more of the layers described above can be omitted. Further, the connections between the interconnects, backplane structures, and other devices (e.g., bond pads, conductive couplers, and/or external devices) can have arrangements different than those described above. In several embodiments, for example, the electrical connectors can include ball-pads at the back side of the dies and electrically coupled to corresponding interconnects and conductive couplers. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. A method of processing a semiconductor substrate, the semiconductor substrate having integrated circuitry and a plurality of terminals electrically coupled to the integrated circuitry, the method comprising:

forming a plurality of electrically conductive interconnects extending at least partially through the substrate and in contact with corresponding terminals, the interconnects having back side portions at a back side of the semiconductor substrate;

constructing a conductive backplane at the back side of the semiconductor substrate, wherein constructing a conductive backplane at the back side of the semiconductor substrate comprises depositing a conductive layer onto the back side of the substrate, the conductive layer having openings around the interconnects and dielectric spacers in the openings between the conductive layer and the interconnects; and

electrically coupling at least one of the back side portions of the interconnects to the backplane via a conductive coupler in one of the openings and in direct contact with the corresponding interconnect and the conductive layer, and electrically isolating at least one of the plurality of other interconnects from the backplane.

2. The method of claim **1** wherein electrically isolating at least one of the plurality of other interconnects comprises placing another conductive coupler in contact with the back side portion of the other particular interconnect and electrically isolated from the backplane.

3. The method of claim **1** wherein electrically coupling at least one of the back side portions of the interconnects to the backplane comprises electrically coupling at least one of the back side portions of the interconnects to the backplane within the footprint of the semiconductor substrate.

4. The method of claim **1** wherein:

constructing a conductive backplane at the back side of the semiconductor substrate comprises (a) depositing a metal layer onto the back side of the substrate and electrically isolated from the interconnects, (b) depositing a dielectric layer over the metal layer, and (c) forming the openings in the dielectric layer to at least partially expose the back side portions of the individual interconnects; and

electrically coupling at least one of the back side portions of the interconnects to the backplane comprises placing a solder ball in a particular opening sized to expose the corresponding interconnect and an adjacent portion of the metal layer, the solder ball being in direct contact with the respective interconnect and the metal layer.

5. The method of claim **1** wherein the plurality of electrically conductive interconnects comprises a first interconnect and a second interconnect, and wherein:

constructing a conductive backplane at the back side of the semiconductor substrate comprises—

depositing a first dielectric layer onto the back side of the substrate and in contact with the first and second interconnects;

depositing the conductive layer over the first dielectric layer;

planarizing the substrate by placing the back side of the substrate against a planarizing medium and moving the substrate and/or the planarizing medium relative to each other in a manner that removes portions of the first dielectric layer and conductive layer from the substrate to leave the remaining portions of the conductive layer out of direct contact with the first and second interconnects;

depositing a second dielectric layer over the first dielectric layer and the conductive layer; and

creating a first opening in the second dielectric layer to expose the first interconnect and a portion of the conductive layer, and creating a second opening the second dielectric layer to expose the second interconnect without exposing the conductive layer; and

electrically coupling at least one of the back side portions of the interconnects to the backplane comprises—

depositing a first conductive coupler into the first opening and in contact with the first interconnect and the conductive layer; and

depositing a second conductive coupler into the second opening and in contact with the second interconnect, wherein the second conductive coupler is out of contact with the conductive layer.

6. The method of claim **5** wherein:

depositing a first dielectric layer comprises depositing a low temperature CVD oxide;

depositing the conductive layer over the first dielectric layer comprises depositing Al, Cu, Ni, W, and/or a conductive polymer; and

depositing a second dielectric layer over the first dielectric layer and the conductive layer comprises depositing a low temperature CVD oxide and/or a photosensitive polyimide.

7. The method of claim **5** wherein the second dielectric layer comprises a low temperature CVD oxide, and wherein creating the first opening and the second opening in the second dielectric layer comprises etching the first and second openings in the second dielectric layer.

8. The method of claim **5** wherein the second dielectric layer comprises a photosensitive polyimide, and wherein creating the first opening and the second opening in the second dielectric layer comprises developing the photosensitive second dielectric layer to have the first and second openings aligned with the first and second interconnects, respectively.

9. A method of processing a semiconductor substrate having a plurality of microelectronic dies, the individual dies including an integrated circuit and bond-pads electrically coupled to the integrated circuit, the method comprising:

constructing a plurality of electrically conductive through-substrate interconnects extending at least partially through the semiconductor substrate and in contact with corresponding bond-pads, wherein the plurality of electrically conductive interconnects comprises first interconnects and second interconnects;

forming a metal layer at a back side of the semiconductor substrate; and

selectively coupling back side portions of the first interconnects of individual dies to the metal layer while keeping the second interconnects of individual dies electrically isolated from the metal layer,

wherein selectively coupling the back side portions of the first interconnects to the metal layer comprises placing solder balls in contact with the back side portions of the first interconnects and portions of the metal layer adjacent to the first interconnects.

10. The method of claim **9** wherein selectively coupling back side portions of the first interconnects of individual dies to the metal layer comprises coupling the back side portions of the first interconnects to the metal layer within the footprint of the respective dies.

11. The method of claim 9, further comprising:

depositing a dielectric layer onto the back side of the substrate and over the metal layer; and

forming first openings in the dielectric layer to expose the back side portions of the first interconnects and adjacent portions of the metal layer, and forming second openings in the dielectric layer to expose a back side portion of the individual second interconnects, wherein the metal layer is isolated from the second openings, and

selectively coupling a back side portion of first interconnects of individual dies to the metal layer while keeping second interconnects of individual dies electrically isolated from the metal layer comprises (a) placing the solder balls in the first openings in direct contact with the corresponding first interconnects and adjacent portions of the metal layer, and (b) placing the solder balls in the second openings in contact with the corresponding second interconnects and electrically isolated from the metal layer.

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