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(54) **III-V FET DEVICE WITH OVERLAPPED EXTENSION REGIONS USING GATE LAST**

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**H01L 29/78** (2006.01)

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CPC ..... **H01L 29/78** (2013.01); **H01L 29/66431** (2013.01)

(58) **Field of Classification Search**  
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USPC ..... 257/192  
See application file for complete search history.

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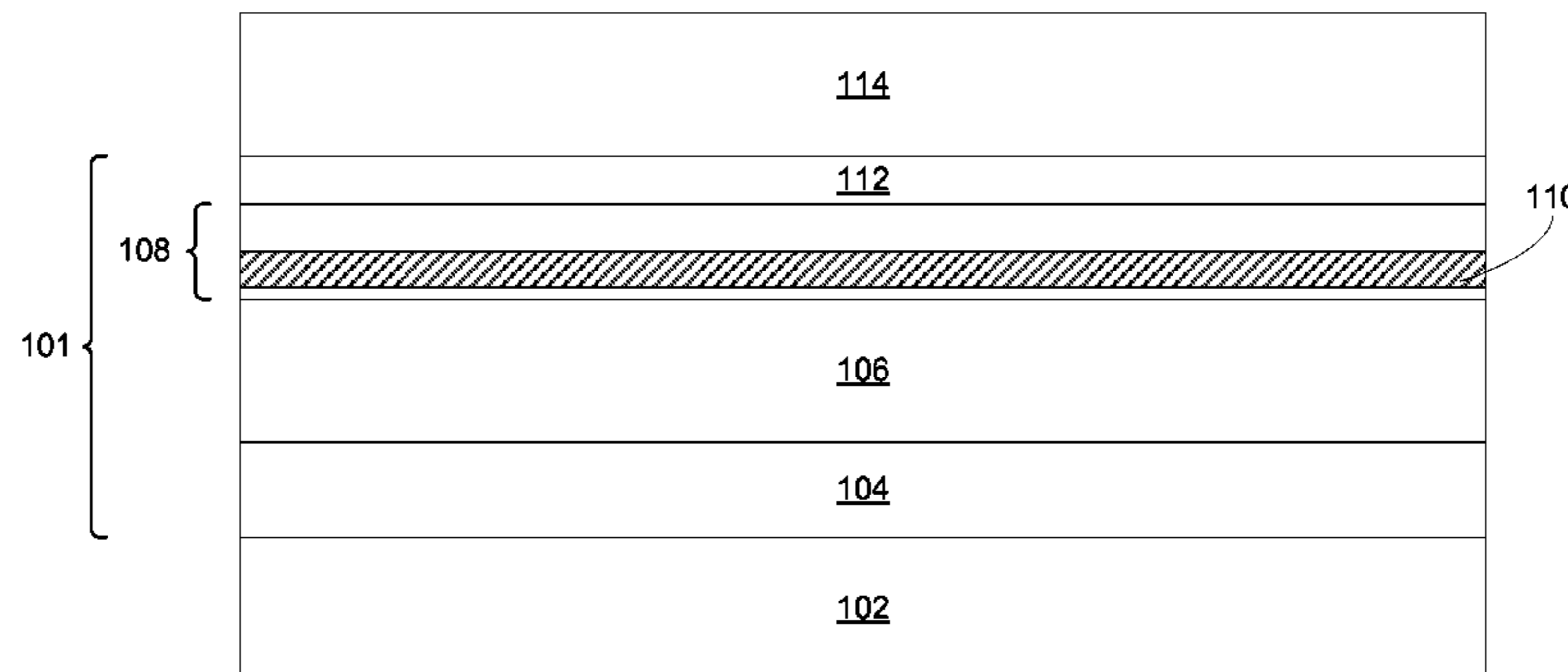
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(57) **ABSTRACT**

A structure and method for fabricating a III-V compound semiconductor-containing heterostructure field-effect transistor (FET) with self-aligned and overlapped extensions using a gate last process is disclosed. The a III-V compound semiconductor-containing heterostructure field-effect transistor (FET) structure may be formed by forming a III-V compound semiconductor-containing heterostructure having at least one layer; forming a doped contact layer on the III-V compound semiconductor-containing heterostructure; and forming a gate structure having a bottom surface substantially below an upper surface of the III-V compound semiconductor-containing heterostructure and an upper surface above the doped contact layer. An undoped region may be formed below the bottom surface of the T-shaped gate structure on a layer of the III-V compound semiconductor-containing heterostructure.

**13 Claims, 8 Drawing Sheets**

100  
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100

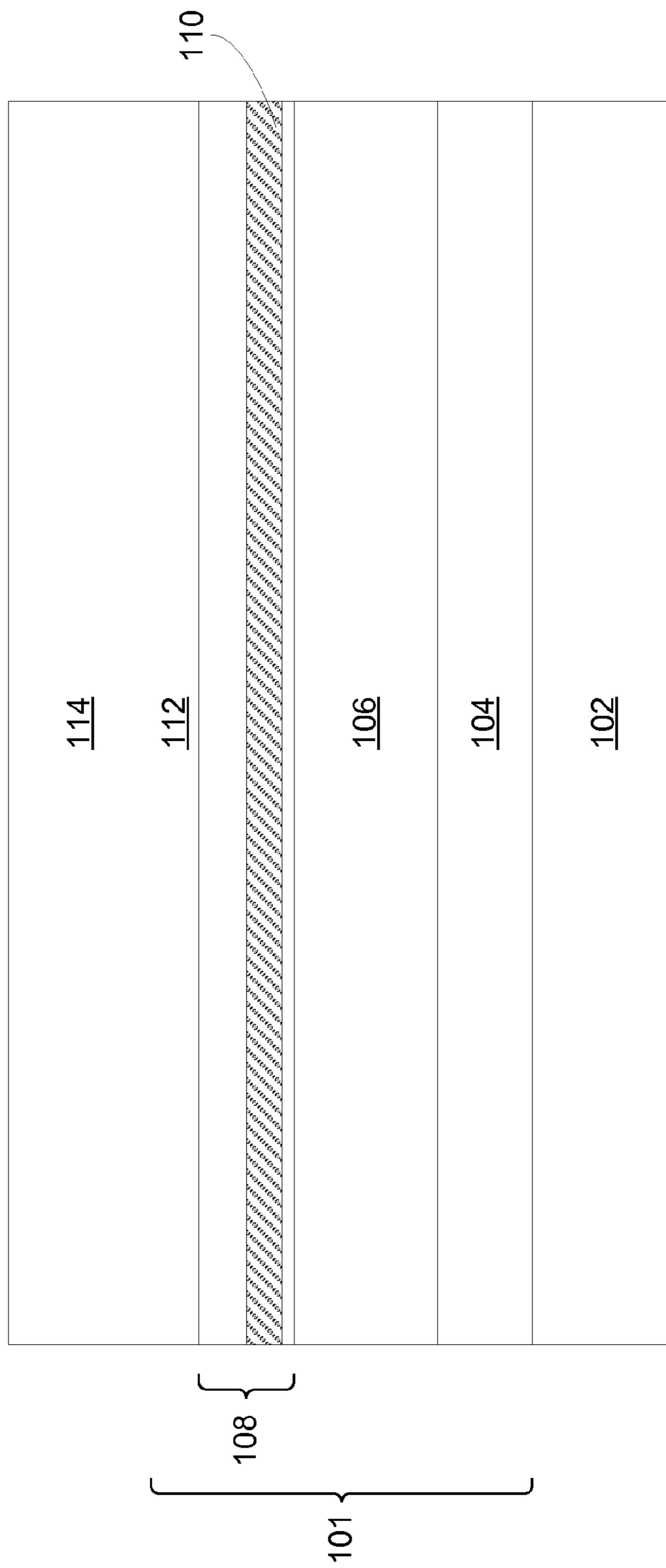


FIG. 1

200

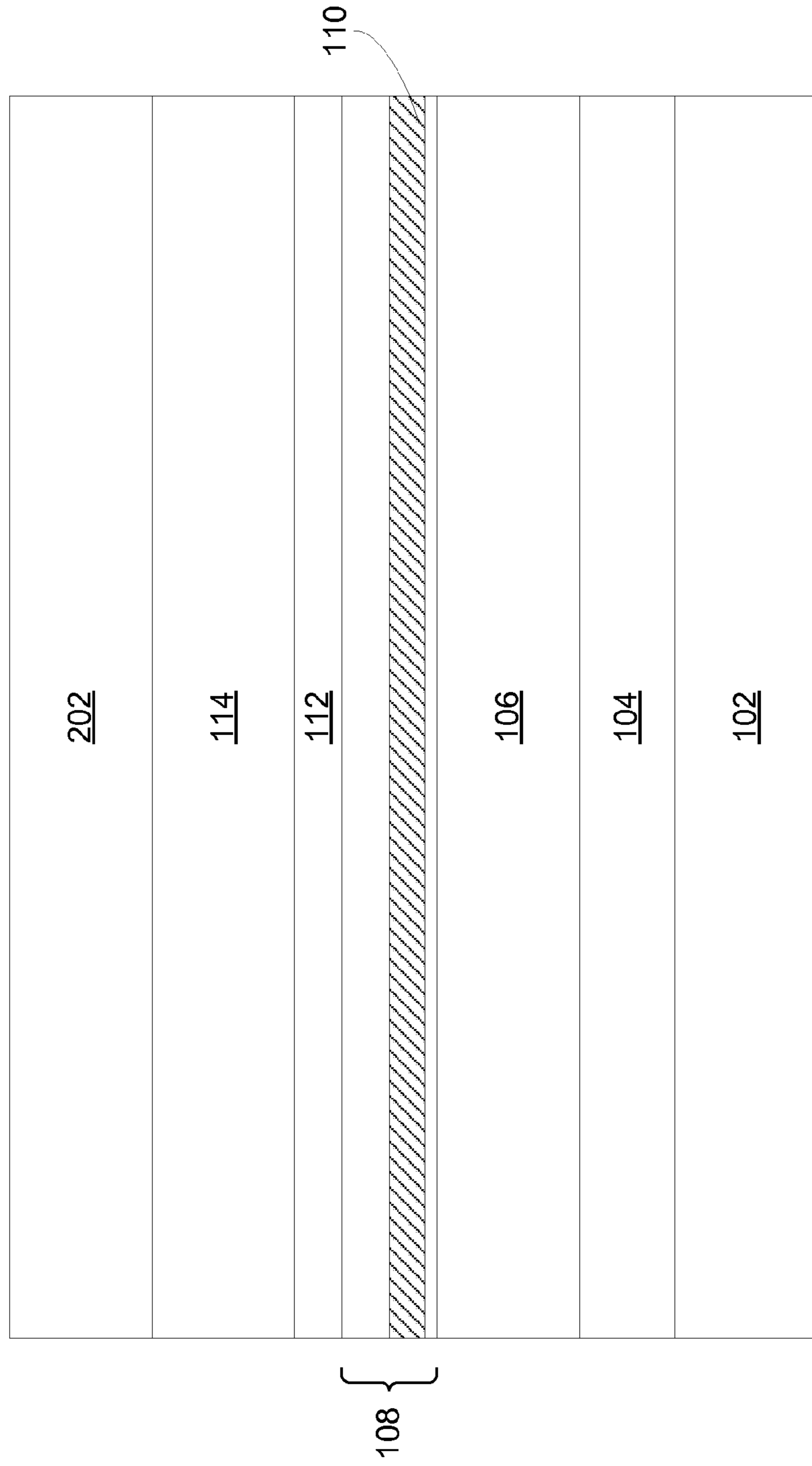


FIG. 2

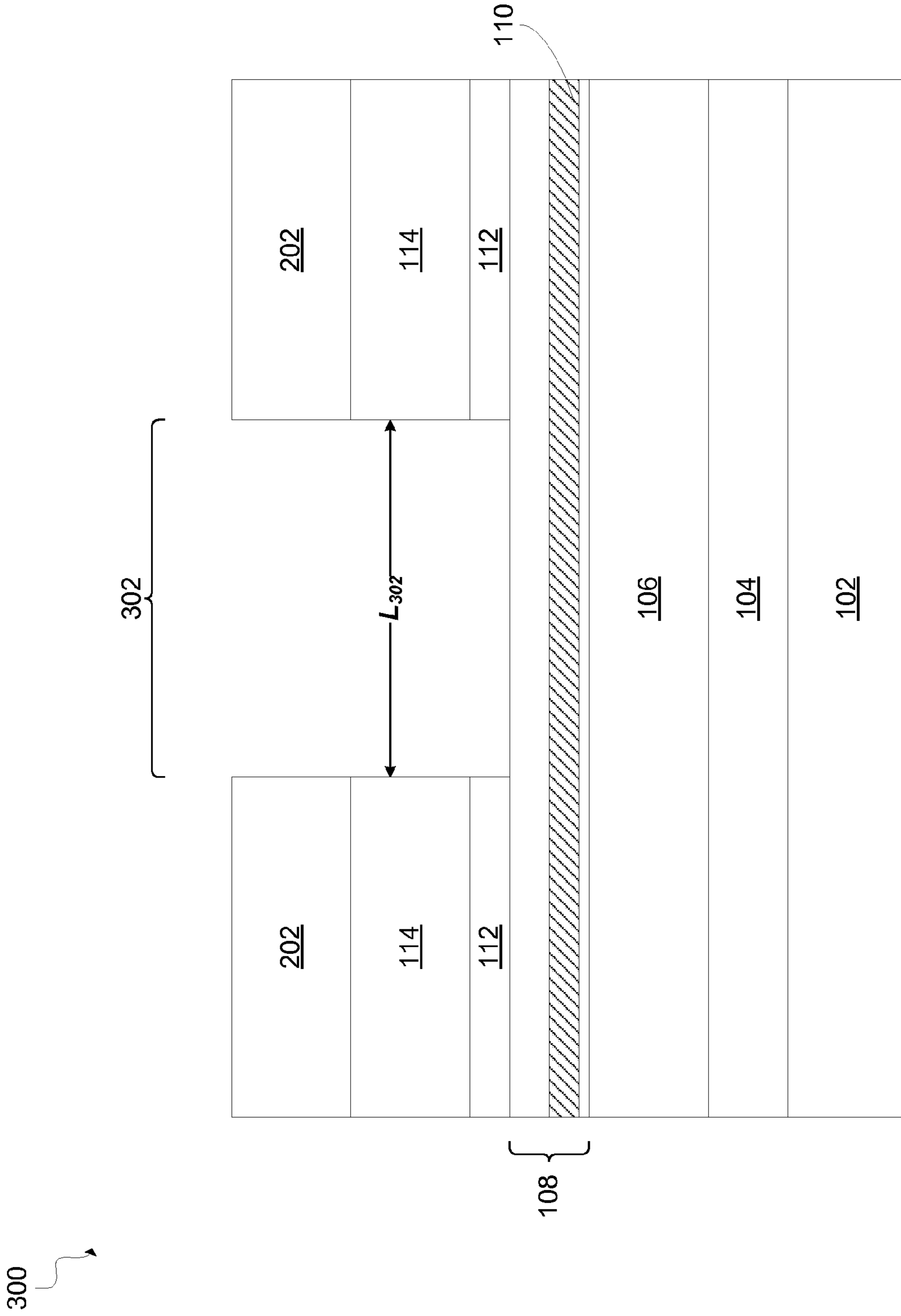


FIG. 3

400

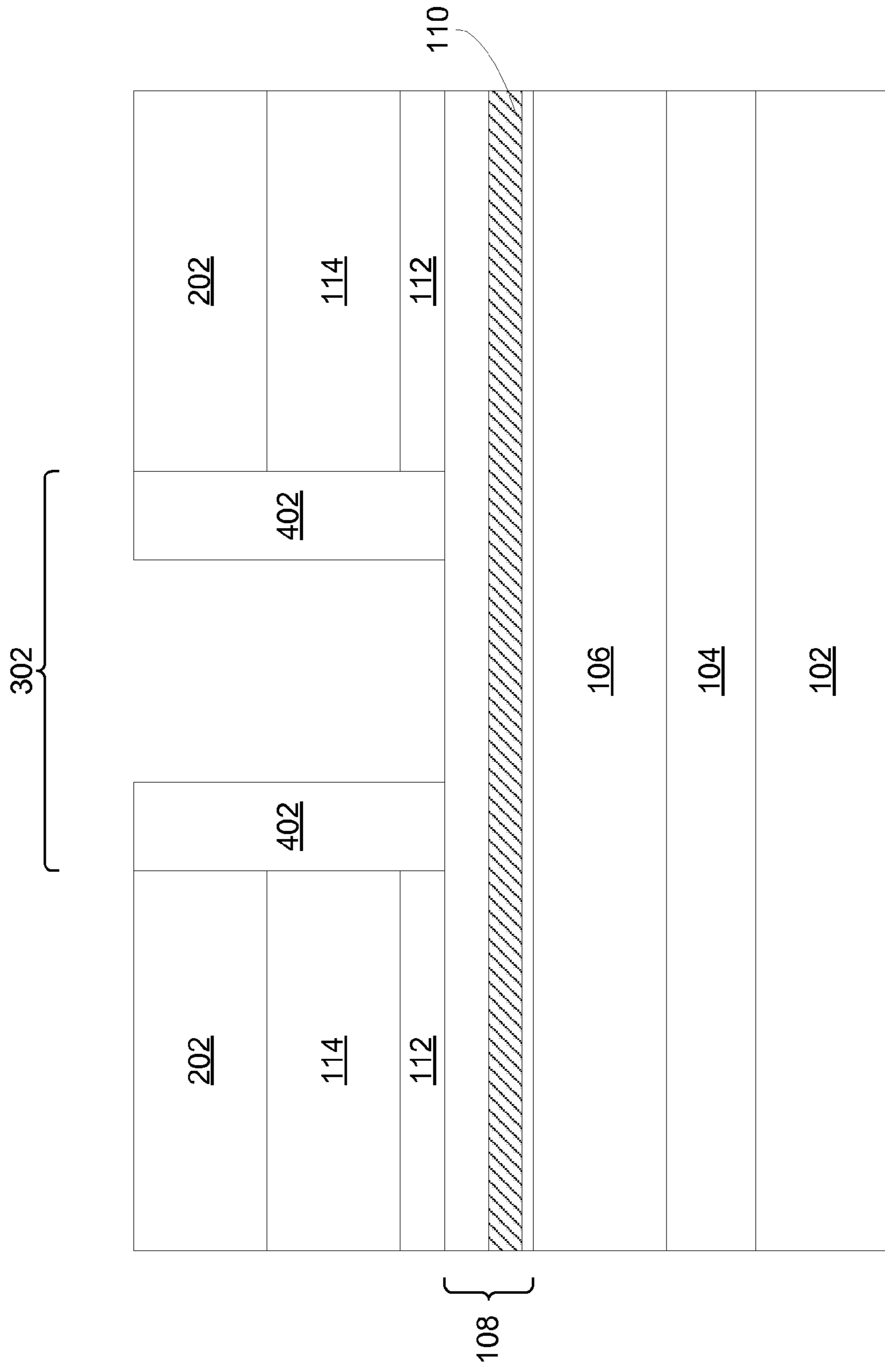


FIG. 4

500A

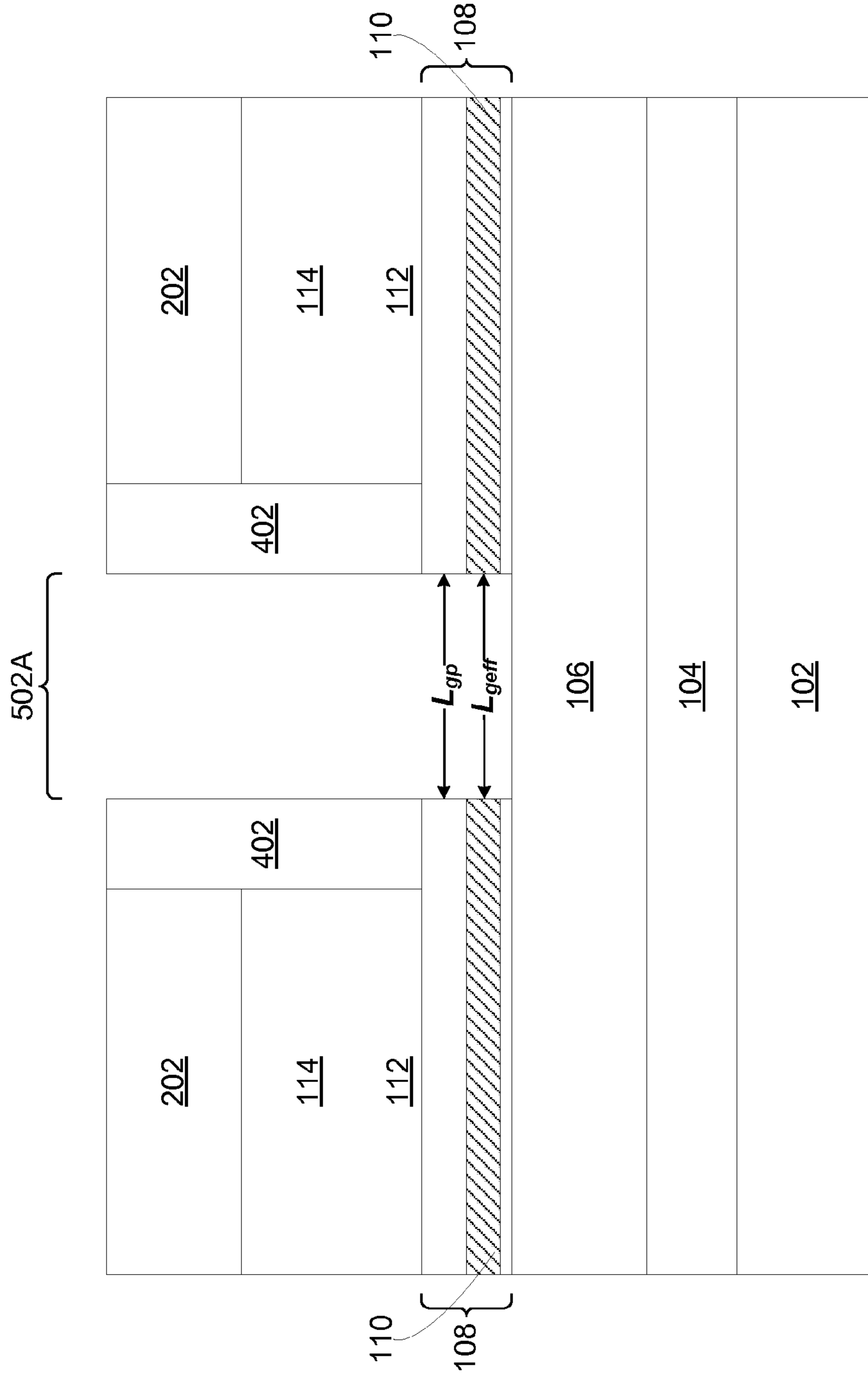


FIG. 5A

500B

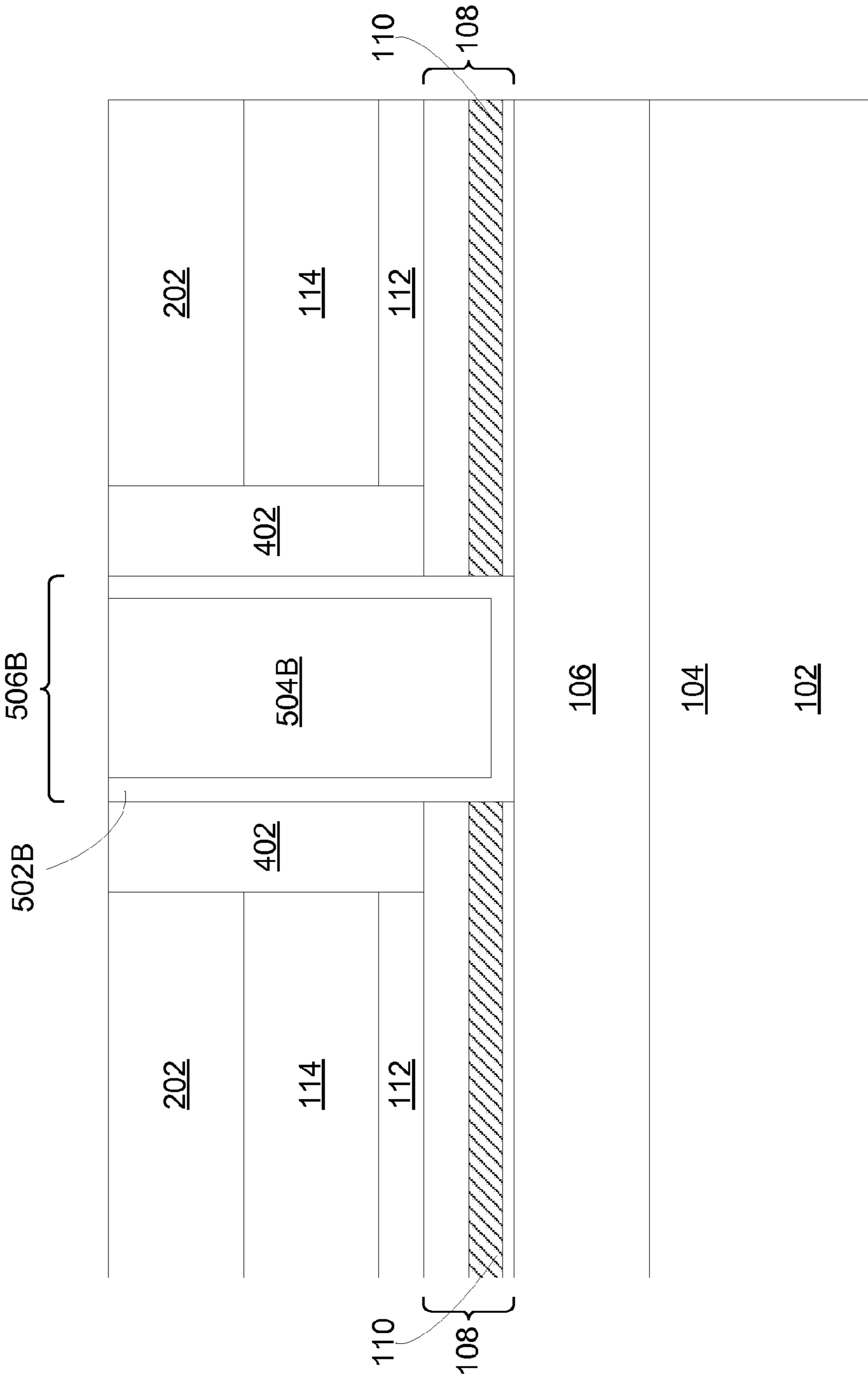


FIG. 5B

600A

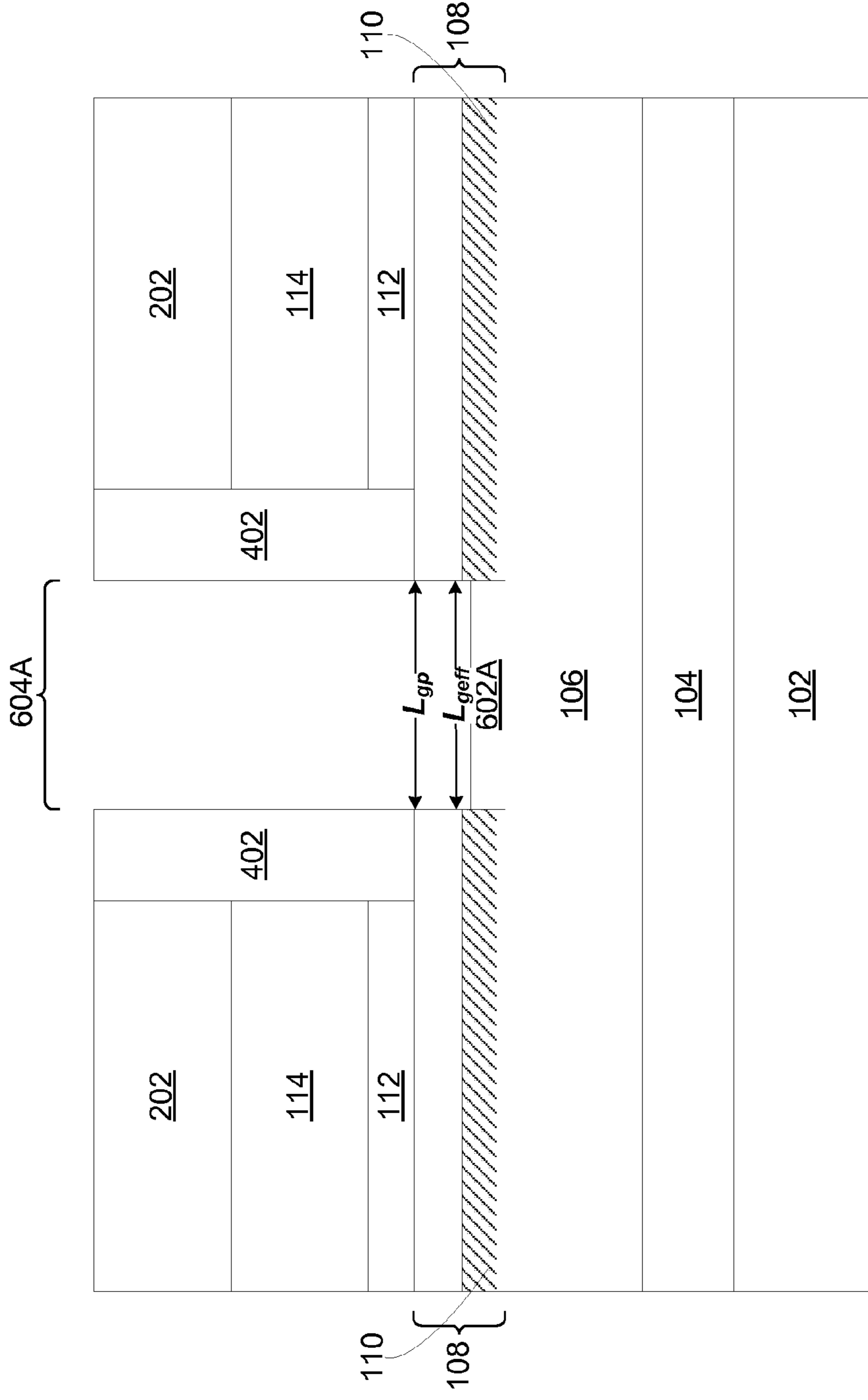


FIG. 6A



600B

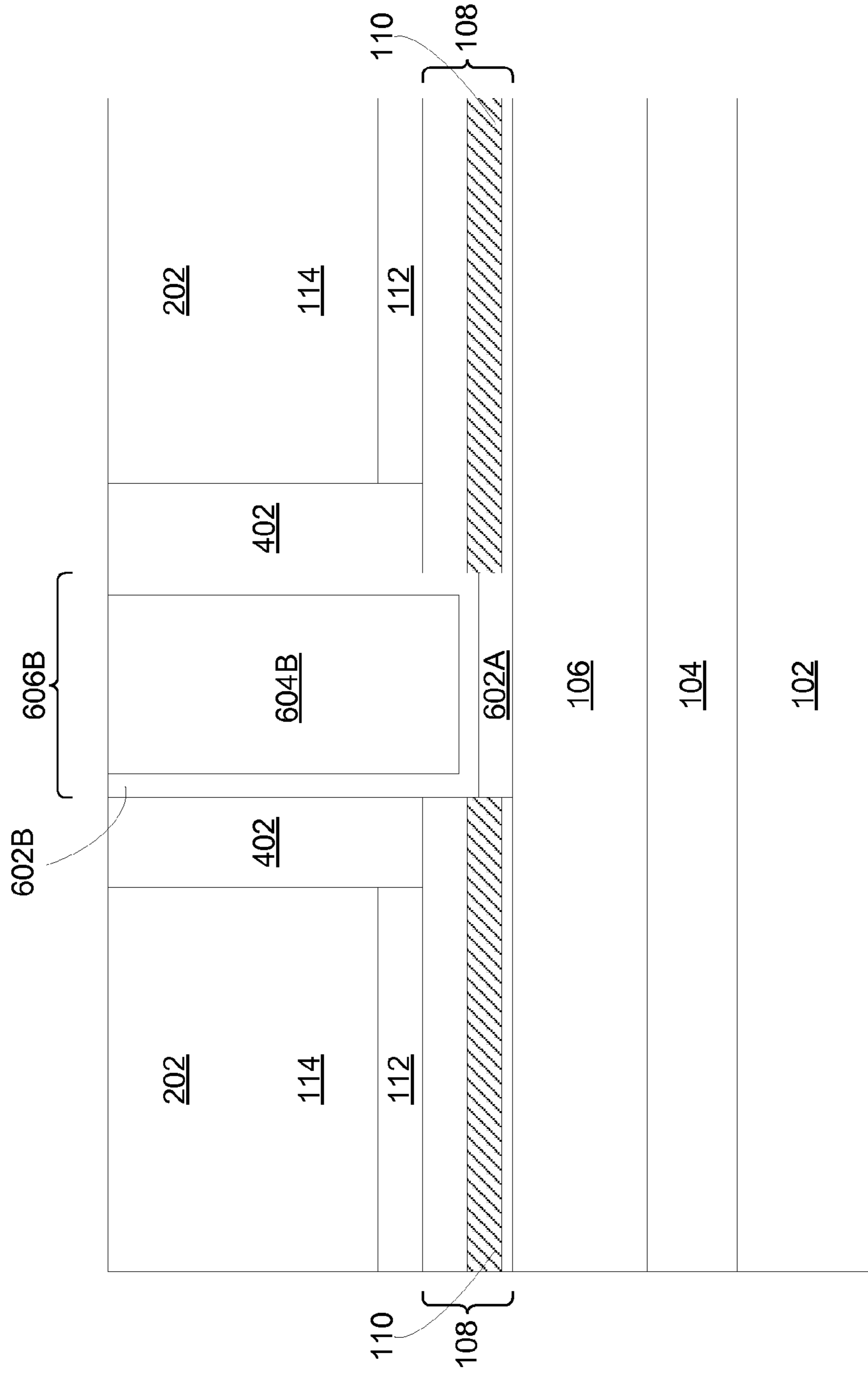


FIG. 6B

## 1

**III-V FET DEVICE WITH OVERLAPPED  
EXTENSION REGIONS USING GATE LAST**

## FIELD

The present invention relates generally to the fabrication of integrated circuits, and more particularly, to a structure and method for fabricating a III-V compound semiconductor-containing heterostructure field-effect transistor (FET) with self-aligned and overlapped extensions using a gate last process.

## BACKGROUND

Compound III-V semiconductors are receiving renewed attention for use as channel materials for advanced ultra large scale integration (ULSI) digital logic applications due to their high electron hole mobility. For example, the InGaAs/InAlAs material system is one of the most promising material systems for this application due to its large conduction-band offsets and high carrier mobility. Schottky-gated InGaAs high electron mobility transistors (III-V HEMTs) grown on InP substrates have produced maximum transconductance  $g_m$  values and have been shown to compare favorably in terms of a power-delay product.

Conventional III-V HEMTs are self-aligned structures in which the physical length of the gate structure equals the effective length of the channel. However, in III-V HEMTs, gate leakage due to a lack of gate dielectric is an important factor limiting their performance reliability. Thus, a thin gate dielectric layer is often inserted between the gate metal and the wide bandgap barrier layer forming a III-V metal-oxide semiconductor HEMT (III-V MOS-HEMT) or a III-V metal-oxide semiconductor field-effect transistor (III-V MOSFET). The use of a gate dielectric layer has the beneficial effect of reducing gate leakage. III-V MOS-HEMTs and III-V MOSFETs devices exhibit a leakage reduction of six to ten orders of magnitude compared to a Schottky barrier HEMT of similar design. However, the use of a gate dielectric has the deleterious effect of reducing the transconductance because of a larger gate-to-channel separation. Furthermore, decrease of gate-to-source capacitance may cause a shift of threshold voltage ( $V_t$ ) for devices with a doped channel.

One limitation with conventional self-aligned III-V MOS-HEMTs and III-V MOSFETs is that they are underlapped (i.e., the effective length of the channel is larger than the physical length of the gate structure) due to the fact that ion implantation techniques used in conventional silicon-based MOSFETs to create overlapped devices are not viable for III-V materials. In III-V devices, damage created from ion implantation and subsequent rapid thermal anneal (RTA) can lead to strain relaxation, which degrades the transport properties of III-V materials. Conventional methods to manage the problem of strain relaxation have involved keeping the RTA temperature low, but this leads to an insufficient diffusion and insufficient activation of implanted ions.

## SUMMARY

According to one embodiment of the present invention, a method of forming a semiconductor device is disclosed. The method may involve forming a III-V compound semiconductor-containing heterostructure having at least one layer; forming a doped contact layer on the III-V compound semiconductor-containing heterostructure; and forming a gate structure having a bottom surface substantially below an upper surface of the III-V compound semiconductor-contain-

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ing heterostructure and an upper surface above the doped contact layer. An undoped region may be formed below the bottom surface of the T-shaped gate structure on a layer of the III-V compound semiconductor-containing heterostructure.

In another embodiment, a method of forming a semiconductor device is disclosed. The method of forming the semiconductor device may include: forming a III-V compound semiconductor-containing heterostructure having at least one layer; forming a doped contact layer on the III-V compound semiconductor-containing heterostructure; forming a dielectric layer on the doped contact layer; forming a gate trench extending from an upper surface of the dielectric layer, through the doped contact layer, to a barrier layer that is substantially below an upper surface of the III-V compound semiconductor-containing heterostructure; forming gate spacers having an upper surface that is substantially flush with the upper surface of the dielectric layer on sidewalls of the gate trench and on the barrier layer; forming a gate region by removing the barrier layer from the region of the gate trench between the gate spacers; and forming a gate structure having an upper surface that is substantially flush with the upper surface of the gate spacers in the gate region. An undoped region may be formed below the bottom surface of the T-shaped gate structure on a layer of the III-V compound semiconductor-containing heterostructure.

In another embodiment, a structure of a semiconductor device is disclosed. The semiconductor structure may include a III-V compound semiconductor-containing heterostructure having at least one layer; a doped contact layer on the III-V compound semiconductor-containing heterostructure; a dielectric layer on the doped contact layer; a gate structure having an upper surface that is substantially flush with an upper surface of the dielectric layer and having a bottom surface on a channel layer that is substantially below an upper surface of the III-V compound semiconductor-containing heterostructure; and gate spacers having an upper surface that is substantially flush with the upper surface of the dielectric layer on an upper surface of the barrier layer adjacent to and contacting the gate structure. The structure may also include an undoped region below the bottom surface of the T-shaped gate structure on the channel layer of the III-V compound semiconductor-containing heterostructure.

BRIEF DESCRIPTION OF THE SEVERAL  
VIEWS OF THE DRAWINGS

The following detailed description, given by way of example and not intended to limit the invention solely thereto, will best be appreciated in conjunction with the accompanying drawings, in which not all structures may be shown.

FIG. 1 is a cross sectional view of a III-V compound semiconductor-containing heterostructure and a doped contact layer formed on a semiconductor substrate, according to an embodiment of the present invention.

FIG. 2 is a cross sectional view illustrating the formation of a dielectric layer, according to an embodiment of the present invention.

FIG. 3 is a cross sectional view illustrating the formation of a gate trench, according to an embodiment of the present invention.

FIG. 4 is a cross sectional view illustrating the formation of gate spacers, according to an embodiment of the present invention.

FIG. 5A is a cross sectional view illustrating the removal of an etch stop layer and barrier layer, according to an embodiment of the present invention.

FIG. 5B is a cross sectional view illustrating the formation of a gate structure, according to an embodiment of the present invention.

FIG. 6A is a cross sectional view illustrating the formation of an undoped region, according to an embodiment of the present invention.

FIG. 6B is a cross sectional view illustrating the formation of a gate structure, according to an embodiment of the present invention.

The drawings are not necessarily to scale. The drawings are merely schematic representations, not intended to portray specific parameters of the invention. The drawings are intended to depict only typical embodiments of the invention. In the drawings, like numbering represents like elements.

### DETAILED DESCRIPTION

Detailed embodiments of the claimed structures and methods are disclosed herein; however, it can be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the scope of this invention to those skilled in the art. In the description and drawings, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments.

In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps, and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by one of ordinary skill of the art that the invention may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the invention. It will be understood that when an element as a layer, region, or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or “directly” over another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “beneath” or “under” another element, it can be directly beneath or under the other element, or intervening elements may be present. In contrast, when an element is referred to as being “directly beneath” or “directly under” another element, there are no intervening elements present.

Two embodiments by which to achieve self-aligned overlapped extensions in a III-V compound semiconductor-containing heterostructure FETs are described in detail below by referring to the accompanying drawings FIGS. 1-6B. Process steps and structures common to both embodiments are described in detail by FIGS. 1-4, while one embodiment is described in detail by FIGS. 5A-5B and another is described in detail by FIGS. 6A-6B.

In the present invention, the term “III-V compound semiconductor” denotes a semiconductor material that includes at least one element from Group III of the Periodic Table of Elements and at least one element from Group V of the Periodic Table of Elements. Typically, each of the III-V compound semiconductor layers is a binary, ternary, or quaternary III-V containing compound. Examples of III-V compound semiconductors that can be used in the present invention

include, but are not limited to, alloys of InGaAs, InAlAs, InAlAsSb, InAlAsP, and InGaAsP.

Referring to FIG. 1, an initial structure **100** may be used in one embodiment of the present invention. Structure **100** may include a III-V compound semiconductor-containing heterostructure **101** formed on top of a semiconductor substrate **102**. The III-V compound semiconductor-containing heterostructure **101** may include a III-V compound semiconductor buffer layer **104** having a first bandgap, a III-V compound semiconductor channel layer **106** having a second bandgap located on a upper surface of the buffer layer **104**, a III-V compound semiconductor barrier layer **108** having a third bandgap located on an upper surface of the channel layer **106**, and an etch stop layer **112** on an upper surface of the barrier layer **108**. A doped contact layer **114** may be formed on the III-V compound semiconductor-containing heterostructure **101**.

In the present embodiment, the barrier layer **108** may include a delta doped region **110** that is located in a lower region of the barrier layer **108** abutting next to, but not in direct contact with, the interface with the underlying channel layer **106**. The dopant atom present in the delta doped region **110** may be an n-type dopant (i.e., an element from Group IV or VI of the Periodic Table of Elements) or a p-type dopant (i.e., an element from Group II or IV of the Periodic Table of Elements). The concentration of dopant in the delta doped region **110** may be approximately  $10^{11}$  atom/cm<sup>2</sup> to approximately  $10^{13}$  atom/cm<sup>2</sup>.

The semiconductor substrate **102** may include any semiconductor material including, for example, Si, SiGe, SiGeC, SiC, Ge alloys, Ga, GaAs, InAs, InP, Ge, and all other III-V compound semiconductors. The semiconductor substrate **102** may be composed of a layered semiconductor material such as, for example, a semiconductor-on-insulator substrate. The semiconductor substrate **102** may be doped, undoped, or contain doped and undoped regions therein. The semiconductor substrate **102** may have a single crystal orientation or it may have surface regions that have different crystal orientation. The semiconductor substrate **102** may be strained, unstrained, or a combination thereof.

The bandgap of the barrier layer **108** (i.e., the third bandgap) may be larger (wider) than the bandgap of the channel layer **106** (i.e., the second bandgap). As stated above, the term “bandgap” refers to the energy difference between the top of the valance band (i.e.,  $E_v$ ) and the bottom of the conduction band (i.e.,  $E_c$ ). The barrier layer **108** may be composed of a III-V compound semiconductor having a bandgap value that is from approximately 0.5 times to approximately 10 times larger than the bandgap of the III-V compound semiconductor material used in the channel layer **106**. In a preferred embodiment, the barrier layer **108** may be composed of a III-V compound semiconductor having a bandgap value that is from approximately 1 times to approximately 5 times larger than the bandgap of the III-V compound semiconductor material used in the channel layer **106**.

The bandgap of the buffer layer **104** (i.e., the first bandgap) may also be larger than that of the channel layer **106**. This helps confine the electrons within the channel layer **106**. The buffer layer **104** may be composed of a III-V compound semiconductor having a band gap value that is from approximately 0.5 times to approximately 10 times larger than the bandgap of the III-V semiconductor material used in the channel layer **106**. In one embodiment, the buffer layer **104** may be composed of a III-V compound semiconductor having a band gap value that is from approximately 1 times to approximately 5 times larger than the bandgap of the III-V semiconductor material used in the channel layer **106**.

It is noted that the bandgap of the buffer layer **104** and the bandgap of the barrier layer **108**, which may be larger than the bandgap of the channel layer **106**, do not necessarily have the same value. Since wide bandgap materials are used for the barrier layer **108** and buffer layer **104**, and a narrow bandgap material is used for the channel layer **106**, carriers are confined to the channel layer **106** under certain gate bias range. The carriers may be confined in the channel layer **106** when typical gate bias conditions are applied.

In one embodiment of the present invention, the barrier layer **108** and the buffer layer **104** may be composed of an alloy of InAlAs, while the channel layer **106** may be composed of an alloy of InGaAs. By "alloy of InAlAs" it is meant a composition of  $\text{In}_x\text{Al}_{1-x}\text{As}$  wherein  $x$  is from approximately 0 to approximately 1, and more preferably from approximately 0.4 to approximately 0.6. By "alloy of InGaAs" it is meant a composition of  $\text{In}_y\text{Ga}_{1-y}\text{As}$  wherein  $y$  is from approximately 0 to approximately 1, and more preferably from approximately 0.3 to approximately 0.8. It is noted that each of the III-V compound semiconductor layers employed in the present invention may be a single crystal material of typical commercial quality. The typical commercial quality of the III-V compound semiconductor layers is a result of utilizing an epitaxial growth process such as, for example, molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition (MOCVD). The III-V compound semiconductor layers may be epitaxially grown utilizing III/V-containing precursors that are well known to those skilled in the art. In some embodiments, a graded III-V compound semiconductor layer can be formed.

When a delta doped region **110** is formed into the lower region of the barrier layer **108**, an in-situ doping deposition process may be used in which the dopant atom is introduced during the initial formation of the barrier layer **108** and following the formation of a desired thickness of the delta doped region **110** (approximately 0.1 nm to approximately 2.0 nm), the dopant is removed from the precursor stream and the barrier layer **108** formation continues. Alternatively, the delta doped region **110** may be formed utilizing ion implantation after the barrier layer **108** has been formed. The conditions of such an implant are selected to provide a delta doped region next to, but not in contact with, the interface **107** of the underlying channel layer **106**.

The doped contact layer **114** may be formed by an epitaxial growth process. As used herein, the terms "epitaxially formed," "epitaxial growth," and/or "epitaxial deposition" mean the growth of a crystalline semiconductor material on a deposition surface. During the epitaxial growth process, chemical reactants are controlled and system parameters are set so that depositing atoms arrive at the deposition surface with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the atoms of the deposition surface. The doped contact layer **114** may be formed by the epitaxial growth of a III-V compound semiconductor. The doped contact layer **114** may also be formed by the epitaxial growth of silicon or germanium. In another embodiment, the doped contact layer **114** may be composed of SiGe.

In one embodiment, a portion of the doped contact layer **114** may be in-situ doped with a p-type conductivity dopant during the selective epitaxial growth process. P-type semiconductor devices (PFETs) in III-V materials are typically produced by doping the source-drain regions with a p-type dopant composed of elements from: group II of the Periodic Table of Elements, including beryllium or magnesium, that replace a group III atom; or group IV of the Periodic Table of Elements, including carbon, that replace a group V atom. In

one embodiment, the doped contact layer **114** may have a p-type dopant in a concentration ranging from approximately  $1 \times 10^{19}$  atoms/cm<sup>3</sup> to approximately  $5 \times 10^{21}$  atoms/cm<sup>3</sup>. In another embodiment, the p-type conductivity dopant may be introduced to the doped contact layer **114** using ion implantation following the epitaxial growth process that is used to form the doped contact layer **114**.

The doped contact layer **114** may also be in-situ doped with an n-type conductivity dopant during the selective epitaxial growth process. N-type semiconductor devices (NFETs) in III-V materials are typically produced by doping the source-drain regions with a dopant composed of elements from: group IV of the Periodic Table of Elements, including silicon or germanium, that replace a group III atom; or (ii) group VI of the Periodic Table of Elements, including sulfur, selenium, or tellurium, that replace a group V atom. In one embodiment, the doped contact layer **114** may have a n-type dopant in a concentration ranging from approximately  $1 \times 10^{19}$  atoms/cm<sup>3</sup> to approximately  $5 \times 10^{21}$  atoms/cm<sup>3</sup>. In another embodiment, the n-type conductivity dopant may be introduced to the doped contact layer **114** using ion implantation following the epitaxial growth process that is used to form the doped contact layer **114**.

Each of the individual III-V compound semiconductor layers shown in FIG. 1 are thin (providing a total thickness of less than approximately 600 nm). The buffer layer **104** may have a thickness of approximately 5 nm to approximately 500 nm. The channel layer **106** may have a thickness of approximately 2 nm to approximately 10 nm. The barrier layer **108** may have a thickness of approximately 1 nm to approximately 5 nm. The etch stop layer **112** may have a thickness of approximately 1 nm to approximately 2 nm. The doped contact layer **114** may have a thickness of approximately 10 nm to approximately 30 nm.

Referring now to FIG. 2, a structure **200** is illustrative of a dielectric layer **202** formed on the doped contact layer **114**. The dielectric layer **202** may be formed utilizing a conventional deposition process including, but not limited to, depositing dielectric material using molecular beam epitaxy (MBE), chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD), evaporation, physical vapor deposition (PVD), chemical solution deposition, and other like deposition processes. The dielectric material may be deposited on the doped contact layer **114** using a blanket deposition process and then planarized using a conventional process such as, for example, chemical mechanical planarization (CMP).

In one embodiment, the dielectric layer **202** may be composed of a low-k dielectric material including, but not limited to, an oxide and/or silicates including metal silicates, aluminates, and titanates. A "low-k" material is a dielectric material with a lower dielectric constant relative to silicon dioxide (SiO<sub>2</sub>), which is 3.9 (i.e., the ratio of the permittivity of SiO<sub>2</sub> divided by the permittivity of a vacuum). In an embodiment in which the dielectric layer **202** is composed of an oxide, the oxide may be selected from the group including, but not limited to, SiO<sub>2</sub>, HfO<sub>2</sub>, ZrO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, SrTiO<sub>3</sub>, LaAlO<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, and mixtures thereof. In another embodiment, the dielectric layer **202** may be composed of a dielectric material with a dielectric constant ranging from approximately 4.0 to approximately 7.0. In such an embodiment, the dielectric layer **202** may be composed of an oxide, including, but not limited to, silicon oxide, carbon doped silicon oxide, fluorine doped silicon oxide, hydrogen silsesquioxane polymer (HSQ), methyl silsesquioxane polymer (MSQ), polyph-

nylene oligomer, methyl doped silica,  $\text{SiO}_x(\text{CH}_3)_y$ ,  $\text{SiC}_x\text{O}_y\text{H}_z$ , organosilicate glass ( $\text{SiCOH}$ ), porous  $\text{SiCOH}$ , and mixtures thereof.

Referring now to FIG. 3, a gate trench 302 may be formed by etching the dielectric layer 202, the doped contact region 114, and the etch stop layer 112 to form a structure 300. In a preferred embodiment, the dielectric layer 202, the doped contact region 114, and the etch stop layer 112 may be patterned and etched to desired dimensions. Standard masking and photolithography techniques may be implemented to pattern the gate trench 302 onto the surface of the dielectric layer 202. Subsequently, standard etching techniques, such as, reactive ion etching (RIE), selective to the barrier layer 108 may then be implemented to etch the gate trench 302 into the dielectric layer 202, the doped contact region 114, and the etch stop layer 112. In a preferred embodiment, the gate trench 302 may have a length  $L_{302}$  that is the desired gate length plus two times the length of each desired gate spacer 402 (shown in FIG. 4). Therefore,  $L_{302} = L_g + 2L_{gs}$ , where  $L_g$  is the desired physical gate length and  $L_{gs}$  is the desired length of each gate spacer.

Referring now to FIG. 4, a pair of gate spacers 402 (hereinafter "gate spacers") may be formed on an upper surface of the barrier layer 108 and vertical sides of the gate trench 302 to form a structure 400. In one embodiment, the gate spacers 402 may be composed of a nitride. The gate spacers 402 may be formed by depositing a conformal layer of nitride, or by bulk deposition, on dielectric layer 202, the doped contact layer 114, the etch stop layer 112, and the barrier layer 108 by standard deposition techniques such as, but not limited to, CVD, PECVD, PVD, MOCVD, ALD, low pressure CVD (LPCVD), evaporation, reactive sputtering, chemical solution deposition, or any other suitable deposition process. Subsequently, an anisotropic etch, such as RIE, may be performed to removed the deposited layer from horizontal surfaces of the dielectric layer 202 and barrier layer 108, leaving the gate spacers 402 present on the vertical sidewalls of the gate trench 302. The deposited layer of gate spacer material may be etched so that the upper surface of the gate spacers 402 is substantially flush with an upper surface of the dielectric layer 202. In another embodiment, the gate spacers 402 may be planarized through a conventional process such as CMP so that the upper surface of the gate spacers 402 is substantially flush with an upper surface of the upper surface of the dielectric layer 202.

Referring now to FIG. 5A, the entirety of the barrier layer 108, including the delta doped region 110, may be removed from the portion of the gate trench 302 not covered by the gate spacers 402 to form a gate region 502A in a structure 500A. In one embodiment, the entirety of the barrier layer 108, including the delta doped region 110, in the portion of the gate trench 302 not covered by the gate spacers 402 may be removed by a conventional etching process selective to the channel layer 106 such as, for example, RIE. The outer edges of the gate region 502A may be self-aligned to the barrier layer 108, including the delta doped region 110, resulting in an effective gate length  $L_{geff}$  that may be equal to the physical gate length  $L_{gp}$ . In other words, there may be available electrons present in the regions below the gate spacers 402 that border the gate region 502A.

Referring now to FIG. 5B, a gate dielectric layer 502B and a gate conductor 504B may be deposited and planarized in the gate region 502A to form a gate structure 506B on the III-V MOSFET structure 700B. The gate dielectric layer 502B may be composed of a dielectric material having a dielectric constant of greater than approximately 4.0; such a dielectric material is referred to hereafter as a high-k dielectric material.

The gate dielectric layer 502B may be composed of a high-k dielectric material having a dielectric constant of greater than approximately 7.0. In a preferred embodiment, the gate dielectric layer 502B may be composed of a high-k dielectric material having a dielectric constant of greater than approximately 10.0. The dielectric constants mentioned herein are relative to a vacuum, unless otherwise stated. The gate dielectric layer 502B may be composed of a high-k dielectric material including, but not limited to: an oxide, nitride, oxynitride and/or silicates including metal silicates, aluminates, titanates, and nitrides. In one embodiment, the gate dielectric layer 502B may be composed of  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_2$ ,  $\text{La}_2\text{O}_3$ ,  $\text{SrTiO}_3$ ,  $\text{LaAlO}_3$ ,  $\text{Y}_2\text{O}_3$ , a perovskite oxide,  $\text{HfSiO}_z$ ,  $\text{HfAlO}_z$ , or  $\text{HfAlO}_a\text{N}_b$ . The gate dielectric layer 502B may be formed utilizing a conventional deposition process including, but not limited to, MBE, CVD, PECVD, ALD, evaporation, PVD, chemical solution deposition, and other like deposition processes.

The thickness of the gate dielectric layer 502B may vary depending on the deposition technique employed in forming the same as well as the composition and number of dielectrics of the gate dielectric layer 502B. Typically, the gate dielectric layer 502B may have a thickness of approximately 0.5 nm to approximately 20 nm.

The gate conductor 504B may be composed of any conductive material such as, for example: polysilicon, polysilicon germanium, conductive metals, conductive metal alloys, conductive silicides, conductive nitrides, and combinations or multilayers thereof. When metallic-containing gate conductors are employed, the metallic gate conductor can be doped so as to shift the workfunction of the gate conductor. Illustrative examples of dopant ions include As, P, B, Sb, Bi, Al, Ga, Ti, or mixtures thereof. The same dopants may be used with the polysilicon or polySiGe mentioned above. In a preferred embodiment, the gate conductor 504B is a conductive metal such as Al, Pt, Au, W, and Ti. The gate conductor 504B may be formed by a conventional deposition process such as, for example, CVD, PECVD, PVD, plating, thermal or ebeam evaporation, and sputtering.

In one embodiment, after the gate dielectric layer 502B and a gate conductor 504B are deposited they may be planarized using a conventional process such as, for example, CMP, so that an upper surface of the gate structure 506B is substantially flush with the upper surface of the dielectric layer 202.

Referring now to FIG. 6A, and in another embodiment, a structure 600A shows an undoped region 602A epitaxially grown on the exposed upper surface of the channel layer 106 to form a gate region 604A. The undoped region 602A may be composed of the same material as the barrier layer 108 and grown through an epitaxial growth process that is selective to the channel layer 106 (i.e., does not result in epitaxial growth on the dielectric layer 202, the gate spacers 402, or the barrier layer 108). The undoped region 602A may have a thickness of approximately 1 nm to approximately 2 nm. The outer edges of the gate region 604A may be self-aligned to the barrier layer 108, including the delta doped region 110, resulting in an effective gate length  $L_{geff}$  that may be equal to the physical gate length  $L_{gp}$ . In other words, there may be available electrons present in the regions below the gate spacers 402 that border the gate region 604A.

Referring now to FIG. 6B, a III-V MOS-HEMT structure 600B may be formed by depositing a gate dielectric layer 602B and a gate conductor 604B in the gate region 604A (FIG. 6) and on the undoped region 602A to form a gate structure 606B using the same processes and techniques described above in reference to FIG. 5B. The gate dielectric layer 602B and gate conductor 604B may be composed of the

same materials as the gate dielectric layer **502B** and gate conductor **504B** as described above in reference to FIG. **5B**. The gate dielectric layer **602B** and gate conductor **604B** may be substantially similar to the gate dielectric layer **502B** and the gate conductor **504B** as described above with reference to FIG. **5B**.

As described above, preferred embodiments of the present invention provide for self-aligned overlapped III-V MOS-HEMTs and III-V MOSFETs using formation methods that avoid the problems associated with ion implantation in III-V devices such as strain relaxation and insufficient diffusion or activation of implanted ions.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiment, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed is:

**1.** A method of forming a semiconductor device, comprising the steps of:

forming a III-V compound semiconductor-containing heterostructure above a substrate, wherein the III-V compound semiconductor-containing heterostructure comprises a buffer layer above the substrate, a channel layer above and in contact with the buffer layer, and a barrier layer above and in contact with the channel layer; and forming a gate structure, the gate structure having a width that extends between two spacers and a lowermost surface of the gate structure that is in contact with, and extends no further than a lowermost surface of the barrier layer, wherein a lowermost surface of the spacers is in contact with, and extends no further than, an uppermost surface of the barrier layer.

**2.** The method of claim **1**, further comprising:

forming an etch stop layer above the barrier layer;  
forming a doped contact layer above the etch stop layer;  
and

forming a dielectric layer above the doped contact layer; the dielectric layer having an uppermost surface that is substantially flush with an uppermost surface of the spacers and an uppermost surface of the gate structure.

**3.** The method of claim **1**, further comprising forming a delta-doped region surface of within the barrier layer by doping a region of the barrier layer with an element from Group IV, II, or VI of the Periodic Table of Elements.

**4.** The method of claim **1**, wherein the forming a gate structure comprises:

removing a portion of the barrier layer between the spacers to form a gate region, wherein the gate region exposes the uppermost surface of the channel layer, and wherein

the gate region has sidewalls that are substantially flush with sidewalls of the spacers;

forming a gate dielectric on the sidewalls of the spacers, on sidewalls of the barrier layer, and on the uppermost surface of the channel layer; and

forming a gate conductor on the gate dielectric.

**5.** The method of claim **4**, wherein the gate dielectric layer has a dielectric constant greater than approximately 4.0.

**6.** The method of claim **1**, further comprising forming an undoped region between the lowermost surface of the gate structure and the uppermost surface of the channel layer.

**7.** The method of claim **2**, wherein the forming a doped contact layer comprises doping the doped contact layer with a p-type or n-type dopant from Group II or Group IV of the Periodic Table of Elements.

**8.** A method of forming a semiconductor device, comprising the steps of:

forming a III-V compound semiconductor-containing heterostructure on a substrate, wherein the III-V compound semiconductor-containing comprises a buffer layer at above the substrate, a channel layer above and in contact with the buffer layer, and a barrier layer above and in contact with the channel layer;

forming an etch stop layer above the barrier layer;

forming a doped contact layer above the etch stop layer;

forming a dielectric layer above the doped contact layer;

forming a gate trench extending from an uppermost surface of the dielectric layer to an uppermost surface of the barrier layer;

forming gate spacers on the uppermost surface of the barrier layer in the gate trench, the gate spacers having a lowermost surface that extends no further than the uppermost surface of the barrier layer;

forming a gate region by removing a portion of the barrier layer between the gate spacers, the gate region exposing an uppermost surface of the channel layer; and

forming a gate structure in the gate region, the gate structure having a lowermost surface that is in contact with, and extends no further than, a lowermost surface of the barrier layer.

**9.** The method of claim **8**, further comprising forming a delta-doped region within the barrier layer by doping a region of the barrier layer with an element from Group IV, II, or VI of the Periodic Table of Elements.

**10.** The method of claim **8**, wherein the forming the gate structure comprises:

forming a gate dielectric on sidewalls of the gate spacers, on sidewalls of the barrier layer, and on the uppermost surface of the channel layer; and

forming a gate conductor on the gate dielectric.

**11.** The method of claim **10**, wherein the gate dielectric layer has a dielectric constant greater than approximately 4.0.

**12.** The method of claim **8**, further comprising forming an undoped region between the lowermost surface of the gate structure and the uppermost surface of the channel layer.

**13.** The method of claim **8**, wherein the forming a doped contact layer comprises doping the doped contact layer with a p-type or n-type dopant from Group II or Group IV of the Periodic Table of Elements.