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(54) **SEMICONDUCTOR DEVICE WITH LOW-CONDUCTING BURIED AND/OR SURFACE LAYERS**

(71) Applicant: **Sensor Electronic Technology, Inc.**, Columbia, SC (US)

(72) Inventors: **Grigory Simin**, Columbia, SC (US); **Michael Shur**, Latham, NY (US); **Remigijus Gaska**, Columbia, SC (US)

(73) Assignee: **Sensor Electronic Technology, Inc.**, Columbia, SC (US)

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CPC ***H01L 29/78*** (2013.01); ***G06F 17/5068*** (2013.01); ***H01L 29/1608*** (2013.01); ***H01L 29/408*** (2013.01); ***H01L 29/423*** (2013.01); ***H01L 29/7786*** (2013.01); ***H01L 29/1075*** (2013.01); ***H01L 29/1079*** (2013.01); *H01L 29/2003* (2013.01)
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See application file for complete search history.

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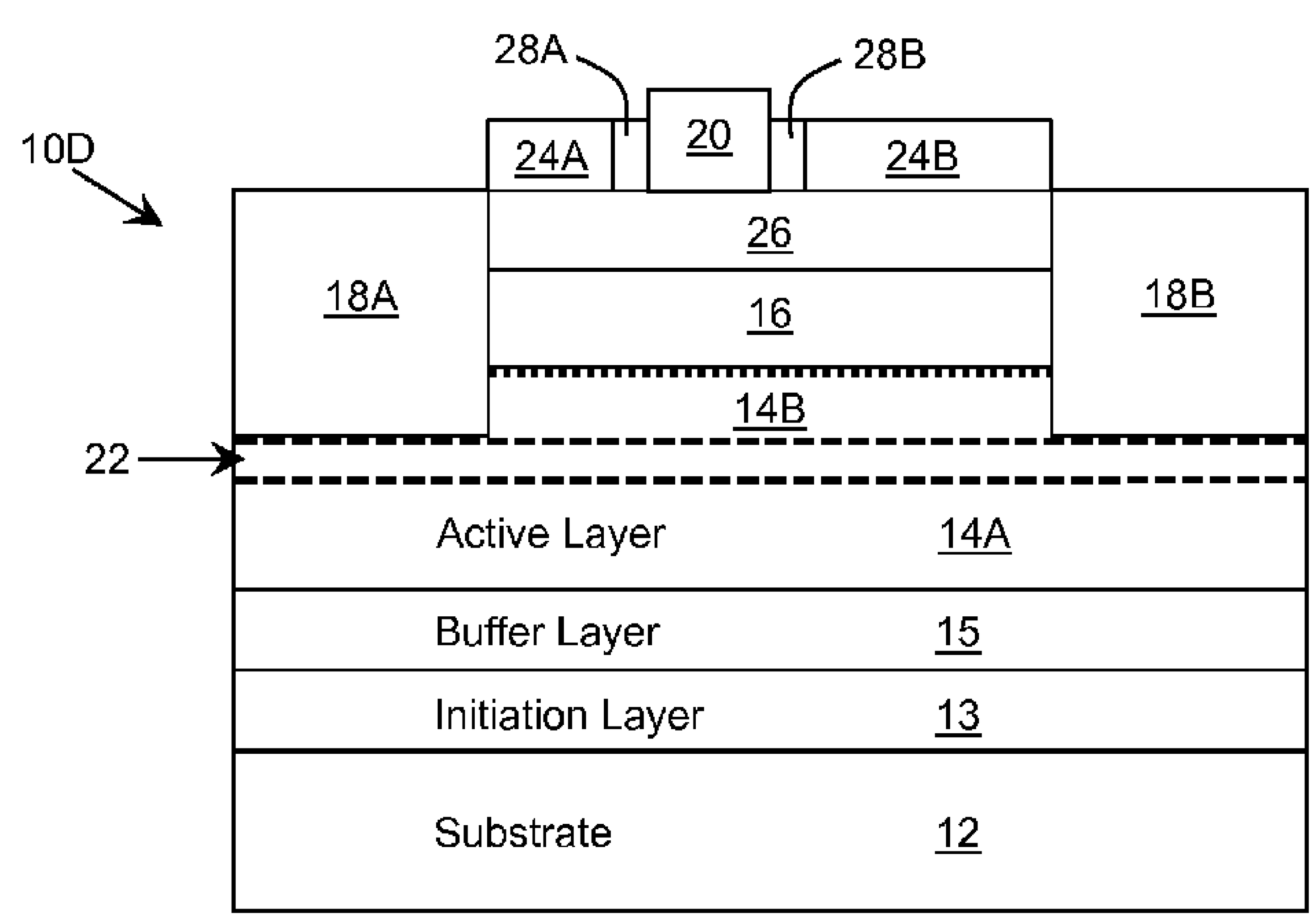
Primary Examiner — Cathy N Lam
(74) *Attorney, Agent, or Firm* — LaBatt, LLC

(57) **ABSTRACT**

A device including one or more low-conducting layers is provided. A low-conducting layer can be located below the channel and one or more attributes of the low-conducting layer can be configured based on a minimum target operating frequency of the device and a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer or a maximum interfering frequency targeted for suppression using the low-conducting layer. For example, a product of the lateral resistance and a capacitance between the low-conducting layer and the channel can be configured to be larger than an inverse of the minimum target operating frequency and the product can be smaller than at least one of: the charge-discharge time or an inverse of the maximum interfering frequency.

20 Claims, 7 Drawing Sheets



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H01L 29/423	(2006.01)
H01L 29/778	(2006.01)
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H01L 29/20	(2006.01)

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FIG. 1A
Prior Art

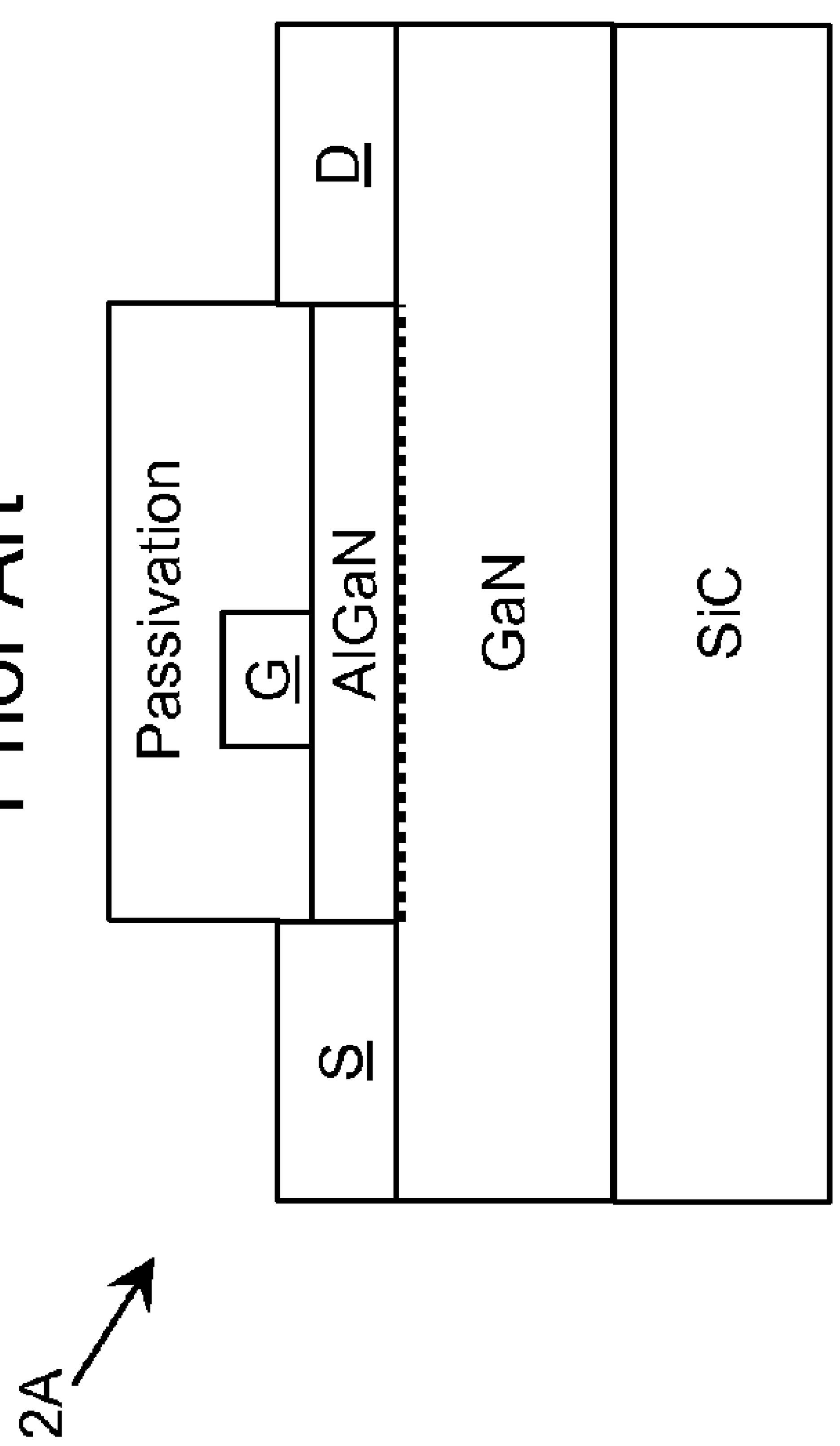


FIG. 1B
Prior Art

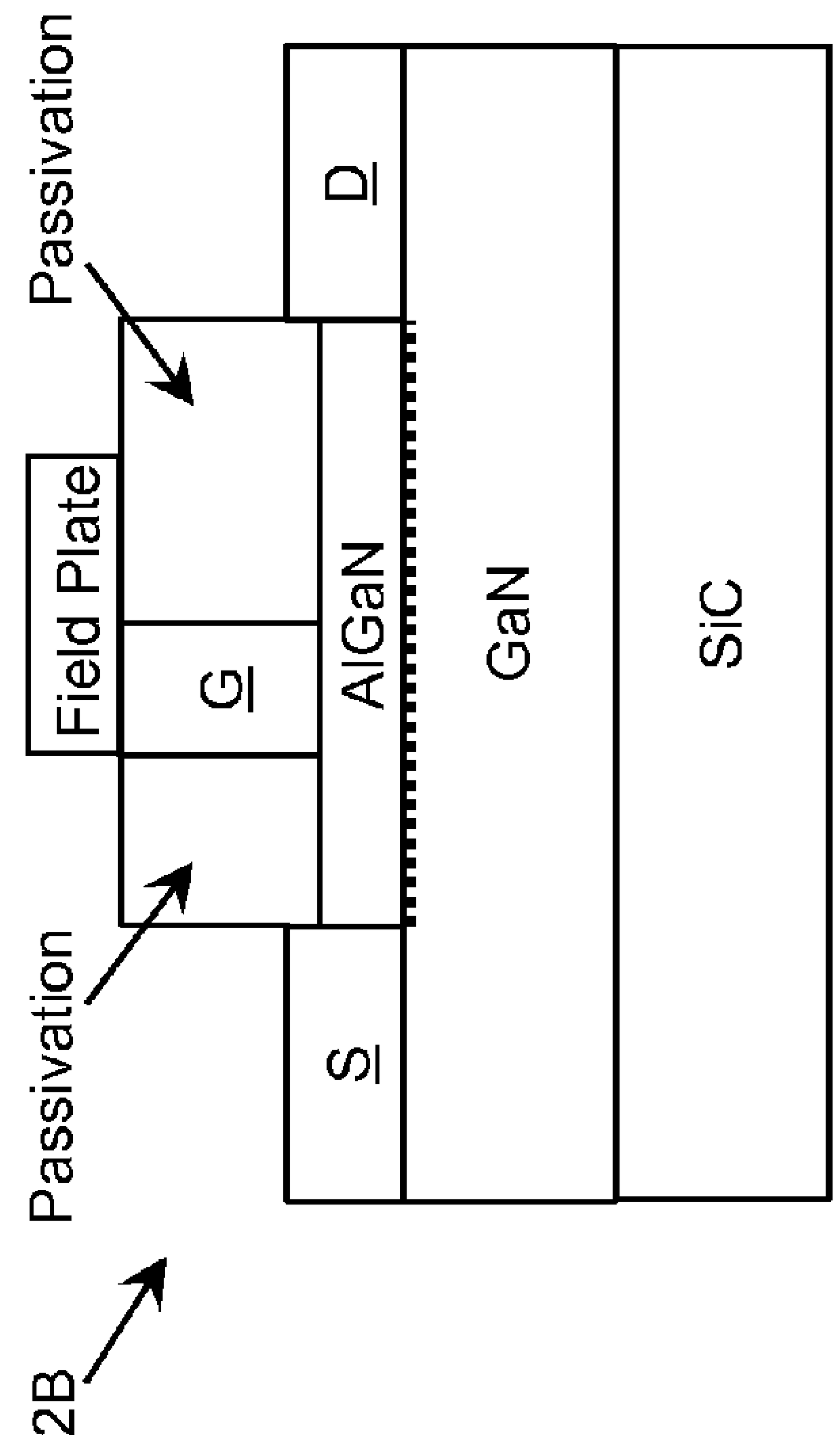


FIG. 2

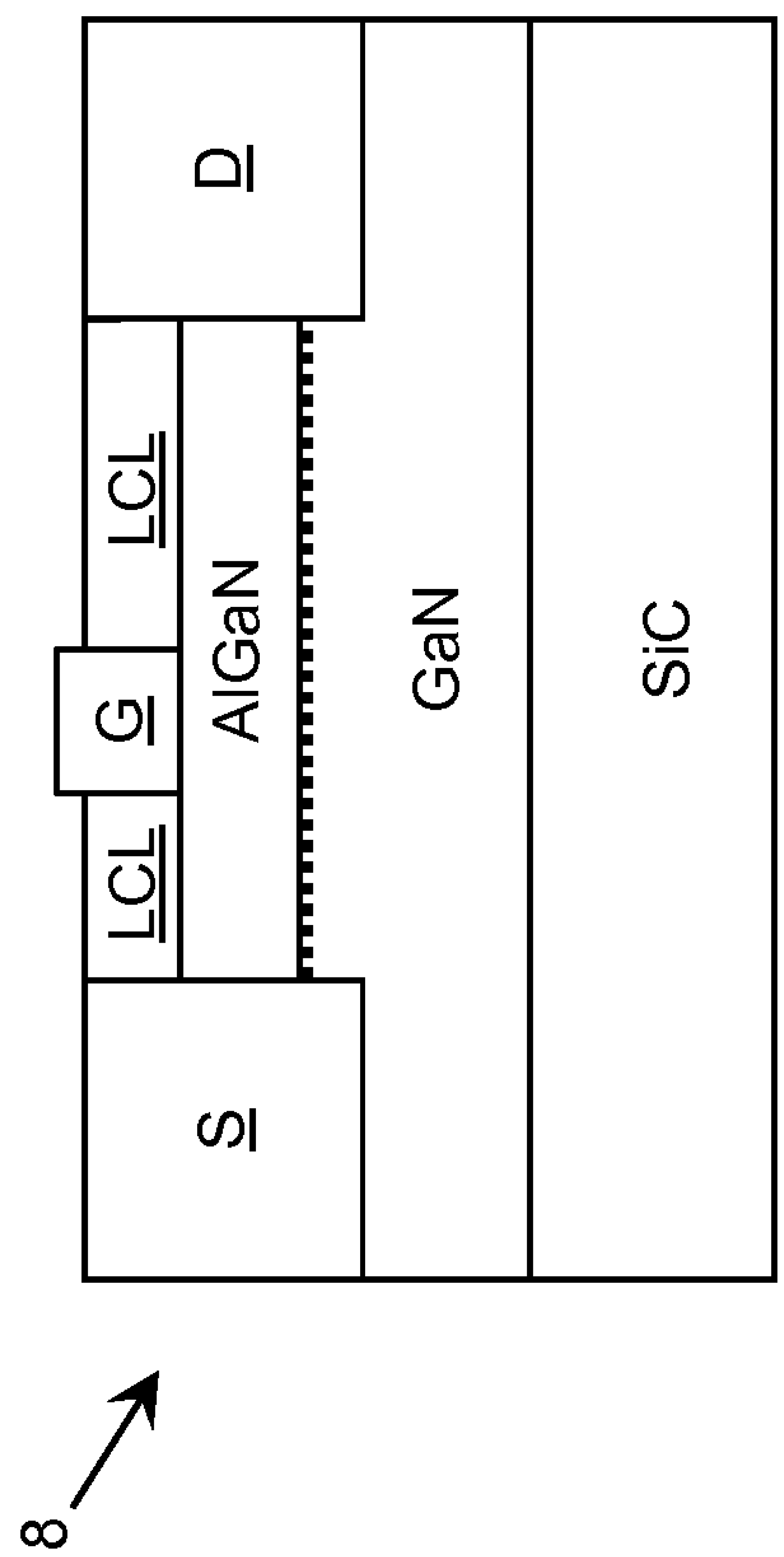


FIG. 3A

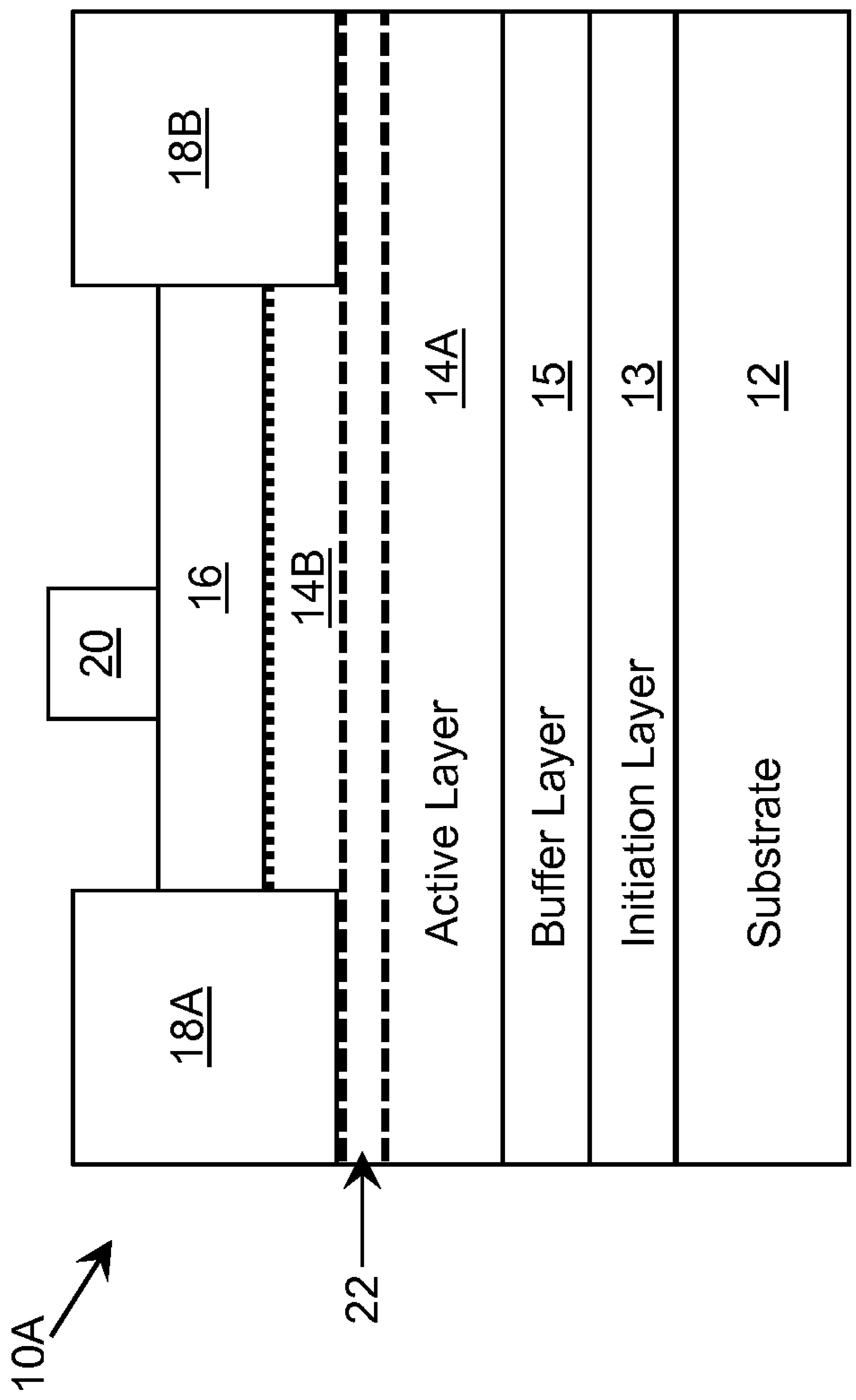

10A
22
18A
18B
20
16
14B
Active Layer
14A
Buffer Layer
15
Initiation Layer
13
Substrate
12

FIG. 3B

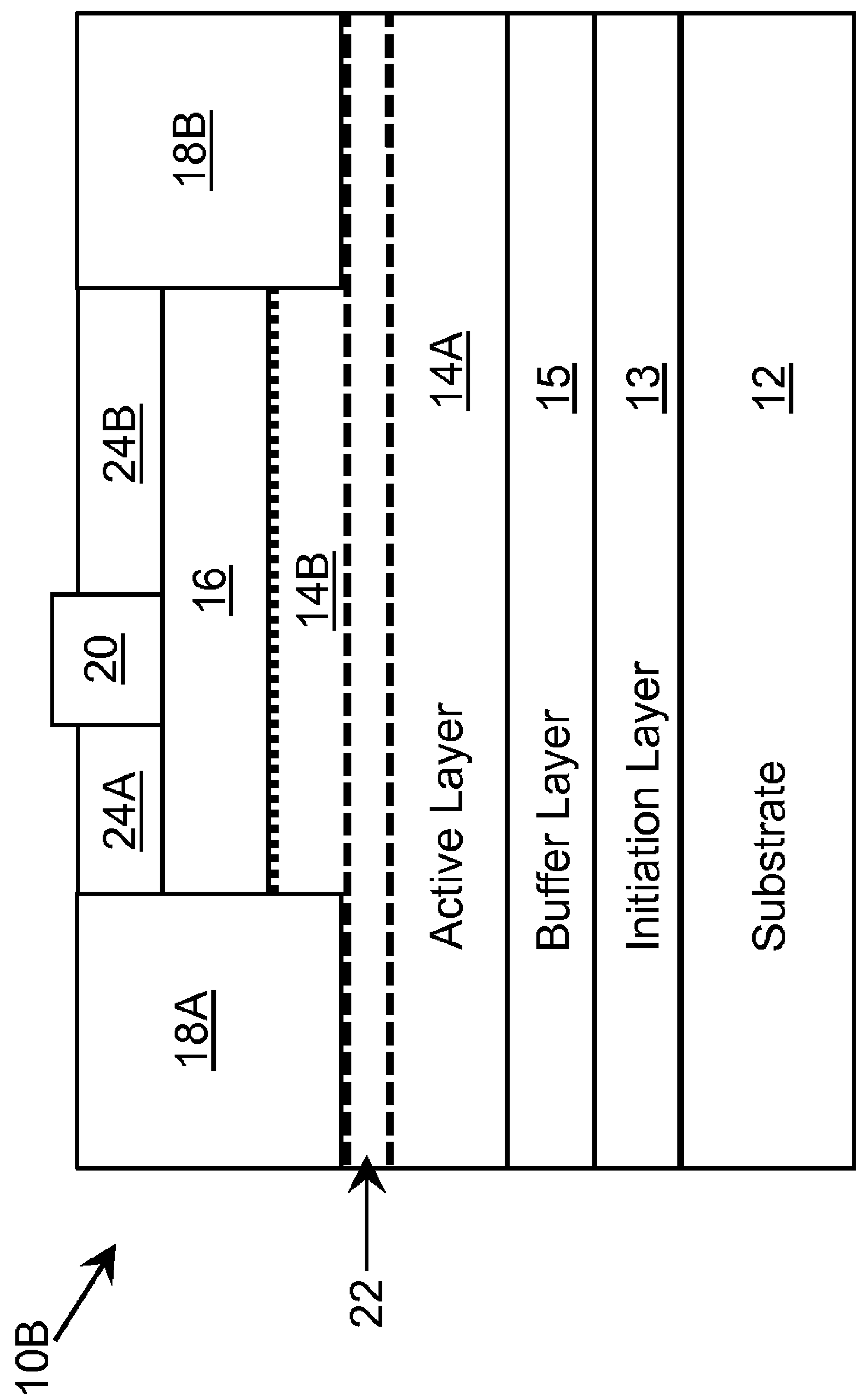

10B
22
18A
18B
24A
20
24B
16
14B
Active Layer
14A
Buffer Layer
15
Initiation Layer
13
Substrate
12

FIG. 3C

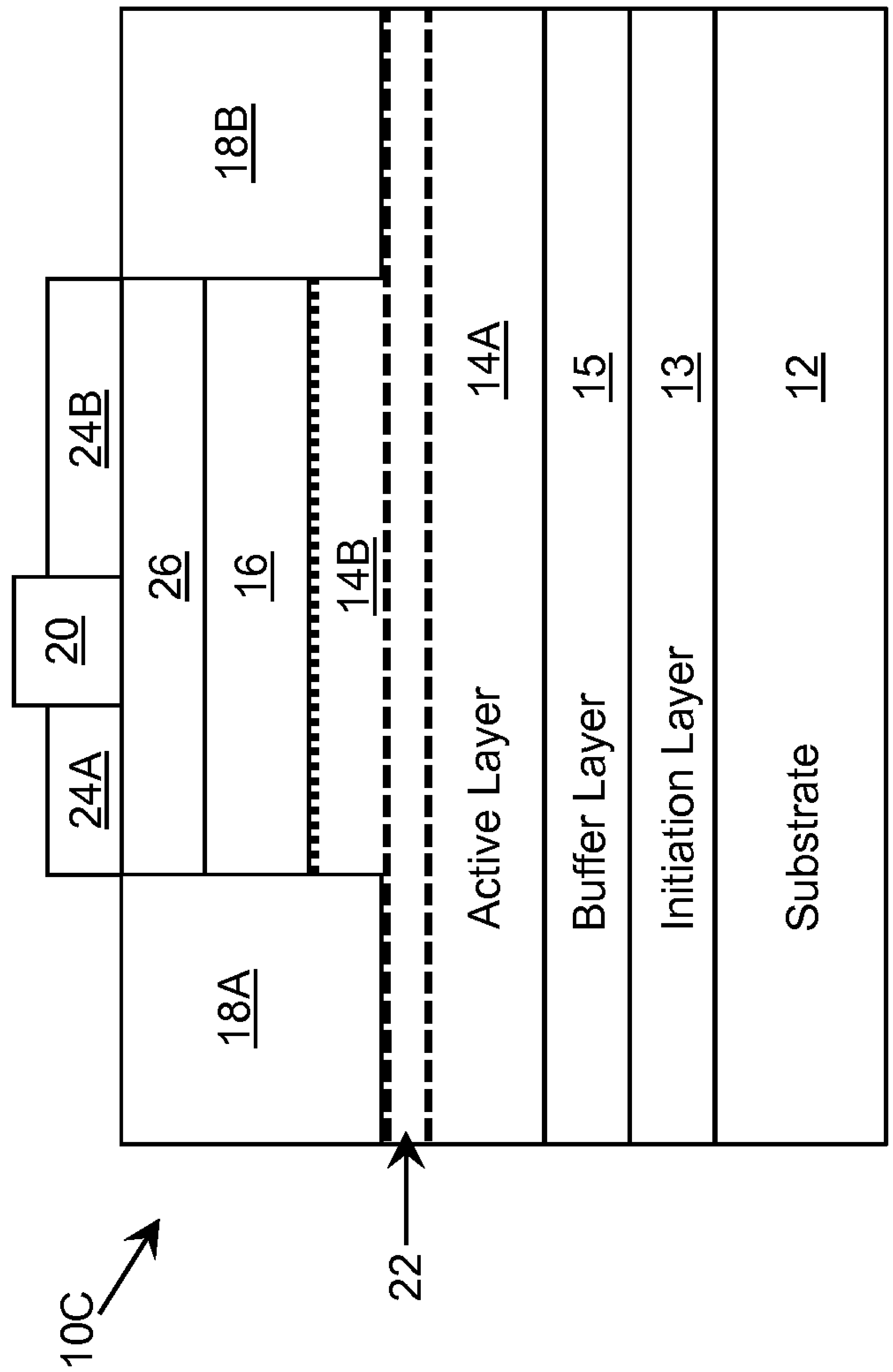
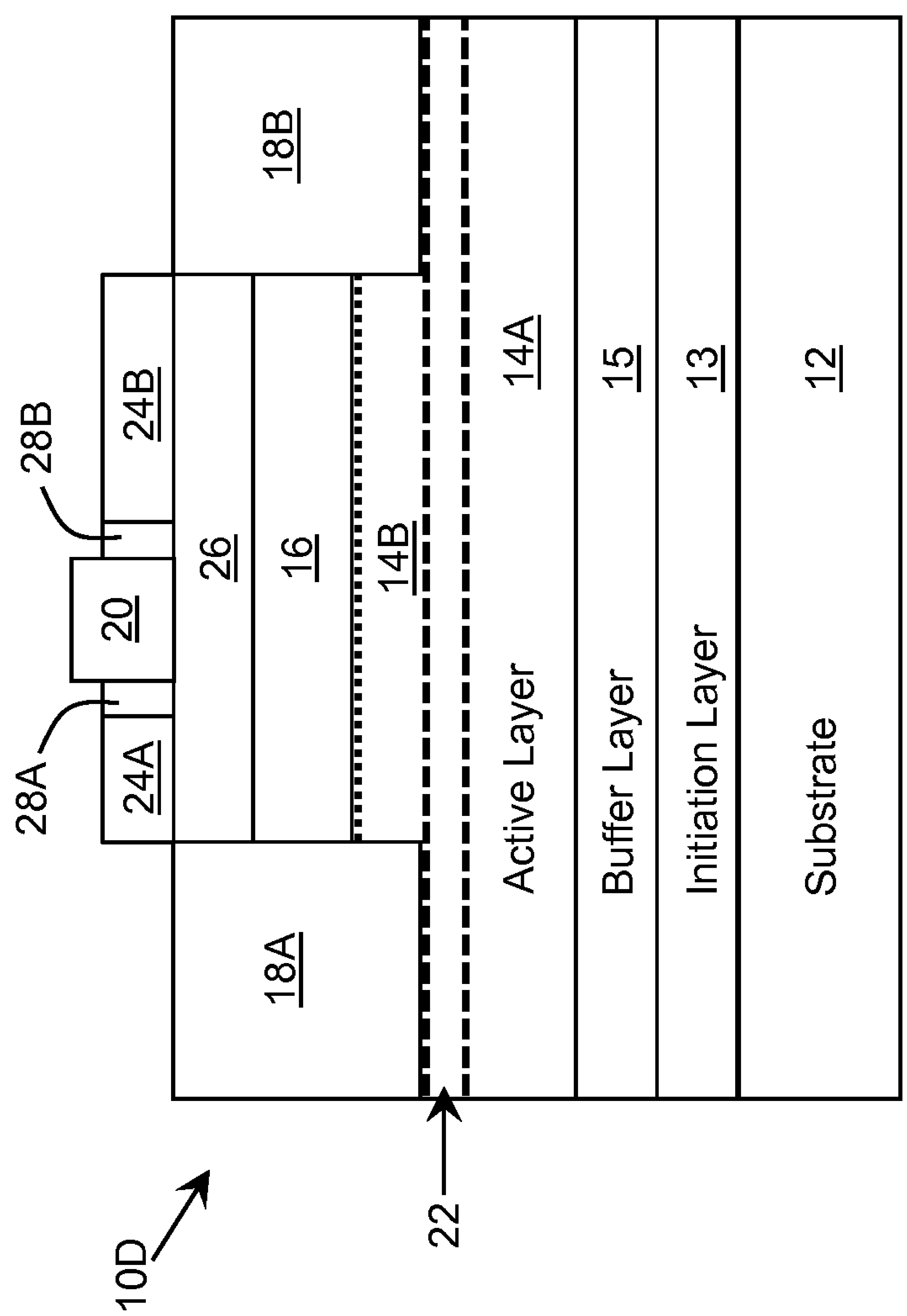
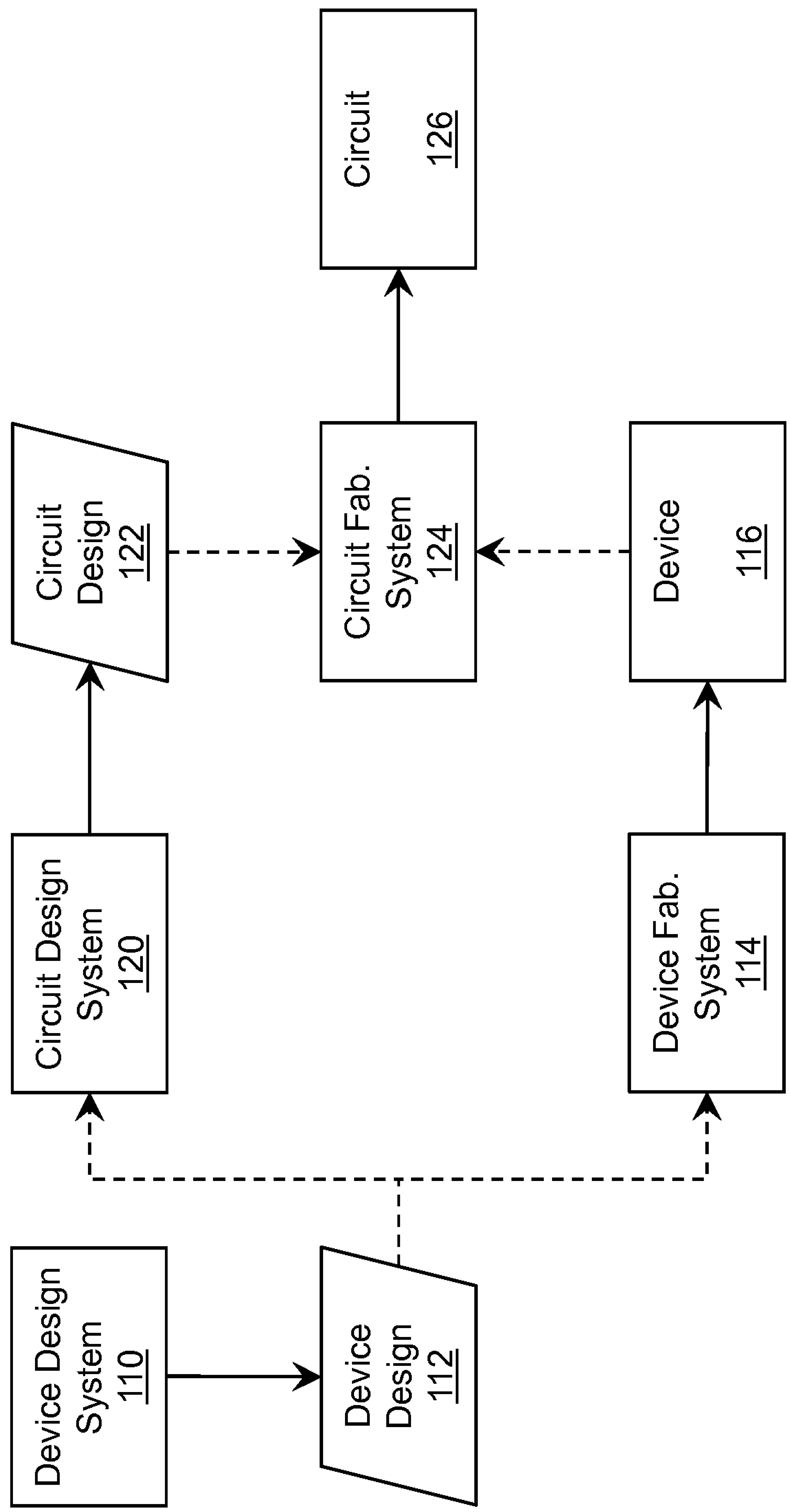

10C
22
18A
24A
20
24B
18B
26
16
14B
14A
Active Layer
15
Buffer Layer
13
Initiation Layer
12
Substrate

FIG. 3D



10D
22
18A
18B
24A
24B
28A
28B
20
26
16
14B
Active Layer
14A
Buffer Layer
15
Initiation Layer
13
Substrate
12

FIG. 4


Device Design System 110
Device Design 112
Circuit Design System 120
Device Fab. System 114
Circuit Design 122
Device 116
Circuit Fab. System 124
Circuit 126

SEMICONDUCTOR DEVICE WITH LOW-CONDUCTING BURIED AND/OR SURFACE LAYERS

REFERENCE TO RELATED APPLICATIONS

The current application claims the benefit of U.S. Provisional Application No. 61/561,989, titled "Semiconductor Device with Low-Conducting Buried and Surface Layers," which was filed on 21 Nov. 2011, and which is hereby incorporated by reference. Aspects of the current application also are related to U.S. patent application Ser. No. 13/396,059, titled "Semiconductor Device with Low-Conducting Field-controlling Element," which was filed on 14 Feb. 2012, and U.S. patent application Ser. No. 13/604,984, titled "Semiconductor Device with Low-Conducting Field-controlling Element," which was filed on 6 Sep. 2012, both of which are hereby incorporated by reference.

TECHNICAL FIELD

The disclosure relates generally to semiconductor devices, and more particularly, to a semiconductor device including one or more low-conducting layers.

BACKGROUND ART

The trapping of mobile carriers, i.e., electrons and holes, reduces the peak current, maximum operating frequency, microwave power, and efficiency of a semiconductor device. In many semiconductor devices, particularly in those made of wide bandgap materials such as gallium nitride (GaN), gallium phosphide (GaP), gallium arsenide (GaAs), indium phosphide (InP), and/or the like, mobile carrier trapping occurs due to the presence of various types of defects. Mobile carrier trapping can occur in the bulk of the material as well as at the device surface. Trapping occurring at the device surface is important in lateral devices, such as field effect transistors (FETs) having an active channel located close to the device surface.

Noise and interference are related issues that can affect the performance of a semiconductor device. Such noise and interference can be caused by a surface potential modulation occurring due to noise sources, industrial equipment, power lines, etc.

FIGS. **1**A and **1**B show illustrative heterostructure field effect transistors (HFETs) **2**A and **2**B, respectively, according to the prior art. In the HFET **2**A, the active heterostructure is passivated using a passivation layer included over the gate G and covering an entire spacing between the source S and drain D. In the HFET **2**B, a field plate electrically connected to the gate G is also included above the passivation layer. Various alternative configurations are possible. For example, an HFET can include several field plates connected to different electrodes. In each case, the surface element(s) are included to alleviate mobile carrier trapping and/or noise and interference.

SUMMARY OF THE INVENTION

Aspects of the invention provide a device including one or more low-conducting layers. A low-conducting layer can be located below the channel and one or more attributes of the low-conducting layer can be configured based on a minimum target operating frequency of the device and a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer or a maximum interfering frequency

targeted for suppression using the low-conducting layer. For example, a product of the lateral resistance and a capacitance between the low-conducting layer and the channel can be configured to be larger than an inverse of the minimum target operating frequency and the product can be smaller than at least one of: the charge-discharge time or an inverse of the maximum interfering frequency.

A first aspect of the invention provides a device comprising: a semiconductor structure including a channel; a set of contacts to the channel; and a set of buried low-conducting layers located below the channel in the semiconductor structure, wherein, for each buried low-conducting layer in the set of buried low-conducting layers, a product of a lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer.

A second aspect of the invention provides a field-effect transistor comprising: a source contact, a drain contact, and a device channel there between; a gate located on a surface side of the device channel; and a set of buried low-conducting layers located on a side opposite the surface side of the device channel, wherein, for each buried low-conducting layer in the set of buried low-conducting layers, a product of a lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer.

A third aspect of the invention provides a method comprising: designing a semiconductor device including a channel, a set of contacts to the channel, and a set of buried low-conducting layers located below the channel in the semiconductor structure, wherein the designing the semiconductor device includes: determining a minimum target operating frequency of the device; and for each buried low-conducting layer in the set of buried low-conducting layers, determining a target lateral resistance for the buried low-conducting layer such that a product of the target lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer; and designing each buried low-conducting layer in the set of buried low-conducting layers based on the corresponding target lateral resistance.

The illustrative aspects of the invention are designed to solve one or more of the problems herein described and/or one or more other problems not discussed.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the disclosure will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various aspects of the invention.

FIGS. **1**A and **1**B show illustrative heterostructure field effect transistors according to the prior art.

FIG. **2** shows an illustrative device according to a previously disclosed solution.

FIGS. **3**A-**3**D show illustrative semiconductor devices according to embodiments.

FIG. **4** shows an illustrative flow diagram for fabricating a circuit according to an embodiment.

It is noted that the drawings may not be to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

In previously disclosed solutions described in U.S. patent application Ser. No. 13/396,059 and U.S. patent application Ser. No. 13/604,984, the inventors describe the use of one or more surface layers of low-conducting field-controlling elements. For example, FIG. **2** shows an illustrative device **8** according to the previously disclosed solution. In the device **8**, a set of low-conducting layers LCL is included, which includes one or more layers electrically connected to the gate G as well as the source S and/or the drain D. In the previously disclosed solution, the low-conducting field-controlling elements are configured based on a minimal operating frequency of the device and an inverse of a maximum control frequency of the device. During operation of the device **8**, the set of low-conducting layers LCL can serve as a conduction path to remove trapped charges, and therefore reduce the gate G and/or drain D lags, which can be observed in group III nitride HFETs and other types of devices.

As indicated above, aspects of the invention provide a device including one or more low-conducting layers. A low-conducting layer can be located below the channel and one or more attributes of the low-conducting layer can be configured based on a minimum target operating frequency of the device and a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer or a maximum interfering frequency targeted for suppression using the low-conducting layer. For example, a product of the lateral resistance and a capacitance between the low-conducting layer and the channel can be configured to be larger than an inverse of the minimum target operating frequency and the product can be smaller than at least one of: the charge-discharge time or an inverse of the maximum interfering frequency. As used herein, unless otherwise noted, the term “set” means one or more (i.e., at least one) and the phrase “any solution” means any now known or later developed solution.

Returning to the drawings, FIGS. **3**A-**3**D show illustrative semiconductor devices **10**A-**10**D, respectively, according to embodiments. Each device **10**A-**10**D is shown including a substrate **12**, an active layer **14**A, **14**B, a barrier layer **16**, a source contact **18**A, a drain contact **18**B, and a gate **20**, each of which can be manufactured and fabricated using any solution. The substrate **12** can be formed of any of various types of compound semiconductor or dielectric materials, including for example, sapphire, diamond, germanium (Ge), gallium nitride (GaN), silicon, silicon carbide (SiC), gallium arsenic (GaAs), and/or the like. Furthermore, the substrate **12** can comprise a conducting and/or semiconducting substrate.

As illustrated, an initiation layer **13** and a buffer layer **15** can be located between the substrate **12** and the active layer **14**. However, it is understood that this is only illustrative of various possible configurations, each of which can include or not include the initiation layer **13** and/or the buffer layer **15**. Similarly, a device **10**A-**10**D can include one or more additional layers, which are not shown. Regardless, the heterostructure of a device **10**A-**10**D can include various layers made from any of a plurality of materials systems. Furthermore, one or more of the layers in a heterostructure described herein can include one or more attributes to alleviate strain. For example, a layer can be formed of a superlattice structure.

In an embodiment, the substrate **12** is formed of SiC, the active layer **14** is formed of gallium nitride (GaN), and the barrier layer **16** is formed of aluminum gallium nitride (AlGaN). However, it is understood that this is only illustrative of various possible group III nitride based devices. To this extent, layers **13**, **14**, **15**, **16** can be formed of any combination of various types of group III nitride materials comprising one or more group III elements (e.g., boron (B), aluminum (Al), gallium (Ga), and indium (In)) and nitrogen (N), such that $B_WAl_XGa_YIn_ZN$, where $0 \leq W, X, Y, Z \leq 1$, and $W+X+Y+Z=1$. Illustrative group III nitride materials include AlN, GaN, InN, BN, AlGaN, AlInN, AlBN, InGaN, AlGaInN, AlGaBN, AlInBN, and AlGaInBN with any molar fraction of group III elements. Furthermore, it is understood that a device **10**A-**10**D can be formed from other semiconductor materials, including other types of group III-V materials, such as such as GaAs, GaAlAs, InGaAs, indium phosphorus (InP), and/or the like.

Additionally, each device **10**A-**10**D is shown including a buried low-conducting layer **22**. The buried low-conducting layer **22** is located below the active region (e.g., a device channel formed at an interface of the active layer **14**B and the barrier layer **16**) within the device epitaxial structure in a vicinity of the device channel, e.g., within a channel space-charge region (generally within a distance of ten nanometers to one micrometer from the device active region). As illustrated, the buried low-conducting layer **22** can extend under all of the active region. However, it is understood that the buried low-conducting layer **22** also can only extend under a portion of the active region. Similarly, a device **10**A-**10**D can include any combination of multiple buried low-conducting layers, each of which is located under a portion of the active region. The buried low-conducting layer **22** can be electrically connected and/or capacitively coupled to one or more of the device contacts.

A resistivity of the buried low-conducting layer **22** can be designed such that a characteristic time constant of the buried low-conducting layer **22** is lower than that of a trapped charge, but much higher than a period of a signal corresponding to a lowest target operating frequency for the device **10**A-**10**D. In this manner, the buried low-conducting layer **22** can have a minimal effect on the operating frequency of the device, while being capable of removing the trapped charge. Such a configuration can be beneficial, for example, in group III nitride and other semiconductor materials in which a significant amount of carriers may be trapped in the buffer layer **15** of the device heterostructure.

Devices **10**B-**10**D also are shown including a set of surface low-conducting layers (e.g., field-controlling elements) **24**A, **24**B. As illustrated, a device **10**B-**10**D can include a surface low-conducting layer **24**A located in the surface region between the source contact **18**A and the gate **20** (gate-source region), and a surface low-conducting layer **24**B located in the surface region between the gate **20** and the drain contact **18**B (gate-drain region) of the device **10**B-**10**D. However, it is understood that a device can include one or more surface low-conducting layers **24**A, **24**B located in any combination of one or more of: the gate-source region; the gate-drain region; the source-drain region; and/or the like. Furthermore, a device can include a low-conducting layer that forms an additional contact or passivation layer. To this extent, a low-conducting layer with low surface conductivity as described herein can be used in addition to or instead of regular metal electrodes.

An embodiment of a device can comprise an insulated gate configuration. To this extent, devices **10**C, **10**D also are shown including a gate insulating layer **26** located between the gate **20** and the barrier layer **16**. As illustrated, the gate insulating layer **26** can extend across the entire region between the source contact **18**A and the drain contact **18**B. In this case, the low-conducting layers **24**A, **24**B also can be located on the gate insulating layer **26**. Furthermore, the gate **20** also can be insulated from one or more of the low-conducting layers **24**A, **24**B. For example, the device **10**D is shown including gate insulating walls **28**A, **28**B, each of which isolates the gate **20** from a corresponding low-conducting layer **24**A, **24**B, respectively. The insulating layers **26**, **28**A, **28**B can be formed of any type of insulating material, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), and/or the like.

It is understood that the various device configurations shown herein are only illustrative of numerous device configurations possible. To this extent, a device can include more or fewer layers having any of various configurations. For example, a device can include an isolation layer and/or a passivation layer over some or all of the surface of the structure. Additionally, it is understood that the low-conducting layers **22**, **24**A-**24**B described herein can be implemented in various types of field-effect transistors, including, for example, a field-effect transistor, a heterostructure field-effect transistor, an insulated gate field-effect transistor, an insulated gate heterostructure field-effect transistor, a multiple heterostructure field-effect transistor, a multiple heterostructure insulated gate field-effect transistor, an inverted field-effect transistor, an inverted heterostructure field-effect transistor, an inverted insulated gate field-effect transistor, an inverted insulated gate heterostructure field-effect transistor, an inverted multiple heterostructure field-effect transistor, an inverted insulated gate multiple heterostructure field-effect transistor, and/or the like. Additionally, the low-conducting layer(s) can be implemented in other types of semiconductor devices, including for example, a diode of any type, a semiconductor resistor, a semiconductor sensor, a light emitting diode, a laser, an integrated element, and/or the like.

In any event, each low-conducting layer **22**, **24**A-**24**B can be formed of a layer of any type of low-conducting material. The low-conducting material can have a surface resistance that is significantly higher than that of metal electrodes, but is also much lower than that of a dielectric material. Similarly, the low-conducting material can have a surface conductivity that is significantly lower than that of metal electrodes, but is also much higher than that of a dielectric material. As a result, the associated characteristic charging-recharging time of the low-conducting layer **22**, **24**A-**24**B is much higher than that of metal electrodes. To this extent, during operation of a device **10**A-**10**D at DC or low frequencies (e.g., below 10 megahertz (MHz)), typically used for pulse or sinusoidal modulation, the low-conducting layers **22**, **24**A-**24**B will behave similar to metal electrodes. However, during operation of the device **10**A-**10**D at high (signal) frequencies, (e.g., typically exceeding 100 MHz) the low-conducting layers **22**, **24**A-**24**B will behave similar to an insulator, thereby not deteriorating the device frequency performance. Illustrative low-conducting materials include, for example: InGaN; a semiconductor; a low-conducting dielectric single crystal; a textured, poly-crystalline or amorphous material; a semi-metal material; oxides of nickel and other metals; composite materials, such as aluminum oxide with embedded platinum; and/or the like.

As described herein, in an embodiment, it is desired for each low-conducting layer **22**, **24**A-**24**B to act as a conductor (e.g., electrode) when the corresponding device **10**A-**10**D is operating at low frequencies. The low frequencies can correspond to, for example, an inverse of the characteristic carrier trapping/de-trapping times, a frequency at which interfering (e.g., noise, interference, and/or the like) signals occur, a highest frequency at which the interfering signals should be suppressed, and/or the like. However, within a target device operating frequency range, which includes much higher frequencies (e.g., at least ten times higher) than the low frequencies, each low-conducting layer **22**, **24**A-**24**B can act as a dielectric, thereby making only a minor increase in the total electrode area and, as a result, in the device capacitance.

In an embodiment, the design and configuration of each low-conducting layer **22**, **24**A-**24**B accounts for the characteristic charging-discharging time of the low-conducting layer **22**, **24**A-**24**B. For example, contrary to other approaches, the design and configuration of the low-conducting layer **22**, **24**A-**24**B identifies a range of acceptable lateral and/or sheet resistances/conductances and/or a target lateral and/or sheet resistance/conductance for a set of low-conducting layers **22**, **24**A-**24**B included in a device **10**A-**10**D based on a target operating frequency (e.g., a minimal operating frequency), a characteristic charge-discharge time of a trapped charge targeted for removal, a frequency targeted for suppression (e.g., interfering frequency), and/or the like. In a more particular example, a low-conducting layer **22**, **24**A-**24**B is configured to have a sheet conductivity such that an associated characteristic charging-discharging time of the low-conducting layer **22**, **24**A-**24**B is much (e.g., at least ten times) higher than an inverse of the minimal target operating frequency and much (e.g., at least ten times) lower than a characteristic charge-discharge time of the trapped charge targeted for removal and/or an inverse of the maximum interfering frequency targeted for suppression. When a low-conducting layer **22**, **24**A-**24**B is configured in such a manner, the low-conducting layer **22**, **24**A-**24**B can normally behave as a conducting layer at direct current or low frequencies, but as an insulator within a target device operating frequency range, therefore not deteriorating the device frequency performance.

The following discussion provides a theoretical basis for determining an illustrative set of attributes of the device **10**A-**10**D and the low-conducting layer **22**, **24**A-**24**B as currently understood by the inventors. As discussed herein, depending on a target function, the low-conducting layer **22**, **24**A, **24**B can be located in the gate-source, gate-drain, or source-drain spacing, form an additional contact or passivation layer, be formed on a surface of the heterostructure or buried within the heterostructure, and/or the like. The following description uses a low-conducting layer located in the source-drain region of a group III-nitride based HFET as an illustrative example.

In order for the low-conducting layer to not significantly affect a radio frequency (RF) performance (e.g., impedance) of the device, a corresponding time constant for the low-conducting layer, τ_{LC}, must be much larger than $1/(2\pi f)$, where f is the target operating frequency for the device. The time constant for the low-conducting layer can be expressed as $\tau_{LC}=R_{LC}C_{LC}$, where R_{LC} is the lateral resistance of the low-conducting layer measured in a direction of the current flow in the device along the surface of the low-conducting layer and C_{LC} is the total capacitance between the low-conducting layer and the device channel. This yields the following condition:

$$\tau_{LC}=R_{LC}C_{LC}>>1/(2\pi f) \quad (1)$$

Assuming τ_{LC} is at least approximately six times (2π times) greater than 1/(2πf), the condition (1) can be rewritten as:

$$\tau_{LC}=R_{LC}C_{LC}>1/f \quad (2)$$

As used herein, the lateral resistance of the low-conducting layer, R_{LC}, is related to the low-conducting layer sheet resistance, R_{LCSH}, as:

$$R_{LC}=R_{LCSH}*L/W \quad (2a)$$

where L and W are the length and width, respectively, of the low-conducting layer with respect to a direction of the current flow in the device.

Furthermore, the low-conducting layer should be sufficiently fast to allow for de-trapping of trapped carriers and/or screening interfering signals. Assuming a maximum de-trapping or interfering frequency, f_C, and following the derivation that led to condition (2) above, the required τ_{LC} also should meet the following condition:

$$\tau_{LC}<1/f_C \quad (3)$$

As an example, for practical purposes and material selection, in order to meet both conditions (2) and (3), the value of the τ_{LC} can be selected as follows:

$$\tau_{LC}=1/(f\times f_C)^{1/2} \quad (4)$$

As an illustrative example, assume a field effect transistor has the following attributes: a source to drain distance, L=5 μm; a gate-channel separation (also equal to the surface low-conducting layer-channel separation), d=20 nm; a channel width, W=1 mm; a relative dielectric permittivity of the material between the low-conducting layer and the channel, $\in_r=9$; a target operating frequency, f=1 GHz; a characteristic carrier trapping time $\tau_{TR}=0.16$ μs; and a corresponding de-trapping frequency $f_C=1$ MHz. The low-conducting layer-channel capacitance can be calculated as, $C_{LC}=\in_0\in_r L*W/d\approx 20$ pF, where $\in_0$ is vacuum permittivity. From equation (2), the low-conducting layer resistance $R_{LC}=\tau_{LC}/C_{LC}$.

Using the above-described attributes and equations, values for R_{LC} which provide the corresponding desired time constant for the low-conducting layer, τ_{LC}, can be derived. For example, τ_{LC} can be configured to be greater than an inverse of the target operating frequency, e.g., greater than 1/1 GHz and less than an inverse of the de-trapping frequency, e.g., less than 1/1 MHz. Solving for R_{LC}, the R_{LC} can be between $R_{LCMIN}=1.6$ kΩ/sq and $R_{LCMAX}=1.6$ MΩ/sq. As discussed herein, the τ_{LC} can be much larger than the inverse of the target operating frequency of the device and much smaller than the inverse of the de-trapping frequency. A target value of R_{LC} between the R_{LCMIN} and R_{LCMAX} values can be selected based on the application of the corresponding device. In an embodiment, a target (e.g., optimal) value for R_{LC}, R_{LC_OPT}, can be calculated using the formula: $R_{LC\_OPT}=\sqrt{R_{LCMIN} \cdot R_{LCMAX}}$. In this case, using the R_{LCMIN} and R_{LCMAX} calculated above, the target value for R_{LC} in the device described herein is approximately 50.6 kΩ/sq.

Inclusion of one or more low-conducting layers described herein can provide one or more improvements to the operation of the device. For example, inclusion of a low-conducting layer **24**B in the gate-drain spacing on the surface of the device **10**B-**10**D can remove surface trapped charges within that spacing. Furthermore, inclusion of a set of low-conducting layers **24**A, **24**B over substantially an entire source-drain spacing on the surface of the device **10**B-**10**D can remove the surface trapped charges as well as screen the active region from surface potential modulation caused by interfering sources. Additionally, inclusion of a buried low-conducting layer **22** can remove the bulk trapped charges in the corresponding region (e.g., across substantially an entire length of the channel) of the device **10**A-**10**D. As a result, a device **10**A-**10**D including one or more of the low-conducting layers **22**, **24**A-**24**B described herein can have an increased operating frequency, power, and/or efficiency over existing devices that do not include any low-conducting layers. Similarly, a device **10**A-**10**D including one or more of the low-conducting layers **22**, **24**A-**24**B described herein can be more resistant to interfering signals, the impact of which can be reduced due to the presence of one or more of the low-conducting layers **22**, **24**A-**24**B described herein.

One or more aspects of a semiconductor device described herein can be designed using any solution. For example, the materials, dimensions, layer structure, and/or the like, can be selected and configured according to a target set of device operating properties using any solution. As part of designing the semiconductor device, one or more low-conducting layers can be designed as described herein. For example, a minimum target operating frequency for the semiconductor device can be determined. Subsequently, a target lateral resistance for the low-conducting layer can be determined such that a product of the target lateral resistance and a capacitance between the low-conducting layer and the device channel is larger than an inverse of the minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the low-conducting layer. The low-conducting layer can then be designed based on the corresponding target lateral resistance, e.g., a material for the low-conducting layer can be selected to provide a lateral resistance approximately equal to the target lateral resistance.

It is understood that the various semiconductor devices described herein can be manufactured using any solution. For example, a device heterostructure can be formed using any solution, e.g., by obtaining (e.g., forming, preparing, acquiring, and/or the like) a substrate **12**, forming (e.g., growing, depositing, adhering, and/or the like) an initiation layer **13** and/or a buffer layer **15** thereon, forming an active layer **14** thereon, and forming a barrier layer **16** on the active layer **14**. Additionally, metal electrode(s), dielectric layer(s), and/or the like, can be formed on the device heterostructure using any solution. Furthermore, as described herein, the manufacture of the device can include the formation of one or more low-conducting layers using any solution. It is understood that the manufacture of a device described herein can include additional processing, including for example: the deposition and removal of a temporary layer, such as mask layer; the patterning one or more layers; the formation of one or more additional layers/contacts not shown; application to a submount (e.g., via contact pads); and/or the like.

While shown and described herein as a method of designing and/or fabricating a semiconductor device, it is understood that aspects of the invention further provide various alternative embodiments. For example, in one embodiment, the invention provides a method of designing and/or fabricating a circuit that includes one or more of the semiconductor devices designed and fabricated as described herein.

To this extent, FIG. **4** shows an illustrative flow diagram for fabricating a circuit **126** according to an embodiment. Initially, a user can utilize a device design system **110** to generate a device design **112** for a semiconductor device as described herein. The device design **112** can comprise program code, which can be used by a device fabrication system **114** to generate a set of physical devices **116** according to the features defined by the device design **112**. Similarly, the device design **112** can be provided to a circuit design system **120** (e.g., as an available component for use in circuits), which a user can utilize to generate a circuit design **122** (e.g., by connecting one or more inputs and outputs to various devices included in a circuit). The circuit design **122** can comprise program code that includes a device designed as described herein. In any event, the circuit design **122** and/or one or more physical devices **116** can be provided to a circuit fabrication system **124**, which can generate a physical circuit **126** according to the circuit design **122**. The physical circuit **126** can include one or more devices **116** designed as described herein.

In another embodiment, the invention provides a device design system **110** for designing and/or a device fabrication system **114** for fabricating a semiconductor device **116** as described herein. In this case, the system **110**, **114** can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the semiconductor device **116** as described herein. Similarly, an embodiment of the invention provides a circuit design system **120** for designing and/or a circuit fabrication system **124** for fabricating a circuit **126** that includes at least one device **116** designed and/or fabricated as described herein. In this case, the system **120**, **124** can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the circuit **126** including at least one semiconductor device **116** as described herein.

In still another embodiment, the invention provides a computer program fixed in at least one computer-readable medium, which when executed, enables a computer system to implement a method of designing and/or fabricating a semiconductor device as described herein. For example, the computer program can enable the device design system **110** to generate the device design **112** as described herein. To this extent, the computer-readable medium includes program code, which implements some or all of a process described herein when executed by the computer system. It is understood that the term "computer-readable medium" comprises one or more of any type of tangible medium of expression, now known or later developed, from which a stored copy of the program code can be perceived, reproduced, or otherwise communicated by a computing device.

In another embodiment, the invention provides a method of providing a copy of program code, which implements some or all of a process described herein when executed by a computer system. In this case, a computer system can process a copy of the program code to generate and transmit, for reception at a second, distinct location, a set of data signals that has one or more of its characteristics set and/or changed in such a manner as to encode a copy of the program code in the set of data signals. Similarly, an embodiment of the invention provides a method of acquiring a copy of program code that implements some or all of a process described herein, which includes a computer system receiving the set of data signals described herein, and translating the set of data signals into a copy of the computer program fixed in at least one computer-readable medium. In either case, the set of data signals can be transmitted/received using any type of communications link.

In still another embodiment, the invention provides a method of generating a device design system **110** for designing and/or a device fabrication system **114** for fabricating a semiconductor device as described herein. In this case, a computer system can be obtained (e.g., created, maintained, made available, etc.) and one or more components for performing a process described herein can be obtained (e.g., created, purchased, used, modified, etc.) and deployed to the computer system. To this extent, the deployment can comprise one or more of: (1) installing program code on a computing device; (2) adding one or more computing and/or I/O devices to the computer system; (3) incorporating and/or modifying the computer system to enable it to perform a process described herein; and/or the like.

The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to an individual in the art are included within the scope of the invention as defined by the accompanying claims.

What is claimed is:

1. A device comprising:

a semiconductor structure including a channel;

a set of contacts to the channel; and

a set of buried low-conducting layers located below the channel in the semiconductor structure, wherein, for each buried low-conducting layer in the set of buried low-conducting layers, a product of a lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer.

2. The device of claim **1**, wherein each buried low-conducting layer in the set of buried low-conducting layers is formed of one of: a semiconductor material; a semimetal material; or a dielectric material.

3. The device of claim **1**, further comprising a set of surface low-conducting layers located above the channel, wherein, for each surface low-conducting layer in the set of surface low-conducting layers, a product of a lateral resistance of the surface low-conducting layer and a capacitance between the surface low-conducting layer and the channel is larger than the inverse of the minimum target operating frequency of the device and the product of the lateral resistance of the surface low-conducting layer and the capacitance between the surface low-conducting layer and the channel is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the surface low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the surface low-conducting layer.

4. The device of claim **3**, wherein each of the set of buried low-conducting layers and the set of surface low-conducting layers covers substantially all of an area corresponding to the channel.

5. The device of claim **3**, wherein at least one of the set of surface low-conducting layers is at least partially isolated from the semiconductor by an isolation layer having a sheet resistance at least an order of magnitude higher than a sheet resistance of the at least one of the set of surface low-conducting layers.

6. The device of claim 1, wherein at least one of the set of buried low-conducting layers forms at least one of: a passivation layer or a strain relieving layer.

7. The device of claim 1, wherein the semiconductor is formed of one of: silicon, silicon carbide, or a group III-V material.

8. The device of claim 1, wherein the semiconductor is formed of a group III nitride material.

9. The device of claim 1, wherein the device is configured to operate as a field-effect transistor.

10. A field-effect transistor comprising:

a source contact, a drain contact, and a device channel there between;

a gate located on a surface side of the device channel; and

a set of buried low-conducting layers located on a side opposite the surface side of the device channel, wherein, for each buried low-conducting layer in the set of buried low-conducting layers, a product of a lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer.

11. The transistor of claim 10, wherein each buried low-conducting layer in the set of buried low-conducting layers is formed of one of: a semiconductor material; a semimetal material; or a dielectric material.

12. The transistor of claim 10, further comprising a set of surface low-conducting layers located above the channel, wherein, for each surface low-conducting layer in the set of surface low-conducting layers, a product of a lateral resistance of the surface low-conducting layer and a capacitance between the surface low-conducting layer and the channel is larger than the inverse of the minimum target operating frequency of the device and the product of the lateral resistance of the surface low-conducting layer and the capacitance between the surface low-conducting layer and the channel is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the surface low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the surface low-conducting layer.

13. The transistor of claim 12, wherein each of the set of buried low-conducting layers and the set of surface low-conducting layers covers substantially all of an area corresponding to the channel.

14. The transistor of claim 12, wherein at least one of the set of surface low-conducting layers is at least partially isolated from the semiconductor by an isolation layer having a sheet resistance at least an order of magnitude higher than a sheet resistance of the at least one of the set of surface low-conducting layers.

15. A method comprising:

designing a semiconductor device including a channel, a set of contacts to the channel, and a set of buried low-conducting layers located below the channel in the semiconductor structure, wherein the designing the semiconductor device includes:

determining a minimum target operating frequency of the device; and

for each buried low-conducting layer in the set of buried low-conducting layers, determining a target lateral resistance for the buried low-conducting layer such that a product of the target lateral resistance of the buried low-conducting layer and a capacitance between the buried low-conducting layer and the channel is larger than an inverse of a minimum target operating frequency of the device and the product is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the buried low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the buried low-conducting layer; and

designing each buried low-conducting layer in the set of buried low-conducting layers based on the corresponding target lateral resistance.

16. The method of claim 15, wherein the designing each buried low-conducting layer includes selecting a material for the buried low-conducting layer based on the target lateral resistance.

17. The method of claim 15, wherein the semiconductor device further includes a set of surface low-conducting layers, and wherein the designing the semiconductor device further includes:

for each surface low-conducting layer in the set of surface low-conducting layers, determining a target lateral resistance for the surface low-conducting layer such that a product of a lateral resistance of the surface low-conducting layer and a capacitance between the surface low-conducting layer and the channel is larger than the inverse of the minimum target operating frequency of the device and the product of the lateral resistance of the surface low-conducting layer and the capacitance between the surface low-conducting layer and the channel is smaller than at least one of: a charge-discharge time of a trapped charge targeted for removal by the surface low-conducting layer or an inverse of a maximum interfering frequency targeted for suppression using the surface low-conducting layer; and

designing each surface low-conducting layer in the set of surface low-conducting layers based on the corresponding target lateral resistance.

18. The method of claim 17, wherein each of the set of buried low-conducting layers and the set of surface low-conducting layers covers substantially all of an area corresponding to the channel.

19. The method of claim 17, wherein at least one of the set of surface low-conducting layers is at least partially isolated from the semiconductor by an isolation layer having a sheet resistance at least an order of magnitude higher than a sheet resistance of the at least one of the set of surface low-conducting layers.

20. The method of claim 15, wherein the device is configured to operate as a field-effect transistor.

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