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Depetro et al.

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(54) **INTEGRATED DEVICE INCORPORATING LOW-VOLTAGE COMPONENTS AND POWER COMPONENTS, AND PROCESS FOR MANUFACTURING SUCH DEVICE**

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H01L 29/7816 (2013.01)

USPC **257/501**; 457/392; 457/500; 457/E27.064;
438/221; 438/275

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(58) **Field of Classification Search**

CPC H01L 29/0653; H01L 29/41766;
H01L 29/66696

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USPC 257/392, 500, 501, E27.064; 438/221,
438/275

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(21) Appl. No.: **12/839,989**

(Continued)

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(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

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H01L 21/8238 (2006.01)
H01L 29/417 (2006.01)
H01L 21/762 (2006.01)
H01L 29/06 (2006.01)
H01L 29/08 (2006.01)
H01L 29/423 (2006.01)
H01L 29/66 (2006.01)
H01L 29/78 (2006.01)

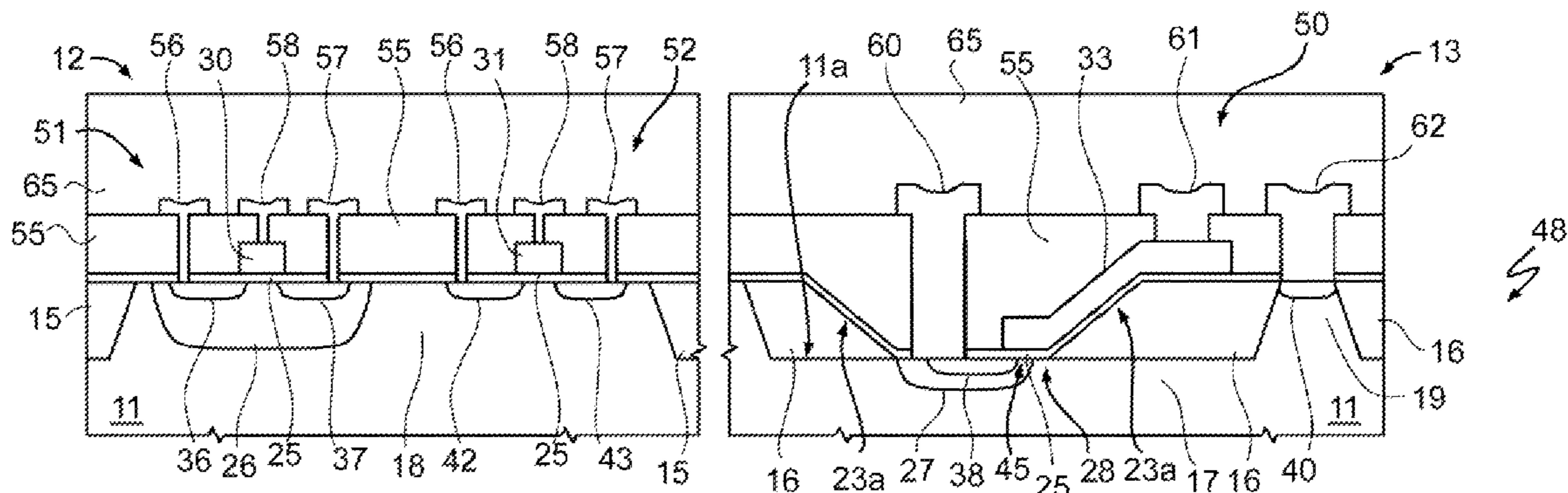
(57) **ABSTRACT**

An integrated device includes: a semiconductor body having a first, depressed, portion and second portions which project from the first portion; a STI structure, extending on the first portion of the semiconductor body, which delimits laterally the second portions and has a face adjacent to a surface of the first portion; low-voltage CMOS components, housed in the second portions, in a first region of the semiconductor body; and a power component, in a second region of the semiconductor body. The power component has at least one conduction region, formed in the first portion of the semiconductor body, and a conduction contact, coupled to the conduction region and traversing the STI structure in a direction perpendicular to the surface of the first portion of the semiconductor body.

(52) **U.S. Cl.**

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(2013.01); **H01L 21/823807** (2013.01); **H01L**
21/823814 (2013.01); **H01L 21/823857**
(2013.01); **H01L 21/76224** (2013.01); **H01L**
29/0653 (2013.01); **H01L 29/0657** (2013.01);
H01L 29/0865 (2013.01); **H01L 29/0882**
(2013.01); **H01L 29/42368** (2013.01); **H01L**

40 Claims, 7 Drawing Sheets



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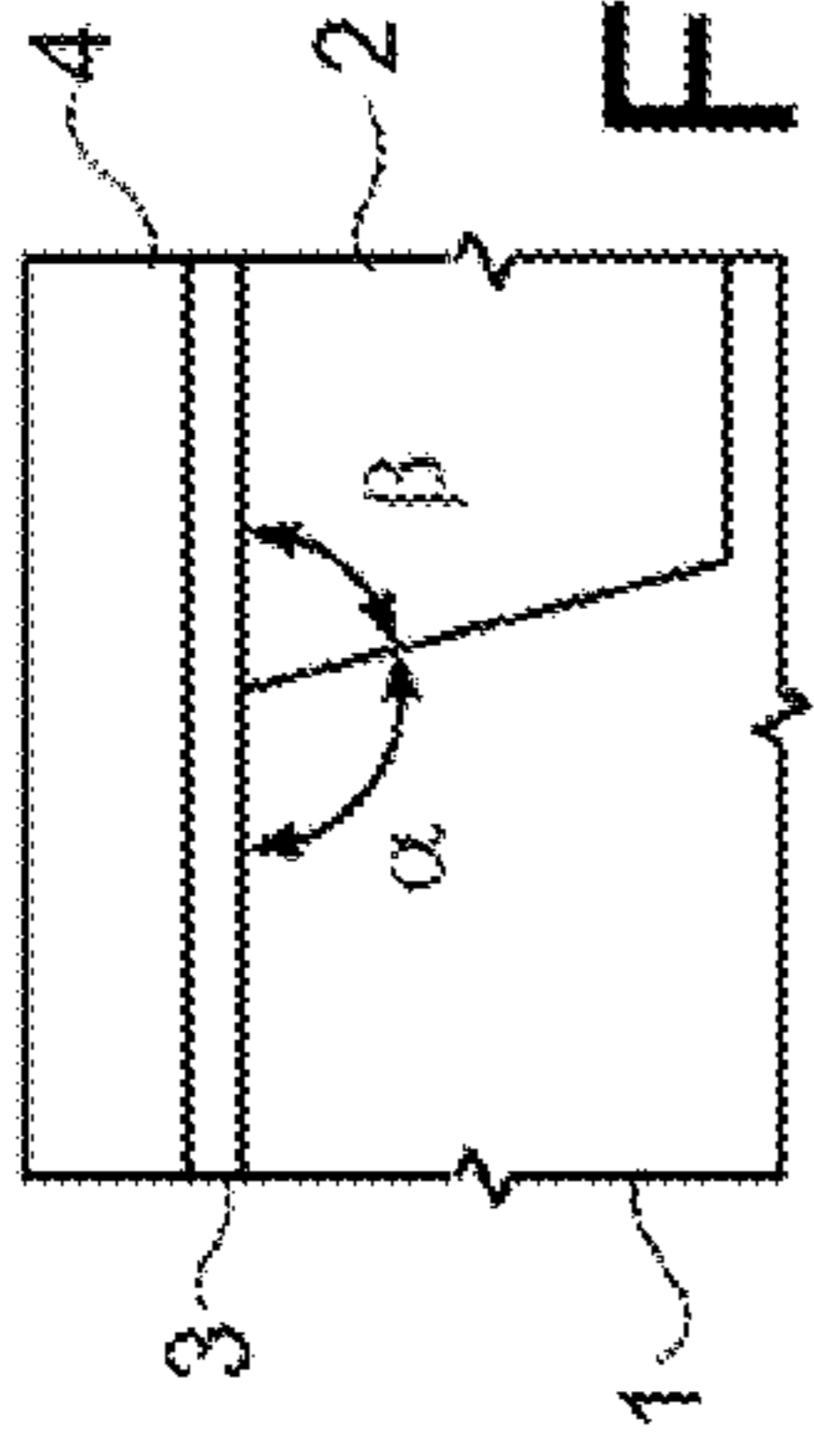


Fig. 1 - Background Art

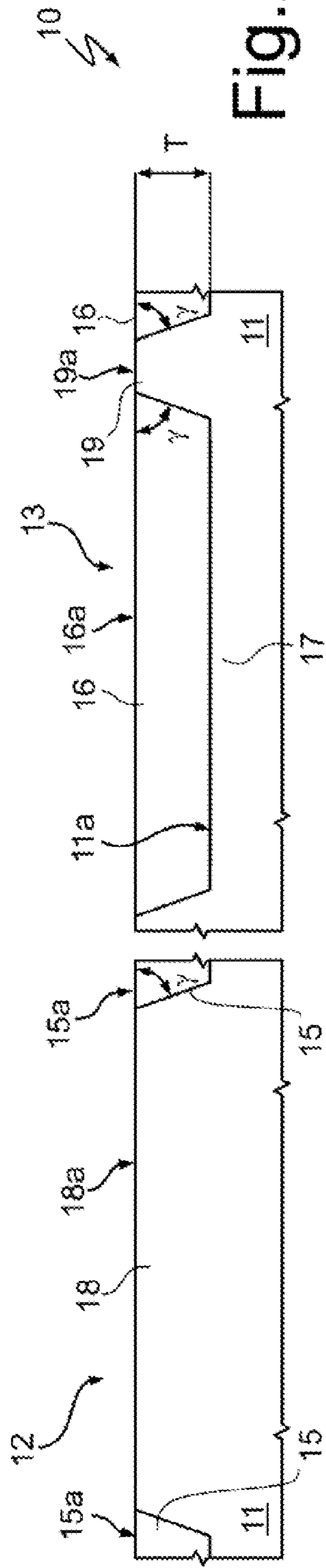


Fig. 2

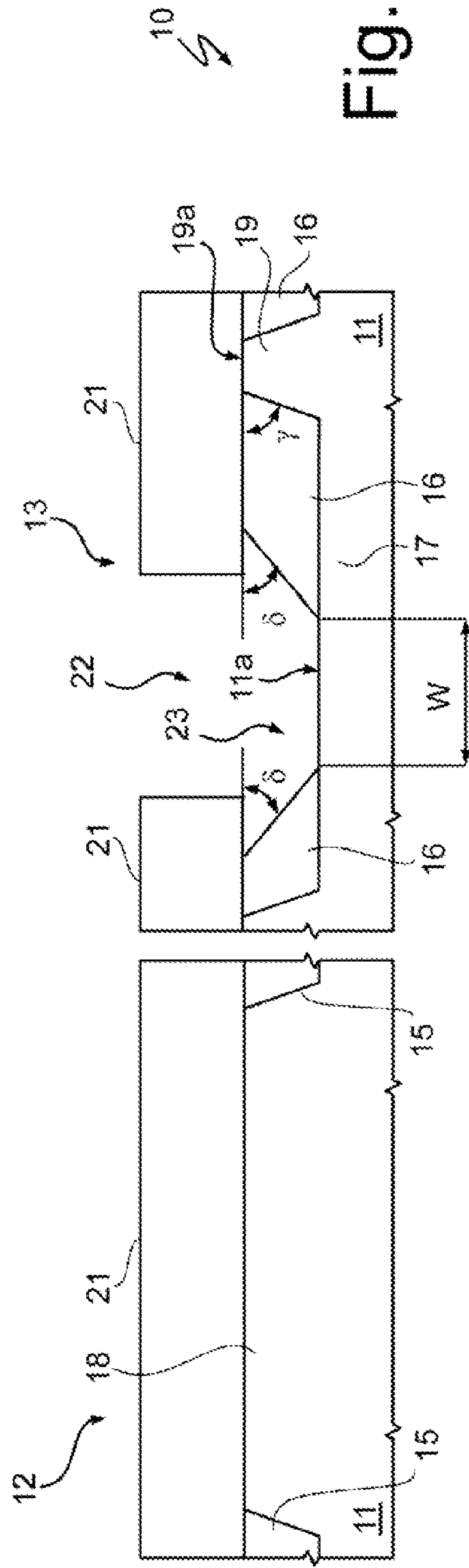


Fig. 3

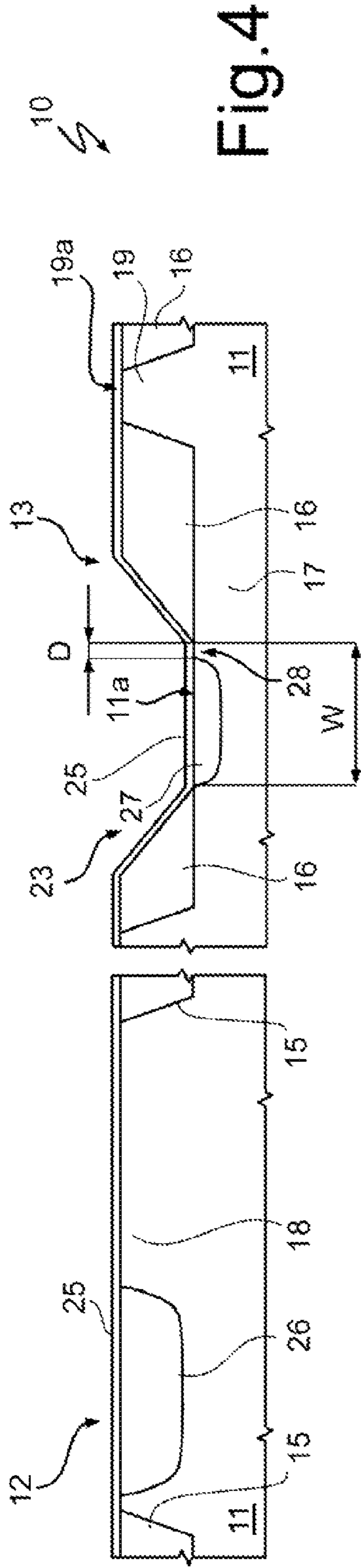


Fig. 4

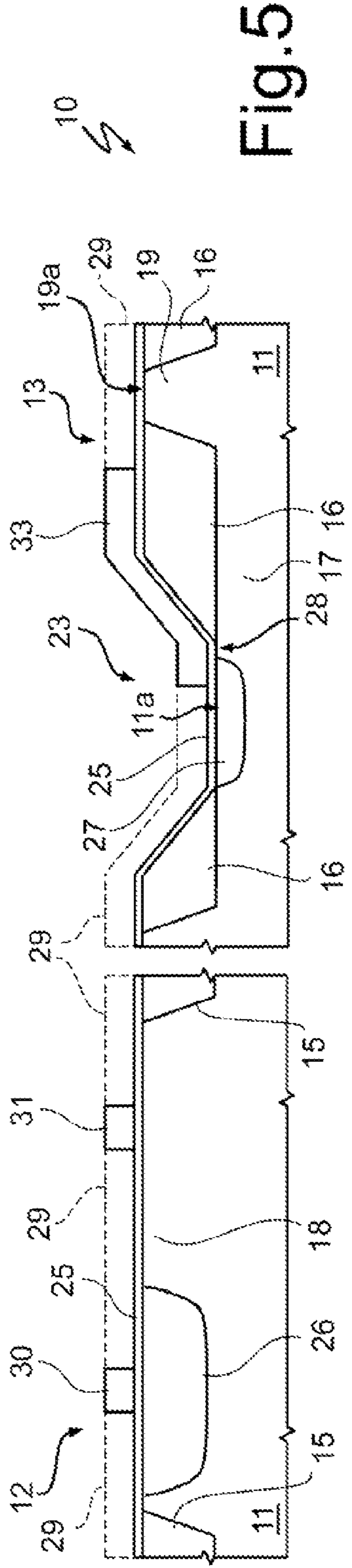


Fig. 5

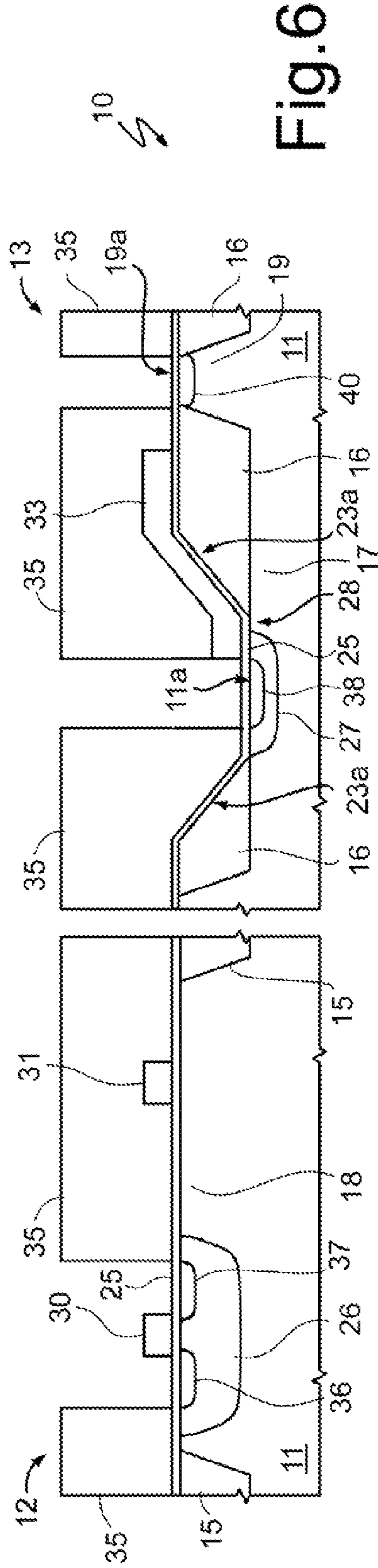


Fig. 6

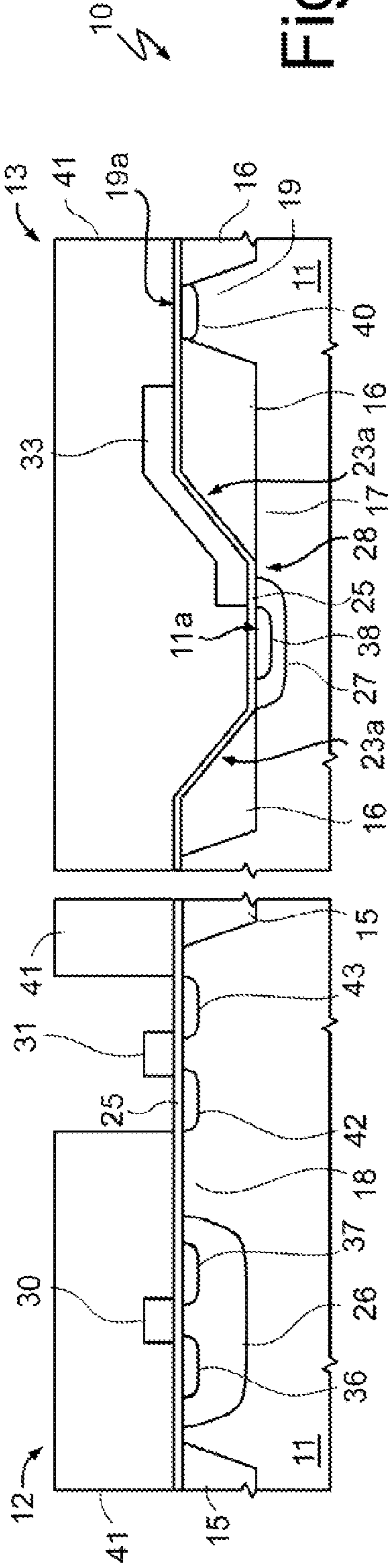


Fig. 7

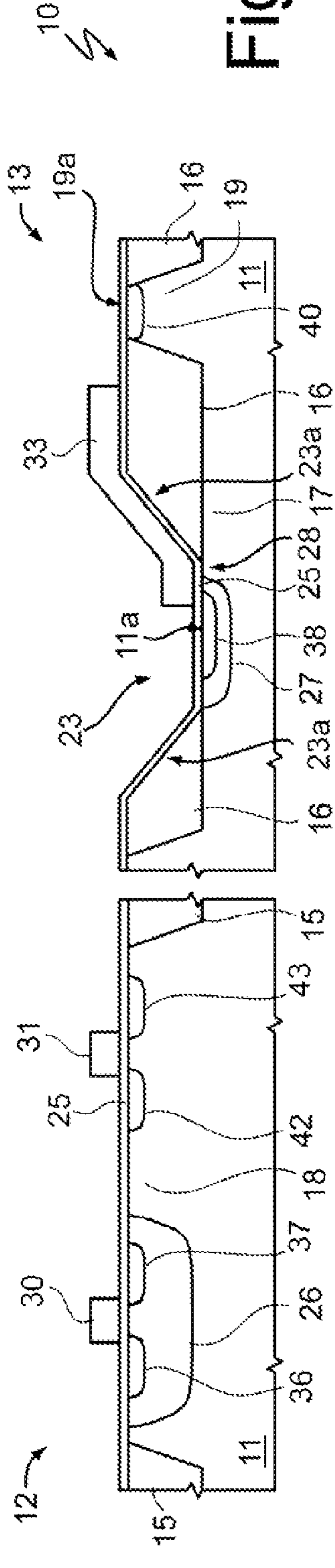


Fig. 8

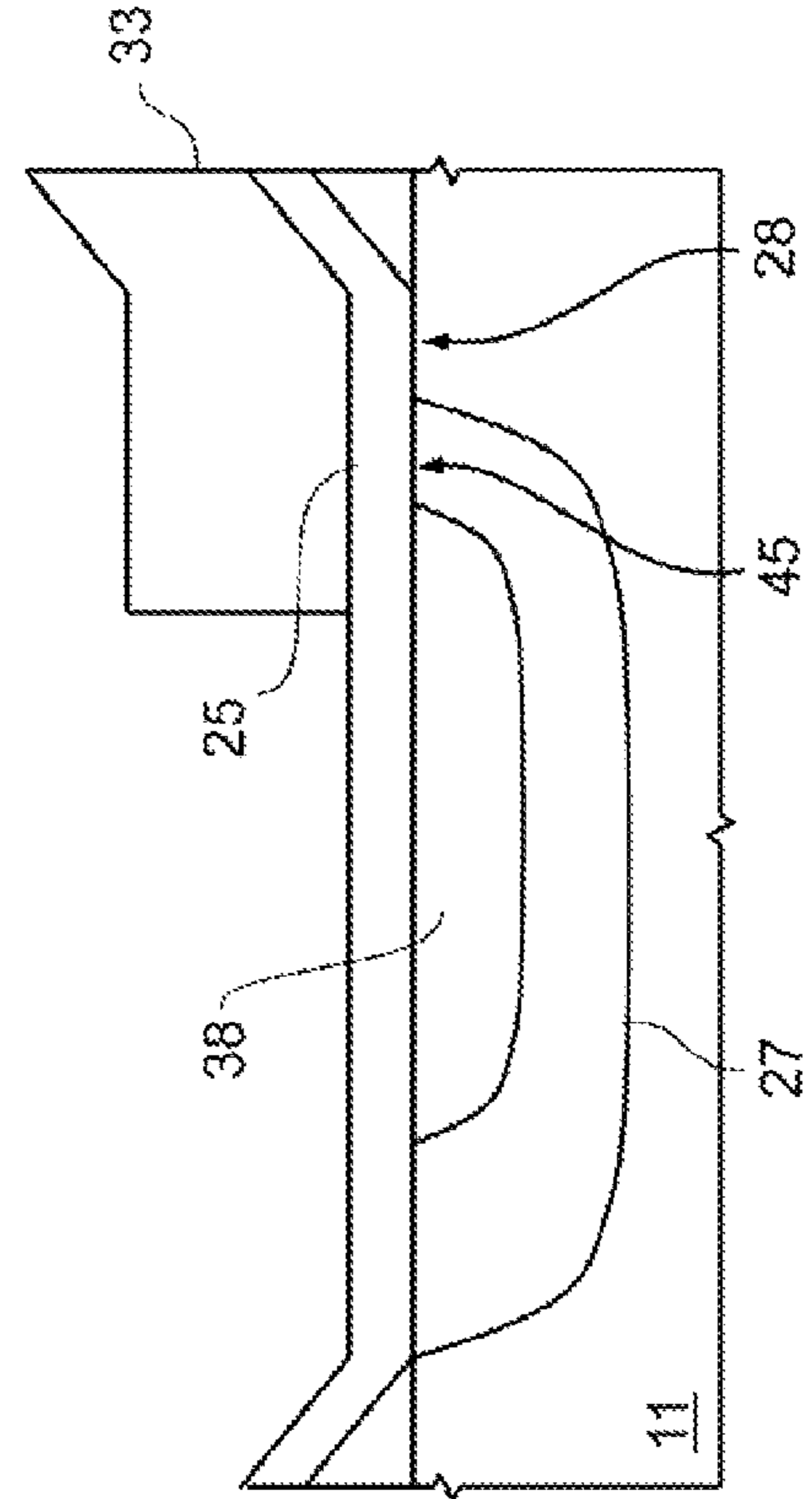


Fig. 9

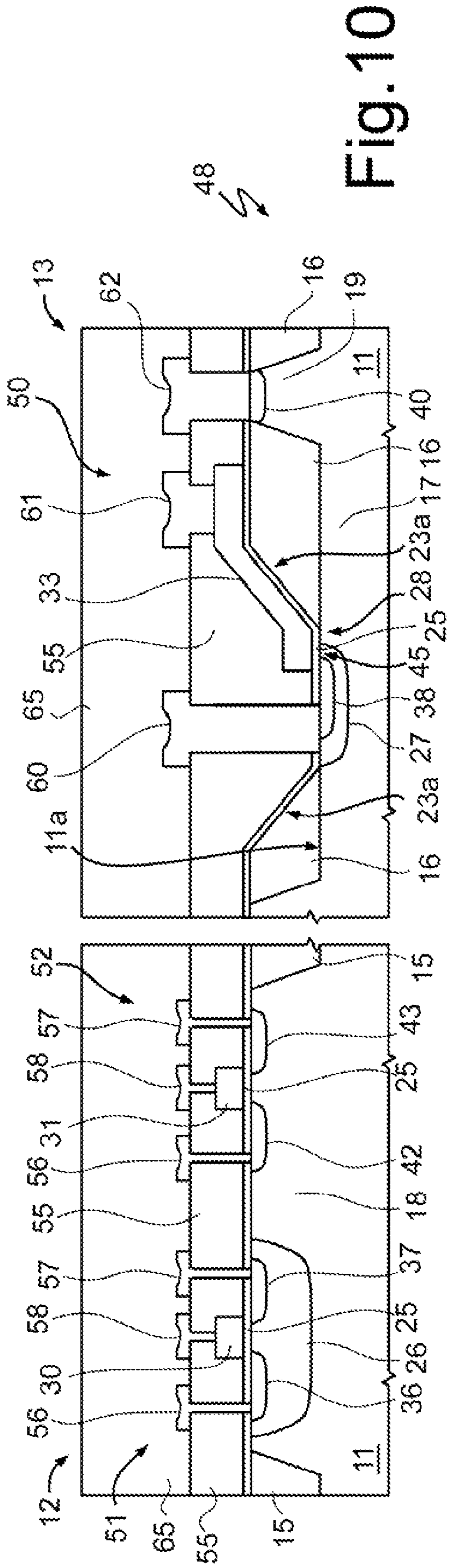


Fig. 10

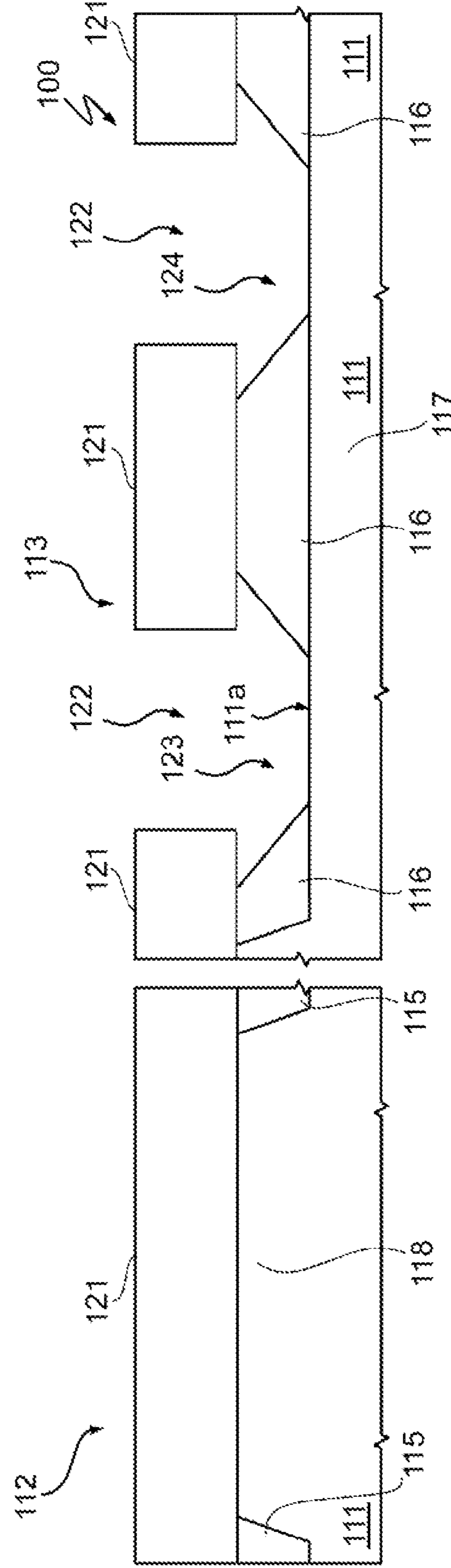


Fig. 11

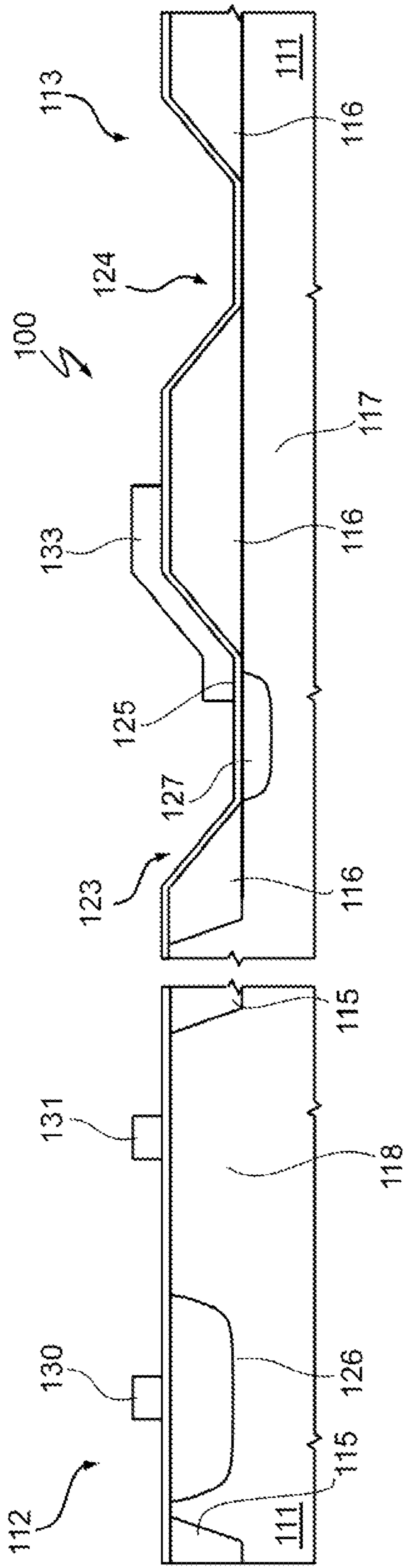


Fig. 12

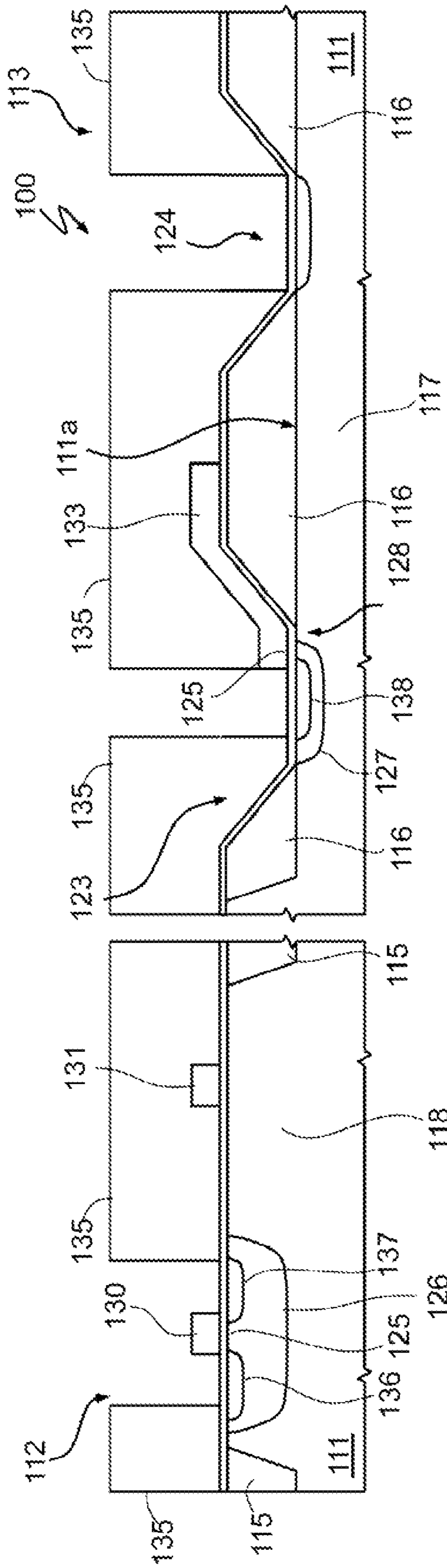


Fig. 13

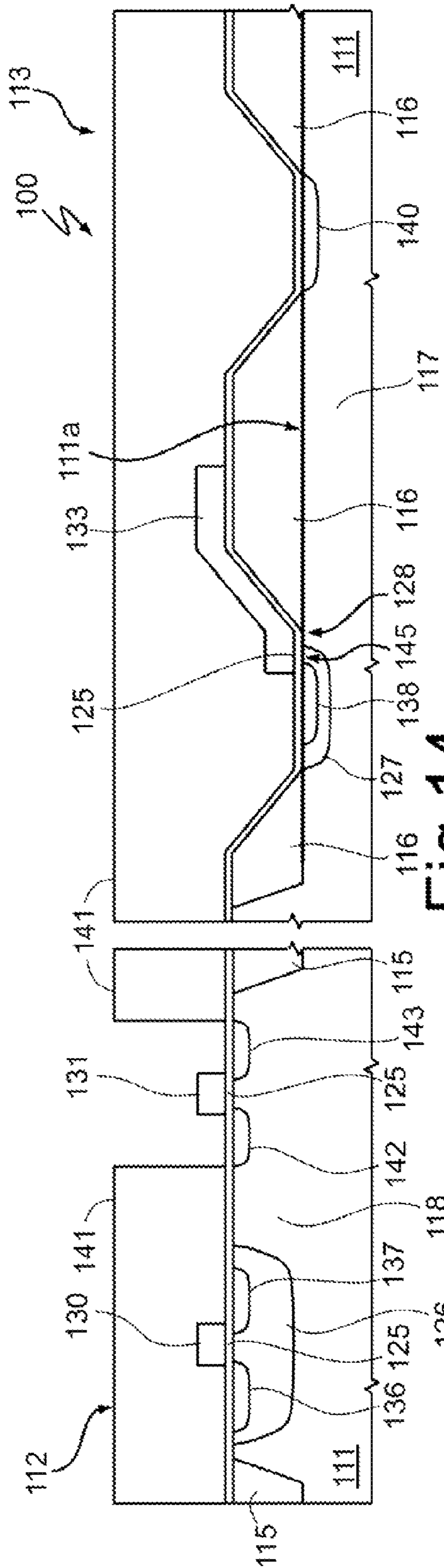


Fig. 14

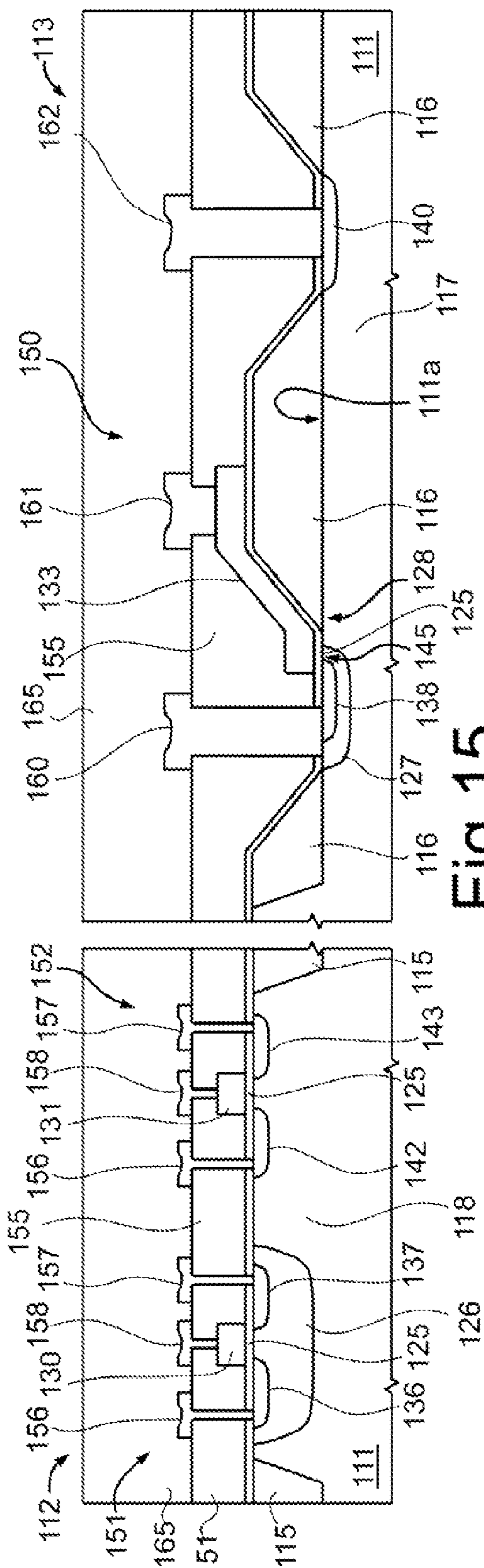


Fig. 15

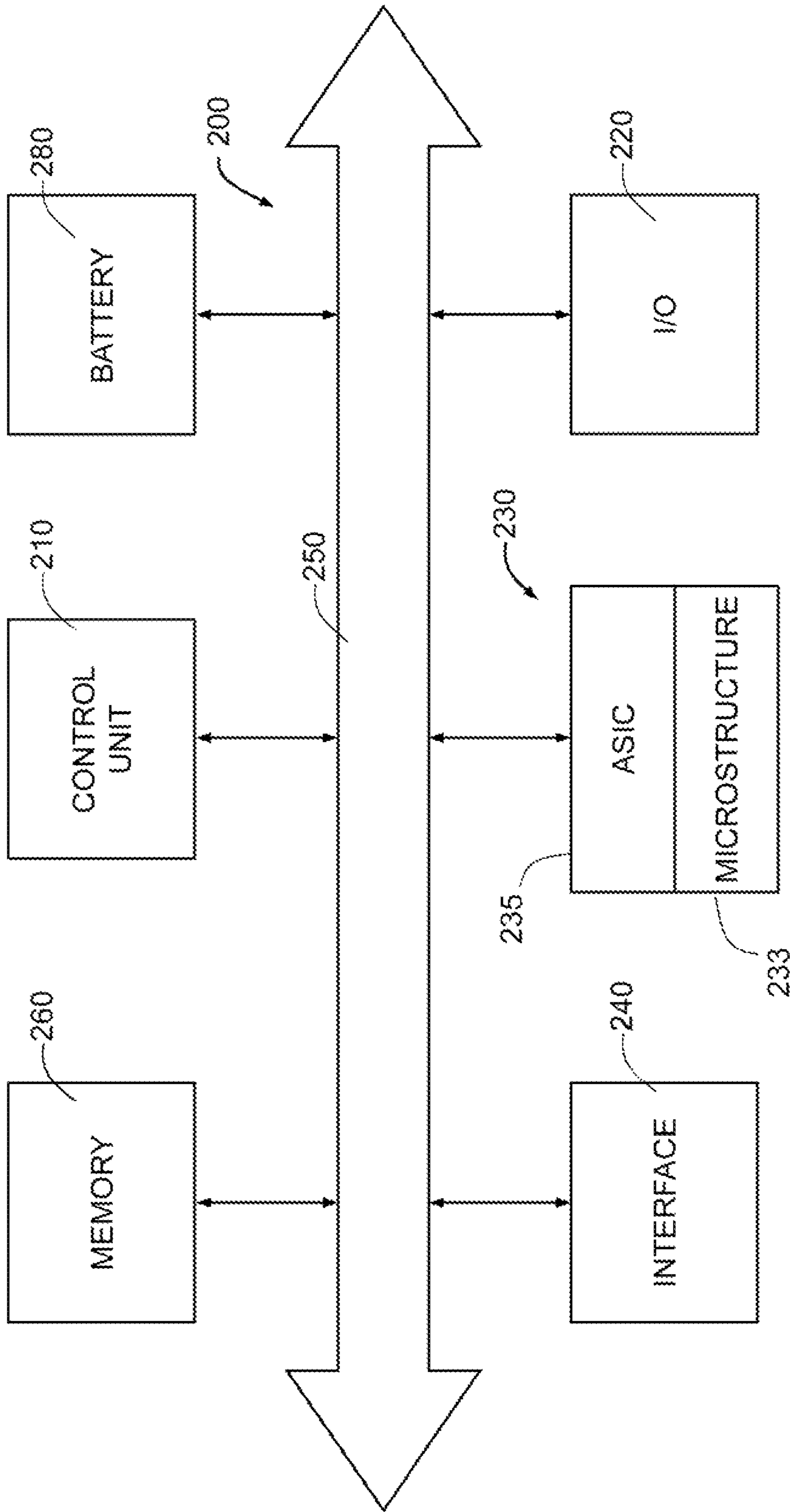


Fig. 16

1

**INTEGRATED DEVICE INCORPORATING
LOW-VOLTAGE COMPONENTS AND POWER
COMPONENTS, AND PROCESS FOR
MANUFACTURING SUCH DEVICE**

PRIORITY CLAIM

The instant application claims priority to Italian Patent Application No. TO2009A000550, filed Jul. 21, 2009, which application is incorporated herein by reference in its entirety.

TECHNICAL FIELD

An embodiment of the present disclosure relates to an integrated device incorporating low-voltage components and power components and to a process for manufacturing said device.

BACKGROUND

As is known, for several applications of microelectronics, a need has risen to integrate low-voltage devices and power devices (which operate at voltages that range from approximately 15 V to beyond 1000 V) in a single semiconductor chip. In particular, it has become increasingly more frequent to provide low-voltage devices in CMOS technology in a first portion of the chip and power devices, which are compatible with CMOS technology, in a second portion of the same chip. The active areas that house the various devices, both low-voltage devices and power devices, are insulated from one another using the shallow-trench insulation (STI) technique, which enables an extremely high degree of integration, with extremely small overall dimensions, and for this reason is typically used in CMOS technology. In practice, the substrate of a semiconductor wafer is selectively etched through a hard mask, for example, a multilayer mask of silicon oxide and silicon nitride, and trenches are formed, which delimit and separate active areas for low-voltage devices and active areas for power devices. The trenches are oxidized and completely filled with deposited dielectric, normally silicon oxide. The wafer is then planarized, and the hard mask is thus removed. The active areas are hence separated from one another by insulating structures with practically vertical walls, which extend for a stretch in the substrate.

SUMMARY

The manufacturing of power devices with CMOS technology, in particular in active areas defined by STI, shows, however, its limits when the scale of integration is pushed beyond a certain threshold. These limits begin to show up with the 0.25- μm technology and become evident with the 0.18- μm technology. As already mentioned, the walls of the STI structures are almost vertical (normally with an inclination of between 80° and 90°), precisely in order to minimize the extension of the transition areas between the thin oxide (gate oxide) and the thick oxide and thus reduce the overall dimensions. The corresponding interface in the silicon consequently has equally marked angles, as is shown in FIG. 1, where the reference number/designates a substrate of semiconductor material, in which a STI structure 2 is provided. The substrate/and the STI structure 2 are overlaid by a gate-oxide layer 3 and by a gate region 4 made of polycrystalline silicon. The angle α formed between the faces of the substrate/contiguous, respectively, to the STI structure 2 and to the gate-oxide layer 3 is $180^\circ - \beta$, where β indicates the slope of the walls of the STI structure 2. The angle α is hence

2

approximately $90^\circ - 100^\circ$ and causes a significant concentration of the electrical-field lines, in particular in the proximity of the region where the channel of the power device is formed. The concentration of the electrical-field lines may adversely affect both the active-state resistance R_{ON} (which is high and instable owing to injection of hot carriers) and the breakdown voltage (BV) of the power components.

In effect, problems of reliability and performance may arise and render incompatible the conventional use of the STI to provide power components integrated with low-voltage CMOS devices.

An embodiment of the present disclosure is to provide an integrated device and a process for manufacturing said integrated device that will enable the limitations described to be overcome.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the disclosure, some embodiments thereof will now be described, purely by way of non-limiting example and with reference to the attached drawings, wherein:

FIG. 1 is a cross section through a known integrated device;

FIG. 2 is a cross section through a semiconductor wafer in an initial step of a process for manufacturing an integrated device according to one embodiment of the present disclosure;

FIGS. 3-8 show the cross section of FIG. 2 in subsequent processing steps according to an embodiment;

FIG. 9 shows an enlarged detail of FIG. 8;

FIG. 10 is a cross section of an integrated device according to one embodiment of the present disclosure, obtained by dicing the wafer of FIG. 8 after final processing steps;

FIG. 11 is a cross section through a semiconductor wafer in an initial step of a process for manufacturing an integrated device according to a different embodiment of the present disclosure;

FIGS. 12-14 show the cross section of FIG. 11 in subsequent processing steps according to an embodiment;

FIG. 15 is a cross section of an integrated device according to another embodiment of the present disclosure, obtained by dicing the wafer of FIG. 14 after final processing steps;

FIG. 16 is a simplified block diagram of an electronic system incorporating an integrated device according to one embodiment of the present disclosure.

DETAILED DESCRIPTION

FIG. 2 shows a cross section through a semiconductor wafer, designated as a whole by the reference number 10, which comprises a structural layer, for example a substrate 11 of monocrystalline silicon of an N type, in which a low-voltage region 12 and a power region 13 have been defined (said regions are not represented in scale in the annexed figures, for simplicity; in particular, the low-voltage region 12 is enlarged). In a different embodiment (not illustrated), the structural layer may be an epitaxial layer grown on the substrate 11.

Inside the substrate 11, in particular, an insulating structure of a shallow-trench-insulation (STI) type has been preliminarily provided, which comprises at least a first insulating well 15 and a second insulating well 16, respectively formed in the low-voltage region 12 and in the power region 13 and having a thickness T. The first insulating well 15 has at least one opening, which laterally delimits an active area 18, which project from depressed portions 17 of the substrate 11 and are designed to house CMOS devices. The second insulating well

16 occupies at least one portion of the power region **13** and extends above the depressed portions **17** of the substrate **11**. In one embodiment, the second insulating well **16** extends substantially throughout the power region **13** and has at least one opening, which delimits laterally a raised drain region **19** and also projects from the depressed portion **17** of the substrate **11**.

The insulating wells **15**, **16** that form the insulating structure are obtained by a conventional STI process (not shown) and can be coupled or separate, according to the design requirements. In practice, the substrate **11** is etched through a hard mask to form trenches of a depth and shape corresponding to those of the first and second insulating wells **15**, **16**. The trenches are filled with a dielectric material, for example silicon oxide, and the wafer **10** is then planarized with a process that is stopped when the highest portions of the substrate **11** are reached (i.e., the surface of the active areas **18** and of the raised drain region **19**), after the hard mask has been removed.

The structure of the substrate **11** is hence not planar. The active areas **18** and the raised drain region **19** have respective raised surfaces **18a**, **19a** substantially aligned with top surfaces **15a**, **16a** of the insulating wells **15**, **16**. In the regions occupied by the insulating wells **15**, **16**, instead, the substrate **11** has depressed surfaces **11a** at a depth, with respect to the raised surfaces **18a**, **19a**, equal to the thickness T of the insulating wells **15**, **16** themselves. The transition areas between the depressed surfaces **11a** and the raised surfaces **18a**, **19a** have a slope γ close to the vertical and comprised, for example, between 80° and 90° .

As shown in FIG. 3, a resist mask **21** is formed on the wafer **10**. The resist mask **21** entirely coats the low-voltage region **12** and has a window **22** on top of the second insulating well **16**. The second insulating well **16** is then selectively etched, for example, in an isotropic way, through the resist mask **21**, and a through source window **23** is formed of a width W at the bottom, which exposes an underlying portion of the substrate **11**. The etch, for example a wet etch, is controlled in such a way that the slope δ of the walls **23a** that delimit the source window **23** is lower than the slope γ of the areas of transition between the depressed surfaces **11a** and the raised surfaces **18a**, **19a**. For example, the slope δ is comprised between 20° and 70° .

After removal of the resist mask **21** (FIG. 4), a gate-oxide layer **25**, having a thickness, for example, of between 5 nm and 50 nm, is thermally grown on the wafer **10**. At this point the wafer **10** is coated by thick-oxide regions (first and second insulating wells **15**, **16**) and by thin-oxide regions, where the gate-oxide layer **25** overlies directly the silicon of the substrate **11**.

By a P-type body implantation and subsequent diffusion, low-voltage body wells **26** are then provided in the low-voltage region **12**, and a power body well **27** is provided in the depressed portion **17** of the substrate **11** underlying the source window **23**.

Implantation of a P-type dopant species and diffusion are performed so that the power body well **27** does not occupy the entire width W of the source window **23**, but is separated by a distance D from the edge of the second insulating well **16** towards the raised drain region **19**. The portion of substrate between the second insulating well **16** and the power body well **27** defines a drain-junction region **28**.

Then, a polysilicon layer **29**, indicated by a dashed line in FIG. 5, is deposited and shaped to form low-voltage gate regions **30**, **31** and a power gate region **33**. The low-voltage gate regions **30**, **31** are made in the low-voltage region **12**, on the active area **18**, where low-voltage CMOS components are

to be provided. The power gate region **33** is arranged in part in the source window **23** and in part on the second insulating well **16**, between the source window **23** and the raised drain region **19**. In greater detail, the power gate region **33** extends on the drain-junction region **28** and on part of the power body well **27**, without, however, occupying the bottom of the source window **23** completely. The power gate region **30** lies moreover on one of the walls **23a** that delimit the source window **23**, towards the raised drain region **19**, and extends for a stretch on the second insulating well **16** in the same direction.

An N+ implantation and a P+ implantation are then carried out.

For the implantation of an N-type dopant species (N+ implantation, FIG. 6), a first implantation mask **35** is used, which exposes portions of the low-voltage body wells **26**, alongside the gate regions **30** (in effect, it is the gate-oxide layer **25** that is exposed, which, however, is traversed by the implanted species; hence, for reasons of simplicity, reference will be hereinafter made to the underlying regions as exposed regions, neglecting the presence of the gate-oxide layer **25** as regards the implantation steps). In the power region **13**, the first implantation mask **35** exposes the power body well **27** and the raised drain region **19**. In particular, in the source window **23** the first implantation mask **35** is aligned with the power gate region **33**. In the low-voltage body wells **26** low-voltage source regions **36** and low-voltage drain regions **37** are thus made, while in the power body well **27** a power source region **38** is formed and in the raised drain region **19** a drain-contact region **40** is formed. Both the power body well **27** and the power source region **38** are thus formed in the depressed portion **17** of the substrate **11** and are adjacent to the second insulating well **16**. The power source region **38** is housed in the power body well **27**.

With reference to FIG. 7, for the implantation of a P-type dopant species (P+ implantation) a second implantation mask **41** is used, which protects the power region **13** and the low-voltage body wells **26** and exposes portions of the substrate **11** in the active area **18** around the low-voltage gate regions **31**. Low-voltage source regions **42** and low-voltage drain regions **43** are thus made.

Once also the second implantation mask **41** has been removed, the dopants implanted are thermally diffused (FIG. 8). In this step, in particular, the power source region **38** diffuses under the power gate region **33**, as shown in the enlarged view of FIG. 9. Consequently, the power gate region **33** extends: on the drain-junction region **28**; on a channel region **45**, defined by a portion of the power body well **27** comprised between the drain-junction region **28** and the power source region **38**; and on a portion of the power source region **38**.

The gate-oxide layer **25** insulates the power gate region **33** from the drain-junction region **28**, from the channel region **45**, and from the power source region **38**.

The process is then terminated by steps of contact manufacturing and protection, to obtain an integrated device **48** (shown in FIG. 10), which comprises a power component **50**, in particular a lateral NMOS transistor, in the power region **13**, and low-voltage CMOS components (NMOS transistors **51** and PMOS transistors **52**), in the low-voltage region **12**.

A first insulating layer **55**, for example, of silicon oxide, is deposited over the entire wafer **10** and selectively etched, together with the gate-oxide layer **25**, to open contact windows on the low-voltage source regions **36**, **42** and on the low-voltage drain regions **37**, **43** in the low-voltage region **12**. Further contact windows are opened on the power source region **38** so as to expose also part of the power body well **27**,

on the power gate region **33** and on the drain-contact region **40**. Then, a metal layer is deposited and shaped so as to form, in the low-voltage region **12**, low-voltage source contacts **56**, low-voltage drain contacts **57**, and low-voltage gate contacts **58**. In the power region **13**, instead, there are made a power source contact **60**, which connects in short circuit the power source region **38** and the power body well **33**, a power gate contact **61** (on the portion of the power gate region **33** that lies on the second insulating well **16**), and a power drain contact **62**, on the drain-contact region **40**. After having provided a second metal layer (not shown for reasons of simplicity), the wafer **10** is coated with a second insulating protection layer **65** and is cut into dies, each of which incorporates an item of the integrated device **48** shown in FIG. **10**.

As mentioned, the integrated device **48** comprises low-voltage CMOS components (NMOS transistors **51** and PMOS transistors **52**), in the low-voltage region **12**, and at least one power component **50** (lateral NMOS transistor) in the power region **13**. The low-voltage CMOS components **51**, **52** are provided in the active area **18**, with the respective conduction regions (low-voltage source regions **36**, **42** and low-voltage drain regions **37**, **43**) which emerge at the raised surface **18a** of the active area **18**. Given that the voltages involved in this region are modest, the characteristic angles of the STI do not pose limitations to proper operation of the CMOS components.

The power source region **38** and the power body well **27** of the power component **50** are, instead, provided in the depressed portion of the substrate **11** under the STI structure, in particular under the second insulating well **16**, and emerge at the depressed surface **11a** of the substrate **11**, which is plane. For this reason, the drain-junction region **28**, which is adjacent to the channel region **45** and is more critical for the high current density in the active state, does not have corners, and hence dangerous concentrations of the electrical-field lines are prevented. The geometry without corners in the areas of higher current density allows improvement in particular the breakdown voltage (BV) and the active-state resistance (R_{ON}) of the power components, which may be more reliable and efficient.

The integrated device described and the corresponding manufacturing process hence enable exploitation of the advantages of the insulation of an STI type, especially as regards the reduction of the area occupied, without, however, incurring in the limitations posed by the accentuated corners, typical of STI, for the production power components.

A different embodiment of the disclosure is shown in FIGS. **11-15**.

A semiconductor wafer **100** (FIG. **11**) has substantially the structure illustrated in FIG. **2** and comprises a substrate **111**, in which a STI structure is provided. The STI structure comprises a first insulating well **115**, which defines laterally active areas **118**, which project from depressed portions **117** of the substrate **111** in a low-voltage region **12**, and a second insulating well **116**, which extends in a continuous way substantially over an entire power region **116**. Also in this case, the structure of the substrate **111** is not planar. The structure of the substrate **111** is hence not planar. The active areas **118** have in fact respective raised surfaces **118a** substantially aligned with top surfaces **115a**, **116a** of the insulating wells **115**, **116**. In the regions occupied by the insulating wells **115**, **116**, instead, the substrate **111** has depressed surfaces **111a** at a depth with respect to raised surfaces **118a** equal to the thickness **T** of the insulating wells **115**, **116** themselves.

On the semiconductor wafer **100** a resist mask **121** is formed, which coats entirely the low-voltage region **112** and has windows **122** on the second insulating well **116**. The

second insulating well **116** is etched through the resist mask **121** and a through source window **123** and a through drain window **124** are formed, which expose respective underlying portions of the substrate **111**.

As already described previously, steps of body implantation, thermal oxidation, polysilicon deposition and subsequent shaping are then carried out to obtain the structure of FIG. **12**. In particular, in these steps there are provided a gate-oxide layer **125**, low-voltage body wells **126** and low-voltage gate regions **130**, **131** in the active area **118**, a power body well **127**, in a depressed portion **117** of the substrate **111** underlying the source window **123**, and a power gate region **133**. The power gate region **133** extends on a part of the power body well **127**, in part on a drain-junction region **128**, adjacent to the power body well **127**, and in part on the second insulating well **116**.

N+ and P+ implantations are then carried out.

For the N+ implantation (FIG. **13**), an implantation mask **135** is used, which exposes portions of the low-voltage body wells **126**, alongside the gate regions **130**. In the power region **113**, the first implantation mask **135** exposes the power body well **127** and a portion of the substrate **111** under the drain window **124**. In the low-voltage body wells **126** low-voltage source regions **136** and low-voltage drain regions **137** are thus provided, while in the power body well **127** a power source region **138** is formed and in the portion of the substrate **111** underlying the drain window **124** a drain-contact region **140** is formed. A channel region **145** is defined between the power body well **127** and the drain-junction region **128**.

The P+ implantation (FIG. **14**) is carried out substantially as already described previously, using a second implantation mask **141**. Low-voltage source regions **142** and low-voltage drain regions **143** are thus provided.

The process is terminated as already described previously, with a diffusion, with the provision of metallizations and protection layers and with dicing of the wafer **100**. In particular (FIG. **15**), in these steps contacts are provided in the low-voltage region **112**, namely, low-voltage source contacts **156**, low-voltage drain contacts **157**, and low-voltage gate contacts **158**, and in the power region **113**, namely, a power source contact **160**, a power gate contact **161**, and a power drain contact **162**.

An integrated device **148** is thus provided, which comprises low-voltage CMOS components (NMOS transistors **151** and PMOS transistors **152**), in the active areas **118** of the low-voltage region **12**, and at least one power component **150** (lateral NMOS transistor) in the power region **113**.

In the embodiment described, also the drain-contact region **140** is formed in a plane portion of the substrate **111**, and hence the risks associated with formation of high electrical fields on account of the presence of sharp corners are further reduced.

The integrated device described can advantageously be used to provide control circuitry for MEMS (microelectromechanical system) devices, which are in turn designed to be incorporated in complex systems.

FIG. **16** illustrates a portion of a system **200** in accordance with one embodiment of the present disclosure. The system **200** may comprise a controller **210**, an input/output (I/O) device **220** (for example, a keyboard or a screen), a microelectromechanical device **230**, a wireless interface **240**, and a memory **260**, of a volatile or non-volatile type, coupled to one another through a bus **250**. In one embodiment, a battery **280** may be used for supplying the system **200**.

The microelectromechanical device **230** comprises a microstructure **233** and an integrated device **235** (ASIC, Application-Specific Integrated Circuit) dedicated to driving

and control of the read microstructure **233** and, possibly, to detection of measurable quantities by means of the microstructure **233**. The integrated device **235** comprises low-voltage CMOS components and power components integrated in one and the same semiconductor chip and is provided according to what is described with reference to FIGS. **1-10** or, alternatively, according to what is described with reference to FIGS. **11-15**.

In one embodiment, the microelectromechanical device **230** is a microelectromechanical sensor, such as, for example, an accelerometer, a gyroscope, a pressure sensor, a microphone. In a different embodiment, the microelectromechanical device **230** is a microactuator.

The controller **210** may comprise, for example, one or more microprocessors, microcontrollers, and the like.

The I/O device **220** may be used for generating a message. The system **200** may use the wireless interface **240** for transmitting and receiving messages to and from a wireless-communication network with a radiofrequency (RF) signal. Examples of wireless interface may comprise an antenna, a wireless transceiver, such as a dipole antenna. In addition, the I/O device **220** may provide a voltage representing what is stored both in the form of digital output (if digital information has been stored) and in the form of analog output (if analog information has been stored).

The system **200** may be used in apparatuses, such as, for example, a palmtop computer (personal digital assistant, PDA), a laptop or portable computer, possibly with wireless capacity, a cellphone, a messaging device, a digital music player, a digital camera, or other devices.

Finally, it is evident that modifications and variations may be made to the device and the process described, without thereby departing from the scope of the present disclosure, as defined in the annexed claims.

In the first place, the integrated device may comprise an arbitrary number of STI wells coupled to one another or separate from one another. In the same way, the integrated device may comprise an arbitrary number of active areas and power components.

The implantations of an N type or P type for providing the body, source, and drain-contact regions may be carried out prior to formation of the STI wells. Clearly, in this case the source windows and, if necessary, the drain windows, are aligned to the underlying implantations.

Of course, it is possible to provide an embodiment in which the conductivity of the different regions of semiconductor material is opposite with respect to the one described above.

One or more of the components of FIG. **16** may be disposed on a same die (e.g., a system or a chip) or on respective dies.

From the foregoing it will be appreciated that, although specific embodiments have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the disclosure. Furthermore, where an alternative is disclosed for a particular embodiment, this alternative may also apply to other embodiments even if not specifically stated.

The invention claimed is:

1. Integrated device comprising:

a semiconductor body having a depressed first portion and second portions projecting from the first portion;

an STI insulation structure, extending on the first portion of the semiconductor body, having a first sidewall with the second portions of the semiconductor body, the first sidewall disposed at a first angle with respect to a plane defined by a top surface of the second portion that is less than ninety degrees, having an aperture exposing part of the first portion, the aperture having sidewalls disposed

at a second angle with respect to the plane defined by the to surface of the second portion that is less than ninety degrees and having a face adjacent to a surface of the first portion of the semiconductor body, the second angle less than the first angle by at least 10 degrees;

low-voltage CMOS components, accommodated in the second portions, in a first region of the semiconductor body; and

a power component, in a second region of the semiconductor body;

wherein the power component comprises at least one conduction region, formed in the first portion of the semiconductor body, and a conduction contact, connected to the conduction region and crossing the STI insulation structure perpendicularly to the plane defined by the to surface of the second portion of the semiconductor body.

2. Device according to claim **1**, wherein the conduction region is formed below the STI insulation structure.

3. Device according to claim **1**, wherein the STI insulation structure aperture is crossed by the conduction contact.

4. Device according to claim **3**, wherein the sidewalls of the aperture have a slope comprised between 20° and 70°.

5. Device according to claim **1**, wherein the conduction region is a source region.

6. Device according to claim **5**, comprising a body region, formed in the first portion of the semiconductor body and accommodating the conduction region.

7. Device according to claim **6**, comprising a gate region, arranged in part in the aperture extending above a junction region of the semiconductor body adjacent to the body region, above a channel region defined by a portion of the body region comprised between the junction region and the conduction region, and above part of the conduction region.

8. Device according to claim **7**, wherein the gate region extends in part above the STI insulation structure.

9. Device according to claim **1**, wherein the semiconductor body comprises at least a third portion projecting from the first portion, laterally delimited by the STI insulation structure and selectively connectable to the conduction region, and wherein the power component comprises a further conduction contact, connected to the third portion of the semiconductor body.

10. Device according to claim **1**, wherein the power component comprises a further conduction contact, connected to the first portion of the semiconductor body and crossing the STI insulation structure perpendicularly to the plane defined by the to surface of the second portion of the semiconductor body.

11. A semiconductor structure, comprising:

a semiconductor region;

a first source region disposed on a first surface at a first level of the semiconductor region and bounded by a first structure at a boundary having a first face disposed at a first angle with respect to a plane defined by the first level of the semiconductor region, the first angle less than ninety degrees; and

a second source region disposed on a second surface at a second level of the semiconductor region below the first level and formed in a source window exposing the second surface and bounded by a second structure at a first boundary having a second face disposed at a second angle with respect to a plane defined by the second level of the semiconductor region, the second angle less than the first angle by at least 10 degrees, said second structure including a second boundary having a third face disposed at the first angle.

11

the second face and having a second sidewall with a slope defining the third face.

26. The semiconductor structure of claim **11**, further comprising:

a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first level;

a first isolation region disposed in the semiconductor region substantially at the first level to form the first structure and having a sidewall with a slope defining the first face;

a higher power transistor that includes the second source region and that includes a drain region disposed in the semiconductor region and having at least a portion at substantially the second level; and

a second isolation region disposed in the semiconductor region substantially at the first level to form the second structure and having a first sidewall with a slope defining the second face and having a second sidewall with a slope defining the third face.

27. An integrated circuit, comprising:

a die having a surface and a semiconductor layer disposed below the surface;

a first source region disposed in the semiconductor layer at a first distance from the surface; and

a second source region disposed in the semiconductor layer at a second distance from the surface, wherein a source window for the second source region is surrounded by a first isolation region having a first sidewall disposed at a first slope greater than a second slope of a second sidewall of the first isolation region, the first slope greater than the second slope by a factor of at least 10%, wherein the first slope and the second slope are less than ninety degrees.

28. The integrated circuit of claim **27**, further comprising: a lower power transistor that includes the first source region; and

a higher power transistor that includes the second source region.

29. The integrated circuit of claim **27**, further comprising: the first isolation region disposed in the semiconductor layer at substantially the first distance from the surface and surrounding the source window; and

a second isolation region disposed in the semiconductor layer at substantially the first distance from the surface and surrounding an active area within which the first source region is formed.

30. The integrated circuit of claim **27**, further comprising: the first isolation region disposed in the semiconductor layer at substantially the first distance from the surface such that the second sidewall is contiguous with the source window; and

a second isolation region disposed in the semiconductor layer at substantially the first distance from the surface contiguous with an active area within which the first source region.

31. The integrated circuit of claim **27**, further comprising: the first isolation region disposed in the semiconductor layer substantially at the first distance from the surface and having the second sidewall adjacent to the source window; and

a second isolation region disposed in the semiconductor layer substantially at the first distance from the surface and having the first sidewall; each of the sidewalls having a different slope.

12

32. The integrated circuit of claim **27**, further comprising: a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface; and

a higher power transistor that includes the second source region and that includes a drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface.

33. The integrated circuit of claim **27**, further comprising: a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface; and

a higher power transistor that includes the second source region and that includes a drain region disposed in the semiconductor region and having at least a portion at substantially the second distance from the surface.

34. The integrated circuit of claim **27**, further comprising: a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface;

the first isolation region disposed in the semiconductor region substantially at the first distance from the surface and having a sidewall with a slope having a first magnitude;

a higher power transistor that includes the second source region and that includes a drain region disposed in the semiconductor region and having at least a portion at substantially the second distance from the surface; and

a second isolation region disposed in the semiconductor region substantially at the first distance from the surface and having a sidewall with a slope having a second magnitude.

35. The integrated circuit of claim **27**, further comprising: a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface;

the first isolation region disposed in the semiconductor region substantially at the first distance from the surface and having a sidewall having a slope with a first magnitude;

a higher power transistor that includes the second source region and that includes a second drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface; and

a second isolation region disposed in the semiconductor region substantially at the first distance from the surface and having a first sidewall with a slope having a second magnitude and having a second sidewall with a slope having substantially the first magnitude.

36. The integrated circuit of claim **33**, further comprising: a lower power transistor that includes the first source region and that includes a first drain region disposed in the semiconductor region and having at least a portion at substantially the first distance from the surface;

the first isolation region disposed in the semiconductor region substantially at the first distance from the surface and having a sidewall with a slope having a first magnitude;

a higher power transistor that includes the second source region and that includes a drain region disposed in the semiconductor region and having at least a portion at substantially the second distance from the surface; and a second isolation region disposed in the semiconductor region substantially at the first distance from the surface

and having a first sidewall with a slope having a second magnitude and having a second sidewall with a slope having substantially the second magnitude.

37. A system, comprising:

a first integrated circuit, including: 5

a die having a surface and a semiconductor layer disposed below the surface;

a first source region disposed in the semiconductor layer at a first distance from the surface; and

a second source region disposed in the semiconductor 10
layer at a second distance from the surface, wherein a source window for the second source region is surrounded by a first insulation region having a first side wall disposed at a first angle with respect to a surface of the second source region, the first angle different 15
from a second angle with respect to a surface of the second source region of a second side wall of the first insulation region, wherein the difference is at least 10 degrees; and

a second integrated circuit coupled to the first integrated 20
circuit.

38. The system of claim **37** wherein the first and second integrated circuits are disposed on a same die.

39. The system of claim **37** wherein the first and second 25
integrated circuits are disposed on respective dies.

40. The system of claim **37** wherein at least one of the first and second integrated circuits comprises a controller.

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