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Yun et al.

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(45) **Date of Patent: Dec. 9, 2014**

(54) **GATE STRUCTURE IN NON-VOLATILE MEMORY DEVICE**

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Related U.S. Application Data

(63) Continuation of application No. 13/759,195, filed on Feb. 5, 2013, now Pat. No. 8,674,429.

(30) **Foreign Application Priority Data**

Apr. 17, 2012 (KR) 10-2012-0039915

(51) **Int. Cl.**

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H01L 29/66	(2006.01)
H01L 21/28	(2006.01)
H01L 27/115	(2006.01)
H01L 29/792	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7926*** (2013.01); ***H01L 29/66833*** (2013.01); ***H01L 21/28282*** (2013.01); ***H01L 27/1157*** (2013.01); ***H01L 29/792*** (2013.01); ***H01L 27/11582*** (2013.01)

USPC **257/314**; 257/321; 257/324; 257/E21.409; 257/E27.103; 257/E29.309

(58) **Field of Classification Search**

CPC H01L 21/28282; H01L 27/1157; H01L 29/792; H01L 29/7926; H01L 29/66833

USPC 257/314–324, 326, E21.409–E21.422, 257/27.103, 29.309

See application file for complete search history.

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Primary Examiner — Michael Lebentritt

(74) *Attorney, Agent, or Firm* — Harness, Dickey & Pierce, P.L.C.

(57) **ABSTRACT**

A gate structure of a non-volatile memory device and a method of forming the same including a tunnel oxide layer pattern, a charge trap layer pattern, a blocking dielectric layer pattern having the uppermost layer including a material having a first dielectric constant greater than that of a material included in the tunnel oxide layer pattern, and first and second conductive layer patterns. The gate structure includes a first spacer to cover at least the sidewall of the second conductive layer pattern. The gate structure includes a second spacer covering the sidewall of the first spacer and the sidewall of the first conductive layer pattern and including a material having a second dielectric constant equal to or greater than the first dielectric constant. In the non-volatile memory device including the gate structure, erase saturation caused by back tunneling is reduced.

15 Claims, 31 Drawing Sheets

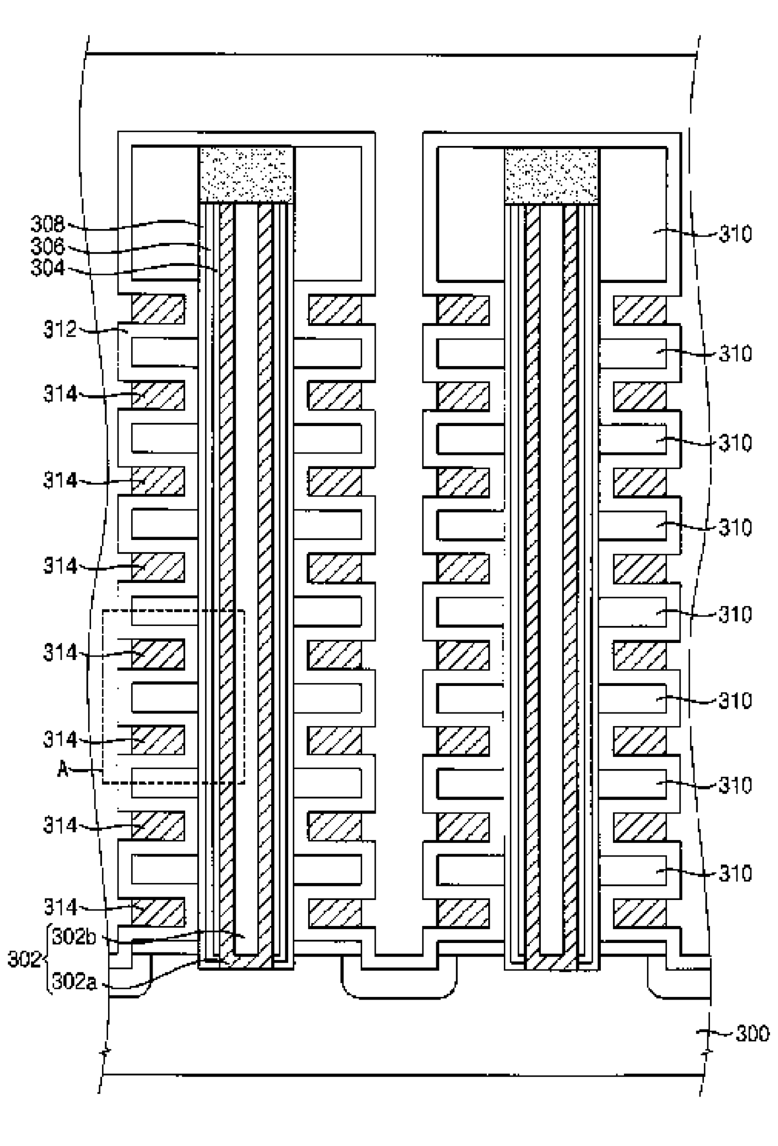

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FIG. 1A

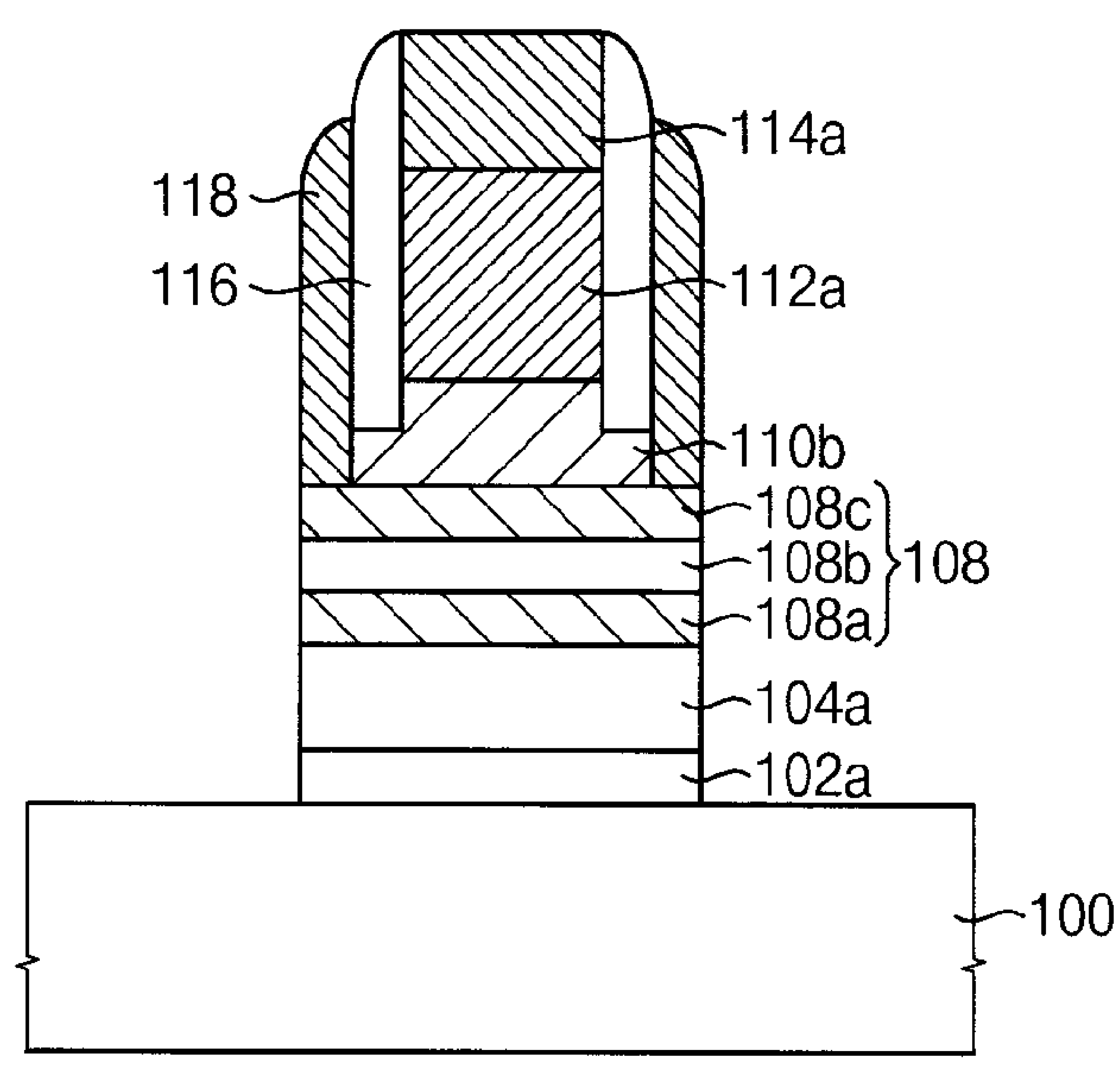
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FIG. 1B

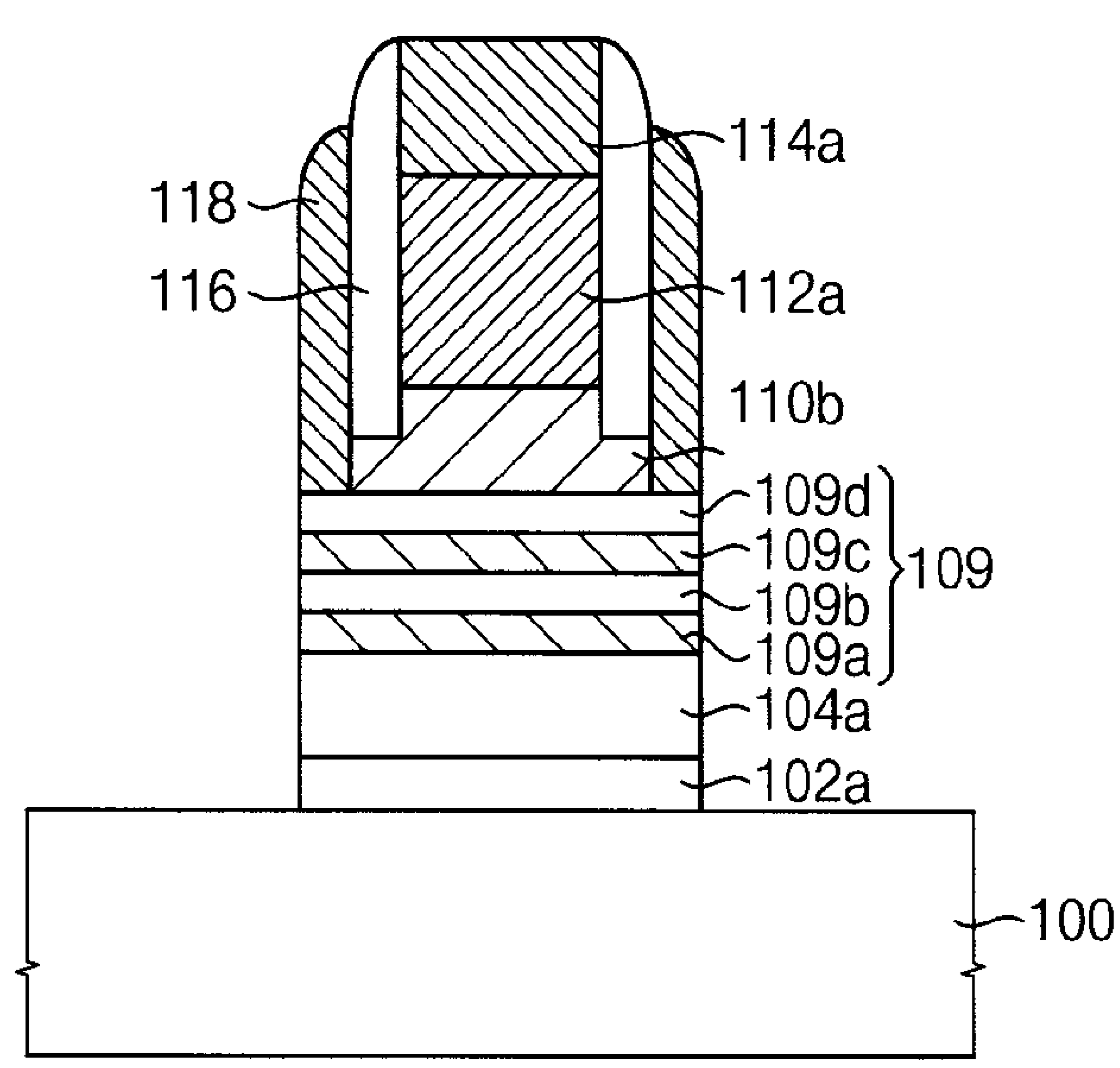
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FIG. 1C

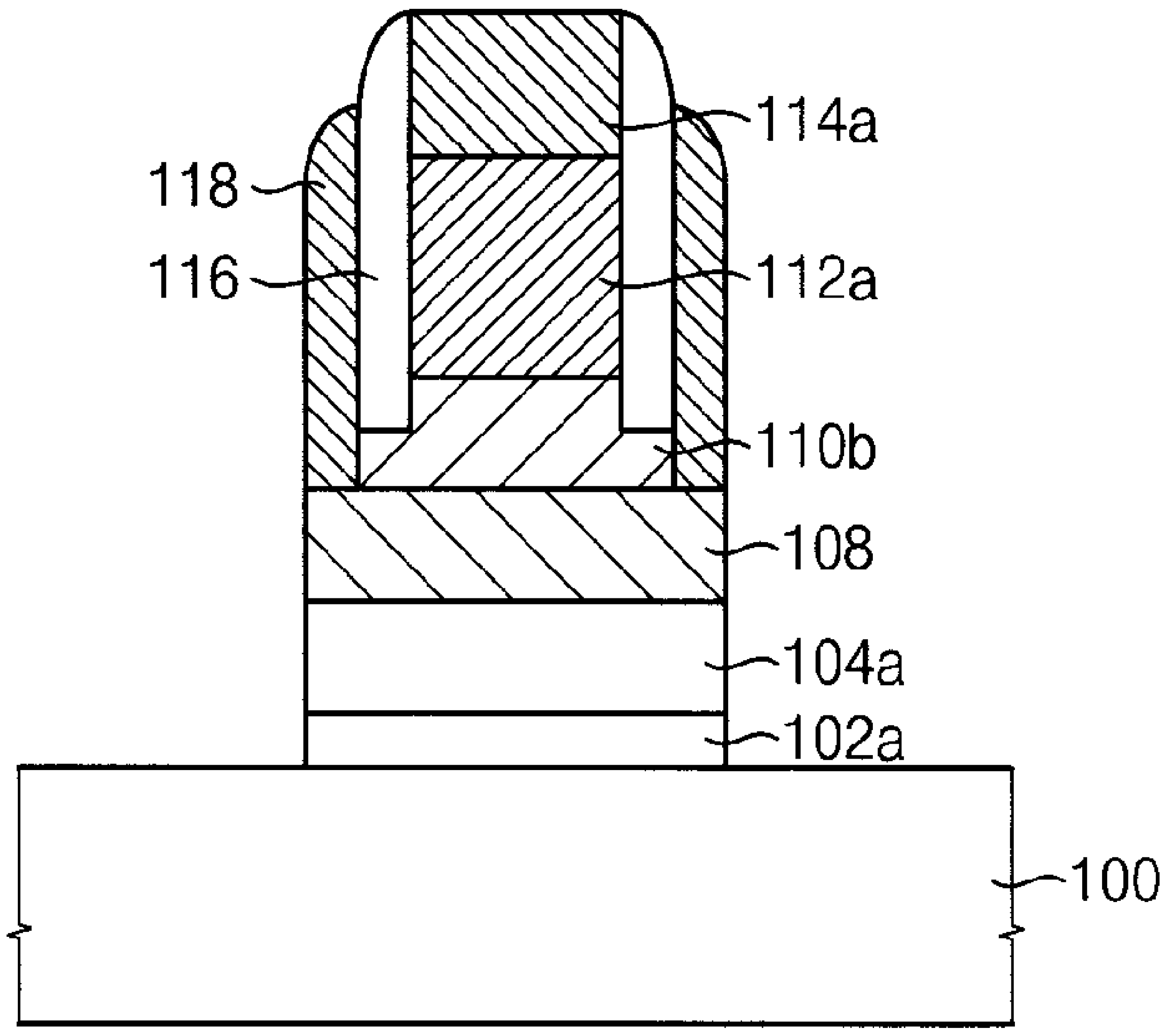
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FIG. 2A

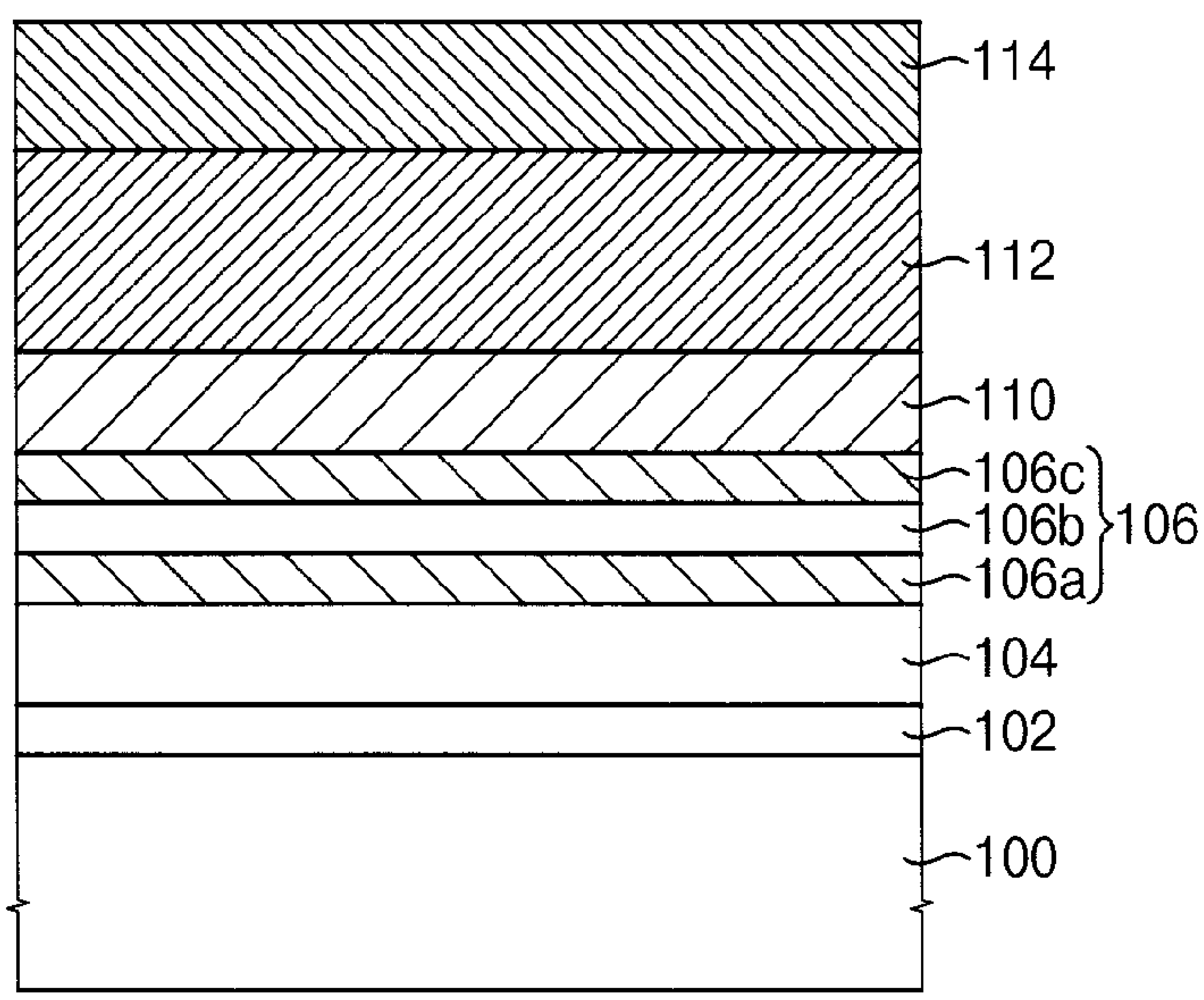
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FIG. 2B

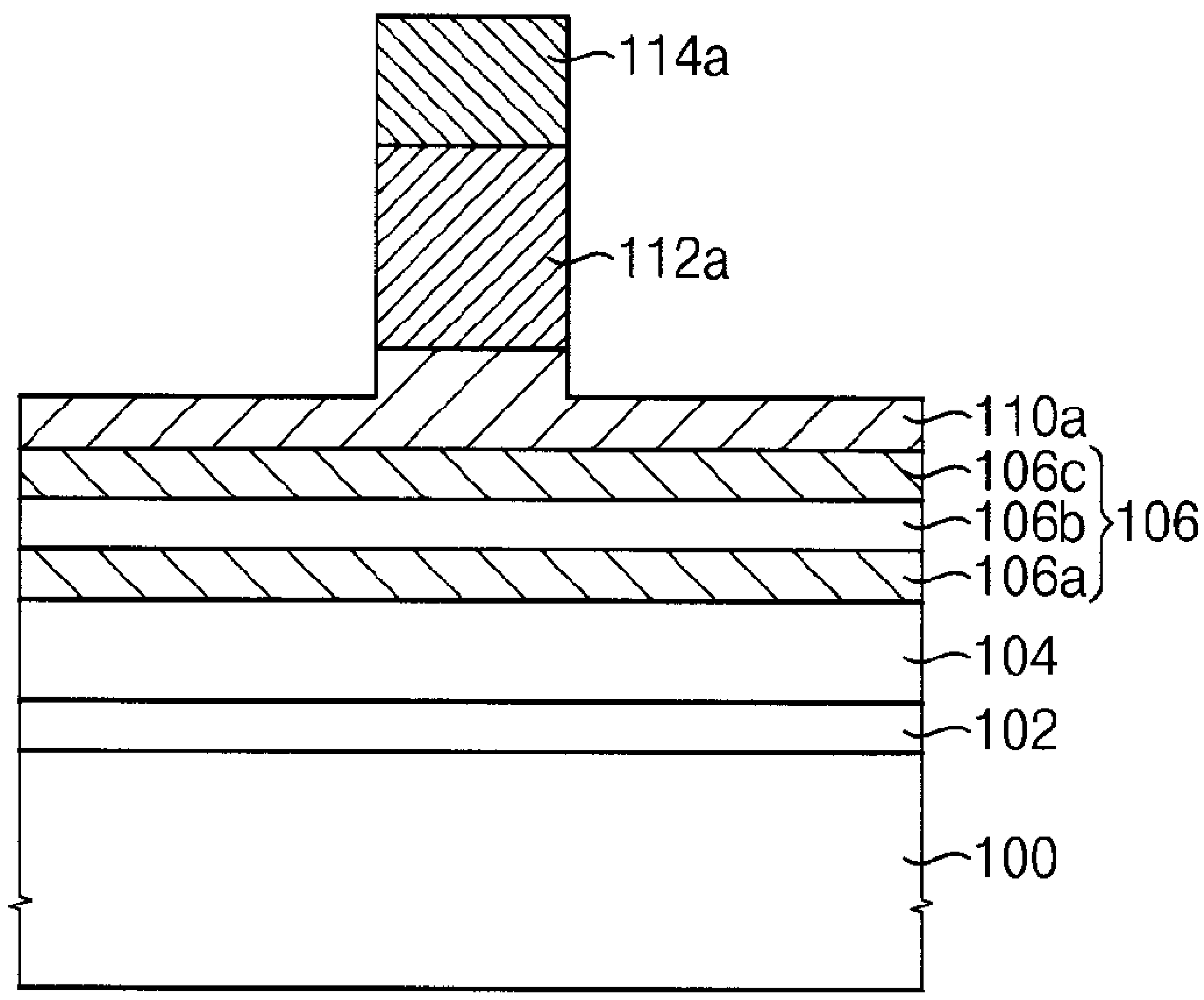
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FIG. 2C

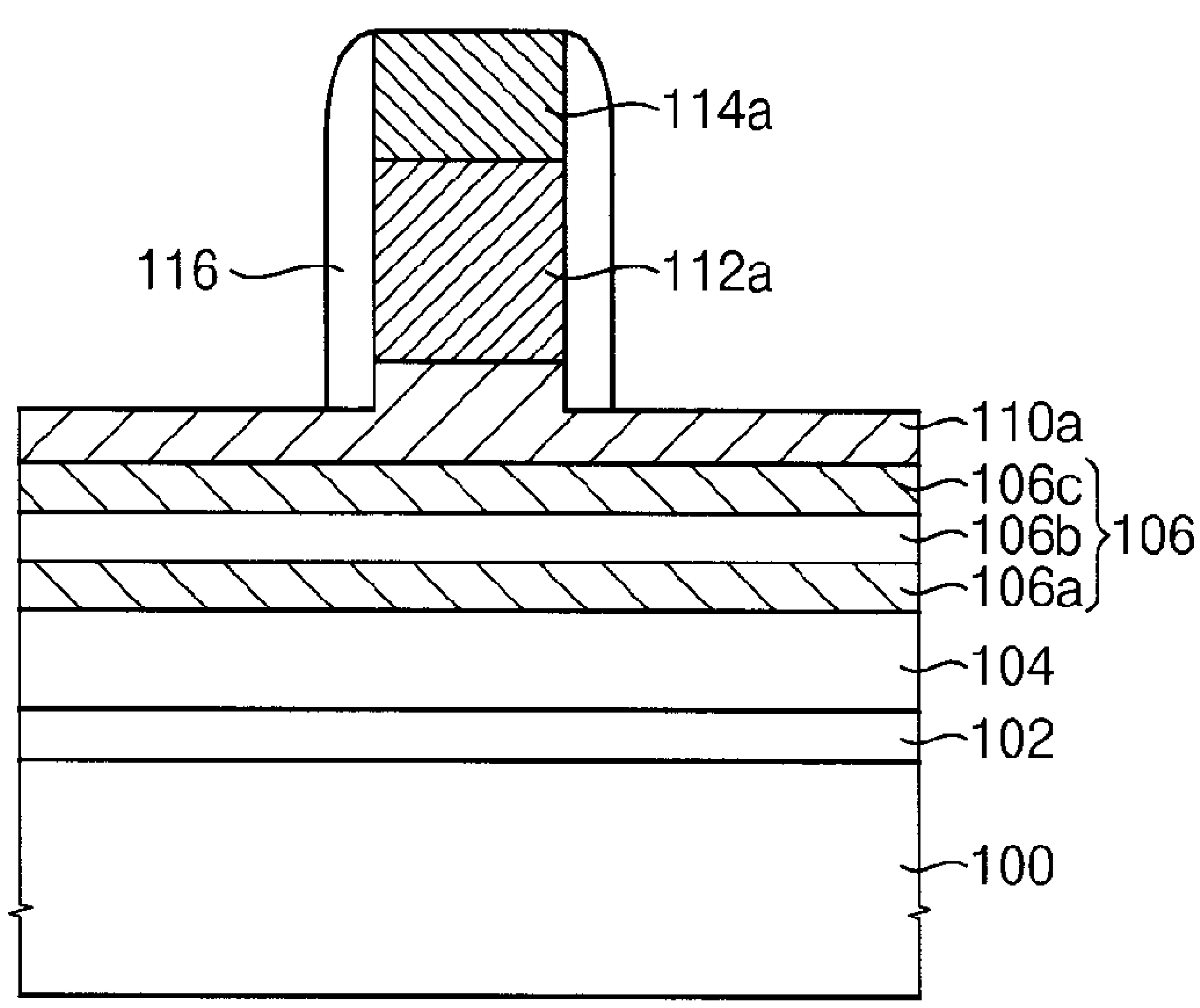
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FIG. 2D

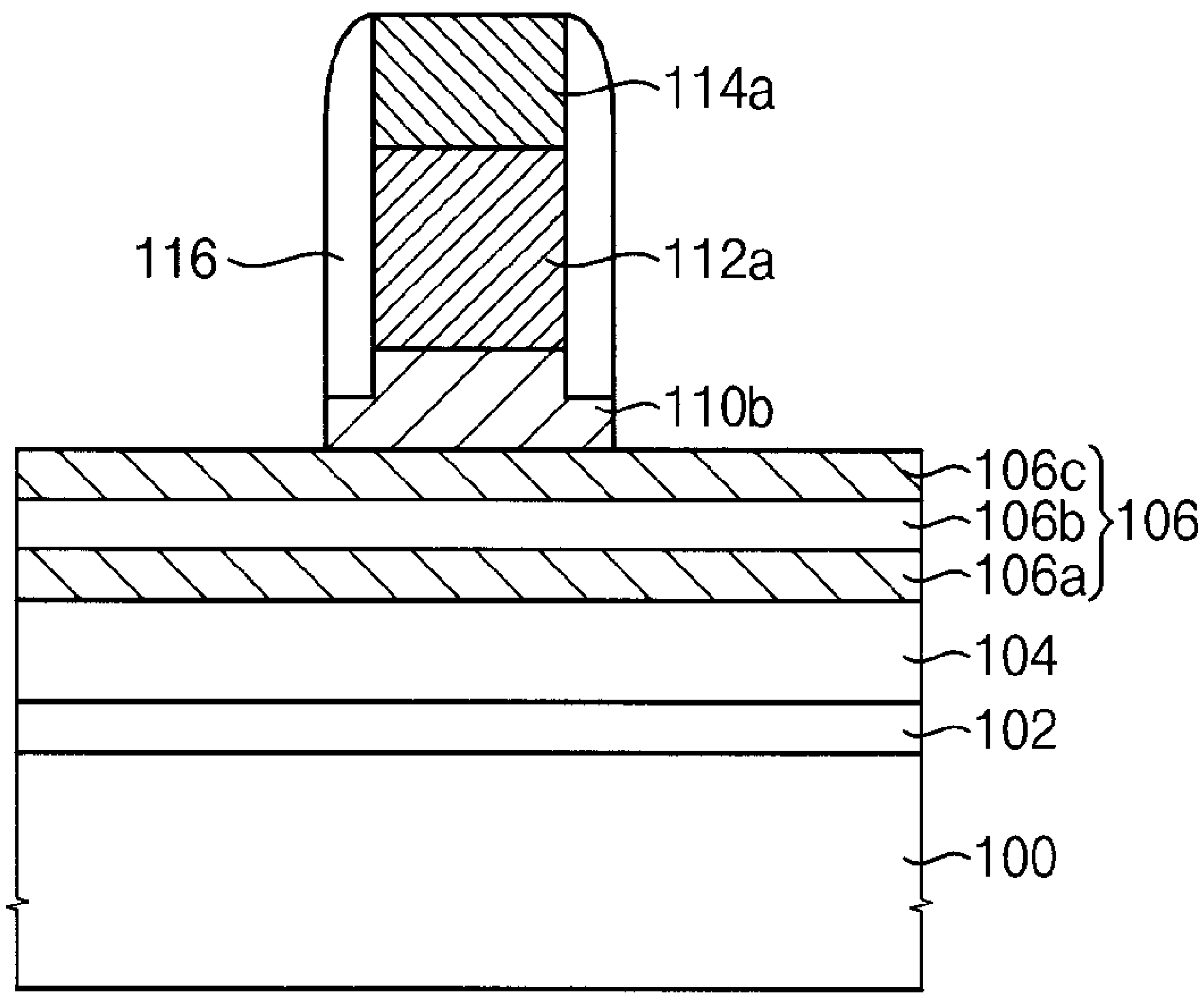
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FIG. 2E

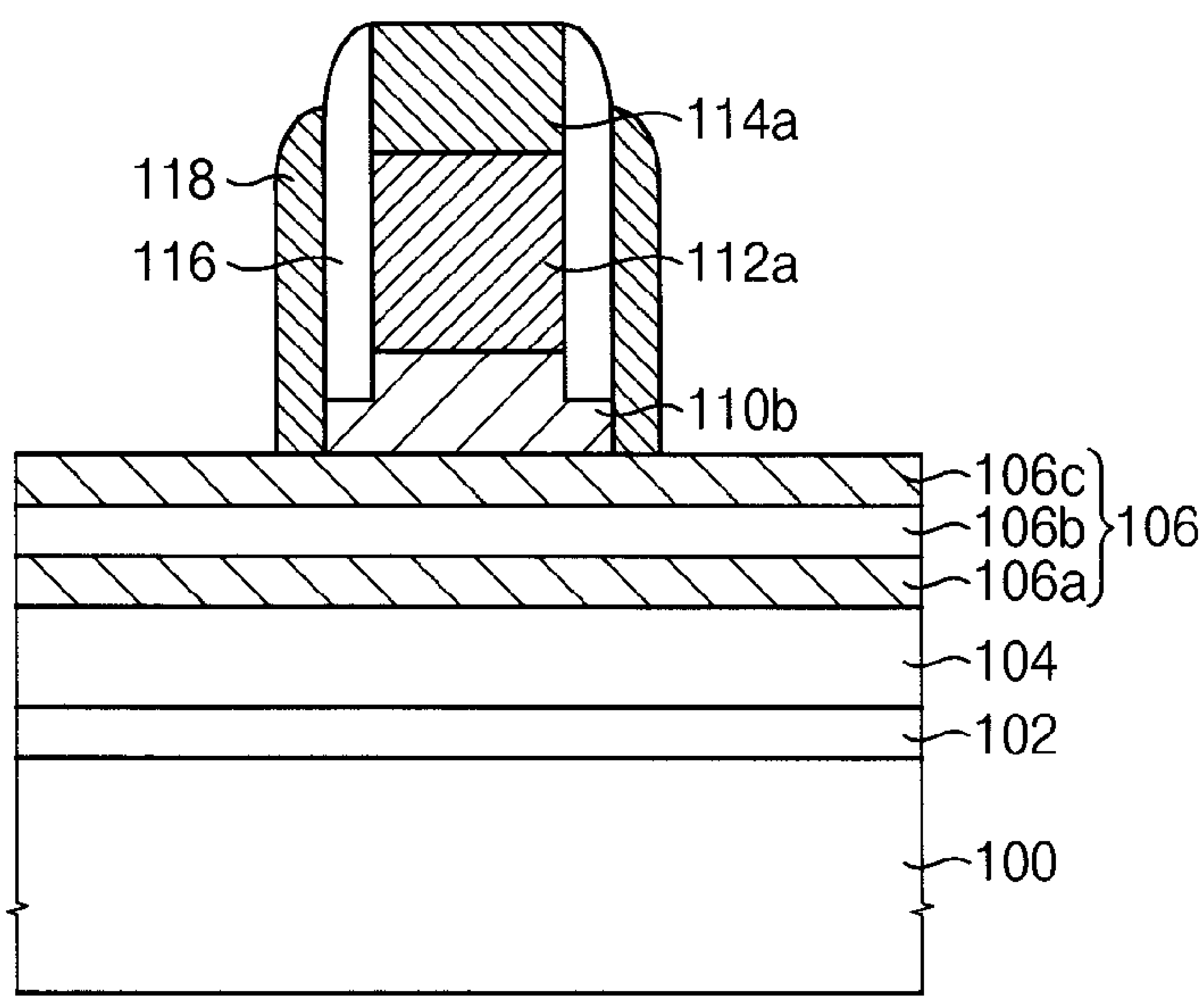
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FIG. 3

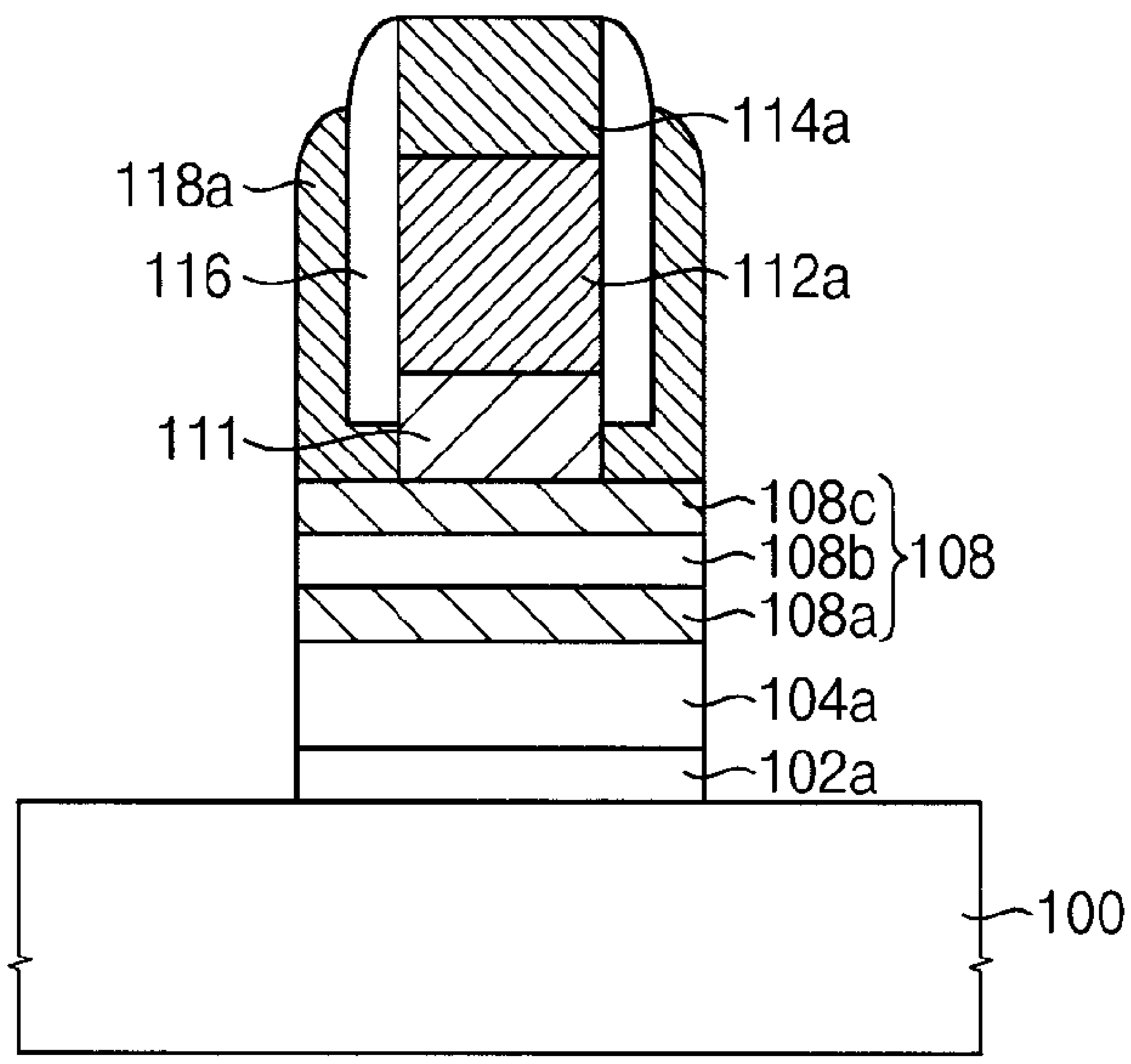
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FIG. 4A

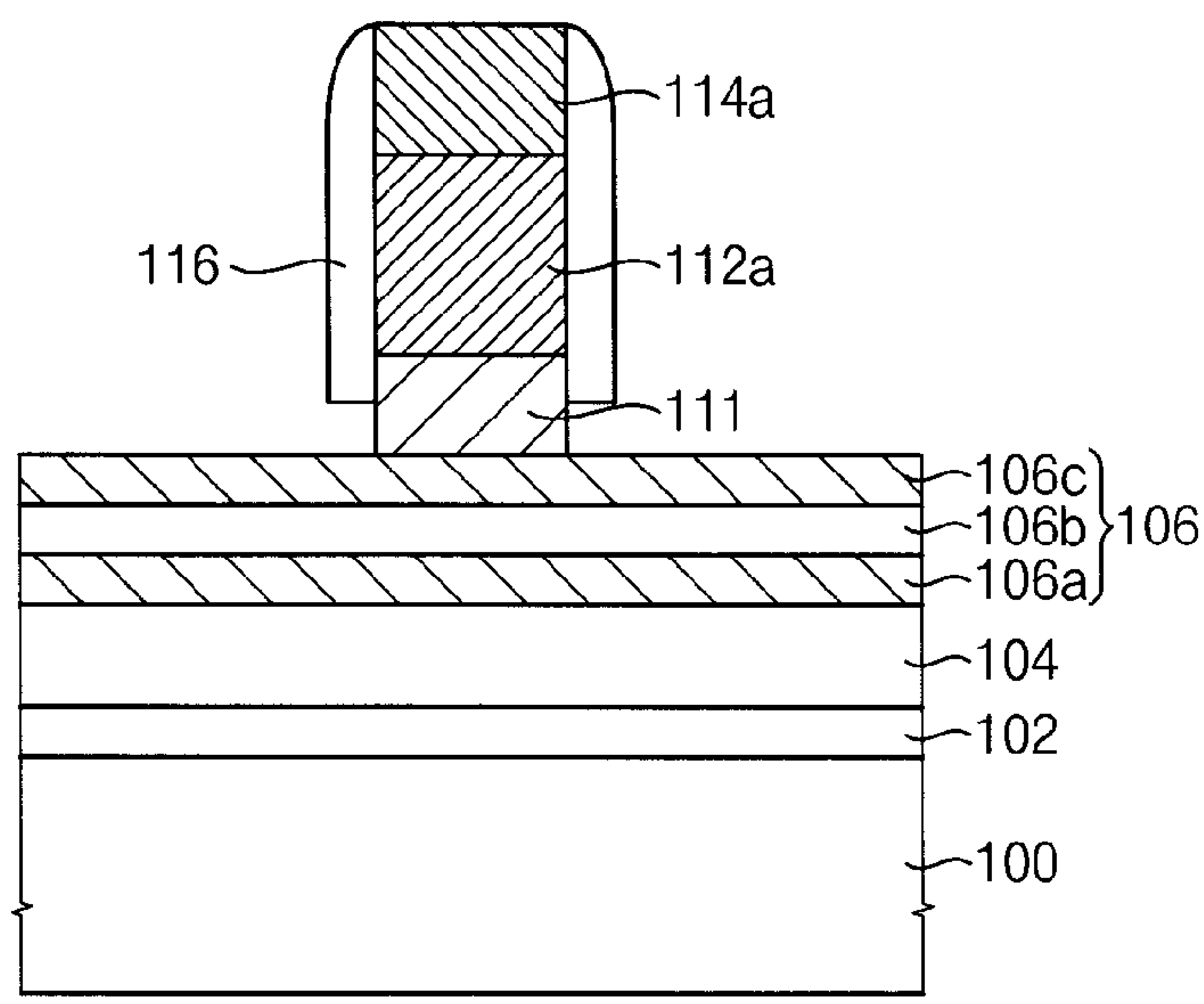
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FIG. 4B

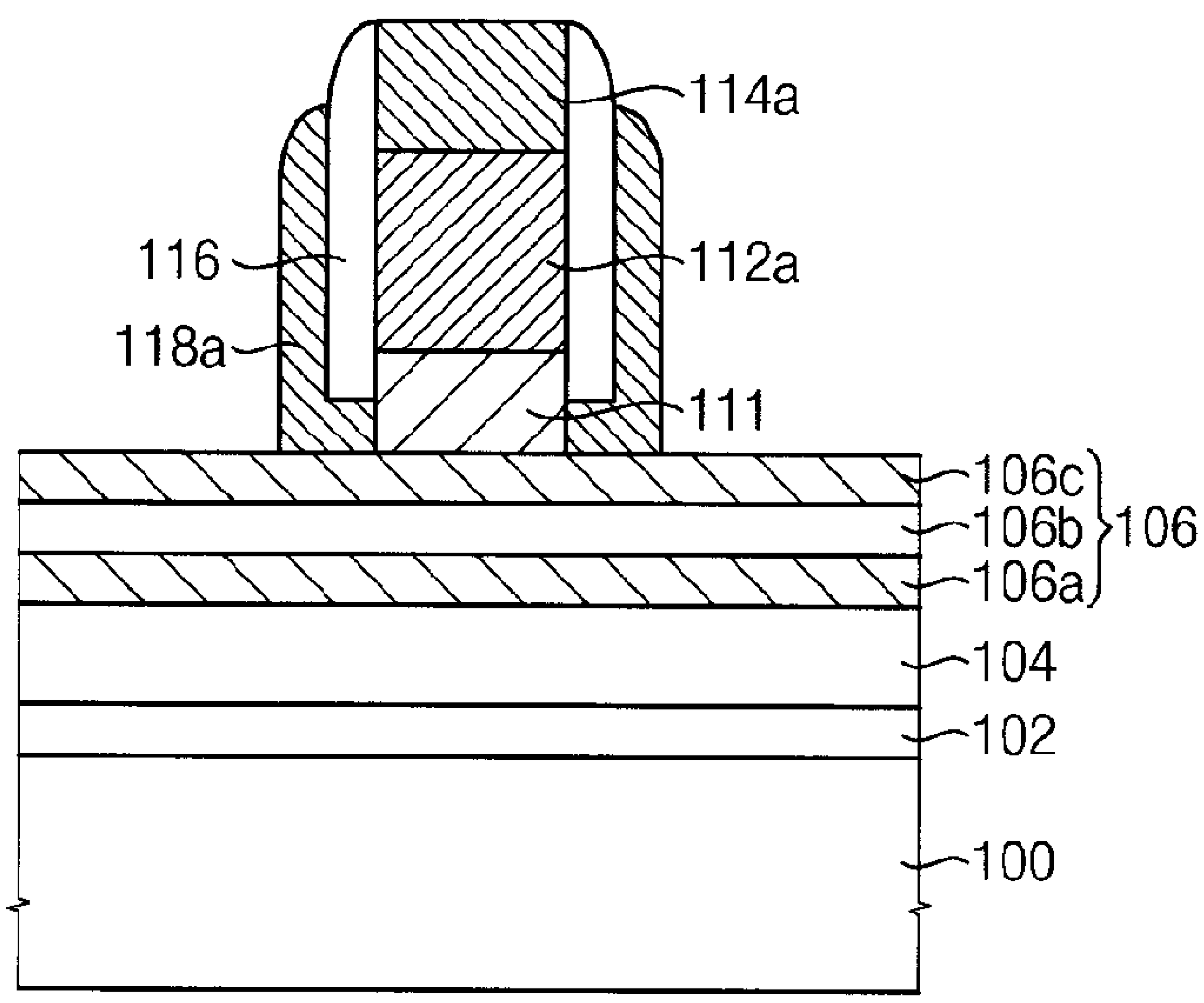
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FIG. 5

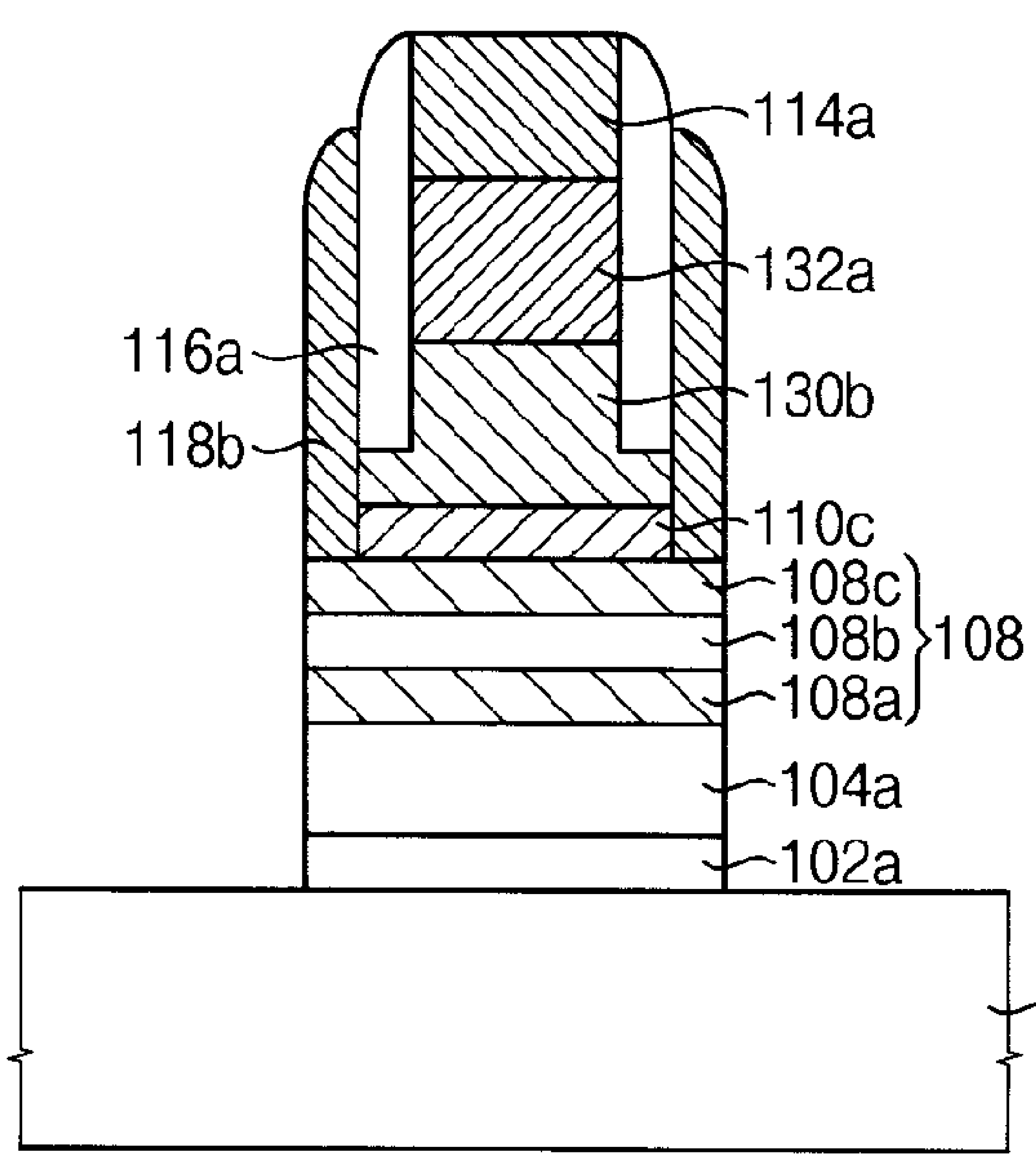
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FIG. 6A

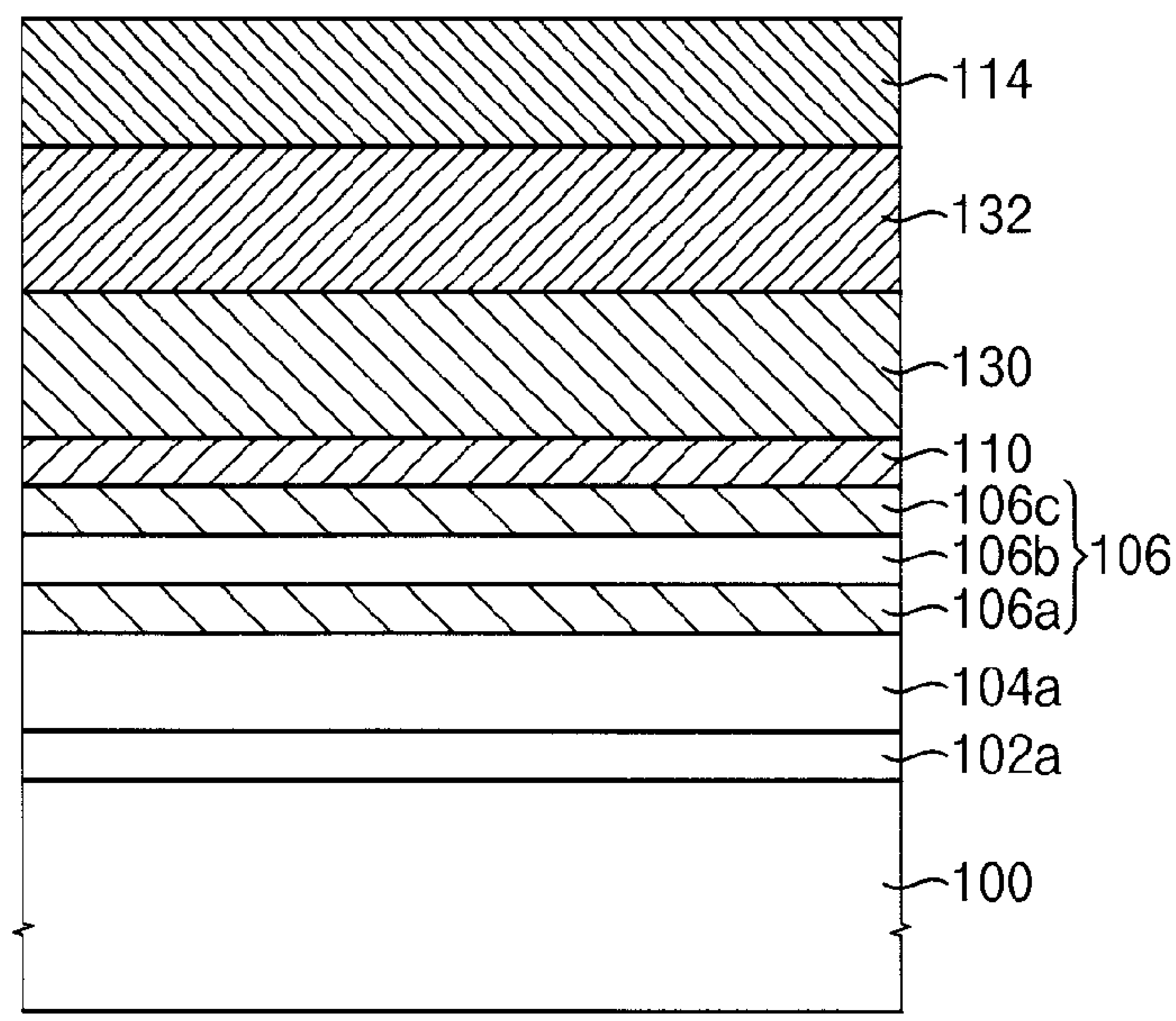
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FIG. 6B

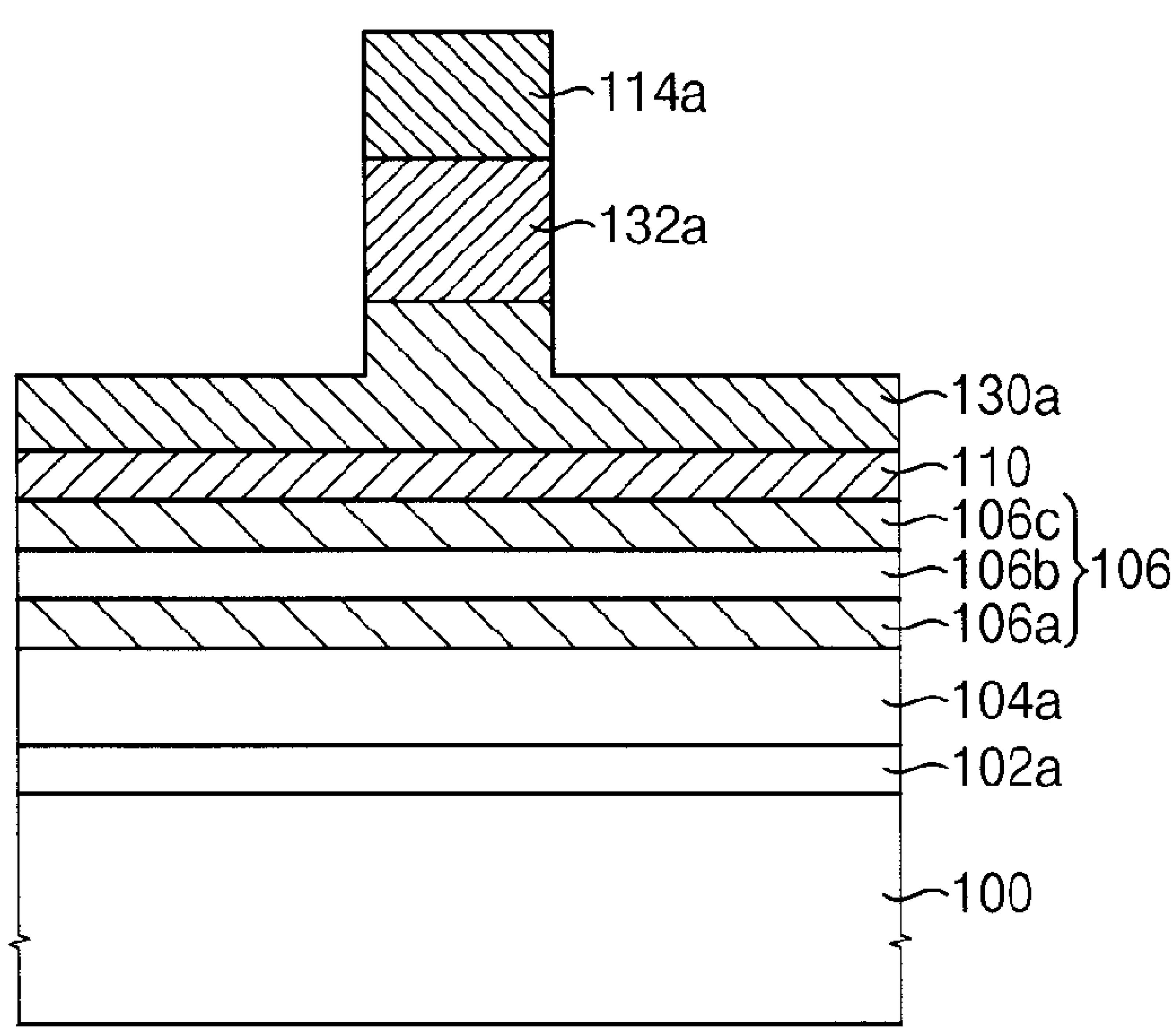
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FIG. 6C

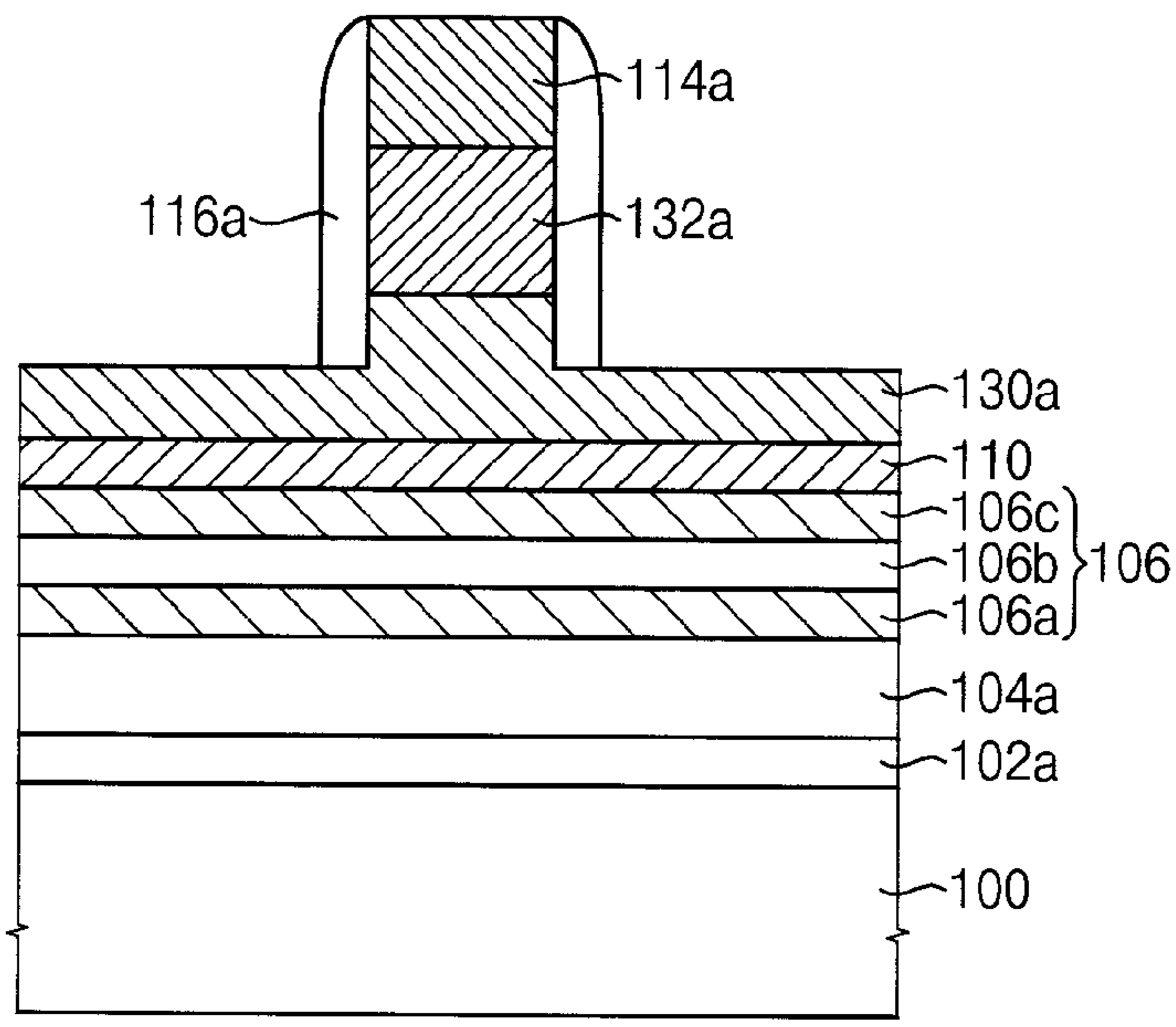
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FIG. 6D

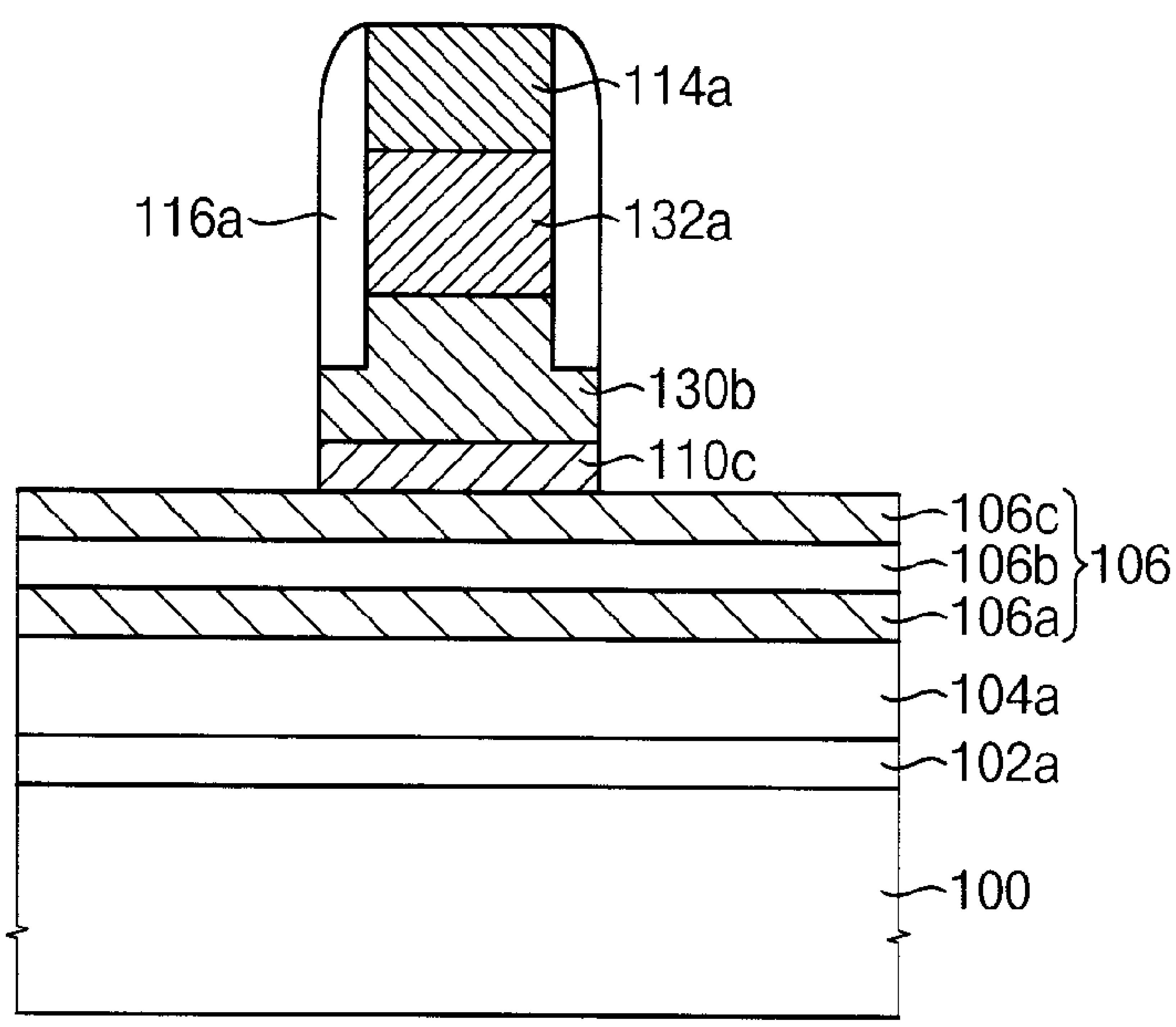
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FIG. 6E

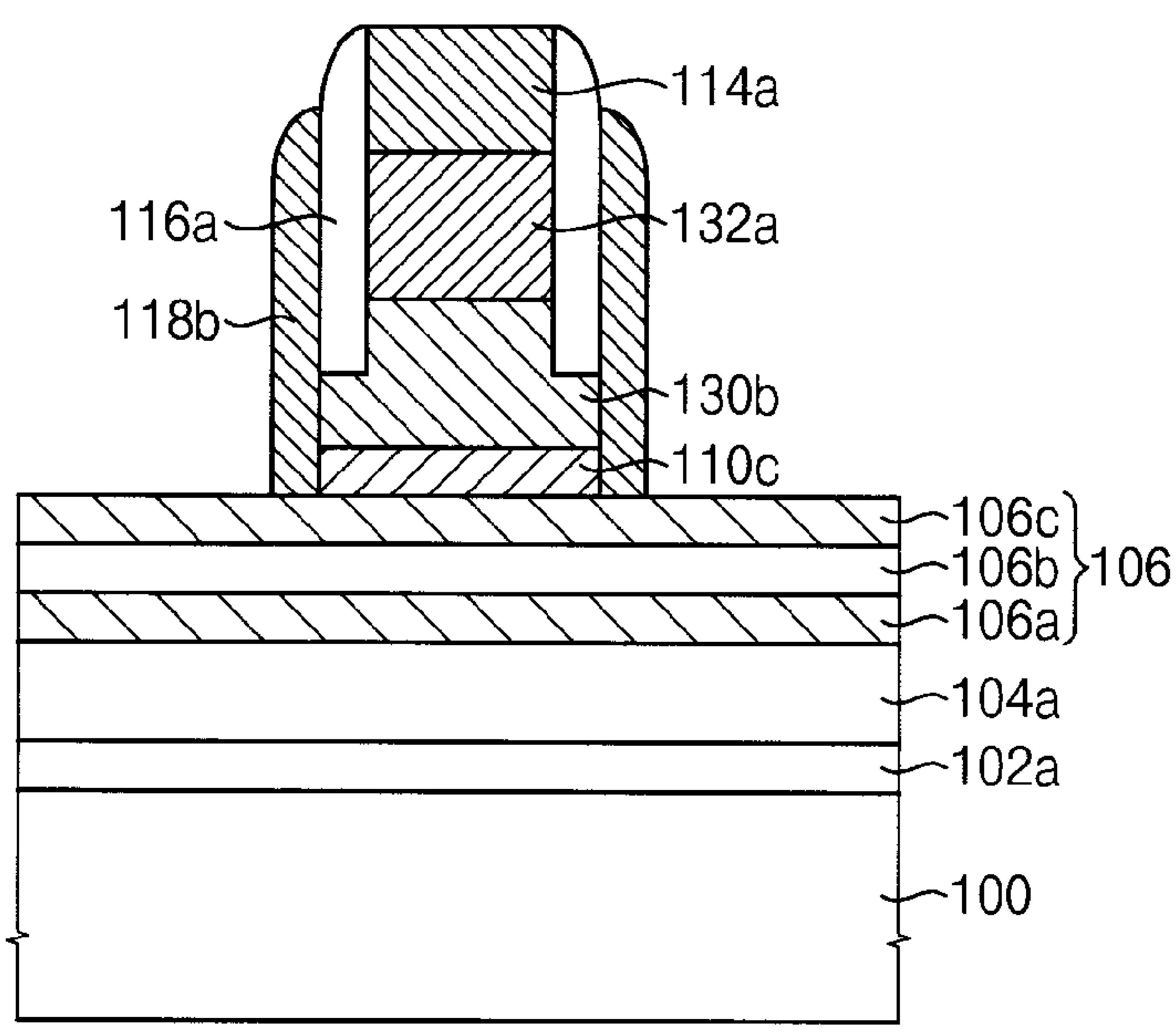
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FIG. 7

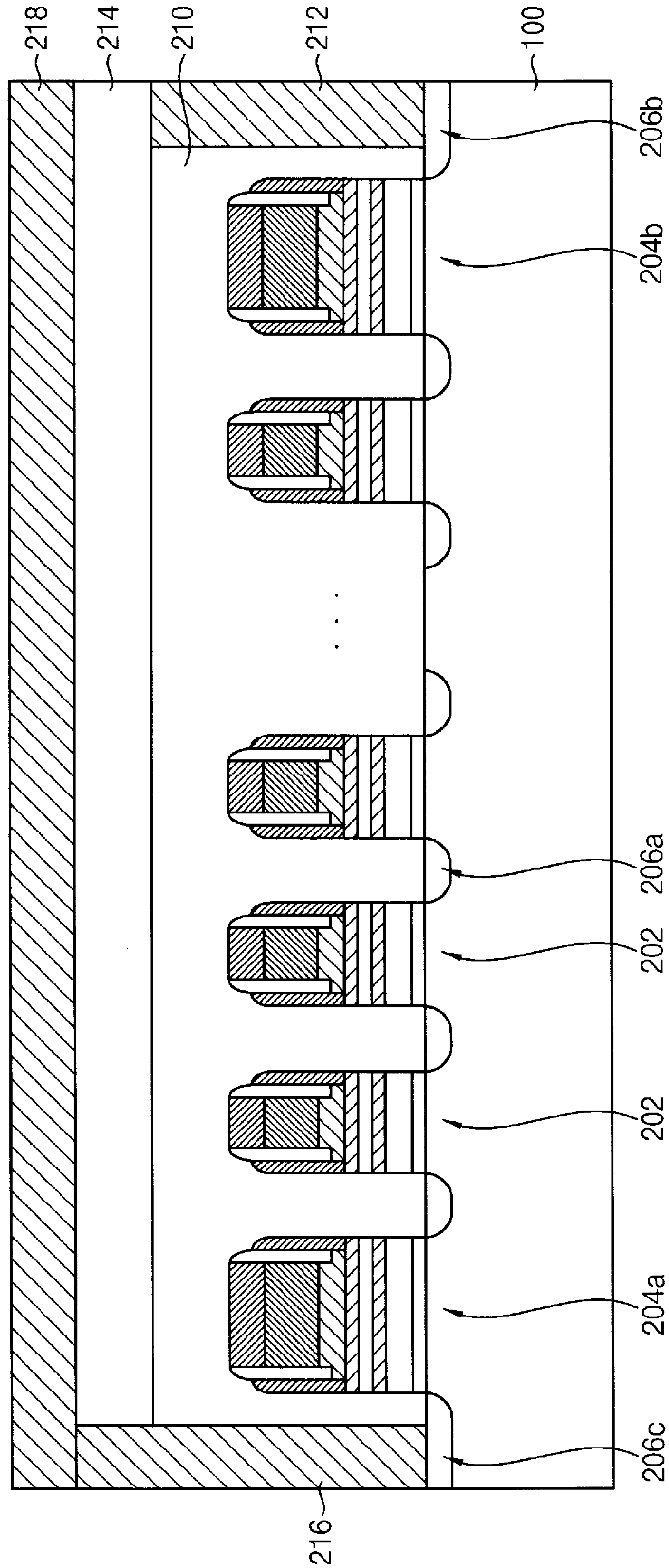

FIG. 8A

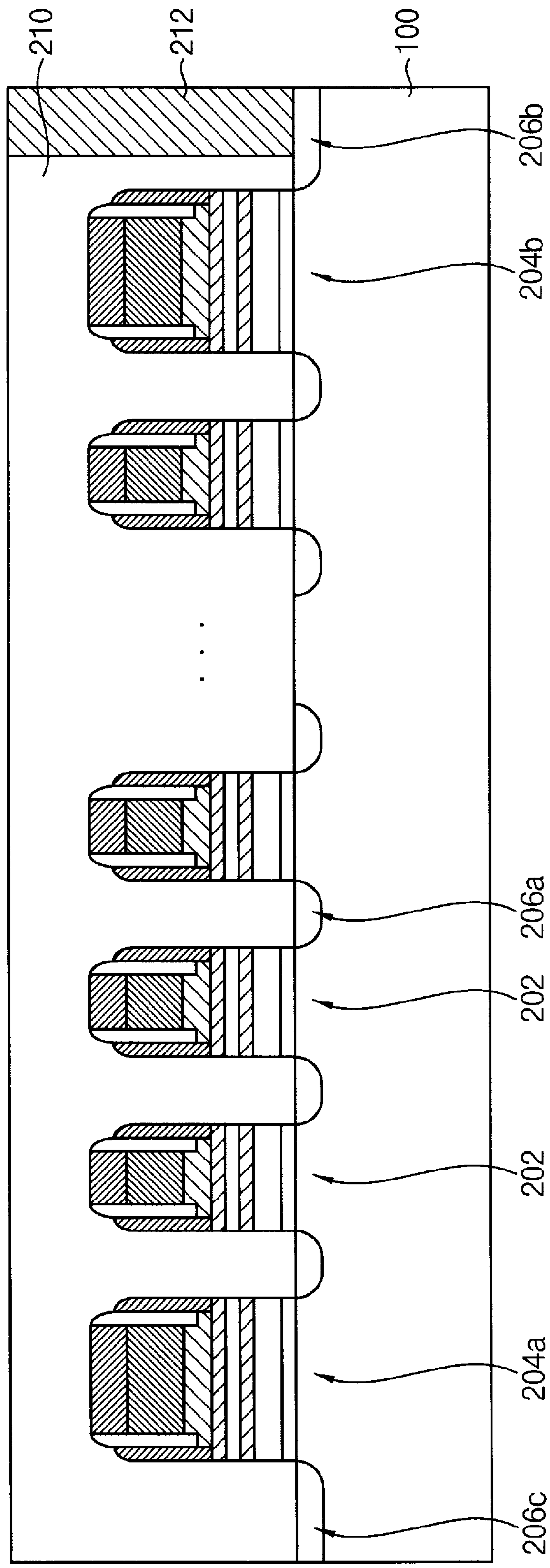

FIG. 8B

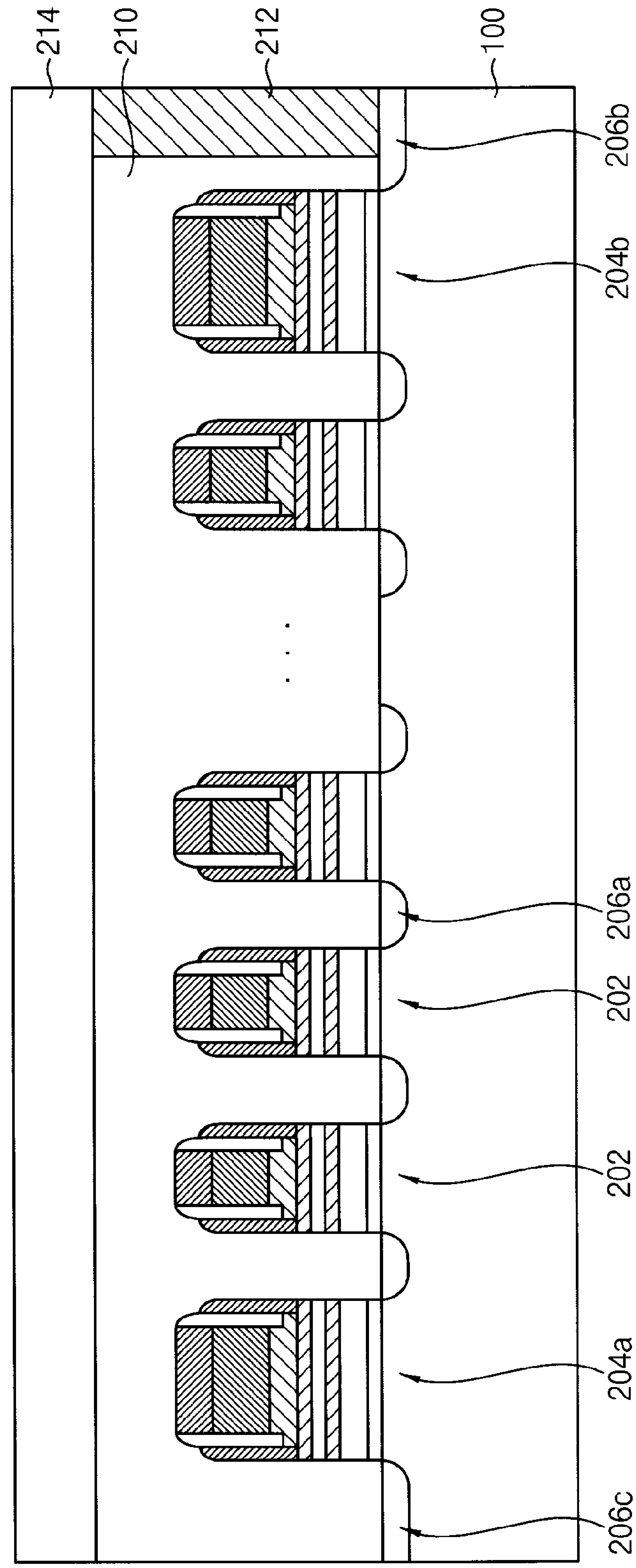

FIG. 9A

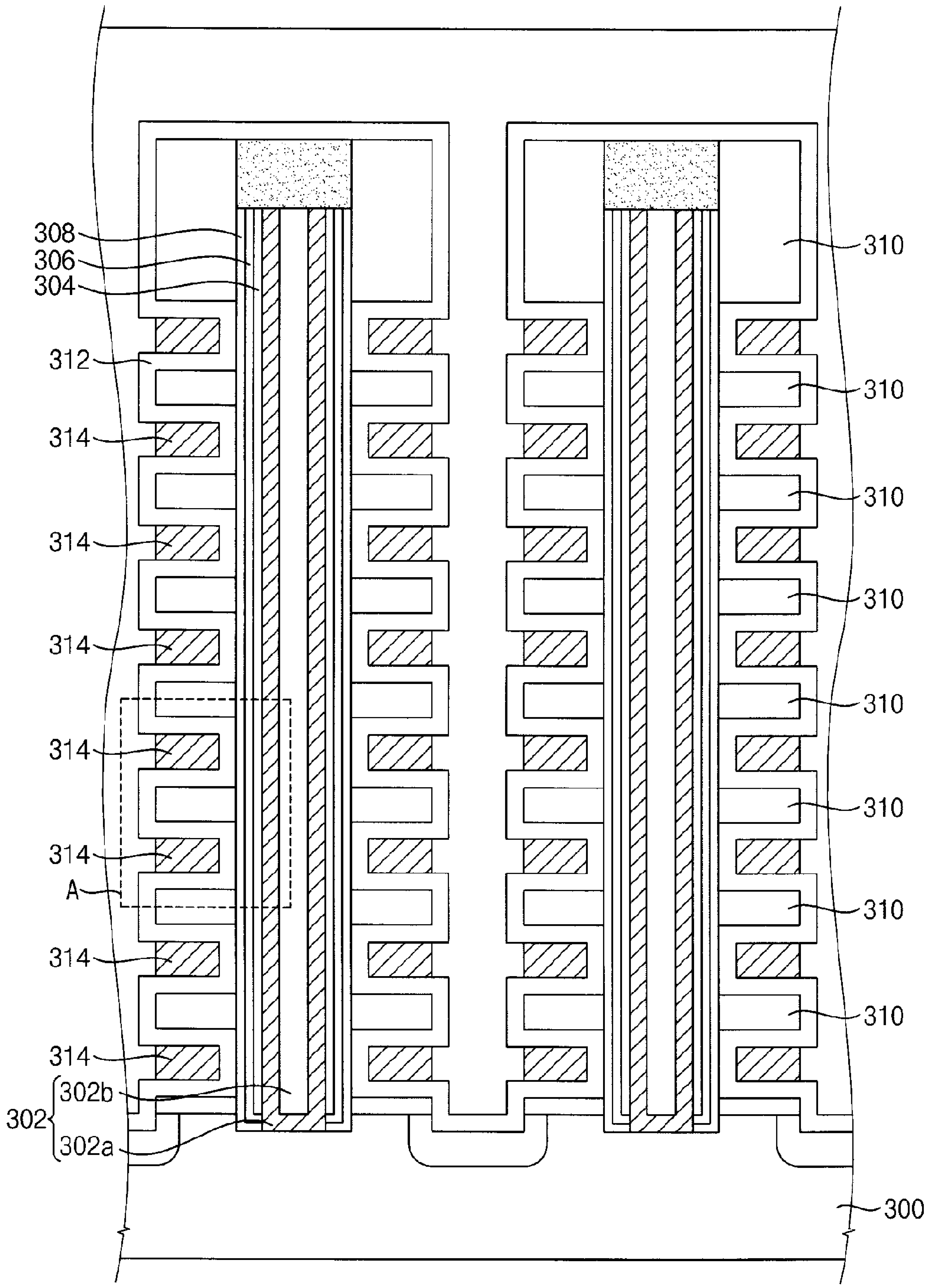
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FIG. 9B

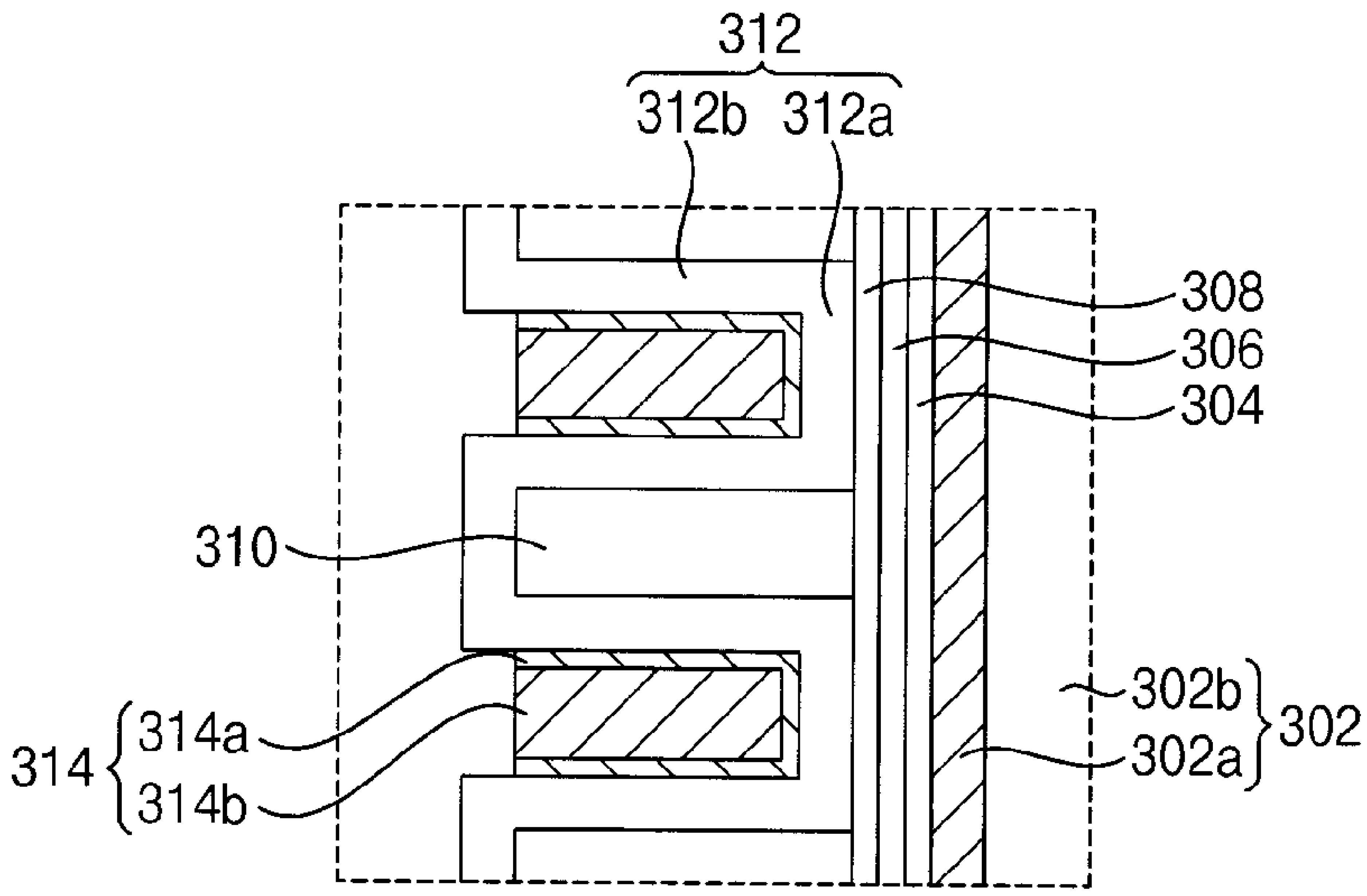
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FIG. 10

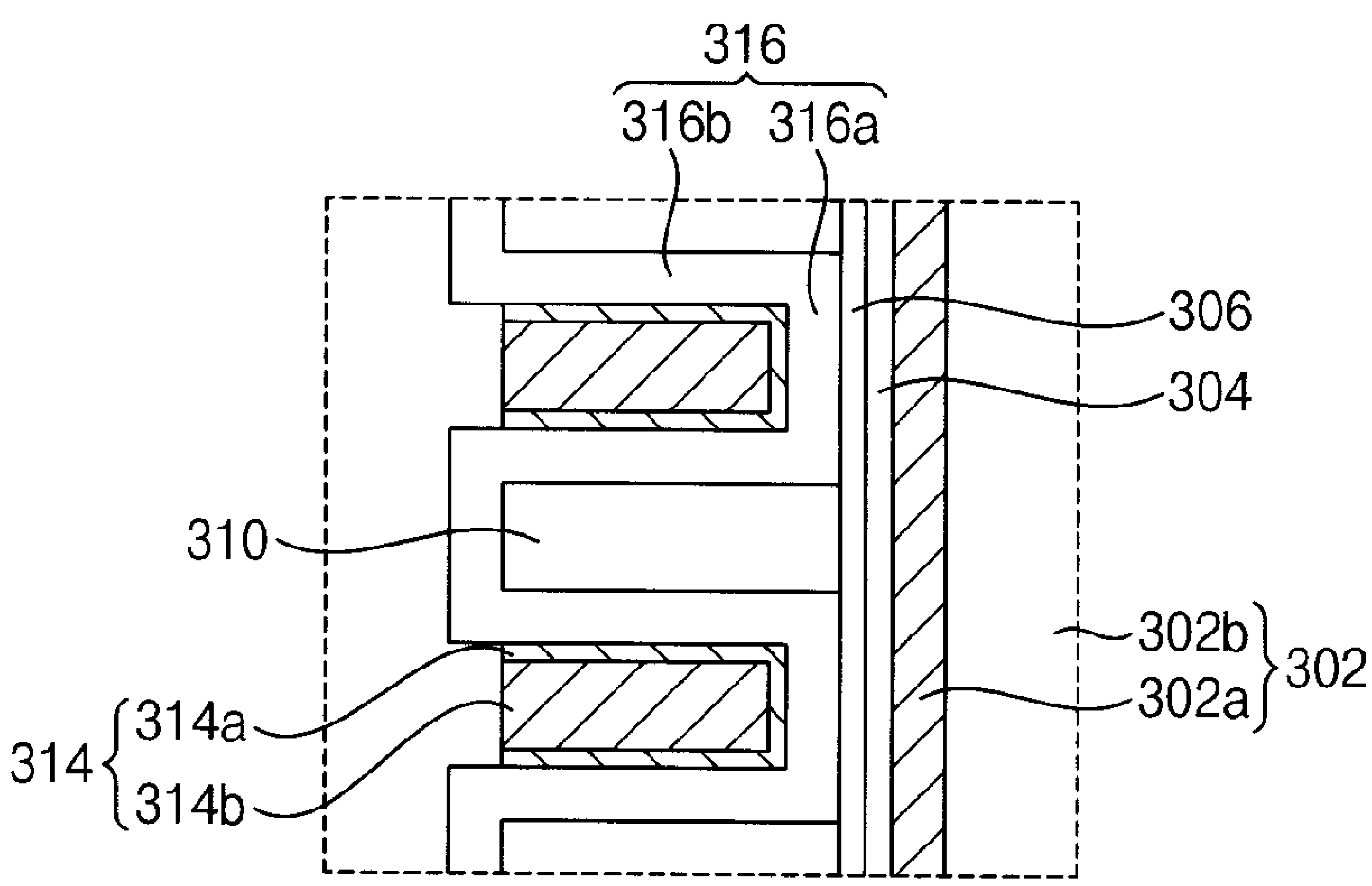
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FIG. 11A

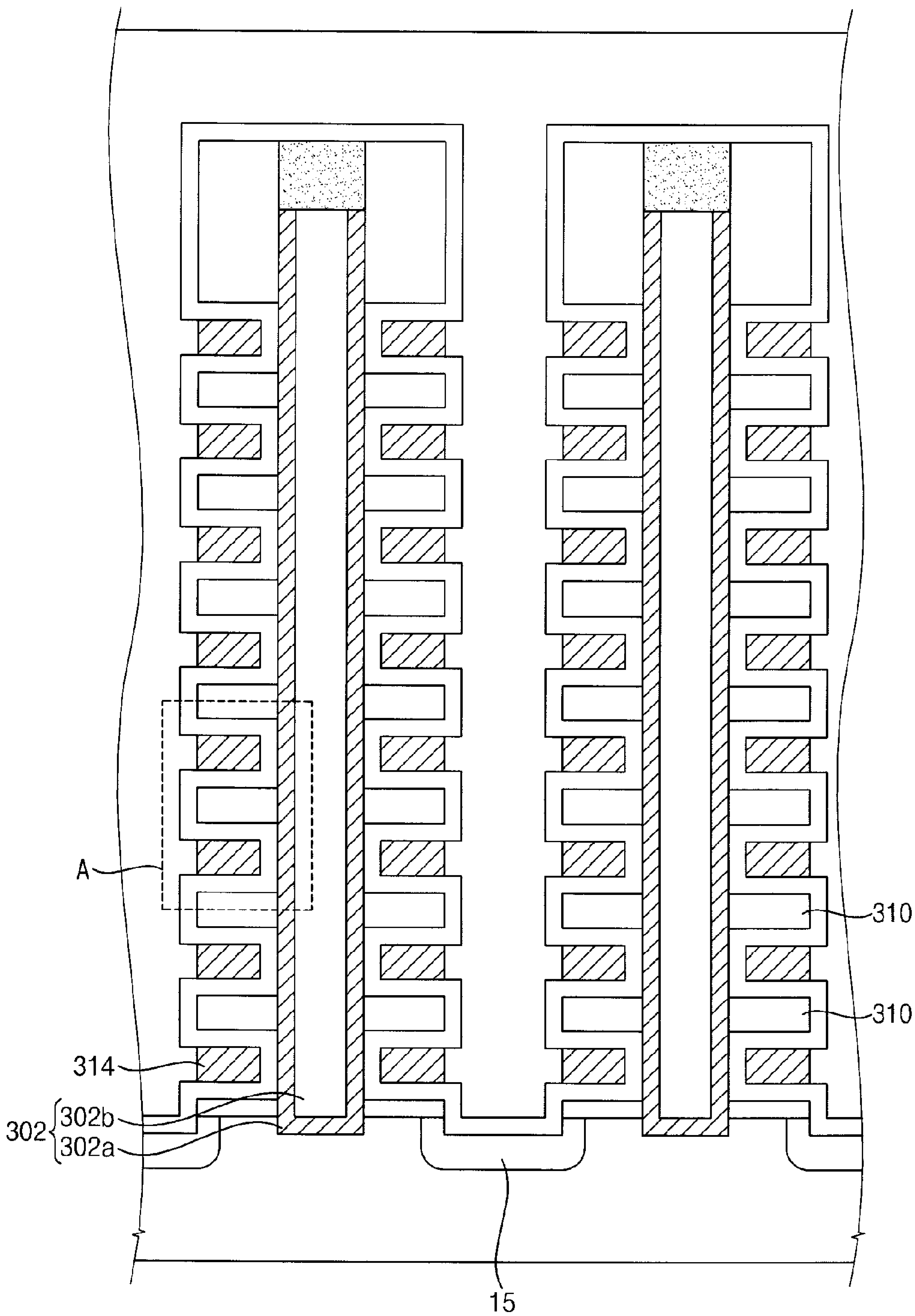
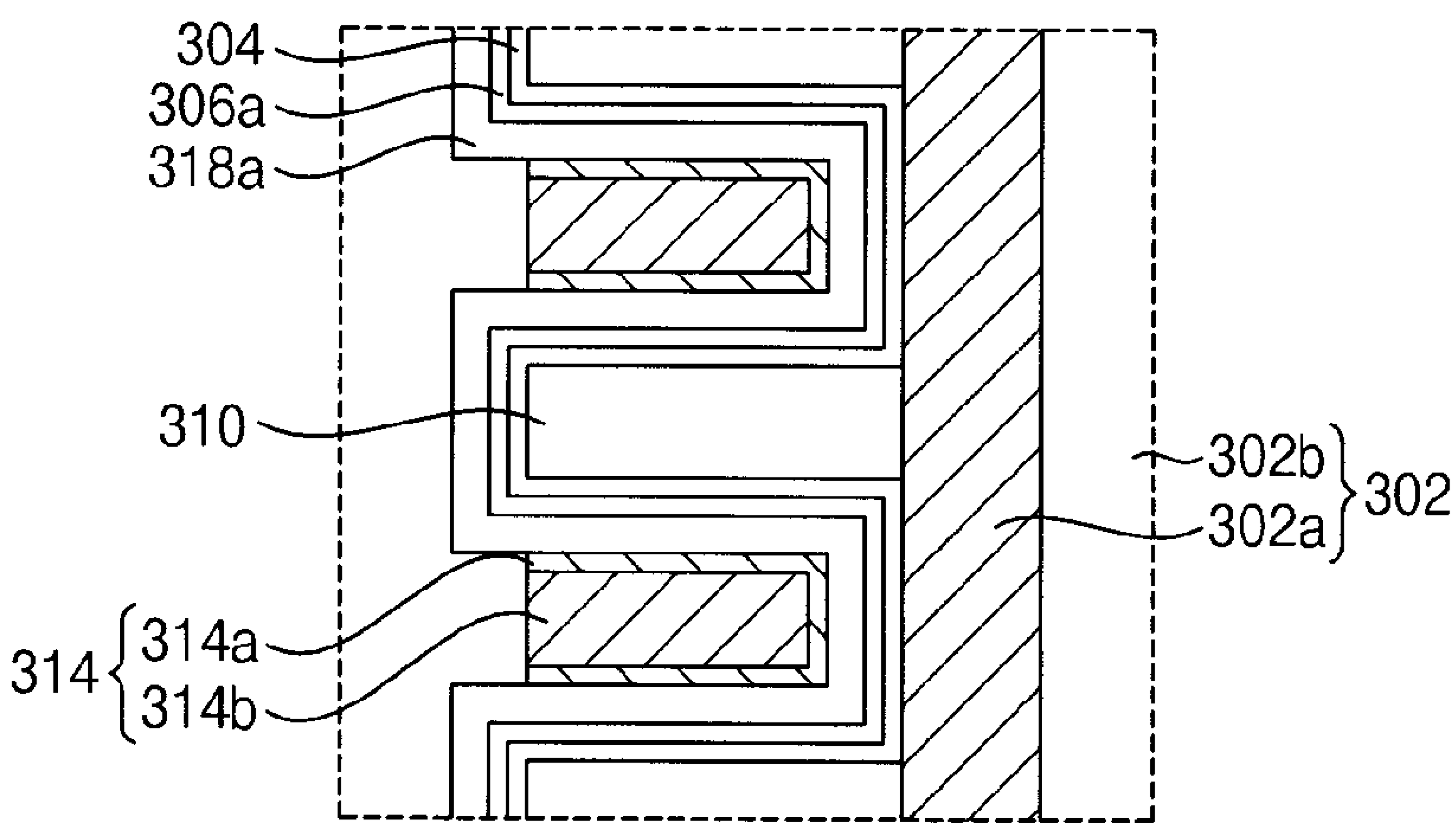


FIG. 11B



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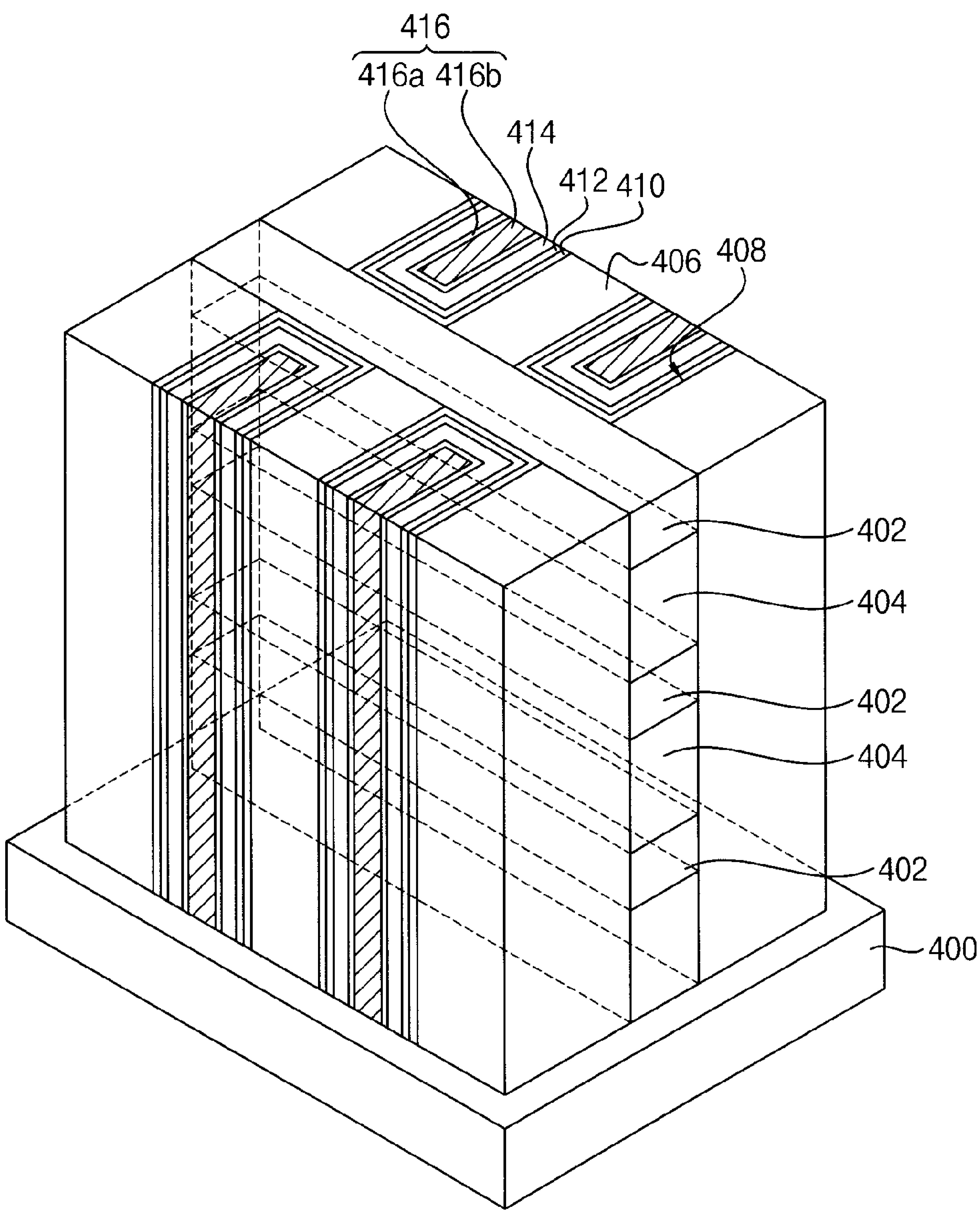

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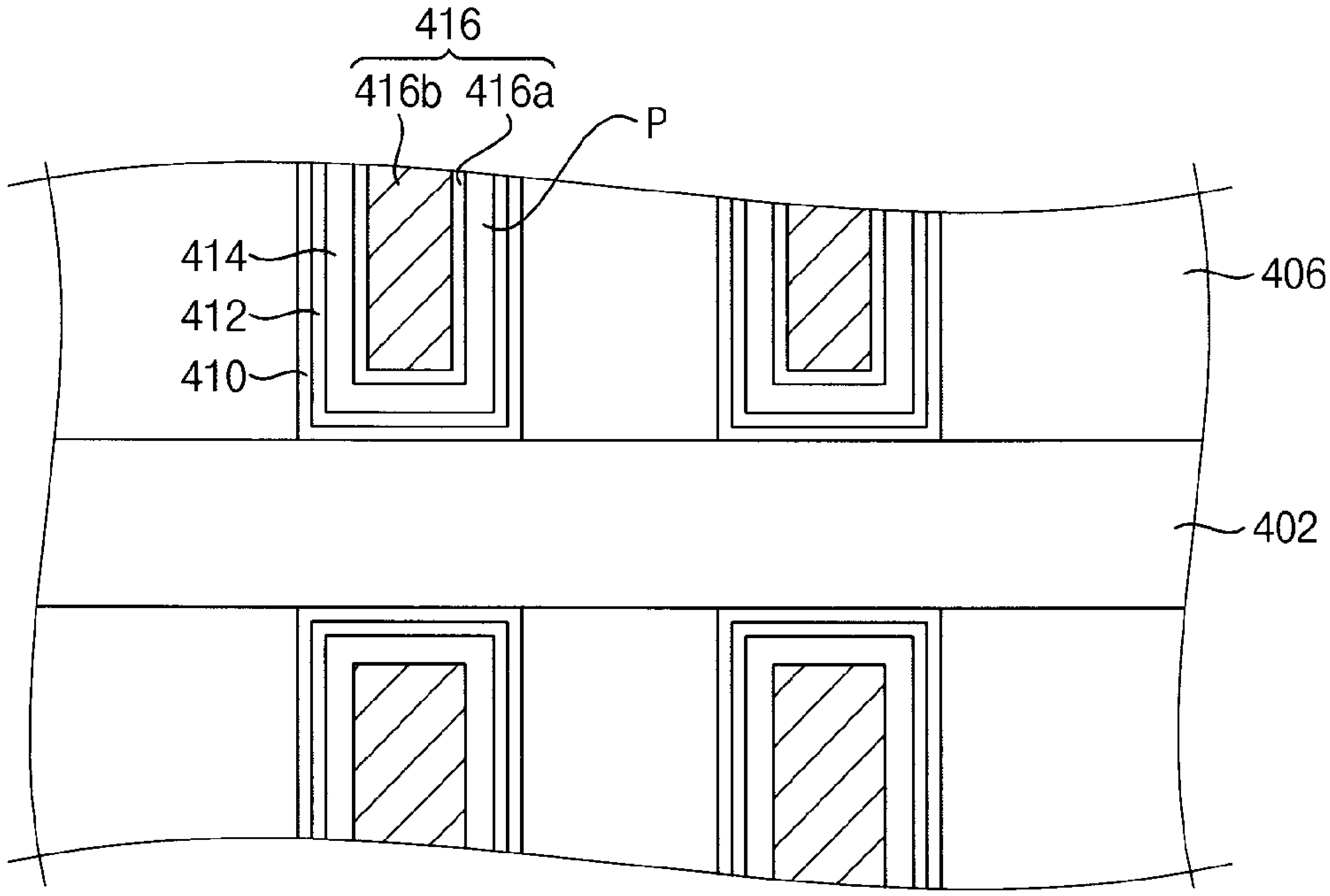


FIG. 13A

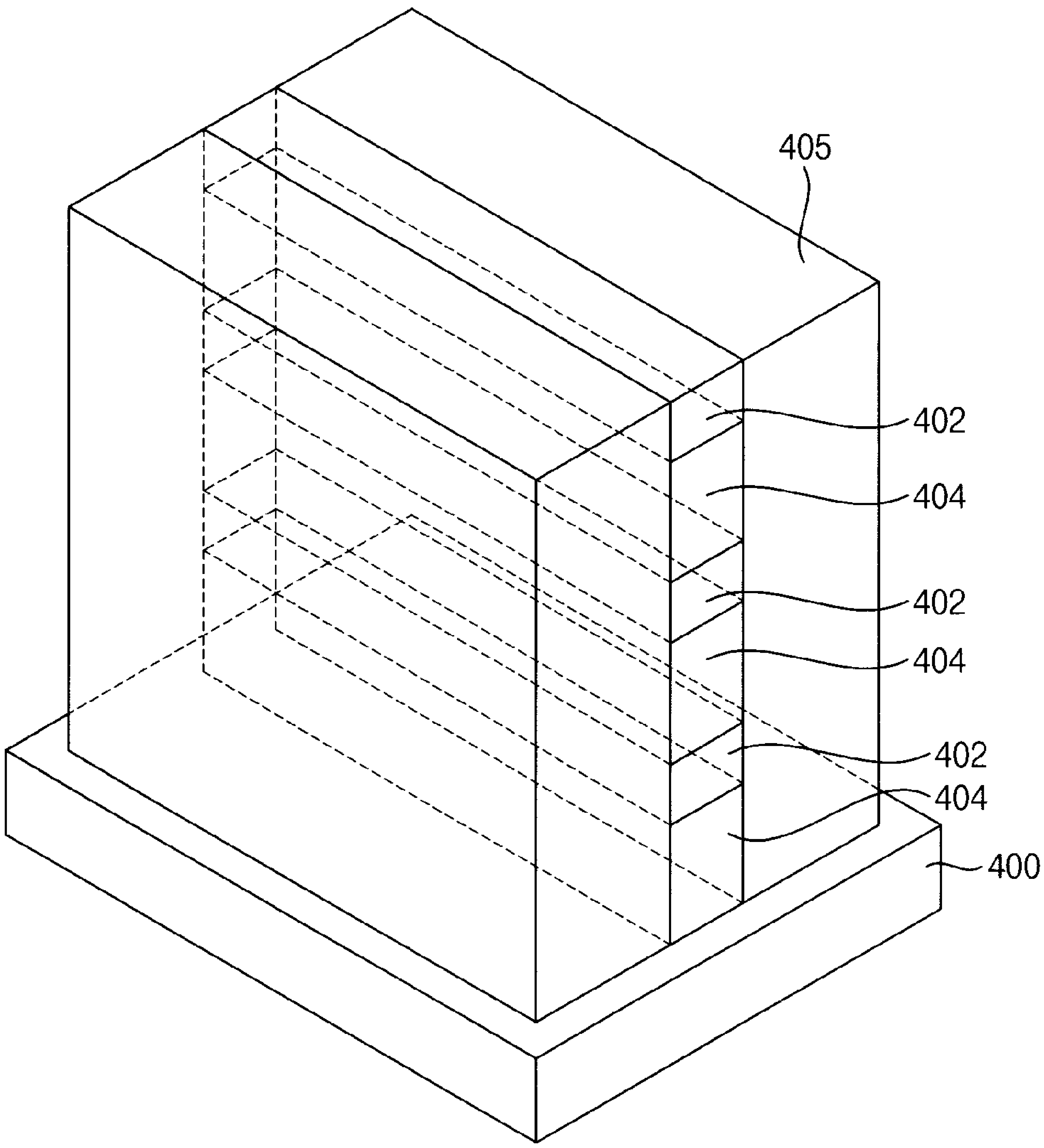


FIG. 13B

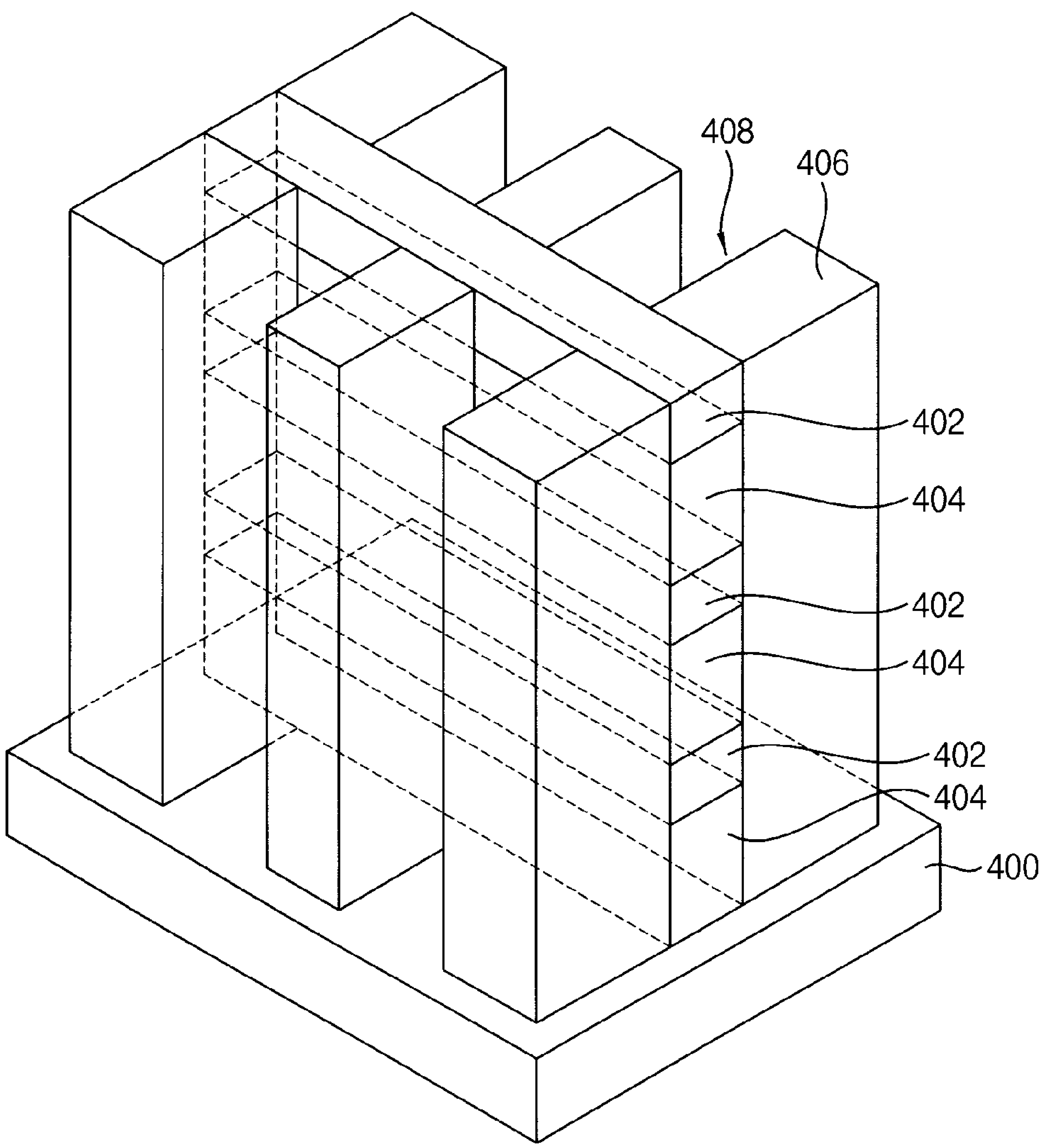


FIG. 14A

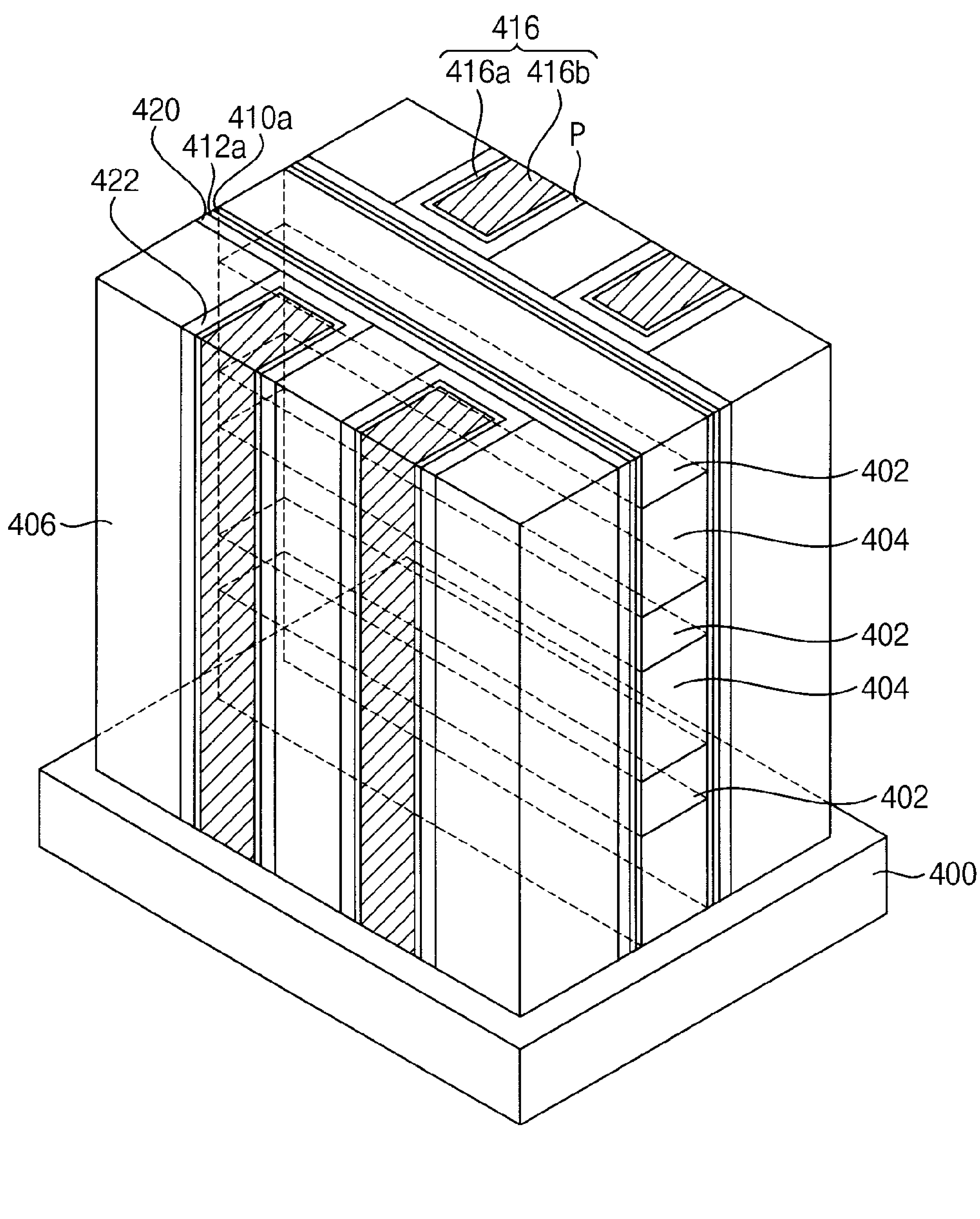


FIG. 14B

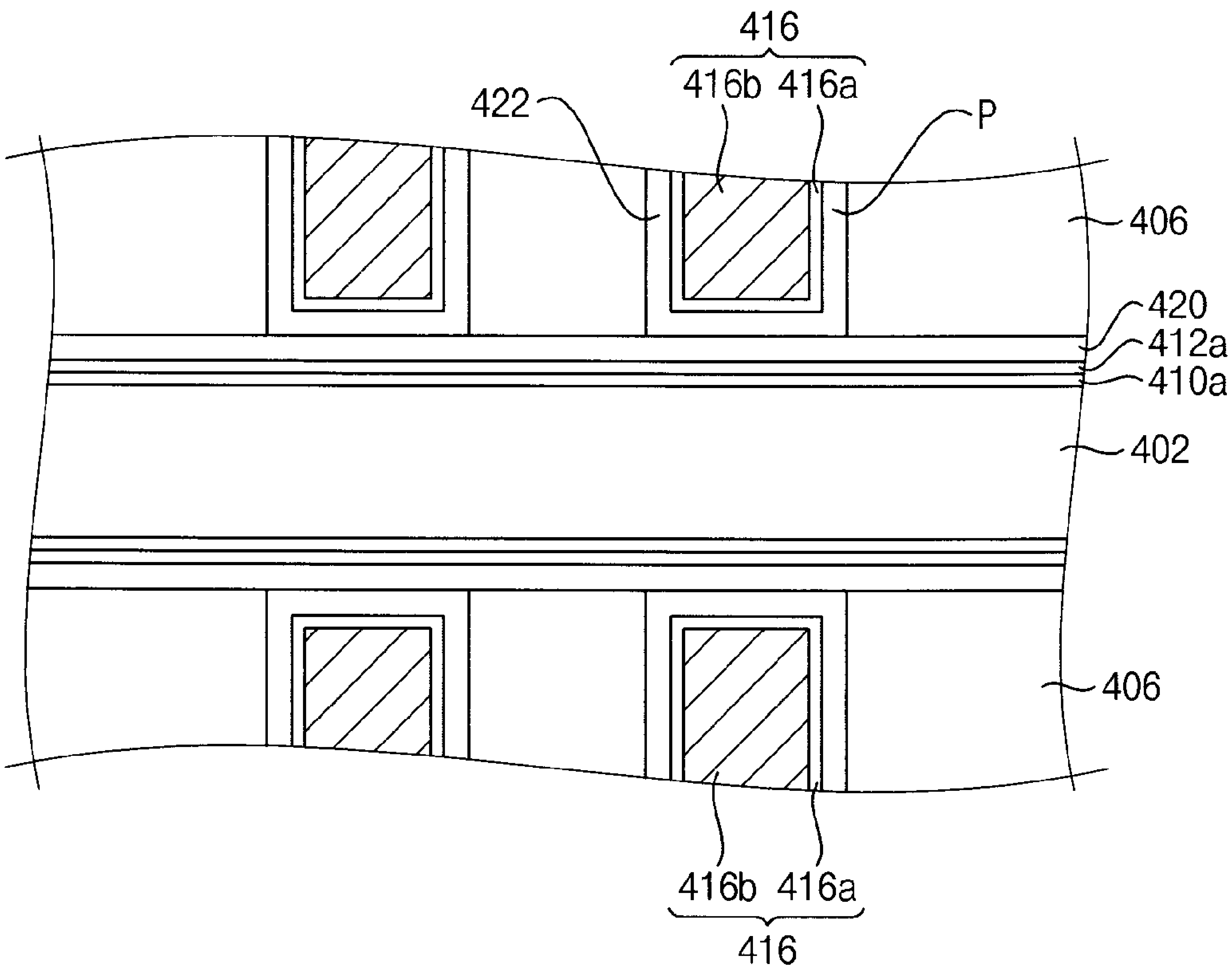


FIG. 15A

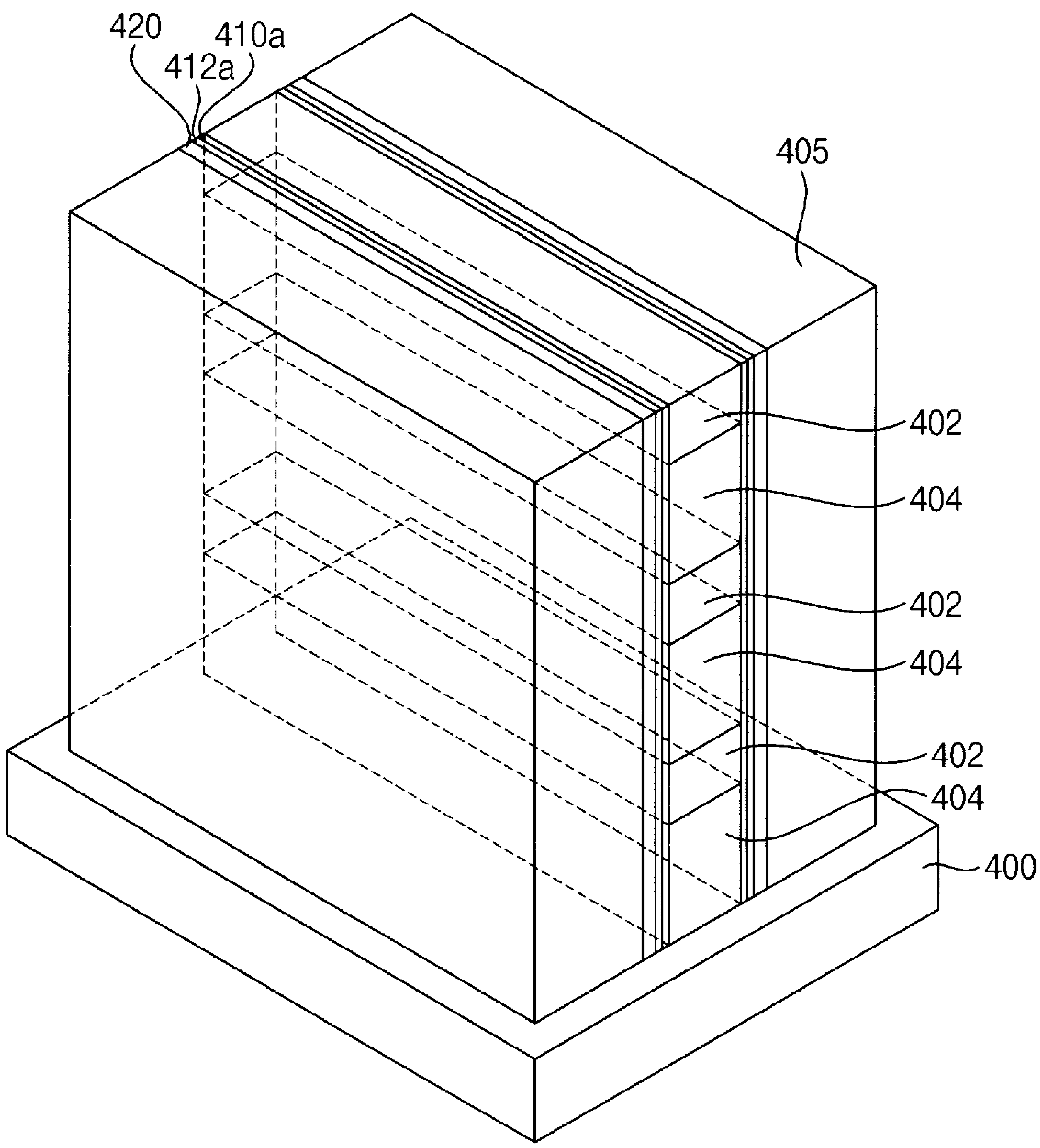


FIG. 15B

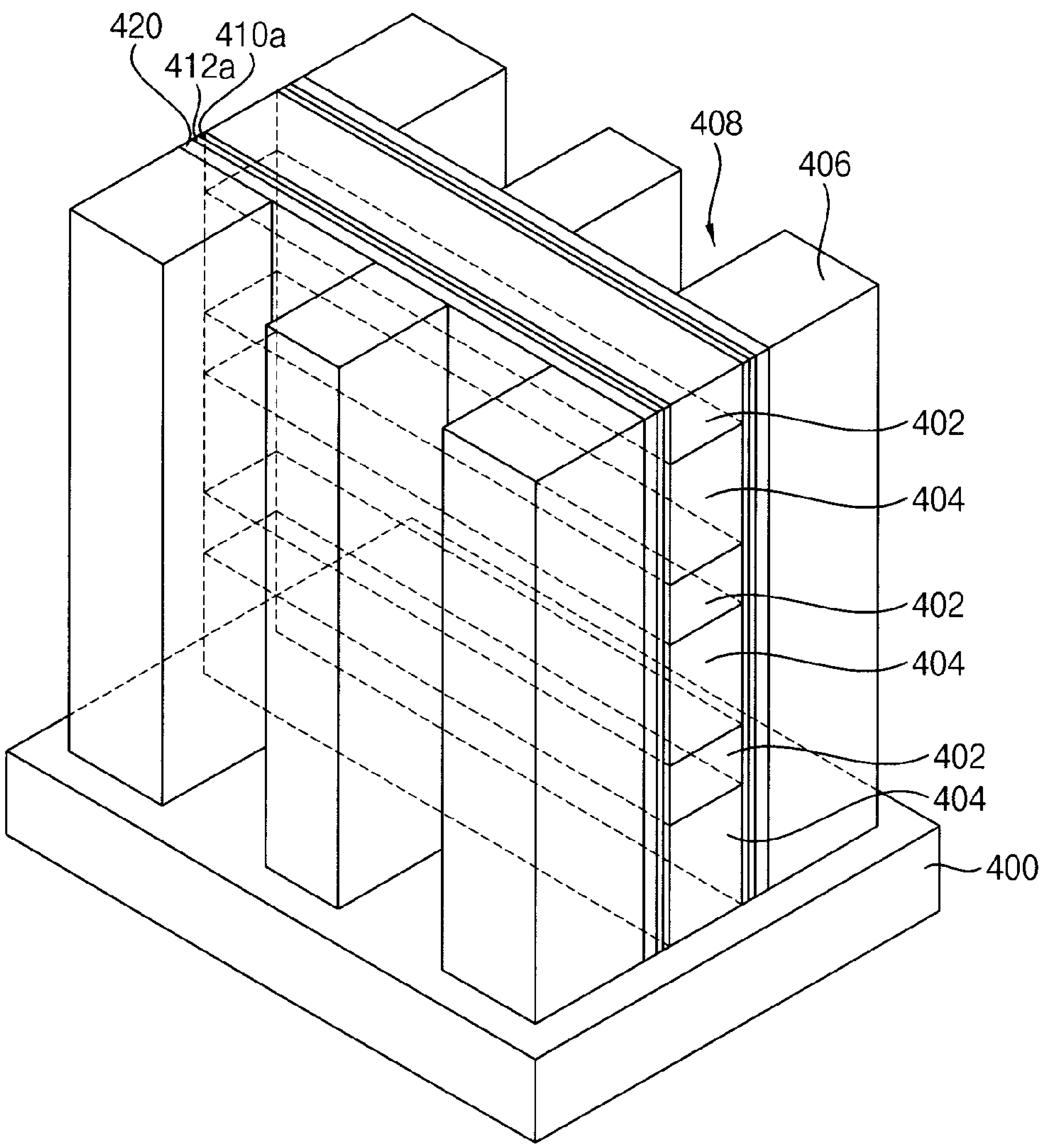


FIG. 16A

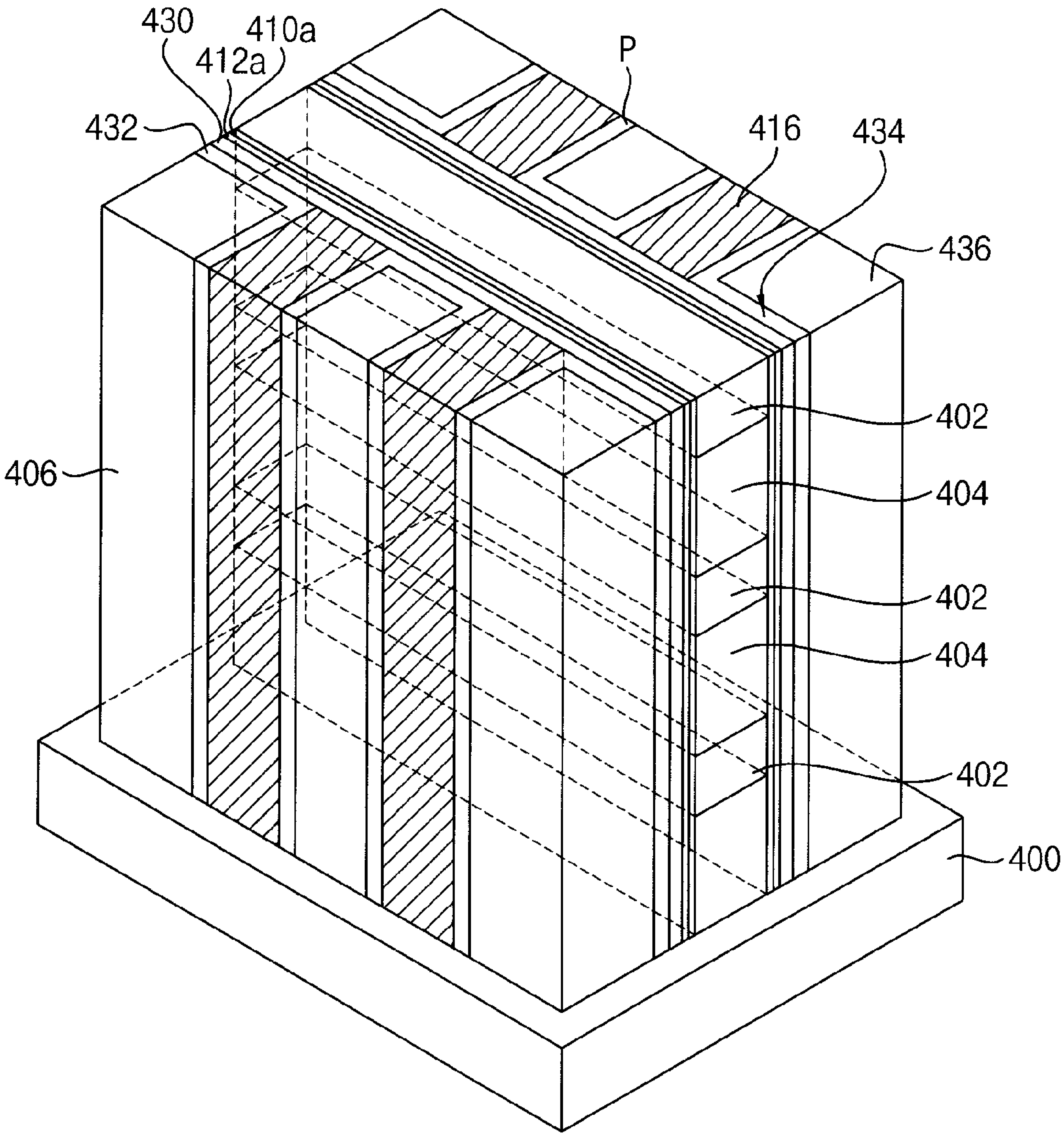


FIG. 16B

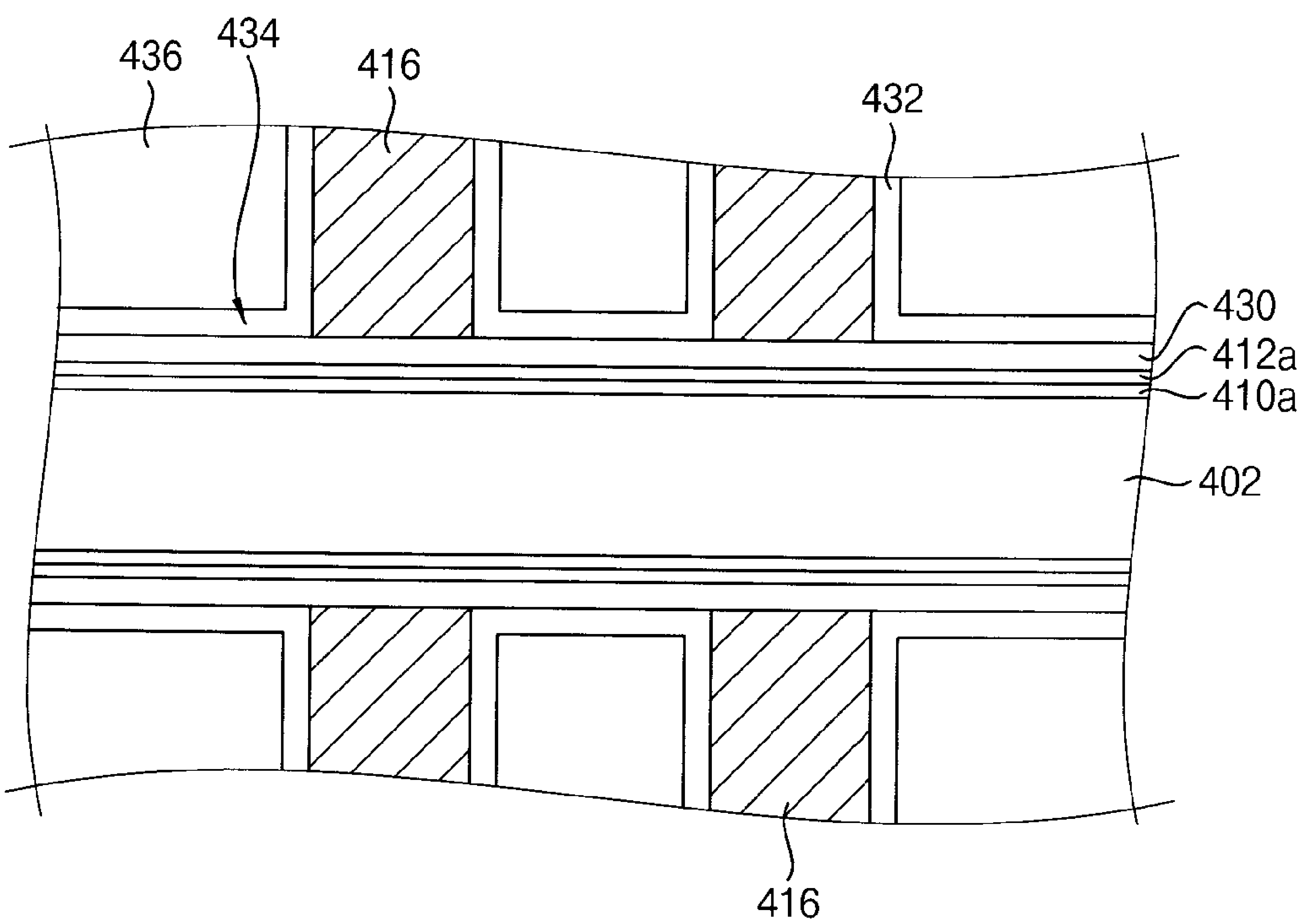


FIG. 17A

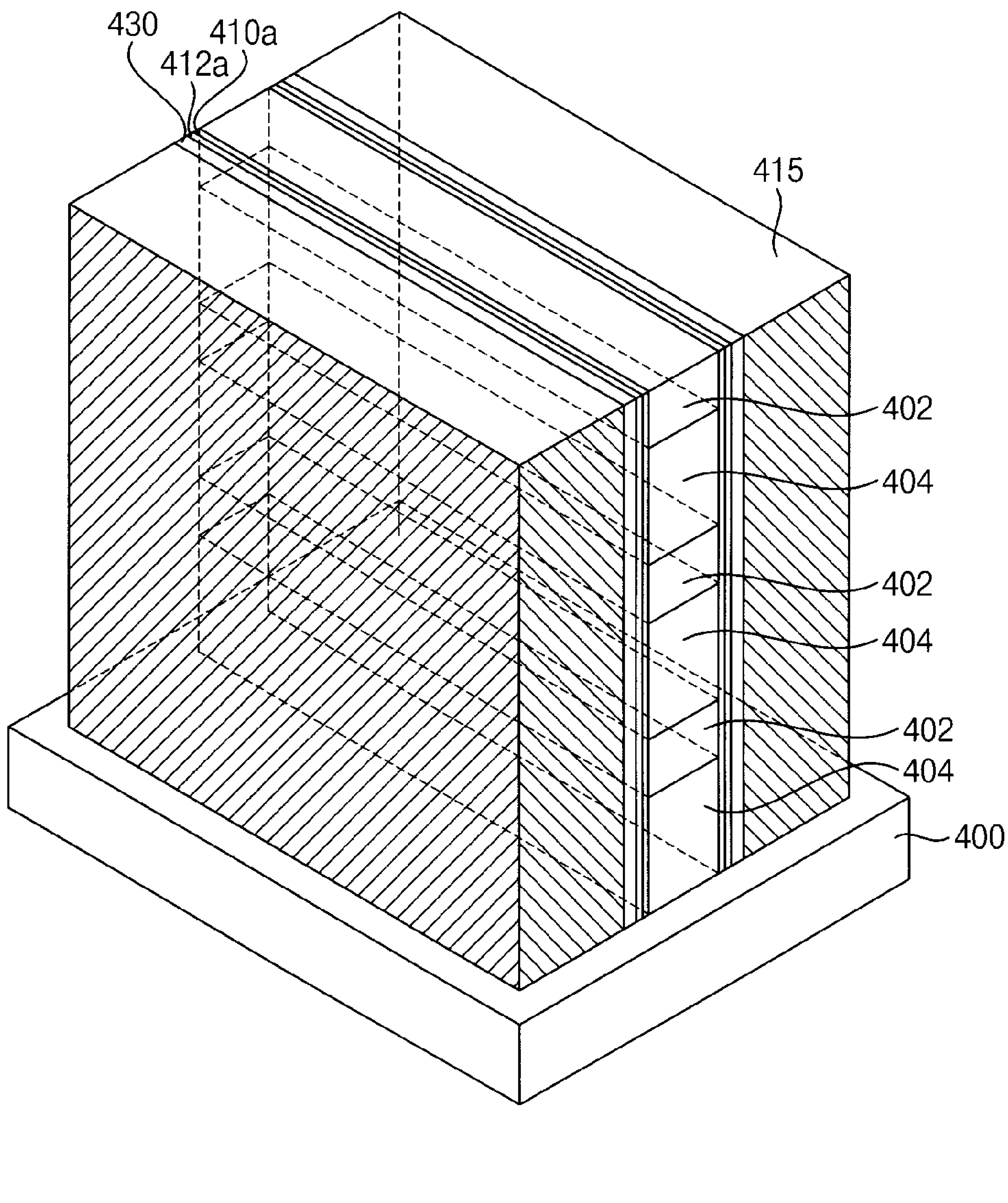


FIG. 17B

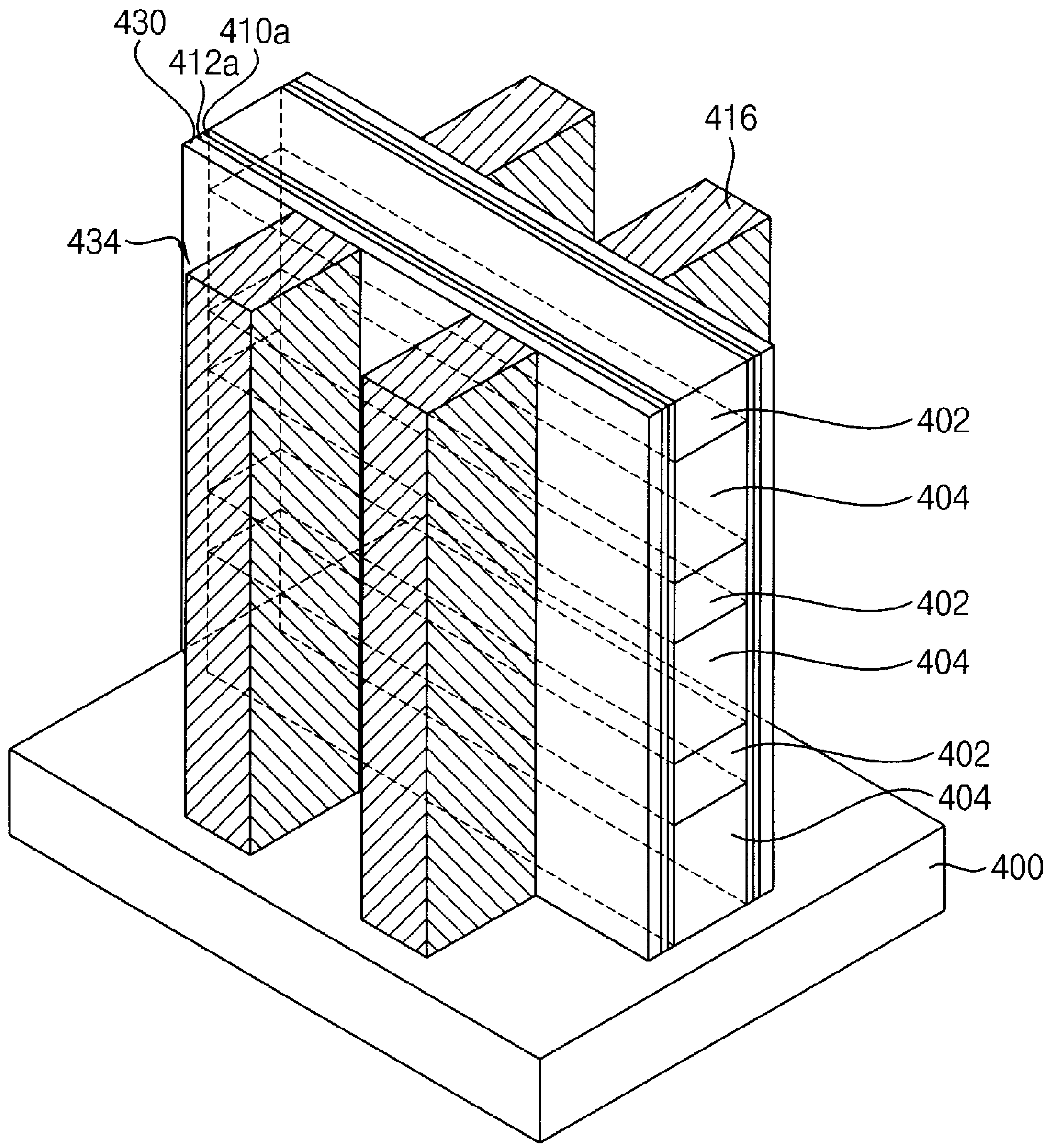


FIG. 17C

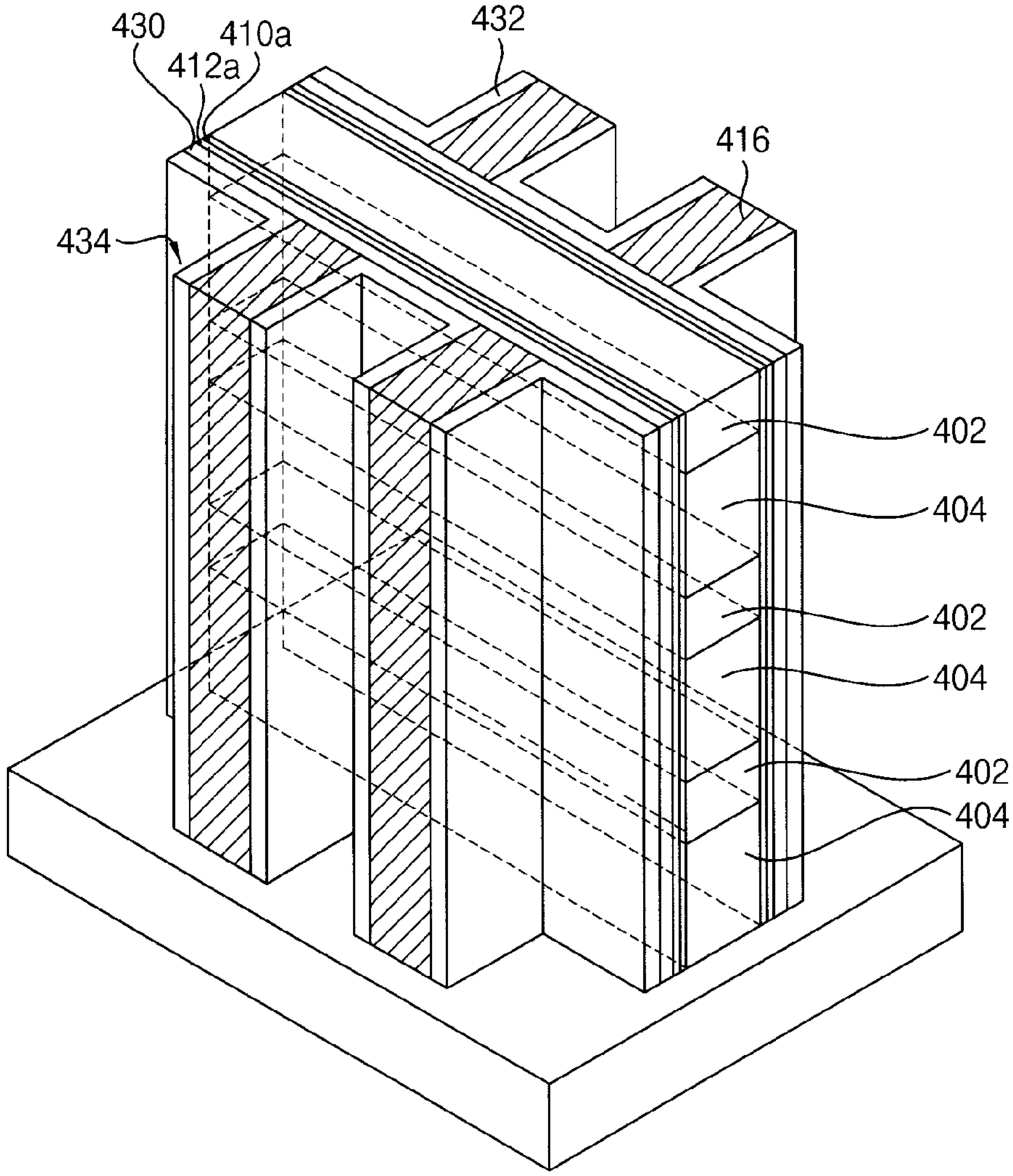


FIG. 18A

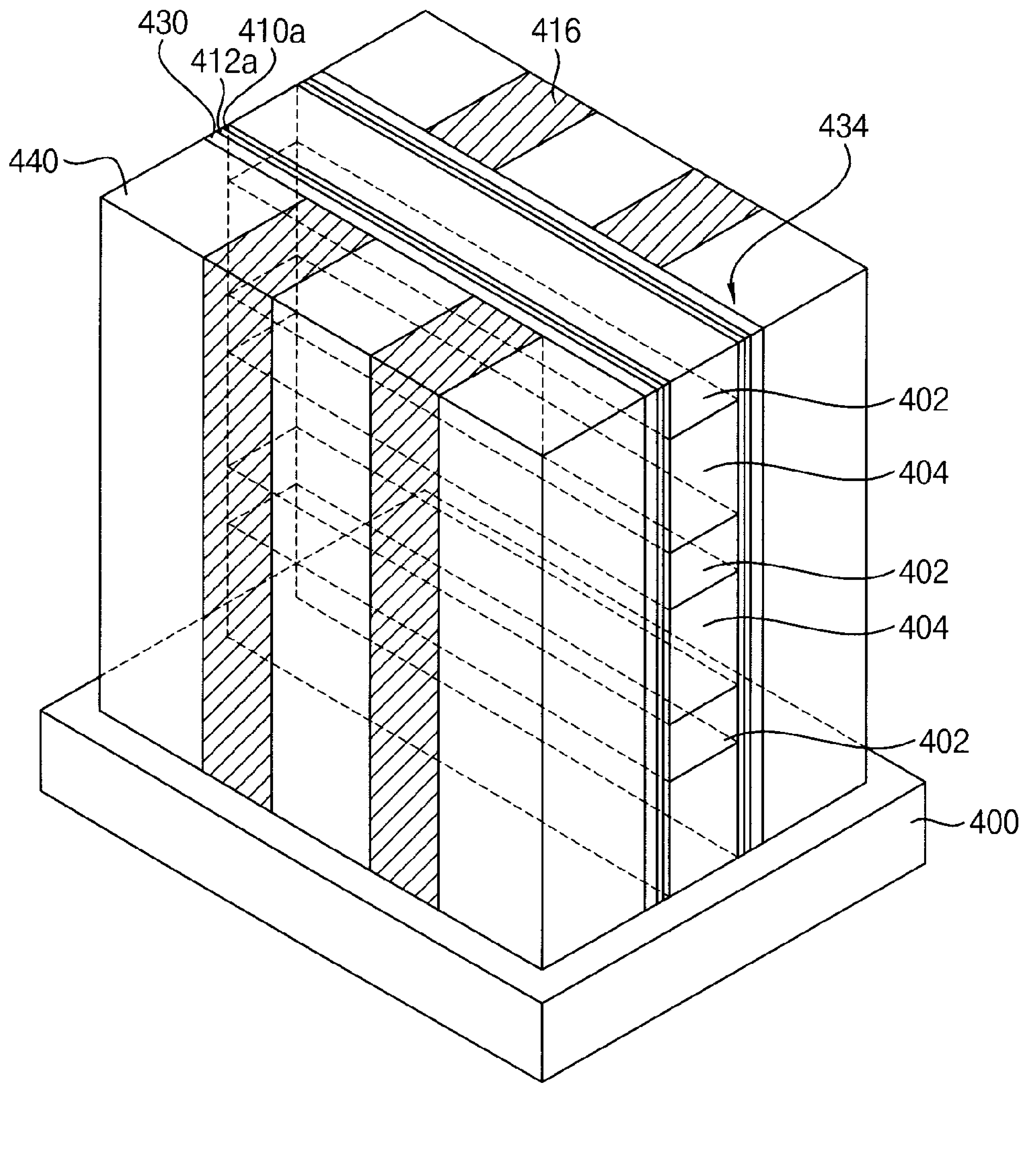


FIG. 18B

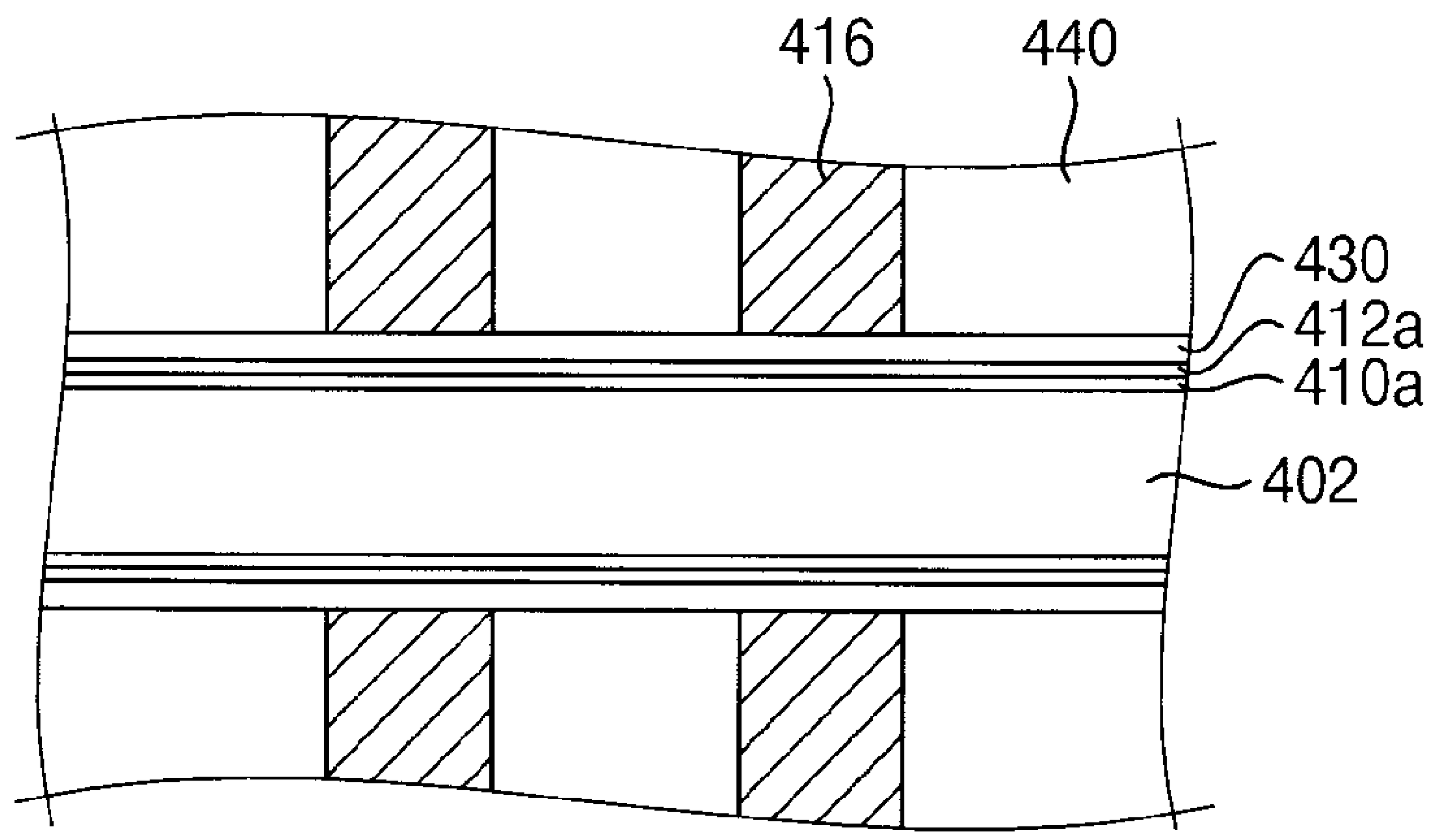
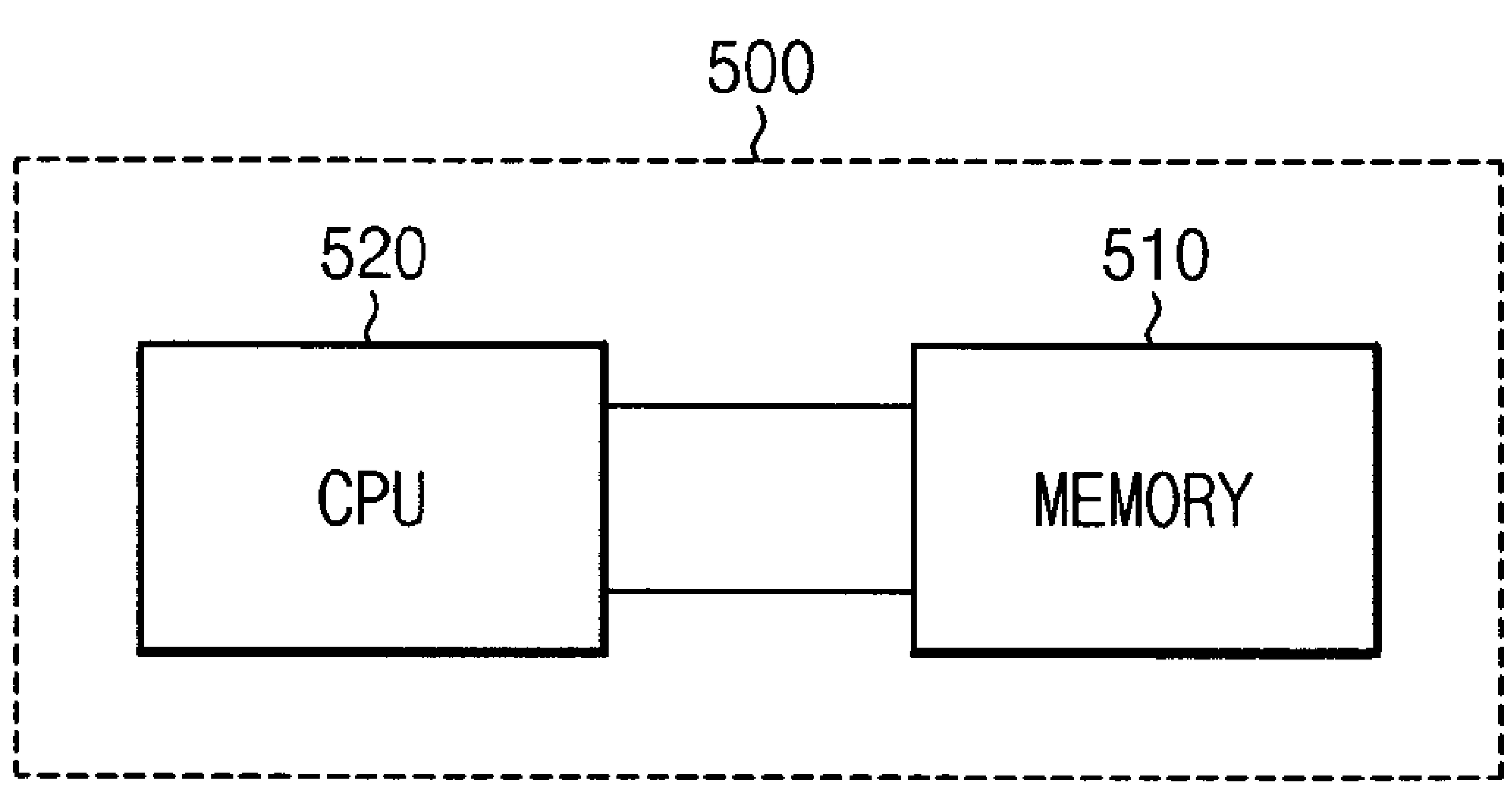


FIG. 19



GATE STRUCTURE IN NON-VOLATILE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. application Ser. No. 13/759,195 filed on Feb. 5, 2013 and claims priority under 35 USC §119 to Korean Patent Application No. 10-2012-0039915 filed on Apr. 17, 2012 in the Korean Intellectual Property Office (KIPO), the entire disclosure of which is incorporated herein by reference.

BACKGROUND

1. Field

Example embodiments relate to a gate structure provided in a non-volatile memory device. More particularly, example embodiments relate to a gate structure provided in a charge-trap NAND flash memory device.

2. Description of the Related Art

In a charge-trap NAND flash memory device, data is recorded by storing charges in a charge trap layer pattern serving as an insulator or erasing charges from the charge trap layer pattern. Since the charge-trap NAND flash memory device can be easily scaled down while representing superior endurance capability and characteristic uniformity, the charge-trap NAND flash memory device has been studied and researched for use as a next generation memory.

SUMMARY

Example embodiments provide a gate structure provided in a non-volatile memory device capable of preventing an erase saturation caused by back tunneling.

Example embodiments provide a method of forming the gate structure.

According to example embodiments, there is provided a gate structure. The gate structure includes a tunnel oxide layer pattern and a charge trap layer pattern sequentially stacked on a substrate. A blocking dielectric layer pattern is formed on the charge trap layer pattern having an uppermost layer including a material having a first dielectric constant that is greater than that of a material included in the tunnel oxide layer pattern. First and second conductive layer patterns are sequentially stacked on the blocking dielectric layer pattern. A first spacer covers at least a sidewall of the second conductive layer pattern, and a second spacer covers sidewalls of the first spacer and the first conductive layer pattern and includes a material having a second dielectric constant, the second dielectric constant equal to or greater than the first dielectric constant.

In the example embodiments, a first material including the first conductive layer pattern may be different from a second material constituting the second conductive layer pattern.

In the example embodiments, the first conductive layer pattern may have a first work function and the second conductive layer pattern may have a second work function that is less than the first work function.

In the example embodiments, the sidewall of the first conductive layer pattern may include a lower portion and an upper portion, the lower portion may have a first width, and an upper portion may have a second width narrower than the first width.

In the example embodiments, a bottom surface of the first spacer may be spaced apart from and above a top surface of the blocking dielectric layer pattern by a thin film.

In the example embodiments, a bottom surface of the second spacer may be closer to the substrate than a bottom surface of the first spacer.

In the example embodiments, the uppermost layer of the blocking dielectric layer pattern may include any one of materials selected from the group consisting of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and zirconium oxide (ZrO_2).

In the example embodiments, the first spacer may cover the sidewall of the second conductive layer pattern and an upper portion of the sidewall of the first conductive layer pattern.

In the example embodiments, the gate structure may further include a buffer conductive layer pattern between the first and second conductive layer patterns.

In the example embodiments, the buffer conductive layer pattern may include a polysilicon material.

In the example embodiments, the first spacer may cover the sidewall of the second conductive layer pattern and a portion of a sidewall of the buffer conductive layer pattern.

In the example embodiments, the second spacer has an upper portion and a lower portion, the lower portion being a portion of the second spacer that makes contact with the first conductive layer pattern, the lower portion having a width wider than a width of the upper portion.

According to example embodiments, there is provided a gate structure. The gate structure includes a tunnel oxide layer pattern and a charge trap layer pattern sequentially stacked on a substrate. A blocking dielectric layer pattern is formed on the charge trap layer pattern and includes at least one dielectric layer. A barrier metallic layer pattern is stacked on the blocking dielectric layer pattern. A metallic layer pattern is formed on the barrier metallic layer pattern. A first spacer covers a sidewall of the metallic layer pattern and an upper sidewall of the barrier metallic layer pattern. A second spacer covers a sidewall of the first spacer and a lower sidewall of the barrier metallic layer pattern and including a material having a first dielectric constant equal to or greater than a second dielectric constant of an uppermost dielectric layer of the blocking dielectric layer pattern.

In the example embodiments, a bottom surface of the second spacer may directly contact a top surface of the blocking dielectric layer pattern.

In the example embodiments, the first spacer may include an insulating material configured to prevent the sidewall of the metallic layer pattern from being oxidized.

According to example embodiments, there is provided a gate structure.

In one example embodiment, the gate structure includes a substrate, a blocking dielectric layer, a first conductive layer pattern, a second conductive layer pattern, a first spacer, and a second spacer. The substrate having sequentially formed thereon a tunnel oxide layer pattern and a charge trap layer pattern, the charge trap layer pattern configured to trap charges therein and the tunnel oxide layer pattern including a material having a first dielectric constant. The blocking dielectric layer formed on the charge trap layer pattern, the blocking dielectric layer having a top surface that includes an inner portion and an outer portion, the inner portion of the top surface including a material having a second dielectric constant, the second dielectric constant being greater than the first dielectric constant. The first conductive layer pattern formed on the inner portion of the blocking dielectric layer, the first conductive layer pattern having sidewalls. The second conductive layer pattern formed on the first conductive layer pattern, the second conductive layer pattern including a metallic material having a resistance lower than that of a material included in the first conductive layer pattern. The first spacer including a material having a third dielectric constant, the first spacer enclosing the second conductive layer to prevent oxidation thereof. The second spacer formed on the outer portion of the blocking dielectric layer such that the spacer covers the sidewalls of the first conductive layer pattern, the second spacer having a third dielectric constant, the third dielectric constant being greater than or equal to the first dielectric constant and greater than the second dielectric constant.

In one example embodiment, the first conductive layer pattern has a top surface that includes an inner conductive portion and an outer conductive portion, the inner conductive portion being in contact with the second conductive layer pattern and the outer conductive portion being in contact with a bottom surface of the first spacer.

In one example embodiment, a bottom surface of the second spacer is closer to the substrate than the bottom surface of the first spacer.

In one example embodiment, the bottom surface of the second spacer is wider than a top surface of the second spacer.

In one example embodiment, the gate structure further includes a buffer conductive layer pattern formed between the first conductive layer pattern and the second conductive layer pattern, the buffer conductive layer having a top surface that includes an inner buffer portion and an outer buffer portion. The inner buffer portion is in contact with the second conductive layer pattern and the outer conductive portion is in contact with a bottom surface of the first spacer, and the buffer conductive layer pattern has a thickness that is greater than a thickness of the first conductive layer pattern.

According to example embodiments, there is provided a method of forming a gate structure. A tunnel oxide layer and a charge trap layer are sequentially formed on a substrate. A blocking dielectric layer including the uppermost layer including a high dielectric material is formed on the charge trap layer. First and second conductive layer are formed on the blocking dielectric layer. A second conductive layer pattern is formed by patterning the second conductive layer. A first spacer is formed on the sidewall of the second conductive layer pattern. A first conductive layer pattern is formed by patterning the first conductive layer. A second spacer is formed to cover the sidewall of the first spacer and the sidewall of the first conductive layer pattern. The second spacer has a first dielectric constant equal to or greater than a second of the uppermost layer of the blocking dielectric layer. In addition, a tunnel oxide layer pattern, a charge trap layer pattern, and a blocking dielectric layer pattern are formed by patterning the tunnel oxide layer, the charge trap layer, and the blocking dielectric layer.

In example embodiments, a preliminary first conductive layer pattern may be formed by etching a portion of the first conductive layer during the process of patterning the second conductive layer.

In example embodiments, the first conductive layer may be patterned through an isotropic etching process so that the sidewall of the first conductive layer pattern is formed inward from the sidewall of the first spacer.

In example embodiments, after forming the first conductive layer pattern, a process of isotropic-etching the sidewall of the first conductive layer pattern by a predetermined thickness may be additionally performed.

According to example embodiments, a buffer conductive layer is formed between the first and second conductive layers. The buffer conductive layer pattern is formed by patterning the buffer conductive layer.

In example embodiments, during the process of patterning the second conductive layer, a preliminary buffer conductive layer pattern may be formed by etching a portion of the buffer conductive layer.

In example embodiments, the first spacer may cover the sidewall of the second conductive layer pattern and a portion of the sidewall of the buffer conductive layer pattern.

In example embodiments, the material including the uppermost layer of the blocking dielectric layer pattern may include any one selected from the group consisting of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and zirconium oxide (ZrO_2).

According to example embodiments, the non-volatile memory device employing the gate structure prevents an erase saturation caused by back tunneling. Therefore, a non-volatile memory device having high performance can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGS. **1***a* to **19** represent non-limiting, example embodiments as described herein.

FIG. **1**A is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a first example embodiment;

FIGS. **1**B and **1**C are cross-sectional views illustrating a gate structure provided in a non-volatile memory device according to modified example embodiments;

FIGS. **2**A to **2**E are cross-sectional views illustrating a method of forming the gate structure of FIG. **1**A;

FIG. **3** is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a second example embodiment;

FIGS. **4**A and **4**B are cross-sectional views illustrating a method of forming the gate structure of FIG. **3**;

FIG. **5** is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a third example embodiment;

FIGS. **6**A to **6**E are cross-sectional views illustrating a method of forming the gate structure of FIG. **5**;

FIG. **7** is a cross-sectional view illustrating a non-volatile memory device according to one example embodiment;

FIGS. **8**A and **8**B are cross-sectional views illustrating a method of fabricating the non-volatile memory device of FIG. **7**;

FIG. **9**A is a cross-sectional view illustrating a vertical type non-volatile memory device according to another example embodiment;

FIG. **9**B is an enlarged view illustrating a part A of FIG. **9**A;

FIG. **10** is a cross-sectional view illustrating a vertical type non-volatile memory device according to another example embodiment;

FIG. **11**A is a cross-sectional view illustrating a vertical type non-volatile memory device according to another example embodiment;

FIG. **11**B is an enlarged view illustrating a part A of FIG. **11**A;

FIG. **12**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment;

FIG. **12**B is a plan view of FIG. **12**A;

FIGS. **13**A and **13**B are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **12**A;

FIG. **14**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to one example embodiment;

FIG. **14**B is a plan view of FIG. **14**A;

FIGS. **15**A and **15**B are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **14**A;

FIG. **16**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment;

FIG. **16**B is a plan view of FIG. **16**A;

FIGS. **17**A to **17**C are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **16**A;

FIG. **18**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment;

FIG. **18**B is a plan view of FIG. **18**A; and

FIG. **19** is a block diagram illustrating a memory system provided with the non-volatile memory device according to example embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Various example embodiments will be described more fully hereinafter with reference to the accompanying drawings, in which some example embodiments are shown. The present inventive concepts may, however, be embodied in many different forms and should not be construed as limited to the example embodiments set forth herein. Rather, these example embodiments are provided so that this description will be thorough and complete, and will fully convey the scope of the present inventive concepts to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity.

It will be understood that when an element or layer is referred to as being "on," "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Like numerals refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present inventive concepts.

Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the example term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting of the present inventive concepts. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

Example embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of idealized example embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, example embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the present inventive concepts.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which these inventive concepts belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

Hereinafter, example embodiments will be described in detail with reference to the accompanying drawings.

Embodiment 1

FIG. **1**A is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a first example embodiment, and FIGS. **1**B and **1**C are cross-sectional views illustrating a gate structure provided in a non-volatile memory device according to modified example embodiments.

Referring to FIG. **1**A, a gate structure includes a tunnel oxide layer pattern **102***a*, a charge trap layer pattern **104***a*, a blocking dielectric layer pattern **108**, first and second conductive layer patterns **110***b* and **112***a*, respectively, and a hard mask pattern **114***a* which are sequentially stacked on a semiconductor substrate **100**. In addition, the gate structure includes first and second spacers **116** and **118**, respectively, formed on a sidewall of the stacked structure.

The semiconductor substrate **100** may include a silicon substrate, a germanium substrate, a silicon-germanium substrate, a silicon-on-insulator (SOI) substrate, or a germanium-on-insulator (GOI) substrate. Although not illustrated in drawings, the semiconductor substrate **100** may further include a well having P-type impurities or N-type impurities.

The tunnel oxide layer pattern **102***a* may include silicon oxide.

The charge trap layer pattern **104***a* may include a material to trap charges. For example, according to one example embodiment, the charge trap layer pattern **104***a* may include silicon nitride.

The blocking dielectric layer pattern **108** may include a high dielectric layer having a high dielectric constant. The high dielectric layer may include a material having a dielectric constant greater than that of silicon oxide. Since the dielectric constant of silicon oxide formed through a thermal oxidation process is about 3.9, the high dielectric layer may include a material having the dielectric constant of at least 3.9. Examples of materials used for the high dielectric layer may include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zirconium oxide (ZrO_2), etc. The above materials may be used alone or in a combination thereof.

The blocking dielectric layer pattern **108** may include only a high dielectric layer. Alternately, the blocking dielectric layer pattern **108** may have a multi-layer structure including various oxides, nitrides, or oxynitrides in addition to the high dielectric layer. In this case, the uppermost part of the blocking dielectric layer pattern **108** may be provided as the high dielectric layer.

In some example embodiments, as illustrated in FIG. **1**A, the blocking dielectric layer pattern **108** may have a structure in which a first high dielectric layer **108***a*, a silicon oxide layer **108***b*, and a second high dielectric layer **108***c* are stacked on each other.

In some modified example embodiments, as illustrated in FIG. **1**B, the blocking dielectric layer pattern **108** may have a structure in which a first silicon oxide layer **109***a*, a first high dielectric layer **109***b*, a second silicon oxide layer **109***c*, and a second high dielectric layer **109***d* are stacked on each other.

In other modified example embodiments, as illustrated in FIG. **1**C, the blocking dielectric layer pattern **108** may include only the first high dielectric layer.

The first and second conductive layer patterns **110***b* and **112***a* formed on the blocking dielectric layer pattern **108** may serve as a control gate electrode.

The first and second conductive layer patterns **110***b* and **112***a* may include a metallic material. In some example embodiments, the first conductive layer pattern **110***b* may include a barrier metallic layer, and the second conductive layer pattern **112***a* may include metal. In other words, the second conductive layer pattern **112***a* has resistance lower than that of the first conductive layer pattern **110***b*, and actually serves as a wiring line. Accordingly, as illustrated in FIG. **1***a*, the second conductive layer pattern **112***a* is thicker than the first conductive layer pattern **110***b*. Examples of materials used for the first conductive layer pattern **110***b* may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), or tantalum nitride (Ta_2N). The above materials may be used alone or in a combination thereof. For example, the second conductive layer pattern **112***a* may include tungsten (W).

Meanwhile, since the high dielectric layer is formed at the uppermost part of the blocking dielectric layer pattern **108**, when polysilicon makes direct contact with an upper portion of the high dielectric layer, a Fermi level pinning may undesirably occur. Therefore, the use of polysilicon for the first conductive layer pattern **110***b* is undesirable because of direct contact with the blocking dielectric layer pattern **108**.

In addition, the threshold voltage characteristic of a cell transistor may be varied according to a first work function of the first conductive layer pattern **110***b* that direct contacts with the blocking dielectric layer pattern **108**. Preferably, the first work function may be greater than 4.0 eV. In addition, the first work function may be greater than a second work function of the second conductive layer pattern **112***a*.

A sidewall of the first conductive layer pattern **110***b* does not have a continuous flat surface, but laterally protrudes at the lower portion thereof. Therefore, the lower portion of the first conductive layer pattern **110***b* has a first width, and the upper portion of the first conductive layer pattern **110***b* has a second width narrower than the first width. The protrusion part of the first conductive layer pattern **110***b* may have a flat top surface.

The second conductive layer pattern **112***a* has a flat surface continuously extending from an upper sidewall of the first conductive layer pattern **110***b*. For example, the second conductive layer pattern **112***a* may have the second width such that the width of the second conductive layer pattern **112***a* is equal to the width of the upper portion of the first conductive layer pattern **110***b*.

The hard mask pattern **114***a* may include silicon nitride.

The first spacer **116** is formed on a top surface of the protrusion part of the first conductive layer pattern **110***b* while being formed on both of a sidewall of the second conductive layer pattern **112***a* and a sidewall of the upper portion of the first conductive layer pattern **110***b*. The first spacer **116** may have a width equal to that of the protrusion part of the first conductive layer pattern **110***b*. Therefore, the first spacer **116** is spaced apart from a top surface of the blocking dielectric layer pattern **108** while being provided higher relative to the substrate **100** than the top surface of the blocking dielectric layer pattern **108**. Therefore, the first spacer **116** does not make direct contact with the blocking dielectric layer pattern **108**. The first spacer **116** prevents the sidewalls of the first and second conductive layer patterns **110***b* and **112***a*, which includes a metallic material, from being oxidized. Accordingly, the first spacer **116** may include silicon nitride.

The second spacer **118** makes contact with both of a sidewall of the first spacer **116** and the sidewall of the protrusion part of the first conductive layer pattern **110***b*. In addition, a bottom surface of the second spacer **118** makes direct contact with a thin film formed at the uppermost part of the blocking dielectric layer pattern **108**. The bottom surface of the second spacer **118** is positioned lower than a bottom surface of the first spacer **116**. The second spacer **118** has a first dielectric constant equal to or greater than a second dielectric constant of the thin film positioned at the uppermost part of the blocking dielectric layer pattern **108**. In addition, the second spacer **118** includes a material different from that of the first spacer **116**, and has the first dielectric constant greater than a that of the first spacer **116**. In other words, the second spacer **118** has the first dielectric constant equal to or greater than that of the second high dielectric layer. Example of materials used for the second spacer **118** may include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide

(LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zirconium oxide (ZrO_2), etc. The above materials can be used alone or in a combination thereof. The second spacer **118** may selectively include materials having the first dielectric constant equal to or greater than that of a material constituting the second high dielectric layer. As described above, a bottom surface and a lateral side of the first conductive layer pattern **110***b* are surrounded by a dielectric layer having a high dielectric constant.

In the non-volatile memory device, data is recorded by storing charges into the charge trap layer pattern **104***a* of the gate structure or erasing charges from the charge trap layer pattern **104***a*.

In the erasing operation, electrons trapped in the charge trap layer pattern **104***a* are drawn out through the tunnel oxide layer pattern **102***a* and erased by applying erase voltage to the second conductive layer pattern **112***a* serving as a control gate. In the erasing operation, when high negative voltage is applied to the second conductive layer pattern **112***a*, charges may be drawn out from the charge trap layer pattern **104***a* through the tunnel oxide layer pattern **102***a*, but electrons existing in the second conductive layer pattern **112***a* may be back-tunneled through the blocking dielectric layer and introduced into the charge trap layer pattern **104***a*. As described above, in example embodiments, in the erasing operation charges are not introduced into the charge trap layer pattern **104***a* through the back tunneling, which is called an erase saturation.

In order to prevent charges from being introduced into the charge trap layer pattern **104***a* through the back tunneling, the blocking dielectric layer pattern **108** that directly contacts the first conductive layer pattern **110***b* preferably includes a material having the high dielectric constant, so that a high tunnel barrier is formed. In addition, preferably, an electric field is uniformly generated between the first conductive layer pattern **110***b* and the blocking dielectric layer pattern **108**, so that the electric field is prevented from being concentrated on a particular region.

In the present example embodiment, the bottom surface and the lateral side of the first conductive layer pattern **110***b* are surrounded by a dielectric layer having a high dielectric constant. In particular, the second spacer **118** including a material having a high dielectric constant is formed on the sidewall of the first conductive layer pattern **110***b*, thereby uniformly generating an electric field at an edge region of the first conductive layer pattern **110***b*, so that the electric field is not concentrated on the edge region of the first conductive layer pattern **110***b*. Accordingly, the back tunneling caused by the concentration of the electric field on the edge region of the first conductive layer pattern **110***b* may be reduced, so that the non-volatile memory device represent an improved erasing operation characteristic.

FIGS. **2**A to **2**E are cross-sectional views illustrating a method of forming the gate structure of FIG. **1***a*.

Referring to FIG. **2**A, a tunnel oxide layer **102**, a charge trap layer **104**, and a blocking dielectric layer **106** are sequentially formed on a semiconductor substrate **100**.

The tunnel oxide layer **102** may include silicon oxide, and may be formed through a thermal oxidation process. According to another example embodiment, the tunnel oxide layer **102** may be formed by performing a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, or a sputtering process.

The charge trap layer **104** may include silicon nitride and may be formed by performing a CVD process, an ALD process, or a sputtering process.

The blocking dielectric layer **106** may have a stacked structure including a high dielectric layer at the uppermost part thereof. For example, as illustrated in FIG. **2**A, the blocking dielectric layer **106** may be formed by sequentially depositing a first high dielectric layer **106***a*, a silicon oxide layer **106***b*, and a second high dielectric layer **106***c*.

The first high dielectric layer **106***a* may be formed by performing a CVD process, an ALD process, or a sputtering process. The first high dielectric layer **106***a* may include a high dielectric material. Example of the high dielectric materials used for the first high dielectric layer **106***a* may include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zirconium oxide (ZrO_2), etc. The high dielectric materials can be used alone or in a combination thereof.

The silicon oxide layer **106***b* may be formed by performing a CVD process, an ALD process, or a sputtering process.

The second high dielectric layer **106***c* may be formed by performing a CVD process, an ALD process, or a sputtering process. The second high dielectric layer **106***c* may include a high dielectric material. Example of the high dielectric materials used for the second high dielectric layer **106***c* may include such as silicon nitride using aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zirconium oxide (ZrO_2), etc. The high dielectric materials can be used alone or in a combination thereof. In some example embodiments, a material used for the second high dielectric layer **106***c* may be same or different material then used for the first high dielectric layer **106***a*.

Although the present example embodiment is described in that the blocking dielectric layer **106** is formed by depositing the first high dielectric layer **106***a*, the silicon oxide layer **106***b*, and the second high dielectric layer **106***c*, the blocking dielectric layer **106** may have various stacked structures. For example, in some example embodiments, the blocking dielectric layer **106** may be formed by sequentially depositing a first silicon oxide layer, a first high dielectric layer, a second silicon oxide layer, and a second high dielectric layer while in some example embodiments, the blocking dielectric layer **106** may include only a high dielectric layer.

Thereafter, a first conductive layer **110**, a second conductive layer **112**, and a hard mask layer **114** are formed on the blocking dielectric layer **106**.

The first conductive layer **110** may be formed by depositing metallic materials. Examples of the metallic materials used for the first conductive layer **110** may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (Ta_2N), etc. The above metallic materials may be used alone or in a stacked form including at least two materials. The first conductive layer **110** serves as a barrier metallic layer.

The second conductive layer **112** may include tungsten (W). The second conductive layer **112** is thicker than the first conductive layer **110**.

The hard mask layer **114** may be formed by depositing silicon nitride.

Referring to FIG. **2**B, the hard mask pattern **114***a* is formed by patterning the hard mask layer **114** using a photoresist pattern.

The second conductive layer **112** is etched by using the hard mask pattern **114***a* so that a top surface of the first conductive layer **110** is exposed. Subsequently, a portion of the first conductive layer **110** provided under the second conductive layer **112** is etched. The second and first conductive layers **110** and **112** may be etched through an anisotropic etching process. In example embodiments, only the second conductive layer **112** need be etched through the anisotropic etching process. However, when the etching process is actually performed, an over etching process must be performed in order to etch the entire exposed portion of the second conductive layer **112**. In this case, the exposed top surface of the first conductive layer **110** may be partially etched to form a preliminary first conductive layer pattern **110***a*.

After the above etching process has been performed, a second conductive layer pattern **112***a* and the preliminary first conductive layer pattern **110***a* are formed.

Referring to FIG. **2**C, the first spacer **116** is formed from a first spacer layer (not illustrated). The first spacer layer is formed on the surfaces of the second conductive layer pattern **112***a*, the preliminary first conductive layer pattern **110***a*, and the hard mask pattern **114***a*. The first spacer layer is formed to prevent the sidewall of the second conductive layer pattern **112***a* from being oxidized. The first spacer layer may be formed by depositing silicon nitride.

The first spacer **116** is formed by anisotropic-etching the first spacer layer. The first spacer **116** is formed on the sidewall of the second conductive layer pattern **112***a* and the sidewall of the preliminary first conductive layer pattern **110***a*.

Referring to FIG. **2**D, the first conductive layer pattern **110***b* is formed by anisotropic-etching the preliminary first conductive layer pattern **110***a* using both of the first spacer **116** and the hard mask pattern **114***a* as an etching mask. In the above etching process, a portion or the entire portion of the second high dielectric layer **106***c*, which is exposed under the preliminary first conductive layer pattern **110***a*, may be etched.

The lower portion of the first conductive layer pattern **110***b* protrudes in a lateral direction. The first conductive layer pattern **110***b* is formed on the sidewall thereof with the first spacer **116**. The lower portion of the first conductive layer pattern **110***b* has the first width and the upper portion of the first conductive layer pattern **110***b* has the second width narrower than the first width.

Referring to FIG. **2**E, the second spacer **1180** is formed from a second spacer layer (not illustrated). The second spacer layer is formed on the surface of the first spacer **116**, the second high dielectric layer **106***c*, and the hard mask pattern **114***a*. The second spacer layer has a first dielectric constant equal to or greater than a second dielectric constant of the second high dielectric layer **106***c* formed at the uppermost part of the blocking dielectric layer **106**. Example of materials used for the second spacer layer may include aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), zirconium oxide (ZrO_2), etc. The above materials may be used alone or in a combination thereof. The second spacer layer may selectively include a material having the first dielectric constant equal to or greater than the second dielectric constant among the above materials.

Thereafter, the second spacer **118** is formed on both of the sidewall of the first spacer **116** and the sidewall of the protrusion part of the first conductive layer pattern **110***b* by anisotropic-etching the second spacer layer.

Subsequently, as illustrated in FIG. **1**A, the second high dielectric layer **106***c*, the silicon oxide layer **106***b*, the first high dielectric layer **106***a*, the charge trap layer **104**, and the tunnel oxide layer **102**, which are provided under the second spacer **118** and the hard mask pattern **114***a*, are etched by using both of the second spacer **118** and the hard mask pattern **114***a* as an etching mask. Accordingly, the tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, and the blocking dielectric layer pattern **108** are formed.

The gate structure is formed by performing the above processes.

Thereafter, although not illustrated in drawings, an impurity region is formed at the upper portion of the semiconductor substrate **100**, which is adjacent to the gate structure, by an ion implantation process using the gate structure as an ion implantation mask. Through the above processes, a cell transistor of the non-volatile memory device may be manufactured.

Embodiment 2

FIG. **3** is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a second example embodiment.

The gate structure according to the present example embodiment has the same as the gate structure according to the first example embodiment except the present example embodiment does not have the first conductive layer pattern **110***b* and the second spacer **118**. Instead, the present example embodiment includes a first conductive layer pattern **111** and a second spacer **118***a* that have shapes that differ from the first conductive layer pattern **110***b* and the second spacer **118**, respectively.

Referring to FIG. **3**, similarly to the gate structure described in the first example embodiment, the gate structure according to the present example embodiment includes the tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, the blocking dielectric layer pattern **108**, first and second conductive layer patterns **111** and **112***a*, and the hard mask pattern **114***a* which are sequentially stacked on the semiconductor substrate **100**. In addition, the gate structure includes first and second spacers **116** and **118***a* formed on a sidewall of the stacked structure.

The tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, and the blocking dielectric layer pattern **108**, which are formed on the semiconductor substrate **100**, have the same structures as those according to the first example embodiment.

The first and second conductive layer patterns **111** and **112***a* formed on the blocking dielectric layer pattern **108** serve as a control gate electrode. The materials constituting the first and second conductive layer patterns **111** and **112***a* are the same as the materials constituting the first and second conductive layer patterns **110***b* and **112***a* described according to the first example embodiment.

The first spacer **116** is positioned on both of the entire sidewall of the second conductive layer pattern **112***a* and the upper portion of sidewall of the first conductive layer pattern **111**. The materials constituting the first spacer **116** are the same as the materials constituting the first spacer **116** described according to the first example embodiment.

The sidewall of the first conductive layer pattern **111** may discontinuously aligned with respect to the sidewall of the first spacer **116**, and may be formed inward from the sidewall of the first spacer **116**. In other words, the first conductive layer pattern **111** may not be provided under the bottom surface of the first spacer **116**. The first conductive layer pattern **111** may be undercut from the bottom surface of the first spacer **116**.

The second spacer **118***a* covers the surface of the first spacer **116**, and the sidewalls of the first conductive layer pattern **111**. The second spacer **118***a* is filled in a region provided under the bottom surface of the first spacer **116**. Therefore, the second spacer **118***a* formed on the sidewall of the first conductive layer pattern **111** has a width wider than that of the second spacer **118***a* formed on the sidewall of the first spacer **116**. The materials constituting the second spacer **118***a* are the same as the materials constituting the second spacer described according to the first example embodiment.

As described above, the bottom surface and the lateral side of the first conductive layer pattern **111** is surrounded by a dielectric layer having a high dielectric constant. Accordingly, the back tunneling caused by the concentration of the electric field on the edge region of the first conductive layer pattern **111** is reduced, so that the non-volatile memory device represent an improved erasing operation characteristic.

FIGS. **4**A and **4**B are cross-sectional views illustrating a method of forming the gate structure of FIG. **3**.

First, the structure illustrated in FIG. **2**C is formed by performing the processes the same as those described with reference to FIGS. **2**A to **2**C.

Referring to FIGS. **2**C and **4**A, the preliminary first conductive layer pattern **110***a* is isotropic-etched by using both of the first spacer **116** and the hard mask pattern **114***a* as an etching mask. When the above isotropic etching process is performed, the preliminary first conductive layer pattern **110***a* provided under the bottom surface of the first spacer **116** is etched to have a shape undercut from the bottom surface of the first spacer **116**, thereby forming the first conductive layer pattern **111**.

Referring to FIG. **4**B, the second spacer **118***a* is formed from a second spacer layer (not illustrated). The second spacer layer is formed on the surface of the first spacer **116**, and the second high dielectric layer **106***c* and the hard mask pattern **114***a*. The second spacer layer has a first dielectric constant equal to or greater than a second dielectric constant of the second high dielectric layer **106***c* positioned at the uppermost part of the blocking dielectric layer. The second spacer layer is filled in an undercut region provided under the bottom surface of the first spacer **116**.

Thereafter, the second spacer **118***a* is formed on the sidewalls of the first spacer **116** and the first conductive layer pattern **111** by anisotropic-etching the second spacer layer.

As illustrated in drawings, since the sidewall of the first conductive layer pattern **111** is formed inward from the sidewall of the first spacer **116**, the second spacer **118***a* has a wider width on the sidewall of the first conductive layer pattern **111**.

Subsequently, as illustrated in FIG. **3**, the second high dielectric layer **106***c*, the silicon oxide layer **106***b*, the first high dielectric layer **106***a*, the charge trap layer **104**, and the tunnel oxide layer **102**, which are provided under the second spacer **118***a* and the hard mask pattern **114***a*, are etched by using both of the second spacer **118***a* and the hard mask pattern **114***a* as an etching mask. Accordingly, the tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, and the blocking dielectric layer pattern **108** are formed.

The gate structure is formed by performing the above processes.

Hereinafter, another method of forming the gate structure illustrated in FIG. **3** will be described.

First, the structure illustrated in FIG. **2***d* is formed by performing the processes the same as those described with reference to FIGS. **2***a* to **2***d*.

As illustrated in **4***a*, the first conductive layer pattern **110***b* is isotropic-etched by using both of the first spacer **116** and the hard mask pattern **114***a* as an etching mask. When the above isotropic etching process is performed, the first conductive layer pattern **110***b* provided under the bottom surface of the first spacer **116** may be etched, thereby forming the first conductive layer pattern **111** finally having a shape undercut from the bottom surface of the first spacer **116**.

In other words, the first conductive layer pattern **110***b* the same as that illustrated in FIG. **2***d* is formed by anisotropic-etching the preliminary first conductive layer pattern **110***a* illustrated in FIG. **2***c*. Thereafter, a portion of the sidewall of the first conductive layer pattern **110***b* is isotropic-etched, thereby forming the first conductive layer pattern **111** of FIG. **4***a* which is the shape undercut from.

Thereafter, the gate structure of FIG. **3** can be formed by performing the processes the same as the processes described with reference to FIG. **4***b*.

Embodiment 3

FIG. **5** is a cross-sectional view illustrating a gate structure provided in a non-volatile memory device according to a third example embodiment.

Referring to FIG. **5**, the gate structure includes the tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, the blocking dielectric layer pattern **108**, a first conductive layer pattern **110***c*, a buffer conductive layer pattern **130***b*, a second conductive layer pattern **132***a*, and the hard mask pattern **114***a* which are sequentially stacked on the semiconductor substrate **100**. In addition, the gate structure includes first and second spacers **116***a* and **118***b*, respectively, formed on a sidewall of the stacked structure.

The tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, and the blocking dielectric layer pattern **108**, which are formed on the semiconductor substrate **100**, have the same structures as those according to the first example embodiment.

The first conductive layer pattern **110***c*, the buffer conductive layer pattern **130***b*, and the second conductive layer pattern **132***a*, which are formed on the blocking dielectric layer pattern **108**, serve as a control gate.

The first conductive layer pattern **110***c* may include a metallic material having a work function of at least 4.0 eV. Example of materials used for the first conductive layer pattern **110***c* may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (Ta_2N), etc. The above materials may be used alone or in a combination thereof.

Since the high dielectric layer is formed at the uppermost part of the blocking dielectric layer pattern **108**, when polysilicon makes direct contact with an upper portion of the high dielectric layer, a Fermi level pinning may undesirably occur. Therefore, the use of polysilicon for the first conductive layer pattern **110***c* making direct contact with the blocking dielectric layer pattern **108** is undesirable.

The buffer conductive layer pattern **130***b* may include polysilicon. The buffer conductive layer pattern **130***b* is provided to easily perform a process of etching a gate electrode. Therefore, the buffer conductive layer pattern **130***b* may be thicker than the first conductive layer pattern **110***c*. The buffer conductive layer pattern **130***b* may be doped with impurities so that the buffer conductive layer pattern **130***b* is conductive.

A sidewall of the buffer conductive layer pattern **130***b* does not have a continuous flat surface, but protrudes at the lower portion thereof. Therefore, the lower portion of the buffer conductive layer pattern **130***b* has the first width, and the upper portion of the buffer conductive layer pattern **130***b* has the second width narrower than the first width. The protrusion part of the buffer conductive layer pattern **130***b* may have a flat top surface.

The second conductive layer pattern **132***a* has a flat surface continuously extending from an upper sidewall of the buffer conductive layer pattern **130***b*. For example, the second conductive layer pattern **132***a* may have the second width. The second conductive layer pattern **132***a* may serve as a wiring line. Therefore, the second conductive layer pattern **132***a* may include a metallic material having low resistance. According to one example embodiment, the second conductive layer pattern **132***a* may include tungsten (W).

The first spacer **116***a* is formed on a top surface of the protrusion part of the buffer conductive layer pattern **130***b* while being formed on both of a sidewall of the second conductive layer pattern **132***a* and an upper portion of the sidewall of the buffer conductive layer pattern **130***b*. The first spacer **116***a* may have a width equal to that of the protrusion part of the buffer conductive layer pattern **130***b*. Therefore, the first spacer **116***a* does not make direct contact with the blocking dielectric layer pattern **108**. The first spacer **116***a* prevents the sidewalls of the second conductive layer pattern **132***a* that include a metallic material from being oxidized. Accordingly, the first spacer **116***a* may include silicon nitride (Si_3N_4).

The second spacer **118***b* makes contact with the sidewall of the first spacer **116***a*, the sidewall of the protrusion part of the buffer conductive layer pattern **130***b*, and the sidewall of the first conductive layer pattern **110***c*. The bottom surface of the second spacer **118***b* is positioned lower than the bottom surface of the first spacer **116***a*.

The second spacer **118***b* has a first dielectric constant equal to or greater than a second dielectric constant of a thin film positioned at the uppermost part of the blocking dielectric layer pattern **108**. In other words, the second spacer **118***b* has the first dielectric constant equal to or greater than that of the second high dielectric layer **108***c*. In addition, the material constituting the second spacer **118***b* is the same as the material described according to the first and second embodiments.

As described above, the bottom surface and the lateral side of the first conductive layer pattern **110***c* is surrounded by a dielectric layer having a high dielectric constant. Accordingly, the back tunneling caused by the concentration of the electric field on the edge region of the first conductive layer pattern **110***c* is reduced, so that the non-volatile memory device represent an improved erasing operation characteristic.

FIGS. **6**A to **6**E are cross-sectional views illustrating a method of forming the gate structure of FIG. **5**.

Referring to FIG. **6**A, the tunnel oxide layer **102**, the charge trap layer **104**, and the blocking dielectric layer **106** are sequentially formed on the semiconductor substrate **100**. The processes of forming the above thin films are the same as those described according to the first example embodiment.

The first conductive layer **110** is formed on the blocking dielectric layer **106**. The first conductive layer **110** may be formed by depositing barrier metallic materials. Examples of the barrier metallic materials used for the first conductive layer **110** may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (Ta_2N), etc. The barrier metallic materials may be used alone or a stacked form including at least two materials. A buffer conductive layer **130** is formed on the first conductive layer **110** with a thickness thicker than that of the first conductive layer **110**. The buffer conductive layer **130** is formed by depositing polysilicon. A second buffer layer **132** is formed on the buffer conductive layer **130**. The second buffer layer **132** may be formed by depositing a metallic material having low resistance. The hard mask layer **114** is formed on the second conductive layer **132**.

Referring to FIG. **6**B, the hard mask pattern **114***a* is formed by patterning the hard mask layer **114** using a photoresist pattern.

The second conductive layer **132** is etched by using the hard mask pattern **114***a* so that the top surface of the buffer conductive layer **130** is exposed. Subsequently, a portion of the buffer conductive layer **130** is etched. The second conductive layer **132** and the buffer conductive layer **130** may be etched through an anisotropic etching process. In the above etching process, the process condition must be adjusted to etch a portion of the buffer conductive layer **130** by a desired (or alternatively, a predetermined) thickness. Since the buffer conductive layer **130** may have a thickness that is larger than that of the first conductive layer **110**, an etching stop point can be easily detected in the etching process.

After the etching process has been performed, the second conductive layer pattern **132***a* and a preliminary buffer conductive layer pattern **130***a* are formed.

Referring to FIG. **6**C, the first spacer **116***a* is formed from a first spacer layer (not illustrated). The first spacer layer is formed on the surfaces of the second conductive layer pattern **132***a*, the preliminary buffer conductive layer pattern **130***a*, and the hard mask pattern **114***a*. The first spacer layer may be formed by depositing silicon nitride.

The first spacer **116***a* is formed by anisotropic-etching the first spacer layer. The first spacer **116***a* is formed on the sidewall of the second conductive layer pattern **132***a* and the sidewall of the preliminary buffer conductive layer pattern **130***a*.

Referring to FIG. **6**D, the preliminary buffer conductive layer pattern **130***a* and the first conductive layer **110** are anisotropic-etched by using the first spacer **116***a* and the hard mask pattern **114***a* as an etching mask, thereby forming the buffer conductive layer pattern **130***b* and the first conductive layer pattern **110***c*.

The lower portion of the buffer conductive layer pattern **130***b* and the first conductive layer pattern **110***c* protrude in a lateral direction.

Referring to FIG. **6**E, the second spacer **118***b* is formed from a second spacer layer (not illustrated). The second spacer layer is formed on the surface of the first spacer **116***a*, the second high dielectric layer **118***b*, and the hard mask pattern **114***a*. The second spacer layer may include a material the same as that described according to the first and second embodiments.

Thereafter, the second spacer **118***b* is formed on the sidewalls of the first spacer **116***a*, the first conductive layer pattern **110***c*, and a protrusion part of the buffer conductive layer pattern **130***b* by anisotropic-etching the second spacer layer.

Subsequently, as illustrated in FIG. **5**, the second high dielectric layer **106***c*, the silicon oxide layer **106***b*, the first high dielectric layer **106***a*, the charge trap layer **104**, and the tunnel oxide layer **102**, which are provided under the second spacer **118***b* and the hard mask pattern **114***a*, are etched by using both of the second spacer **118***b* and the hard mask pattern **114***a* as an etching mask. Accordingly, the tunnel oxide layer pattern **102***a*, the charge trap layer pattern **104***a*, and the blocking dielectric layer pattern **108** are formed.

The gate structure may be formed by performing the above processes.

The gate structure according to each example embodiment described above is applicable to the non-volatile memory device.

Embodiment 4

FIG. **7** is a cross-sectional view illustrating a non-volatile memory device according to an example embodiment.

Referring to FIG. **7**, the non-volatile memory device includes gate structures illustrated in FIG. **1**A. The gate structures serve as gates of a cell transistor **202** and select transistors **204***a* and **204***b*. First to third impurity regions **206***a*, **206***b*, and **206***c*, respectively, are formed between the gate structures in the semiconductor substrate **100**. In addition, the non-volatile memory device further includes a common source line (CSL) **212** and a bit line **218**.

The gate structures have the shape of a line extending in a second direction, and are spaced apart from each other in a first direction perpendicular to the second direction.

A first insulating interlayer **210** is formed on the semiconductor substrate **100** to cover the gate structure.

The CSL **212** makes contact with the second impurity region **206***b* while passing through the first insulating interlayer **210**. The CSL **212** may include doped polysilicon, metal, or metallic silicide.

A second insulating interlayer **214** is formed on both of the first insulating interlayer **210** and the CSL **212**. A bit line contact **216** is formed to make contact with the third impurity region **206***c* while passing through the first and second insulating interlayers **210** and **214**. A bit line **218** electrically connected to the bit line contact **216** is formed on the second insulating interlayer **214**. The bit line **218** extends in the first direction.

As described above, the non-volatile memory device including the gate structure of the example embodiments has improved erase saturation characteristics and improved reliability as compared to a conventional charge-trap non-volatile memory device.

Although the present example embodiment employs the gate structure according to the first example embodiment, the non-volatile memory device may employing the gate structures according to the second and third example embodiments may be provided.

FIGS. **8**A and **8**B are cross-sectional views illustrating a method of fabricating the non-volatile memory device of FIG. **7**.

Gate structures are formed on the semiconductor substrate **100** by performing the processes described with reference to FIGS. **2**A to **2**E. The gate structures have the shape of a line extending in the second direction.

Referring to FIG. **8**A, the first to third impurity regions **206***a*, **206***b*, and **206***c* are formed by implanting impurities into the semiconductor substrate **100** formed between the gate structures.

The first insulating interlayer **210** is formed on the semiconductor substrate **100** to cover the gate structures. The first insulating interlayer **210** may be formed by performing a CVD process, an ALD process, or a sputtering process using oxide such as boron phosphorous silicate glass (BPSG), undoped silicate glass (USG), or spin on glass (SOG).

A first opening (not illustrated) is formed to expose the second impurity region **206***b* while passing through the first insulating interlayer **210**, and a conductive layer is formed in the first opening and on the first insulating interlayer **210**. The first opening may have the shape of a line extending in the second direction. The conductive layer may be formed by using doped polysilicon, metal, or metallic silicide. The upper portion of the conductive layer is planarized until the first insulating interlayer **210** is exposed, thereby forming the CSL **212** making contact with the second impurity region **206***b* in the first opening.

Referring to FIG. **8**B, the second insulating interlayer **214** is formed on the first insulating interlayer **210** and the CSL **212**. The second insulating interlayer **214** may be formed by performing a CVD process, an ALD process, or a sputtering process using oxide such as BPSG, USG, or SOG.

Thereafter, as illustrated in FIG. **7**, a second opening (not illustrated) is formed to expose the third impurity region **206***c* while passing through the first and second insulating interlayers **210** and **214**, and a conductive layer is formed in the second opening and on the second insulating interlayer **214**. The conductive layer may be formed by using doped polysilicon, metal, or metallic silicide. The upper portion of the conductive layer is planarized until the second insulating interlayer **214** is exposed, thereby forming the CSL **216** making contact with the third impurity region **206***c* in the second opening.

In addition, the bit line **218** electrically connected to the bit line contact **216** is formed by depositing a conductive layer on the second insulating interlayer **214** and patterning the conductive layer. The bit line **218** may have a linear shape extending in the second direction. The conductive layer may be formed by using doped polysilicon, metal, or metallic silicide.

The non-volatile memory device illustrated in FIG. **7** may be formed by performing the processes described with reference to FIGS. **8**A and **8**B.

Embodiment 5

FIG. **9**A is a cross-sectional view illustrating a vertical type non-volatile memory device according to one example embodiment. FIG. **9***b* is an enlarged view illustrating a part A of FIG. **9**A, shown in a dotted area of FIG. **9**A.

Referring to FIGS. **9**A and **9**B, the vertical type non-volatile memory device may include channel patterns **302** and control gate electrodes **314** serving as word lines, the channel patterns **302** and word lines are formed on a substrate **300**.

The substrate **300** may include a semiconductor substrate such as a silicon substrate, a germanium substrate, or a silicon-germanium substrate.

The channel patterns **302** may vertically extend from a top surface of the substrate **300** with a desired (or alternatively, a predetermined) height. Each channel pattern **302** may have a pillar shape, cylindrical shape or a rectangular parallelepiped shape. At least the surface of the channel pattern **302** may include a semiconductor material. For example, the entire portion of the channel pattern **302** may include a semiconductor material. Alternately, the outer portion of the channel pattern **302** may include a semiconductor material **302***a*, and the inner portion of the channel pattern **302** may include an insulating material **302***b*. The semiconductor material **302***a* may include single crystal silicon or polysilicon.

A tunnel oxide layer **304** is formed on the surface of the sidewall of the channel pattern **302**. In addition, a charge trap layer **306** is formed on the tunnel oxide layer **304**. A first blocking dielectric layer **308** is formed on the charge trap layer **306**. The first blocking dielectric layer **308** may include a plurality of dielectric layers. In some example embodiments, the first blocking dielectric layer **308** may include a silicon oxide layer. In some example embodiments, the first blocking dielectric layer **308** may have a structure in which a silicon oxide layer and a first high dielectric layer are stacked on each other.

Insulating interlayer patterns **310** are formed in a lateral direction of the channel pattern **302** formed thereon with the first blocking dielectric layer **308**. The insulating interlayer patterns **310** are vertically spaced apart from each other. Accordingly, recess parts are formed between the insulating interlayer patterns **310**.

A second blocking dielectric layer **312** is formed on the first blocking dielectric layer **308** and the insulating interlayer pattern **310** in the recess parts. In some example embodiments, the second blocking dielectric layer **312** may vertically extend as illustrated in FIG. **9**A. In other example embodiments, the second blocking dielectric layer **312** may be formed only in the recess parts of the insulating interlayer pattern **310**.

The second blocking dielectric layer **312** may have a dielectric constant greater than those of the dielectric layers constituting the first blocking dielectric layer **308**. In other words, a material constituting the first blocking dielectric layer **308** may be different from a material constituting the second blocking dielectric layer **312**. In some example embodiments, the second blocking dielectric layer **312** may include a material having the highest dielectric constant among materials constituting the dielectric layers of the first blocking dielectric layer **308**.

The second blocking dielectric layer **312** includes a first part **312***a* making contact with a sidewall part of the channel pattern **302** and a second part **312***b* protruding from the sidewall part of the channel pattern **302** on the end portion of the first part **312***a*.

The second blocking dielectric layer **312** may include a material having a dielectric constant of at least 3.9. The second blocking dielectric layer **312** may include metallic oxide.

Each of the control gate electrodes **314** is formed on the second blocking dielectric layer **312** to fill the recess parts. The control gate electrodes **314** serve as the word lines. The word lines **314** may have the shape of a multi-layer structure, and may be vertically stacked. The word lines **314** may include a metallic material.

Each word line **314** may include a barrier metallic layer pattern **314***a* and a metallic layer pattern **314***b*.

The metallic layer pattern **314***b* may include tungsten (W). The barrier metallic layer pattern **314***a* may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), or tantalum nitride (Ta_2N). The above materials may be used alone or in a combination thereof. The barrier metallic layer pattern **314***a* makes direct contact with the second blocking dielectric layer **312**.

As illustrated in FIGS. **9**A and **9**B, the second blocking dielectric layer **312** is disposed between the word line **314** and the first blocking dielectric layer **308**. In addition, the second blocking dielectric layer **312** makes direct contact with upper and lower portions of the word line **314**. The second part **312***b* of the second blocking dielectric layer **312**, which makes contact with the upper and lower portions of the word line **314**, serves as a second spacer having a high dielectric constant according to the first example embodiment.

As described above, the upper and lower portions of the word line **314** are surrounded by a dielectric layer having a high dielectric constant. Accordingly, the back tunneling caused by the concentration of the electric field on the bending portion of the word line **314** is reduced, so that the vertical type non-volatile memory device of the example embodiments have improved erasing operation characteristics.

Embodiment 6

FIG. **10** is a cross-sectional view illustrating a vertical type non-volatile memory device according to another example embodiment.

The vertical type non-volatile memory device of FIG. **10** has the same structure as that of the vertical type non-volatile memory device according to the example embodiment of FIG. **9** except the vertical type non-volatile memory device illustrated in FIG. **10** does not have the first blocking dielectric layer pattern **308** and the second blocking dielectric layer pattern **312** and instead of the vertical type non-volatile memory device illustrated in FIG. **10** has a single blocking dielectric layer **316**.

Referring to FIG. **10**, the tunnel oxide layer **304** is formed on the surface of the channel pattern **302**. In addition, the charge trap layer **306** is formed on the tunnel oxide layer **304**.

The insulating interlayer patterns **310** are formed in a lateral direction of the channel pattern **302** formed thereon with the charge trap layer **306**. The insulating interlayer patterns **310** are vertically spaced apart from each other. Accordingly, recess parts are formed between the insulating interlayer patterns **310**.

The blocking dielectric layer **316** is formed on the charge trap layer **306** and the insulating interlayer pattern **310** in the recess parts. The blocking dielectric layer **316** includes a first part **316***a* making contact with the sidewall part of the channel pattern **302** and a second part **316***b* protruding from the sidewall part of the channel pattern **302** on the end portion of the part **312***a*.

The blocking dielectric layer **316** may include a material having a dielectric constant of at least 3.9. The blocking dielectric layer **316** may include metallic oxide.

Each of the word lines **314** are formed in the recess parts having the blocking dielectric layer **316** therein. Each of the word lines **314** have the same structure as that described with reference to FIGS. **9**A and **9**B.

The blocking dielectric layer **316** may include a plurality of dielectric layers. When the blocking dielectric layer **316** includes a plurality of dielectric layers, a dielectric layer making direct contact with the word line may have a dielectric constant greater than those of other dielectric layers.

As described above, the upper and lower portions of the word line **314** are surrounded by a dielectric layer having a high dielectric constant. In other words, the second part **316***b* of the blocking dielectric layer serves as the second spacer provided with a high dielectric constant according to the first example embodiment. Accordingly, the back tunneling caused by the concentration of the electric field in the edge portions of the word line **314** is reduced, so that the vertical type non-volatile memory devices of the example embodiments have improved erasing operation characteristics.

Embodiment 7

FIG. **11***a* is a cross-sectional view illustrating a vertical type non-volatile memory device according to another example embodiment. FIG. **11**B is an enlarged view illustrating a part A of FIG. **11**A, shown in a dotted area of FIG. **11**A.

Referring to FIGS. **11**A and **11**B, the vertical type non-volatile memory device may include channel patterns **302** and control gate electrodes **314** serving as word lines, the channel patterns **302** and word lines are formed on the substrate **300**.

The substrate **300** may include a semiconductor substrate such as a silicon substrate, a germanium substrate, or a silicon-germanium substrate.

The channel patterns **302** may vertically extend from a top surface of the substrate **300** with a desired (or alternatively, a predetermined) height. Each channel pattern **302** may have a pillar shape, a cylindrical shape or a rectangular parallelepiped shape. At least the surface of the channel pattern **302** may include a semiconductor material. For example, the entire portion of the channel pattern **302** may include a semiconductor material. Alternately, the outer portion of the channel pattern **302** may include a semiconductor material **302***a*, and the inner portion of the channel pattern **302** may include an insulating material **302***b*. The semiconductor material **302***a* may include single crystal silicon or polysilicon.

The insulating interlayer patterns **310** are formed in a lateral direction of the channel pattern **302**. The insulating interlayer patterns **310** are vertically spaced apart from each other. Accordingly, recess parts are formed between the insulating interlayer patterns **310**.

A tunnel oxide layer **304***a* is formed on the surface of the channel pattern **302** and the insulating interlayer pattern **310** in the recess parts. The tunnel oxide layer **304***a* includes a part making contact with the channel pattern **302** and a part making contact with the surface of the insulating interlayer pattern **310**.

A charge trap layer **306***a* and a blocking dielectric layer **318***a* are formed on the surface of the tunnel oxide layer **304***a*. The blocking dielectric layer **318***a* may include a material having a dielectric constant of at least 3.9. The blocking dielectric layer **318***a* may include metallic oxide.

The blocking dielectric layer **318***a* may include a plurality of dielectric layers.

Each of the control gate electrodes are formed on the blocking dielectric layer **318***a* to fill the recess parts. The control gate electrodes serve as the word lines **314**. The word lines **314** may have the shape of a multi-layer structure, and vertically stacked. The word lines **314** may have the same structure as that of the word lines described with reference to FIGS. **9**A and **9**B.

If the blocking dielectric layer **318***a* includes a plurality of dielectric layers, a dielectric layer making direct contact with the word line **314** may have a dielectric constant greater than those of other dielectric layers.

As illustrated in FIGS. **11**A and **11**B, the blocking dielectric layer **318***a* having a high dielectric constant makes direct contact with upper and lower portions of the word line **314**. The blocking dielectric layer **318***a* making contact with the upper and lower portions of the word line **314** serves as the second spacer provided with a high dielectric constant according to the first example embodiment.

Accordingly, the back tunneling caused by the concentration of the electric field on the edge portions of the word line **314** is reduced, so that the vertical type non-volatile memory devices of the example embodiments have improved erasing operation characteristics.

Embodiment 8

FIG. **12**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment, and FIG. **12**B is a plan view of FIG. **12**A.

Referring to FIGS. **12**A and **12**B, the vertical gate type non-volatile memory device may include channel patterns **402** having a multi-layer structure and word lines **416** having the shape of pillars which are formed on the substrate **400** while facing the sidewalls of the channel patterns **402**.

The channel patterns **402** have the shape of a line extending in the first direction. The channel patterns **402** are stacked while interposing a first insulating interlayer pattern **404** there between. In other words, first insulating interlayer patterns **404** and the channel patterns **402** may be repeatedly and alternately stacked on the substrate. The channel patterns **402** include a semiconductor material. For example, the channel patterns **402** may include a single crystal silicon or polysilicon.

Second insulating interlayer patterns **406** having the shape of pillars are formed at the lateral side of the structure in which the first insulating interlayer patterns **404** and the channel patterns **402** are stacked on each other. Openings **408** are defined between the second insulating interlayer patterns **406** to expose both sidewalls of the channel patterns **402**.

A tunnel oxide layer **410**, a charge trap layer **412**, and a blocking dielectric layer **414** are formed on the sidewall of the opening **408** and the channel pattern **402**. The blocking dielectric layer **414** may include a plurality of dielectric layers.

The blocking dielectric layer **414** may include a material having a dielectric constant of at least 3.9. The blocking dielectric layer **414** may include metallic oxide. When the blocking dielectric layer **414** has a multi-layer structure, the blocking dielectric layer **414** making direct contact with the word line **416** has a dielectric constant greater than those of the blocking dielectric layers **414** formed at other layers.

The word lines **416** are formed in the openings **408** while making contact with the blocking dielectric layers **414**. In other words, the word lines **416** have the shape of a pillar.

The word lines **416** may include a metallic material. The word line **416** may include a barrier metallic layer pattern **416***a* and a metallic layer pattern **416***b*.

The metallic layer pattern **416***b* may include tungsten (W). The barrier metallic layer pattern **416***a* may include titanium (Ti), titanium nitride (TiN), tantalum (Ta), or tantalum nitride (Ta_2N). The above materials may be used alone or in a combination thereof. The barrier metallic layer pattern **416***a* may make direct contact with the blocking dielectric layer **414**.

The word line **416** is surrounded by the blocking dielectric layer **414**. A portion P of the blocking dielectric layer **414** protruding in a lateral direction of the channel pattern **402** serves as the second spacer provided with a high dielectric constant according to the first example embodiment. Accordingly, the back tunneling caused by the concentration of the electric field on the edge portions of the edge region of the word line **416** is reduced, so that the non-volatile memory device of the example embodiments have improved erasing operation characteristics.

FIGS. **13**A and **13**B are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **12**A.

Referring to FIG. **13**A, a structure that stacks the channel patterns **402** and the first insulating interlayer patterns **404** may be formed on a substrate **100**. The structure has the shape of a line extending in the first direction.

In some example embodiments, the structure may be formed by sequentially forming channel layers and first insulating interlayers and then patterning the channel layers and the first insulating interlayers. In another example embodiment, the structure may be formed by sequentially forming channel layers including a semiconductor material and sacrificial layers, forming a recess parts by removing the sacrificial layers, and filling first insulating interlayer patterns in the recess parts.

A second insulating interlayer **405** is filled in a gap between structures described above.

Referring to FIG. **13**B, second insulating interlayer patterns **406** are formed in the shape of a pillar while protruding in a lateral direction of the structure by etching a portion of the second insulating interlayer **405**. The opening **408** is formed between the second insulating interlayer patterns **406**. The sidewalls of the channel patterns **402** and the first insulating interlayer patterns are exposed in the openings.

Referring to FIG. **12**A again, the tunnel oxide layer **410**, the charge trap layer **412**, and the blocking dielectric layer **414** are formed on the sidewall of the opening **408** and exposed the channel pattern **402** in the opening **408**. The blocking dielectric layer **414** may include a material having a dielectric constant of at least 3.9. The blocking dielectric layer **414** may include metallic oxide. When the blocking dielectric layer **414** has a multi-layer structure, a blocking dielectric layer making direct contact with the word line has a dielectric constant greater than those of the blocking dielectric layers formed at other layers.

Thereafter, a word line **416** is fully filled in the opening **408** while making contact with the blocking dielectric layer **414**.

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FIG. **14**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment, and FIG. **14**B is a plan view of FIG. **14**A.

Referring to FIGS. **14**A and **14**B, the vertical gate type non-volatile memory device may include the channel patterns **402** having a multi-layer structure and word lines **416** having a shape of pillars which are formed on the substrate **400** while facing the sidewalls of the channel patterns **402**.

The channel patterns **402** have the shape of a line extending in the first direction. The channel patterns **402** are stacked in a multi-layer structure while interposing the first insulating interlayer pattern **404** there between. In other words, first insulating interlayer patterns **404** and the channel patterns **402** may be repeatedly and alternately stacked on the substrate.

A tunnel oxide layer **410***a*, a charge trap layer **412***a*, and a first blocking dielectric layer **420** are provided in such a manner that the tunnel oxide layer **410***a*, the charge trap layer **412***a*, and the first blocking dielectric layer **420** make direct contact with the sidewall of the structure in which the channel pattern **402** and the first insulating interlayer pattern **404** are stacked. The first blocking dielectric layer **420** may include a plurality of dielectric layers.

The second insulating interlayer patterns **406** having the shape of a pillar are formed at the lateral side of the first blocking dielectric layer **420**. Openings **408** are defined between the second insulating interlayer patterns **406** to expose both sidewalls of the channel patterns **402**

The second blocking dielectric layer **422** is formed on the sidewall of the opening **408** and exposed the first blocking dielectric layer in the opening **408**. The second blocking dielectric layer **422** has a dielectric constant greater than those of the dielectric layers constituting the first blocking dielectric layer **420**. The second blocking dielectric layer **422** includes a first part making contact with the sidewall of the channel pattern **402** and a second part protruding from the sidewall of the channel pattern **402** on the end point of the first part.

The word lines **416** extend perpendicularly to the substrate **400** while making contact with the second blocking dielectric layer **422**. In other words, the word lines **416** have a shape of a pillar. The word lines **416** may have the same structure as those described with reference to FIGS. **13***a* and **13***b*.

The second blocking dielectric layer **422** includes a material having a dielectric constant of at least 3.9. The second blocking dielectric layer **422** may include metallic oxide.

The word line **416** is surrounded by the second blocking dielectric layer **422**. A portion P of the blocking dielectric layer **422** protruding in a lateral direction of the channel pattern **402** serves as the second spacer provided with a high dielectric constant according to the first example embodiment. Accordingly, the back tunneling caused by the concentration of the electric field on the bending portion of the edge region of the word line **416** is reduced, so that the non-volatile memory device according to example embodiments have improved erasing operation characteristics.

FIGS. **15**A and **15**B are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **14**A.

Referring to FIG. **15**A, a structure that stacks the channel patterns **402** and the first insulating interlayer patterns **404** may be formed on a substrate **100**. The structure has the shape of a line extending in the first direction. The structure may be formed in the same manner as that described with reference to FIG. **13**A.

The tunnel oxide layer **410***a*, the charge trap layer **412***a*, and the first blocking dielectric layer **420** are sequentially formed to cover both sidewalls of the structure. The first blocking dielectric layer **420** may include a plurality of dielectric layers.

The second insulating interlayer **405** is fully filled in the gap between the structures.

Referring to FIG. **15**B, the second insulating interlayer patterns **406** having the shape of pillars are formed protruding in a lateral direction of the structure by etching a portion of the second insulating interlayer **405**. The opening **408** between the second insulating interlayer patterns **406** may be formed. The first blocking dielectric layer **420** may be exposed in the opening **408**.

Referring to FIG. **14**A again, the second blocking dielectric layer **422** is formed on the sidewall of the opening **408** and exposed the first blocking dielectric layer in the opening **408**. The second blocking dielectric layer **422** has a dielectric constant greater than those of the dielectric layers constituting the first blocking dielectric layer **420**. The second blocking dielectric layer **422** includes the first part making contact with the sidewall of the channel pattern **402** and the second part protruding from the sidewall of the channel pattern **402** on the end point of the first part.

Thereafter, the word line **416** is fully filled in the opening **408** while making contact with the second blocking dielectric layer **422**.

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FIG. **16**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment. FIG. **16**B is a plan view of FIG. **16**A.

Referring to FIGS. **16**A and **16**B, the vertical gate type non-volatile memory device may include the channel patterns **402** having a multi-layer structure and word lines **416** having the shape of a pillar which are formed on the substrate **400** while facing the sidewalls of the channel patterns **402**.

The channel patterns **402** have the shape of a line extending in the first direction. The channel patterns **402** are stacked in a multi-layer structure while interposing the first insulating interlayer pattern **404** there between. In other words, the first insulating interlayer patterns **404** and the channel patterns **402** may be repeatedly and alternately stacked on the substrate.

The tunnel oxide layer **410***a*, the charge trap layer **412***a*, and a first blocking dielectric layer **430** may be sequentially stacked. The tunnel oxide layer **410***a* may make direct contact with the sidewall of the structure in which the channel pattern **402** and the first insulating interlayer pattern **404** are stacked. The first blocking dielectric layer **430** may include a plurality of dielectric layers.

The blocking dielectric layer **430** includes a material having a dielectric constant of at least 3.9. The blocking dielectric layer **430** may include metallic oxide. If the blocking dielectric layer **430** has a multi-layer structure, the blocking dielectric layer **430** making direct contact with the word line has a dielectric constant greater than those of the blocking dielectric layers formed at other layers.

The word lines **416** have the shape of a pillar on the substrate **400** while making contact with the blocking dielectric layer **430**. The word lines **416** extend in the first direction while being provided in parallel to each other. The word lines **416** may include a metallic material.

Openings **424** are defined between the word lines **416** to expose the blocking dielectric layer **420**.

A high dielectric layer pattern **432** is formed on the sidewall of the opening **434** and exposed the blocking dielectric layer **430** in the opening **434**. The high dielectric layer pattern **432** is formed on the sidewalls of the word lines **416** and the top surface of the blocking dielectric layer **430** between word lines **416**.

The high dielectric layer pattern **432** has a dielectric constant equal to or greater than that of a dielectric layer making direct contact with the word line among dielectric layers constituting the blocking dielectric layer **430**. The high dielectric layer pattern **432** may include a material the same as that of a dielectric layer constituting the blocking dielectric layer **430**. Alternately, the high dielectric layer pattern **432** may include a material different from that of the dielectric layer constituting the blocking dielectric layer **430**.

A second insulating interlayer pattern **436** is formed on the high dielectric layer pattern **432** so that the second insulating interlayer pattern **436** is filled in a gap between the word lines.

The high dielectric layer pattern **432** covers the sidewall of the word line **416**. Accordingly, the high dielectric layer pattern **432** serves as the second spacer provided with a high dielectric constant according to the first example embodiment. Accordingly, the back tunneling caused by the concentration of the electric field at the bending portion of the edge region of the word line **416** is reduced, so that the non-volatile memory device according to example embodiments have improved erasing operation characteristics.

FIGS. **17**A to **17**C are perspective views showing a method of fabricating the vertical gate type non-volatile memory device of FIG. **16***a*.

Referring to FIG. **17**A, the structure stacked the channel patterns **402** and the first insulating interlayer patterns **404** may be formed on a substrate **100**. The structure has the shape of a line extending in the first direction. The structure may be formed in the same manner as that described with reference to FIG. **13**A.

The tunnel oxide layer **410***a*, the charge trap layer **412***a*, and the blocking dielectric layer **430** are sequentially formed to cover both sidewalls of the structure. The blocking dielectric layer **430** may include a plurality of dielectric layers.

The blocking dielectric layer **430** includes a material having a dielectric constant of at least 3.9. The blocking dielectric layer **430** may include metallic oxide. If the blocking dielectric layer **430** has a multi-layer structure, the blocking dielectric layer **430** making direct contact with the word line has a dielectric constant greater than those of the blocking dielectric layers formed at other layers.

A conductive layer **415** is formed on the blocking dielectric layer **430** so that the conductive layer **415** is fully filled in the gap between structures described above. The conductive layer **415** is used to form a word line. The conductive layer **415** may include a metallic material.

Referring to FIG. **17**B, the word lines **416** are formed in the shape of pillars while protruding in a lateral direction of the structure by etching a portion of the conductive layer **415**. An opening **434** is defined between the word lines **416**. The blocking dielectric layer **430** may be exposed in the opening **434**.

Referring to FIG. **17**C, the high dielectric layer pattern **432** is formed on the sidewall of the opening **434** and exposed the first blocking dielectric layer in the opening **434**.

The high dielectric layer pattern **432** has a dielectric constant equal to or greater than that of a dielectric layer making direct contact with the word line among dielectric layers constituting the blocking dielectric layer **430**. The high dielectric layer pattern **432** may include a material the same as that of a dielectric layer constituting the blocking dielectric layer **430**. In addition, the high dielectric layer pattern **432** may include a material different from that of the dielectric layer constituting the blocking dielectric layer **430**.

Referring to FIG. **16**A again, the second insulating interlayer pattern **436** is formed on the high dielectric layer patterns so that the second insulating interlayer pattern **436** is fully filled in the opening **434**.

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FIG. **18**A is a perspective view showing a part of a vertical gate type non-volatile memory device according to another example embodiment. FIG. **18**B is a plan view of FIG. **18***a*.

Referring to FIGS. **18**A and **18**B, the vertical gate type non-volatile memory device may include the channel patterns **402** having a multi-layer structure and the word lines **416** having the shape of a pillar on the substrate **400** while facing the sidewalls of the channel patterns **402**.

The channel patterns **402** have the shape of a line extending in the first direction. The channel patterns **402** are stacked in a multi-layer structure while interposing the first insulating interlayer pattern **404** there between. In other words, the first insulating interlayer patterns **404** and the channel patterns **402** may be repeatedly and alternately stacked on the substrate.

The tunnel oxide layer **410***a*, the charge trap layer **412***a*, and a first blocking dielectric layer **430** may be sequentially stacked. The tunnel oxide layer **410***a* may make direct contact with the sidewall of the structure in which the channel pattern **402** and the first insulating interlayer pattern **404** are stacked. The blocking dielectric layer **430** may include a plurality of dielectric layers.

The blocking dielectric layer **430** includes a material having a dielectric constant of at least 3.9. The blocking dielectric layer **430** may include metallic oxide. If the blocking dielectric layer **430** has a multi-layer structure, the blocking dielectric layer **430** making direct contact with the word line has a dielectric constant greater than those of the blocking dielectric layers formed at other layers.

The word lines **416** having the shape of a pillar on substrate **400** make contact with the blocking dielectric layer **430**. In other words, the word lines **416** are formed in the first direction in parallel to each other. The word lines **416** include a metallic material.

Openings **434** are defined between the word lines **416** to expose both sidewalls of the blocking dielectric layer **430**.

The high dielectric layer pattern **440** is provided in such a manner that the high dielectric layer pattern **440** is fully filled in the opening **434**. The high dielectric layer pattern **440** may have the shape of a pillar making contact with the blocking dielectric layer **430** and the sidewall of the word line **416**.

The high dielectric layer pattern **440** has a dielectric constant equal to or greater than that of a dielectric layer making direct contact with the word line among dielectric layers constituting the blocking dielectric layer **430**. The high dielectric layer pattern **440** may include a material the same as that of a dielectric layer constituting the blocking dielectric layer **430**. In addition, the high dielectric layer pattern **440** may include a material different from that of the dielectric layer constituting the blocking dielectric layer **430**.

The high dielectric layer pattern **440** covers the sidewall of the word line **416**. Accordingly, the high dielectric layer pattern **440** serves as the second spacer provided with a high dielectric constant according to the first example embodiment. Accordingly, the back tunneling caused by the concentration of the electric field at the bending portion of the edge region of the word line **416** is reduced, so that the non-volatile memory device according to example embodiments has improved erasing operation characteristics.

The vertical gate type non-volatile memory device illustrated in FIG. **18**A may be formed in the same manner as that described with reference to FIGS. **17**A and **17**B.

First, the structure illustrated in FIG. **17**B is formed by performing the processes the same as those described with reference to FIGS. **17**A and **17**B.

Next, as illustrated in FIG. **18**A, the high dielectric layer pattern **440** is formed on the blocking dielectric layer while being fully filled in the opening. Accordingly, the high dielectric layer pattern **440** has the shape of pillars.

The high dielectric layer pattern **440** has a dielectric constant equal to or greater than that of a dielectric layer making direct contact with the word line among dielectric layers constituting the blocking dielectric layer **430**. The high dielectric layer pattern **440** may include a material the same as that of a dielectric layer constituting the blocking dielectric layer **430**. Alternately, the high dielectric layer pattern **440** may include a material different from that of the dielectric layer constituting the blocking dielectric layer **430**.

FIG. **19** is a block diagram illustrating a memory system provided with the non-volatile memory device according to one of the example embodiments.

Referring to FIG. **19**, a non-volatile memory device **510** is electrically connected to a central processing unit (CPU) **520** provided in a memory system **500** such as a computer. The memory system **500** may include a personal computer (PC), a personal data assistant (PDA), and the like. The non-volatile memory device **510** may be directly connected with the CPU **520** or may be connected with the CPU **520** through a bus. The non-volatile memory device **510** has a gate structure according to the various example embodiments. Accordingly, the non-volatile memory device **510** has improved erase saturation characteristics and improved reliability. Since the non-volatile memory device **510** is applied to the memory system **500**, the performance of the memory system **500** can be improved.

As described above, the non-volatile memory device including the gate structure according to the example embodiments that have improved erase saturation characteristics and superior reliability. The non-volatile memory device is applicable to various memory systems and various electronic products.

The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the present inventive concepts. Accordingly, all such modifications are intended to be included within the scope of the present inventive concepts as defined in the claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A vertical type non-volatile memory device, comprising:

a channel pattern vertically extending from a substrate;

a tunnel oxide layer and a charge trap layer sequentially stacked on a sidewall of the channel pattern;

a blocking layer pattern structure including a first portion and a second portion, the first portion being on the charge trap layer, the second portion extending from an end of the first portion to protrude from a sidewall of the channel pattern, and the blocking layer pattern structure having a dielectric constant that is greater than that of the tunnel oxide layer pattern; and

at least one word line formed on the first and second portions of the blocking layer pattern structure.

2. The vertical type non-volatile memory device of claim **1**, wherein the second portion of the blocking layer pattern structure contacts an upper surface and a lower surface of the word line, and extends in a horizontal direction.

3. The vertical type non-volatile memory device of claim **1**, wherein the blocking layer pattern structure includes a first blocking layer pattern and a second blocking layer pattern, the first blocking layer pattern contacting the charge trap layer and having a first dielectric constant, and the second blocking layer pattern being on the first blocking layer pattern and having a second dielectric constant that is greater than the first dielectric constant.

4. The vertical type non-volatile memory device of claim **3**, wherein the first blocking layer pattern includes the first portion, and the second blocking layer pattern includes both of the first and second portions.

5. The vertical type non-volatile memory device of claim **4**, wherein the second portion of the second blocking layer pattern contacts an upper surface and a lower surface of the word line.

6. The vertical type non-volatile memory device of claim **1**, wherein the at least one word line includes a plurality of word lines that are vertically spaced apart from each other on the sidewall of the channel pattern.

7. The vertical type non-volatile memory device of claim **6**, further comprising:

insulating interlayer patterns that are disposed between the word lines on the sidewall of the channel pattern.

8. The vertical type non-volatile memory device of claim **7**, wherein the second portion of the blocking layer pattern structure is on surfaces of the insulating interlayer patterns.

9. The vertical type non-volatile memory device of claim **1**, wherein at least one of the tunnel oxide layer and the charge trap layer extends on surfaces of the insulating interlayer patterns and the channel pattern.

10. The vertical type non-volatile memory device of claim **1**, wherein the tunnel oxide layer and the charge trap layer are stacked on an entire surface of the channel pattern.

11. The vertical type non-volatile memory device of claim **1**, wherein the blocking layer pattern structure includes any one selected from the group consisting of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and zirconium oxide (ZrO_2).

12. The vertical type non-volatile memory device of claim **1**, wherein the word line includes a barrier layer pattern and a metal layer pattern.

13. A vertical type non-volatile memory device, comprising:

a channel pattern vertically extending from a substrate, the channel pattern having a pillar shape;

a tunnel oxide layer and a charge trap layer sequentially stacked on a sidewall of the channel pattern;

insulating interlayer patterns vertically spaced apart from each other on a sidewall of the channel pattern;

a blocking layer pattern structure including a first portion and a second portion, the first portion being on the charge trap layer, the second portion extending on surfaces of the insulating interlayer patterns, and the blocking layer pattern structure having a dielectric constant that is greater than that of the tunnel oxide layer pattern; and

word lines being between the insulating interlayer patterns and contacting the first and second portions of the blocking layer pattern structure.

14. The vertical type non-volatile memory device of claim **13**, wherein the blocking layer pattern structure includes a first blocking layer pattern and a second blocking layer pattern, the first blocking layer pattern contacting the charge trap layer and having a first dielectric constant, and the second blocking layer pattern being on the first blocking layer pattern and having a second dielectric constant that is greater than the first dielectric constant.

15. The vertical type non-volatile memory device of claim **13**, wherein the blocking layer pattern structure includes any one selected from the group consisting of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAlO_3$), lanthanum hafnium oxide (LaHfO), hafnium aluminum oxide (HfAlO), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and zirconium oxide (ZrO_2).

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