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(54) **ELECTROSTATIC DISCHARGE PROTECTION STRUCTURE**

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H01L 23/62 (2006.01)
H01L 29/739 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7393*** (2013.01)
USPC **257/360**; 257/355; 257/361

(58) **Field of Classification Search**
USPC 257/360
See application file for complete search history.

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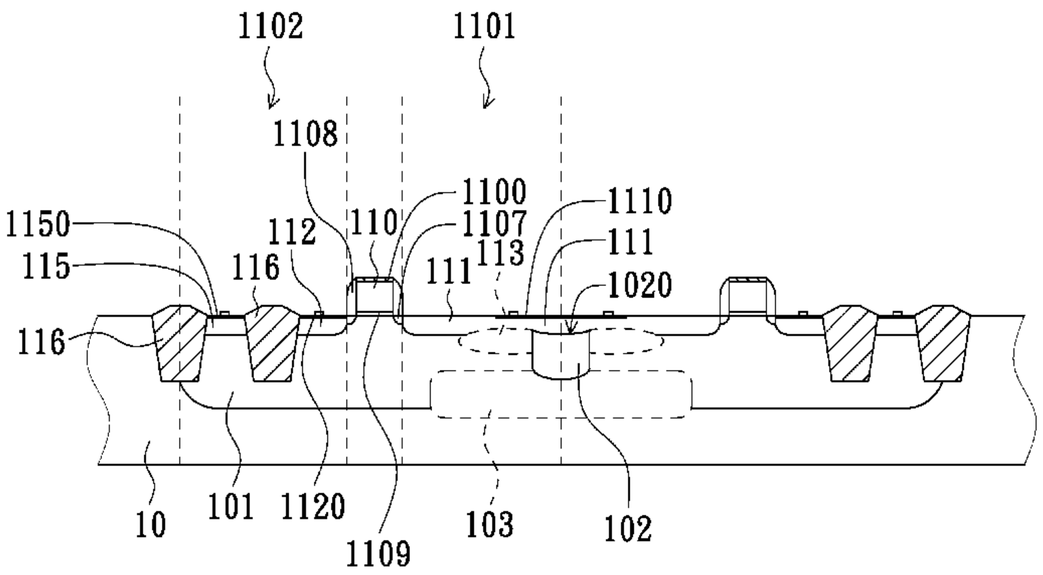
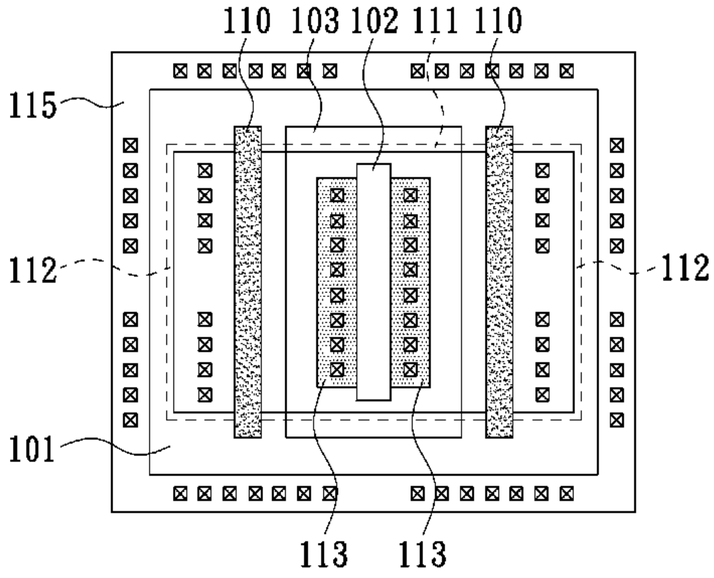
(57) **ABSTRACT**

An electrostatic discharge protection structure includes a semiconductor substrate, a first well region, a gate structure, a second well region, a second well region, a second conductive region, and a deep well region. The first well region contains first type conducting carriers. The second well region is disposed within the first well region, and contains second type conducting carriers. The first conductive region is disposed on the surface of the first well region, and contains the second type conducting carriers. The deep well region is disposed under the second well region and the first conductive region, and contacted with the second well region. The deep well region contains the second type conducting carriers.

14 Claims, 17 Drawing Sheets





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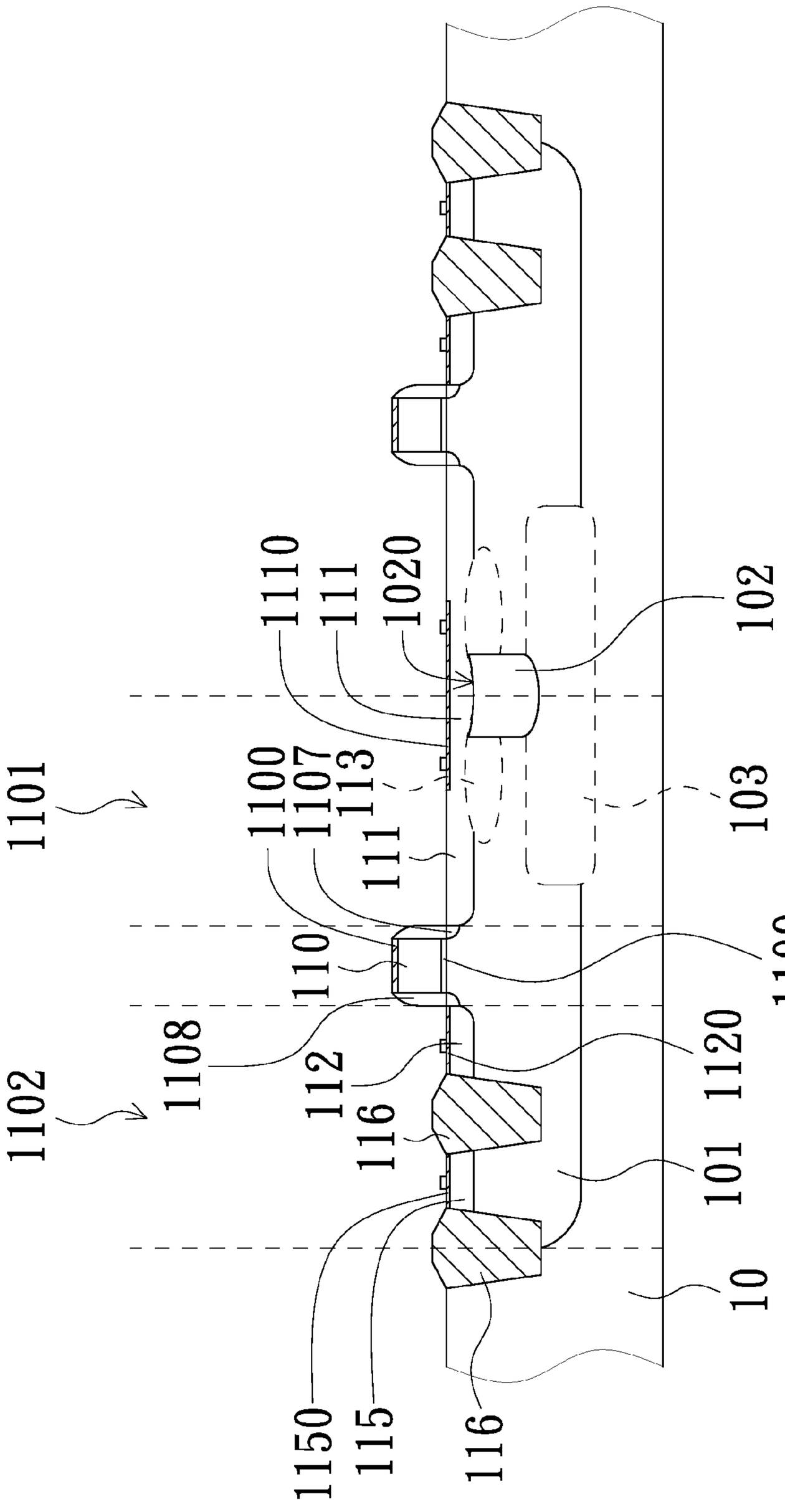
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FIG. 1A

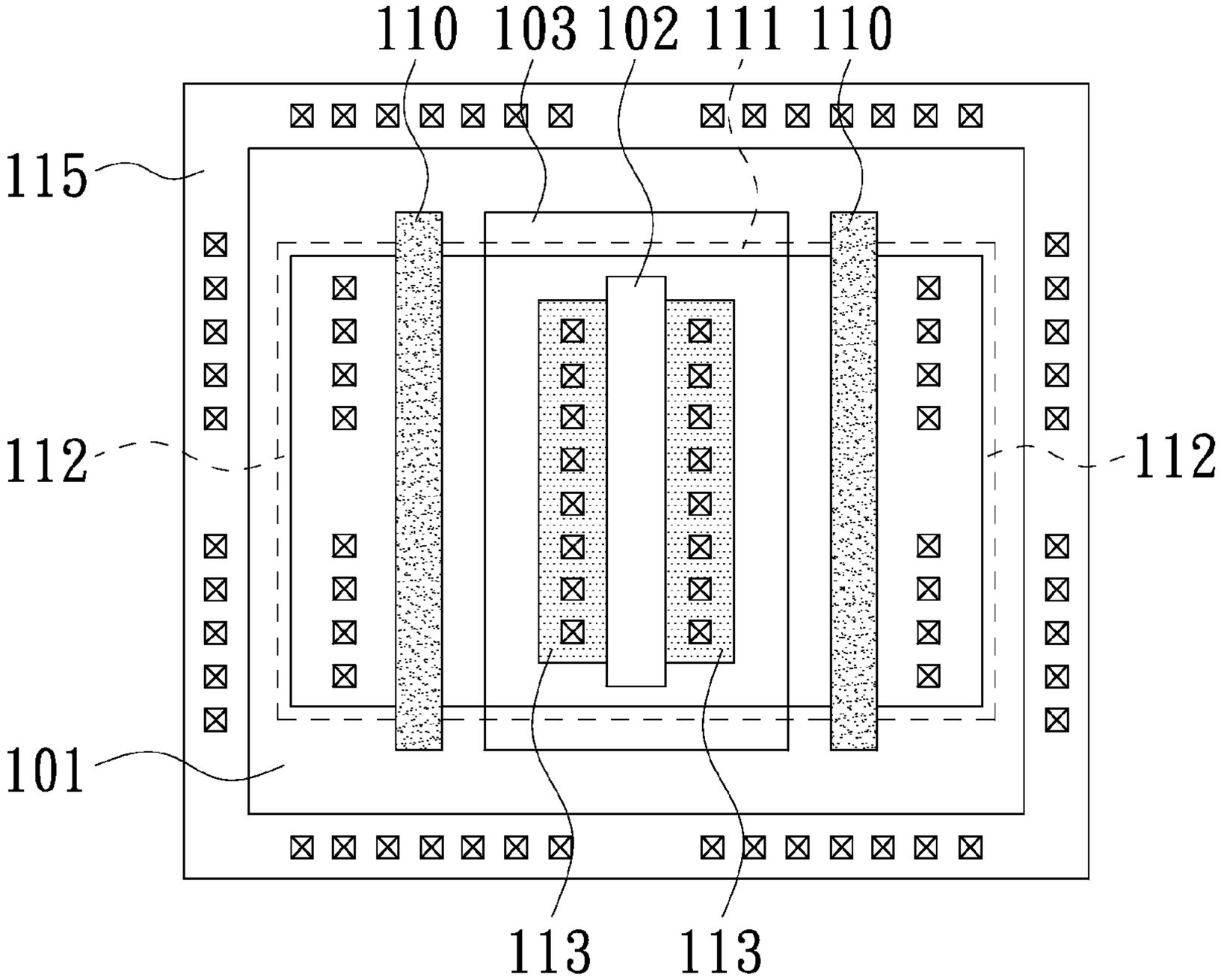

FIG. 1B

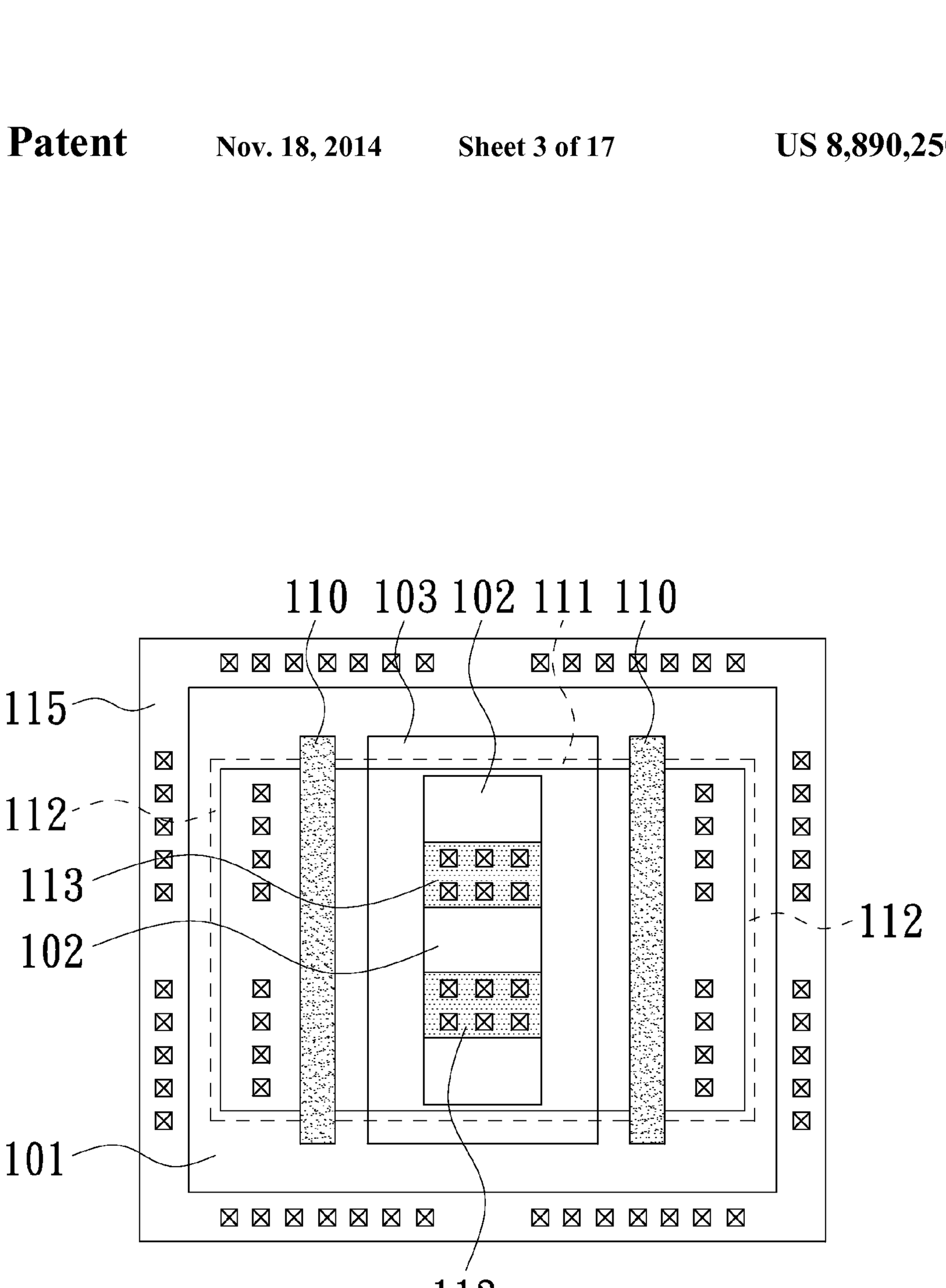

FIG. 1C

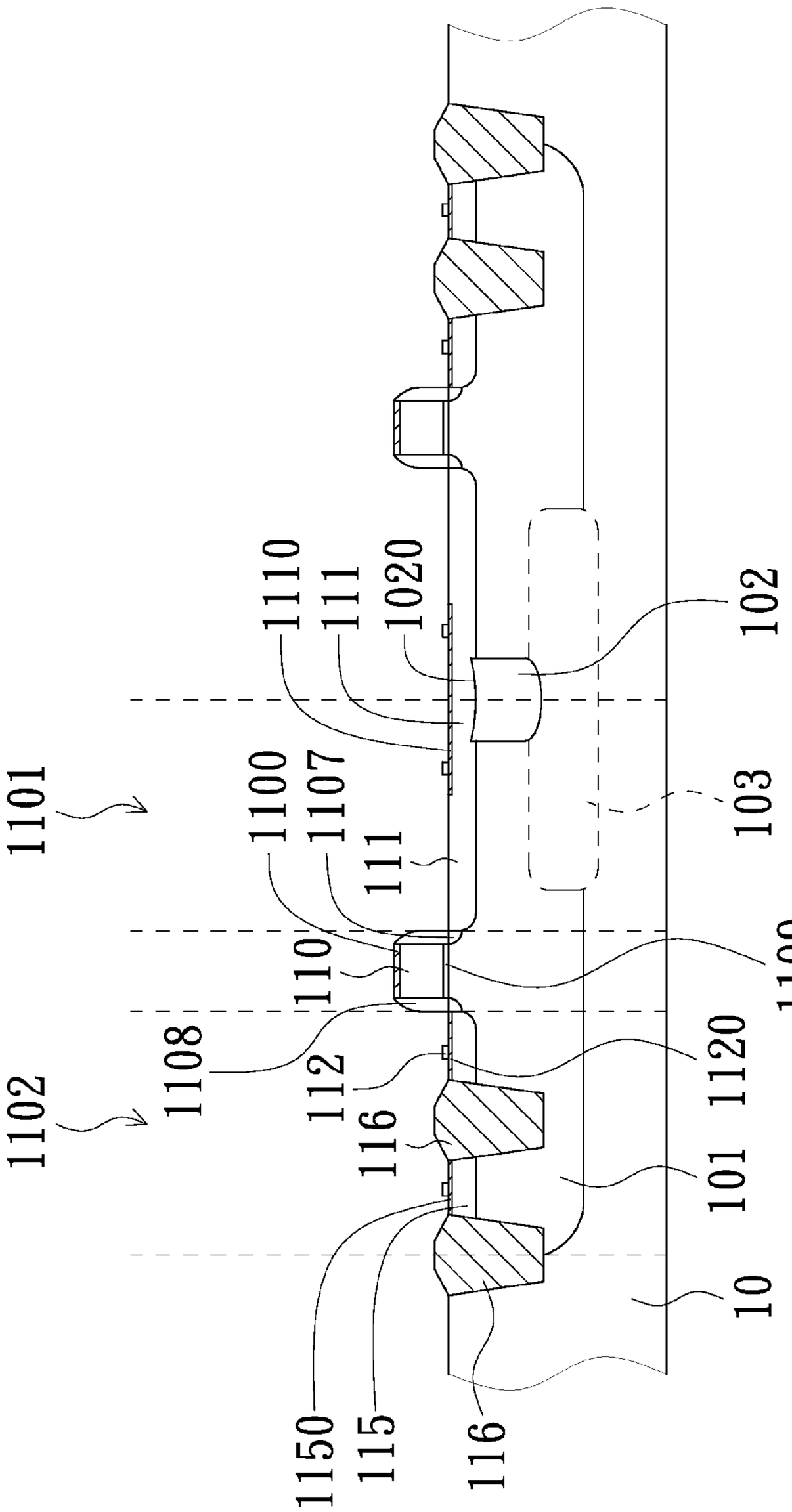
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FIG. 2A

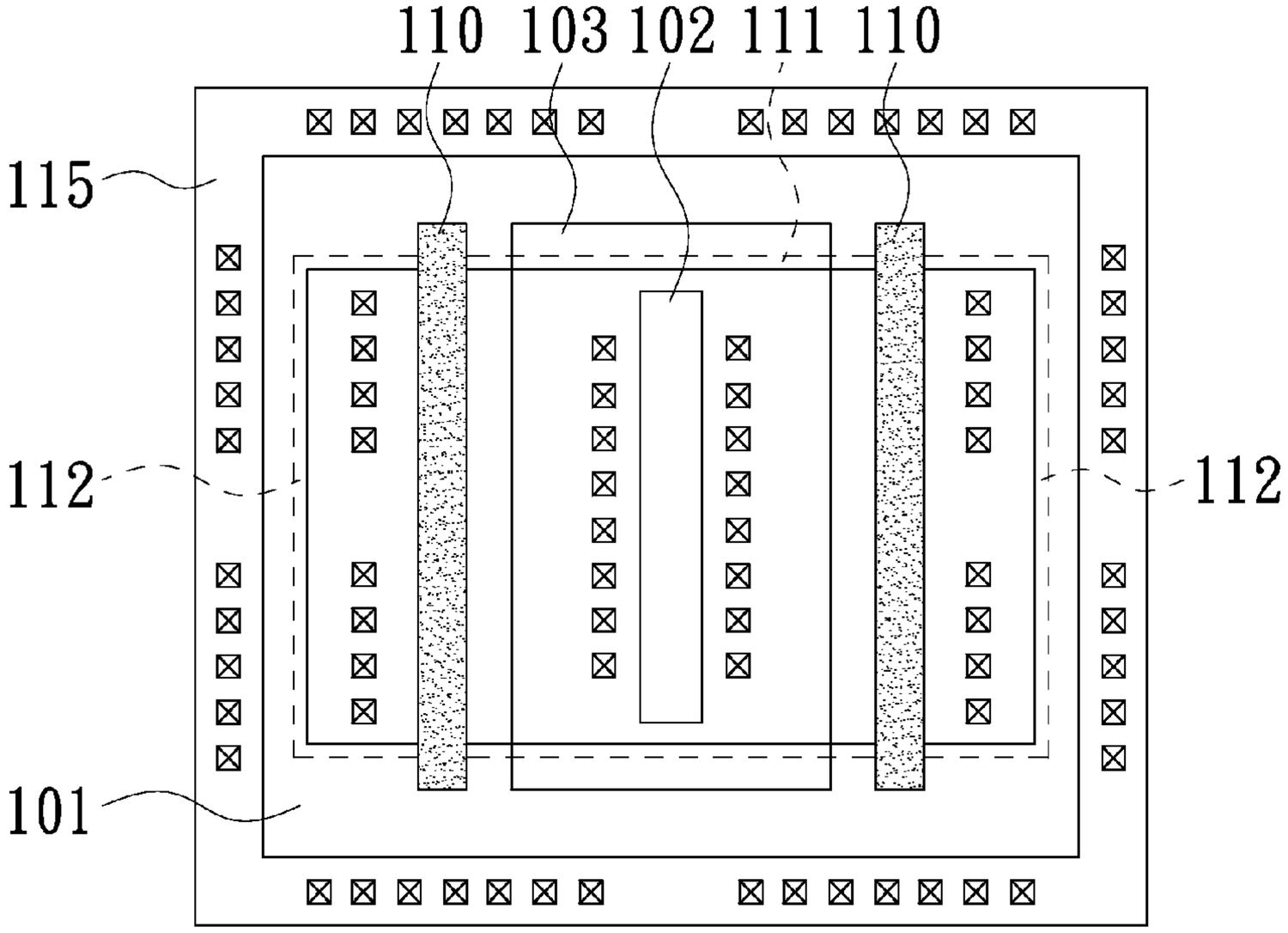

FIG. 2B

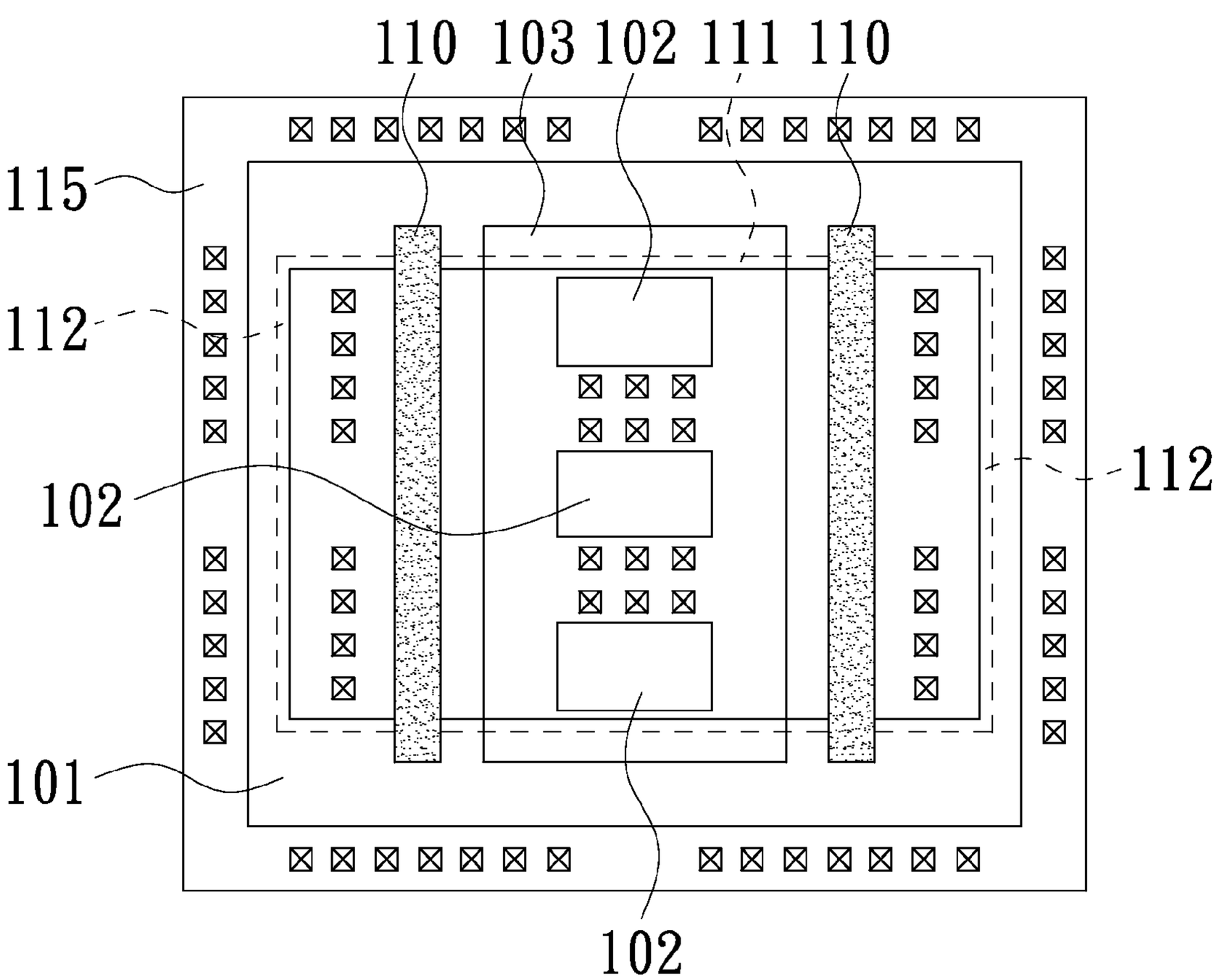

FIG. 2C

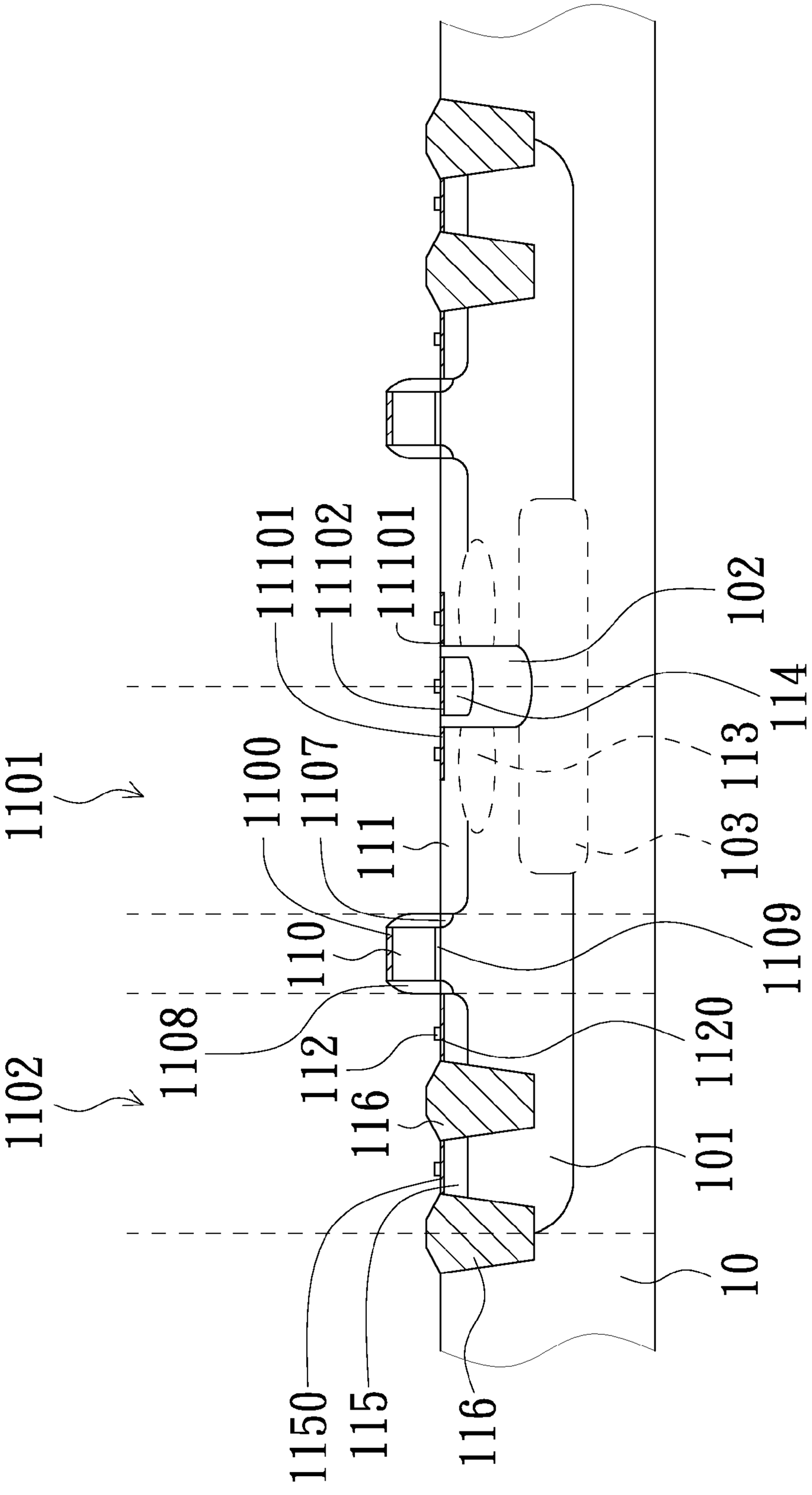
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FIG. 3A

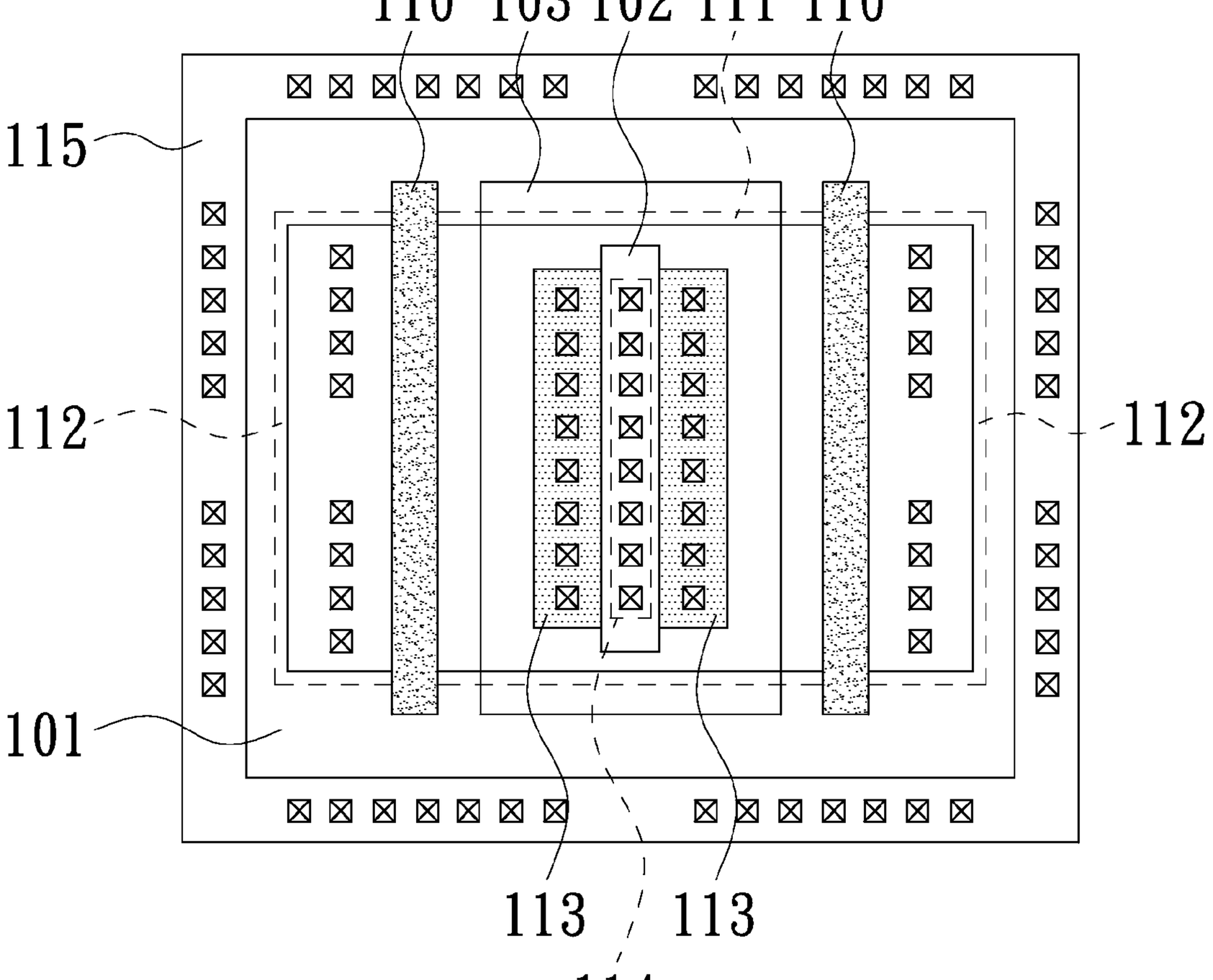

FIG. 3B

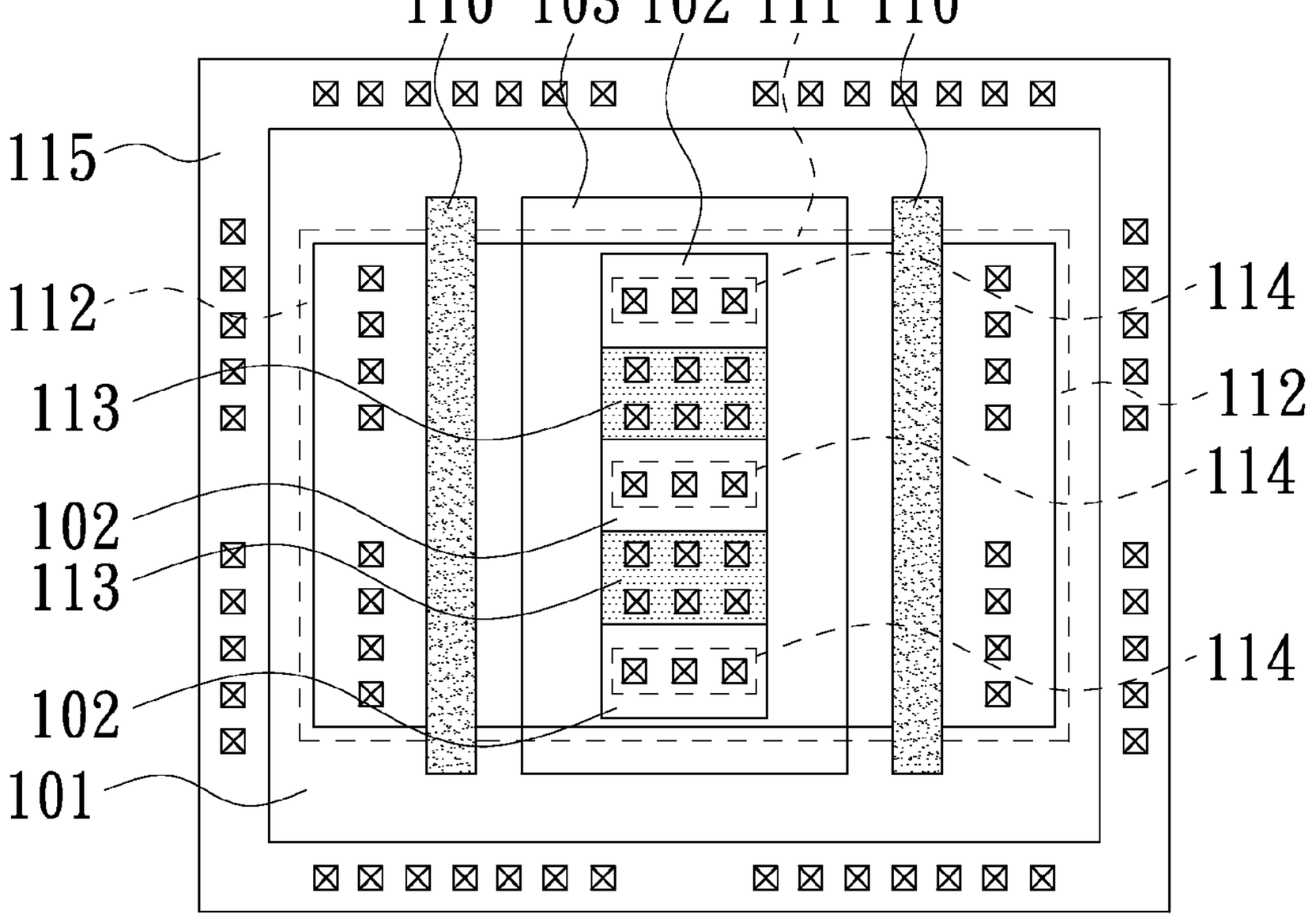

FIG. 3C

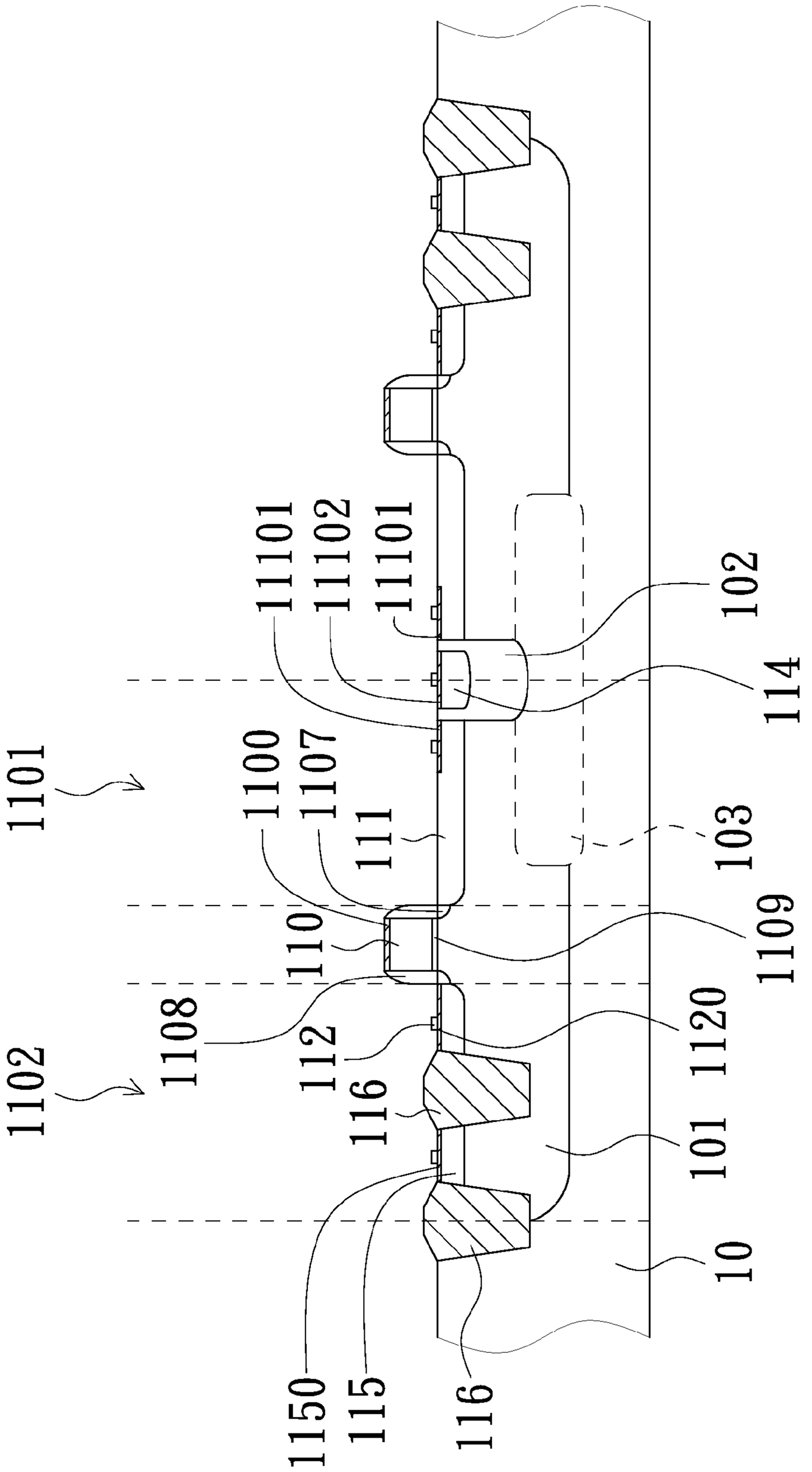
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FIG. 4A

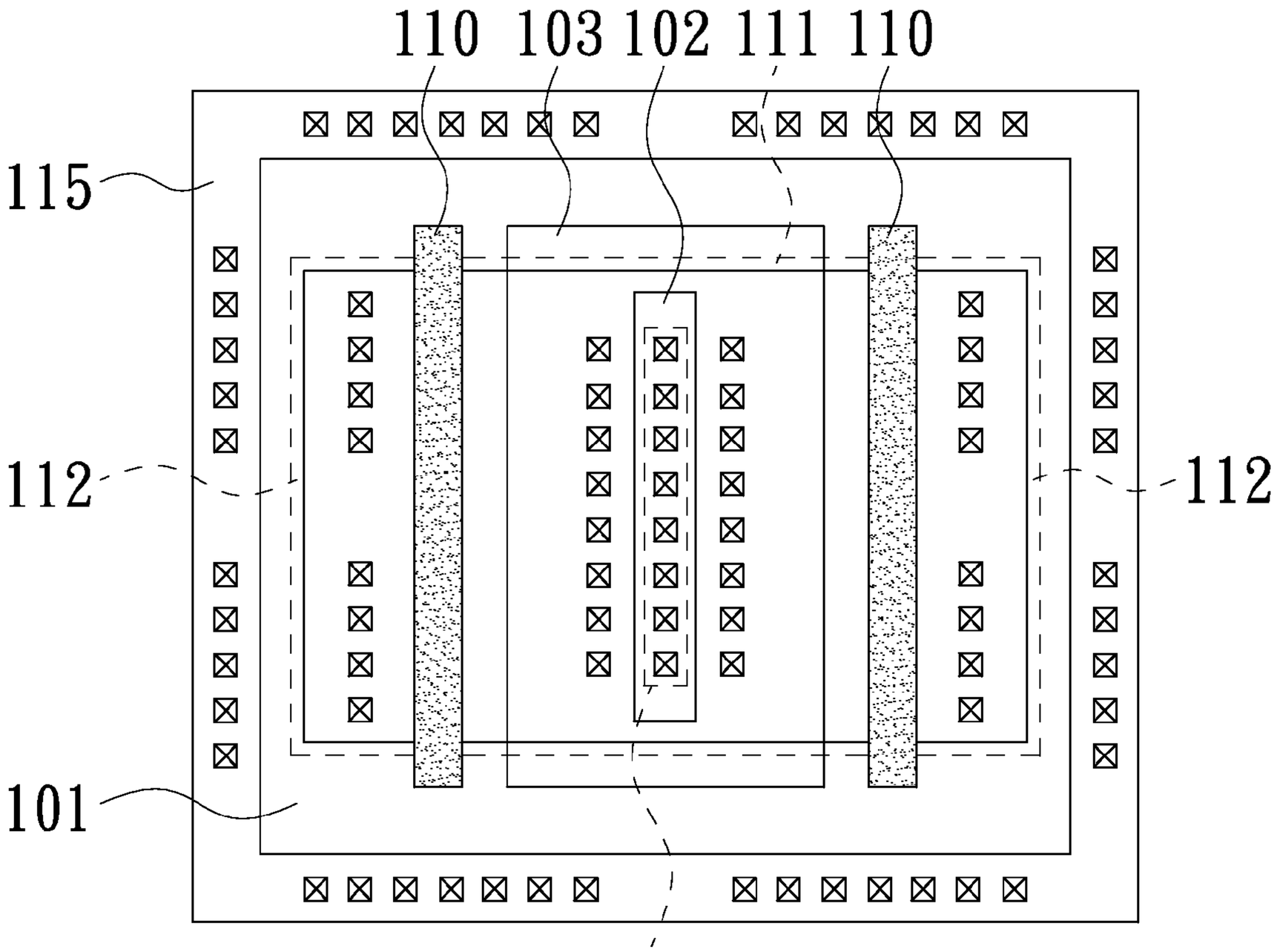

FIG. 4B

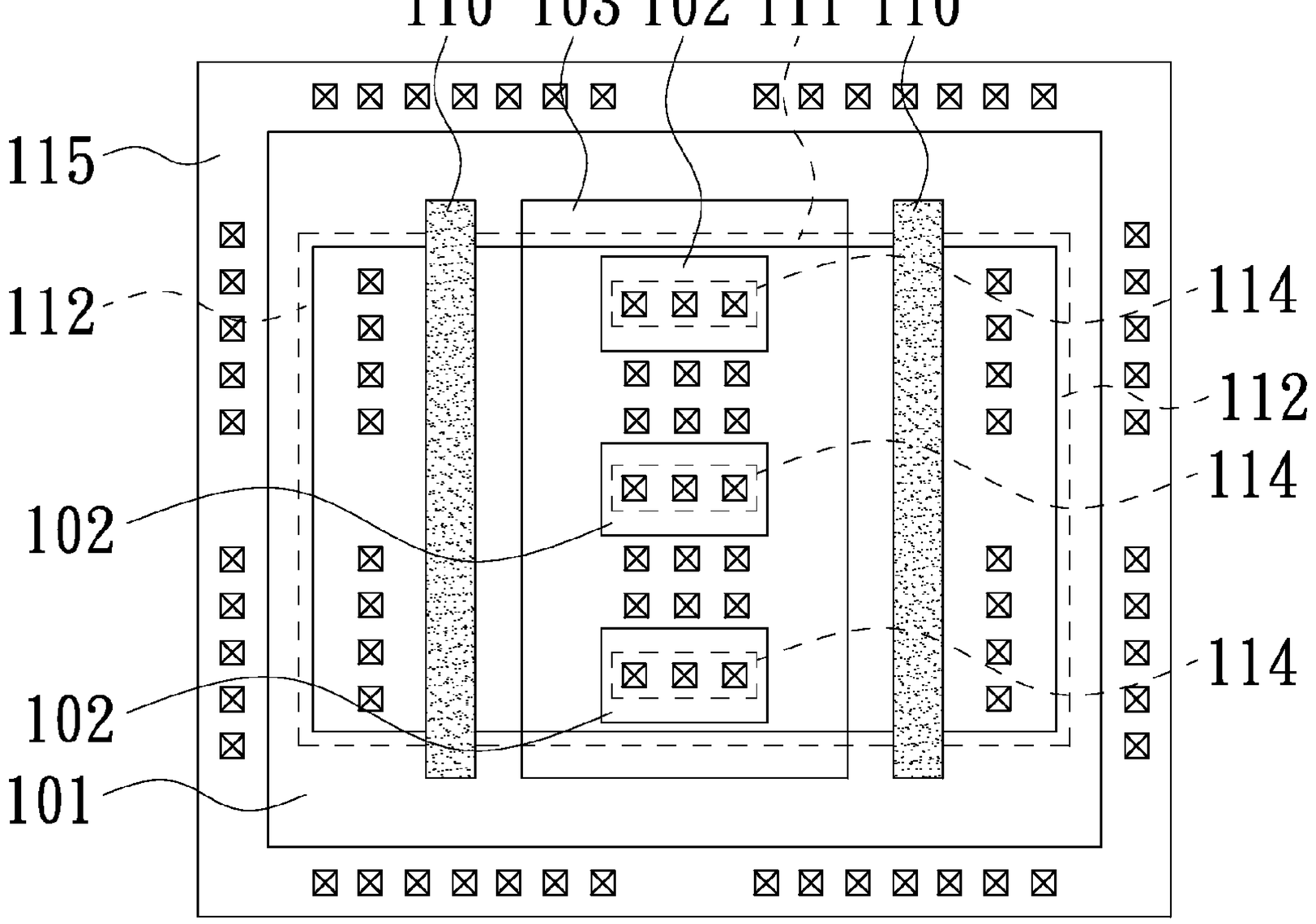

FIG. 4C

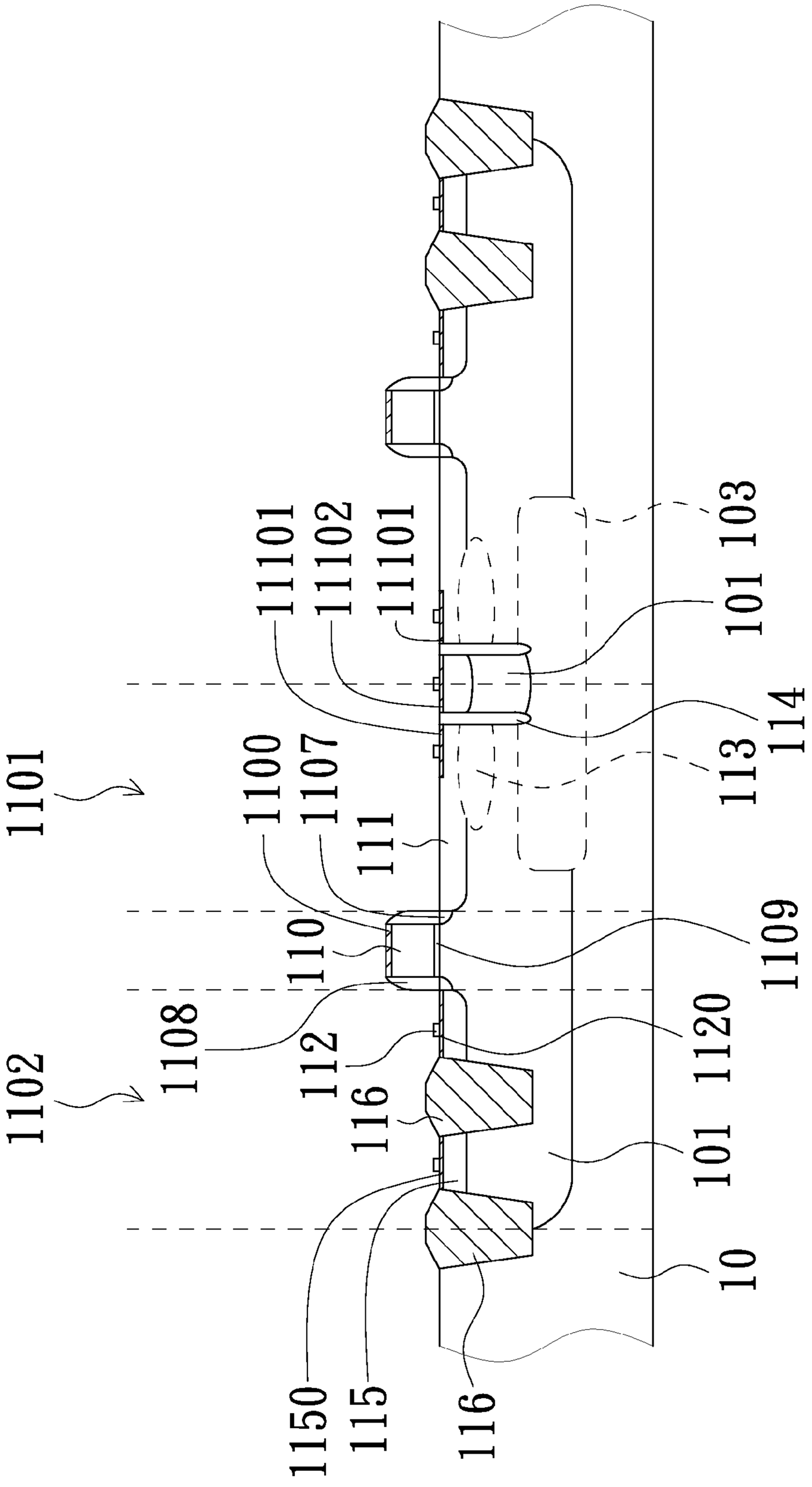
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FIG. 5A

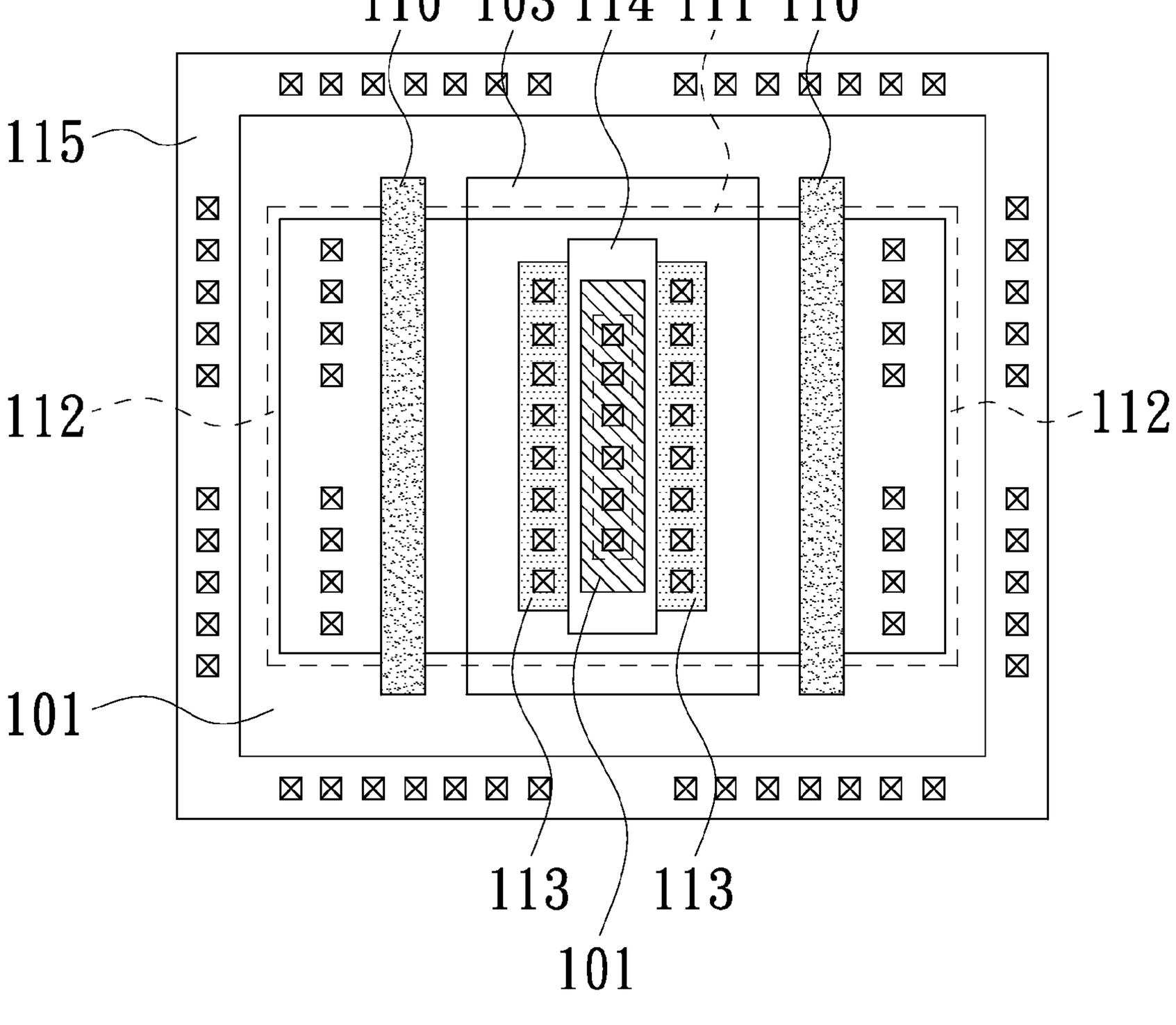

FIG. 5B

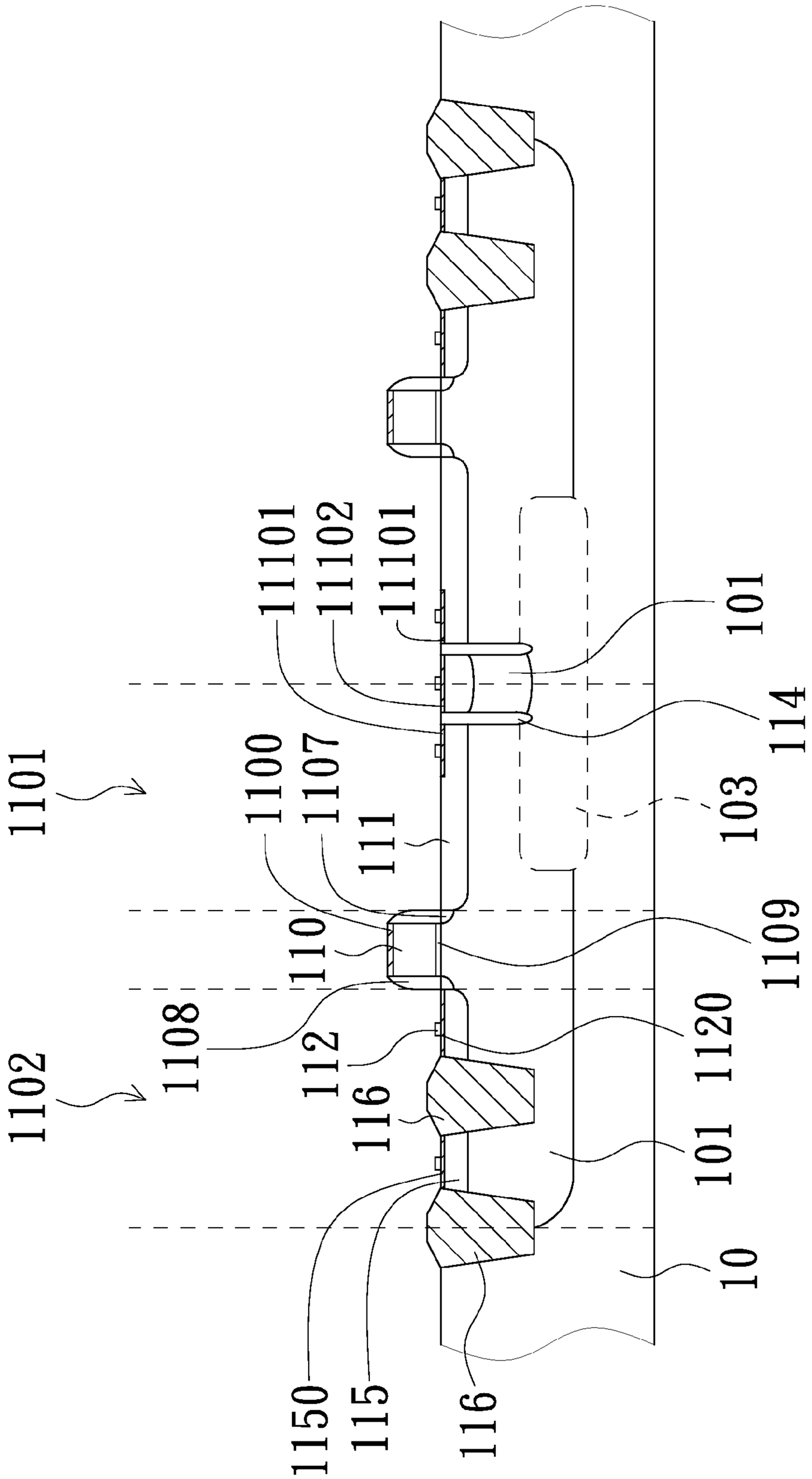
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FIG. 6A

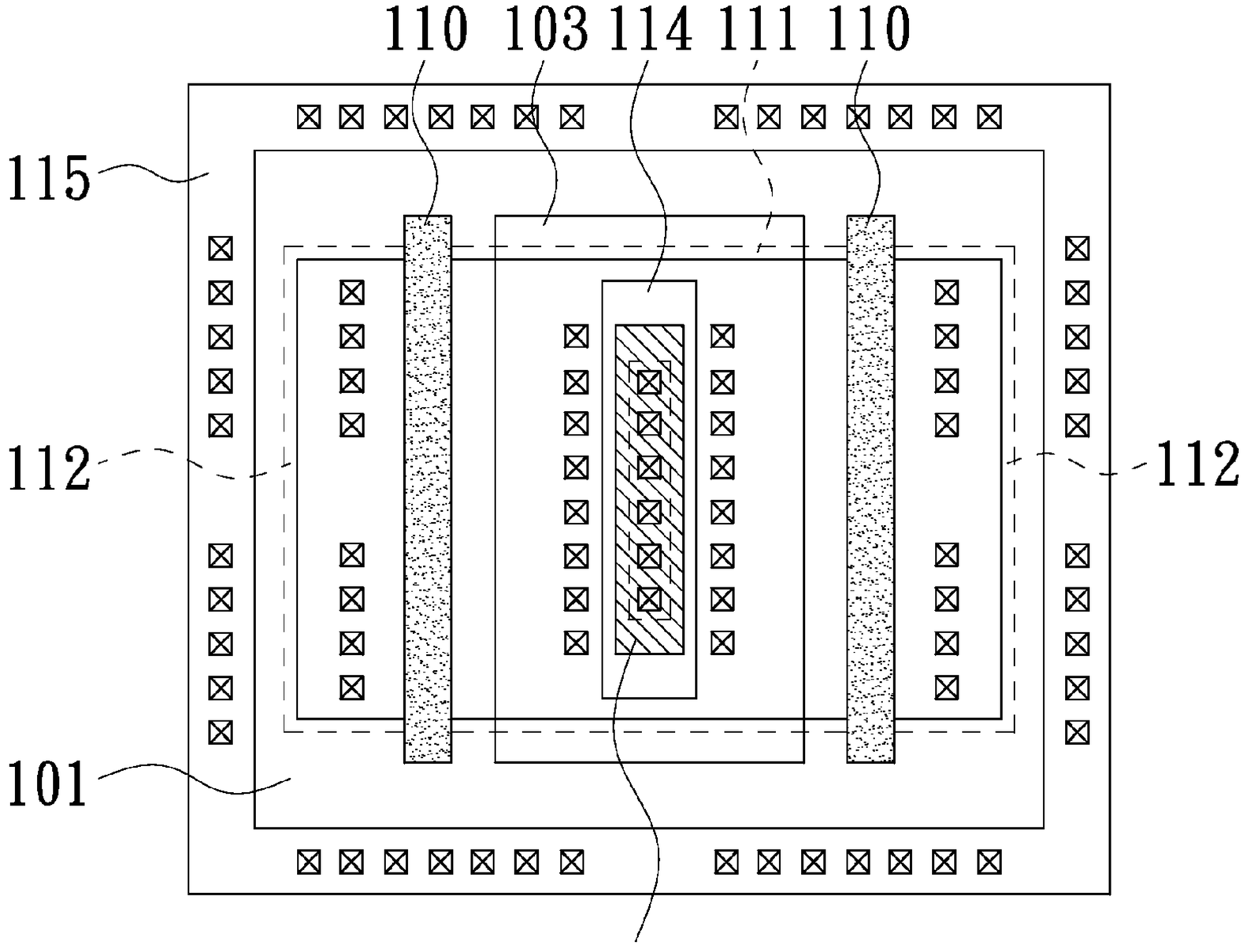

FIG. 6B

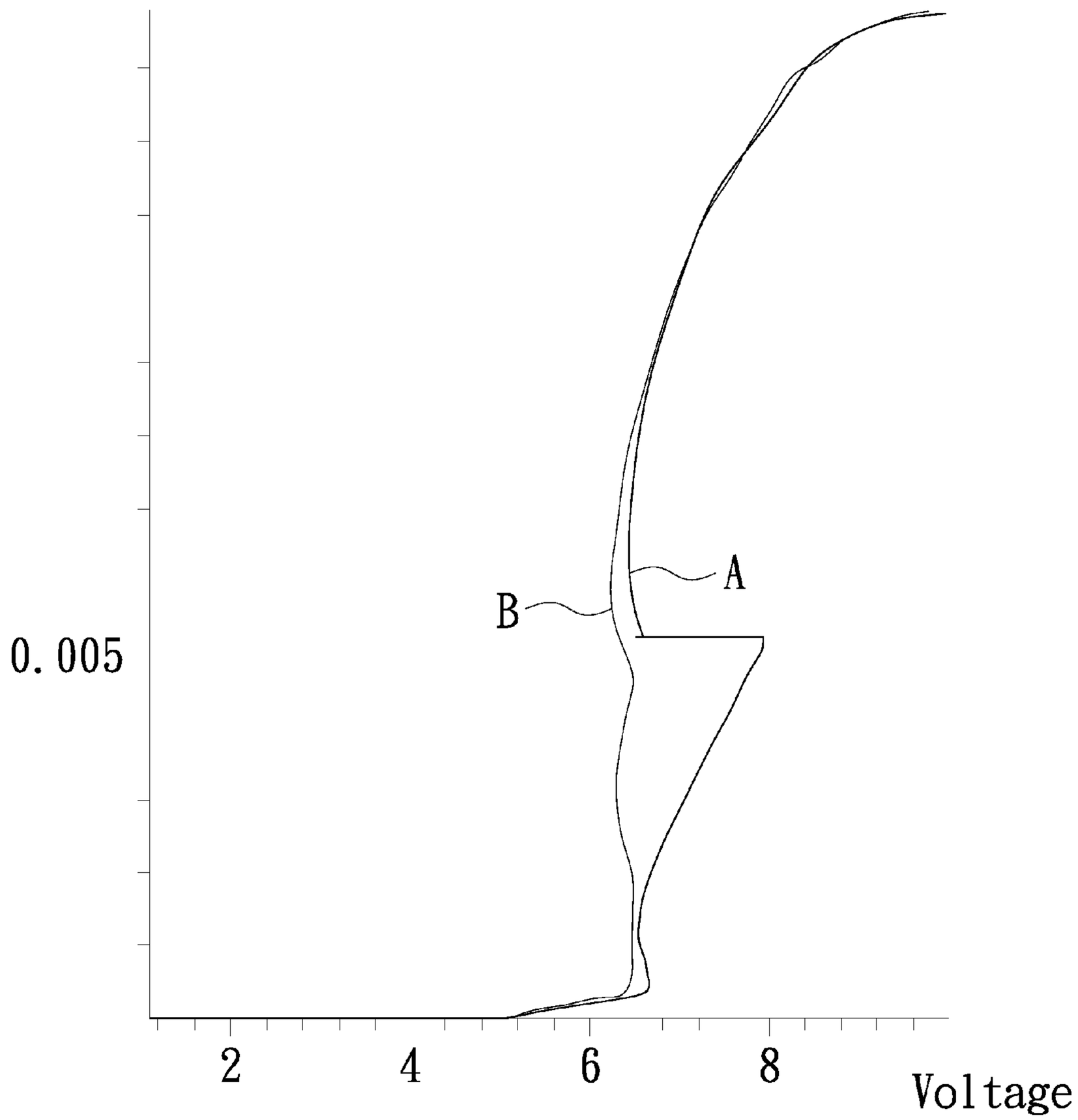

FIG. 7

ELECTROSTATIC DISCHARGE PROTECTION STRUCTURE

FIELD OF THE INVENTION

The present invention relates to an electrostatic discharge protection structure, and more particularly to an electrostatic discharge protection structure for a semiconductor integrated circuit device.

BACKGROUND OF THE INVENTION

In the process of producing or using a semiconductor integrated circuit device, electrostatic discharge (ESD) may result in sudden flow of electricity. The sudden flow of electricity may cause damage to the semiconductor integrated circuit device or the functional circuit, and reduce the production efficiency and the product yield.

For reducing the influence of the high ESD current on the semiconductor integrated circuit device, an electrostatic discharge protection structure is integrated into the semiconductor integrated circuit device. Generally, once the electrostatic discharge protection structure is triggered, the holding voltage of the electrostatic discharge protection structure in a snapback breakdown condition may be pulled down to a low voltage. If the holding voltage is lower than a high power supply voltage of the integrated circuit device, the high-voltage integrated circuit device is susceptible to the latchup-like danger in the real life application system.

Therefore, there is a need of providing an electrostatic discharge protection structure to eliminate the above drawbacks.

SUMMARY OF THE INVENTION

In accordance with an aspect, the present invention provides an electrostatic discharge protection structure. The electrostatic discharge protection structure includes a semiconductor substrate, a first well region, a gate structure, a second well region, a second well region, a second conductive region, and a deep well region. The first well region is disposed in the semiconductor substrate, and contains first type conducting carriers. The gate structure is disposed over a surface of the first well region. The second well region is disposed within the first well region and located at a first side of the gate structure. The second well region contains second type conducting carriers. The first conductive region is disposed on the surface of the first well region, and arranged between the gate structure and the second well region, wherein the first conductive region contains the second type conducting carriers. The second conductive region is disposed on the surface of the first well region, and the located at a second side of the gate structure, wherein the second conductive region contains the second type conducting carriers. The deep well region is disposed under the second well region and the first conductive region, and contacted with the second well region. The deep well region is separated from the first conductive region by the first well region. The deep well region contains the second type conducting carriers. Preferably, the concentration of the second type conducting carriers of the deep well region may be lower than the concentration of second type conducting carriers of the second well region.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

FIG. **1**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a first embodiment of the present invention;

FIG. **1**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **1**A;

FIG. **1**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **1**A;

FIG. **2**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a second embodiment of the present invention;

FIG. **2**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **2**A;

FIG. **2**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **2**A;

FIG. **3**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a third embodiment of the present invention;

FIG. **3**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **3**A;

FIG. **3**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **3**A;

FIG. **4**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a fourth embodiment of the present invention;

FIG. **4**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **4**A;

FIG. **4**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **4**A;

FIG. **5**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a fifth embodiment of the present invention;

FIG. **5**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **5**A;

FIG. **6**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a sixth embodiment of the present invention;

FIG. **6**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **6**A; and

FIG. **7** schematically illustrates the relationships between the voltage and current of a conventional electrostatic discharge protection structure and of the electrostatic discharge protection structure of the first embodiment of present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of preferred embodiments of this invention are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

Hereinafter, an electrostatic discharge protection structure according to a first embodiment of the present invention is illustrated in FIGS. **1**A~**1**C.

FIG. **1**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to the first embodiment of the present invention. In this embodiment, the electrostatic discharge protection structure is implemented by a metal-oxide-semiconductor. The metal-oxide-semiconductor is constructed in a semiconductor substrate **10**. A first well region **101** with first type conducting carriers is formed in the semiconductor substrate **10**. In this embodiment, the first type conducting carriers are hole carriers. That

is, the first well region **101** is a P well region. A gate structure **110** of the metal-oxide-semiconductor is disposed over a surface of the first well region **101**. The gate structure **110** comprises a gate dielectric layer **1109**, a gate sidewall **1108**, and a lightly doped drain region **1107**. A first conductive region **111** is used as a drain region of the metal-oxide-semiconductor structure. The first conductive region **111** is disposed on the surface of the first well region **101**, and is located at a first side **1101** of the gate structure **110**. A second conductive region **112** is used as a source region of the metal-oxide-semiconductor structure. The second conductive region **112** is disposed on the surface of the first well region **101**, and located at a second side **1102** of the gate structure **110**. The first conductive region **111**, the first well region **101** and the second conductive region **112** collaboratively define a parasitic bipolar junction transistor. The parasitic bipolar junction transistor provides a current path for discharging the electrostatic discharge current. For achieving desired electrical properties, the first conductive region **111** is wider than the second conductive region **112**.

A second well region **102** is disposed within the first well region **101**, and located at the first side **1101** of the gate structure **110**. A top surface **1020** of the second well region **102** is contacted with the first conductive region **111**. The second well region **102** contains second type conducting carriers. Both of the first conductive region **111** and the second conductive region **112** contain the second type conducting carriers. In this embodiment, the second type conducting carriers are electron carriers. Consequently, the first conductive region **111** and the second conductive region **112** are n+ regions, wherein the concentration of the second type conducting carriers of the second well region **102** is lower than the concentration of the second type conducting carriers of the n+ regions.

Moreover, a deep well region **103** is disposed under the second well region **102** and the first conductive region **111**, and contacted with the second well region **102**. The deep well region **103** contains the second type conducting carriers. The deep well region **103** is also separated from the first conductive region **111** by the first well region **101**. The concentration of the second type conducting carriers (e.g. electron carriers) of the deep well region **103** is lower than the concentration of the second type conducting carriers of the second well region **102**. The combination of the second well region **102** and the deep well region **103** also provides an additional current path for discharging the electrostatic discharge current. Generally, if the current path provided by the parasitic bipolar junction transistor results in a snapback breakdown condition, the holding voltage of the electrostatic discharge protection structure may be pulled down to a very low voltage. Due to the additional current path provided by the combination of the second well region **102** and the deep well region **103**, the above drawbacks can be effectively solved.

Moreover, a third conductive region **113** is arranged between the second well region **102**, the first conductive region **111** and the deep well region **103**. The third conductive region **113** contains the first type conducting carriers (e.g. hole carriers). The concentration of the first type conducting carriers of the third conductive region **113** is higher than the concentration of the first type conducting carriers of the first well region **101**. The third conductive region **113** is separated from the deep well region **103** by the first well region **101**. In this embodiment, the third conductive region **113** is formed by performing an implantation process to implant P-type dopants into the first well region **101** to increase concentration of the hole carriers. Moreover, since the third conductive region **113** is contacted with a bottom surface of the first conductive region **111**, a high-concentration PN junction is formed between the third conductive region **113** and the first conductive region **111**. The PN junction is effective to reduce the breakdown voltage of the parasitic bipolar junction transistor. Moreover, a drain contact region **1110** is disposed on a surface of the first conductive region **111**. The second well region **102** is disposed under the drain contact region **1110**. In addition, the entire second well region **102** is covered by a projection area of the drain contact region **1110**. A source contact region **1120** is disposed on a surface of the second conductive region **112**. A gate contact region **1100** is disposed on a surface of the gate structure **110**. Moreover, a fifth conductive region **115** is disposed within the first well region **101** and arranged between two isolation structures **116**. The fifth conductive region **115** contains the first type conducting carriers (e.g. hole carriers). The concentration of the first type conducting carriers of the fifth conductive region **115** is higher than the concentration of the first type conducting carriers of the first well region **101**. In addition, a body contact region **1150** is formed on a surface of the fifth conductive region **115**.

For saving space of the layout area, the electrostatic discharge protection structure has a symmetrical shared source region. FIG. **1**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **1**A. FIG. **1**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **1**B. Except for the relative locations between the second well region **102** and the third conductive region **113**, the layout configurations of the FIGS. **1**B and **1**C are substantially identical.

FIG. **2**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a second embodiment of the present invention. FIG. **2**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **2**A. FIG. **2**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **2**B. In comparison with the first embodiment of FIGS. **1**A~**1**C, the third conductive region **113** is not included in the electrostatic discharge protection structure of this embodiment. In a case where the breakdown voltage of the parasitic bipolar junction transistor does not need to be adjusted, the electrostatic discharge protection structure of this embodiment is feasible. The other components of the electrostatic discharge protection structure of the second embodiment are similar to those of the first embodiment, and are not redundantly described herein.

FIG. **3**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a third embodiment of the present invention. FIG. **3**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **3**A. FIG. **3**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **3**B. In comparison with FIGS. **1**A~**1**C, the electrostatic discharge protection structure of this embodiment further comprises a fourth conductive region **114**. The fourth conductive region **114** is formed in the surface of the semiconductor substrate **10**. In addition, a sidewall of the fourth conductive region **114** is enclosed by the second well region **102**. The fourth conductive region **114** contains the first type conducting carriers (e.g. hole carriers). In addition, the concentration of the first type conducting carriers of the fourth conductive region **114** is higher than the concentration of the first type conducting carriers of the first well region **101**. In this embodiment, the drain contact region of the electrostatic discharge protection structure is divided into a first drain contact region **11101** and a second drain contact region **11102**. The first drain contact region **11101** is disposed

on a surface of the first conductive region **111**. The second drain contact region **11102** is disposed on a surface of the fourth conductive region **114**. The other components of the electrostatic discharge protection structure of the third embodiment are similar to those of the above embodiments, and are not redundantly described herein.

FIG. **4**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a fourth embodiment of the present invention. FIG. **4**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **4**A. FIG. **4**C is a schematic top view illustrating a variation of the electrostatic discharge protection structure of FIG. **4**B. In comparison with the third embodiment of FIGS. **3**A~**3**C, the third conductive region **113** is not included in the electrostatic discharge protection structure of this embodiment. In a case where the breakdown voltage of the parasitic bipolar junction transistor does not need to be adjusted, the electrostatic discharge protection structure of this embodiment is thus feasible. The other components of the electrostatic discharge protection structure of the fourth embodiment are similar to those of the above embodiments, and are not redundantly described herein.

FIG. **5**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a fifth embodiment of the present invention. FIG. **5**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **5**A. In comparison with the third embodiment of FIGS. **3**A~**3**B, the profile of the second well region **102** of the electrostatic discharge protection structure of this embodiment is distinguished. Consequently, the fourth conductive region **114** is separated from the deep well region **103** by the first well region **101**. By the electrostatic discharge protection structure of this embodiment, the drawbacks of causing the low holding voltage from the snapback breakdown condition of the parasitic bipolar junction transistor can be also effectively solved. The other components of the electrostatic discharge protection structure of the fourth embodiment are similar to those of the above embodiments, and are not redundantly described herein.

FIG. **6**A is a schematic cross-sectional view illustrating an electrostatic discharge protection structure according to a sixth embodiment of the present invention. FIG. **6**B is a schematic top view illustrating the electrostatic discharge protection structure of FIG. **6**A. In comparison with the fifth embodiment of FIGS. **5**A~**5**B, the third conductive region **113** is not included in the electrostatic discharge protection structure of this embodiment. In a case where the breakdown voltage of the parasitic bipolar junction transistor does not need to be adjusted, the electrostatic discharge protection structure of this embodiment is feasible. The other components of the electrostatic discharge protection structure of the sixth embodiment are similar to those of the above embodiments, and are not redundantly described herein.

From the above descriptions, the present invention provides an electrostatic discharge protection structure. In the electrostatic discharge protection structure of the present invention, the combination of the second well region **102** and the deep well region **103** provides an additional current path for discharging the electrostatic discharge current. Consequently, the drawbacks of causing the low holding voltage from the snapback breakdown condition of the parasitic bipolar junction transistor can be solved.

FIG. **7** schematically illustrates the relationships between the voltage and the current of a conventional electrostatic discharge protection structure and of the electrostatic discharge protection structure of the first embodiment of the present invention. As shown in FIG. **7**, the conventional electrostatic discharge protection structure has a characteristic curve A, and the present electrostatic discharge protection structure has a characteristic curve B. As shown in the characteristic curve B, the holding voltage of the present electrostatic discharge protection structure in the snapback breakdown condition is maintained at a specified voltage.

In the above embodiments, the semiconductor substrate **10** used in the electrostatic discharge protection structure of the present invention is a silicon substrate, a germanium substrate or a compound semiconductor substrate.

While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. An electrostatic discharge protection structure, comprising:

a semiconductor substrate;

a first well region disposed in the semiconductor substrate, and containing first type conducting carriers;

a gate structure disposed over a surface of the first well region;

a second well region disposed within the first well region, and located at a first side of the gate structure, wherein the second well region contains second type conducting carriers;

a first conductive region disposed on the surface of the first well region, and arranged between the gate structure and the second well region, wherein the first conductive region contains the second type conducting carriers;

a second conductive region disposed on the surface of the first well region, and located at a second side of the gate structure, wherein the second conductive region contains the second type conducting carriers;

a deep well region disposed under the second well region and the first conductive region, and contacted with the second well region, wherein the deep well region is separated from the first conductive region by the first well region, wherein the deep well region contains the second type conducting carriers; and

a third conductive region arranged between the second well region, the first conductive region and the deep well region, wherein the third conductive region is contacted with a bottom surface of the first conductive region.

2. The electrostatic discharge protection structure according to claim **1**, wherein the concentration of the second type conducting carriers of the deep well region is lower than the concentration of the second type conducting carriers of the second well region.

3. The electrostatic discharge protection structure according to claim **1**, wherein the concentration of the second type conducting carriers of the second well region is lower than the concentration of the second type conducting carriers of the first conductive region, and the concentration of the second type conducting carriers of the second well region is lower than the concentration of the second type conducting carriers of the second conductive region.

4. The electrostatic discharge protection structure according to claim **1**, wherein the third conductive region contains the first type conducting carriers, and the concentration of the first type conducting carriers of the third conductive region is

higher than the concentration of the first type conducting carriers of the first well region.

5. The electrostatic discharge protection structure according to claim **4**, wherein the third conductive region is separated from the deep well region by the first well region.

6. The electrostatic discharge protection structure according to claim **1**, wherein the first well region, the gate structure, the first conductive region and the second conductive region are defined as a metal-oxide-semiconductor structure, wherein the first conductive region is used as a drain region of the metal-oxide-semiconductor structure, and the second conductive region is used as a source region of the metal-oxide-semiconductor structure.

7. The electrostatic discharge protection structure according to claim **6**, wherein a top surface of the second well region is contacted with the first conductive region.

8. The electrostatic discharge protection structure according to claim **6**, further comprising a drain contact region, wherein the drain contact region is disposed on a surface of the first conductive region, and the entire second well region is covered by a projection area of the drain contact region.

9. The electrostatic discharge protection structure according to claim **1**, further comprising a fourth conductive region, wherein the fourth conductive region is formed in a surface of the semiconductor substrate, and a sidewall of the fourth conductive region is enclosed by the second well region, wherein the fourth conductive region contain the first type conducting carriers, and the concentration of the first type conducting carriers of the fourth conductive region is higher than the concentration of the first type conducting carriers of the first well region.

10. The electrostatic discharge protection structure according to claim **9**, further comprising a first drain contact region and a second drain contact region, wherein the first drain contact region is disposed on a surface of the first conductive region, and the second drain contact region is disposed on a surface of the fourth conductive region.

11. The electrostatic discharge protection structure according to claim **9**, wherein the fourth conductive region is separated from the deep well region by the first well region.

12. The electrostatic discharge protection structure according to claim **1**, further comprising a gate contact region and a source contact region, wherein the gate contact region is disposed on a surface of the gate structure, and the source contact region is disposed on a surface of the second conductive region.

13. The electrostatic discharge protection structure according to claim **1**, further comprising a fifth conductive region and a body contact region, wherein the fifth conductive region is disposed within the first well region, and the body contact region is formed on a surface of the fifth conductive region, wherein the fifth conductive region contains the first type conducting carriers, and the concentration of the first type conducting carriers of the fifth conductive region is higher than the concentration of the first type conducting carriers of the first well region.

14. The electrostatic discharge protection structure according to claim **1**, wherein the first conductive region is wider than the second conductive region.

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