US008836114B2

(12) **United States Patent**
Oh et al.

(10) **Patent No.: US 8,836,114 B2**
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(54) **SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP HAVING CONDUCTIVE LAYERS AND CONDUCTIVE VIAS SEPARATED BY POLYMER LAYERS**

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(73) Assignee: **STATS ChipPAC, Ltd.**, Singapore (SG)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **13/679,792**

(22) Filed: **Nov. 16, 2012**

(65) **Prior Publication Data**

US 2013/0075919 A1 Mar. 28, 2013

Related U.S. Application Data

(63) Continuation of application No. 12/857,362, filed on Aug. 16, 2010, now Pat. No. 8,343,810.

(51) **Int. Cl.**
H01L 23/52 (2006.01)
H05K 1/18 (2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ***H01L 23/5384*** (2013.01); *H05K 2201/0195* (2013.01); *H01L 2224/0345* (2013.01); *H01L 2924/12044* (2013.01); *H01L 2224/1145* (2013.01); *H01L 2224/25171* (2013.01); *H05K 2201/10674* (2013.01); *H01L 2924/01047* (2013.01); *H01L 2224/03464* (2013.01); *H01L 2224/45144* (2013.01); *H01L 2224/05639*

(Continued)

USPC **257/734**

(58) **Field of Classification Search**
CPC H01L 25/065
USPC 257/686, 777, 774, 737; 438/107, 122, 438/133
See application file for complete search history.

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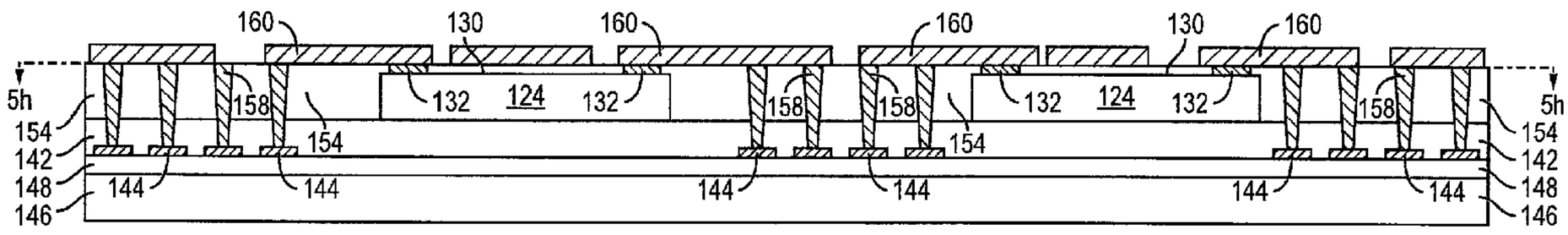
Primary Examiner — Nathan Ha
(74) *Attorney, Agent, or Firm* — Robert D. Atkins; Patent Law Group

(57) **ABSTRACT**

A Fo-WLCSP has a first polymer layer formed around a semiconductor die. First conductive vias are formed through the first polymer layer around a perimeter of the semiconductor die. A first interconnect structure is formed over a first surface of the first polymer layer and electrically connected to the first conductive vias. The first interconnect structure has a second polymer layer and a plurality of second vias formed through the second polymer layer. A second interconnect structure is formed over a second surface of the first polymer layer and electrically connected to the first conductive vias. The second interconnect structure has a third polymer layer and a plurality of third vias formed through the third polymer layer. A semiconductor package can be mounted to the WLCSP in a PoP arrangement. The semiconductor package is electrically connected to the WLCSP through the first interconnect structure or second interconnect structure.

31 Claims, 22 Drawing Sheets



(51) **Int. Cl.**

H01L 21/683	(2006.01)
H01L 23/538	(2006.01)
H01L 21/56	(2006.01)
H01L 21/50	(2006.01)
H05K 3/46	(2006.01)
H01L 21/768	(2006.01)
H01L 25/10	(2006.01)
H05K 3/00	(2006.01)
H01L 23/00	(2006.01)
H01L 23/31	(2006.01)
H01L 21/48	(2006.01)

(52) **U.S. Cl.**

CPC ..... (2013.01); *H05K 3/007* (2013.01); *H01L 24/48* (2013.01); *H01L 2224/03462* (2013.01); *H01L 2224/29144* (2013.01); ***H01L 24/25*** (2013.01); *H01L 2224/04042* (2013.01); *H01L 2924/01029* (2013.01); *H01L 2224/131* (2013.01); *H01L 2224/06131* (2013.01); *H01L 2224/05644* (2013.01); *H01L 2224/48599* (2013.01); *H01L 2224/73267* (2013.01); *H01L 2924/01073* (2013.01); ***H01L 24/97*** (2013.01); *H01L 2224/48105* (2013.01); ***H05K 1/186*** (2013.01); *H01L 2924/01322* (2013.01); *H01L 2224/97* (2013.01); *H01L 2224/215* (2013.01); *H01L 2224/13155* (2013.01); *H01L 2224/245* (2013.01); ***H01L 24/82*** (2013.01); *H01L 2224/48091* (2013.01); ***H01L 21/6835*** (2013.01); *H01L 2924/01082* (2013.01); *H01L 2224/48228* (2013.01); *H01L 2224/13124* (2013.01); ***H01L 24/24*** (2013.01); *H01L 2224/82005* (2013.01); *H01L 2224/05647* (2013.01); *H01L 2224/22* (2013.01); *H01L 24/13* (2013.01); *H01L 2224/48647* (2013.01); *H01L 2224/48624* (2013.01); *H01L 23/3107* (2013.01); ***H01L 21/561*** (2013.01); *H01L 2224/32225* (2013.01); *H01L 2224/05624* (2013.01); *H01L 2924/01049* (2013.01); *H01L 2225/1035* (2013.01); *H01L 2224/24105* (2013.01); *H01L 2224/13116* (2013.01); ***H01L 24/19*** (2013.01); ***H01L 23/3128*** (2013.01); *H01L 2924/12041* (2013.01); *H01L 2224/32145* (2013.01); *H01L 2224/2919* (2013.01); *H01L 2924/014* (2013.01); *H01L 2224/221* (2013.01); *H01L 2224/11464* (2013.01); *H01L 2924/15311* (2013.01); *H01L 2224/24011* (2013.01); *H01L 2224/13113* (2013.01); ***H01L 21/50*** (2013.01); *H01L 2224/05655* (2013.01); *H01L 2224/11901* (2013.01); ***H01L 24/20*** (2013.01); *H01L 2924/01074* (2013.01); *H01L 2224/73265* (2013.01); *H01L 24/29* (2013.01); *H01L 2224/11334* (2013.01); *H01L 2224/11849* (2013.01); *H01L 2924/13091* (2013.01); *H01L 2224/21* (2013.01); ***H05K 3/4608*** (2013.01); ***H01L 24/11*** (2013.01); *H01L 2224/2105* (2013.01); *H01L 24/03* (2013.01); ***H05K 3/4602*** (2013.01); *H01L 2224/05611* (2013.01); *H01L 2224/24226* (2013.01); *H01L 2224/48175* (2013.01); *H01L 2224/1132* (2013.01); *H01L 2221/68386* (2013.01); *H01L 2924/01079* (2013.01); *H01L 23/5389* (2013.01); *H01L 2221/68381* (2013.01); *H01L 2221/68359* (2013.01); *H01L 2924/09701* (2013.01); *H01L 2225/1041* (2013.01); *H01L 2221/68363* (2013.01); *H01L 2224/92244* (2013.01); *H01L 2224/13111* (2013.01); *H01L 2224/48227* (2013.01); *H01L 2221/68345* (2013.01); *H01L 2224/13144* (2013.01); *H01L 24/05* (2013.01); *H01L 224/95001* (2013.01); *H01L 2224/13147* (2013.01); *H01L 2224/11462* (2013.01); *H01L 2224/04105* (2013.01); *H01L 2224/2405* (2013.01); *H01L 2924/01013* (2013.01); *H01L 2225/1058* (2013.01); ***H01L 21/568*** (2013.01); *H01L 2224/16225* (2013.01); *H01L 2224/48644* (2013.01); *H01L 21/486* (2013.01); *H01L 2224/03452* (2013.01); ***H01L 21/768*** (2013.01); *H01L 2924/3011* (2013.01); *H01L 2224/13139* (2013.01); ***H01L 25/105*** (2013.01); *H01L 24/16* (2013.01); *H01L 24/32* (2013.01)

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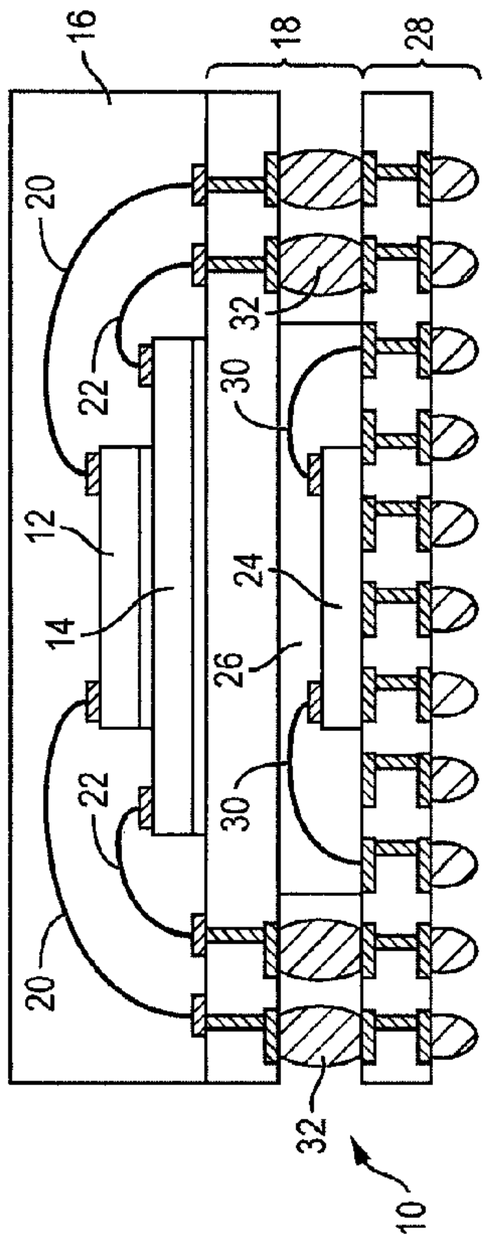

FIG. 1
(PRIOR ART)

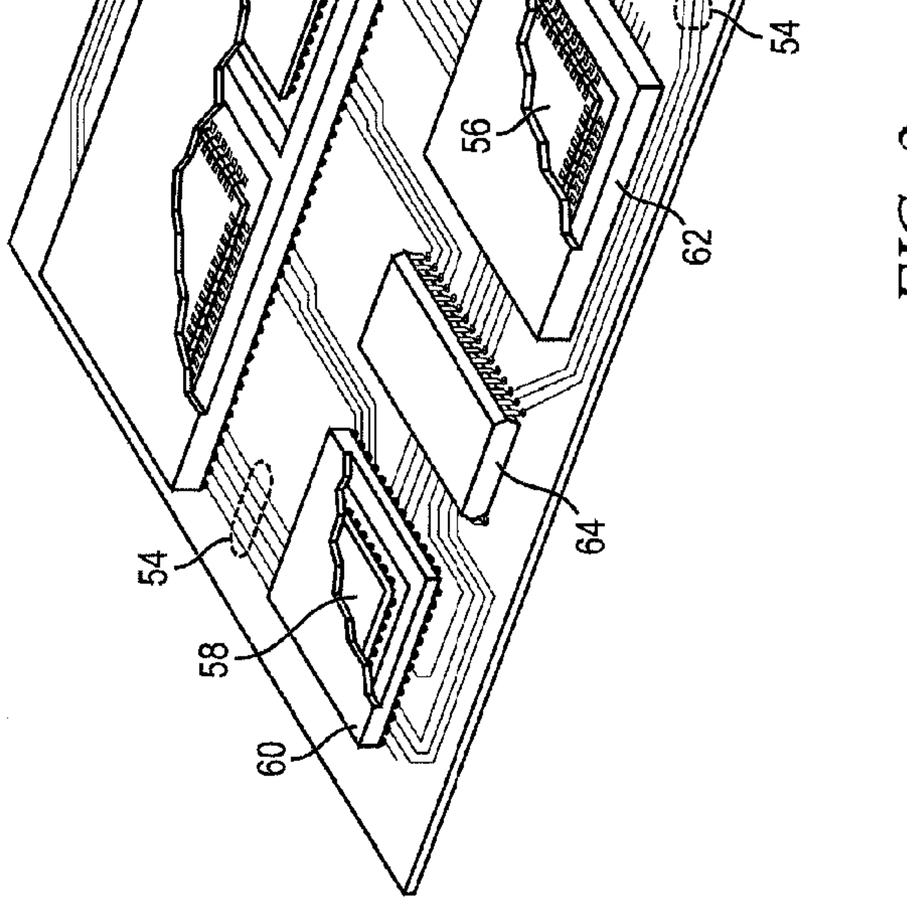

FIG. 2

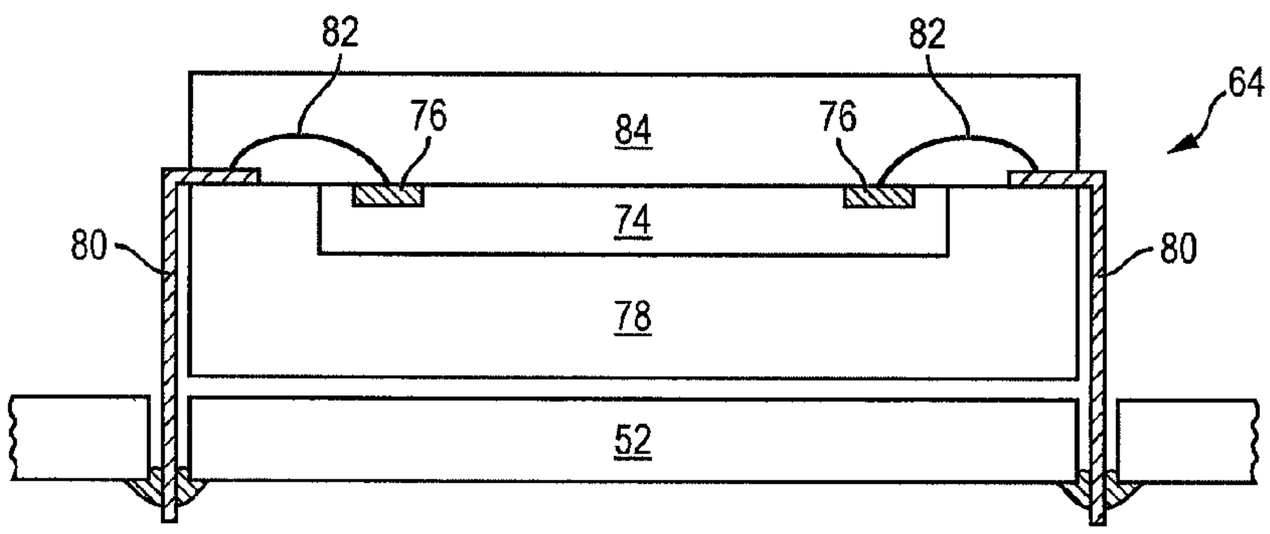

FIG. 3a

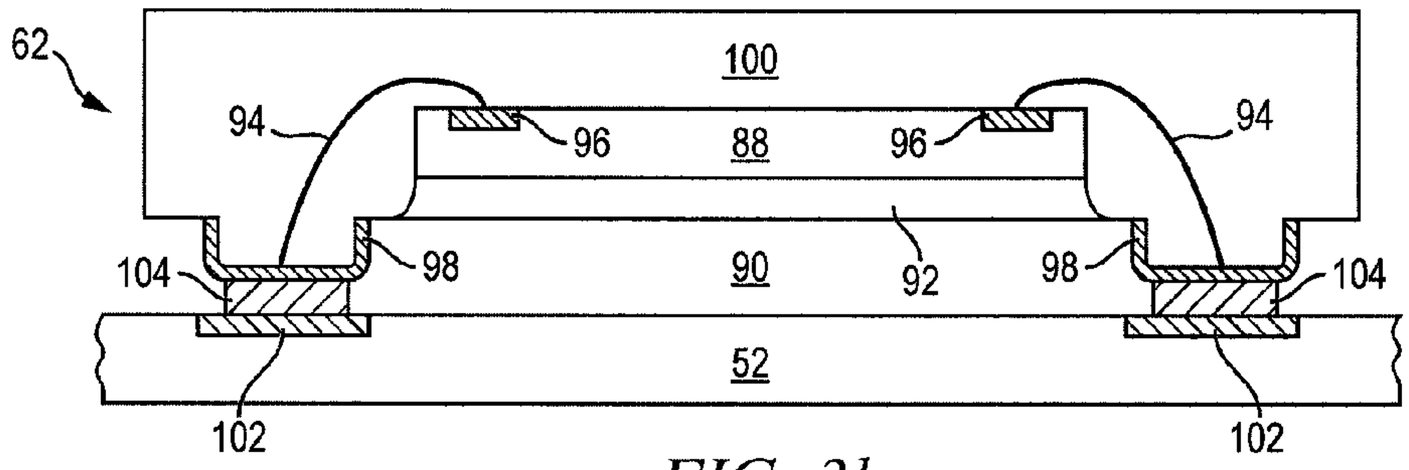

FIG. 3b

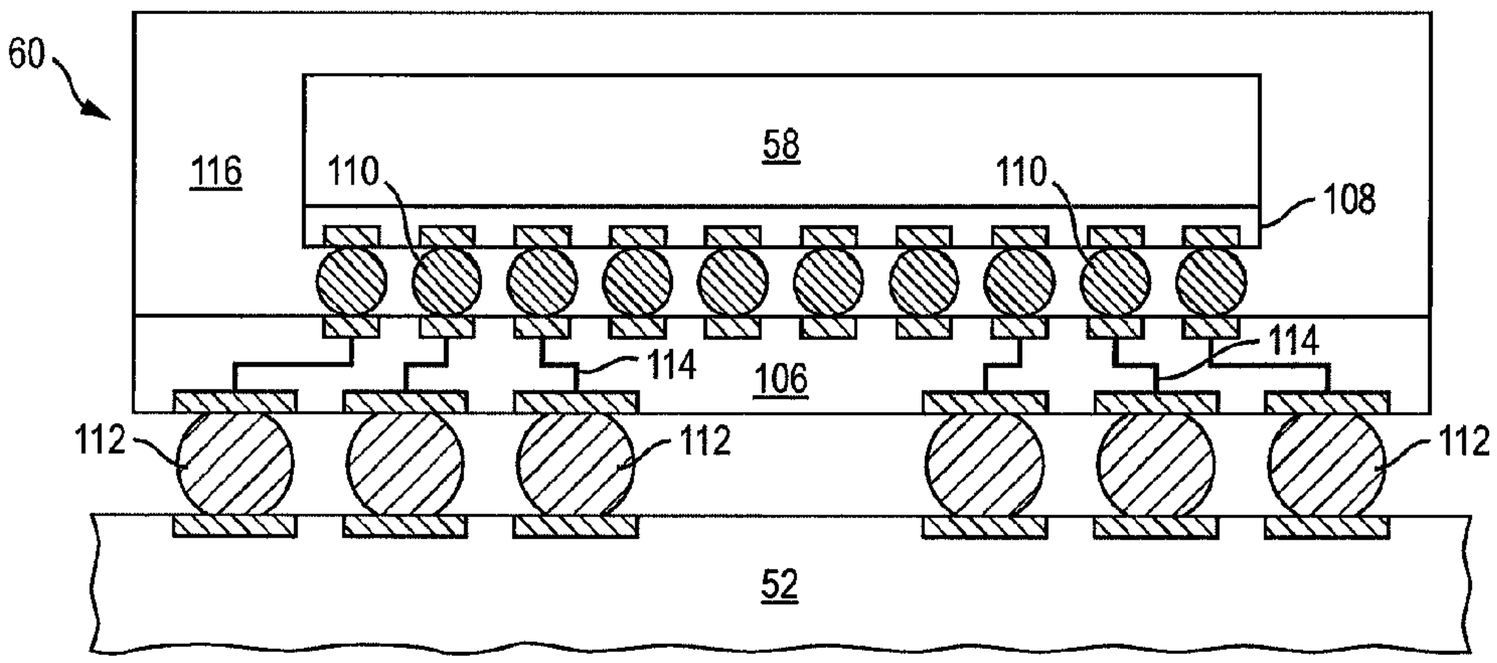

FIG. 3c

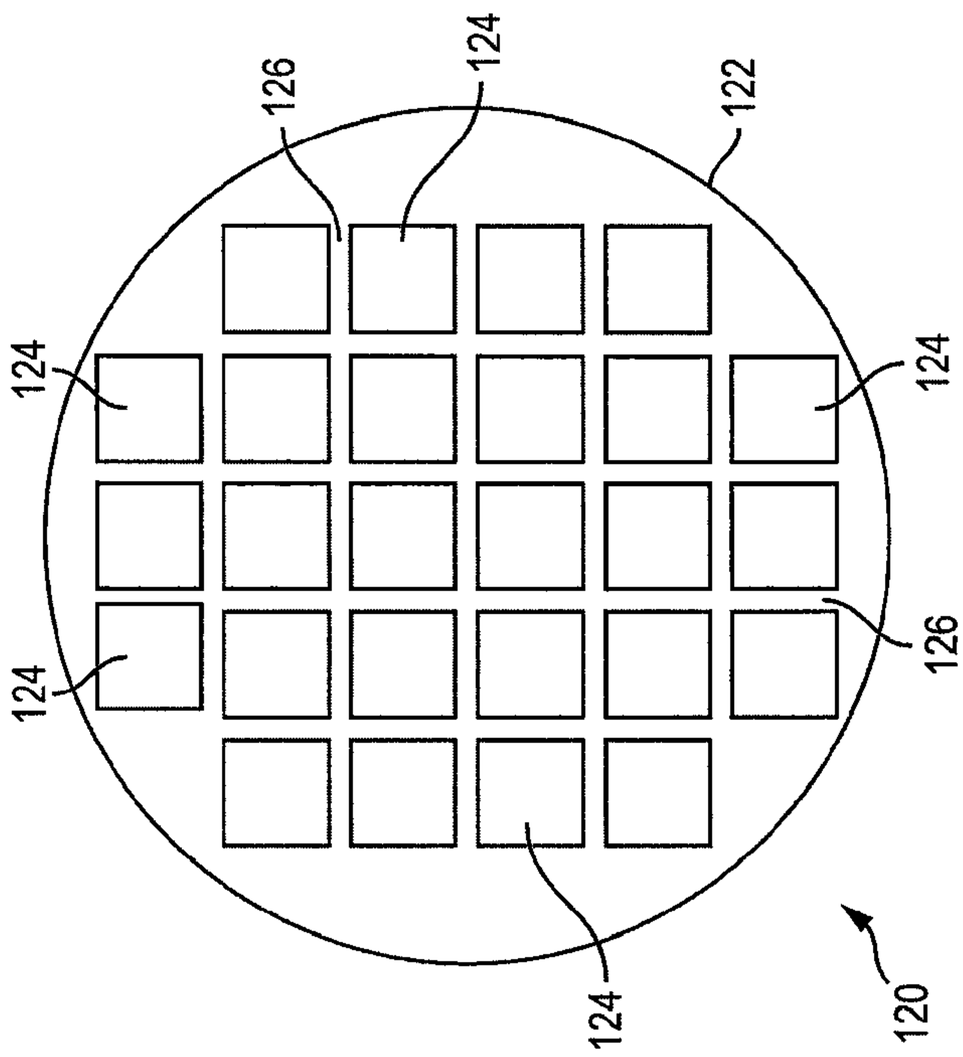
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FIG. 4a

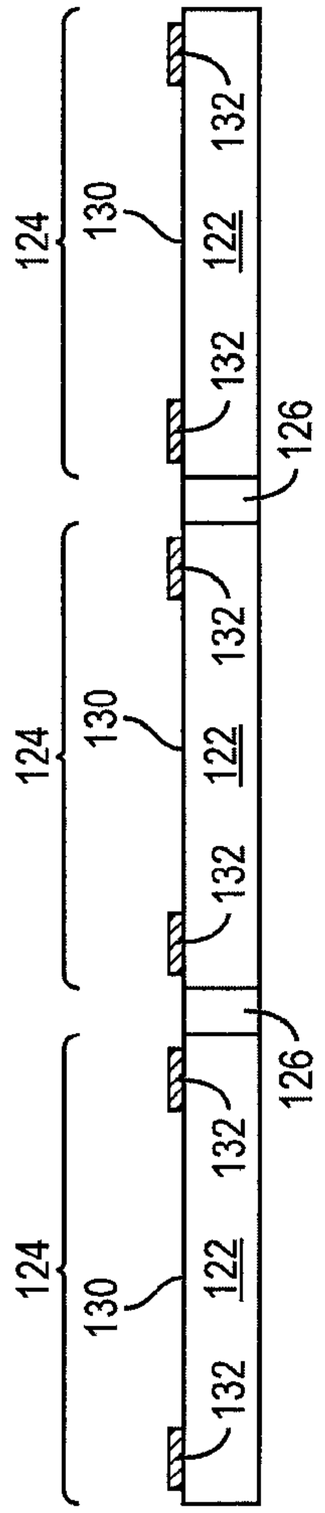
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FIG. 4b

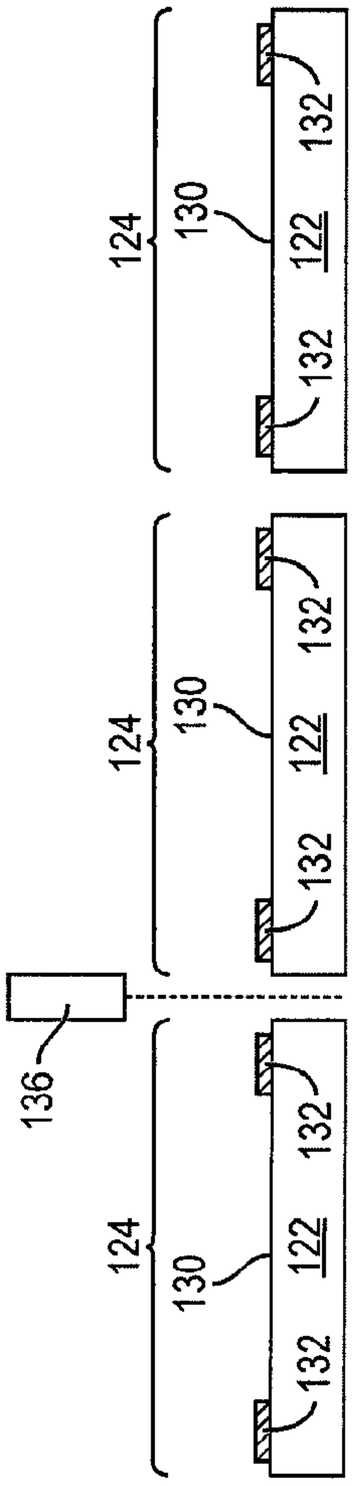

FIG. 4c

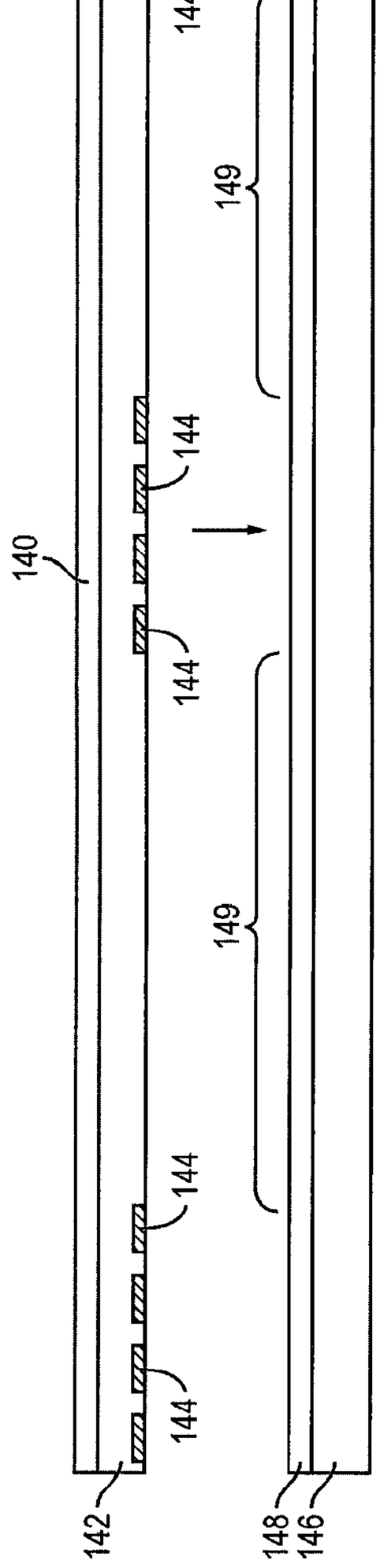

FIG. 5a

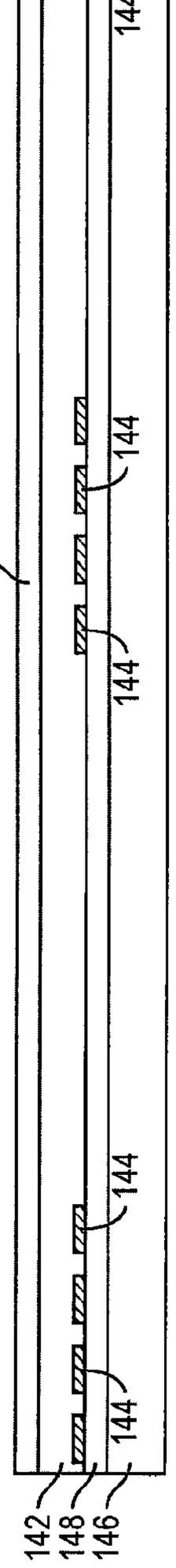

FIG. 5b

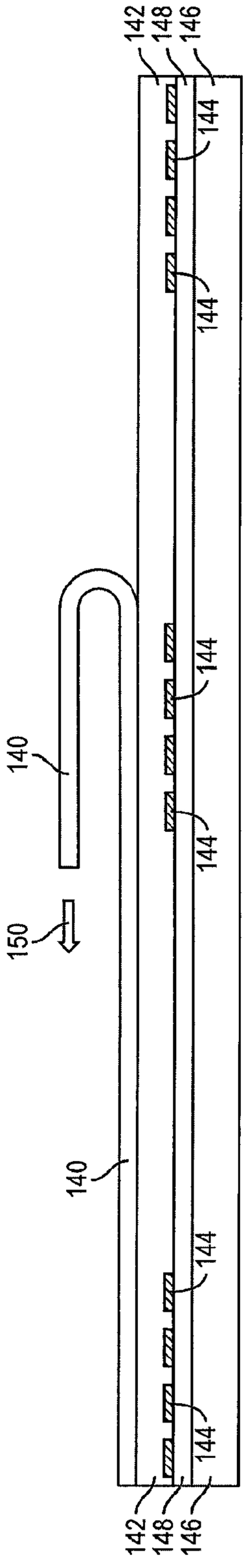

FIG. 5c

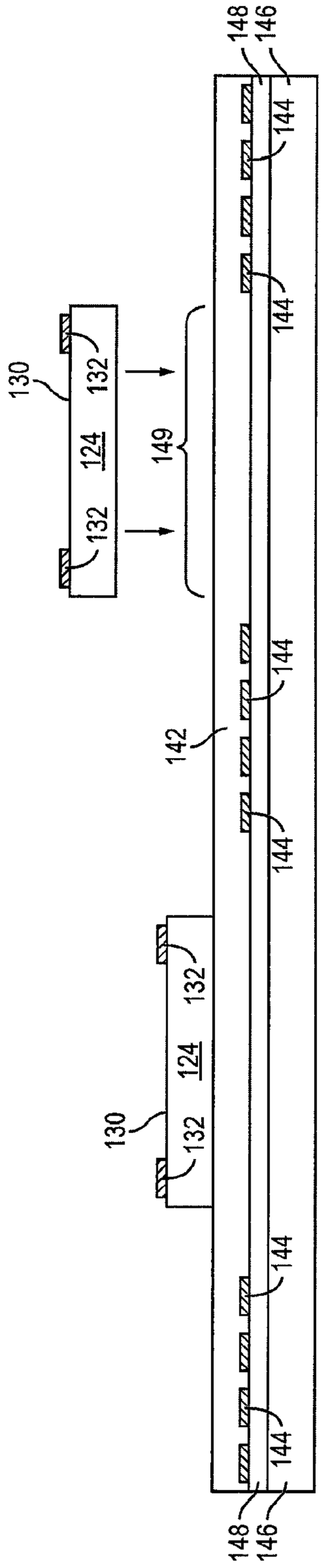

FIG. 5d

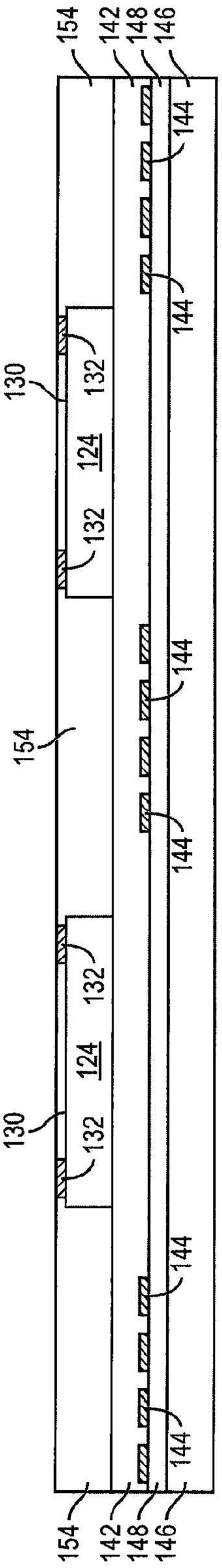

FIG. 5e

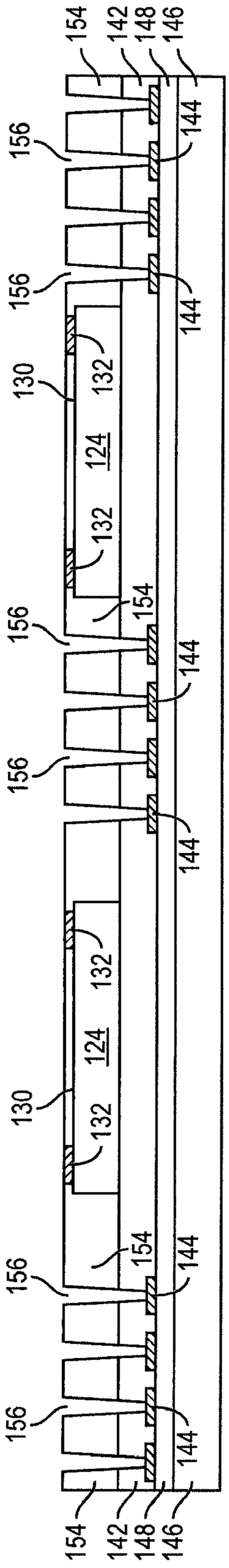
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FIG. 5f

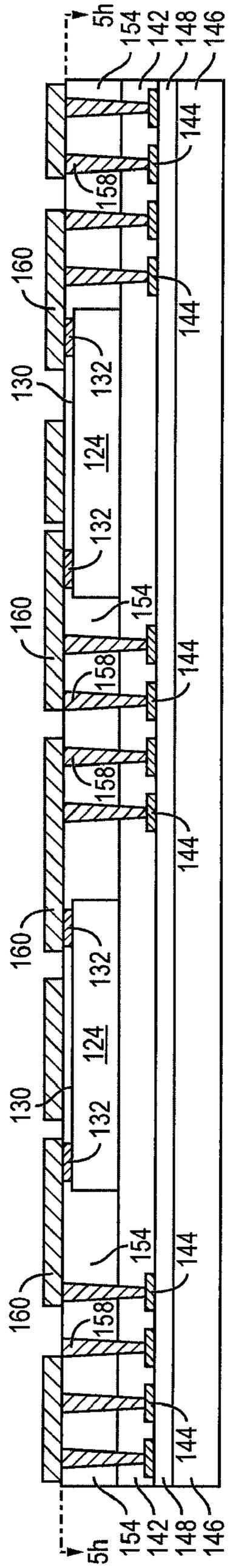
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FIG. 5g

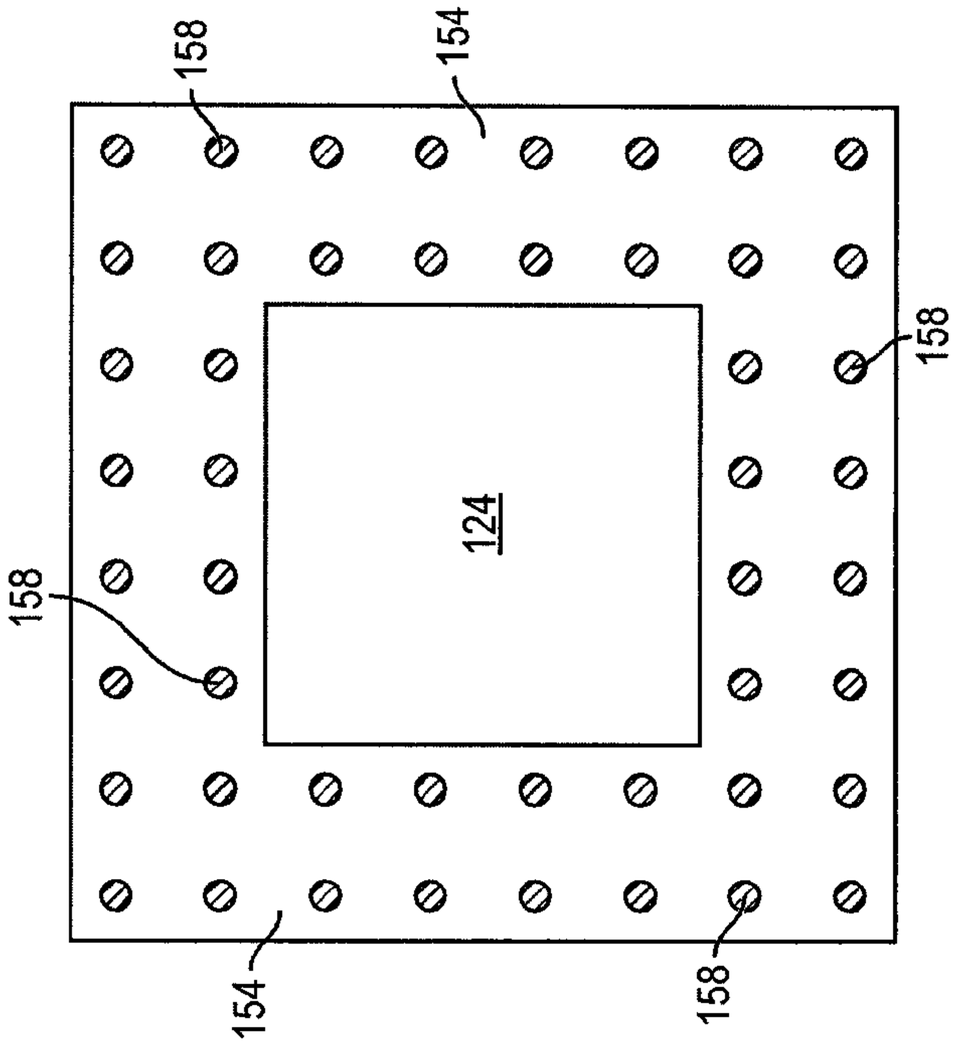
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FIG. 5h

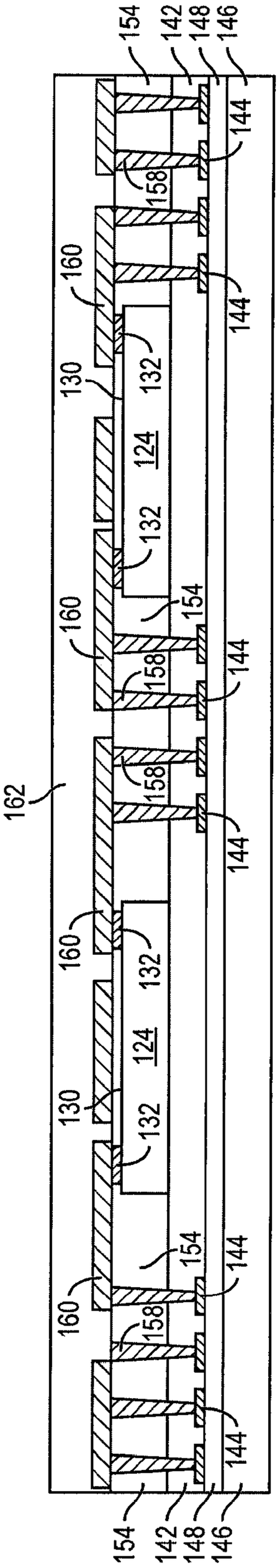
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FIG. 5i

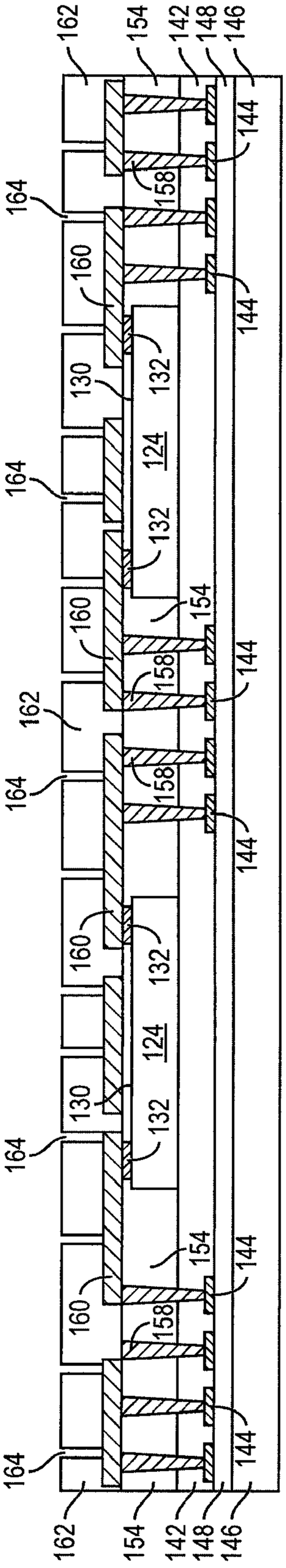
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FIG. 5j

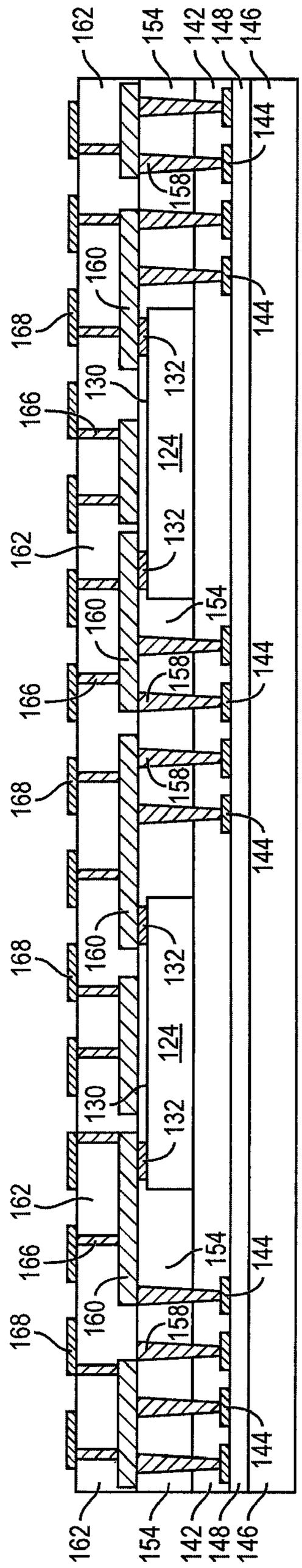
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FIG. 5k

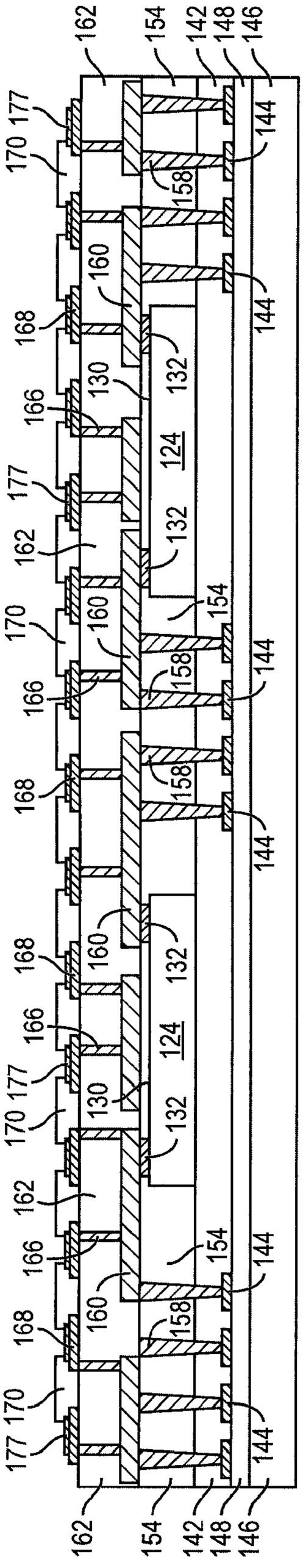
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FIG. 5l

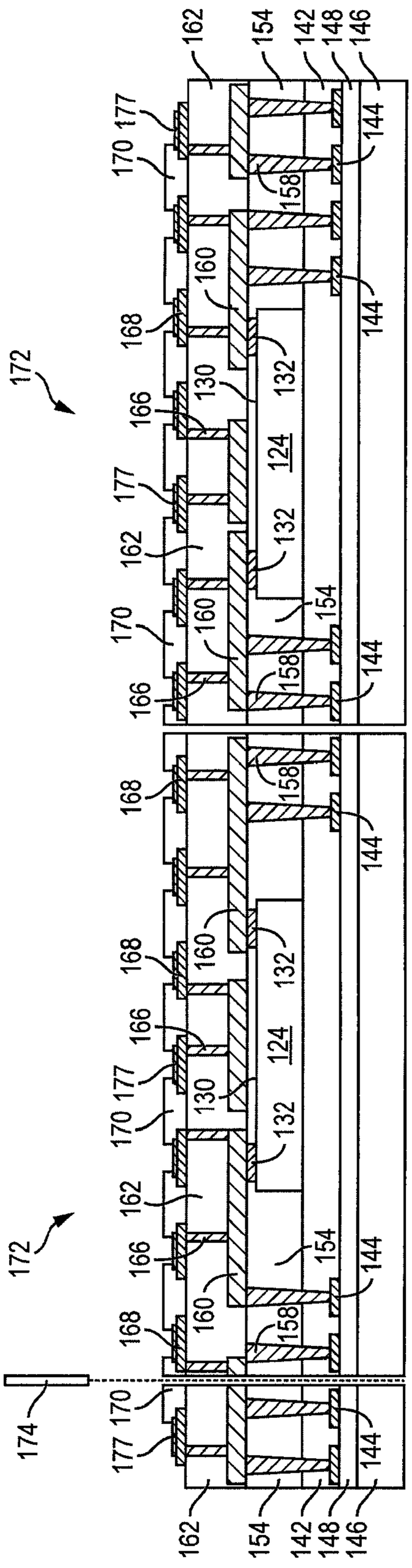
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FIG. 5m

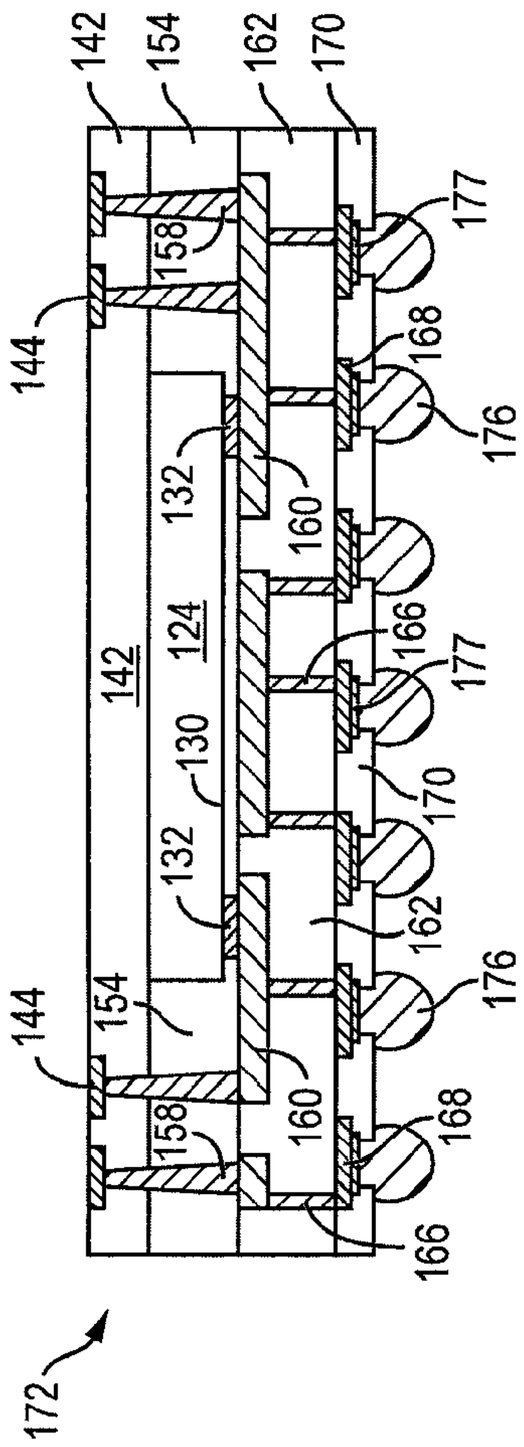
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FIG. 6a

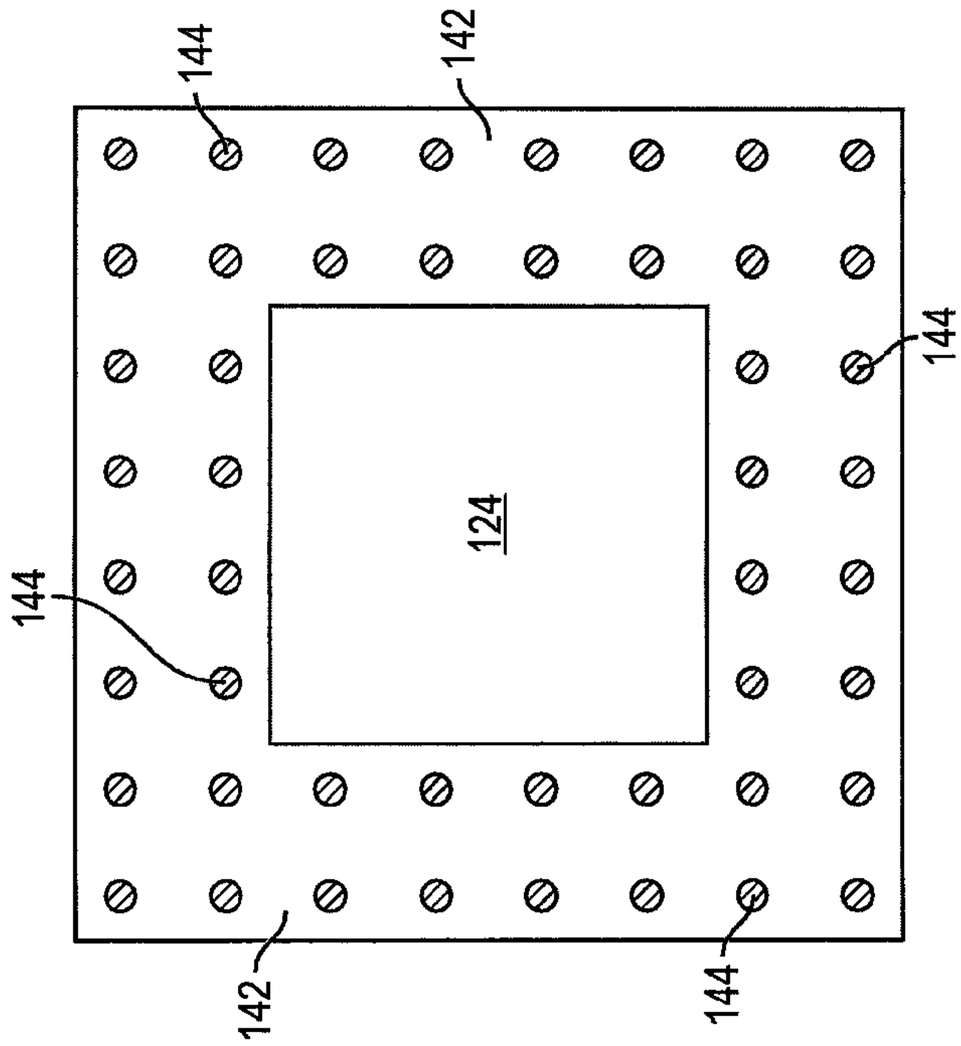
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FIG. 6b

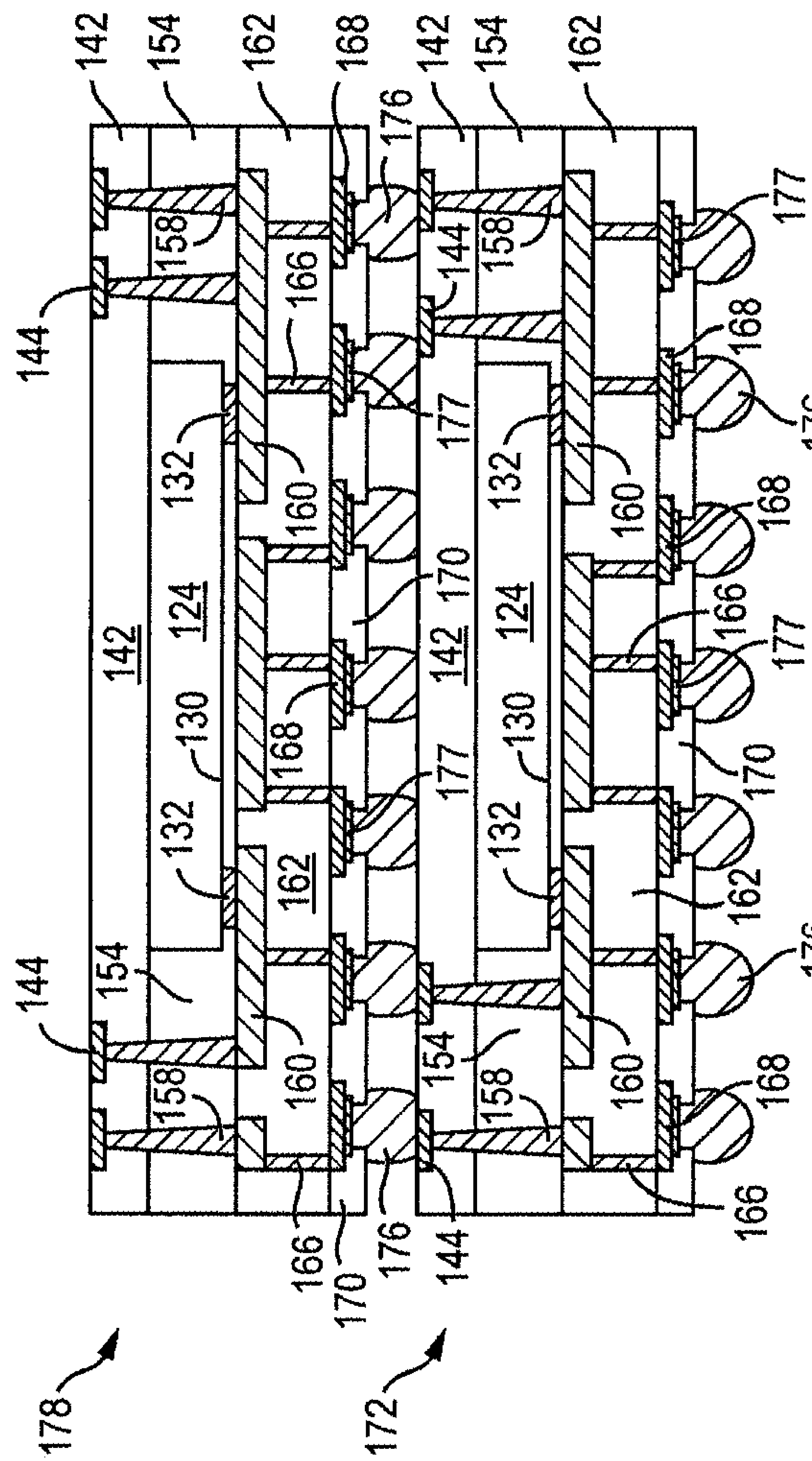
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FIG. 7

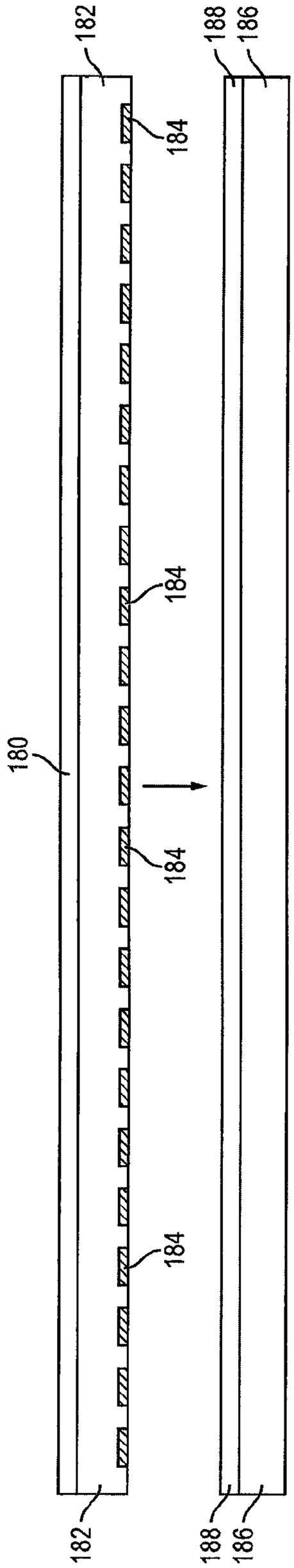

FIG. 8a

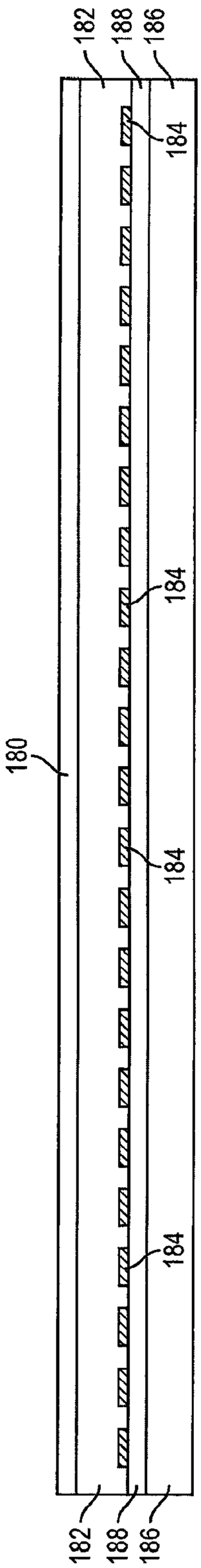

FIG. 8b

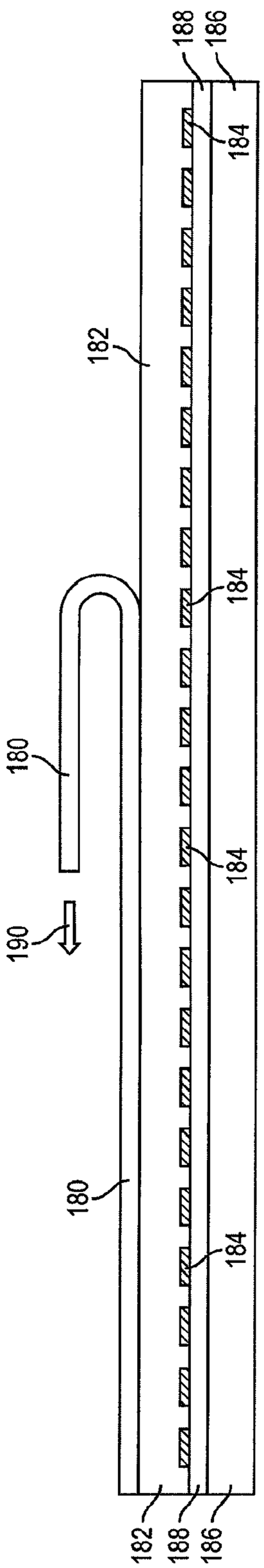

FIG. 8c

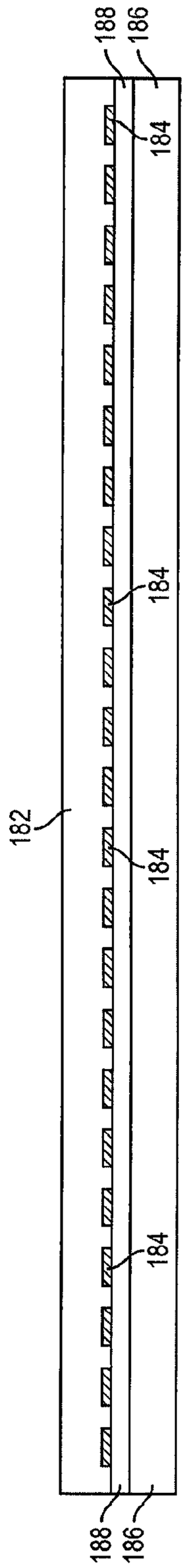

FIG. 8d

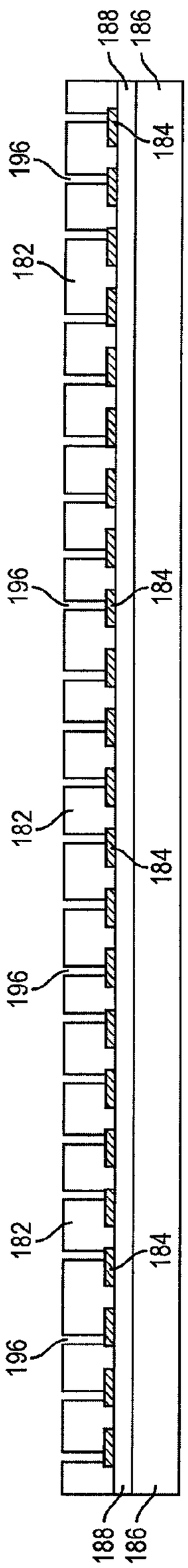

FIG. 8e

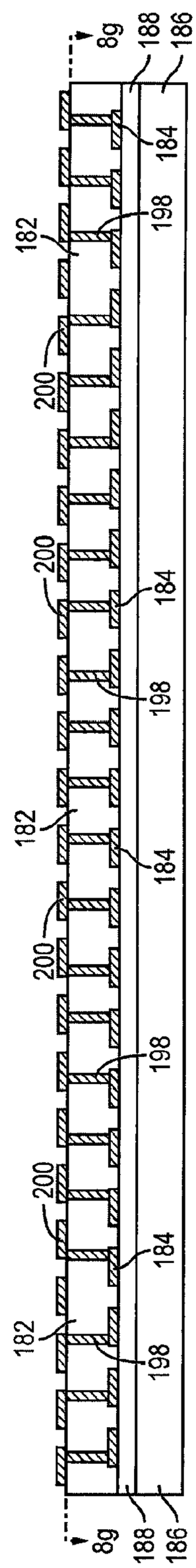

FIG. 8f

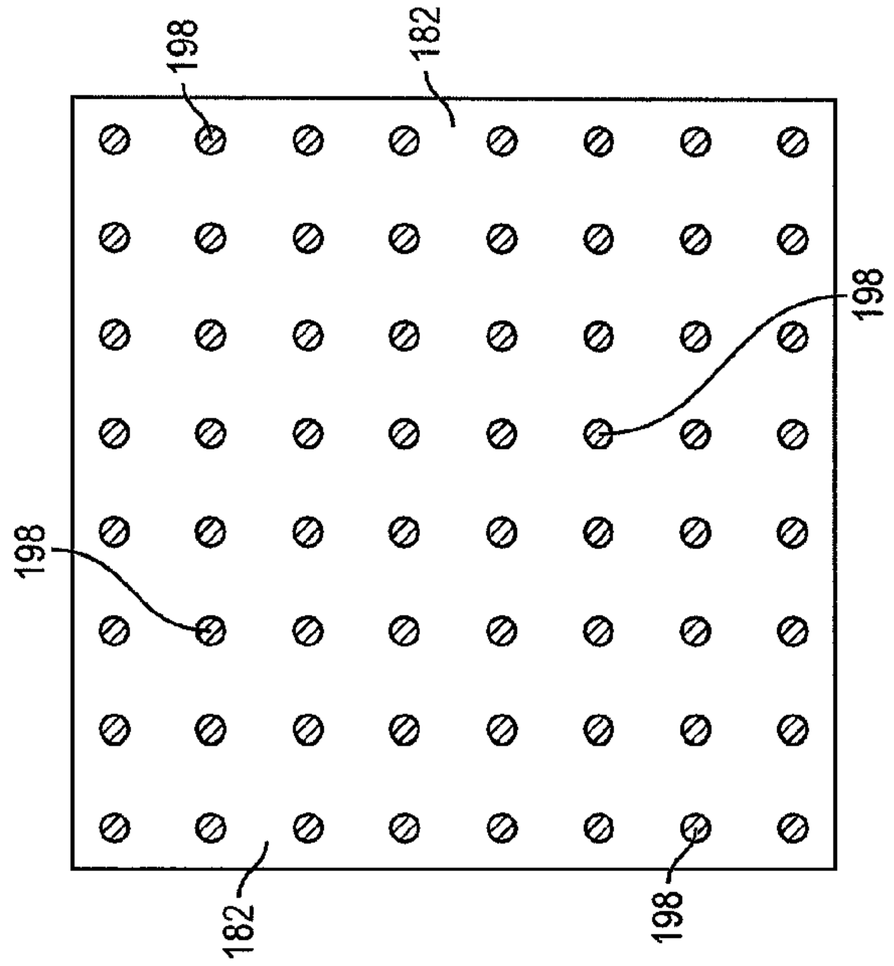

FIG. 8g

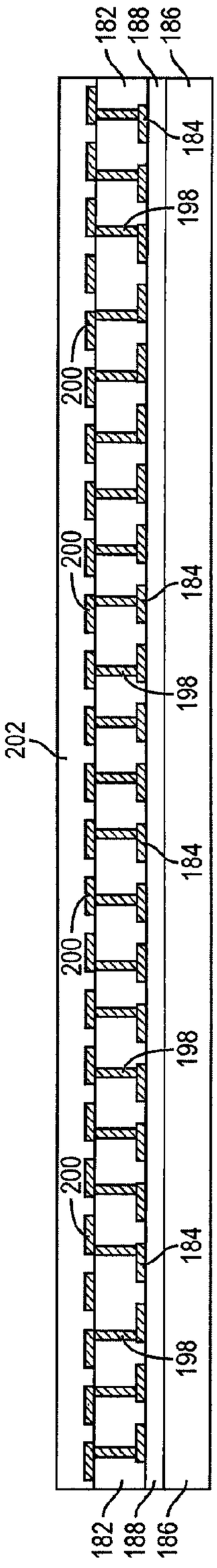

FIG. 8h

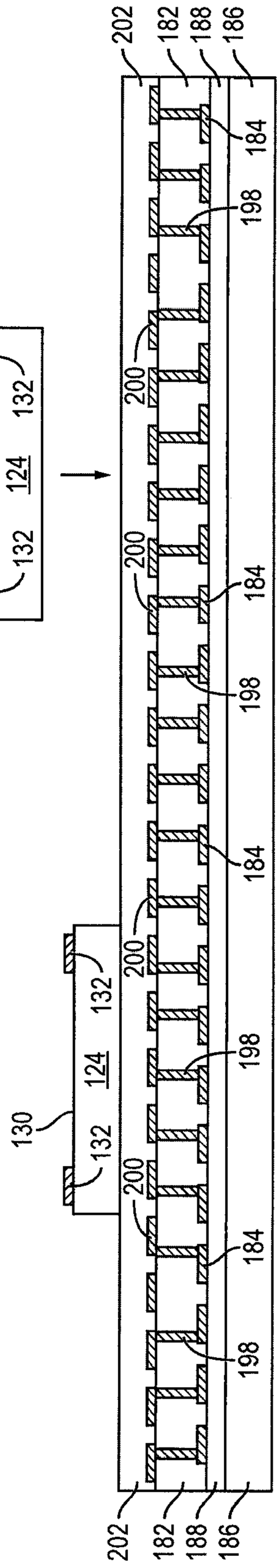
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FIG. 8i

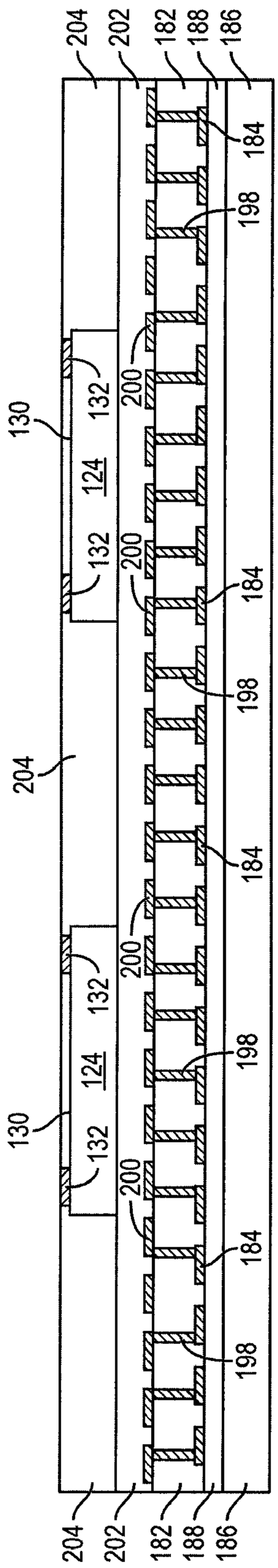
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FIG. 8j

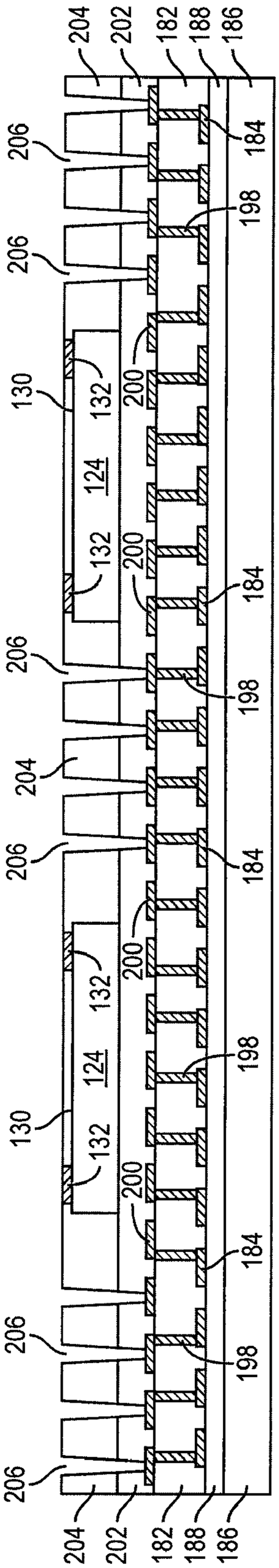
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FIG. 8k

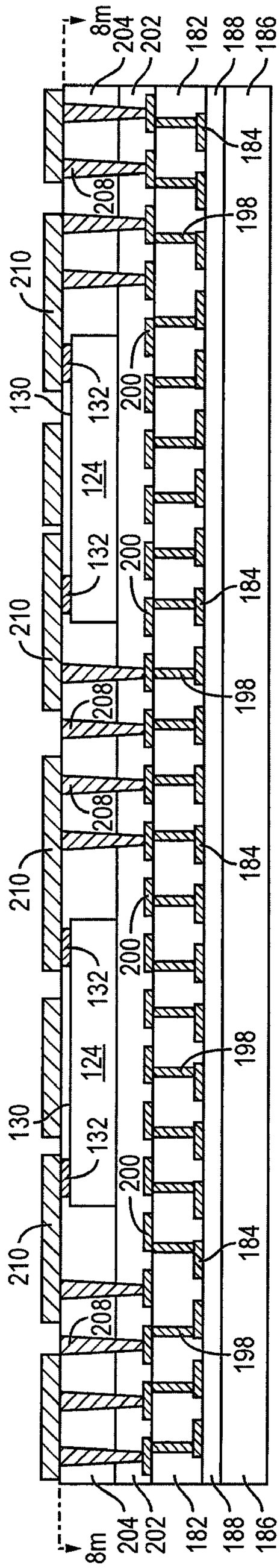
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FIG. 8l

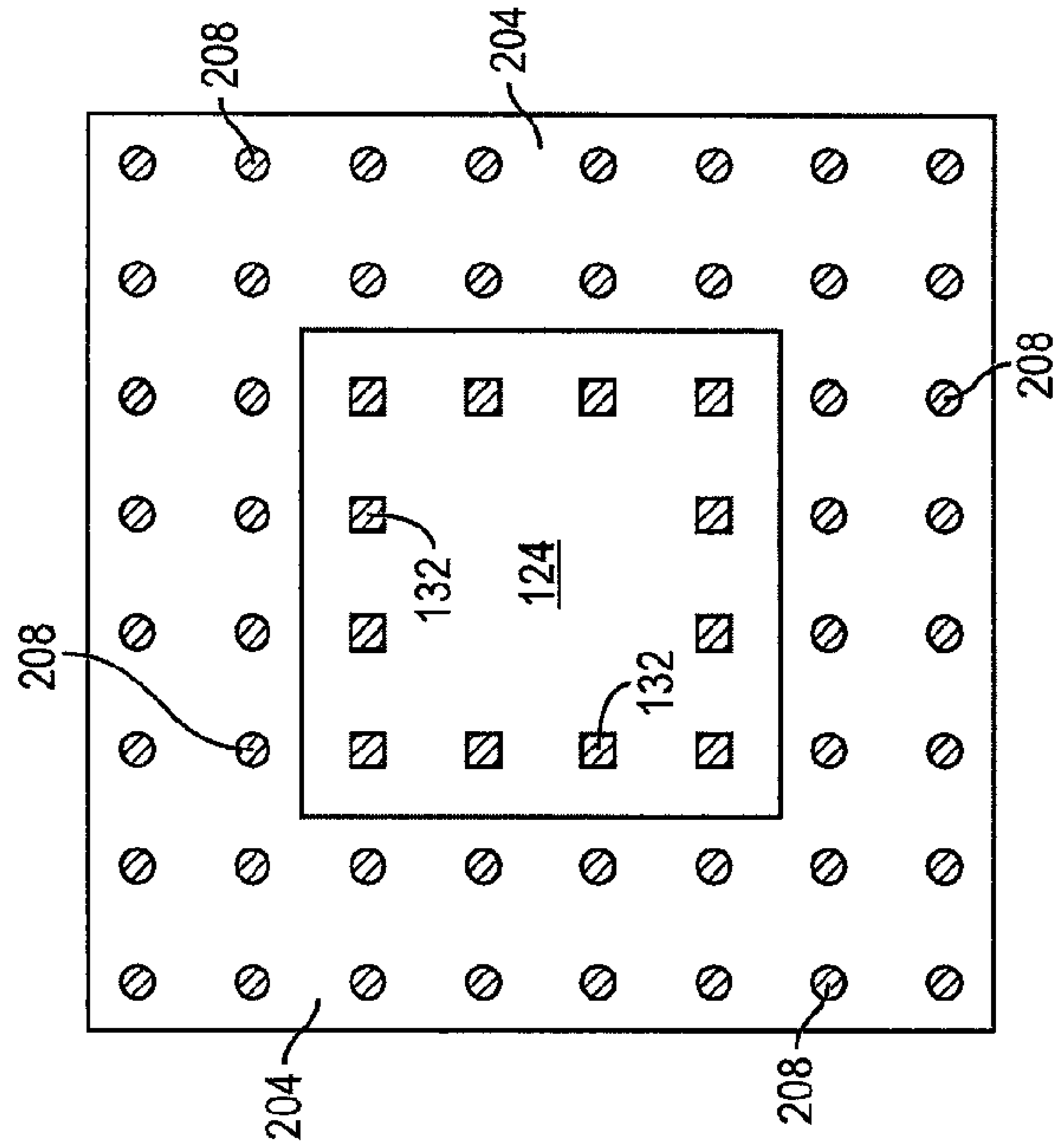
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FIG. 8m

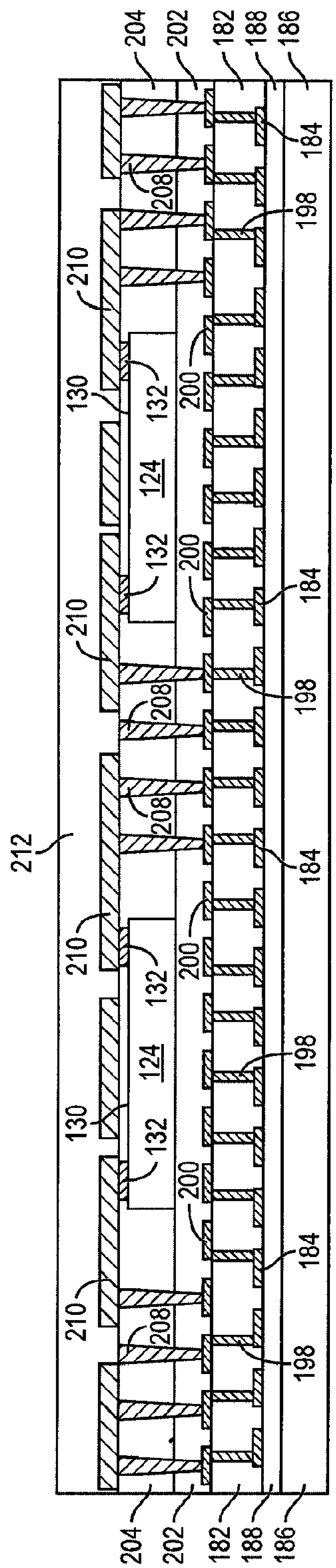
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FIG. 8n

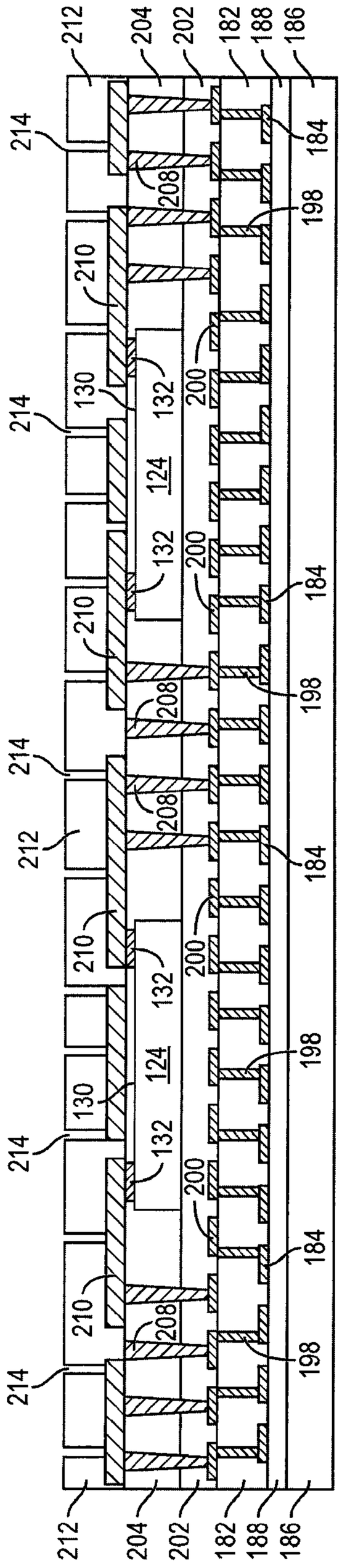
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FIG. 8o

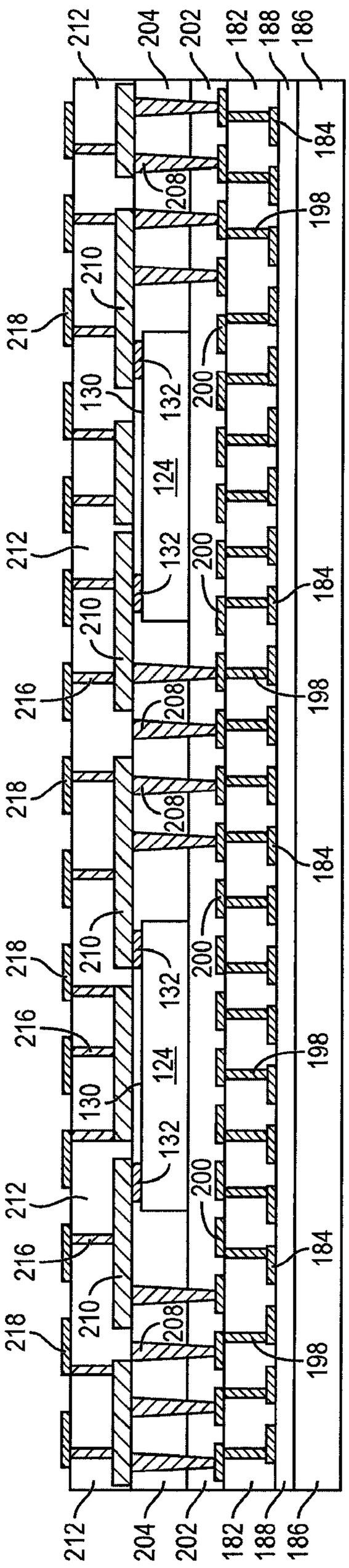
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FIG. 8p

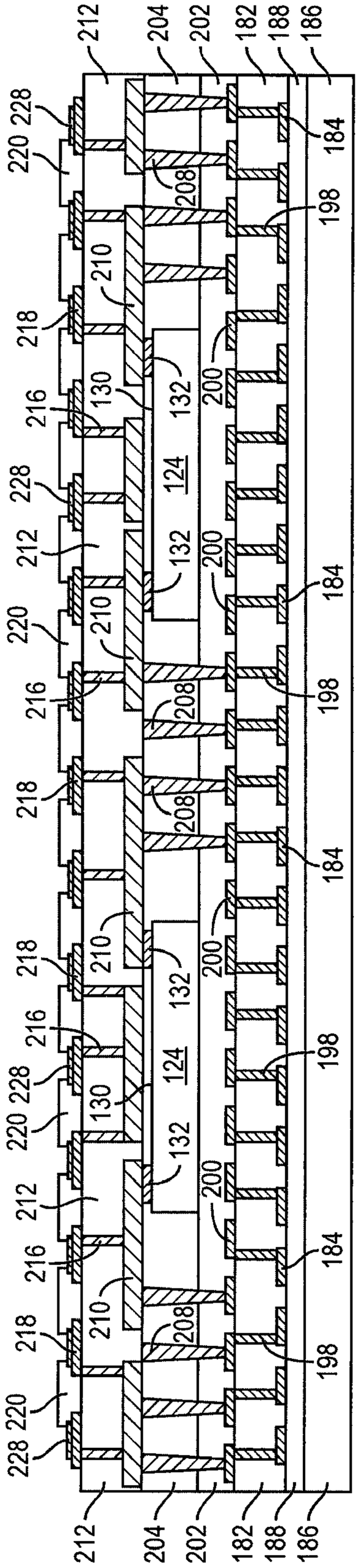
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FIG. 8q

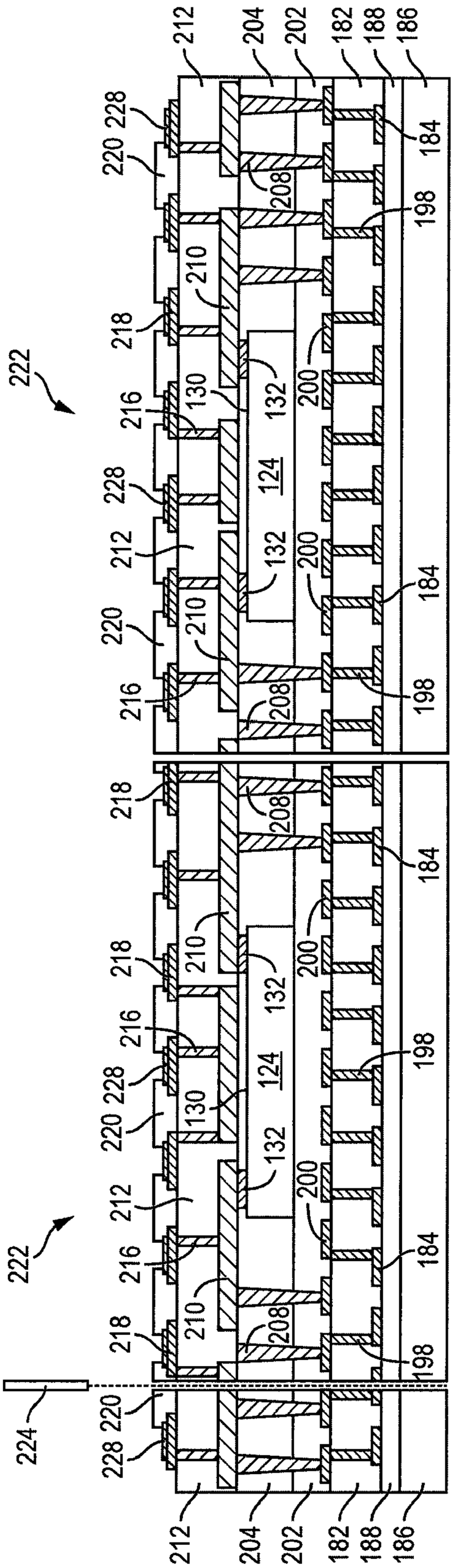
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FIG. 8r

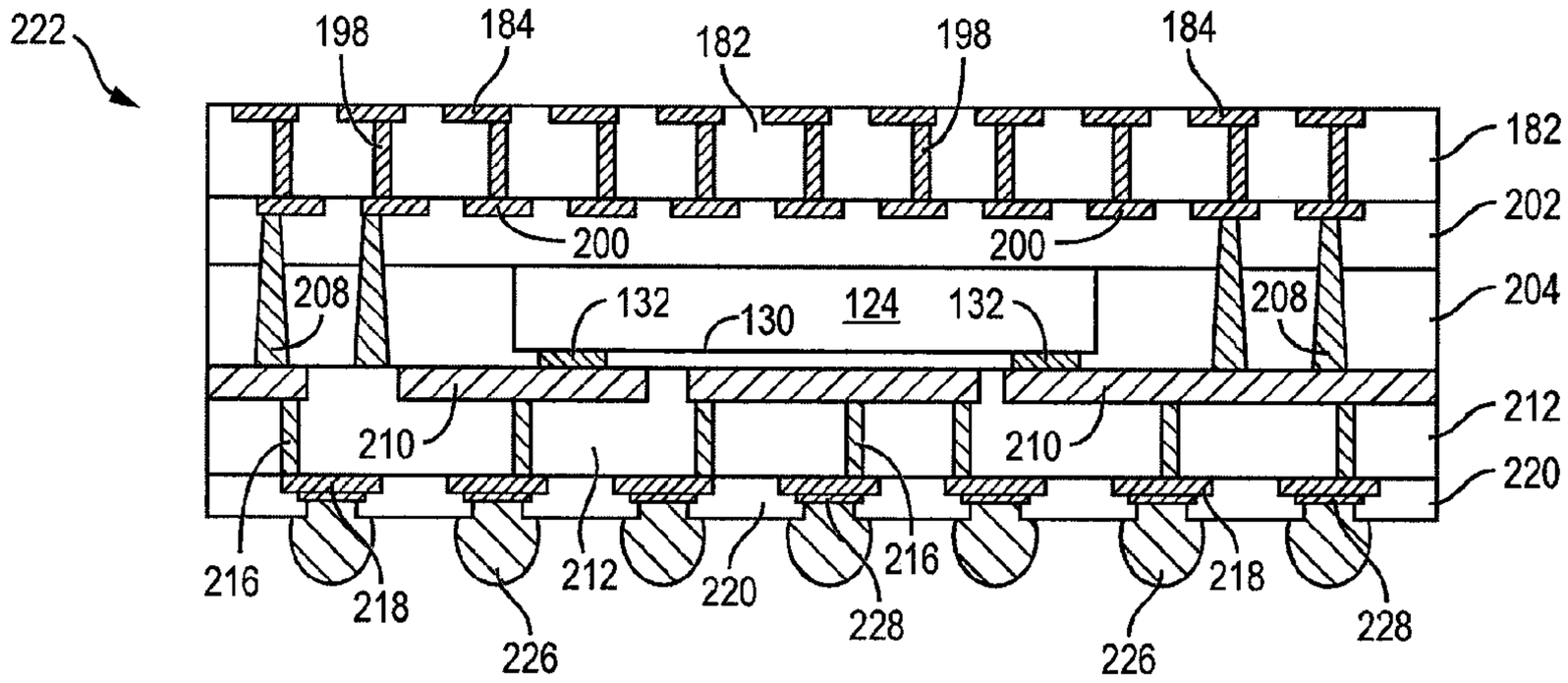
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FIG. 9

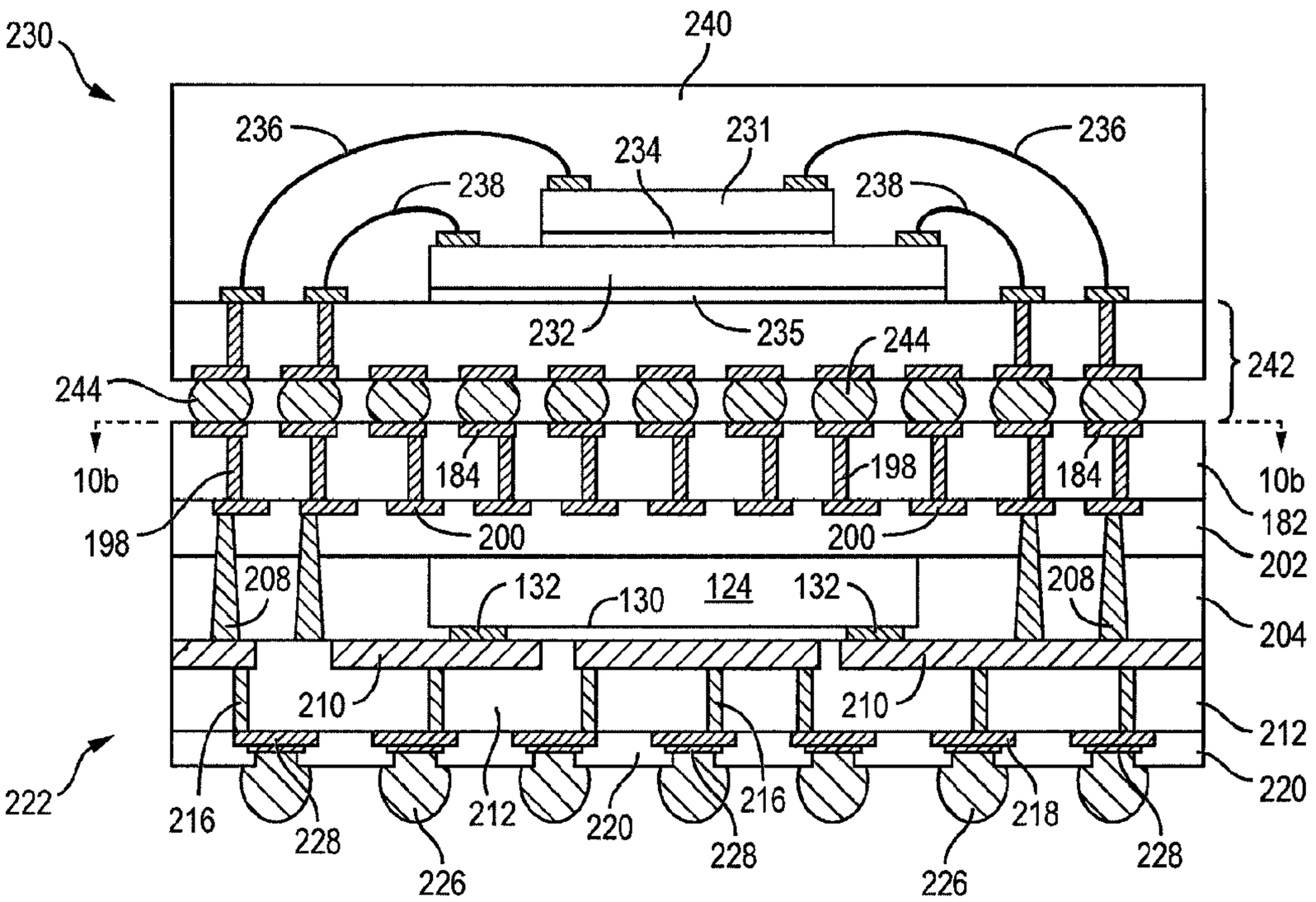
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FIG. 10a

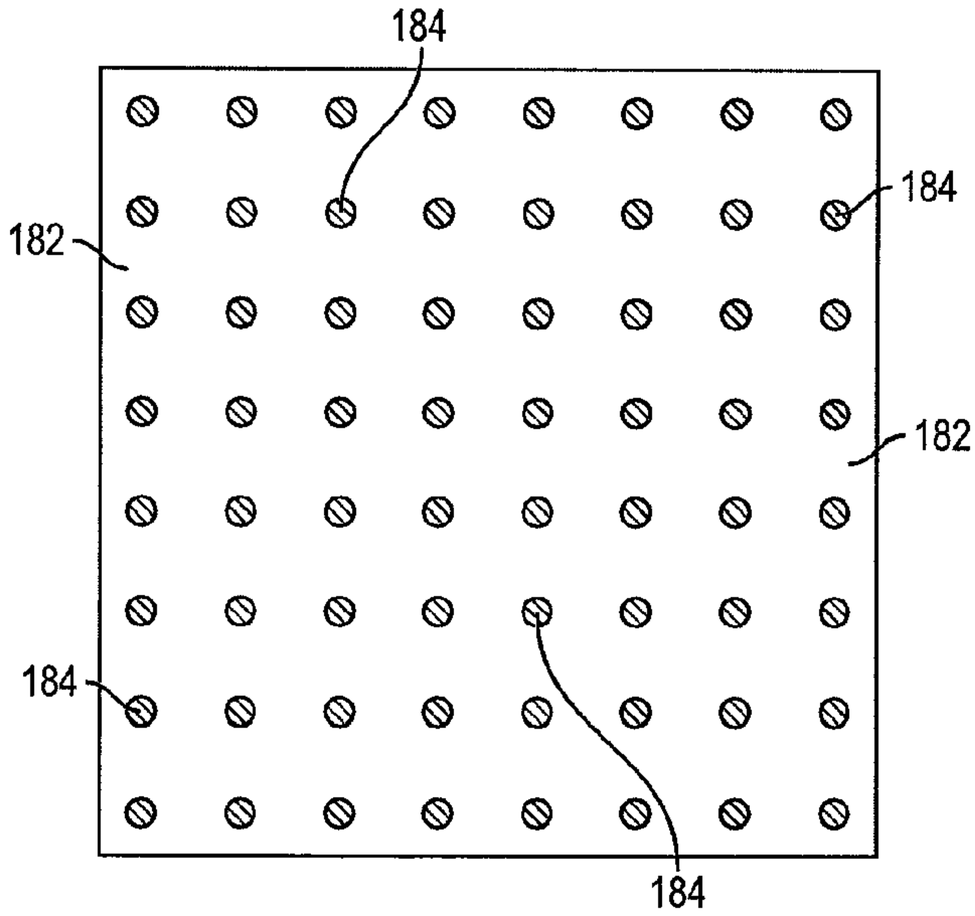

FIG. 10b

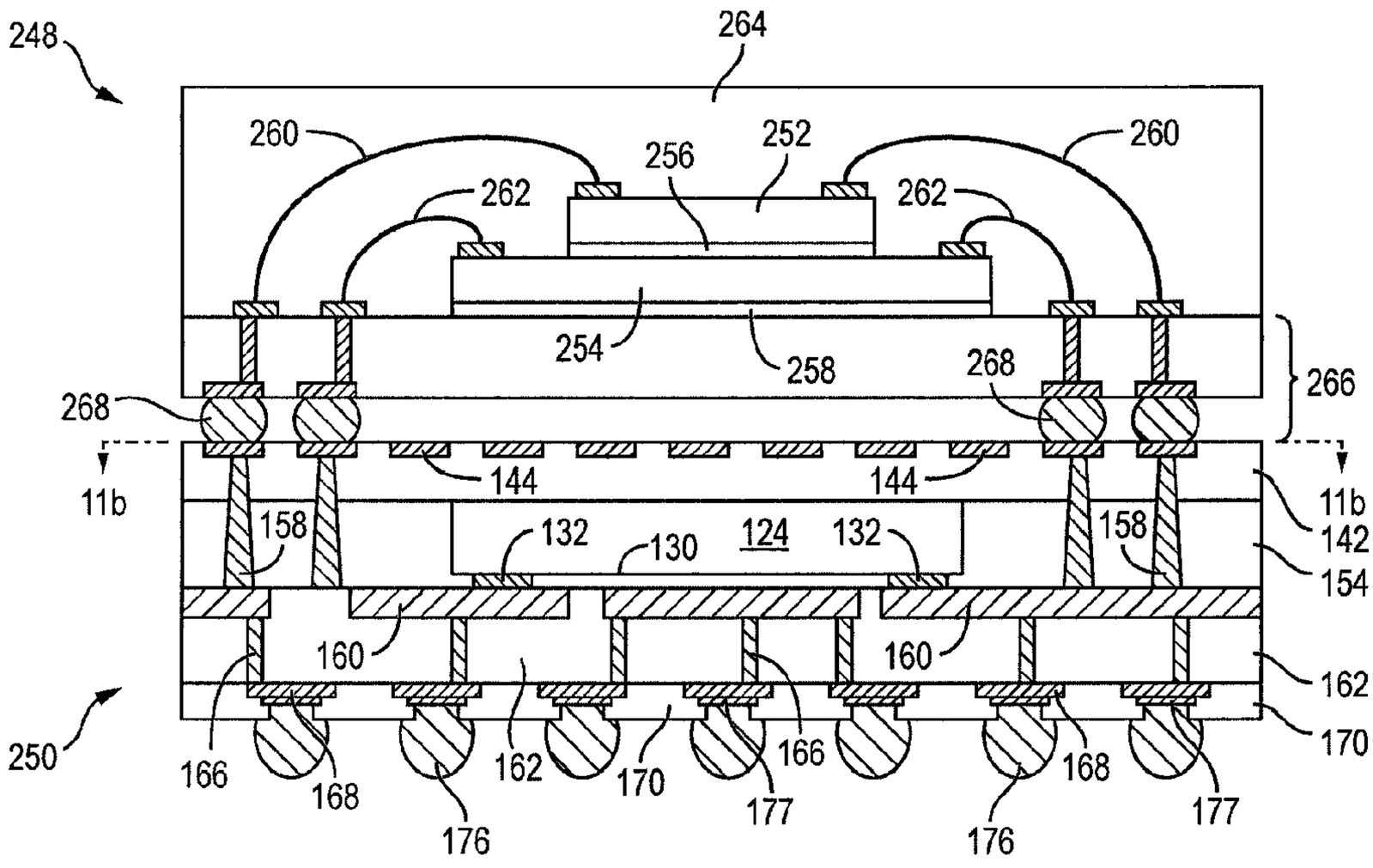

FIG. 11a

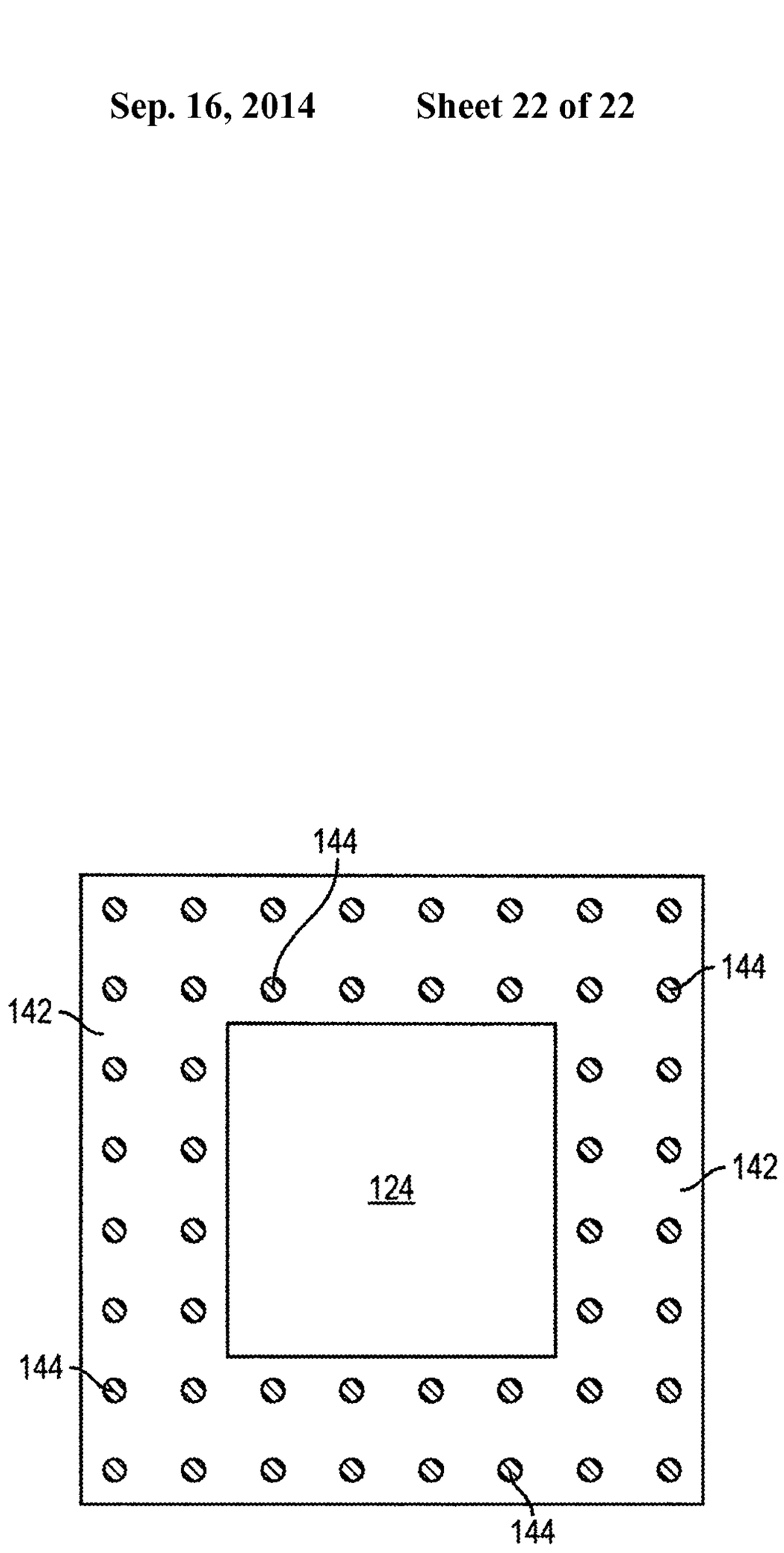

FIG. 11b

SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP HAVING CONDUCTIVE LAYERS AND CONDUCTIVE VIAS SEPARATED BY POLYMER LAYERS

CLAIM TO DOMESTIC PRIORITY

The present application is a continuation of U.S. patent application Ser. No. 12/857,362, now U.S. Pat. No. 8,343,810, filed Aug. 16, 2010, which application is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming fan-out wafer level chip scale package (Fo-WLCSP) having conductive layers and conductive vias separated by polymer layers.

BACKGROUND OF THE INVENTION

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The atomic structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed calculations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing

involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual die from the finished wafer and packaging the die to provide structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller die size may be achieved by improvements in the front-end process resulting in die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

FIG. **1** shows a conventional package-on-package (PoP) Fo-WLCSP **10** with semiconductor die **12** stacked over semiconductor die **14** and enclosed by encapsulant **16**. A build-up interconnect structure **18** is formed over the stacked semiconductor die **12-14** and encapsulant **16**. Semiconductor die **12** and **14** are electrically connected to interconnect structure **18** with bond wires **20** and **22**. Semiconductor die **24** is enclosed by encapsulant **26**. A build-up interconnect structure **28** is formed over semiconductor die **24** and encapsulant **26**. Semiconductor die **24** is electrically connected to interconnect structure **28** with bond wires **30**. The build-up interconnect structure **18** is electrically connected to build-up interconnect structure **28** using bumps **32** formed around a perimeter of semiconductor die **24** and encapsulant **26**.

The interconnect capability of Fo-WLCSP **10** is limited by the height requirement of encapsulant **26** formed around semiconductor die **24**. That is, bumps **32** must be formed with sufficient size to span the gap between build-up interconnect structures **18** and **28**. The gap is dictated by the height of encapsulant **26**. Accordingly, the height of encapsulant **26** restricts the bump arrangement options, bump pitch, bump size, and input/output (I/O) count.

SUMMARY OF THE INVENTION

A need exists to provide a Fo-WLCSP without using encapsulant around the semiconductor die to reduce bump pitch and bump size, as well as increase bump arrangement options and I/O count. Accordingly, in one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a first polymer layer, forming a first conductive layer over a first surface of the first polymer layer, disposing a first semiconductor die over a second surface of the first polymer layer opposite the first surface of the first polymer layer, forming a second polymer layer over the first polymer layer and first semiconductor die, forming a first conductive via through the first polymer layer and second polymer layer and electrically connected to the first conductive layer, and forming a third polymer layer over the second polymer layer.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a first polymer layer including a first conductive layer, disposing a first semiconductor die over a surface of the first polymer layer opposite the first conductive layer, forming a second polymer layer over the first polymer layer and first semiconductor die, and forming a first conductive via through the first polymer layer and second polymer layer and electrically connected to the first conductive layer.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a first polymer layer, disposing a first semiconductor die over the first polymer layer, forming a second polymer layer over the first polymer layer and first semiconductor die, and forming a first conductive via through the first polymer layer and second polymer layer.

In another embodiment, the present invention is a semiconductor device comprising a first polymer layer and first semiconductor die disposed over the first polymer layer. A second polymer layer is formed over the first polymer layer and first semiconductor die. A first conductive via is formed through the first polymer layer and second polymer layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a conventional PoP Fo-WLCSP with the semiconductor die enclosed by encapsulant;

FIG. **2** illustrates a PCB with different types of packages mounted to its surface;

FIGS. **3***a*-**3***c* illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGS. **4***a*-**4***c* illustrate a semiconductor wafer containing a plurality of semiconductor die;

FIGS. **5***a*-**5***m* illustrate a process of forming a Fo-WLCSP with conductive layers and conductive vias separated by polymer layers;

FIGS. **6***a*-**6***b* illustrate the Fo-WLCSP with conductive layers and conductive vias separated by polymer layers;

FIG. **7** illustrates a PoP arrangement of stacked Fo-WLCSP with conductive layers and conductive vias separated by polymer layers;

FIGS. **8***a*-**8***r* illustrate another process of forming a Fo-WLCSP with conductive layers and conductive vias separated by polymer layers;

FIG. **9** illustrates the Fo-WLCSP with conductive layers and conductive vias separated by polymer layers;

FIGS. **10***a*-**10***b* illustrate a PoP Fo-WLCSP formed in accordance with FIG. **9**; and

FIGS. **11***a*-**11***b* illustrate a PoP Fo-WLCSP formed in accordance with FIGS. **6***a*-**6***b*.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices, transforming the semiconductor material into an insulator, conductor, or dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition may involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

The layers can be patterned using photolithography, which involves the deposition of light sensitive material, e.g., photoresist, over the layer to be patterned. A pattern is transferred from a photomask to the photoresist using light. The portion of the photoresist pattern subjected to light is removed using a solvent, exposing portions of the underlying layer to be patterned. The remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive components. Planarization can be used to remove material from the surface of the wafer and produce a uniformly flat surface. Planarization involves polishing the surface of the wafer with a polishing pad. An abrasive material and corrosive chemical are added to the surface of the wafer during polishing. The combined mechanical action of the abrasive and corrosive action of the chemical removes any irregular topography, resulting in a uniformly flat surface.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and environmental isolation. To singulate the die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. **2** illustrates electronic device **50** having a chip carrier substrate or printed circuit board (PCB) **52** with a plurality of semiconductor packages mounted on its surface. Electronic

device **50** may have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. **2** for purposes of illustration.

Electronic device **50** may be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device **50** may be a subcomponent of a larger system. For example, electronic device **50** may be part of a cellular phone, personal digital assistant (PDA), digital video camera (DVC), or other electronic communication device. Alternatively, electronic device **50** can be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. The miniaturization and the weight reduction are essential for these products to be accepted by the market. The distance between semiconductor devices must be decreased to achieve higher density.

In FIG. **2**, PCB **52** provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces **54** are formed over a surface or within layers of PCB **52** using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces **54** provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces **54** also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including wire bond package **56** and flip chip **58**, are shown on PCB **52**. Additionally, several types of second level packaging, including ball grid array (BGA) **60**, bump chip carrier (BCC) **62**, dual in-line package (DIP) **64**, land grid array (LGA) **66**, multi-chip module (MCM) **68**, quad flat non-leaded package (QFN) **70**, and quad flat package **72**, are shown mounted on PCB **52**. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB **52**. In some embodiments, electronic device **50** includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using cheaper components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGS. **3***a*-**3***c* show exemplary semiconductor packages. FIG. **3***a* illustrates further detail of DIP **64** mounted on PCB **52**. Semiconductor die **74** includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active region of semiconductor die **74**. Contact pads **76** are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die **74**. During assembly of DIP **64**, semiconductor die **74** is mounted to an intermediate carrier **78** using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads **80** and wire bonds **82** provide electrical interconnect between semiconductor die **74** and PCB **52**. Encapsulant **84** is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating die **74** or wire bonds **82**.

FIG. **3***b* illustrates further detail of BCC **62** mounted on PCB **52**. Semiconductor die **88** is mounted over carrier **90** using an underfill or epoxy-resin adhesive material **92**. Wire bonds **94** provide first level packaging interconnect between contact pads **96** and **98**. Molding compound or encapsulant **100** is deposited over semiconductor die **88** and wire bonds **94** to provide physical support and electrical isolation for the device. Contact pads **102** are formed over a surface of PCB **52** using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads **102** are electrically connected to one or more conductive signal traces **54** in PCB **52**. Bumps **104** are formed between contact pads **98** of BCC **62** and contact pads **102** of PCB **52**.

In FIG. **3***c*, semiconductor die **58** is mounted face down to intermediate carrier **106** with a flip chip style first level packaging. Active region **108** of semiconductor die **58** contains analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit may include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region **108**. Semiconductor die **58** is electrically and mechanically connected to carrier **106** through bumps **110**.

BGA **60** is electrically and mechanically connected to PCB **52** with a BGA style second level packaging using bumps **112**. Semiconductor die **58** is electrically connected to conductive signal traces **54** in PCB **52** through bumps **110**, signal lines **114**, and bumps **112**. A molding compound or encapsulant **116** is deposited over semiconductor die **58** and carrier **106** to provide physical support and electrical isolation for the device. The flip chip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die **58** to conduction tracks on PCB **52** in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die **58** can be mechanically and electrically connected directly to PCB **52** using flip chip style first level packaging without intermediate carrier **106**.

FIG. **4***a* shows a semiconductor wafer **120** with a base substrate material **122**, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. A plurality of semiconductor die or components **124** is formed on wafer **120** separated by saw streets **126** as described above.

FIG. **4***b* shows a cross-sectional view of a portion of semiconductor wafer **120**. Each semiconductor die **124** has an active surface **130** containing analog or digital circuits imple-

mented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface **130** to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die **124** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die **124** is a flipchip type semiconductor die.

An electrically conductive layer **132** is formed over active surface **130** using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer **132** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer **132** operates as contact pads electrically connected to the circuits on active surface **130**.

In FIG. **4***c*, semiconductor wafer **120** is singulated through saw street **126** using a saw blade or laser cutting tool **136** into individual semiconductor die **124**.

FIGS. **5***a*-**5***m* illustrate, in relation to FIGS. **2** and **3***a*-**3***c*, a process of forming a Fo-WLCSP with conductive layers and conductive vias separated by polymer layers. In FIG. **5***a*, a substrate or carrier **140** contains temporary or sacrificial base material such as silicon, polymer, beryllium oxide, or other suitable low-cost, rigid material for structural support. In one embodiment, carrier **140** is a tape.

A polymer layer **142** is formed over carrier **140**. Polymer layer **142** can be an oxide, nitride, or glass material. An electrically conductive layer **144** is formed within polymer layer **142** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **144** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material.

A temporary carrier or substrate **146** contains sacrificial base material such as silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape **148** is formed over carrier **146** as a temporary adhesive bonding film or etch-stop layer.

In FIG. **5***b*, leading with polymer layer **142** and contact pads **144**, carrier **140** is mounted to interface layer **148** over carrier **146**. In one embodiment, polymer layer **142** is laminated to interface layer **148**. Conductive layer **144** operates as an array of contact pads formed around a perimeter of die attach area **149**. Polymer layer **142** and contact pads **144** constitute an interconnect structure.

In FIG. **5***c*, carrier **140** is removed from polymer layer **142** by mechanical peeling in the direction of arrow **150**. Polymer layer **142** and contact pads **144** remain affixed to interface layer **148** and carrier **146**. Alternatively, carrier **140** can be removed by chemical etching, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose polymer layer **142**.

In FIG. **5***d*, semiconductor die **124** from FIG. **4***a*-**4***c* are mounted to polymer layer **142** with active surface **130** oriented away from the polymer layer using a pick and place operation. Semiconductor die **124** is positioned over die attach area **149** within the array of contact pads **144**.

In FIG. **5***e*, a polymer layer **154** is formed over semiconductor die **124** and polymer layer **142**. Polymer layer **154** can be an oxide, nitride, or glass material. A portion of polymer layer **154** can be removed by an etching process to expose contact pads **132** for subsequent electrical interconnect.

In FIG. **5***f*, a plurality of vias **156** is formed through polymer layer **154** and **142** extending down to contact pads **144** using mechanical drilling, laser drilling, or deep reactive ion etching (DRIE). In FIG. **5***g*, vias **156** are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, tungsten (W), poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction conductive pillars or vias **158**. Conductive vias **158** are electrically connected to contact pads **144**.

FIG. **5***h* shows a top view of conductive vias **158** formed through polymer layer **154** around a perimeter of semiconductor die **124** taken along line **5***h*-**5***h* in FIG. **5***g*.

An electrically conductive layer or redistribution layer (RDL) **160** is formed over polymer layer **154** and conductive vias **158** using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **160** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer **160** is electrically connected to contact pads **132** and conductive vias **158**. Other portions of conductive layer **160** can be electrically common or electrically isolated depending on the design and function of semiconductor die **124**.

In FIG. **5***i*, a polymer layer **162** is formed over polymer layer **154** and conductive layer **160**. Polymer layer **162** can be an oxide, nitride, or glass material. A plurality of vias **164** is formed through polymer layer **162** extending down to conductive layer **160** using mechanical drilling, laser drilling, or DRIE, as shown in FIG. **5***j*. In FIG. **5***k*, vias **164** are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction conductive pillars or vias **166**. Conductive vias **166** are electrically connected to conductive layer **160**.

An electrically conductive layer or RDL **168** is formed over polymer layer **162** and conductive vias **166** using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **168** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer **168** is electrically connected to conductive vias **166**. Other portions of conductive layer **168** can be electrically common or electrically isolated depending on the design and function of semiconductor die **124**.

In FIG. **5***l*, an optional under bump metallization (UBM) **177** is formed over conductive layer **168**. A solder resist layer **170** is formed over polymer layer **162**, conductive layer **168**, and UBM **177**. A portion of solder resist layer **170** is removed by an etching process to expose conductive layer **168** or UBM **177** for bump formation or additional package interconnect. Alternatively, an insulating or passivation layer is formed over polymer layer **162**, conductive layer **168**, and UBM **177** using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer contains one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), or other material having similar insulating and structural properties. Polymer layer **162**, conductive vias **166**, conductive layer **168**, UBM **177**, and photoresist layer **170** constitute an interconnect structure.

In FIG. **5***m*, semiconductor die **124** are singulated into individual Fo-WLCSP **172** using saw blade or laser cutting tool **174**. FIG. **6***a* shows a cross-sectional view of Fo-WLCSP **172** after singulation. The temporary carrier **146** and interface

layer **148** are removed by chemical etching, mechanical peel-off, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose contact pads **144**.

An electrically conductive bump material is deposited over UBM **177** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to UBM **177** using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps **176**. In some applications, bumps **176** are reflowed a second time to improve electrical contact to UBM **177**. The bumps can also be compression bonded to UBM **177**. Bumps **176** represent one type of interconnect structure that can be formed over UBM **177**.

In Fo-WLCSP **172**, semiconductor die **124** is electrically connected through conductive layers **160** and **168** and conductive vias **158** and **166** to bumps **176** and contact pads **144** for external electrical interconnect. The array of contact pads **144** and bumps **176** are formed around a perimeter of semiconductor die **124**. FIG. **6***b* shows a top view of Fo-WLCSP **172** with the array of contact pads **144**. Fo-WLCSP **172** is formed without encapsulant or molding compound, as described in FIG. **1**. Instead, polymer layers **142**, **154**, and **162** are formed around semiconductor die **124**, conductive layers **160** and **168**, conductive vias **158** and **166**, and contact pads **144** to provide electrical isolation and structural support. Polymer layers **142**, **154**, and **162** can be formed with less height than the encapsulant found in the prior art. Accordingly, polymer layers **142**, **154**, and **162** provide flexible bump arrangement options, reduced bump pitch, increased I/O count, as well as reducing the height of Fo-WLCSP **172**.

Fo-WLCSP **172** is suitable for package-on-package (PoP) applications, such as shown in FIG. **7**, with Fo-WLCSP **178** stacked over Fo-WLCSP **172**. Fo-WLCSP **178** is configured similar to Fo-WLCSP **172**. The electrical signals between Fo-WLCSP **172** and Fo-WLCSP **178** are routed through the array of bumps **176** formed around the perimeter of semiconductor die **124**. Since no gold wire bonds are used for signal transmission between the Fo-WLCSPs, the interconnect inductance and capacitance is reduced and signal integrity is improved. Reflection noise and crosstalk can be reduced by matching the impedance between semiconductor die **124** and conductive layers **160** and **168**, conductive vias **158** and **166**, and contact pads **144** formed in polymer layers **142**, **154**, and **162**.

FIGS. **8***a*-**8***r* illustrate, in relation to FIGS. **2** and **3***a*-**3***c*, another process of forming a Fo-WLCSP with conductive layers and conductive vias separated by polymer layers. In FIG. **8***a*, a substrate or carrier **180** contains temporary or sacrificial base material such as silicon, polymer, beryllium oxide, or other suitable low-cost, rigid material for structural support. In one embodiment, carrier **180** is a tape.

A polymer layer **182** is formed over carrier **180**. Polymer layer **182** can be an oxide, nitride, or glass material. An electrically conductive layer **184** is formed within polymer layer **182** using a patterning and metal deposition process such as PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **184** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material.

A temporary carrier or substrate **186** contains sacrificial base material such as silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape **188** is formed over carrier **186** as a temporary adhesive bonding film or etch-stop layer.

In FIG. **8***b*, leading with polymer layer **182** and contact pads **184**, carrier **180** is mounted to interface layer **188** over carrier **186**. In one embodiment, polymer layer **182** is laminated to interface layer **188**. Conductive layer **184** operates as an array of contact pads uniformly disposed over substantially an entire surface area of polymer layer **182**.

In FIG. **8***c*, carrier **180** is removed from polymer layer **182** by mechanical peeling in the direction of arrow **190**. Polymer layer **182** and contact pads **184** remain affixed to interface layer **188** and carrier **186**. Alternatively, carrier **180** can be removed by chemical etching, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose polymer layer **182**.

FIG. **8***d* shows polymer layer **182** after removal of carrier **182**. A plurality of vias **196** is formed through polymer layer **182** extending down to contact pads **184** using mechanical drilling, laser drilling, or DRIE, as shown in FIG. **8***e*. In FIG. **8***f*, vias **196** are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction conductive pillars or vias **198**. Conductive vias **198** are electrically connected to contact pads **184**. FIG. **8***g* shows a top view of conductive vias **198** formed over contact pads **184** taken along line **8***g*-**8***g* of FIG. **8***f*.

An electrically conductive layer or RDL **200** is formed over polymer layer **182** and conductive vias **198** using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **200** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer **200** is electrically connected to conductive vias **198**. Other portions of conductive layer **200** can be electrically common or electrically isolated depending on the design and function of semiconductor die **124**.

In FIG. **8***h*, a polymer layer **202** is formed over polymer layer **182** and conductive layer **200**. Polymer layer **202** can be an oxide, nitride, or glass material. Polymer layers **182** and **202**, conductive vias **198**, and conductive layer **200** constitute an interconnect structure.

In FIG. **8***i*, semiconductor die **124** from FIG. **4***a*-**4***c* are mounted to polymer layer **202** with active surface **130** oriented away from the polymer layer using a pick and place operation.

In FIG. **8***j*, a polymer layer **204** is formed over semiconductor die **124** and polymer layer **202**. Polymer layer **204** can be an oxide, nitride, or glass material. A portion of polymer layer **204** can be removed by an etching process to expose contact pads **132** of semiconductor die **124** for subsequent electrical interconnect.

In FIG. **8***k*, a plurality of vias **206** is formed through polymer layer **204** and **202** extending down to conductive layer **200** using mechanical drilling, laser drilling, or DRIE. The vias **206** are formed around a perimeter of semiconductor die **124**. In FIG. **8***l*, vias **206** are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction conductive pillars or vias **208**. Conductive vias **208** are electrically connected to conductive layer **200**.

FIG. **8***m* shows a top view of conductive vias **208** formed around semiconductor die **124** taken along line **8***m*-**8***m* in FIG. **8***l*.

An electrically conductive layer or redistribution layer RDL **210** is formed over polymer layer **204** and conductive vias **208** using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **210** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer **210** is electrically connected to contact pads **132** and conductive vias **208**. Other portions of conductive layer **210** can be electrically common or electrically isolated depending on the design and function of semiconductor die **124**.

In FIG. **8***n*, a polymer layer **212** is formed over polymer layer **204** and conductive layer **210**. Polymer layer **212** can be an oxide, nitride, or glass material. A plurality of vias **214** is formed through polymer layer **212** extending down to conductive layer **210** using mechanical drilling, laser drilling, or DRIE, as shown in FIG. **80**.

In FIG. **8***p*, vias **214** are filled with Al, Cu, Sn, Ni, Au, Ag, Ti, W, poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction conductive pillars or vias **216**. Conductive vias **216** are electrically connected to conductive layer **210**.

An electrically conductive layer or RDL **218** is formed over polymer layer **212** and conductive vias **216** using a patterning and metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer **218** can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer **218** is electrically connected to conductive vias **216**. Other portions of conductive layer **218** can be electrically common or electrically isolated depending on the design and function of semiconductor die **124**.

In FIG. **8***q*, an optional UBM **228** is formed over conductive layer **218**. A solder resist layer **220** is formed over polymer layer **212**, conductive layer **218**, and UBM **228**. A portion of solder resist layer **220** is removed by an etching process to expose conductive layer **218** or UBM **228** for bump formation or additional package interconnect. Alternatively, an insulating or passivation layer is formed over polymer layer **212**, conductive layer **218**, and UBM **228** using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation. The insulating layer contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, or other material having similar insulating and structural properties. Polymer layer **212**, conductive vias **216**, conductive layer **218**, UBM **228**, and photoresist layer **220** constitute an interconnect structure.

In FIG. **8***r*, semiconductor die **124** are singulated into individual Fo-WLCSP **222** using saw blade or laser cutting tool **224**. FIG. **9** shows a cross-sectional view of Fo-WLCSP **222** after singulation. The temporary carrier **186** and interface layer **188** are removed by chemical etching, mechanical peel-off, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose contact pads **184**.

An electrically conductive bump material is deposited over UBM **228** using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to UBM **228** using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form spherical balls or bumps **226**. In some applications, bumps **226** are reflowed a second time to improve electrical contact to UBM **228**. The bumps can also be compression bonded to UBM **228**. Bumps **226** represent one type of interconnect structure that can be formed over UBM **228**.

In Fo-WLCSP **222**, semiconductor die **124** is electrically connected through conductive layers **200**, **210**, and **218** and conductive vias **198**, **208**, and **216** to bumps **226** and contact pads **184** for external electrical interconnect. The array of contact pads **184** and bumps **226** are formed over the full surface area of Fo-WLCSP **222**. Fo-WLCSP **222** is formed without encapsulant or molding compound, as described in FIG. **1**. Instead, polymer layers **182**, **202**, **204**, and **212** are formed around semiconductor die **124**, conductive layers **200**, **210**, and **218**, conductive vias **198**, **208**, and **216**, and contact pads **184** to provide electrical isolation and structural support. Polymer layers **182**, **202**, **204**, and **212** can be formed with less height than the encapsulant found in the prior art. Accordingly, polymer layers **182**, **202**, **204**, and **212** provide flexible bump arrangement options, reduced bump pitch, increased I/O count, as well as reducing the height of Fo-WLCSP **222**.

Fo-WLCSP **222** is suitable for PoP applications as shown in FIG. **10***a* with Fo-WLCSP **230** stacked over Fo-WLCSP **222**. In Fo-WLCSP **230**, semiconductor die **231** is mounted to semiconductor die **232** with die attach adhesive **234**. Semiconductor die **231** and **232** each have an active surface containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within the active surface to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die **231** and **232** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. Bond wires **236** and **238** are electrically connected to contact pads on semiconductor die **231** and **232**, respectively. An encapsulant **240** is deposited over semiconductor die **231** and **232** and bond wires **236** and **238**. A build-up interconnect structure **242** is formed over semiconductor die **232** and encapsulant **240**. Semiconductor die **232** is bonded to interconnect structure **242** with die attach adhesive **235**. Bond wires **236** and **238** are electrically connected through interconnect structure **242** to bumps **244**, which in turn are electrically connected to contact pads **184** of Fo-WLCSP **222**. Semiconductor die **231** and **232**, encapsulant **240**, and interconnect structure **242** constitute a semiconductor package. FIG. **10***b* shows a cross-sectional view of contact pads **184** and polymer layer **182** taken through line **10***b*-**10***b* in FIG. **10***a*.

The electrical signals between Fo-WLCSP **222** and Fo-WLCSP **230** are routed through the array of contact pads **184** and bumps **244**. Since no gold wire bonds are used for signal transmission between the Fo-WLCSPs, the interconnect inductance and capacitance is reduced and signal integrity is improved. Reflection noise and crosstalk can be reduced by matching the impedance between semiconductor die **124** and conductive layers **200**, **210**, and **218**, conductive vias **198**, **208**, and **216**, and contact pads **184** formed in polymer layers **182**, **202**, **204**, and **212**.

FIG. **11***a* shows another PoP configuration with Fo-WLCSP **248** stacked over Fo-WLCSP **250**, similar to FIG. **6***a*. In Fo-WLCSP **248**, semiconductor die **252** is mounted to semiconductor die **254** with die attach adhesive **256**. Semiconductor die **252** and **254** each have an active surface containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielec-

tric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within the active surface to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die **252** and **254** may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. Bond wires **260** and **262** are electrically connected to contact pads on semiconductor die **252** and **254**, respectively. An encapsulant **264** is deposited over semiconductor die **252** and **254** and bond wires **260** and **262**. A build-up interconnect structure **266** is formed over semiconductor die **252** and **254** and encapsulant **264**. Semiconductor die **254** is bonded to interconnect structure **266** with die attach adhesive **258**. Bond wires **260** and **262** are electrically connected through interconnect structure **266** to bumps **268**, which in turn are electrically connected to contact pads **144** of Fo-WLCSP **250**. Semiconductor die **252** and **254**, encapsulant **264**, and interconnect structure **266** constitute a semiconductor package. FIG. **11***b* shows a cross-sectional view of contact pads **144** and polymer layer **142** taken through line **11***b*-**11***b* in FIG. **11***a*.

The electrical signals between Fo-WLCSP **248** and Fo-WLCSP **250** are routed through the array of contact pads **144** and bumps **268**. Since no gold wire bonds are used for signal transmission between the Fo-WLCSPs, the interconnect inductance and capacitance is reduced and signal integrity is improved. Reflection noise and crosstalk can be reduced by matching the impedance between semiconductor die **124** and conductive layers **160** and **168**, conductive vias **158** and **166**, and contact pads **144** formed in polymer layers **142**, **154**, and **162**.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

What is claimed:

1. A semiconductor device, comprising:
a first polymer layer;
a first semiconductor die disposed over the first polymer layer;
a second polymer layer formed over the first polymer layer and first semiconductor die; and
a first conductive via formed through openings in the first polymer layer and second polymer layer.

2. The semiconductor device of claim **1**, further including:
a third polymer layer formed over the second polymer layer; and
a second conductive via formed through the third polymer layer.

3. The semiconductor device of claim **1**, further including an interconnect structure formed over the second polymer layer.

4. The semiconductor device of claim **1**, further including:
a third polymer layer formed over the second polymer layer;
a second conductive via formed through the third polymer layer; and
a conductive layer formed over the third polymer layer and electrically connected to the second conductive via.

5. The semiconductor device of claim **4**, further including a second semiconductor die disposed over the first polymer layer or third polymer layer.

6. The semiconductor device of claim **1**, further including a plurality of the first conductive vias formed around a perimeter of the first semiconductor die.

7. A semiconductor device, comprising:
a first polymer layer including a first conductive layer within the first polymer layer;
a first semiconductor die disposed over a surface of the first polymer layer opposite the first conductive layer;
a second polymer layer formed over the first polymer layer and first semiconductor die; and
a first conductive via formed through the first polymer layer and second polymer layer and coupled to the first conductive layer.

8. The semiconductor device of claim **7**, further including:
a third polymer layer formed over the second polymer layer; and
a second conductive via formed through the third polymer layer.

9. The semiconductor device of claim **7**, further including a second conductive layer formed over the second polymer layer.

10. The semiconductor device of claim **7**, further including an interconnect structure formed over the second polymer layer.

11. The semiconductor device of claim **8**, further including a second semiconductor die disposed over the first polymer layer or third polymer layer.

12. The semiconductor device of claim **7**, further including a plurality of the first conductive vias formed around a perimeter of the first semiconductor die.

13. A semiconductor device, comprising:
a first polymer layer;
a first semiconductor die disposed over the first polymer layer;
a second polymer layer formed over the first polymer layer; and
a first interconnect structure formed through openings in the first polymer layer and second polymer layer.

14. The semiconductor device of claim **13**, further including:
a third polymer layer formed over the second polymer layer; and
a conductive via formed through the third polymer layer.

15. The semiconductor device of claim **13**, further including a second interconnect structure formed over the second polymer layer.

16. The semiconductor device of claim **13**, further including:
a third polymer layer formed over the second polymer layer;
a conductive via formed through the third polymer layer; and
a conductive layer formed over the third polymer layer and electrically connected to the conductive via.

17. The semiconductor device of claim **16**, further including a second semiconductor die disposed over the first polymer layer or third polymer layer.

18. The semiconductor device of claim **13**, further including a plurality of conductive vias formed around a perimeter of the first semiconductor die.

19. A method of making a semiconductor device, comprising:
providing a first polymer layer including a first conductive layer within the first polymer layer;

disposing a first semiconductor die over a surface of the first polymer layer opposite the first conductive layer;

forming a second polymer layer over the first polymer layer and first semiconductor die; and

forming a first conductive via through openings in the first polymer layer and second polymer layer and coupled to the first conductive layer.

20. The method of claim **19**, further including:

forming a third polymer layer over the first polymer layer; and

forming a second conductive via through the third polymer layer.

21. The method of claim **19**, further including forming a second conductive layer over the second polymer layer.

22. The method of claim **19**, further including forming an interconnect structure over the second polymer layer.

23. The method of claim **19**, further including:

forming a third polymer layer over the second polymer layer;

forming a second conductive via through the third polymer layer; and

forming a second conductive layer over the third polymer layer and electrically connected to the second conductive via.

24. The method of claim **23**, further including disposing a second semiconductor die over the first polymer layer or third polymer layer.

25. The method of claim **19**, further including forming a plurality of the first conductive vias around a perimeter of the first semiconductor die.

26. A method of making a semiconductor device, comprising:

providing a first polymer layer;

disposing a first semiconductor die over the first polymer layer;

forming a second polymer layer over the first polymer layer and first semiconductor die; and

forming a first conductive via through openings in the first polymer layer and second polymer layer.

27. The method of claim **26**, further including:

forming a third polymer layer over the first polymer layer; and

forming a second conductive via through the third polymer layer.

28. The method of claim **26**, further including forming an interconnect structure over the second polymer layer.

29. The method of claim **26**, further including:

forming a third polymer layer over the second polymer layer;

forming a second conductive via through the third polymer layer; and

forming a conductive layer over the third polymer layer and electrically connected to the second conductive via.

30. The method of claim **29**, further including disposing a second semiconductor die over the first polymer layer or third polymer layer.

31. The method of claim **26**, further including forming a plurality of the first conductive vias around a perimeter of the first semiconductor die.

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