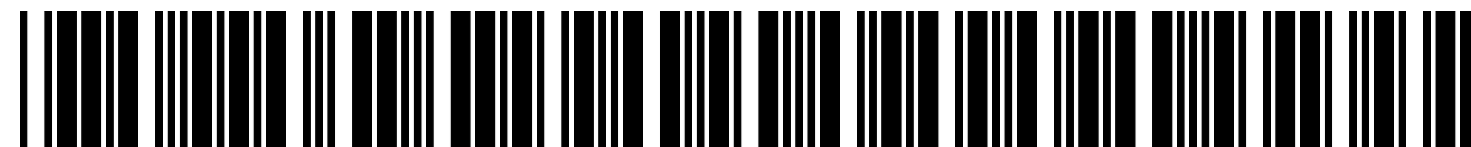


(12) **United States Patent**
Lugani et al.

(10) **Patent No.: US 8,652,926 B1**
(45) **Date of Patent: Feb. 18, 2014**

(54) **METHODS OF FORMING CAPACITORS**

(75) Inventors: **Gurpreet Lugani**, Punjab (IN); **Kevin J. Torek**, Meridian, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/559,073**

(22) Filed: **Jul. 26, 2012**

(51) **Int. Cl.**
H01L 21/20 (2006.01)
H01L 21/8242 (2006.01)
H01L 21/302 (2006.01)
H01L 21/461 (2006.01)

(52) **U.S. Cl.**
USPC **438/396**; 438/397; 438/381; 438/253; 438/706; 438/710; 438/738; 438/386; 438/387

(58) **Field of Classification Search**
USPC 438/238, 239, 243, 244, 381, 386–389, 438/396–399
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,517,729	A	5/1985	Batra
4,871,688	A	10/1989	Lowrey
5,236,860	A	8/1993	Fazan et al.
5,252,517	A	10/1993	Blalock et al.
5,340,763	A	8/1994	Dennison
5,401,681	A	3/1995	Dennison
5,467,305	A	11/1995	Bertin et al.
5,498,562	A	3/1996	Dennison et al.
5,532,089	A	7/1996	Adair et al.
5,604,696	A	2/1997	Takaishi
5,605,857	A	2/1997	Jost et al.
5,652,164	A	7/1997	Dennison et al.
5,654,222	A	8/1997	Sandhu et al.
5,672,534	A	9/1997	Huang
5,686,747	A	11/1997	Jost et al.
5,702,990	A	12/1997	Jost et al.
5,705,838	A	1/1998	Jost et al.
5,767,561	A	6/1998	Frei et al.
5,784,112	A	7/1998	Ogasawara et al.
5,821,140	A	10/1998	Jost et al.
5,869,382	A	2/1999	Kubota
5,900,660	A	5/1999	Jost et al.
5,955,758	A	9/1999	Sandhu et al.
5,956,594	A	9/1999	Yang et al.

(Continued)

FOREIGN PATENT DOCUMENTS

CN	1230778	10/1999
CN	101154620	4/2008

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 12/854,446, filed Aug. 11, 2010, Lee

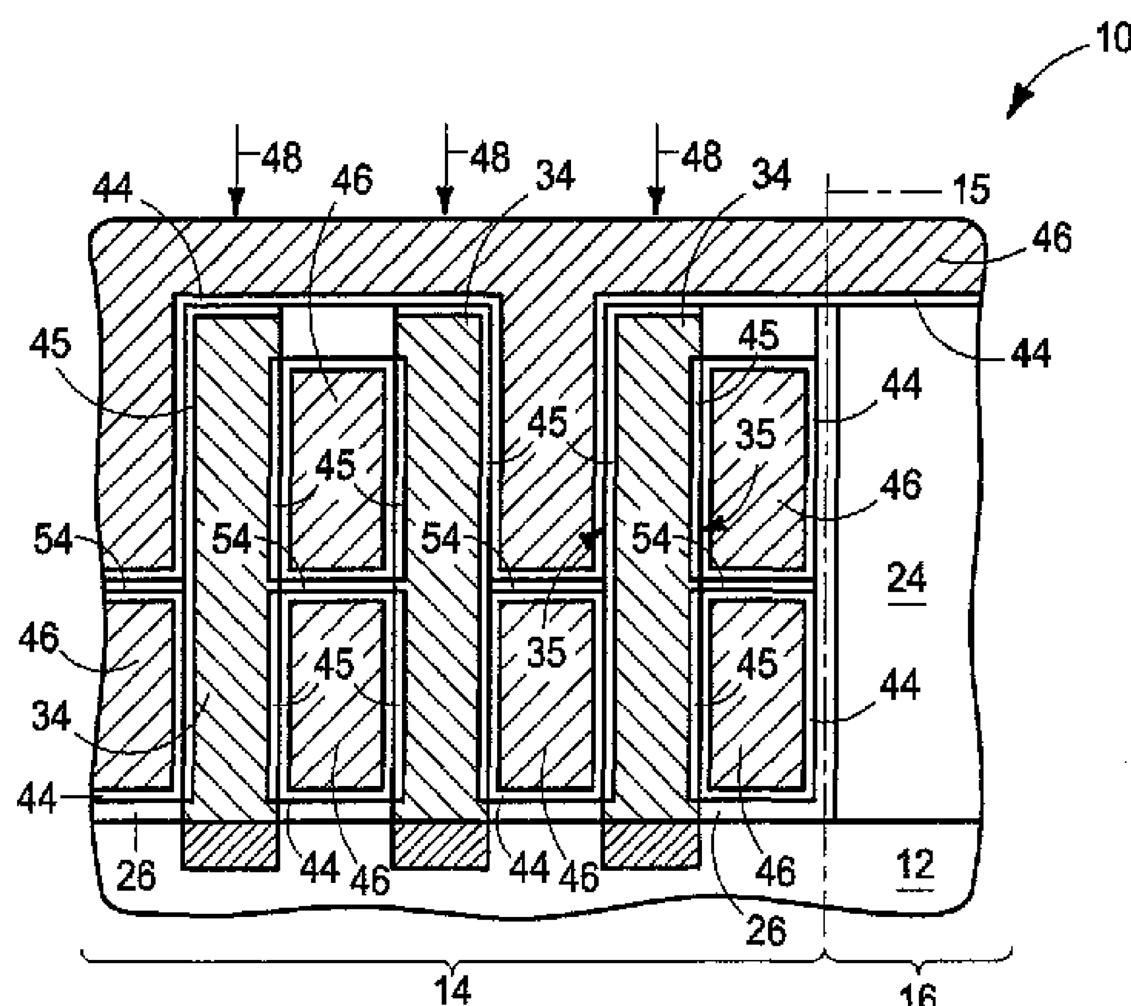
(Continued)

Primary Examiner — Mary Wilczewski
Assistant Examiner — Erik T Peterson
(74) *Attorney, Agent, or Firm* — Wells St. John, P.S.

(57) **ABSTRACT**

A method of forming capacitors includes providing first capacitor electrodes within support material. The first capacitor electrodes contain TiN and the support material contains polysilicon. The polysilicon-containing support material is dry isotropically etched selectively relative to the TiN-containing first capacitor electrodes using a sulfur and fluorine-containing etching chemistry. A capacitor dielectric is formed over sidewalls of the first capacitor electrodes and a second capacitor electrode is formed over the capacitor dielectric. Additional methods are disclosed.

14 Claims, 4 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

5,981,350	A	11/1999	Geusic et al.
5,981,992	A	11/1999	Kenney
5,989,953	A	11/1999	Liang et al.
5,990,021	A	11/1999	Prall et al.
6,037,212	A	3/2000	Chao
6,037,218	A	3/2000	Dennnison et al.
6,059,553	A	5/2000	Jin et al.
6,090,700	A	7/2000	Tseng
6,108,191	A	8/2000	Bruchhaus et al.
6,110,774	A	8/2000	Jost et al.
6,121,084	A	9/2000	Coursey
6,133,620	A	10/2000	Uochi
6,159,818	A	12/2000	Durcan et al.
6,159,820	A	12/2000	Park
6,180,450	B1	1/2001	Dennison
6,204,143	B1	3/2001	Roberts et al.
6,204,178	B1	3/2001	Marsh
6,232,168	B1	5/2001	Coursey
6,245,684	B1	6/2001	Zhao et al.
6,249,019	B1	6/2001	Sandhu et al.
6,258,650	B1	7/2001	Sunouchi
6,274,497	B1	8/2001	Lou
6,303,518	B1	10/2001	Tian et al.
6,303,956	B1	10/2001	Sandhu et al.
6,323,528	B1	11/2001	Yamazaki et al.
6,329,683	B2	12/2001	Kohyama
6,331,461	B1	12/2001	Juengling
6,372,554	B1	4/2002	Kawakita et al.
6,372,574	B1	4/2002	Lane et al.
6,383,861	B1	5/2002	Gonzalez et al.
6,399,490	B1	6/2002	Jammy et al.
6,403,442	B1	6/2002	Reinberg
6,432,472	B1	8/2002	Farrell et al.
6,458,653	B1	10/2002	Jang
6,458,925	B1	10/2002	Fasano
6,459,138	B2	10/2002	Reinberg
6,475,855	B1	11/2002	Fishburn
6,476,432	B1	11/2002	Basceri et al.
6,482,749	B1	11/2002	Billington et al.
6,583,063	B1	6/2003	Khan et al.
6,617,222	B1	9/2003	Coursey
6,620,680	B2	9/2003	Durcan et al.
6,620,724	B1	9/2003	Schroeder et al.
6,645,869	B1	11/2003	Chu et al.
6,656,748	B2	12/2003	Hall et al.
6,667,502	B1	12/2003	Agarwal et al.
6,673,693	B2	1/2004	Kirchhoff
6,696,745	B2	2/2004	Sandhu et al.
6,703,273	B2	3/2004	Wang et al.
6,707,088	B2	3/2004	Fishburn
6,709,978	B2	3/2004	Geusic et al.
6,720,232	B1	4/2004	Tu et al.
6,767,789	B1	7/2004	Bronner et al.
6,784,112	B2	8/2004	Arita et al.
6,784,479	B2	8/2004	Park
6,787,833	B1	9/2004	Fishburn
6,812,513	B2	11/2004	Geusic et al.
6,822,261	B2	11/2004	Yamazaki et al.
6,822,280	B2	11/2004	Ito et al.
6,844,230	B2	1/2005	Reinberg
6,849,496	B2	2/2005	Jaiprakash et al.
6,853,023	B2	2/2005	Goebel
6,861,330	B2	3/2005	Basceri et al.
6,890,814	B2	5/2005	Sandhu et al.
6,893,914	B2	5/2005	Kim et al.
6,897,109	B2	5/2005	Jin et al.
6,927,122	B2	8/2005	Geusic et al.
6,927,170	B2	8/2005	Zheng
6,930,640	B2	8/2005	Chung et al.
6,936,880	B2	8/2005	Park
6,939,794	B2	9/2005	Yin et al.
6,962,846	B2	11/2005	Fishburn et al.
6,991,980	B2	1/2006	Park
7,005,379	B2	2/2006	Sinha et al.
7,042,040	B2	5/2006	Horiguchi
7,053,435	B2	5/2006	Yeo et al.
7,053,453	B2	5/2006	Tsao et al.
7,064,028	B2	6/2006	Ito et al.
7,064,365	B2	6/2006	An et al.
7,067,385	B2	6/2006	Manning
7,071,055	B2	7/2006	Fishburn
7,073,969	B2	7/2006	Kamm
7,074,669	B2	7/2006	Iijima et al.
7,081,384	B2	7/2006	Birner et al.
7,084,451	B2	8/2006	Forbes et al.
7,087,484	B2	8/2006	Goldbach et al.
7,094,701	B2	8/2006	Umemoto et al.
7,115,500	B1	10/2006	Torres
7,115,531	B2	10/2006	Shaffer et al.
7,122,424	B2	10/2006	Tu et al.
7,125,781	B2	10/2006	Manning et al.
7,153,778	B2	12/2006	Busch et al.
7,160,788	B2	1/2007	Sandhu et al.
7,179,706	B2	2/2007	Patraw et al.
7,199,005	B2	4/2007	Sandhu et al.
7,202,127	B2	4/2007	Busch et al.
7,223,690	B2	5/2007	Kondo et al.
7,226,845	B2	6/2007	Manning et al.
7,235,441	B2	6/2007	Yasui et al.
7,235,479	B2	6/2007	Verhaverbeke
7,235,485	B2	6/2007	Kwak et al.
7,268,034	B2	9/2007	Basceri et al.
7,268,039	B2	9/2007	Fishburn et al.
7,271,051	B2	9/2007	Manning et al.
7,273,779	B2	9/2007	Fishburn et al.
7,279,379	B2	10/2007	Tran et al.
7,282,756	B2	10/2007	Agarwal et al.
7,288,806	B2	10/2007	Tran et al.
7,320,911	B2	1/2008	Basceri et al.
7,321,149	B2	1/2008	Busch et al.
7,321,150	B2	1/2008	Fishburn et al.
7,335,935	B2	2/2008	Sinha et al.
7,341,909	B2	3/2008	McDaniel et al.
7,384,847	B2	6/2008	Tran et al.
7,387,939	B2	6/2008	Manning
7,393,741	B2	7/2008	Sandhu et al.
7,393,743	B2	7/2008	Manning
7,413,952	B2	8/2008	Busch et al.
7,420,238	B2	9/2008	Manning et al.
7,439,152	B2	10/2008	Manning
7,440,255	B2	10/2008	McClure et al.
7,442,600	B2	10/2008	Wang et al.
7,445,990	B2	11/2008	Busch et al.
7,445,991	B2	11/2008	Manning
7,449,391	B2	11/2008	Manning et al.
7,459,362	B2	12/2008	Juengling
7,474,215	B2	1/2009	Scott et al.
7,517,754	B2	4/2009	McDaniel et al.
7,534,694	B2	5/2009	Manning
7,538,036	B2	5/2009	Busch et al.
7,544,563	B2	6/2009	Manning
7,557,013	B2	7/2009	Bhat et al.
7,557,015	B2	7/2009	Sandhu et al.
7,573,088	B2	8/2009	Juengling
7,576,441	B2	8/2009	Yin et al.
7,629,262	B2	12/2009	Kim et al.
7,638,392	B2	12/2009	Wang et al.
7,655,968	B2	2/2010	Manning
7,682,924	B2	3/2010	Bhat et al.
7,700,469	B2 *	4/2010	Benson 438/552
7,759,193	B2	7/2010	Fishburn
7,785,962	B2	8/2010	Bhat et al.
7,807,580	B2	10/2010	Lee et al.
7,902,081	B2	3/2011	Raghu et al.
8,105,904	B2	1/2012	Oh et al.
8,134,823	B2	3/2012	Chen et al.
2001/0012223	A1	8/2001	Kohyama
2001/0026974	A1	10/2001	Reinberg
2001/0038111	A1	11/2001	DeBoer et al.
2001/0044181	A1	11/2001	Nakamura
2002/0003249	A1	1/2002	Park
2002/0022339	A1	2/2002	Kirchhoff
2002/0030221	A1	3/2002	Sandhu et al.
2002/0039826	A1	4/2002	Reinberg

(56) **References Cited**

U.S. PATENT DOCUMENTS

2002/0090779	A1	7/2002	Jang	
2002/0098654	A1	7/2002	Durcan et al.	
2002/0153589	A1	10/2002	Oh	
2002/0153614	A1	10/2002	Ema et al.	
2002/0163026	A1	11/2002	Park	
2003/0085420	A1	5/2003	Ito et al.	
2003/0134468	A1	7/2003	Wang et al.	
2003/0153146	A1	8/2003	Won et al.	
2003/0178684	A1	9/2003	Nakamura	
2003/0190782	A1	10/2003	Ko et al.	
2003/0227044	A1	12/2003	Park	
2004/0018679	A1	1/2004	Yu et al.	
2004/0150070	A1	8/2004	Okada et al.	
2004/0188738	A1	9/2004	Farnworth et al.	
2004/0232106	A1	11/2004	Oka et al.	
2005/0023588	A1	2/2005	Sandhu et al.	
2005/0051822	A1	3/2005	Manning	
2005/0158949	A1	7/2005	Manning	
2005/0176210	A1	8/2005	Kim et al.	
2005/0287738	A1	12/2005	Cho et al.	
2005/0287780	A1	12/2005	Manning et al.	
2005/0287795	A1	12/2005	Torek et al.	
2006/0006502	A1	1/2006	Yin et al.	
2006/0024958	A1	2/2006	Ali	
2006/0024966	A1	2/2006	Umemoto et al.	
2006/0046420	A1	3/2006	Manning	
2006/0063344	A1	3/2006	Manning et al.	
2006/0115951	A1	6/2006	Mosley	
2006/0115952	A1	6/2006	Wu	
2006/0121672	A1	6/2006	Basceri et al.	
2006/0148190	A1	7/2006	Busch	
2006/0176210	A1	8/2006	Nakamura et al.	
2006/0186451	A1	8/2006	Dusberg et al.	
2006/0211196	A1	9/2006	Tanaka et al.	
2006/0211211	A1	9/2006	Sandhu et al.	
2006/0237762	A1	10/2006	Park	
2006/0249798	A1	11/2006	Manning	
2006/0261440	A1	11/2006	Manning	
2006/0263968	A1	11/2006	Manning	
2006/0286783	A1	12/2006	Papanu et al.	
2006/0289914	A1	12/2006	Juengling	
2007/0032014	A1	2/2007	Sandhu et al.	
2007/0045699	A1	3/2007	Liao et al.	
2007/0048976	A1	3/2007	Raghu	
2007/0057304	A1	3/2007	Boescke et al.	
2007/0066010	A1	3/2007	Ando	
2007/0093022	A1	4/2007	Basceri	
2007/0099328	A1	5/2007	Chiang et al.	
2007/0099423	A1	5/2007	Chen et al.	
2007/0145009	A1	6/2007	Fucsko et al.	
2007/0196978	A1	8/2007	Manning	
2007/0202686	A1	8/2007	Dixit et al.	
2007/0207622	A1	9/2007	Rana et al.	
2007/0238259	A1	10/2007	Bhat	
2007/0257323	A1	11/2007	Tsui et al.	
2008/0090416	A1	4/2008	Raghu et al.	
2008/0171137	A1	7/2008	Kim et al.	
2008/0174430	A1	7/2008	Scott et al.	
2009/0047769	A1	2/2009	Bhat et al.	
2009/0176011	A1	7/2009	Kiehlbauch	
2009/0251845	A1	10/2009	Kiehlbauch	
2010/0009512	A1	1/2010	Fishburn	
2010/0041204	A1	2/2010	Kielbauch	
2010/0112798	A1	5/2010	Lai et al.	
2011/0151655	A1	6/2011	Chan et al.	
2011/0183522	A1	7/2011	Mikhaylichenko et al.	
2011/0227167	A1	9/2011	Chuang et al.	
2012/0012922	A1	1/2012	Jang	
2012/0040507	A1*	2/2012	Lee	438/381
2013/0164902	A1*	6/2013	Greeley et al.	438/381

FOREIGN PATENT DOCUMENTS

CN	101208775	6/2008
CN	200980126565.1	1/2013
DE	4447804	1/2011
JP	2004-155810	5/1992
JP	1996-274278	10/1996
JP	1998-189912	7/1998
JP	1999-026719	1/1999
JP	1999-191615	7/1999
JP	2000-196038	7/2000
JP	2001-189438	7/2001
JP	2003-142605	5/2003
JP	2003-264246	9/2003
JP	2003-273247	9/2003
JP	2003-297952	10/2003
JP	2004-072078	3/2004
JP	2004-111626	4/2004
JP	2004-128463	4/2004
JP	2005-032982	2/2005
JP	2006-032695	2/2006
JP	2006-135364	5/2006
KR	20010061020	7/2001
KR	2001-0114003	12/2001
KR	102001108963	12/2001
KR	1020030058018	7/2003
KR	1020050000896	1/2005
KR	10-520223	10/2005
TW	513801	12/2002
TW	I252511	4/2006
TW	I307160	3/2009
TW	098121062	8/2012
WO	PCT/US04/0027898	2/2005
WO	WO 2005/024936	3/2005
WO	PCT/US04/0040252	5/2005
WO	WO 2005/062349	7/2005
WO	PCT/US06/06806	7/2006
WO	PCT/US06/06806	1/2007
WO	PCT/US06/06806	2/2007
WO	PCT/US2008/070071	7/2009
WO	PCT/US09/046946	1/2010
WO	PCT/US08/070071	2/2010
WO	PCT/US2009/046946	1/2011

OTHER PUBLICATIONS

"Conductive Polymer" Wikipedia http://en/wikipedia.org/w/index.php?title=Conductive_polymer&printable=yes.

Banhart., "Aluminum Foams: on the road to real applications", MRS Bulletin, Apr. 2003, pp. 290-295.

Crouse et al., "Self-Assembled Nanostructures Using Anodized Alunmina Thin Films for Optoelectronic applications", IEEE, pp. 234-235, 1999.

Gibson et al., "Cellular Solids", MRS Bulletin, Apr. 2003, pp. 270-274.

Green et al., "Cellular Ceramics: Intriguing Structures, Novel Properties, and Innovative Applications", MRS Bulletin, Apr. 2003, pp. 296-300.

Green et al., "The Structure and Applications of Cellular Ceramics", MRS Bulletin, Apr. 2003, 10 pages.

J Robertson, Diamond-like amorphous carbon, Material Science and Engineering R 37 (2002) 129-281.

John Robertson, Hard Amorphous (Diamond-Like) Carbons, Prog Solid St Chem. vol. 21, pp. 199-333, (1991).

Karp et al., "Scaffolds for Tissue Engineering", MRS Bulletin, Apr. 2003, pp. 301-302.

Kim et al., "A mechanically enhanced storage node for virtually unlimited height (MESH) capacitor aiming at sub 70nm DRAMs", IEEE, Jan. 2004, pp. 69-72.

Konovalov et al., "Chemistry of Materials", Chem. Mater., vol. 11, No. 8, pp. 1949-1951 (Aug. 1999).

Kraynik, "Foam Structure: From Soap Froth to Solid Foams", MRS Bulletin, Apr. 2003, pp. 275-278.

Li., "Metal-assisted chemical etching in HF/H202 produces porous silicon", Applied Physics Letters, vol. 77, No. 16, Oct. 16, 2000, pp. 2572-2574.

(56) **References Cited**

OTHER PUBLICATIONS

Liang et al., "Nonlithographic Fabrication of Lateral Superlattices for Nanometric Electromagnetic-Optic . . . ", IEEE J. Selected Topics in Quantum Electr., vol. 8, No. 5, pp. 998-1008 (Sep./Oct. 2002).
Liu et al., "Ordered anodic alumina nanochannels on focused-ion-beam-prepatterned aluminum surfaces", appl. Phys. Lett. vol. 78, No. 1, pp. 120-122 (Jan. 2001).
Maire et al., "In Situ X-Ray tomography Measurements of Deformation in Cellular Solids", MRS Bulletin, Apr. 2003, pp. 284-289.
Masuda et al., "Highly ordered nanochannel-array architecture in anodic alumina", App. Phys. Lett, vol. 71, No. 19, Nov. 1997, pp. 2770-2772.
Nadeem et al., "Fabrication of Microstructures Using Aluminum Anodization Techniques", pre-2004, pp. 274-277.
Oh et al., "Preparation and Pore-Characteristics Control of Nano-Porous Materials Using Organometallic Building Blocks", Carbon Science, vol. 4, No. 1, Mar. 2003, pp. 1-9.
Onck, "Scale Effects in Cellular Metals", MRS Bulletin, Apr. 2003, pp. 279-283.
O'Sullivan et al., "The Morphology and Mechanism of Formation of Porous Anodic Films on Aluminum", Proc. Roy. Soc. Lond. A, vol. 317, 1970, pp. 511-543.
Park et al., "Block Copolymer Lithography: Periodic Arrays of~1011 Holes in 1 Square Centimeter", Science, vol. 276, May 1997, pp. 1401-1404.
Park et al., "Novel Robust Cell Capacitor (Leaning Exterminated Ring Type Insulator) and New Storage Node Contact", IEEE, 2004 Symposium on VLSI Technology Digest of Technical Papers, pp. 34-35.
Shingubara, "Fabrication of nanomaterials using porous aluina templates", J. Nanoparticle Res., vol. 5, 2003, pp. 17-30.
Tan et al., "High Aspect Ratio Microstructures on Porous Anodic Aluminum Oxide", IEEE, 1995, pp. 267-272.
Terai et al. "Newly developed RELACS process and materials for 65nm node device and beyond", Feb. 21, 2006; website: ieeexplore.ieee.org/iel5/10631/33565/01595193.pdf, pp. 20-21.
Tsukada et al., "Preparation and Application of Porous Silk Fibroin Materials", J. Appl. Polymer Sci., vol. 54, 1994, pp. 507-514.
Yasaitis et al., "A modular process for integrating thick polysilicon MEMS devices with submicron CMOS", Analog Devices, Pre-2004.

* cited by examiner

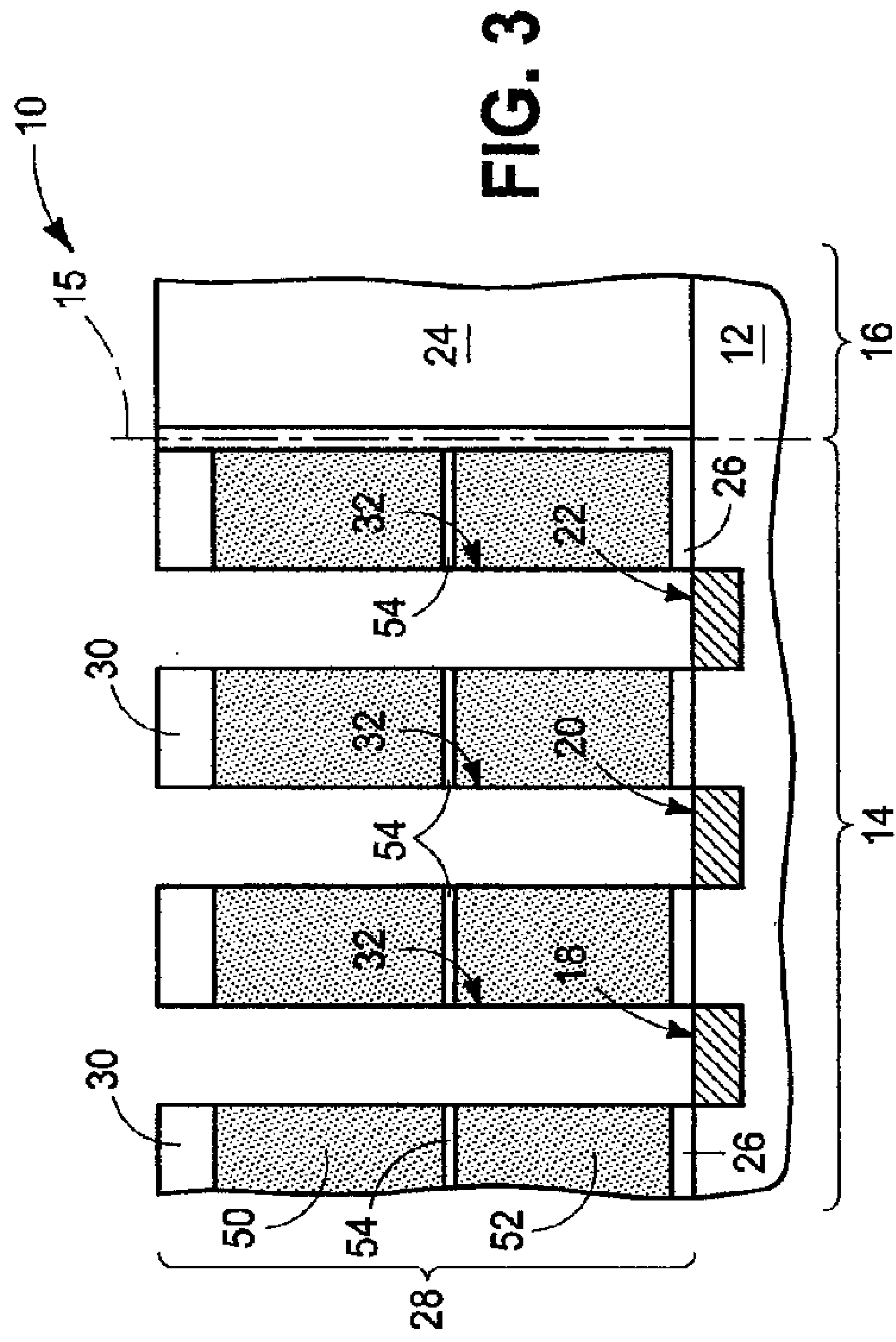


FIG. 3
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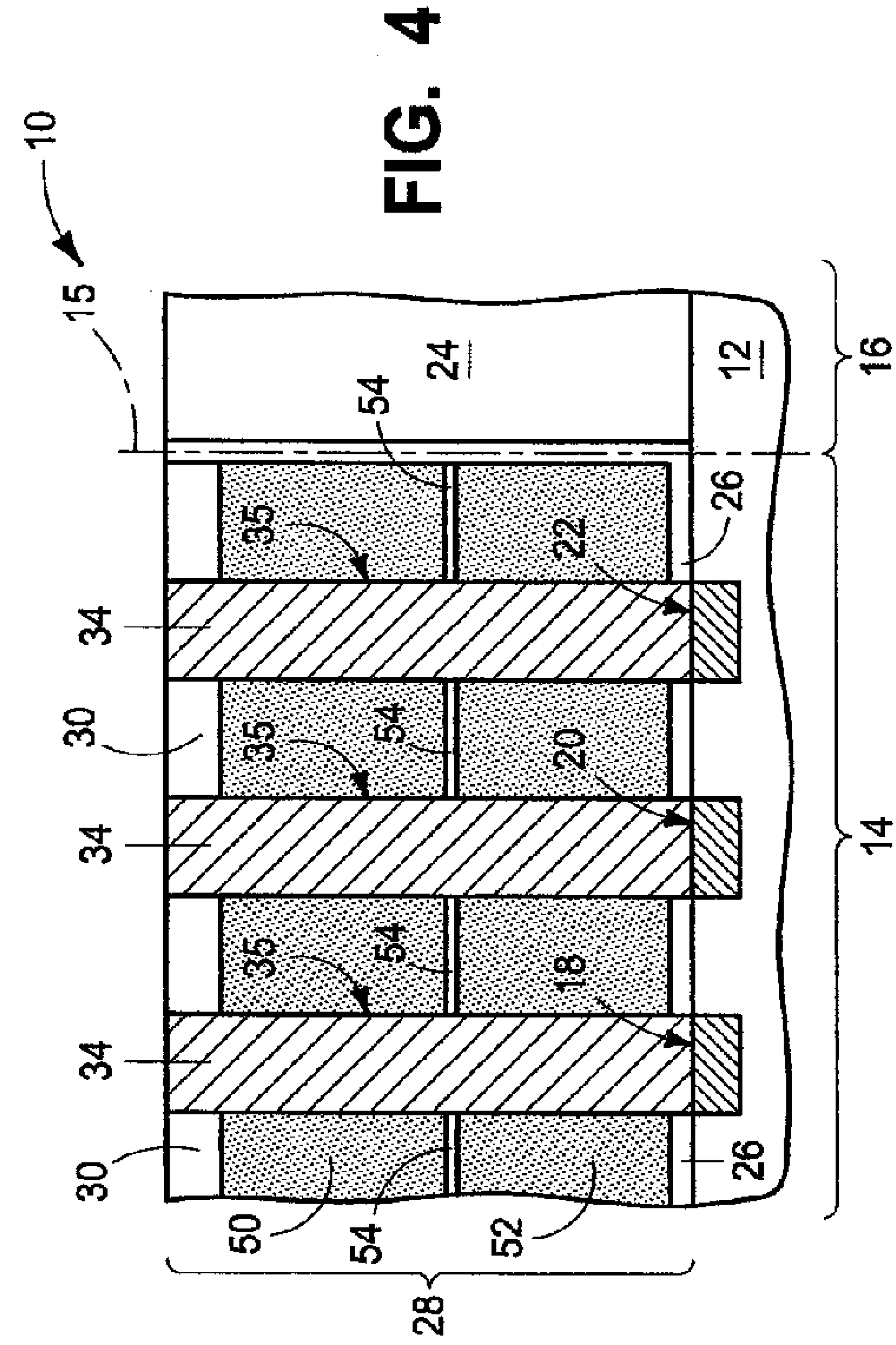
FIG. 4
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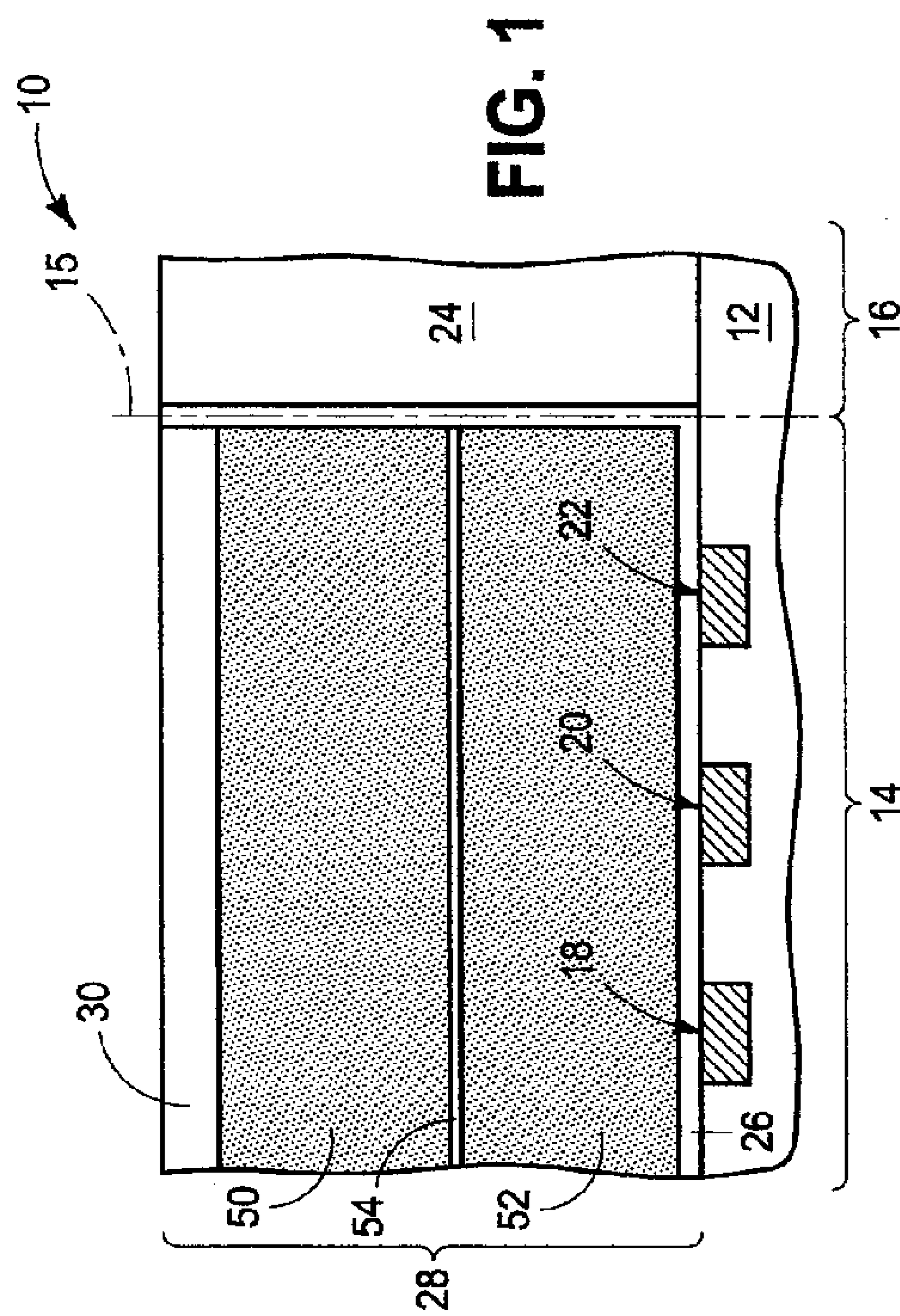
FIG. 1
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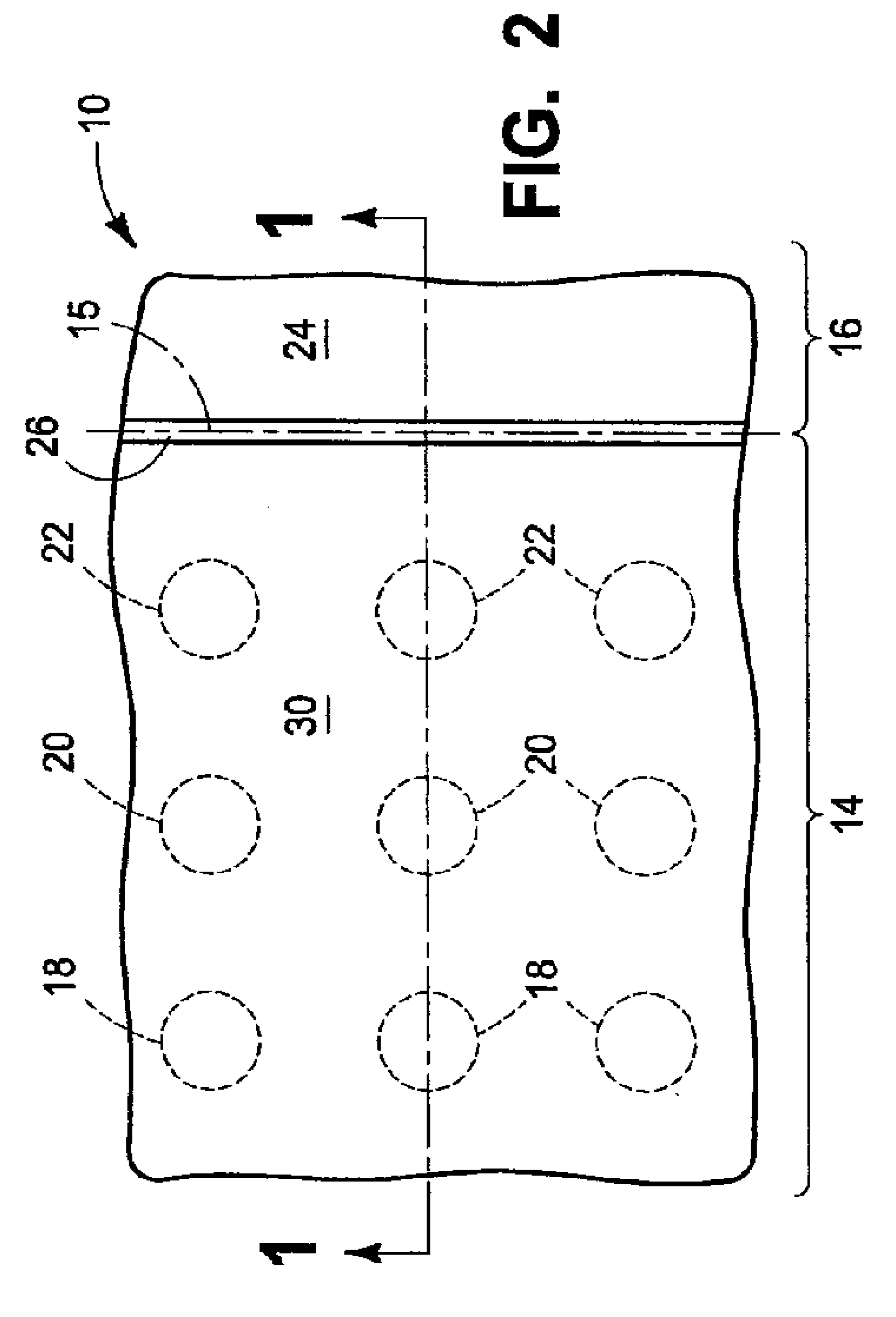
FIG. 2
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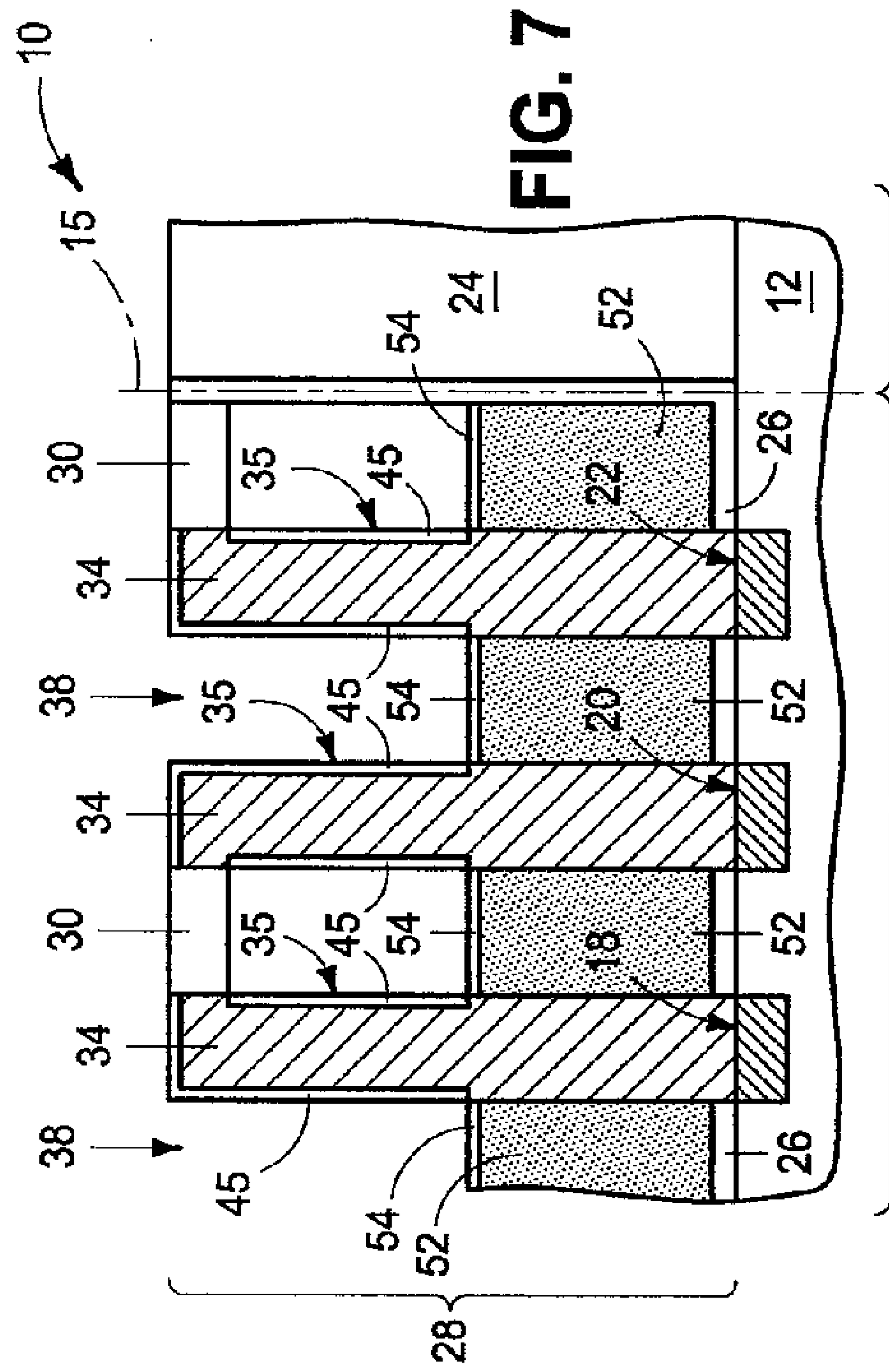
FIG. 7

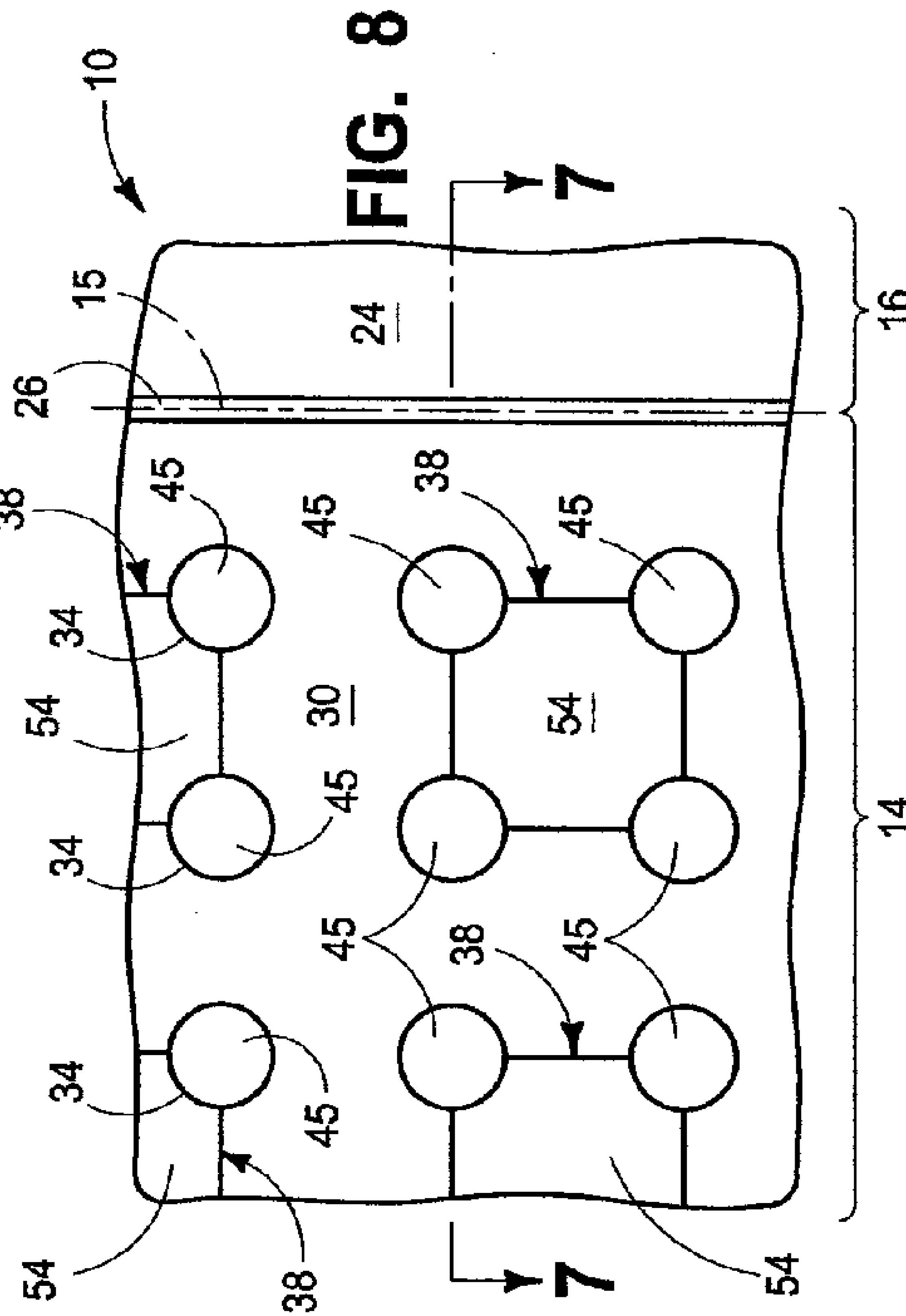
FIG. 8

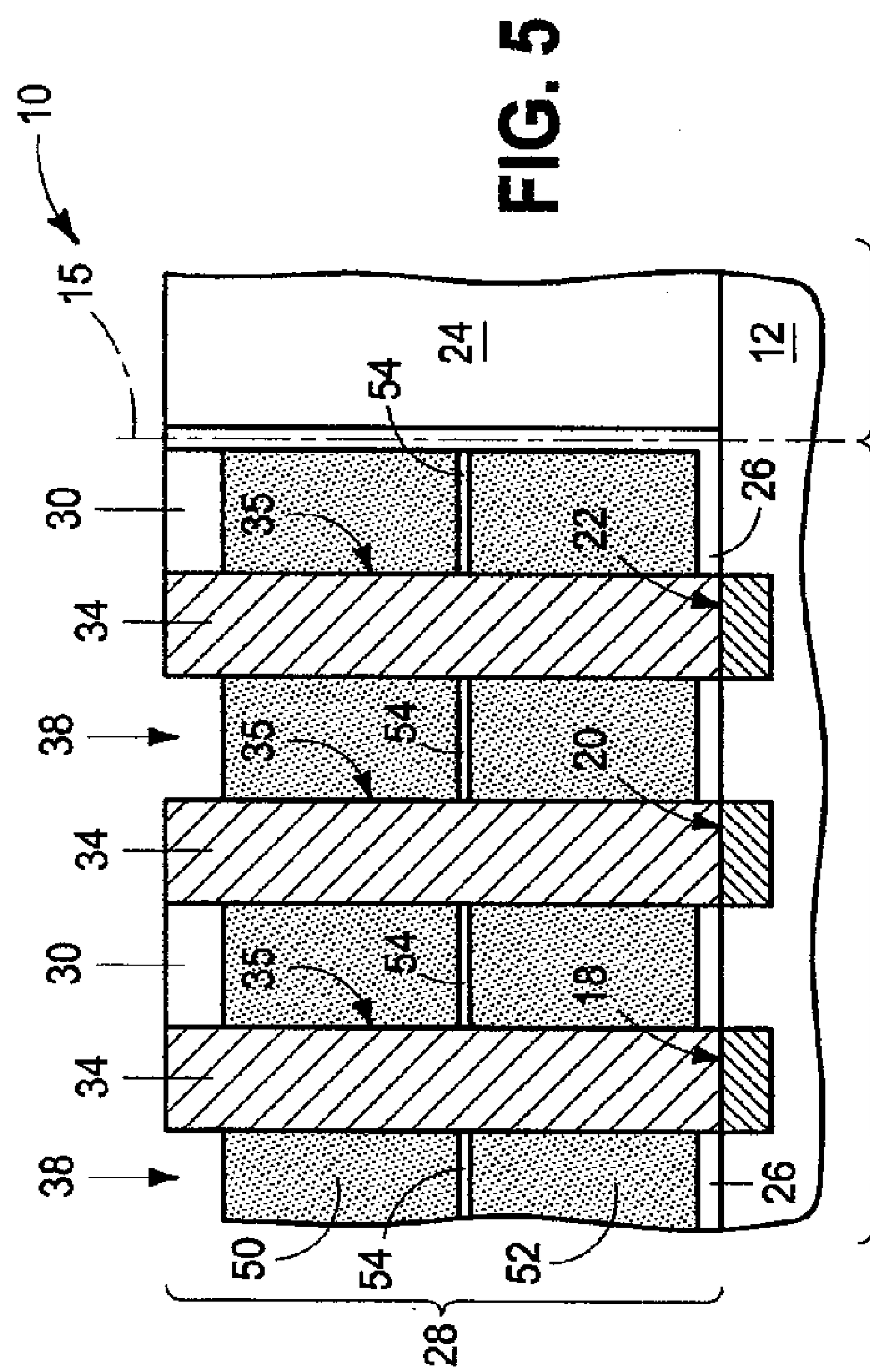
FIG. 5

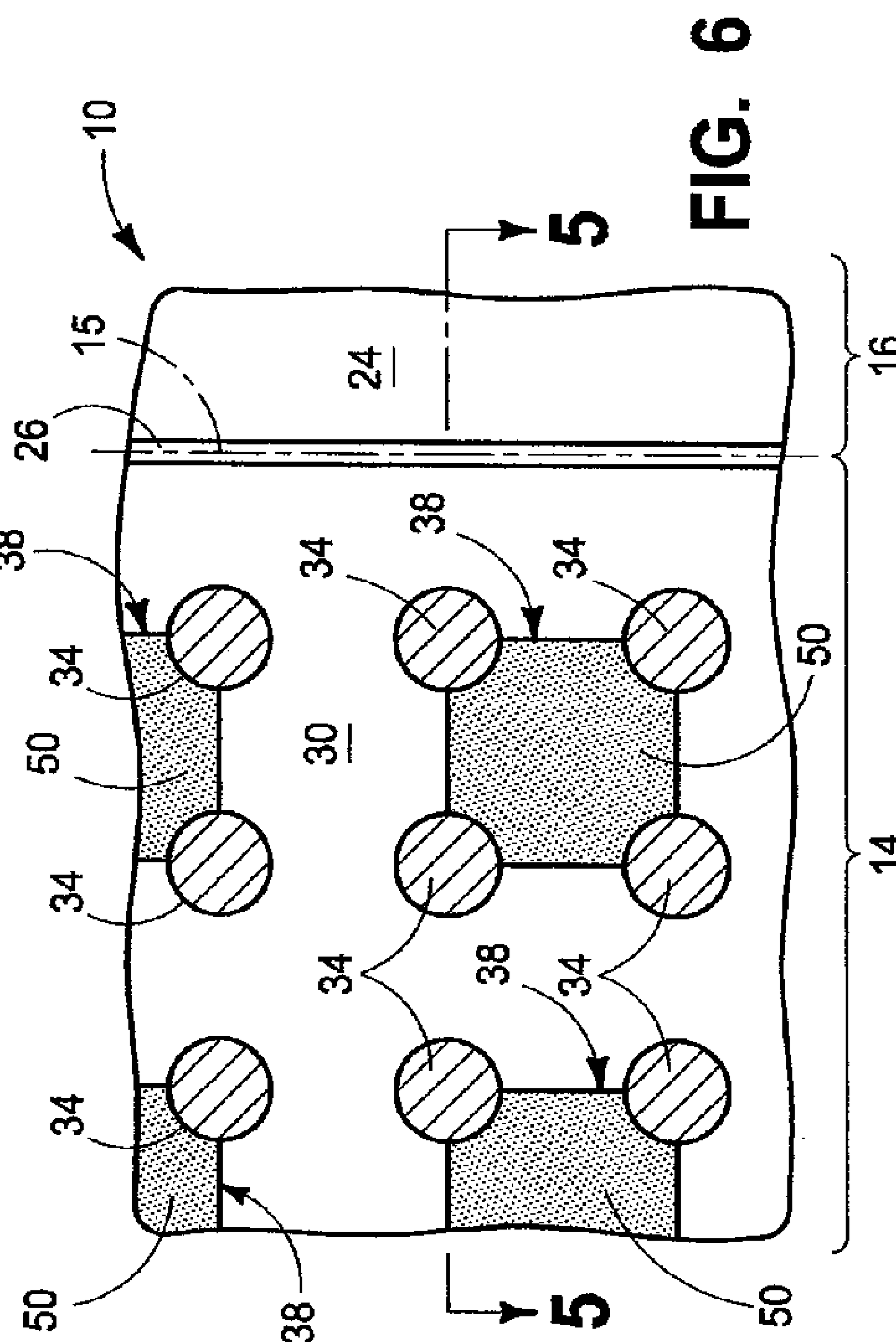
FIG. 6

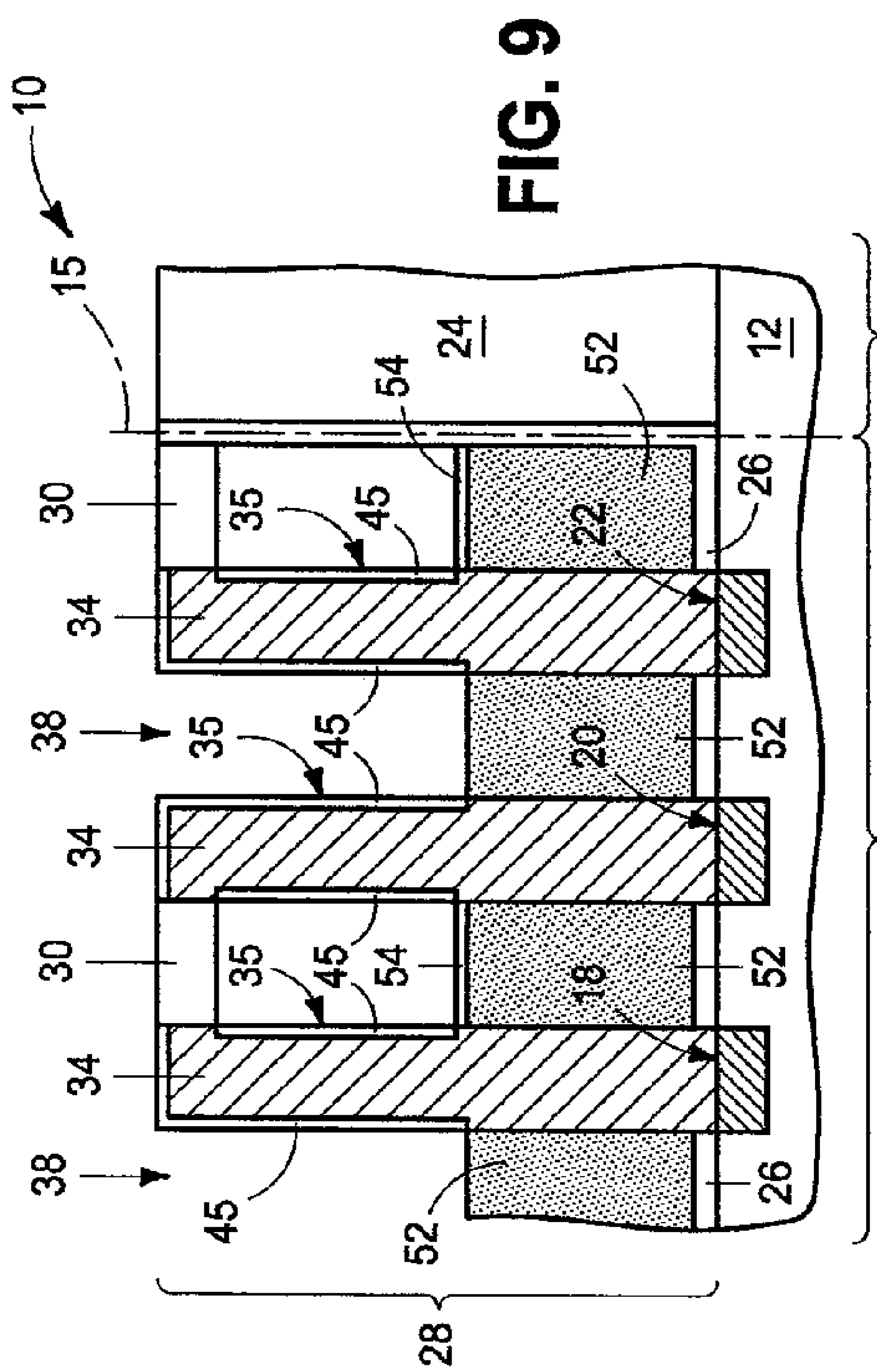

FIG. 9

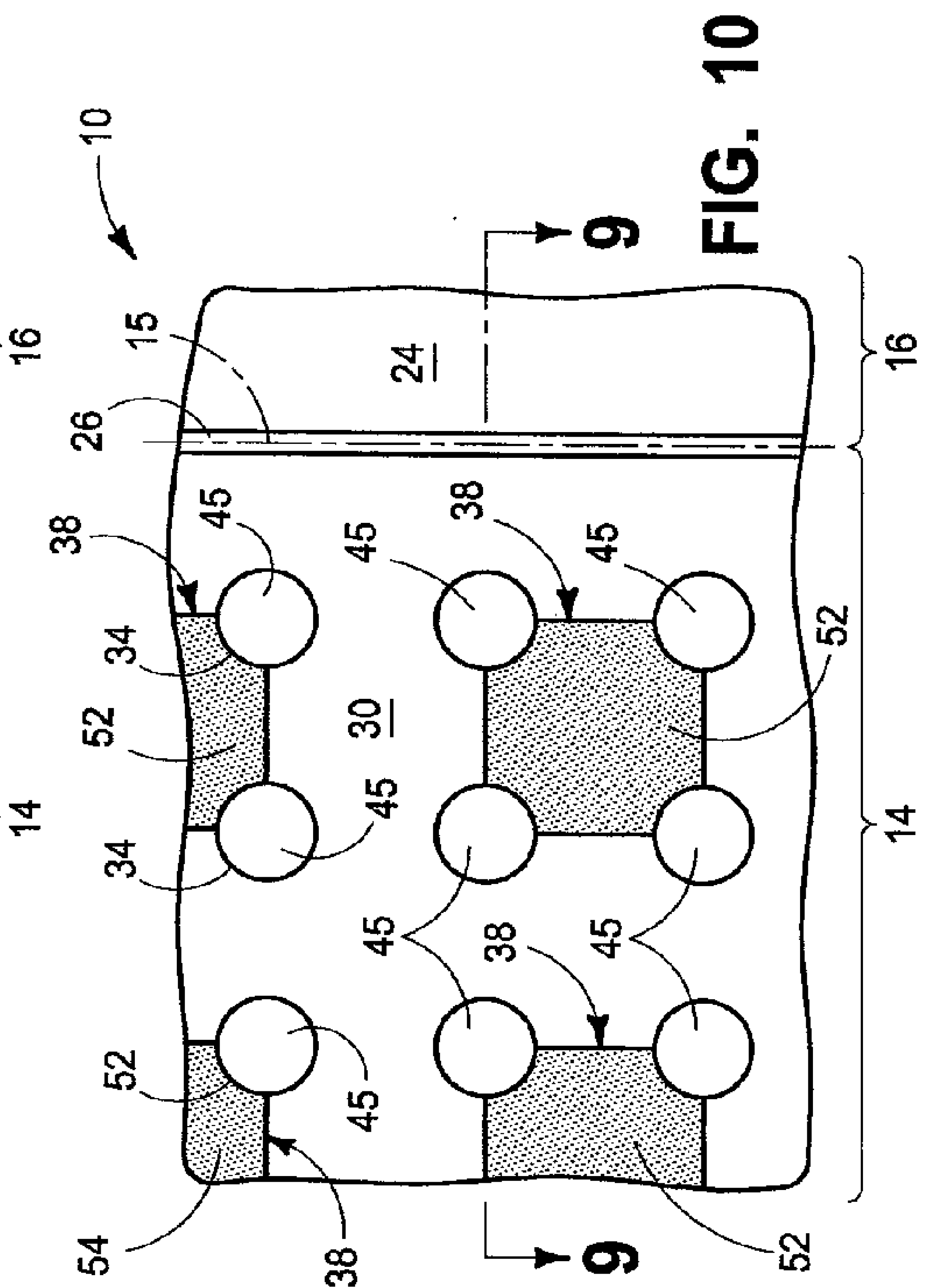

FIG. 10

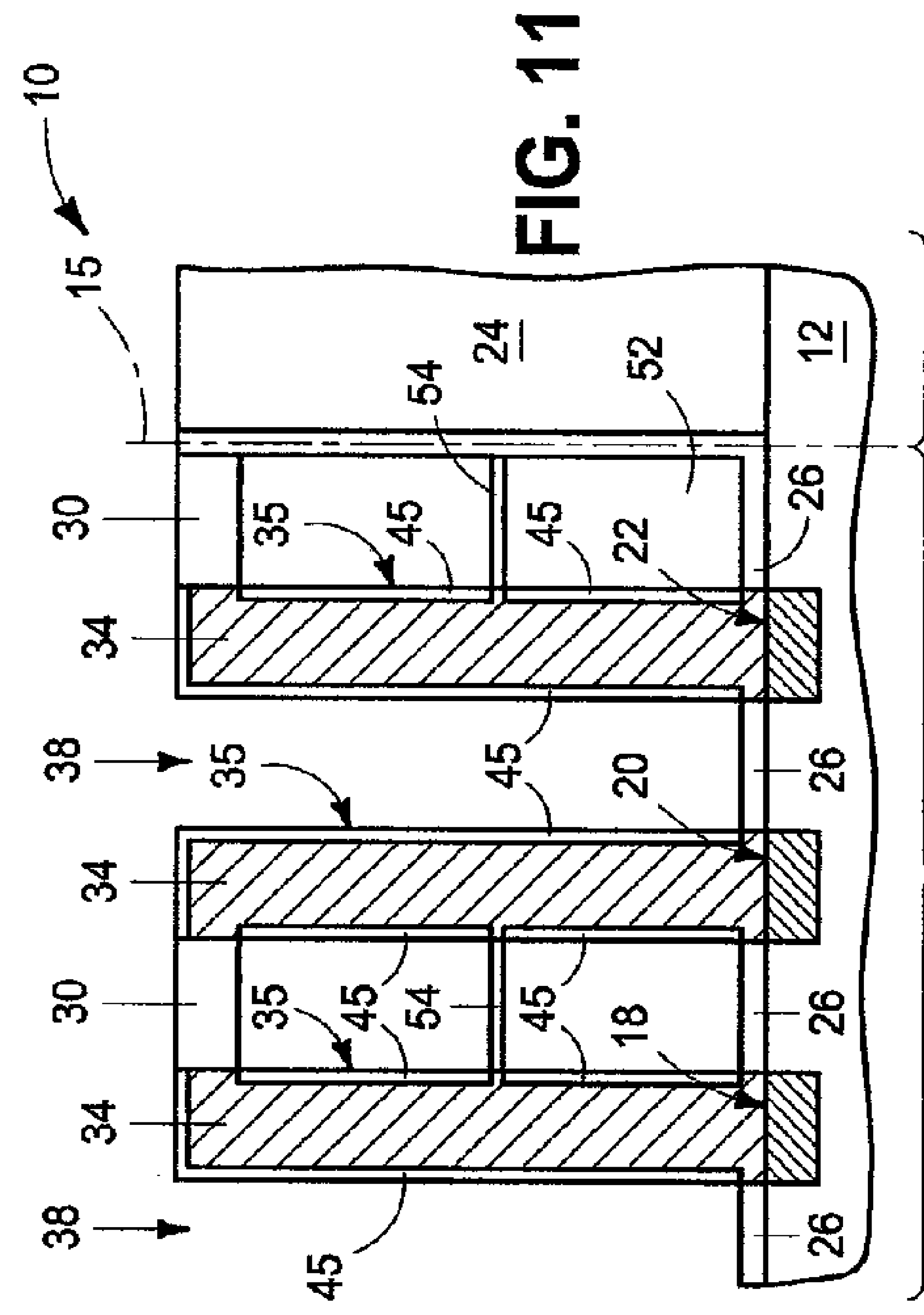

FIG. 11

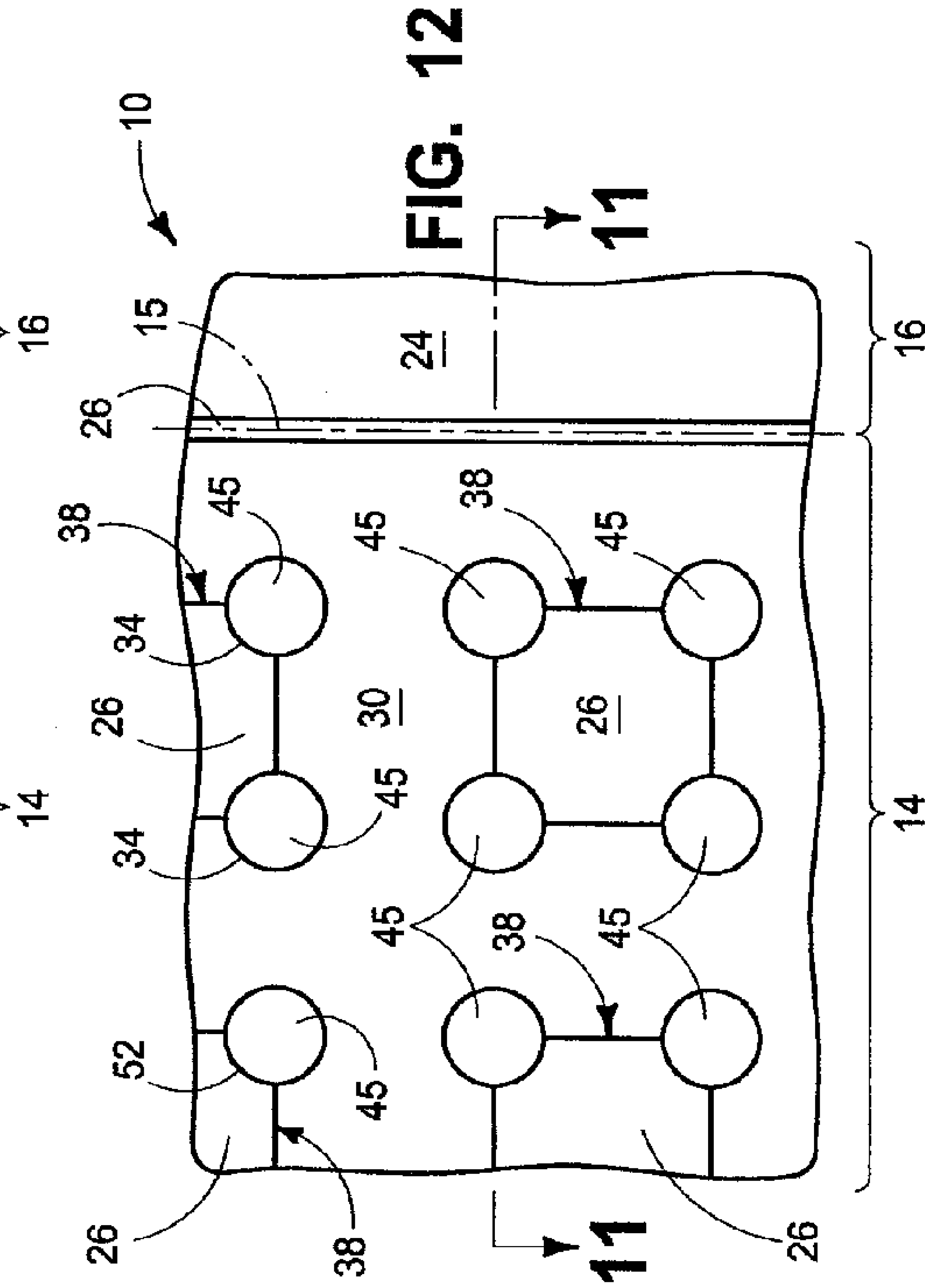

FIG. 12

FIG. 13

METHODS OF FORMING CAPACITORS

TECHNICAL FIELD

Embodiments disclosed herein pertain to methods of forming capacitors.

BACKGROUND

Capacitors are one type of component used in the fabrication of integrated circuits, for example in DRAM and other memory circuitry. A capacitor is comprised of two conductive electrodes separated by a non-conducting dielectric region. As integrated circuitry density has increased, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing capacitor area. The increase in density has typically resulted in greater reduction in the horizontal dimension of capacitors as compared to the vertical dimension. In many instances, the vertical dimension of capacitors has increased.

One manner of fabricating capacitors is to initially form an insulative material within which a capacitor storage electrode is formed. For example, an array of capacitor electrode openings for individual capacitors may be fabricated in an insulative support material, with an example material being silicon dioxide doped with one or both of phosphorus and boron. Openings within which some or all of the capacitors are formed are etched into the support material. It can be difficult to etch such openings through the support material, particularly where the openings are deep.

Further and regardless, it is often desirable to etch away most if not all of the capacitor electrode support material after individual capacitor electrodes have been formed within the openings. This enables outer sidewall surfaces of the electrodes to provide increased area and thereby increased capacitance for the capacitors being formed. However, capacitor electrodes formed in deep openings are often correspondingly much taller than they are wide. This can lead to toppling of the capacitor electrodes during etching to expose the outer sidewalls surfaces, during transport of the substrate, during deposition of the capacitor dielectric layer, and/or outer capacitor electrode layer. U.S. Pat. No. 6,667,502 teaches the provision of a brace or retaining structure intended to alleviate such toppling. Other aspects associated in the formation of a plurality of capacitors, some of which include bracing structures, have also been disclosed, such as in:

U.S. Pat. No. 7,067,385;
U.S. Pat. No. 7,125,781;
U.S. Pat. No. 7,199,005;
U.S. Pat. No. 7,202,127;
U.S. Pat. No. 7,387,939;
U.S. Pat. No. 7,439,152;
U.S. Pat. No. 7,517,753;
U.S. Pat. No. 7,544,563;
U.S. Pat. No. 7,557,013;
U.S. Pat. No. 7,557,015;
U.S. Patent Publication No. 2008/0090416;
U.S. Patent Publication No. 2008/0206950;
U.S. Pat. No. 7,320,911;
U.S. Pat. No. 7,682,924; and
U.S. Patent Publication No. 2010/0009512.

Fabrication of capacitors in memory circuitry may include forming an array of capacitors within a capacitor array area. Control or other circuitry area is often displaced from the

capacitor array area, and the substrate may include an intervening area between the capacitor array area and the control or other circuitry area.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic, cross-sectional view of a portion of a semiconductor substrate at a preliminary processing stage of an embodiment in accordance with the invention.

FIG. **2** is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. **1** along the line **1-1**.

FIG. **3** is a view of the FIG. **1** substrate at a processing stage subsequent to that of FIG. **1**.

FIG. **4** is a view of the FIG. **3** substrate at a processing stage subsequent to that of FIG. **3**.

FIG. **5** is a view of the FIG. **4** substrate at a processing stage subsequent to that of FIG. **4**.

FIG. **6** is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. **5** along the line **5-5**.

FIG. **7** is a view of the FIG. **5** substrate at a processing stage subsequent to that of FIG. **5**.

FIG. **8** is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. **7** along the line **7-7**.

FIG. **9** is a view of the FIG. **7** substrate at a processing stage subsequent to that of FIG. **7**.

FIG. **10** is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. **9** along the line **9-9**.

FIG. **11** is a view of the FIG. **9** substrate at a processing stage subsequent to that of FIG. **9**.

FIG. **12** is a diagrammatic top view of a portion of the semiconductor substrate comprising the cross-section shown in FIG. **11** along the line **11-11**.

FIG. **13** is a view of the FIG. **11** substrate at a processing stage subsequent to that of FIG. **11**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example methods of forming capacitors in accordance with embodiments of the invention are described with reference to FIGS. **1-13**. Referring initially to FIGS. **1** and **2**, a construction **10** is shown at a preliminary processing stage of an embodiment. Construction **10** includes a substrate **12** which may comprise semiconductive material. To aid in interpretation of the claims that follow, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Construction **10** may comprise a capacitor array area **14** and a peripheral circuitry area **16**. An interface line **15** has been used in the figures as an example interface of capacitor array area **14** and peripheral circuitry area **16**. Logic circuitry may be fabricated within peripheral circuitry area **16**. Control and/or other peripheral circuitry for operating a memory array may or may not be fully or partially within array area **14**, with an example memory array area **14** as a minimum encompassing all of the memory cells of a given memory array/sub-

memory array. Further, multiple sub-arrays may also be fabricated and operated independently, in tandem, or otherwise relative one another. As used herein, a "sub-array" or "sub-memory array" may be considered as an array. Various circuit devices (not shown) may be associated with peripheral circuitry area **16**, as well as with capacitor array area **14**, at the processing stage of FIGS. **1** and **2**.

Electrically conductive node locations **18**, **20**, and **22** are shown within memory array area **14**. Node locations **18**, **20**, and **22** may correspond to, for example, conductively-doped diffusion regions within a semiconductive material of substrate **12**, and/or to conductive pedestals associated with substrate **12**. Although the node locations are shown to be electrically conductive at the processing stage of FIG. **1**, the electrically conductive materials of the node locations could be provided at a processing stage subsequent to that of FIG. **1**. The node locations may ultimately be electrically connected with transistor or other constructions (not shown), may correspond to source/drain regions of transistor constructions, or may be ohmically connected to source/drain regions of transistor constructions. As alternate examples, the node locations may correspond to, connect to, or be parts of conductive interconnect lines. Regardless, as used herein, "node locations" refers to the elevationally outermost surfaces to which first capacitor electrodes electrically connect, for example as described below.

Dielectric material **24** may be over peripheral circuitry area **16**. Such may be homogenous or non-homogenous, with doped silicon dioxide such as phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG) being examples. Dielectric material **24** may be formed by blanket deposition over substrate **12**, and then removed by subtractive patterning from array circuitry area **14**. An example thickness range for dielectric material **24** is about 0.5 micron to about 3 microns.

A support material **28** has been formed elevationally over substrate **12** within capacitor array area **14**. In one embodiment, support material **28** may be directly against node locations **18**, **20**, and **22**. In this document, a material or structure is "directly against" another when there is at least some physical touching contact of the stated materials or structures relative one another. In contrast, "over", "on", and "against" not proceeded by "directly", encompass "directly against" as well as constructions where intervening material(s) or structure(s) result(s) in no physical touching contact of the stated materials or structures relative one another. Support material **28** may be homogenous or non-homogenous, and may be any one or more of dielectric, conductive, or semiconductive. For example, support material **28** may be a single homogenous layer of a dielectric, conductive or semiconductive material; multiple layers of a single homogenous dielectric, conductive, or semiconductive material; or multiple layers of differing compositions of dielectric, conductive, and or semiconductive materials. An example thickness for support material **28** is about 0.25 micron to about 3 microns.

FIGS. **1** and **2** show support material **28** as comprising covering material **30**, an elevationally outer material **50**, an elevationally inner material **52**, an elevationally intermediate material **54** between materials **50** and **52**, and dielectric material **26**. Each may be homogenous or non-homogenous. Covering material **30** and intermediate material **54** are of different composition from composition of outer material **50** and inner material **52**. Covering material **30** and intermediate material **54** may be of the same or different composition relative each other, and regardless are ideally dielectric when remaining as part of the finished circuitry construction. Example materials include one or both of silicon nitride and silicon dioxide. An example thickness for covering material **30** is about 600 Angstroms to about 1,500 Angstroms, with that for intermediate material **54** being about 50 Angstroms to about 600 Angstroms. Elevationally outer material **50** and elevationally inner material **52** may be of the same or different composition relative each other. Example materials include one or more of doped or undoped silicon, carbon, polyimide, and oxide, with an ideal example being polysilicon. An example thickness for outer material **50** is about 500 Angstroms to about 1,000 Angstroms, with that for inner material **54** being about 1,000 Angstroms to about 8,000 Angstroms. Examples for dielectric material **26** are one or both of silicon nitride and undoped silicon dioxide. An example thickness range for dielectric material **26** is about 50 Angstroms to about 300 Angstroms. Regardless, multiple intermediate materials **54** (e.g., that are elevationally spaced from one another) may be used (not shown).

Referring to FIG. **3**, individual capacitor openings **32** have been formed through covering material **30**, outer material **50**, intermediate material **54**, elevationally inner material **52**, and dielectric material **26** to node locations **18**, **20**, and **22**. An example technique for forming openings **32** includes photolithographic patterning and anisotropic etch. Multiple etching chemistries may be used for etching material(s) **28** as selected by the artisan. An example for anisotropically etching silicon nitride includes plasma etching using an inductively coupled plasma reactor with about 700 W to 900 W top power, about 250V to 450V chuck bias, chamber pressure about 6 mTorr to 20 mTorr, substrate temperature about 25° C. to 45° C., CH_2F_2 flow about 15 sccm to 35 sccm, and CF_4 flow about 75 sccm to 125 sccm. An example for anisotropically etching doped or undoped polysilicon includes NF_3:O_2:HBr at a volumetric ratio of 1:1:3 to 5. Alternate examples for anisotropically etching polysilicon include substituting SF_6 or Cl_2 for the NF_3, and in such events providing an alternate volumetric ratio of 1:1:1.

Referring to FIG. **4**, a first capacitor electrode **34** has been formed within individual openings **32** in support material **28** in conductive electrical connection with respective node locations **18**, **20**, and **22**. First capacitor electrodes **34** may be homogenous or non-homogenous, and may be of any suitable shape(s) with a solid pillar-like shape being shown. As an alternate example, the first capacitor electrodes may be in the shape of upwardly open containers. First capacitor electrodes **34** may be formed by depositing one or more conductive materials to overfill openings **32**, followed by planarizing the conductive material back at least to the outermost surface of covering material **30**. Example conductive materials are one or combinations of titanium, titanium nitride, and ruthenium. First capacitor electrodes may be considered as comprising sidewalls **35**.

Referring to FIGS. **5** and **6**, openings **38** have been formed through covering material **30**, for example by anisotropic etching, to expose support material **28**. In one embodiment, a mask (not shown) over covering material **30** and first capacitor electrodes **34** may be used as an etch mask during such anisotropic etching, with such a mask having openings the shape of openings **38**. That mask may be everywhere spaced elevationally from covering material **30** and capacitor electrodes **34**, or may comprise one or more materials (i.e., photosensitive, hard-mask, and/or antireflective materials) deposited over covering material **30** and capacitor electrodes **34**. Regardless, an example mask thickness is about 1,000 Angstroms to about 10,000 Angstroms.

Referring to FIGS. **7** and **8**, outer material **50** (not shown) has been dry isotropically etched from being over capacitor electrode **34**, and in one embodiment as shown from being over intermediate material **54**. The etching of outer material

50 is conducted selectively relative to capacitor electrode 34, and in one embodiment selectively relative to intermediate material 54, in one embodiment selectively relative to covering material 30. In the context of this document, a selective etch requires removal of one material relative to a stated another material at a removal rate of at least 2:1. In one embodiment, the dry isotropic etching of material 50 uses plasma. In one embodiment, no wet etching is used in removing any of outer material 50. In one embodiment and as shown, all of outer material 50 is removed. In one embodiment, a mask used in forming openings 38 through covering material 30 remains over the substrate during etching of outer material 50 (not shown).

In one embodiment where outer material 50 comprises polysilicon and capacitor electrodes 34 comprise TiN, the dry isotropic etching of outer material 50 comprises plasma etching using a sulphur and fluorine-comprising chemistry. The sulfur and fluorine-comprising chemistry may be derived from a single compound (e.g., SF_6) and/or from multiple compounds (e.g. COS, SO_2, H_2S, NF_3, and F_2). In one embodiment, the etching is conducted at a pressure of at least about 150 mTorr and in one embodiment at a pressure of at least about 200 mTorr. In one embodiment, the etching is conducted at a substrate temperature of no greater than about 30° C., in one embodiment at no greater than 10° C., and in one embodiment at no greater than 0° C. Ideal results may be achieved at higher pressure and lower temperature (i.e., at least 200 mTorr and no greater than 10° C.). In one embodiment, the etching chemistry is derived from gas comprising SF_6, and with or without one or more inert gases.

An example first set of etching conditions in an inductively coupled plasma reactor for etching polysilicon-comprising support material selectively relative to TiN-comprising first capacitor electrodes includes about 700 W to 900 W top power, 0V to about 20V chuck bias, chamber pressure about 150 mTorr to 250 mTorr, substrate temperature about −10° C. to 40° C., SF_6 flow about 200 sccm to 400 sccm, NF_3 flow about 40 sccm to 60 sccm, and He and/or Ar flow 0 sccm to about 350 sccm. An example second set of etching conditions for etching polysilicon-comprising support material selectively relative to TiN-comprising first capacitor electrodes includes about 1,000 W to 2,000 W top power, 0V to about 20V chuck bias, chamber pressure about 150 mTorr to 250 mTorr, substrate temperature about −10° C. to 30° C., SF_6 flow about 50 sccm to 900 sccm, and He and/or Ar flow about 300 sccm to 1500 sccm. Use of SF_6 solely as the contributor to reactive species formation may provide better etch selectivity relative to TiN and Si_3N_4 in comparison to combining SF_6 and NF_3, but more etch residue.

In one embodiment, the etching of polysilicon-comprising support material selectively relative to TiN-comprising first capacitor electrodes includes a plurality of sulphur and fluorine-comprising etching steps individually separated by a hydrogen treating step. In one embodiment, the hydrogen treating steps are conducted at lower pressure than are the sulphur and fluorine-comprising etching steps. In one embodiment, the hydrogen treating steps are individually longer than are individual of the sulphur and fluorine-comprising etching steps. In one embodiment, the hydrogen treating and the etching steps are each conducted using plasma. In one embodiment, a hydrogen-containing plasma is used in the hydrogen treating step and is derived from gas consisting essentially of H_2. An example set of hydrogen treating conditions in an inductively coupled plasma reactor includes about 800 W to 5,000 W top power, 0V to about 20V chuck bias, chamber pressure about 40 mTorr to 250 mTorr, substrate temperature about −10° C. to 30° C., H_2 flow about 200 sccm to 1,200 sccm, and He and/or Ar flow 0 sccm to about 1500 sccm. An example time period for individual etching steps is about 2 seconds to 6 seconds, and that for individual hydrogen treating steps about 8 seconds to 10 seconds. Hydrogen treating may be conducted to remove residue, if any, that might result from the act of etching with a sulphur and fluorine-comprising etching chemistry.

In one embodiment and as shown, TiF 45 is formed on first capacitor electrode sidewalls 35 from Ti of the TiN of first capacitor electrodes 34 and from fluorine of the sulfur and fluorine-comprising etching chemistry. In one embodiment, TiF is formed to a thickness that is self-limited in spite of further exposure of capacitor electrodes 34 to the sulphur and fluorine-comprising etching chemistry. Such an example self-limited thickness is about 10 Angstroms. Regardless, TiF is electrically conductive but not as much as TiN.

In one embodiment of a method of forming capacitors, polysilicon-comprising support material is dry isotropically etched selectively relative to TiN-comprising first capacitor electrodes using a sulphur and fluorine-comprising etching chemistry regardless of presence of covering material 30, intermediate material 54, and/or dielectric material 26. Any other attribute as described above may be used. In one embodiment of a method of forming capacitors, polysilicon-comprising support material is dry isotropically etched using a fluorine-comprising etching chemistry that combines Ti of the TiN of the capacitor electrodes with fluorine of the etching chemistry to form TiF on sidewalls of the first capacitor electrodes. In one embodiment, the etching chemistry comprises S. In one embodiment, the etching is conducted selectively relative to the TiN-comprising first capacitor electrodes. Any other attribute as described above may be used.

Referring to FIGS. 9 and 10, openings 38 have been anisotropically etched through intermediate material 54 to expose inner material 52 using covering material 30 having openings 38 therein as an etch mask. The etching of openings 38 through intermediate material 54 is conducted selectively relative to first capacitor electrodes 34, and in one embodiment selectively relative to covering material 30. In one embodiment, such etching is conducted using plasma. Where, for example, intermediate material 54 comprises silicon nitride, the same example etching conditions described above for etching openings 38 through covering material 30 may be used. In one embodiment, a mask used in forming openings 38 through covering material 30 remains over the substrate during anisotropic etching of intermediate material 54. Such may enable ions in a plasma etching to achieve better directionality. For example, areas bombarded by etching ions may achieve better removal rate than shadowed/off-axis areas in comparison to plasma etching conducted where the mask does not remain over the substrate during the etching.

Referring to FIGS. 11 and 12, inner material 52 (not shown) has been etched through openings 38 in intermediate material 54. The etching of inner material 52 has been conducted selectively relative to first capacitor electrodes 34, in one embodiment selective relative to covering material 30, in one embodiment selective relative to intermediate material 54, and in one embodiment selectively relative to dielectric material 26. In one embodiment, such etching has been conducted isotropically, and in one embodiment comprises dry plasma etching. In one embodiment, most if not all of inner material 52 is removed, with all of such shown as having been removed in FIGS. 11 and 12. Where dry isotropic etching conditions are used, such conditions/chemistry may be the same or different from that used in the dry isotropic etching of outer material 50. In one embodiment during the etching of inner material 52, TiF 45 may be formed on first capacitor

electrode sidewalls **35** from Ti of the TiN and from fluorine of the sulphur and fluorine-comprising etching chemistry.

Referring to FIG. **13**, a capacitor dielectric **44** is provided over sidewalls **35** of first capacitor electrodes **34**. Such may be homogenous or non-homogenous. A second capacitor electrode **46** is formed over capacitor dielectric **44**, thereby forming individual capacitors **48**. Second capacitor electrode **46** may be homogenous or non-homogenous, and may be of the same composition or of different composition from that of first capacitor electrodes **34**. Second capacitor electrode **46** is shown as being a single capacitor electrode common to the individual capacitors, although separate or other multiple second capacitor electrodes may be used. Likewise, capacitor dielectric **44** may be continuously or discontinuously received over multiple first capacitor electrodes **34**.

Appropriate circuitry (not shown) would be associated with capacitor electrodes **46** and **34** of capacitors **48** to enable selective operation of individual capacitors **48**. This other circuitry is not material to embodiments of this invention, and may be existing or later-developed circuitry within the skill of the artisan.

CONCLUSION

In some embodiments, a method of forming capacitors comprises providing first capacitor electrodes within support material. The first capacitor electrodes comprise TiN and the support material comprises polysilicon. The polysilicon-comprising support material is dry isotropically etched selectively relative to the TiN-comprising first capacitor electrodes using a sulfur and fluorine-containing etching chemistry. A capacitor dielectric is formed over sidewalls of the first capacitor electrodes and a second capacitor electrode is formed over the capacitor dielectric.

In some embodiments, a method of forming capacitors comprises providing first capacitor electrodes within support material. The first capacitor electrodes comprise TiN and the support material comprises polysilicon. The polysilicon-comprising support material is dry isotropically etched using a fluorine-comprising etching chemistry that combines with Ti of the TiN to form TiF on sidewalls of the first capacitor electrodes. A capacitor dielectric is formed over the TiF of the first capacitor electrodes and a second capacitor electrode is formed over the capacitor dielectric.

In some embodiments, a method of forming capacitors comprises providing first capacitor electrodes within support material. The support material comprises an elevationally outer material, an elevationally inner material, an elevationally intermediate material between the outer and inner materials, and a covering material over the outer material. The covering material and the intermediate material are of different composition from composition of the outer and inner materials. Openings are formed through the covering material to expose the outer material. The outer material is dry isotropically etched from being over the first capacitor electrodes and the intermediate material. The etching of the outer material is conducted selectively relative to the first capacitor electrodes and the intermediate material. Openings are anisotropically etched through the intermediate material to expose the inner material using the covering material with openings therein as an etch mask. The etching of openings through the intermediate material is conducted selectively relative to the first capacitor electrodes. The inner material is etched through the openings in the intermediate material. The etching of the inner material is conducted selectively relative to the first capacitor electrodes. A capacitor dielectric is formed over sidewalls of the first capacitor electrodes and a second capacitor electrode is formed over the capacitor dielectric.

In some embodiments, a method of forming capacitors comprises providing first capacitor electrodes comprising TiN within support material. The support material comprises an elevationally outer material comprising polysilicon, an elevationally inner material comprising poly silicon, an elevationally intermediate material between the outer and inner materials, and a covering material over the outer material. The covering material and the intermediate material are of different composition from composition of the outer and inner materials. Openings are anisotropically etched through the covering material to expose the outer material. The polysilicon-comprising outer material is dry isotropically plasma etched from being over the first capacitor electrodes and the intermediate material. The etching of the outer material is conducted selectively relative to the covering material, the first capacitor electrodes, and the intermediate material. The etching of the polysilicon-comprising outer material is conducted with a sulfur and fluorine-comprising etching chemistry, at a pressure of at least about 150 mTorr, and at a substrate temperature of no greater than about 10° C. The etching of the polysilicon-comprising outer material includes a plurality of sulfur and fluorine-comprising plasma etching steps individually separated by a hydrogen-plasma treating step. Openings are anisotropically plasma etched through the intermediate material to expose the inner material using the covering material with openings therein as an etch mask. The etching of openings through the intermediate material is conducted selectively relative to the first capacitor electrodes and the covering material. The polysilicon-comprising inner material is dry isotropically plasma etched through the openings in the intermediate material. The etching of the polysilicon-comprising inner material is conducted selectively relative to the covering material, the first capacitor electrodes, and the intermediate material, and removes at least most of the inner material. The etching of the polysilicon-comprising inner material is conducted with a sulfur and fluorine-comprising etching chemistry, at a pressure of at least about 150 mTorr, and at a substrate temperature of no greater than about 10° C. The etching of the polysilicon-comprising inner material includes a plurality of sulfur and fluorine-comprising plasma etching steps individually separated by a hydrogen-plasma treating step. A capacitor dielectric is formed over sidewalls of the first capacitor electrodes and a second capacitor electrode is formed over the capacitor dielectric.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. A method of forming capacitors, comprising:

providing first capacitor electrodes within support material; the support material comprising an elevationally outer material, an elevationally inner material, an elevationally intermediate material between the outer and inner materials, and a covering material over the outer material; the covering material and the intermediate material being of different composition from composition of the outer and inner materials;

forming openings through the covering material to expose the outer material;

dry isotropically etching the outer material from being over the first capacitor electrodes and the intermediate material, the etching of the outer material being conducted selectively relative to the first capacitor electrodes and the intermediate material;

anisotropically etching openings through the intermediate material to expose the inner material using the covering material with openings therein as an etch mask, the etching of openings through the intermediate material being conducted selectively relative to the first capacitor electrodes;

etching the inner material through the openings in the intermediate material, the etching of the inner material being conducted selectively relative to the first capacitor electrodes; and

forming a capacitor dielectric over sidewalls of the first capacitor electrodes and forming a second capacitor electrode over the capacitor dielectric.

2. The method of claim **1** comprising conducting the etching of the outer material selectively relative to the covering material.

3. The method of claim **1** comprising conducting the etching of the intermediate material selectively relative to the covering material.

4. The method of claim **1** comprising conducting the etching of the inner material selectively relative to the covering material.

5. The method of claim **1** comprising conducting the etching of the inner material selectively relative to the intermediate material.

6. The method of claim **1** comprising conducting the etching of the inner material selectively relative to the covering material and the intermediate material.

7. The method of claim **1** wherein the etching of the inner material is dry and isotropic.

8. The method of claim **7** wherein the isotropic etching of the inner material removes at least most of the inner material.

9. The method of claim **7** wherein the outer material comprises polysilicon, the capacitor electrodes comprise TiN, and the etching of the outer material comprises plasma etching using a sulfur and fluorine-comprising chemistry.

10. The method of claim **9** wherein the etching is conducted at a pressure of at least about 200 mTorr and at a substrate temperature of no greater than about 10° C.

11. The method of claim **9** wherein the etching includes a plurality of sulfur and fluorine-comprising etching steps individually separated by a hydrogen treating step.

12. The method of claim **9** wherein the etching removes all of the polysilicon-comprising outer material.

13. A method of forming capacitors, comprising:

providing first capacitor electrodes comprising TiN within support material; the support material comprising an elevationally outer material comprising polysilicon, an elevationally inner material comprising polysilicon, an elevationally intermediate material between the outer and inner materials, and a covering material over the outer material; the covering material and the intermediate material being of different composition from composition of the outer and inner materials;

anisotropically etching openings through the covering material to expose the outer material;

dry isotropically plasma etching the polysilicon-comprising outer material from being over the first capacitor electrodes and the intermediate material; the etching of the outer material being conducted selectively relative to the covering material, the first capacitor electrodes, and the intermediate material; the etching of the polysilicon-comprising outer material being conducted with a sulfur and fluorine-comprising etching chemistry, at a pressure of at least about 150 mTorr, and at a substrate temperature of no greater than about 10° C.; the etching of the polysilicon-comprising outer material including a plurality of sulfur and fluorine-comprising plasma etching steps individually separated by a hydrogen-plasma treating step;

anisotropically plasma etching openings through the intermediate material to expose the inner material using the covering material with openings therein as an etch mask, the etching of openings through the intermediate material being conducted selectively relative to the first capacitor electrodes and the covering material;

dry isotropically plasma etching the polysilicon-comprising inner material through the openings in the intermediate material; the etching of the polysilicon-comprising inner material being conducted selectively relative to the covering material, the first capacitor electrodes, and the intermediate material and removing at least most of the inner material; the etching of the polysilicon-comprising inner material being conducted with a sulfur and fluorine-comprising etching chemistry, at a pressure of at least about 150 mTorr, and at a substrate temperature of no greater than about 10° C.; the etching of the polysilicon-comprising inner material including a plurality of sulfur and fluorine-comprising plasma etching steps individually separated by a hydrogen-plasma treating step; and

forming a capacitor dielectric over sidewalls of the first capacitor electrodes and forming a second capacitor electrode over the capacitor dielectric.

14. The method of claim **13** comprising:

during the etching of the polysilicon-comprising outer material, forming TiF on the first capacitor electrode sidewalls from Ti of the TiN and from fluorine of the sulfur and fluorine-comprising etching chemistry; and

during the etching of the polysilicon-comprising inner material, forming TiF on the first capacitor electrode sidewalls from Ti of the TiN and from fluorine of the sulfur and fluorine-comprising etching chemistry.

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