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(57) **ABSTRACT**

An integrated circuit (IC) current sensor that self-calibrates to adjust its signal gain when employed in a current divider configuration is presented. The current sensor includes an integrated current conductor, a magnetic field transducer, a controllable gain stage and a calibration controller. The integrated current conductor is adapted to receive a portion of a calibration current. The calibration current corresponds to a full scale current. The magnetic field transducer, responsive to the calibration current portion, provides a magnetic field signal having a magnitude proportional to a magnetic field generated by the calibration current portion. The controllable gain stage is configured to amplify the magnetic field signal with an adjustable gain to provide an amplified magnetic field signal. The calibration controller is responsive to a calibration command signal to adjust the adjustable gain of the controllable gain stage to a calibrated gain in order to provide the amplified magnetic field signal at a predetermined voltage level that corresponds to a desired current sensor output signal voltage level if the full scale current were received by the integrated current conductor.

20 Claims, 8 Drawing Sheets

The diagram illustrates a magnetic field sensor system 50. It features a Hall SE 54 connected to inputs 18a, 18b, 18c, and 18d. The system includes a Dynamic Offset Cancellation block 66, a Sensitivity Temp. Coefficient Trim block 72, a Sensitivity Trim block 70, an Amp block 68, a Low Pass Filter block 74, a Sensing Interface Stage block 82, a Calibration Controller block 84, a Controllable Gain Stage block 86, and an Output Stage block 56. The system is powered by VCC 18c and Vcal 18g. The diagram shows the internal components and their interconnections, including a Current Drive 106 and a Calibration Control Stage 86. The system has inputs 18a, 18b, 18c, 18d and outputs 18f, 18h.

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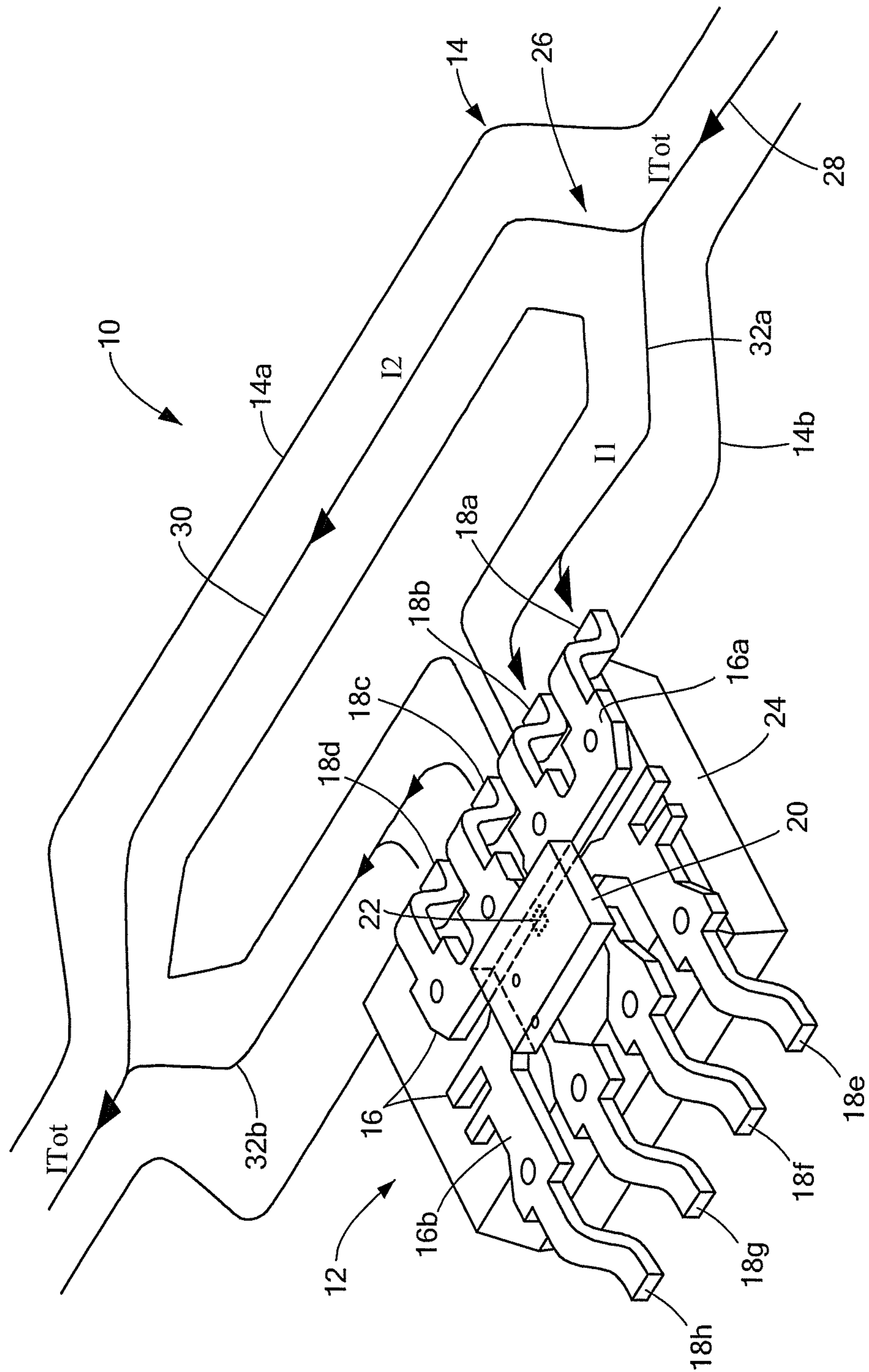


FIG. 1

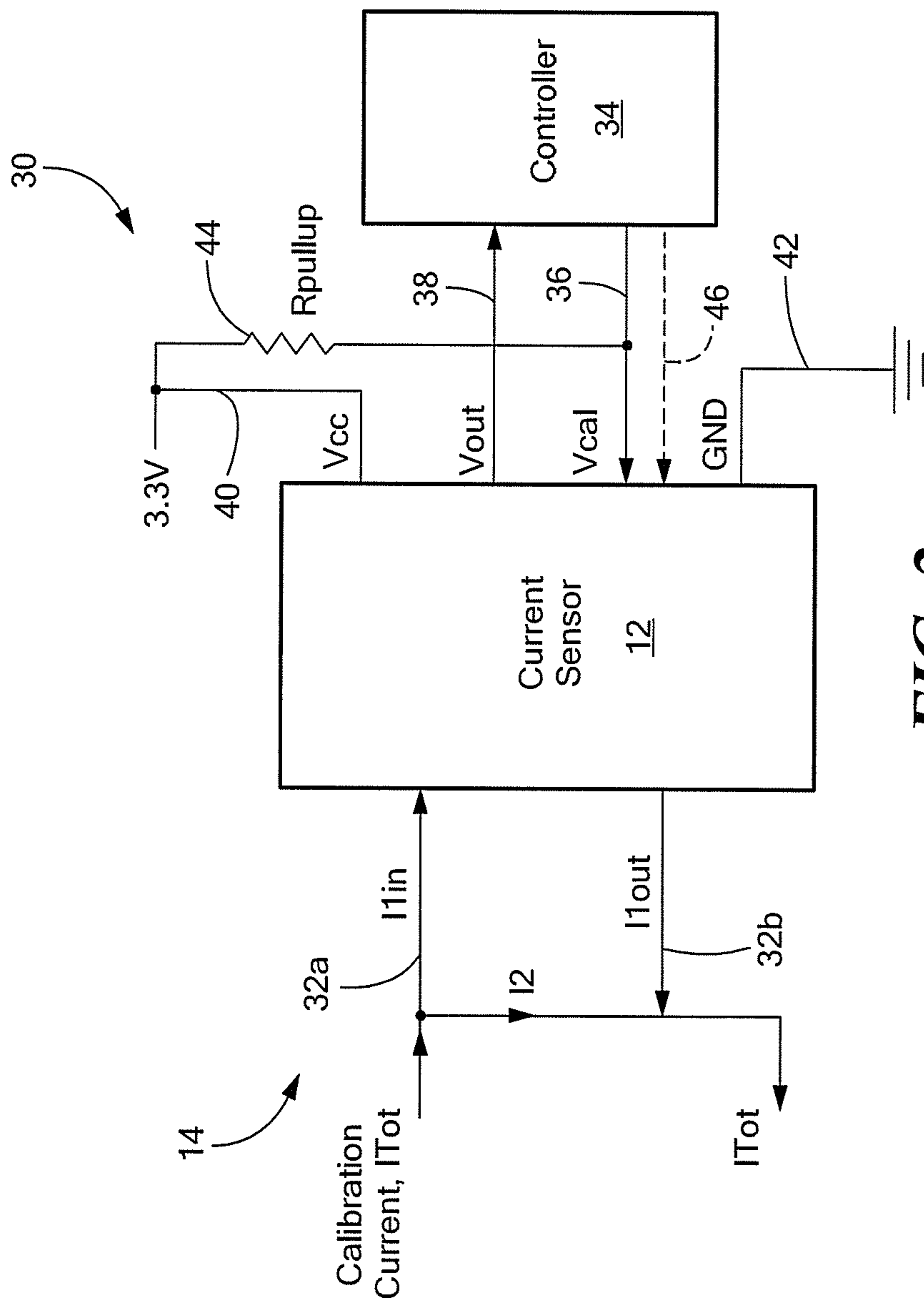


FIG. 2

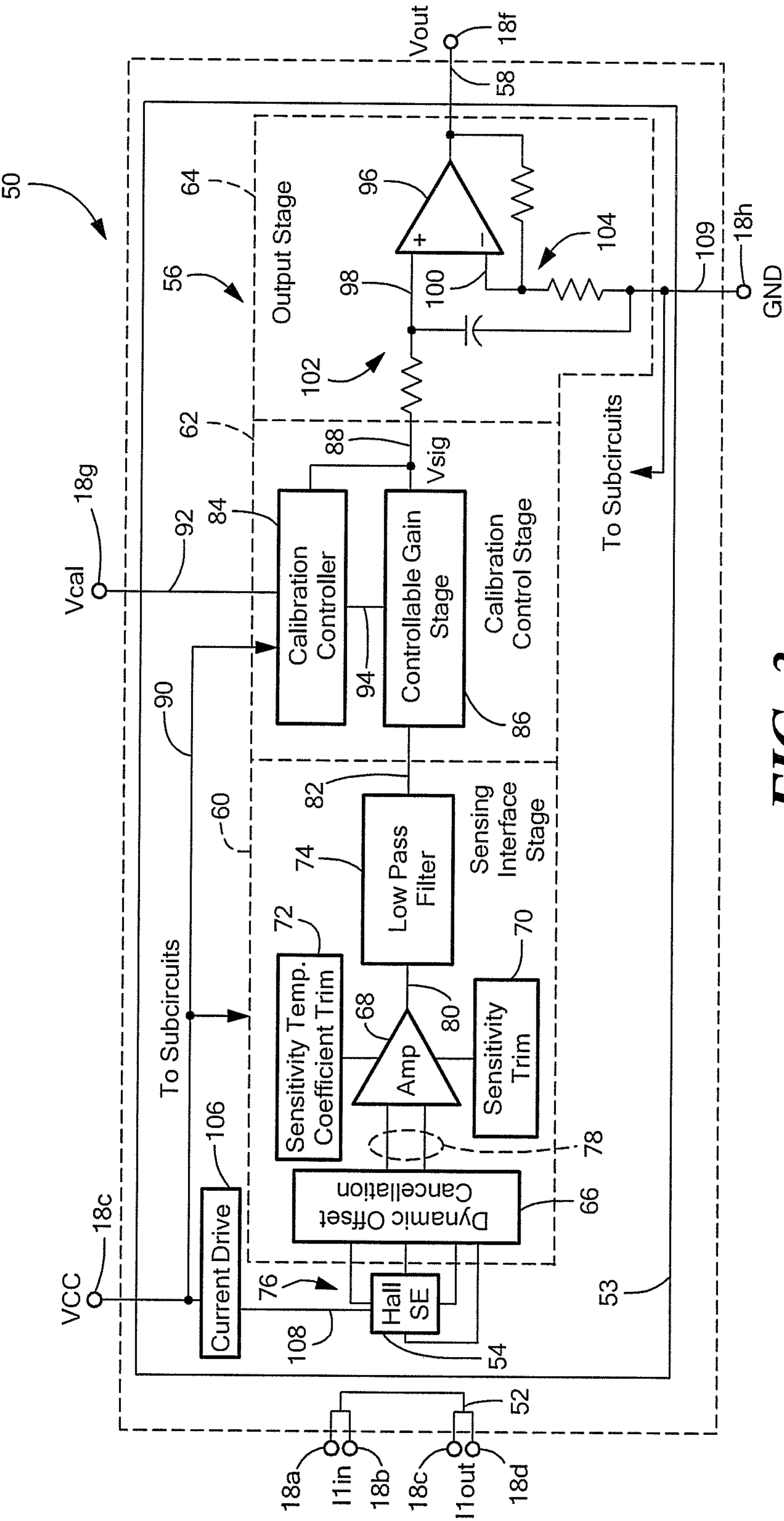


FIG. 3

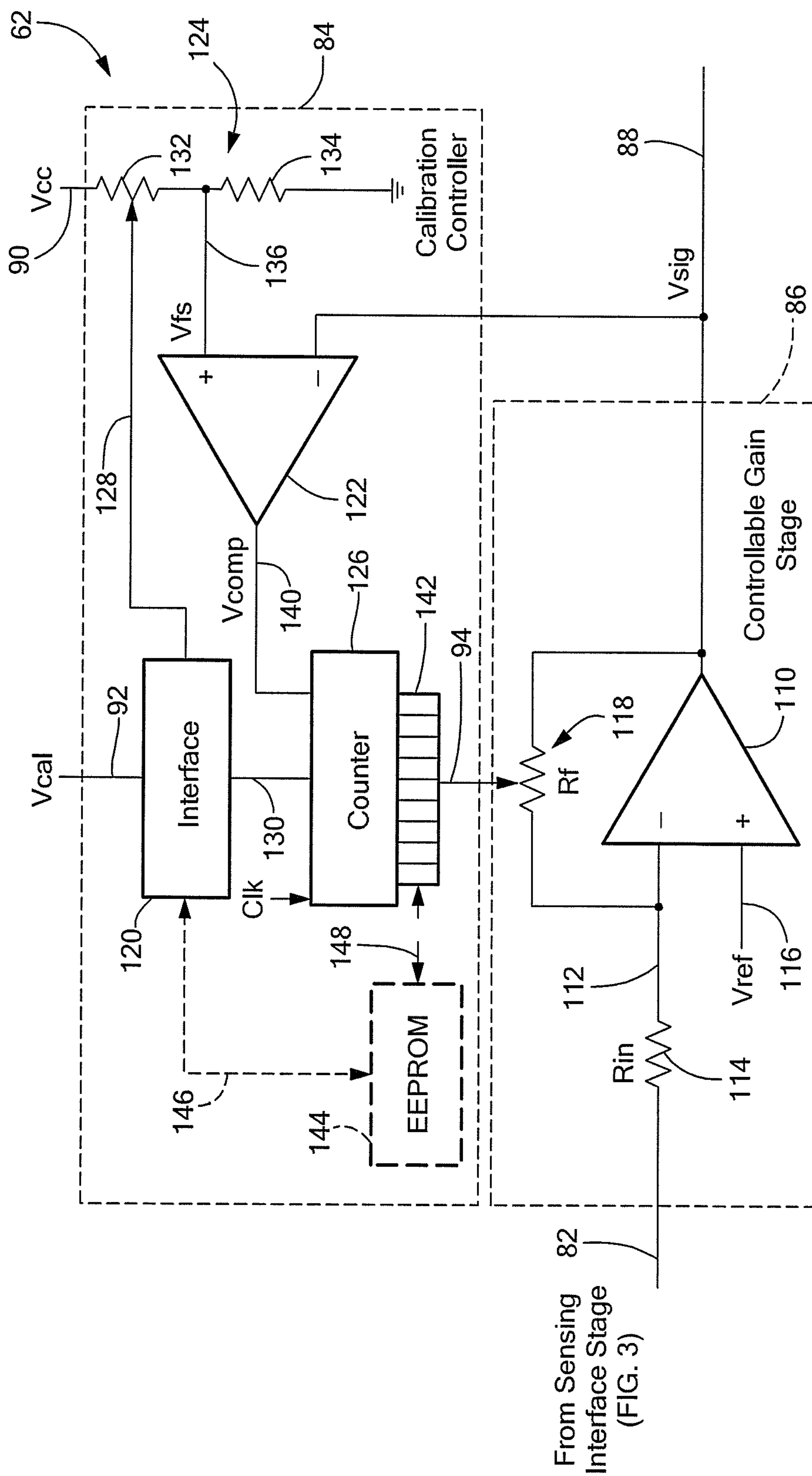


FIG. 4A

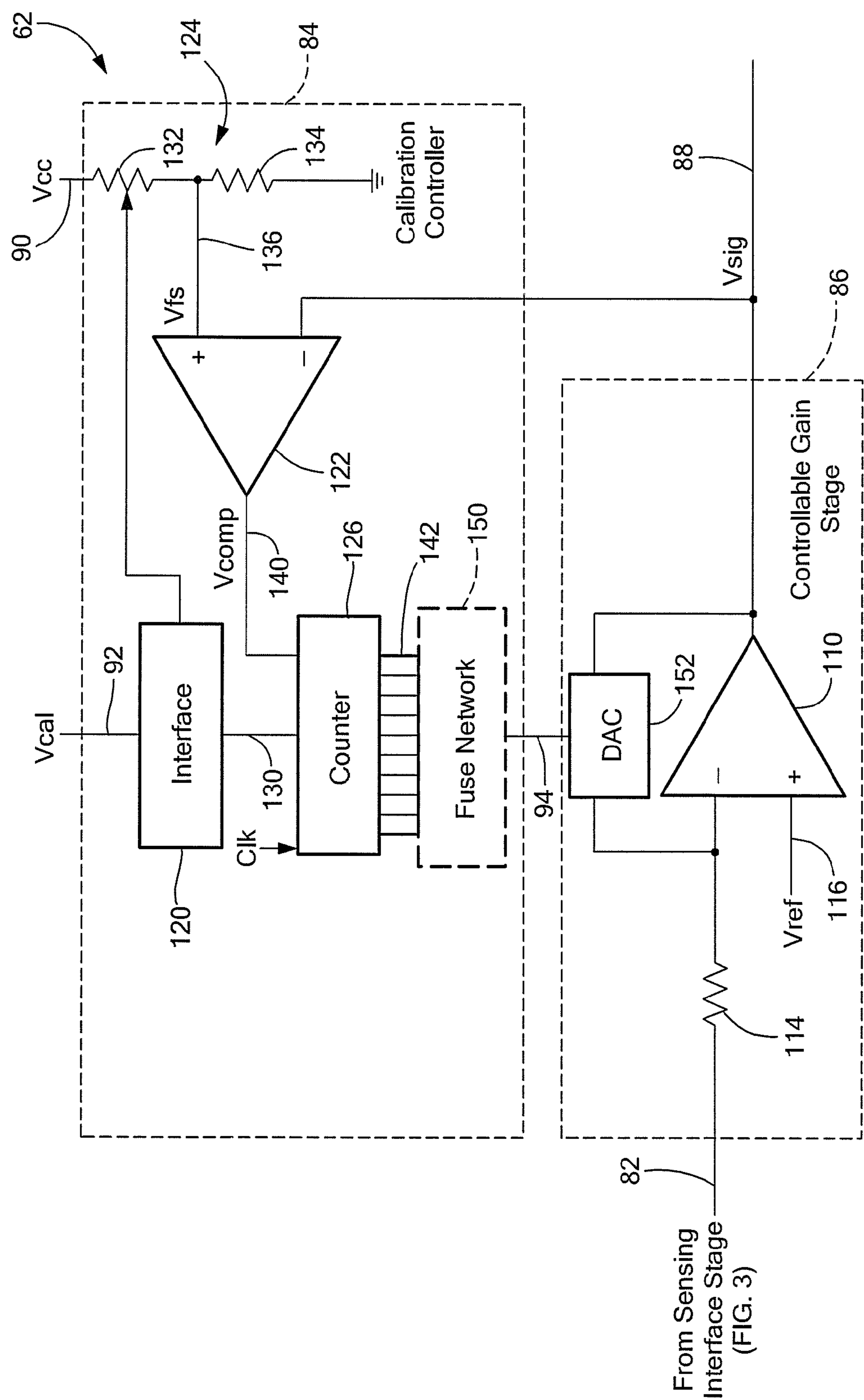
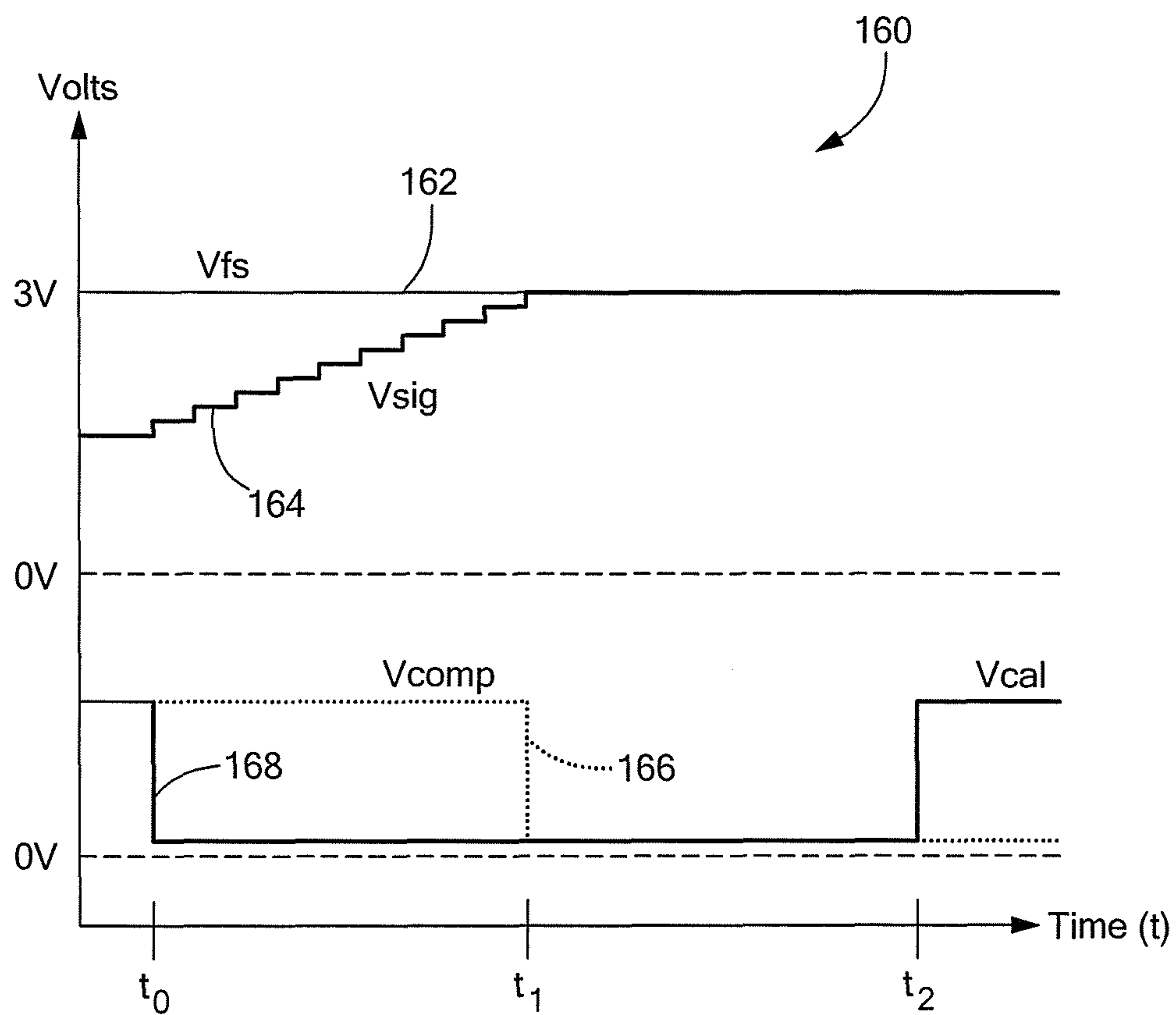


FIG. 4B

**FIG. 5**

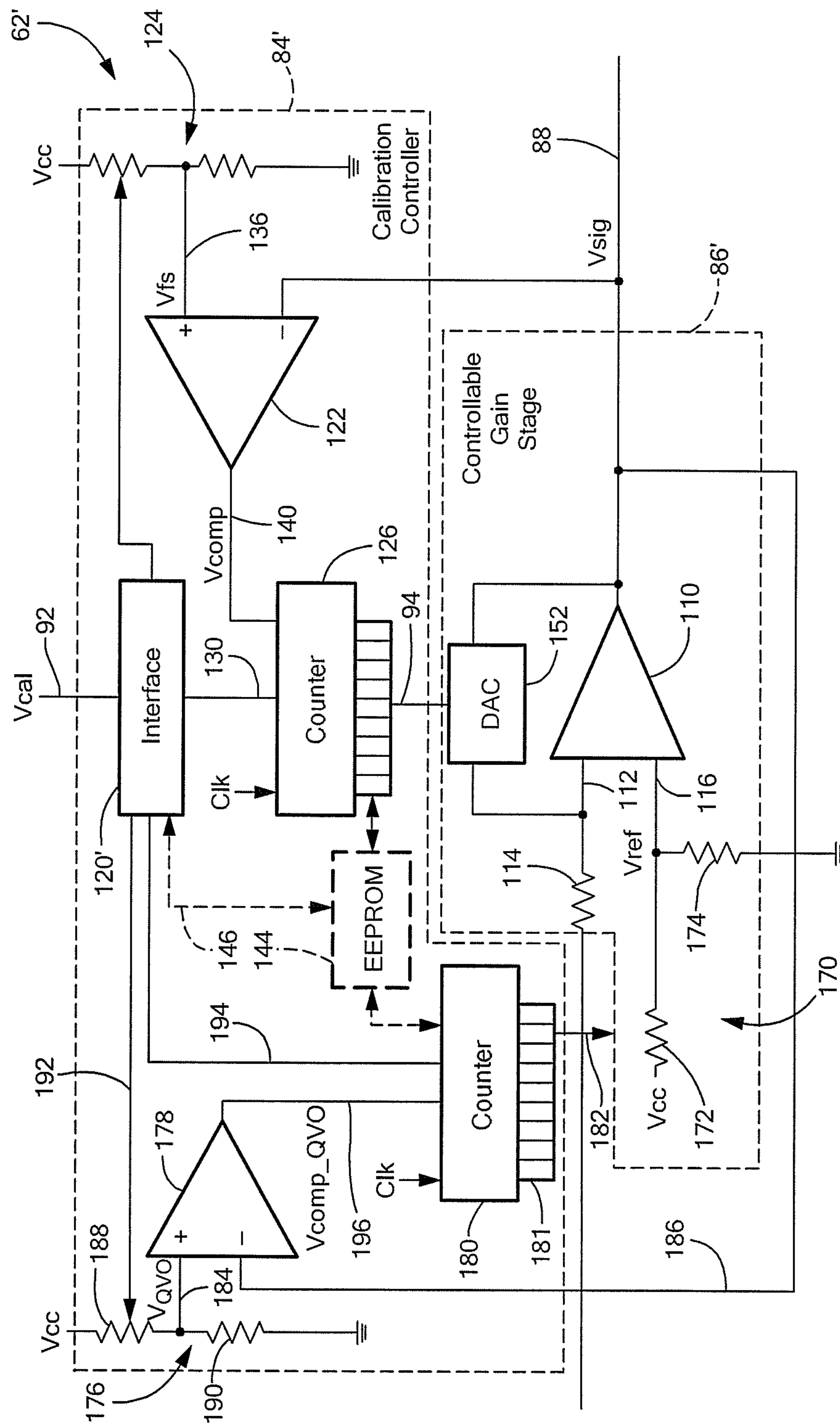


FIG. 6

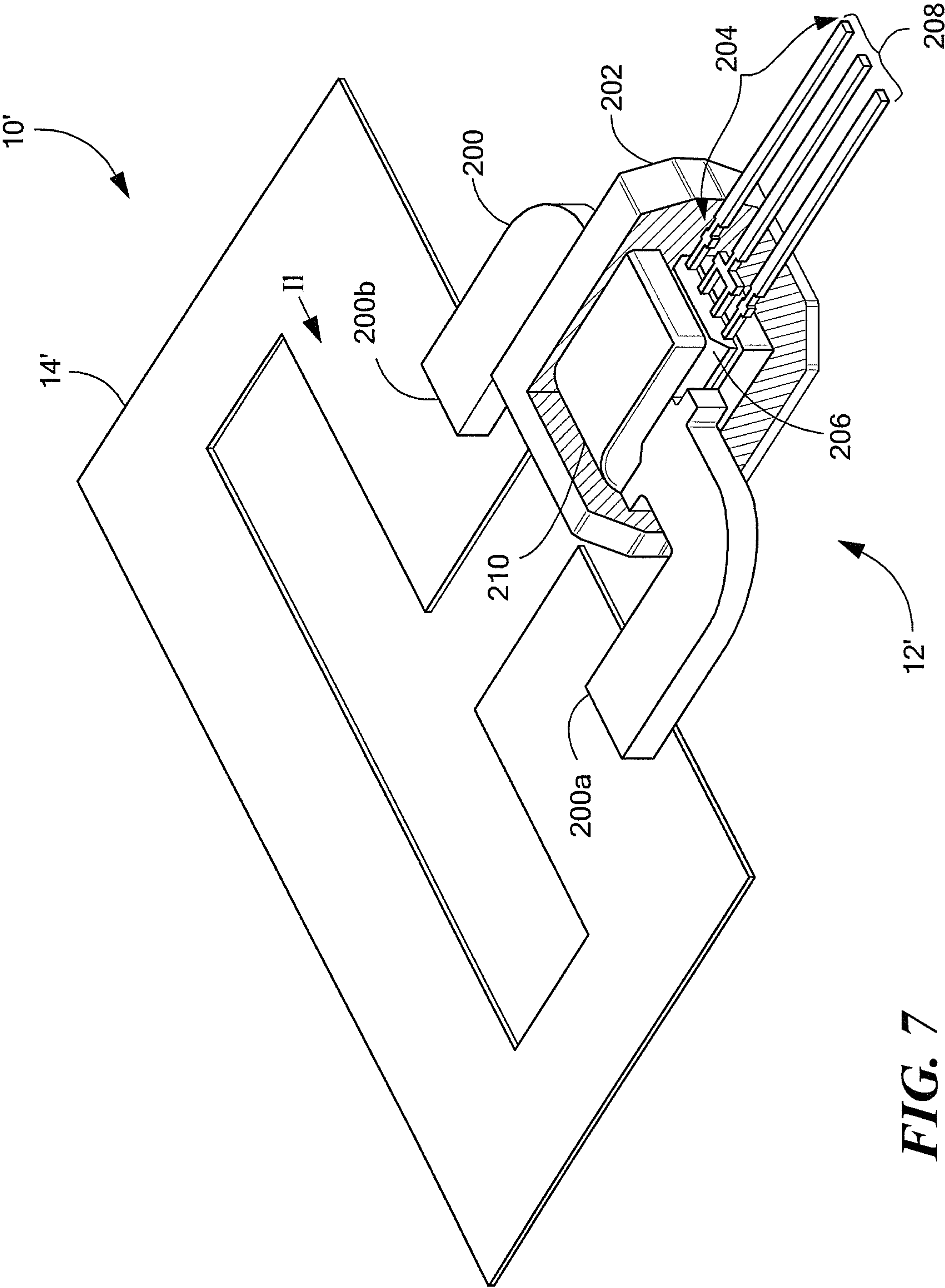


FIG. 7

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CURRENT SENSOR WITH CALIBRATION FOR A CURRENT DIVIDER CONFIGURATION

CROSS REFERENCE TO RELATED APPLICATIONS

Not Applicable.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH

Not Applicable.

FIELD OF THE INVENTION

This invention relates generally to current sensors with integrated current conductors and, more particularly, to such a current sensor for use in a current divider configuration.

BACKGROUND OF THE INVENTION

As is known in the art, one type of conventional current sensor uses a magnetic field transducer (for example a Hall effect or magnetoresistive transducer) in proximity to a current conductor. The magnetic field transducer generates an output signal having a magnitude proportional to the magnetic field induced by a current that flows through the current conductor. Typically, the current sensor also includes circuitry to amplify and condition the output signal of the magnetic field transducer.

The magnetic field transducer and circuitry are sometimes provided as an integrated circuit (IC) in an IC package that also contains a current conductor. Illustrative current sensors of this type are sold under part numbers ACS712 and ACS758xCB by Allegro MicroSystems, Inc. of Worcester, Mass. 01615, the Assignee of the subject application.

Various parameters characterize the performance of current sensors, including sensitivity. Sensitivity is related to the magnitude of a change in output voltage from the Hall effect transducer in response to a sensed current. The sensitivity of a current sensor is related to a variety of factors. One important factor is the physical separation between the Hall effect element and the current conductor.

Integration of the current conductor into an IC package allows for close and precise positioning of the current conductor relative to the magnetic field transducer. However, the amount of current that can be routed through the current conductor is limited by the physical and thermal limitations of the IC package.

One technique for measuring current levels that exceed the current carrying capability of the current sensor is to physically split the current path between the integrated current conductor and an external shunt current conductor that is coupled in parallel with the integrated current conductor. This technique can also be used to increase the current transient survival capability of the current sensor (also referred to as the current sensor's "over-current capability") by diverting some current away from the current sensor. With such a current divider arrangement, only a portion of the total current to be measured is carried by the integrated current conductor and the remainder of the current is carried by the external shunt current conductor. The external shunt current conductor can be implemented with a trace or layer on a printed circuit board (PCB) on which the current sensor is mounted or with a bus bar. Current conductors that are configured as current dividers are designed to achieve a known division of current so that

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measurement of the current carried by the integrated current conductor can be used to determine the total current.

While this type of arrangement can be used to increase current measurement levels of an application as well as current carrying capability of the current sensor, there are disadvantages. Namely, since less current will flow through the integrated current conductor, the resulting magnetic field signal level (i.e., the resolution) will be lower. Also, manufacturing and assembly tolerances, both at the device and at the board level, result in some variability in the division of current between the integrated current conductor and the shunt current conductor from the designed division of current. For example, the resistance of the current sensor package's lead frame can vary over the course of time due to production tolerances. The manufacturing process of soldering the current sensor package leads to a PCB trace is also very important, as higher solder resistance can cause more current to pass through the shunt conductor and less through the integrated current conductor of the current sensor. The thickness and width of PCB traces can also vary as a function of manufacturing tolerances. Such variability is undesirable since the total current cannot be accurately determined from the measurement of current carried by the integrated current conductor. In applications where accuracy requirements make it necessary to compensate for these variations, some current sensors allow the sensitivity to be programmed after assembly as is described in an Application Note AN295036, Rev. 3, of Allegro MicroSystems, Inc. entitled "Using Allegro Current Sensor ICs in Current Divider Configurations for Extended Measurement Range" (and published at <http://www.allegromicro.com/en/Products/Design/an/an295036.pdf>), which Application Note is incorporated by reference herein in its entirety.

SUMMARY OF THE INVENTION

In general, in one aspect, the invention is directed to an integrated circuit current sensor that allows for self-calibration in a current divider configuration. The current sensor includes an integrated current conductor, a magnetic field transducer, a controllable gain stage and a calibration controller. The integrated current conductor is adapted to receive a portion of a calibration current. The calibration current corresponds to a full scale current. The magnetic field transducer, responsive to the calibration current portion, provides a magnetic field signal having a magnitude proportional to a magnetic field generated by the calibration current portion. The controllable gain stage is configured to amplify the magnetic field signal with an adjustable gain to provide an amplified magnetic field signal. The calibration controller is responsive to a calibration command signal to adjust the adjustable gain of the controllable gain stage to a calibrated gain in order to provide the amplified magnetic field signal at a predetermined voltage level that corresponds to a desired current sensor output signal voltage level if the full scale current were received by the integrated current conductor.

Embodiments of the invention may include one or more of the following features. The calibration controller can include a comparator having a first input responsive to a full scale reference voltage indicative of the predetermined voltage level, a second input responsive to the amplified magnetic field signal, and an output at which a comparator output signal is provided in a first state when the amplified magnetic field signal is less than the full scale reference voltage and in a second state when the amplified magnetic field signal is greater than the full scale reference voltage. The calibration controller can further include a counter that is responsive to

the calibration command signal to start counting, responsive to the comparator output signal to stop counting, and that provides a counter output signal to the controllable gain stage for adjusting the adjustable gain. The full scale reference voltage can be determined by the calibration command signal. The controllable gain stage can include a variable resistor controlled by the counter output signal from the calibration controller. The controllable gain stage can further include an adjustable reference voltage and the calibration controller can be responsive to a calibration command signal for adjusting the reference voltage to provide the amplified magnetic field signal at a predetermined voltage level corresponding to the calibration current when the calibration current is zero amps.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the invention, as well as the invention itself, may be more fully understood from the following detailed description of the drawings, in which:

FIG. 1 is a pictorial showing a current sensor in a current divider configuration;

FIG. 2 is a simplified block diagram of the current sensor of FIG. 1 in a control system;

FIG. 3 is a block diagram showing an exemplary architecture of the current sensor of FIGS. 1 and 2;

FIG. 4A shows a block diagram of a portion of the current sensor of FIG. 3 including a gain calibration feature, according to an exemplary embodiment;

FIG. 4B shows a block diagram of an alternative embodiment of a portion of the current sensor of FIG. 3 including a gain calibration feature;

FIG. 5 shows illustrative waveforms associated with the gain calibration feature depicted in FIGS. 4A-4B;

FIG. 6 is a block diagram showing an alternative embodiment of a portion of the current sensor of FIG. 3 including a quiescent voltage output (QVO) calibration feature; and

FIG. 7 is a pictorial showing an alternative current sensor in a current divider configuration.

DETAILED DESCRIPTION

Referring to FIG. 1, an exemplary current divider current sensing configuration 10 includes a current sensor 12 coupled to a current conductor 14. The current conductor may be, for example, a printed circuit board (PCB) trace or layer or a bus bar. In a current divider configuration, as illustrated, the current conductor 14 includes a current sense conductor portion 14a and a shunt conductor portion 14b that are connected in parallel. The figure shows the internal structure of the current sensor 12, which includes a lead frame 16 having a first portion 16a that includes leads (or pins) 18a-18d and a second portion 16b that includes leads 18e-18h. The leads 18a and 18b are coupled to leads 18c and 18d to form an internal current path or conductor. The current sensor 12 also includes an integrated circuit (IC) die 20 having at least one magnetic field transducer or sensing element 22, e.g., a Hall effect element, and interface circuitry (not shown) of a magnetic field sensor provided therein. The die 20 is disposed above the lead frame 16 so that the sensing element 22 is proximate to a "loop" portion of the internal current conductor, the loop portion being located underneath the die 20 (and not shown in the illustrated view the figure). The die 20 is mounted or coupled to the second lead frame portion 16b, and the die and lead frame assembly encased in plastic material 24. The illustrated package style is a surface mount package known as a small outline IC (SOIC).

Other package styles that can accommodate some type of internal current conductor along with the die 20 may be used. Another possible package option will be described later with reference to FIG. 7. A current sensor 12 having an integrated current conductor (like that formed between leads 18a, 18b and 18c, 18d) and sensor die (like die 20), regardless of package style, will be referred to herein as an IC current sensor or, simply, a current sensor.

In the current divider configuration, a total current to be measured, labeled "ITot", is applied to the current conductor 14. A current sense portion of the current, labeled "I1", flows through the current sense conductor portion 14a into the leads 18a, 18b, which are shown to be electrically coupled in parallel, through the loop portion (not shown), and out of leads 18c, 18d, which are also electrically coupled in parallel. The remainder of the total current, or shunt current labeled "I2", flows through the shunt conductor portion 14b, thus bypassing the current sensor 12. The path of the current is indicated by reference numeral 26, and includes a total current path 28 for total current ITot, and separate subpaths including a shunt path 30 for shunt current I2 and a current sense path 32a, 32b for current sense current I1.

In this configuration the current to be measured by the current sensor, I1, travels in and out of the current sensor 12 on the primary side. Inside the IC package, the IC die 20 is placed over but does not make contact with the integrated current conductor loop, thereby providing galvanic (voltage) isolation. Although different package technologies can be used, the use of a flip-chip assembly allows the magnetic field transducer 22 of the IC die 20 to be positioned in very close proximity to the internal current conductor loop so that the magnetic signal coupling is maximized.

As noted above in the Background, the disadvantages of using a current divider configuration include loss of current sensor resolution and variability in current division (i.e., mismatch between I1 and I2). Various prior techniques used to address these sources of error include system-level calibration (or compensation) and PCB trace trimming. A system-level calibration involves applying current to a current conductor designed for a desired current division, recording the current sensor's output and scaling that output in an external controller to the desired value. This method requires a more complex control system to be implemented by the user. Alternatively, the PCB trace can be laser trimmed to achieve a desired division of current. The PCB trim method is even more complex than system level calibration and would be time consuming in the application test environment, resulting in a high cost system. As yet another alternative, some current sensors allow device sensitivity to be programmed after device assembly (as mentioned in the above-referenced application note).

In contrast, according to the present invention, the current sensor 12 employs a self-calibration technique. The self-calibration feature allows the current sensor to calibrate itself, more specifically, to adjust sensitivity until the current sensor accurately reflects at its output a value indicative of the total amount current to be measured by an application having a given current divider configuration, that is, ITot. Sensitivity refers to the change in a current sensor's output in response to a change in current being sensed by the device. The sensitivity of the device is the product of the magnetic circuit sensitivity (in G/A) and the current sensor's linear amplifier gain (in mV/G). The sensitivity of the current sensor may be optimized by adjusting the gain. The term "full scale current", as it is used herein, refers to the maximum level of current that would be sensed by the current sensor in absence of a shunt path, that is, the total current ITot. The term "full scale volt-

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age” refers to the output voltage that corresponds to the full scale current. During the self-calibration, as will be described in fuller detail later, the current sensor 12 adjusts gain so that it provides an output signal that is the equivalent of the output signal that would be provided by the current sensor if a shunt path were not utilized, that is, if the current sensor were to sense the full scale current I_{Tot} . In this manner, the self-calibration allows for increased current transient survival, i.e., improved over-current capability, on the part of the current sensor (as achieved through the use of a current divider configuration), but unlike prior calibration approaches requires minimal input from the user as well as provides a simpler and less expensive solution to the problems of a shunt system design.

FIG. 2 shows a control system 30 in which a current divider configuration (as depicted in FIG. 1) is provided for calibration. On the primary conductor side of the current sensor 12, the sense current I_1 is carried to the current sensor 12 via current input “ I_{1in} ” 32a and is carried out of the current sensor 12 via output “ I_{1out} ” 32b. On the secondary side, the current sensor 12 is connected to and controlled by a controller 34. The controller 34 is operated with input from a user. Connections between the controller 34 and current sensor 12 include at least one control line (“ V_{cal} ”) 36 for sending a calibration command signal to the current sensor 12 and a current sensor output line (V_{out}) 38 for providing the sensor’s output to the controller 34. After self-calibration, during normal operation, the output V_{out} 38 provides a voltage that is proportional to the total current I_{Tot} . Other connections include a supply (V_{cc}) line 40 connecting the current sensor 12 to a supply voltage shown as 3.3V and a GND line 42 connecting the current sensor 12 to ground. The control line 36 is coupled to V_{cc} via a pull-up resistor “ R_{pullup} ” 44. The current sensor 12, in this arrangement, is operable as a self-calibrating current sensor. The control line 36 is used by the controller 34 to initiate self-calibration on the part of the current sensor 12. In one implementation, as shown, pulling the control line 36 from V_{cc} to GND (active low) would initiate the calibration sequence. An active high control signal where the control line is normally pulled low and released to a high voltage to initiate calibration could also be used. The user applies a known “calibration” current (as I_{Tot}) corresponding to the full scale current, to the current conductor 14, a portion of which will flow into and out of the current sensor 12 as I_1 , that is, a calibration current sensing portion, and uses the control signal 36 to initiate the self-calibration. During the self-calibration, the current sensor 12 adjusts an internal gain value until the output signal provided at output 38 has a desired value, that is, a level that corresponds to the selected, full scale calibration current I_{Tot} .

One or more additional control lines, e.g., line 46 (shown in dashed lines) may be provided for calibration purposes as well. For example, the controller 34 may be configured to use control line 36 to initiate self-calibration, either through the type of signaling described above, or by using a simple serial calibration command, and to use a separate control line, line 46, to set values of certain calibration-required reference voltages to user-selected values, as will be described in further detail later. All of the calibration control could be provided to the current sensor using the same control signal line as well. A single control line like line 36 may be used to control/initiate different “phases” of self-calibration, or separate lines like lines 36 and 46 may be used as dedicated control lines to control/initiate a particular phase, as will be discussed later with reference to FIG. 6.

FIG. 3 shows an internal architecture of the self-calibrating current sensor 12, indicated here by reference numeral 50,

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according to one exemplary embodiment. Two central components of the architecture are an integrated current conductor 52 and a magnetic field sensor 53. That portion of the current sensor 50 that contains the magnetic field sensor 53 is implemented as a monolithic IC (and thus corresponds to IC die 20 of current sensor 12 from FIGS. 1-2). The magnetic field sensor 53 includes a magnetic field transducer or sensing element shown here as a Hall effect element (“Hall SE”) 54 as well as sensor interface circuitry 56. The sensing element 54 senses the magnetic field generated by the current I_1 flowing through the current conductor 52. The integrated current conductor 52 may be formed by a portion of the current sensor’s lead frame, as was described earlier with reference to FIG. 1.

The circuitry 56 operates to receive an output of the sensing element 54, in this example a Hall voltage, and generate from it a current sensor output 58. For purposes of illustration, the circuitry 56 is partitioned into various functional blocks or stages, including a sensing interface (or magnetic field signal generating) stage 60, a calibration control stage 62 and an output stage 64.

The sensing interface stage 60 can be implemented to include a number of different components to amplify and condition the sensing element’s magnetic field signal output. The illustrated architecture includes a dynamic offset cancellation circuit 66, an amplifier 68, trim circuits 70 and 72, and a filter 74 shown as a low pass filter. The dynamic offset cancellation circuit 66, which is coupled to the SE 54 by connections 76, provides a DC offset adjustment for DC voltage errors associated with the magnetic field signal produced by the sensing element 54. The dynamic offset cancellation circuit 66 is coupled to the amplifier 68, which amplifies an offset adjusted SE output signal 78 provided by the dynamic offset cancellation circuit 66. Accuracy is optimized through trimming of sensitivity and temperature response, via the sensitivity trim circuit 70 and sensitivity temperature coefficient trim circuit 72, respectively. The sensitivity trim circuit 70 permits adjustment of the gain of the amplifier 68. The sensitivity temperature coefficient trim circuit 72 permits adjustment of the gain of the amplifier 68 in order to compensate for gain variations due to temperature.

The output of the amplifier 68, or amplifier output 80, is coupled to the filter 74. The filter 74 can be a low pass filter, as shown, and/or a notch filter. The filter 74 is selected in accordance with a variety of factors, including but not limited to, a desired response time and a frequency spectrum of noise associated with the sensing element, the dynamic offset cancellation circuit and the amplifier. The filter produces at its output a filtered, magnetic field output signal 82, which is provided as an input to the calibration control stage 62. Other implementations of the sensing interface stage 60 are possible.

Still referring to FIG. 3, the calibration control stage 62 includes a calibration controller 84 and a controllable gain stage 86. It is the calibration control stage 62 that performs the self-calibration. The controllable gain stage 86 produces an amplified magnetic field output signal (labeled “ V_{sig} ”) 88, which is provided to output stage 64 and as an input to the calibration controller 84. In addition to V_{sig} , the calibration controller 84 receives as inputs V_{cc} via a supply line 90 and a V_{cal} “calibration command” input 92 (which is connected to the external calibration control signal line 36 from the external controller 34, as shown in FIG. 2). The calibration controller 84 is coupled to and provides a gain adjustment output 94 as an input to the controllable gain stage 86 to adjust an adjustable gain of the controllable gain stage 86, as will be

described in further detail in reference to FIGS. 4A-4B. The output of the calibration control stage 86 is coupled to an output stage 64.

The output stage 64 is implemented in the illustrated architecture to provide an analog buffered output. The output stage 64, as depicted, includes a buffer amplifier 96 having a first (non-inverting) input 98 and a second input 100. An RC filter 102 is connected between the first input and the Vsig output 88 from the controllable gain stage 86. Applied to the second input 100 is a reference voltage developed by a resistive voltage divider 104 coupled between Vout 58 and ground.

The magnetic field sensor 53 can be any type of magnetic field sensor and is therefore not limited to Hall effect technology. Thus, the sensing element 54 may take a form other than that of a Hall effect element, such as a magnetoresistance (MR) element. The magnetic field sensor 53 is provided in the form of an IC or die containing a substrate on which the various circuit elements (including the sensing element 54) are formed. Although only one sensing element is shown, that sensing element 54 could be replaced by a pair of sensing elements connected in a differential arrangement, or multiple MR elements connected in a bridge circuit. Components to be included in the stage 60 can vary with the type of sensing technology that is chosen.

The current sensor, in a current divider (or shunt) configuration, as shown in FIGS. 1 and 2, with the self-calibration feature, operates to produce an analog output voltage Vout 58 having a magnitude that is proportional to the magnitude of the total current ITot (not I1 as would be the case without such calibration).

The current sensor 50 will have least one terminal (or pin or lead) to correspond to I1in and I1out, VCC (to connect to an external power supply), GND (to connect to ground), an input and output. For example, and referring back to the SOIC 12 shown in FIG. 1 in conjunction with FIG. 3, the terminals or leads for the current conductor 52 and various signals can be indicated by the reference numerals 18a, 18b for I1in, 18c, 18d for I1out, 18e for Vcc, 18h for GND, 18g for Vcal and 18f for Vout. The current sensor 50 provides the current sensor output signal Vout 58 at the Vout pin 18f for coupling to an external controller (such as controller 34 from FIG. 2) or for transmission to other application electronics (not shown). Power is supplied to the current sensor 50 through the VCC pin 18e, which is connected internally to the various subcircuits via supply bus interconnect 90, as well as a drive circuit 106 which provides a biasing signal to the Hall sensing element 54 via a connection 108. The GND pin 18h is connected internally via a GND bus interconnect 109 to provide a ground connection for subcircuits of the sensor IC. Other circuitry, to implement clock generation and control functions, for example, is largely omitted from this figure and other figures for purposes of simplification.

Details of the calibration control stage 62, in particular, the controllable gain stage 86 and the calibration controller 84, according to an exemplary embodiment, are shown in FIGS. 4A-4B. Referring to FIG. 4A, the controllable gain stage 86 includes an operational amplifier 110 having a first input 112 which couples the output 82 from the previous stage through an input resistor (Rin) 114 to the amplifier 110. The amplifier 110 has a second input 116 corresponding to a reference voltage Vref. A feedback resistor (Rf) 118 is coupled between the first input 112 and the output 88 (Vsig). The value of the feedback resistor 118, a variable resistor, is adjusted by the calibration controller 84 to set the gain of the amplifier 110. The gain or magnetic field signal amplification of amplifier 110 is given by $-Rf/Rin$. In the illustrated embodiment, the

resistor 118 is a digitally-controllable resistor that is controlled by the calibration controller 84 via signal 94.

Still referring to FIG. 4A, the calibration controller 84 includes an interface 120, a comparator 122, a resistive voltage divider 124 and a counter 126. The interface 120 receives as an input the Vcal control signal 92 and provides output signals 128 and 130 to the voltage divider 124 and the counter 126, respectively. The voltage divider 124 includes a first, variable resistor 132 and a fixed value resistor 134. The value of the variable resistor 132 is set by the user and provided via the interface 120 and interface output signal 128 to the voltage divider 124. The voltage divider 124 is used to generate a full scale reference voltage "Vfs", that is provided at a first input to the comparator, first comparator input 136. Through the programming of the resistor 132, therefore, the user is able to specify a desired value for Vfs. The comparator 122 receives the amplified magnetic field signal Vsig 88 (from the output of the amplifier 110, amplifier output 88) as the second input. The comparator's output, comparator output "Vcomp" 140, is provided as a counter input signal to the counter 126. The Vcomp output 140 serves as a counter disable and interface output signal 130 serves as counter enable.

The calibration control signal or command is provided to the calibration controller (via the Vcal line 92) to initiate the self-calibration. Before the self-calibration is initiated, the user causes the desired, full scale calibration current ITot to be applied to the current conductor (current conductor 14 as shown in FIG. 2), which results in a portion of that current, corresponding to I1, flowing into the current sensor's I1in terminal or terminals (e.g., terminals 18a, 18b, as shown in FIG. 3). When the self-calibration has been initiated, the interface 120 signals to the counter 126 via the counter enable input 130 to begin counting. Thus, the counter 126 is enabled to change its internal binary count value corresponding to a gain value, indicated by reference numeral 142. Each count results in an adjustment of the gain of the controllable gain stage 86. More specifically, the gain is adjusted by using the count value to vary the value of the variable feedback resistor 118, which results in a change to Vsig 88. Meanwhile, the comparator 122 compares the signal Vsig 88 with the predetermined reference input Vfs 136. The value of variable resistor 118 is adjusted with each count by the counter 126 until the comparator 122 determines the voltage level of Vsig 88 has passed the full scale threshold value of the full scale reference voltage Vfs 136. Typically, a voltage comparator of the type to be used for comparator 122 changes its output when the voltage difference between its inputs crosses through approximately zero volts. The process of counting, adjusting and comparing continues until the comparator 122 determines that Vsig has reached Vfs, at which point the comparator output Vcomp 140 changes state. More specifically, the comparator output signal Vcomp 140 is provided in a first state when the amplified magnetic field signal Vsig 88 is less than the full scale reference voltage Vfs 136 and in a second state when the amplified magnetic field signal Vsig 88 is greater than the full scale reference voltage Vfs. This change in the state of Vcomp 140 causes the counter 126 to stop counting. The count/gain value corresponding to the final count value is used as the calibrated gain value, to be applied to the controllable gain stage's feedback resistor 118 via counter output 94.

Once the gain adjustment portion of the self-calibration has been completed, the interface 120 can permanently store the calibrated gain value 142 on the chip, e.g., in a nonvolatile memory such as an EEPROM 144, as shown, or in some alternative manner. The EEPROM 144, if used, will be coupled to the interface 122 and count 142 (of the counter

126) via lines 146 and 148, respectively. Once the adjusted gain has been saved, the self-calibration is complete. These interconnections 146 and 148 are used to accomplish a transfer of the calibrated gain value 142 between counter 126 and the nonvolatile memory.

During subsequent, non-calibrating operation of the current sensor in the same current divider configuration with ITot as the total current to flow through the current conductor and I1 the portion to be sensed by the current sensor, the current sensor uses the calibrated gain to provide at the output a signal that has been scaled from a voltage level corresponding to the sensed current to a predetermined voltage level corresponding to the total current ITot.

Certain implementation details of the calibration controller 84 and controllable gain stage 86 are a matter of design choice. For example, as shown in FIG. 4B, the EEPROM or other nonvolatile memory may be replaced with a fuse network 150. Also, the variable resistor 118 may be implemented with any type of digitally controllable variable resistor circuit that allows a range of resistance values to be selectable using a digital code. As shown in FIG. 4B, it could be implemented with a DAC 152, for example, an R/2R ladder DAC, or other type of circuit that provides digital control of variable resistance. It will be understood that the design of the counter and digitally-controllable variable resistor will determine the range and "step" size (i.e., resistance value change per count) of the gain adjustment. Other details of FIG. 4B are as shown in FIG. 4A.

It will be understood that the current sensor 50 could have more input pins so that the calibration command and specification of Vfs (via the adjustment to the voltage divider variable resistor 132) may be provided as separate control signals. The interface 120 can be implemented as a digital serial interface, such as Inter-Integrated Circuit (I²C), Single-Edge Nibble Transmission (SENT), Peripheral Sensor Interface 5 (PSI5) or Serial Peripheral Interface (SPI), or a simple RS232 interface. Thus, for example, the calibration command provided at input 92 and transfer of the count to nonvolatile memory (e.g., EEPROM 144) can be achieved with messages according to a selected one of these or other suitable protocols.

FIG. 5 shows a graph 160 of various calibration-related waveforms, including a waveform 162 corresponding to Vfs, a waveform 164 corresponding to Vsig, a waveform 166 corresponding to Vcomp and a waveform 168 corresponding to Vcal. The Vcomp waveform 166 is indicated in dotted lines to distinguish it from the Vcal waveform 168. At time t₀, the Vcal signal (waveform 168) transitions from high to low to initiate the calibration sequence. After the calibration control signal transition, the value of Vsig is being increased as the gain is adjusted with each count. The comparator 122 (from FIGS. 4A-4B) compares Vsig to Vfs. In the illustrated graph, the value of Vfs is shown to be set to a desired value of 3V. The initial value for Vsig is set to VCC/2 (or 1.65V for VCC=3.3V). The value of the gain is adjusted until the value of Vsig is determined to have reached the value of Vfs, which occurs at t₁. When Vsig reaches the desired value of Vfs, the comparator output Vcomp changes state (e.g., goes low, as illustrated in the figure). At t₁ the gain adjustment portion of the calibration sequence ends. At t₂, the control signal Vcal goes high again to signal the end of the calibration sequence. Between t₁ and t₂, the calibration controller 84 (from FIGS. 4A-4B) saves the gain (count) value reached during the gain adjustment, e.g., by storing the value in nonvolatile memory, as discussed earlier.

Thus, for a predetermined voltage level of Vfs and corresponding full scale current level of calibration current (both

user-selected levels for a given current divider configuration), the current sensor 50 can self-calibrate to adjust an adjustable gain of the controllable gain stage 86 to scale the value of that stage's output, the amplified magnetic field signal Vsig 88 (and therefore, the output provided at Vout 58 (from FIG. 3)), to the predetermined voltage level of Vfs. For example, assuming that the magnetic circuit sensitivity is in the order of magnitude of approximately 10 Gauss per amp (which means that for every amp flowing through the sensor's integrated current conductor 52, 10 Gauss of field is generated and sensed by the Hall element 54) and that the desired output is 3V when 20 Amps is flowing through the current sensor, then the gain of the controllable gain output stage 62 is calculated to be (3V-1.65V)/20 A/10 G/A or 67.5 mV/A. If a total current, "ITot", of 20 Amps is passed through the current divider system and the current is split perfectly at 10 A through the shunt path ("I2") and 10 A through the sensor ("I1") and the desired output voltage on Vout is 3V, then the gain would be adjusted by the self-calibration to be twice the value calculated above, or (3-1.65)V/10 A/10 G/A, or 135 mV/A.

Adjustable gain values for the 3V output example and different current level splitting are given below in Table 1. The perfect 10 A split between the shunt and current sensor is shown in row 11 of table.

TABLE 1

| Current splitting and required gain for a 3 V output | | | | | | |
|--|--------------------------|------------|------------|--------------|---------------------------|------------------------|
| Row | Amps Total Current | Amps I2 | Amps I1 | mV/A Gain | Volts Vout @ 0 Amps | Volts Vout at I1 |
| 1 | 20 | 0 | 20 | 68 | 1.65 | 3 |
| 2 | 20 | 1 | 19 | 71 | 1.65 | 3 |
| 3 | 20 | 2 | 18 | 75 | 1.65 | 3 |
| 4 | 20 | 3 | 17 | 79 | 1.65 | 3 |
| 5 | 20 | 4 | 16 | 84 | 1.65 | 3 |
| 6 | 20 | 5 | 15 | 90 | 1.65 | 3 |
| 7 | 20 | 6 | 14 | 96 | 1.65 | 3 |
| 8 | 20 | 7 | 13 | 104 | 1.65 | 3 |
| 9 | 20 | 8 | 12 | 113 | 1.65 | 3 |
| 10 | 20 | 9 | 11 | 123 | 1.65 | 3 |
| 11 | 20 | 10 | 10 | 135 | 1.65 | 3 |
| 12 | 20 | 11 | 9 | 150 | 1.65 | 3 |
| 13 | 20 | 12 | 8 | 169 | 1.65 | 3 |
| 14 | 20 | 13 | 7 | 193 | 1.65 | 3 |
| 15 | 20 | 14 | 6 | 225 | 1.65 | 3 |
| 16 | 20 | 15 | 5 | 270 | 1.65 | 3 |
| 17 | 20 | 16 | 4 | 338 | 1.65 | 3 |
| 18 | 20 | 17 | 3 | 783 | 1.65 | 3 |
| 19 | 20 | 18 | 2 | 1675 | 1.65 | 3 |

In practice, designing a current configuration system that would require that the self-calibration increase the gain to very high levels (e.g., gains above 300 mV/A) is not practical because the Hall transducer output generates a weak signal, which means lower resolution and signal to noise ratio (since both the signal and the noise are amplified as the gain increases). On the other hand, designing the system so that most of the current flows through the current sensor and not the shunt path would do little to improve the over-current capability of the current sensor (which, of course, is one of the advantages of using a shunt path). In the 20 Amp example above, the current sensor could amplify the signal with less than 5 A in the current sensor and greater than 15 A provided through the shunt path for a gain of approximately 300 mV/A as shown in Table 1. This would allow for a split of 5 A/20 A or a 25% to 75% split through the current sensor and shunt

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path, respectively, while compensating for any error in splitting the current as discussed above.

Normally, when no current is flowing through the current sensor, the value of V_{ref} (at amplifier input 116, FIGS. 4A-4B) is set at a value ("0 amp offset value") that ensures that the zero current output voltage V_{sig} (referred to as the quiescent voltage output or "QVO", the voltage of the output signal when the current sensed by the sensing element is zero) is at $V_{cc}/2$ for bi-directional current sensing (i.e., sensing of current flowing in either direction) or a low voltage near ground, for example, 0.5V, for uni-directional current sensing (i.e., sensing of currents flowing in only in the direction). For example, a bi-directional sensor with a V_{cc} of 3.3V would have a 0 Amp output of 1.65V.

Because QVO often changes as a function of the gain of the current sensor IC, it may be desirable to expand the self-calibration of the calibration control stage 62 to include a second calibration, a QVO calibration, to be performed following the gain adjustment calibration. Referring to FIG. 6, an exemplary embodiment of the calibration control stage 62 that incorporates QVO calibration functionality, calibration control stage 62', is shown. A modified controllable gain stage 86, shown as controllable gain stage 86', further includes a resistive voltage divider 170 formed by a variable resistor 172 and a fixed value resistor 174 to set a value for an adjustable reference voltage V_{ref} at amplifier input 116. A modified calibration controller 84, shown here is calibration controller 84', includes a second resistive voltage divider 176, comparator 178 and counter 180. A count 181 of the counter 180, at counter output 182, is used to set the value of the variable resistor 172 in the controllable gain stage 86'. The comparator 178 has as a first input a voltage V_{QVO} 184 and as a second input the voltage V_{sig} , fed back from the output of the amplifier 110 in the controllable gain stage 86' via a feedback line 186. The value of V_{QVO} is generated by the voltage divider 176, which is formed by a variable resistor 188 and fixed value resistor 190. The value of the variable resistor 188 is user-programmable via the interface, shown here is interface 120'. The user can therefore specify the V_{QVO} voltage by providing a resistance value to the interface 120' on the V_{cal} control signal 92 (or separate control signal). The interface 120' provides the resistance value to the variable resistor 188 along line 192. The interface 120' is also coupled to the counter 180 via line 194, which provides a counter enable to the counter 180. Also connected to the counter 180 is the comparator 178, which produces a V_{comp} signal ("Vcomp_QVO") at 196 to disable the counting by the counter 180.

Once a self-calibration has been initiated, and a gain adjustment portion and calibrated gain store has been completed, the QVO calibration can begin. First the user must set the current I_{Tot} through the system to 0 A and then send a second calibration command to the interface 120'. Upon receipt of the calibration command, the interface signals (via line 194) to the counter 180 to start counting. The count of the counter 180 changes and with each count iteration the value of variable resistor 188 is adjusted (thereby adjusting the value of V_{ref} that is provided to the amplifier 110) until the comparator 178 determines that voltage level or magnitude of V_{sig} has passed the threshold provided by V_{QVO} . That is, the comparator output signal 196 is provided in a first state when the magnitude of the amplified magnetic field signal V_{sig} (provided at 186) is less than that of the V_{QVO} signal 184 and in a second state when the magnitude of the amplified magnetic field signal V_{sig} is greater than the magnitude of the V_{QVO} signal 184. Once the value of V_{sig} has reached V_{QVO} , the voltage reference adjustment portion of this second phase

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of the self-calibration is complete and the "final" count value from the counter 180 is saved in the EEPROM 144 or other suitable nonvolatile memory (or, alternately, a fuse network like fuse network 150 shown in FIG. 4B).

The sequencing of these two phases of the self-calibration activity is managed externally through control signals or commands provided by an external controller. A single control line or separate control lines, one to control the gain adjustment and the other to control the offset adjustment, may be used. The self-calibration may be repeated if desired. Also, a QVO calibration could be performed before and after the gain adjustment to provide an initial setting for the adjustable reference voltage and an updated setting following the gain adjustment. The QVO calibration, if performed at least once (following a gain adjustment), would increase the accuracy of the current sensor, especially for designs in which the gain is increased to high levels, e.g., gains above a 300 mV/A level. The QVO calibration could be performed only prior to the gain calibration but with less accurate results (for the reasons discussed above).

To support higher current measurements, another current sensor package option having a thicker current conductor may be used. An example is provided in FIG. 7, which shows the internal structure of a current sensor in a current divider configuration, indicated by reference numeral 10'. The current divider configuration 10' includes a current sensor 12' coupled to the current conductor 14' (depicted as a bus bar). The current sensor 12' includes a primary current conductor 200, a package or housing 202, and a packaged current sensor IC 204. The packaged current sensor IC 204 is shown as a single in-line (SIP) IC with a package body 206 (containing the sensor IC 53 from FIG. 3) and signal pins 208. Because of the magnetic coupling between this thicker current conductor and the IC's sensing element, a flux concentrator 210 is used. The current conductor 200, the SIP device 204 and concentrator 210 are assembled and then overmolded to form the current sensor 12'. Portions of the current conductor 200 that are external to the package 202, that is, portions 200a and 200b, are used to carry the current I_1 from the current conductor 14' and through the package 202 containing the assembly of concentrator 210 and SIP 204 and return I_1 to the current conductor 14'.

In sum, the current sensor with integrated current conductor and self-calibration as described above can be controlled (with minimal external control) to calibrate itself to have a calibrated gain that results in the current sensor output signal having a voltage level that corresponds to the full scale calibration current, not the sensed portion of the calibration current. In this manner, the self-calibrating current sensor can, with relative ease, compensate for lower signal resolution and "calibrate out" any current mismatch associated with a current divider configuration.

All references cited herein are hereby incorporated herein by reference in their entirety.

Having described preferred embodiments, which serve to illustrate various concepts, structures and techniques, which are the subject of this patent, it will now become apparent to those of ordinary skill in the art that other embodiments incorporating these concepts, structures and techniques may be used. Accordingly, it is submitted that that scope of the patent should not be limited to the described embodiments but rather should be limited only by the spirit and scope of the following claims.

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What is claimed is:

1. An integrated circuit current sensor, comprising: an integrated current conductor adapted to receive a portion of a calibration current, wherein the calibration current corresponds to a full scale current; a magnetic field transducer responsive to the calibration current portion for providing a magnetic field signal having a voltage level proportional to a magnetic field generated by the calibration current portion; a controllable gain stage configured to amplify the magnetic field signal with an adjustable gain in order to provide an amplified magnetic field signal; and a calibration controller responsive to a calibration command signal from a controller for adjusting the adjustable gain of the controllable gain stage to a calibrated gain to provide the amplified magnetic field signal at a predetermined voltage level that corresponds to a desired current sensor output signal voltage level if the full scale current were received by the integrated current conductor.

2. The integrated circuit current sensor of claim 1 wherein the calibration controller comprises:

a comparator having a first input responsive to a full scale reference voltage indicative of the predetermined voltage level, a second input responsive to the amplified magnetic field signal, and an output at which a comparator output signal is provided in a first state when the amplified magnetic field signal is less than the full scale reference voltage and in a second state when the amplified magnetic field signal is greater than the full scale reference voltage; and

a counter that is responsive to the calibration command signal to start counting, responsive to the comparator output signal to stop counting, and that provides a counter output signal to the controllable gain stage for adjusting the adjustable gain.

3. The integrated circuit current sensor of claim 2 wherein the full scale reference voltage is determined by the calibration command signal.

4. The integrated circuit current sensor of claim 3 wherein the calibration controller further comprises a resistive voltage divider configured to provide the full scale reference voltage, wherein the resistive voltage divider has a variable resistance and a fixed resistance and wherein the variable resistance is determined by the calibration command signal.

5. The integrated circuit sensor of claim 2 wherein the controllable gain stage comprises a variable resistor controlled by the counter output signal.

6. The integrated circuit current sensor of claim 5 wherein the variable resistor comprises a digital-to-analog converter (DAC).

7. The integrated circuit current sensor of claim 6 wherein the DAC comprises an R/2R DAC.

8. The integrated circuit current sensor of claim 1 wherein the calibration command signal is a serial binary signal in a format selected from Inter-Integrated Circuit (I²C), Single-Edge Nibble Transmission (SENT), Peripheral Sensor Interface 5 (PSI5) or Serial Peripheral Interface (SPI).

9. The integrated circuit current sensor of claim 1 further comprising a gain storage device, wherein the calibrated gain is stored in the gain storage device.

10. The integrated circuit current sensor of claim 9 wherein the gain storage device is selected from an EEPROM and a fuse network.

11. The integrated circuit current sensor of claim 1 wherein the controllable gain stage comprises an adjustable reference voltage and wherein the calibration controller is responsive to a calibration command signal for adjusting the adjustable reference voltage to provide the amplified magnetic field

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signal at a predetermined voltage level corresponding to a calibration current of zero amps.

12. The integrated circuit current sensor of claim 11 wherein the calibration controller further comprises:

a comparator having a first input responsive to an adjustable quiescent voltage output voltage (V_{QVO}) reference voltage indicative of the predetermined voltage level corresponding to the calibration current when the calibration current is zero amps, a second input responsive to the amplified magnetic field signal, and an output at which a comparator output signal is provided in a first state when the amplified magnetic field signal is less than the predetermined voltage level and in a second state when the amplified magnetic field signal is greater than the predetermined voltage level; and

a counter that is responsive to the calibration command signal to start counting, responsive to the comparator output signal to stop counting, and that provides a counter output signal to the controllable gain stage to adjust the adjustable reference voltage.

13. The integrated circuit current sensor of claim 12 wherein the adjustable V_{QVO} reference voltage is determined by the calibration command signal.

14. The integrated circuit current sensor of claim 13 wherein the calibration controller further comprises a resistive voltage divider configured to provide the (V_{QVO}) reference voltage, wherein the resistive voltage divider has a variable resistance and a fixed resistance and wherein variable resistance is determined by the calibration command signal.

15. The integrated circuit current sensor of claim 12 wherein the controllable gain stage further comprises a resistive voltage divider configured to provide the adjustable reference voltage, wherein the resistive voltage divider has a variable resistance and a fixed resistance and wherein variable resistance is controlled by the counter output signal.

16. The integrated circuit current sensor of claim 1 wherein the magnetic field transducer, the calibration controller and the controllable gain stage are provided in an integrated circuit.

17. The integrated circuit current sensor of claim 1 wherein the controllable gain stage comprises an adjustable reference voltage and the calibration controller is responsive to a second calibration control signal to control the adjustable reference voltage.

18. The integrated circuit sensor of claim 1 further comprising a package including a lead frame having a lead frame portion that forms the integrated current conductor.

19. A method of self-calibration by a current sensor having an integrated current conductor when coupled in parallel with an external shunt conductor in a current divider configuration, comprising:

sensing a magnetic field generated by a portion of a calibration current that is provided at a full scale current level to the current divider configuration, the calibration current portion being carried through the integrated current conductor, with a magnetic field transducer positioned in proximity to the integrated current conductor to provide a magnetic field signal having a voltage level proportional to the magnetic field;

amplifying the magnetic field signal with an adjustable gain to provide an amplified magnetic field signal; and adjusting the adjustable gain to a calibrated gain in order to provide the amplified magnetic field signal at a predetermined voltage level associated with the calibration current when the calibration current is provided at a full scale current level.

20. The method of claim 19 further comprising:
sensing a magnetic field generated by the calibration cur-
rent portion when the calibration current is provided at a
current level of zero amps, to provide a magnetic field
signal having a voltage level proportional to the mag- 5
netic field;
amplifying the magnetic field signal with the calibrated
gain to provide an amplified magnetic field signal; and
adjusting an adjustable reference voltage to provide the
amplified magnetic field signal at a predetermined volt- 10
age level associated with the calibration current when
the calibration current is provided at a current level of
zero amps.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,604,777 B2
APPLICATION NO. : 13/181926
DATED : December 10, 2013
INVENTOR(S) : Michael C. Doogue et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification

Column 8, Line 6 delete “input the veal control” and replace with --input the Vcal control--.

Column 9, Line 60 delete “signal veal goes” and replace with --signal Vcal goes--.

Column 10, Line 11 delete “52, 10 Gauss” and replace with --52, 10Gauss--.

Column 10, Line 15 delete “(3V-1.65V)/20 A/10 G/A” and replace with --(3V-1.65V)/20A/10G/A--.

Column 10, Line 17 delete “at 10 A through” and replace with --at 10A through--.

Column 10, Line 18 delete “and 10 A through” and replace with --and 10A through--.

Column 10, Line 21 delete “or (3-1.65)V/10 A/10 G/A, or 135” and replace with --or (3-1.65)V/10A/10/G/A, or 135--.

Column 10, Line 25 delete “perfect 10 A split” and replace with --perfect 10A split--.

Column 10, Line 62 delete “the 20 Amp” and replace with --the 20 Amp--.

Column 10, Line 64 delete “than 5 A in” and replace with --than 5A in--.

Column 10, Line 64 delete “than 15 A provided” and replace with --than 15A provided--.

Column 10, Line 65 delete “300 mV/A” and replace with --300mV/A--.

Column 10, Line 66 delete “split of 5 A/20 A” and replace with --split of 5A/20A--.

Column 11, Line 52 delete “system to 0 A and” and replace with --system to 0A and--.

Signed and Sealed this
Twenty-ninth Day of December, 2015



Michelle K. Lee
Director of the United States Patent and Trademark Office