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(54) **LASER BONDING FOR STACKING SEMICONDUCTOR SUBSTRATES**

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(60) Provisional application No. 61/144,668, filed on Jan. 14, 2009.

(51) **Int. Cl.**
H01L 21/30 (2006.01)

(52) **U.S. Cl.**
USPC **438/455; 438/109**

(58) **Field of Classification Search**

USPC 438/108, 109, 455, 456, 457, 459, 464; 257/621

See application file for complete search history.

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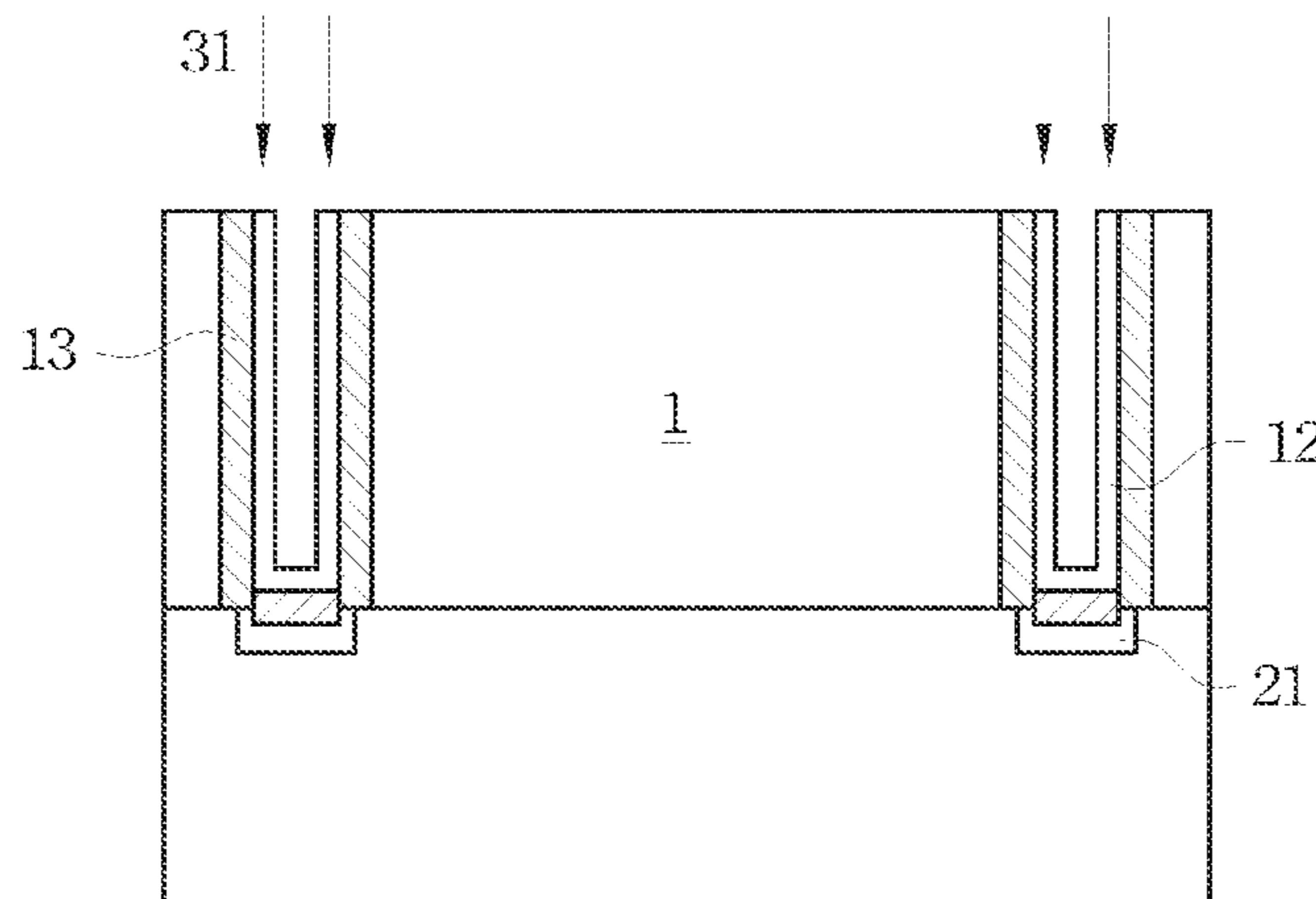
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(57) **ABSTRACT**

Methods and structures using laser bonding for stacking semiconductor substrates are described. In one embodiment, a method of forming a semiconductor device includes forming a trench in a first substrate, and a bond pad on a second substrate comprising active circuitry. A top surface of the bond pad includes a first material. The first substrate is aligned over the second substrate to align the trench over the bond pad. An electromagnetic beam is directed into the trench to form a bond between the first material on the bond pad and a second material at a bottom surface of the first substrate.

20 Claims, 7 Drawing Sheets



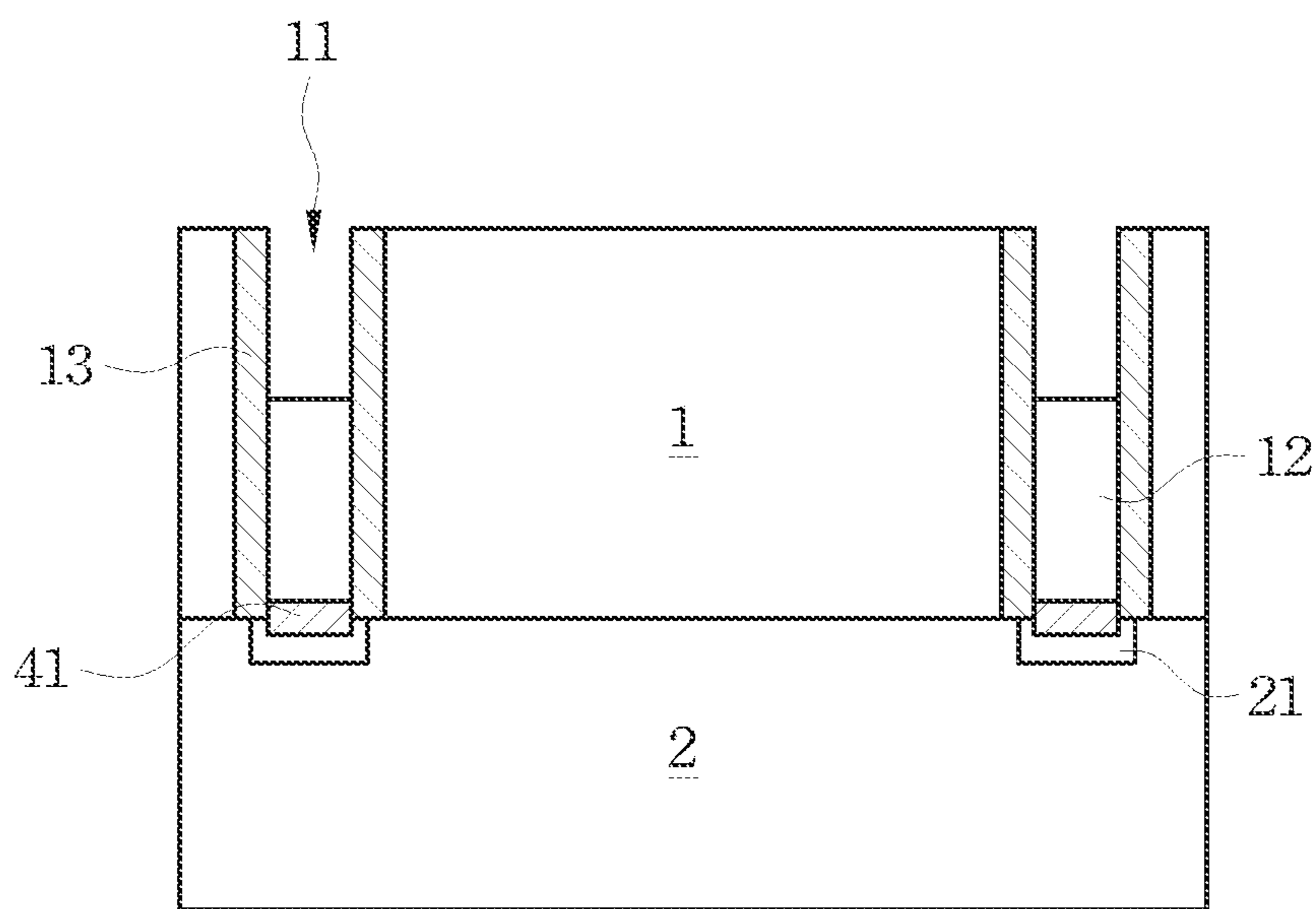


Fig. 1

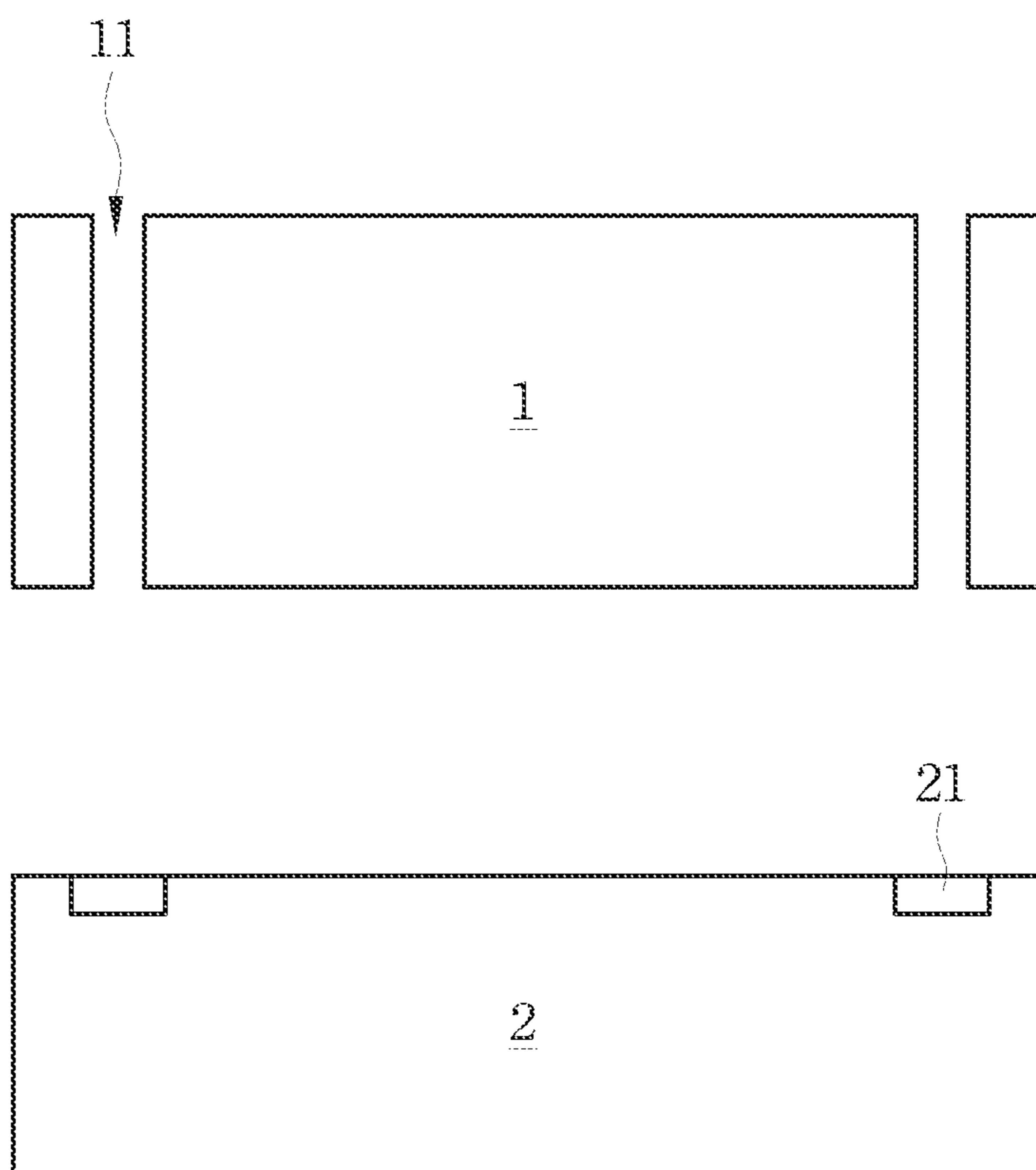


Fig. 2a

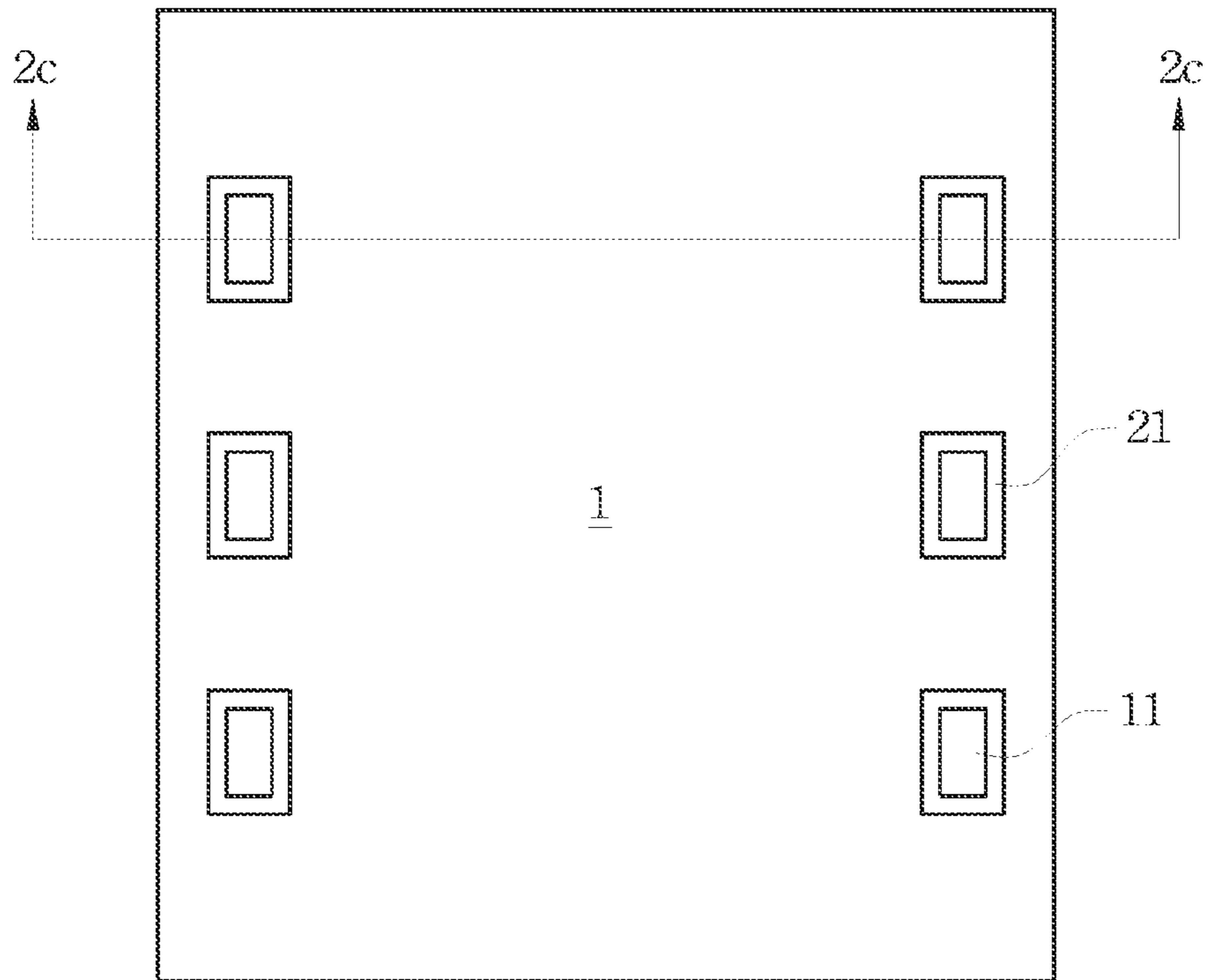


Fig. 2b

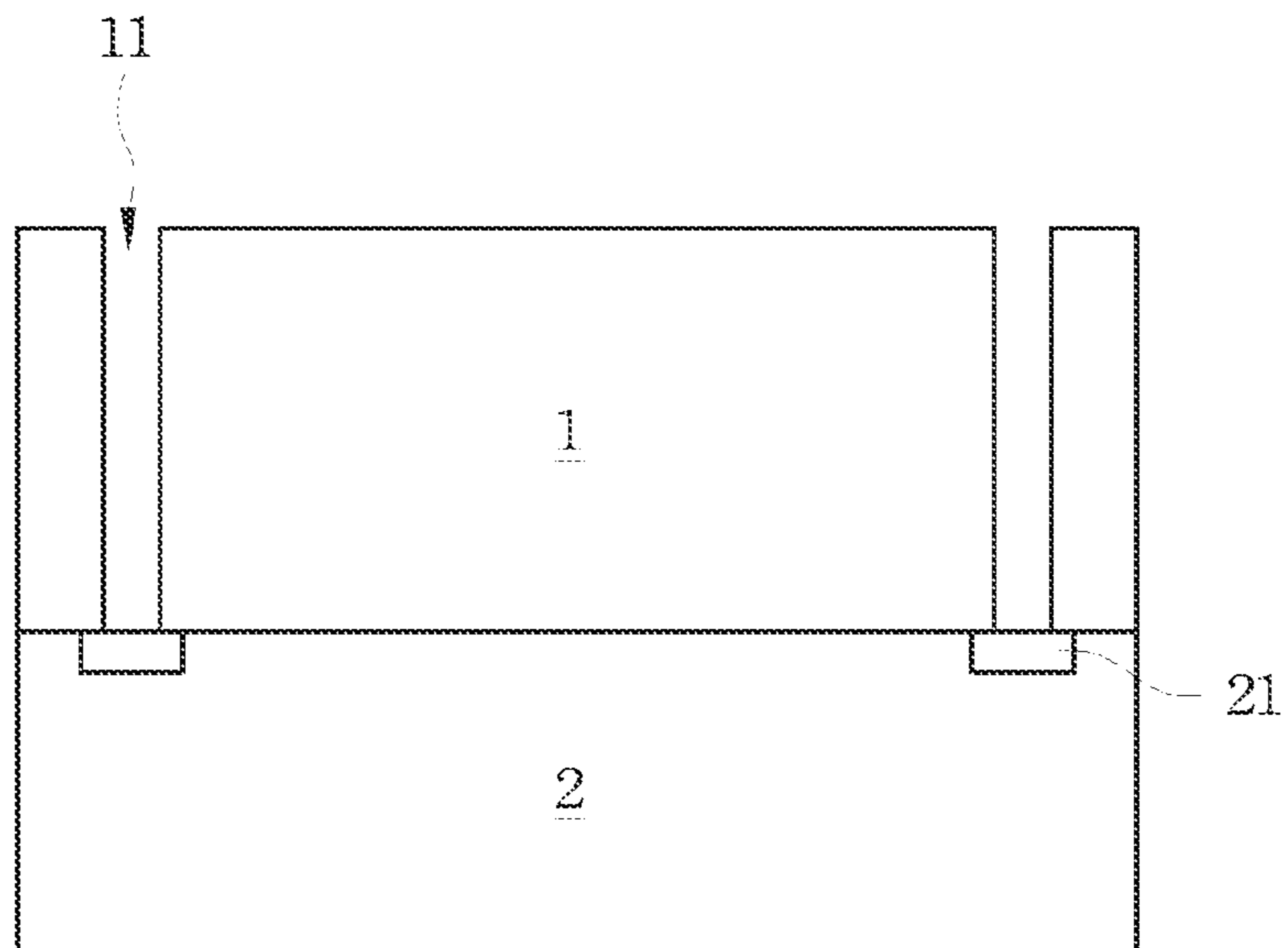


Fig. 2c

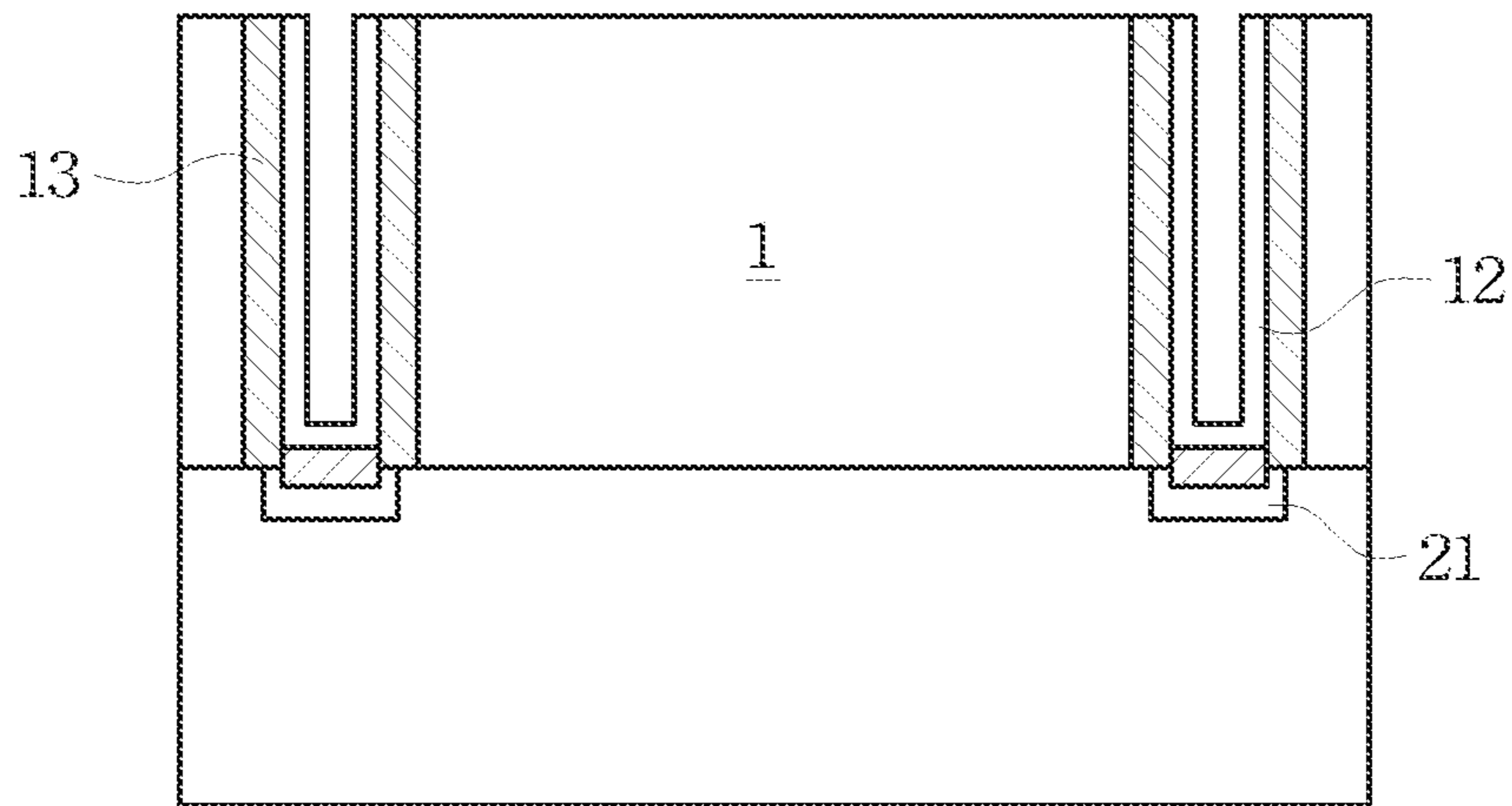


Fig. 2d

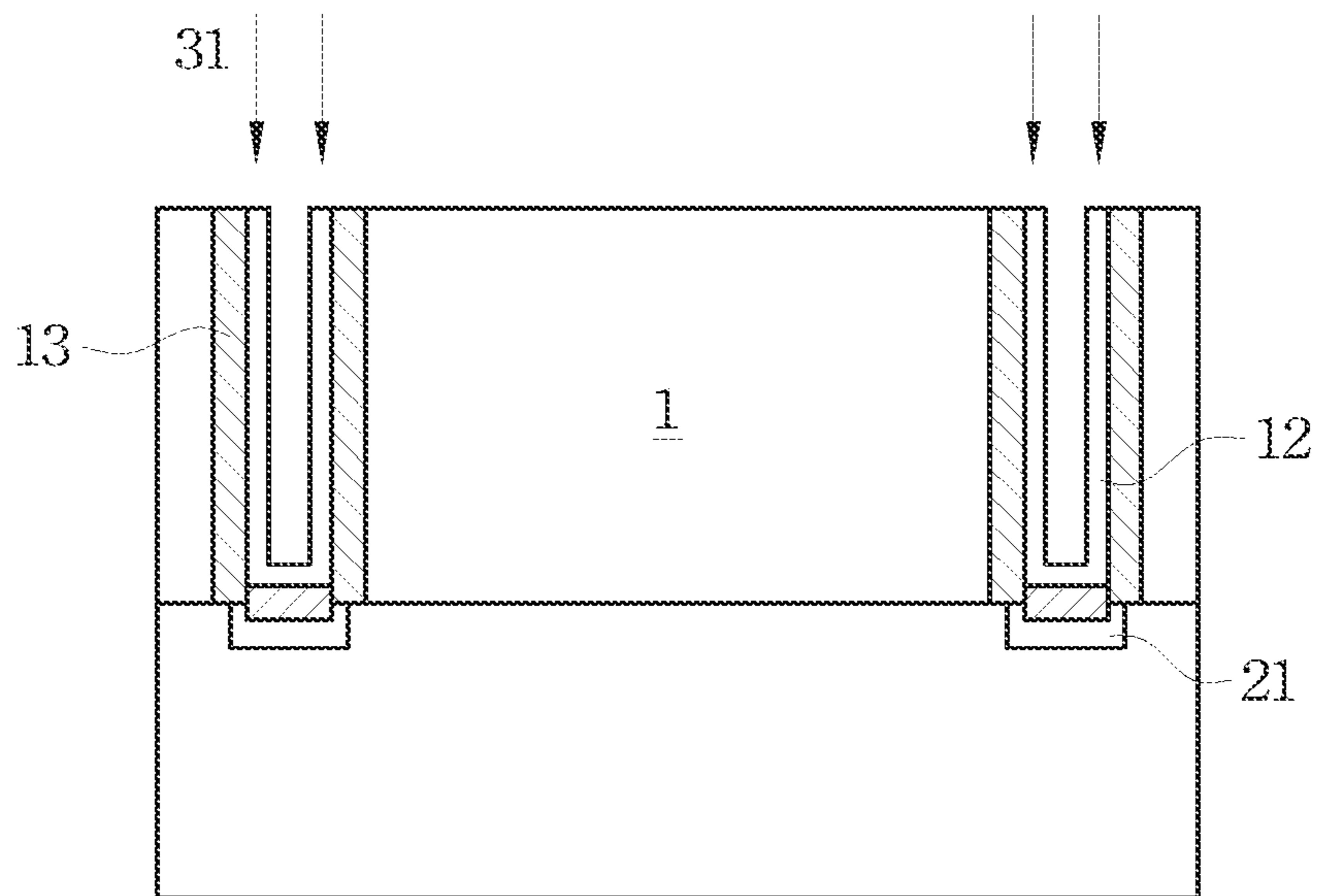


Fig. 2e

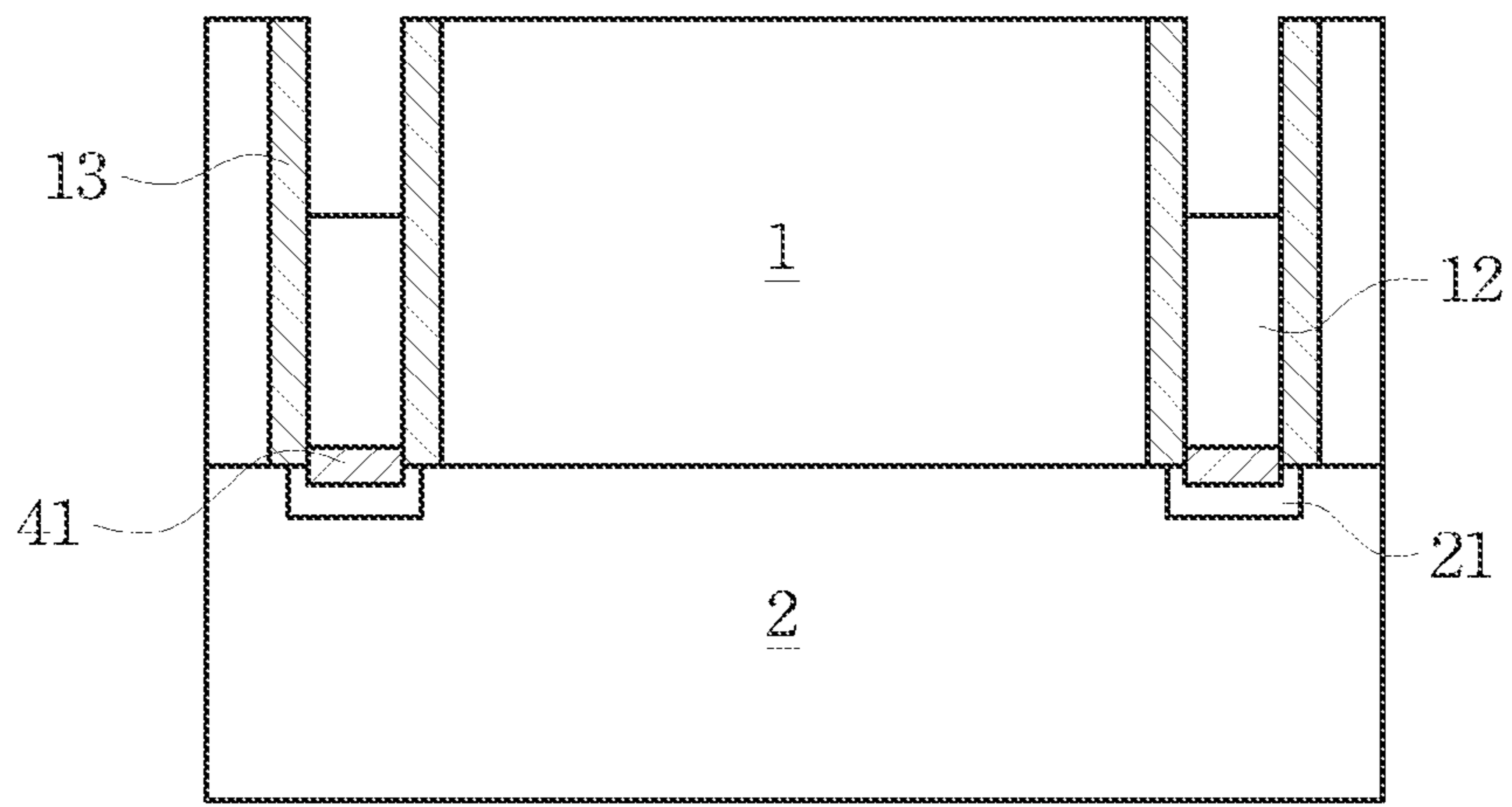


Fig. 2f

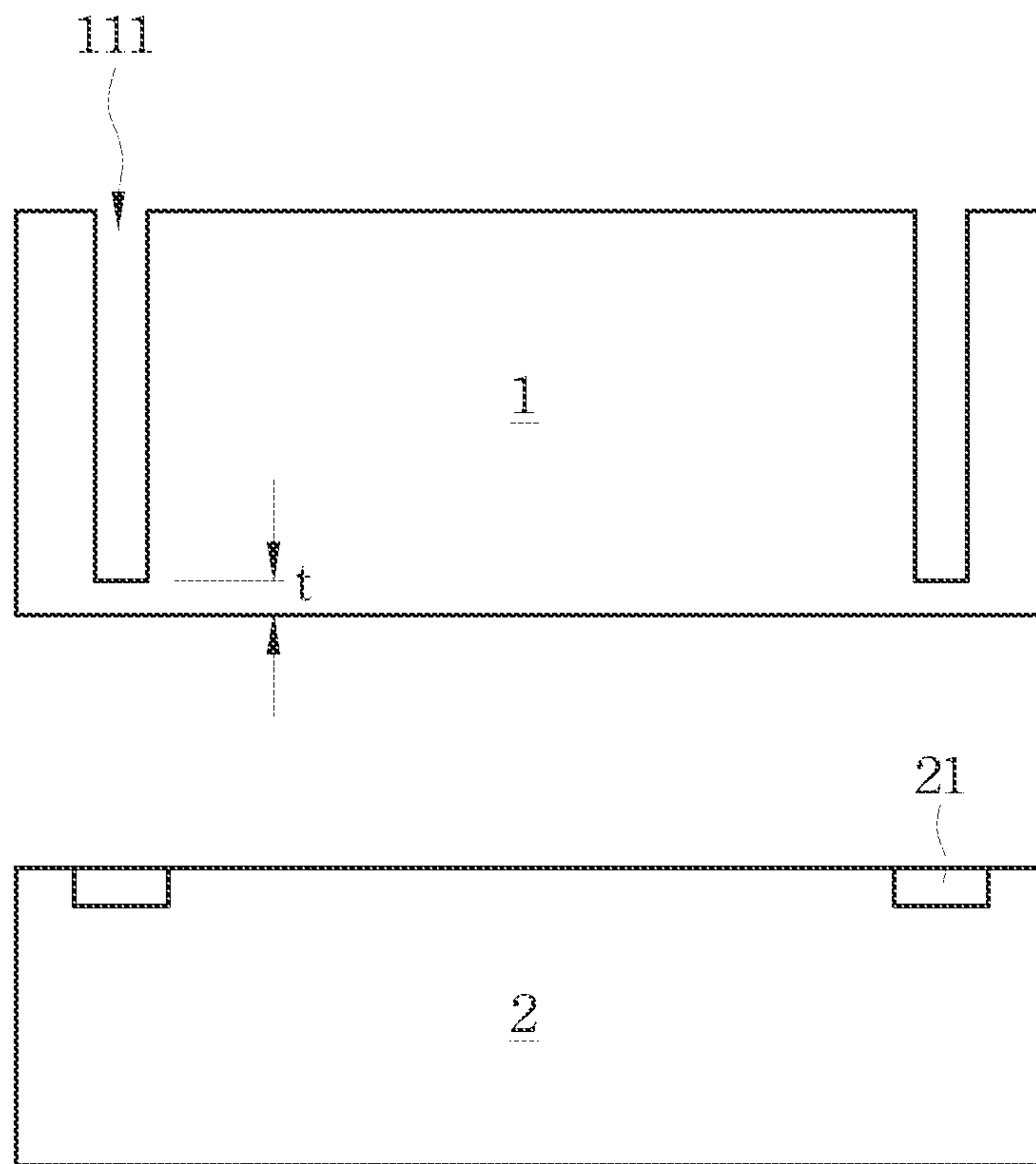


Fig. 3a

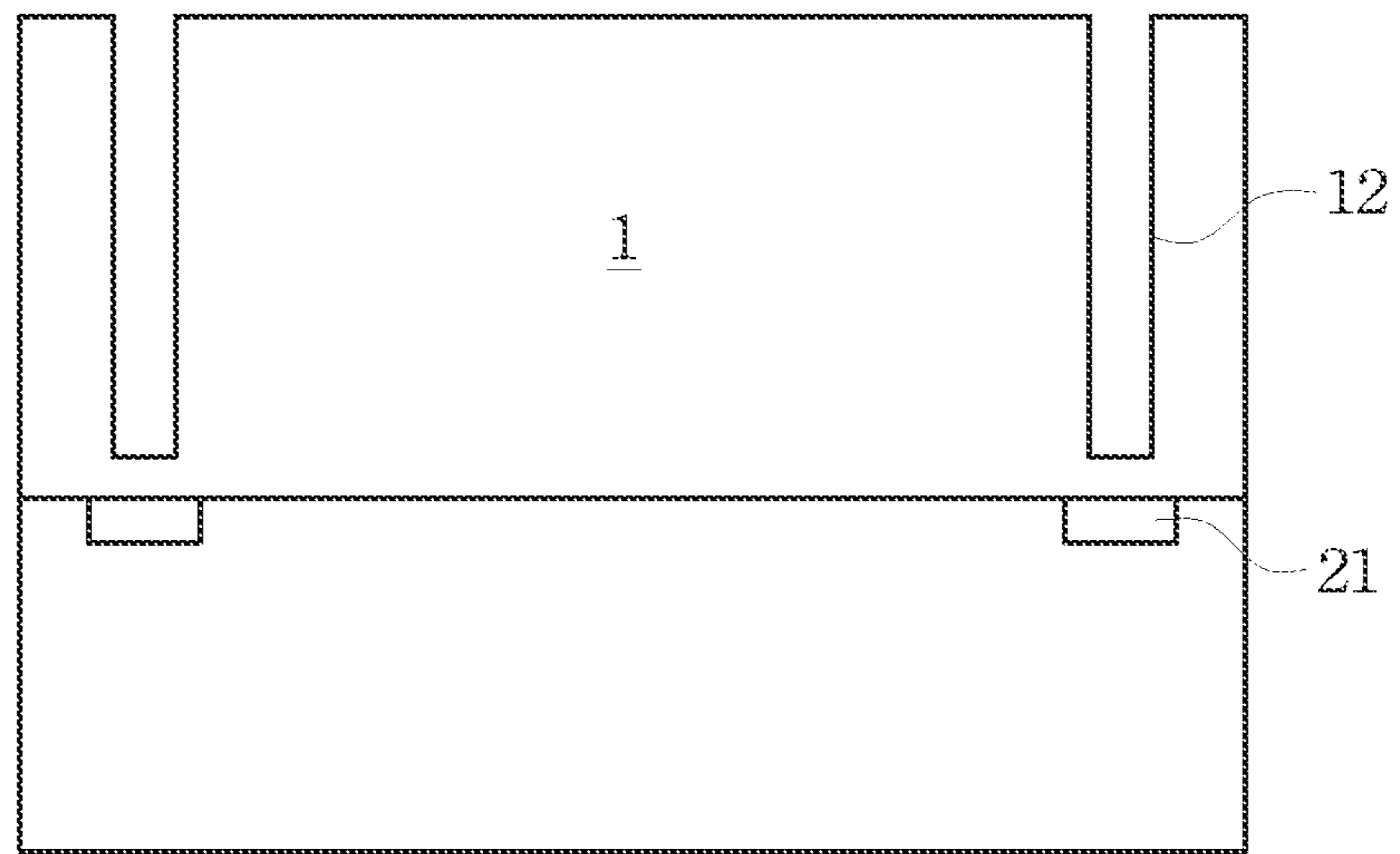


Fig. 3b

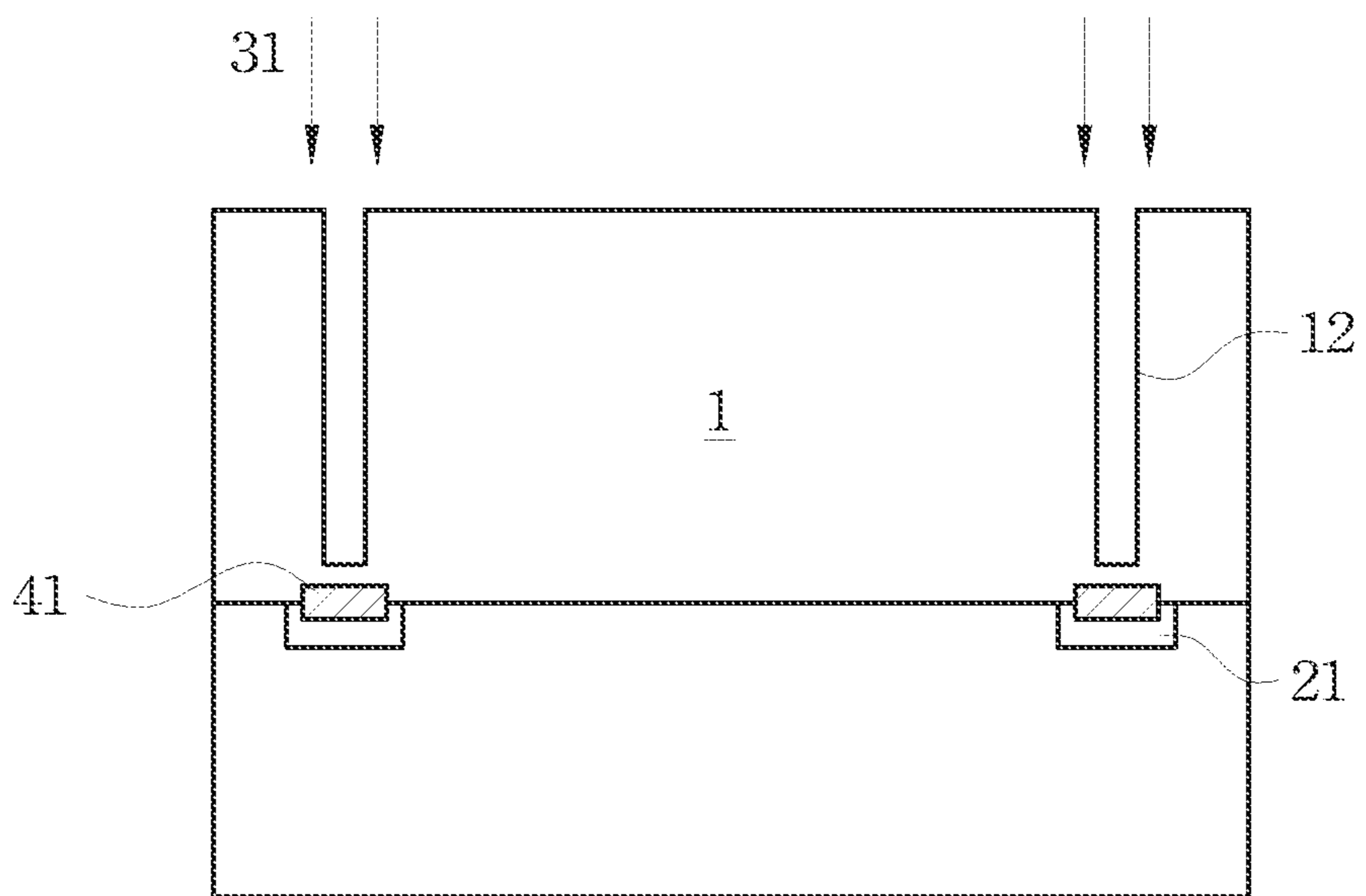


Fig. 3c

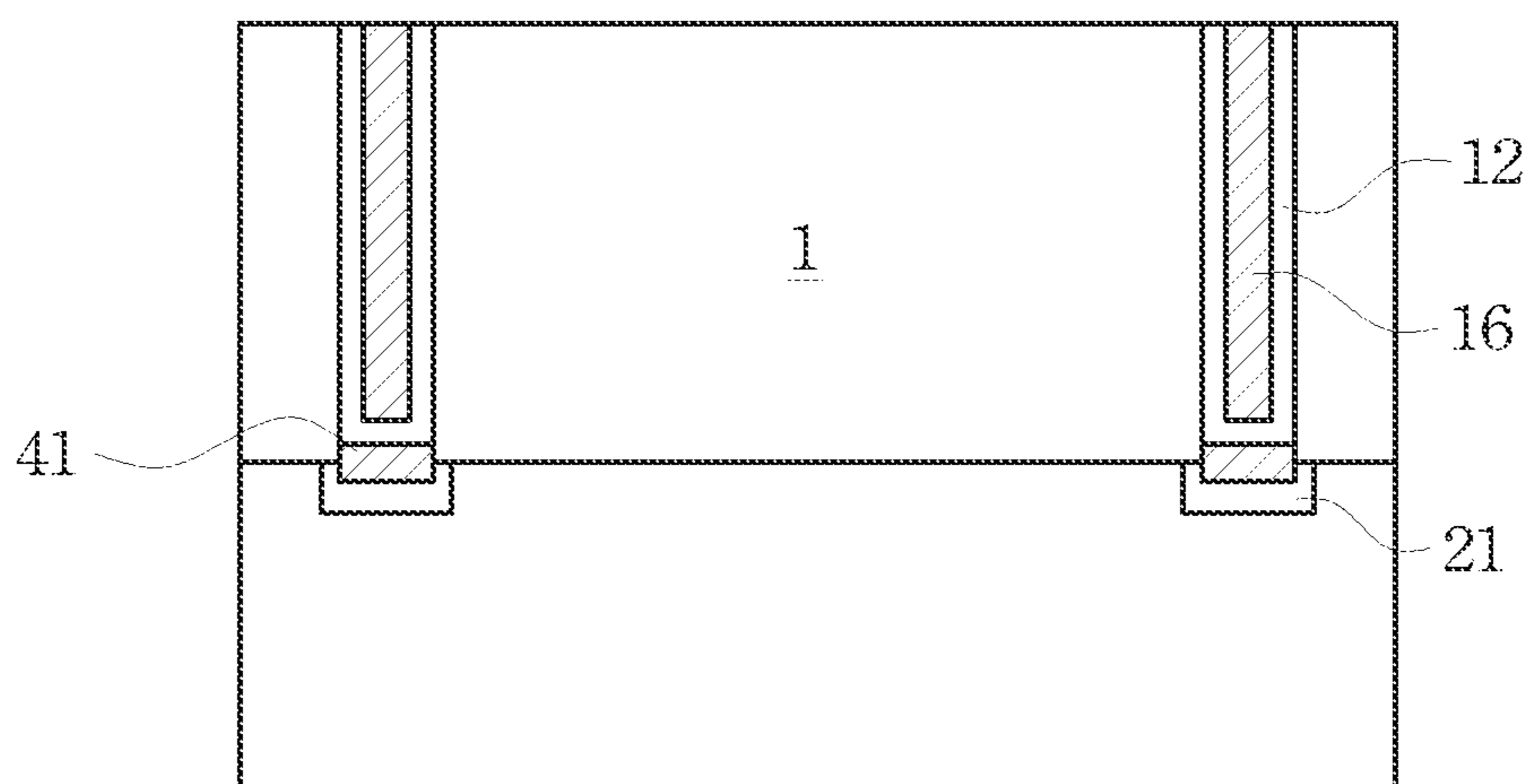


Fig. 4a

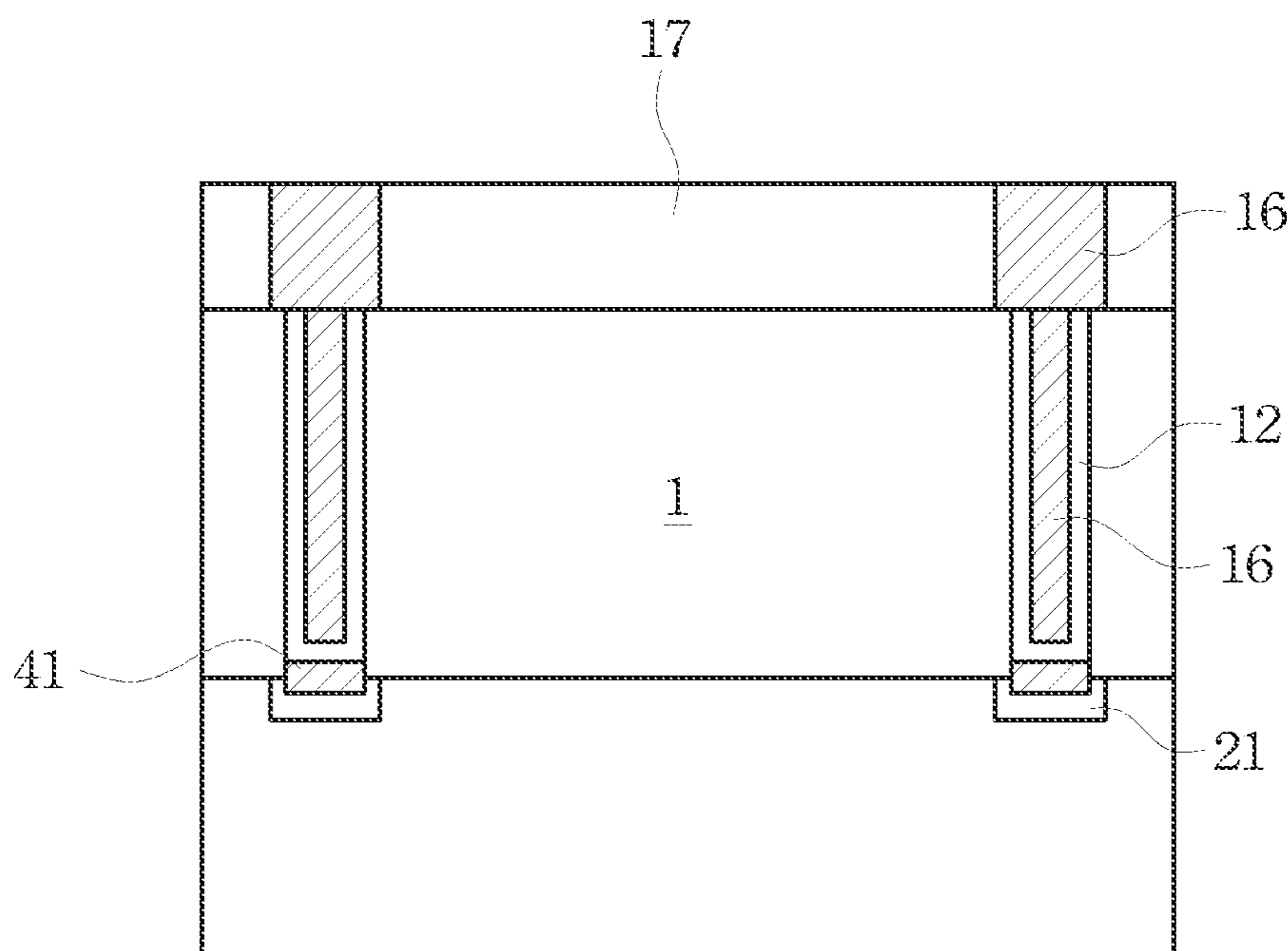


Fig. 4b

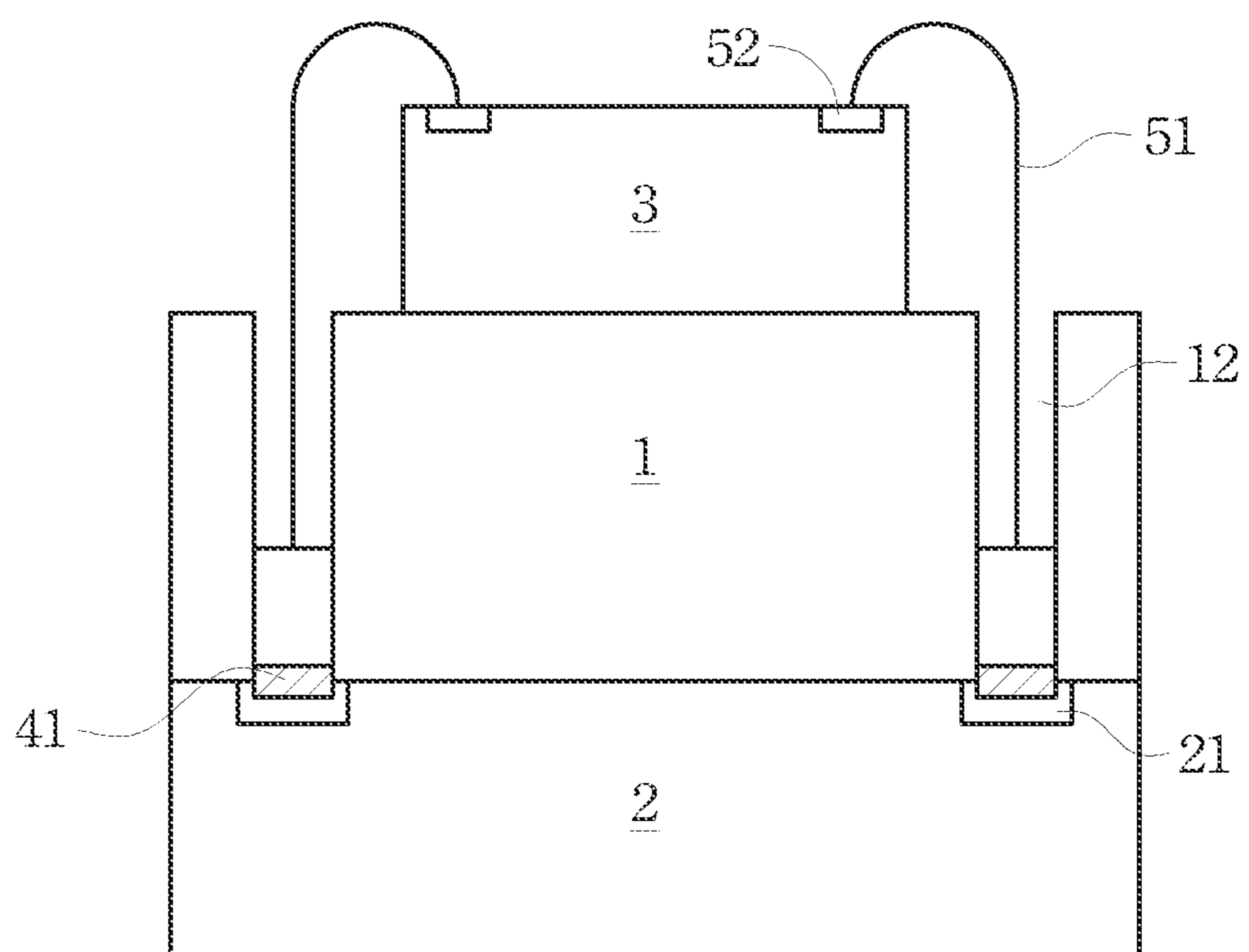


Fig. 5

1

LASER BONDING FOR STACKING SEMICONDUCTOR SUBSTRATES

This application is a continuation of U.S. patent application Ser. No. 12/618,477, filed Nov. 13, 2009 entitled "Laser Bonding for Stacking Semiconductor Substrates," which claims the benefit of U.S. Provisional Application No. 61/144,668 filed on Jan. 14, 2009, entitled "Laser Bonding for Stacking Semiconductor Substrates," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

The present invention relates generally to bonding, and more particularly to bonding for stacking semiconductor substrates using laser annealing.

BACKGROUND

One of the goals in the fabrication of electronic components is to minimize the size of various components. For example, it is desirable that handheld devices such as cellular telephones and personal digital assistants (PDAs) be as small as possible. To achieve this goal, the semiconductor circuits that are included within the devices should be as small as possible. One way of making these circuits smaller is to stack the chips that carry the circuits.

A number of ways of interconnecting the chips within the stack are known. For example, bond pads formed at the surface of each chip can be wire-bonded, either to a common substrate or to other chips in the stack. Another example is a so-called micro-bump 3D package, where each chip includes a number of micro-bumps that are routed to a circuit board, e.g., along an outer edge of the chip. However, introduction of such interconnects may introduce additional challenges.

The integration of chips brings-forth a number of new challenges that need to be addressed. One of the challenges arises due to heating required to form an adhesive bond between the two chips or between a chip and a substrate. Problems due to heating include wafer bowing as well melting of critical components within the chips. These challenges increase dramatically as the diameter of the wafer increases. Hence, what is needed in the art are improved structures and methods of producing structures for chip bonding that overcome these and other challenges.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

FIG. 1 is a structural embodiment of a semiconductor device formed in accordance with embodiments of the invention;

FIG. 2, which includes FIGS. 2a-2f, illustrates a semiconductor device in various stages of fabrication in accordance with an embodiment of the invention;

FIG. 3, which includes FIGS. 3a-3c, illustrates a semiconductor device in various stages of fabrication in accordance with an embodiment of the invention;

FIG. 4, which includes FIGS. 4a and 4b, illustrates a semiconductor device in various stages of fabrication in accordance with an embodiment of the invention; and

FIG. 5 is a structural embodiment of a semiconductor device formed in accordance with an embodiment of the invention.

2

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

Conventional bonding techniques use a wafer level heating technique that requires heating the entire wafer in a furnace. This results in unwanted heating of other sensitive components within the wafer resulting in deleterious effects to these sensitive components. For example, due to mismatch in coefficient of thermal expansion between various layers, the wafer warps. Increase in wafer warpage or wafer bowing may result in misalignment of the wafer with tools used in subsequent processing or testing. Other problems arising from increased heating of sensitive components include cracking of sensitive layers, formation of bubbles and/or residue, as well as deterioration of active devices due to boron penetration and/or dopant deactivation.

However, bonding techniques frequently require a minimum temperature for forming the adhesive layer that also forms the conductive bond. In various embodiments, embodiments of the present invention overcome these limitations by using a local heating technique that allows heating the regions that are being bonded without substantially heating the sensitive components.

The present invention will be described with respect to preferred embodiments in a specific context, namely a eutectic laser bonding technique for coupling two substrates. The invention may also be applied, however, to other bonding processes that require heating as well as to bonding individual components such as diced wafers.

A structural embodiment will be described using FIG. 1. An embodiment of a method of fabricating a stacked chip will be described in FIG. 2. Additional embodiments of fabrication are described with respect to FIGS. 3 and 4. Another structural embodiment including wire bonding techniques will be described using FIG. 5.

FIG. 1 is a structural embodiment of a semiconductor device formed in accordance with embodiments of the invention.

A first substrate 1 is stacked over a second substrate 2. The second substrate 2 comprises devices such as micro electro-mechanical devices and/or electrical devices. The first substrate 1 comprises a silicon substrate, a germanium substrate, or other compound semiconductor substrates.

Through substrate trenches 11 are disposed in the first substrate 1. The through substrate trenches 11 are disposed over the bond pads 21 of the second substrate 2. The bond pads 21 are electrically coupled to the devices in the second substrate 2. The bond pads 21 comprise a first material. The first material comprises Au, Ag, Sn, Pb, and/or Al as examples. The bond pads 21 are electrically coupled to a second material 12 disposed within the through substrate trenches 11. The second material 12 comprises Au, Ag, Sn, Pb, Al, Si, Ge, as examples. The bond pads are physically coupled to the second material 12 through a eutectic alloy

region **41**. The eutectic alloy region **41** is disposed between the second material **12** and the bond pads **21**. The eutectic alloy region **41** comprises a eutectic alloy of the first material and the second material **12**. For example, the eutectic alloy region **41** comprises a eutectic comprising Au/Si, Au/Ge, Sn/Pb, Ag/Si, Ag/Ge, or combinations thereof. In some embodiments, an optional liner **13** is disposed between the second material **12** and the first substrate **1**. The liner **13** comprises a barrier layer such as TiN or TaN.

FIG. 2, which includes FIGS. 2a-2f, illustrates a method of fabricating a stacked substrate by local bonding in accordance with embodiments of the invention.

Referring to FIG. 2a, a first substrate **1** and a second substrate **2** are independently fabricated. The second substrate **2** includes electrical circuitry and includes electrical devices such as transistors, diodes, capacitors, etc. as well as electro-mechanical structures and devices. For example, in one embodiment, the second substrate **2** comprises micro electro mechanical systems (MEMS) devices, while in another embodiment, the second substrate **2** comprises MOS devices.

In one embodiment, the first substrate **1** comprises a silicon or germanium substrate with no active circuitry or devices disposed within it. In such an embodiment, the first substrate **1** is a carrier or substrate to hold the second substrate **2**. Alternately, in another embodiment, the first substrate **1** comprises active circuitry or devices.

Referring to FIG. 2a, a through substrate trench **11** is fabricated in the first substrate **1**. The through substrate trench **11** extends from the top surface to an opposite bottom surface of the first substrate **1**. The through substrate trench **11** is fabricated using, for example, a reactive ion etcher, in one embodiment.

The second substrate **2** comprises bond pads **21** that are electrically coupled to the electrical circuitry of the second substrate **2**. The top surface of the bond pads **21** are coated with a first material, for example, by depositing the first material using a subtractive patterning process. For example, a blanket layer of the first material is deposited over the second substrate **2**, followed by selective removal of the first material by using a photo lithographic process. Alternately, the first material is a part of the bond pad, for example, part of a top metal level.

In various embodiments, the first material on the bond pads **21** of the second substrate **2** comprises gold, silver, tin, lead, aluminum, or combinations thereof. In various embodiments, the through substrate trench **11** comprises a dimension similar to the bond pads **21** of the second substrate **2**. In one embodiment, a maximum dimension of the through substrate trench **11** is smaller than the maximum dimension of the bond pads **21** by at least 20%.

Referring to FIGS. 2c and 2d, the first substrate **1** is aligned with the second substrate **2**, and stacked. FIG. 2c illustrates a cross sectional view and FIG. 2b illustrates a top view of the stacked substrates. The first substrate **1** and the second substrate **2** are aligned such that the through substrate trenches **11** are aligned with respect to the bond pads **21**.

Referring next to FIG. 2d, a second material **12** is deposited into the through substrate trenches **11**. The second material **12** comprises gold, silver, tin, lead, or combinations thereof such that the first material on the bond pads **21** and the second material **12** are capable of forming an eutectic alloy. In various embodiments, examples of eutectic alloys include Au—Si, Au—Ge, Al—Si, Al—Ge, Sn—Pb, or combinations thereof.

A liner **13** is optionally formed prior to depositing the second material to protect the first substrate **1**, and prevent out-diffusion of the second material **12** into the first substrate

1. The optional liner **13** is deposited and etched to form a spacer. In various embodiments, the liner **13** is formed before or after aligning the first substrate **1** with the second substrate **2**. The liner **13** comprises a conductive material such as TiN, or TaN, and preferably materials that are inert with respect to the first material and/or second material **12**.

The stacked substrates are locally heated using a laser source as illustrated in FIG. 2e. A laser spot beam **31** is moved over the wafer over the through substrate trenches **11**. The laser spot beam **31** is moved along a row thereby heating the first substrate only along a rectangular area with a width defined by the spot beam width. Hence, in this embodiment, regions of the first substrate **1** between adjacent through substrate trenches **11** is not heated unless they are in the direction of the movement of the laser spot beam **31**.

Alternately in another embodiment, the laser is pulsed so that the laser spot beam **31** is activated only when the laser spot beam **31** is over the through substrate trenches **11**. Thus, even along the direction of movement of the laser spot beam **31**, the regions of the first substrate **1** between adjacent through substrate trenches **11** are not heated.

In various embodiments, the power density, scan speed, and beam width of the laser spot beam **31** are selected such that the through substrate trenches **11** are locally heated up to over its eutectic temperature. For example, the through substrate trenches **11** are heated to about 365° C. for joining using a Si/Au eutectic mixture and 420° C. for joining using a Ge/Al eutectic mixture. The laser scan speed can be controlled and, in one embodiment is greater than about 100 mm/sec. In various embodiments, the laser wavelength depends on its source, which can be about 0.3 nm (X-ray), 405 nm (Blue ray) to about 648 nm (red laser).

In some embodiments, other electromagnetic radiation may be used, for example, electro magnetic radiation that is incoherent. Alternately, in some embodiments, other radiation such as ionic radiation may be used as the heating beam. Any source of energy may be used as a heating source if it can be focused into the required area and imparts the energy to the substrate.

In the through substrate trenches **11**, the first material and the second material are locally melted and form an eutectic alloy region **41** that bonds the first substrate **1** to the bond pads **21** of the second substrate **2** (FIG. 2f). Subsequent processing continues using conventional processing. For example, the second substrate **2** may be thinned from the back side by grinding/etching processes, and a protective fill material formed over the stacked substrates.

FIG. 3, which includes FIGS. 3a-3c, illustrates an embodiment of the invention wherein the trenches are not formed as through substrate openings.

Referring to FIG. 3a, a trench **111** is formed within the first substrate **1**. Unlike the through substrate trenches **11** (e.g. FIG. 2a), the trench **111** does not extend from the top surface to the bottom surface of the first substrate **1**. However, only a small layer of the first substrate **1** comprising a thickness t is disposed underneath the trench **111**. The thickness t in various embodiments varies from about 10 nm to about 100 nm. The trench **111** is aligned with the bond pads **21** of the second substrate **2** as in prior embodiment (FIG. 3b). The trench **111** is heated locally using a laser spot beam forming the eutectic alloy region **41** that bonds the first substrate **1** with the second substrate **2** (FIG. 3c).

The first substrate **1** comprises a doped substrate such that the layer of first substrate **1** with the thickness t does not increase the contact resistance to the bond pads **21** through the trenches **111**. Additionally, a low energy implant (e.g., B<1000 eV, As<2 keV) is performed to dope the bottom

5

surface of the trench 111 with a conductive material. In one embodiment, the implant is performed before heating with the laser spot beam.

FIG. 4, which includes FIGS. 4a and 4b, illustrates an embodiment of the invention using heat absorbing materials.

FIG. 4 illustrates an additional step relative to the prior embodiments of FIGS. 2 and 3. FIG. 4, unlike the prior embodiments, uses an additional heat absorbing material to concentrate or further localize the heating to a smaller zone around the bond pads 21 of the second substrate 2. By using an absorbing layer, the area of the trench is preferentially heated relative to the rest of the substrate minimizing the heat transferred to the second substrate 2. In some embodiments, the absorbing layer may be used if the trench material reflects a substantial portion of the impinging laser energy.

FIG. 4a illustrates an embodiment wherein a heat absorber layer 16 fills the through substrate trench 11. Alternately, the heat absorber layer 16 may not fill the through substrate trench 11. The heat absorber layer 16 helps to absorb more of the radiation locally over the through substrate trench 11. The heat absorber layer 16 is preferably formed over the through substrate trench 11 by filling the voids of the through substrate trench 11 (FIG. 4a), or patterned as in FIG. 4b.

FIG. 4b shows the heat absorber layer 16 formed by patterning a non heat absorbing material 17. The local presence of heat absorber layer 16 enables the use of a lower power laser source or alternately a faster laser scan speed due to improved efficiency of the heat transfer process. The heat absorber layer 16 substantially absorbs any laser radiation impacting it. The layer reflects little if any of the electromagnetic radiation emitted by the laser. In various embodiments, the heat absorber layer 16 comprises amorphous carbon including amorphous carbon doped with impurities such as nitrogen, phosphorus, fluorine, oxygen, or combinations thereof.

For example, using the heat absorber layer 16 of this embodiment, the laser spot beam may be directly along a continuous line (continuous line scan) rather than pulsing the laser. In some embodiments, pulsing the laser may be not be preferable due to misalignment issues because the laser spot beam needs to be turned on accurately when the laser spot beam is over the through substrate trench 11.

FIG. 5 illustrates an embodiment showing a third substrate 3 stacked over the stacked substrates, e.g., of FIG. 2 or FIG. 3.

A third substrate 3 is stacked over the first substrate 1. The third substrate 3 comprises electrical circuitry and includes electrical, and/or electro-mechanical devices. The third substrate 3 is coupled electrically to the second substrate 2 through the through substrate trenches 11 (or trench 111 of FIG. 3), for example, using wire bonds 51. The wire bonds 51 couple the pads 52 on the third substrate 3 to the bond pads 21 on the second substrate 2.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that many of the features, functions, processes, and materials described herein may be varied while remaining within the scope of the present invention.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines,

6

manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method of forming a semiconductor device package comprising:

aligning a first substrate and a second substrate, the first substrate having a trench formed therein, and the second substrate having a conductive element formed thereon, wherein the trench and the conductive element are aligned;

impinging a radiative beam onto the trench; and forming a bond between the conductive element and material of the first substrate.

2. The method of claim 1, wherein the material of the first substrate is a metal deposited within the trench.

3. The method of claim 2 wherein the metal is selected from the group consisting essentially of gold, silver, tin, lead, aluminum, alloys thereof, and combinations thereof.

4. The method of claim 1, wherein the material of the first substrate is a semiconductor material.

5. The method of claim 4, wherein the semiconductor material is selected from the group consisting essentially of silicon, germanium, doped silicon, doped germanium, and combinations thereof.

6. The method of claim 1, wherein forming the bond comprises forming a eutectic alloy of the conductive element and the material of the first substrate.

7. The method of claim 1, wherein impinging a radiative beam onto the trench comprises scanning a laser across a major surface of the first substrate.

8. The method of claim 7, wherein the laser is pulsed such that the radiative beam is active when the laser beam is aligned with the trench and inactive when the laser beam is not aligned with the trench.

9. The method of claim 1, wherein forming a bond between the conductive element and material of the first substrate includes heating the conductive element and the material of the first substrate to a temperature of at least about 365° C.

10. The method of claim 1, further comprising forming a liner in the trench.

11. The method of claim 1, further comprising forming a heat absorbing material in the trench.

12. The method of claim 1 further comprising aligning a third substrate on the first substrate and electrically connecting the third substrate to the second substrate through the bond.

13. The method of claim 12 wherein the third substrate is wire bonded to the bond.

14. A method of forming a semiconductor package device comprising:

aligning a plurality of trenches having been formed in a first substrate to a plurality of respective contact pads having been formed on a second substrate, the first substrate including a first material and the contact pad including a second material;

directed a heating beam onto the plurality of trenches; and forming a plurality of bonds between the first substrate and the second substrate, the plurality of bonds being formed of an alloy of the first material and the second material.

15. The method of claim 14, wherein the alloy is a eutectic alloy.

16. The method of claim **14**, wherein individual trenches of the plurality of trenches extend through the first substrate and wherein the first material is a metal deposited within the respective trenches.

17. The method of claim **14**, wherein individual trenches of the plurality of trenches extend partly through but not fully through the first substrate, and wherein the first material is a semiconductor material of which the first substrate is formed. 5

18. The method of claim **14** wherein directing the heating beam comprises scanning the heating beam across a major surface of the first substrate. 10

19. The method of claim **18**, further comprising pulsing the heating beam during the scanning operation.

20. The method of claim **14** further comprising bonding a plurality of contact pads on a third substrate to the respective contact pads on the second substrate through respective trenches. 15

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