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(12) **United States Patent**
Bangsaruntip et al.

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(45) **Date of Patent: *Aug. 13, 2013**

(54) **OMEGA SHAPED NANOWIRE TUNNEL FIELD EFFECT TRANSISTORS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 29/66 (2006.01)

(52) **U.S. Cl.**
USPC **257/24**; 257/27; 257/347; 257/E29.168

(58) **Field of Classification Search**
USPC 257/24, 38, 296, 368
See application file for complete search history.

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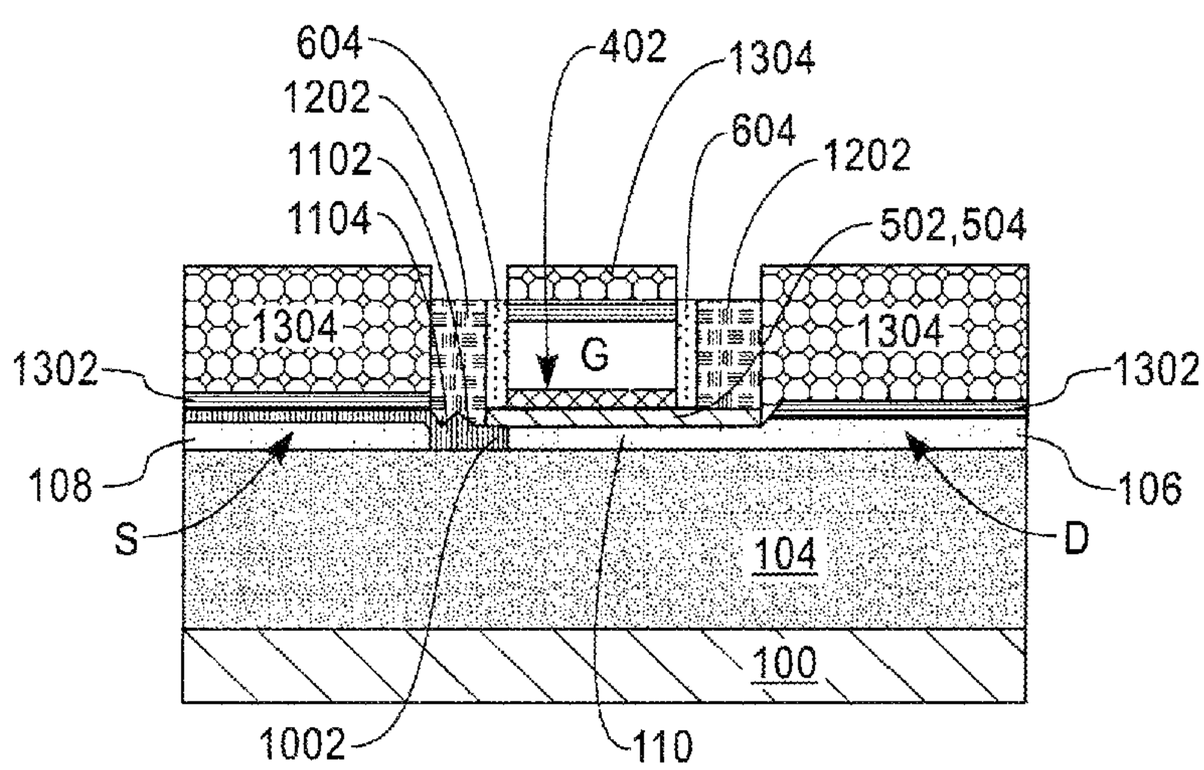
(57) **ABSTRACT**

A method for forming a nanowire tunnel field effect transistor device includes forming a nanowire connected to a first pad region and a second pad region, the nanowire including a core portion and a dielectric layer, forming a gate structure on the dielectric layer of the nanowire, forming a first protective spacer on portions of the nanowire, implanting ions in a first portion of the exposed nanowire and the first pad region, implanting in the dielectric layer of a second portion of the exposed nanowire and the second pad region, removing the dielectric layer from the second pad region and the second portion, removing the core portion of the second portion of the exposed nanowire to form a cavity, and epitaxially growing a doped semiconductor material in the cavity to connect the exposed cross sections of the nanowire to the second pad region.

7 Claims, 6 Drawing Sheets



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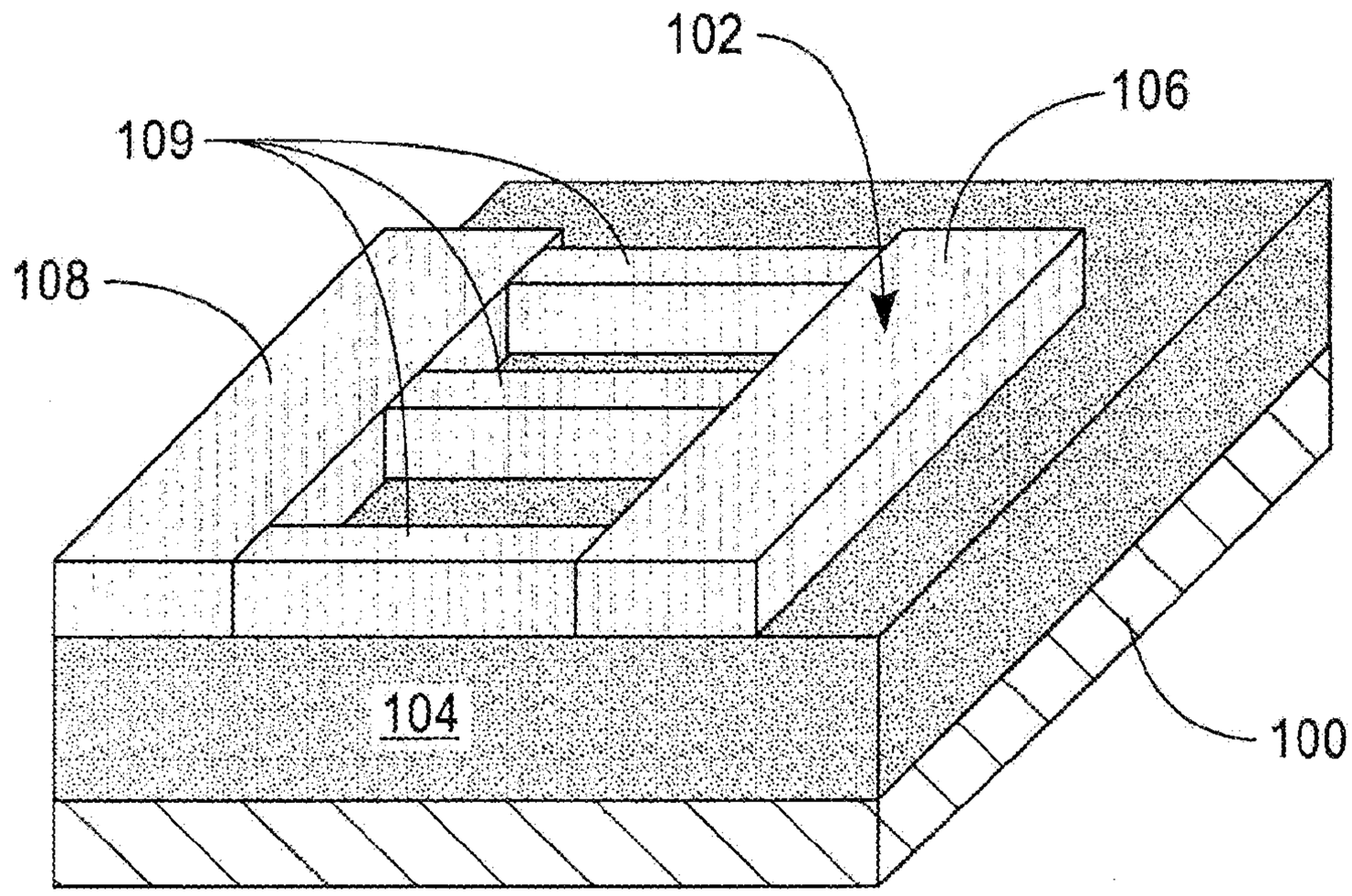
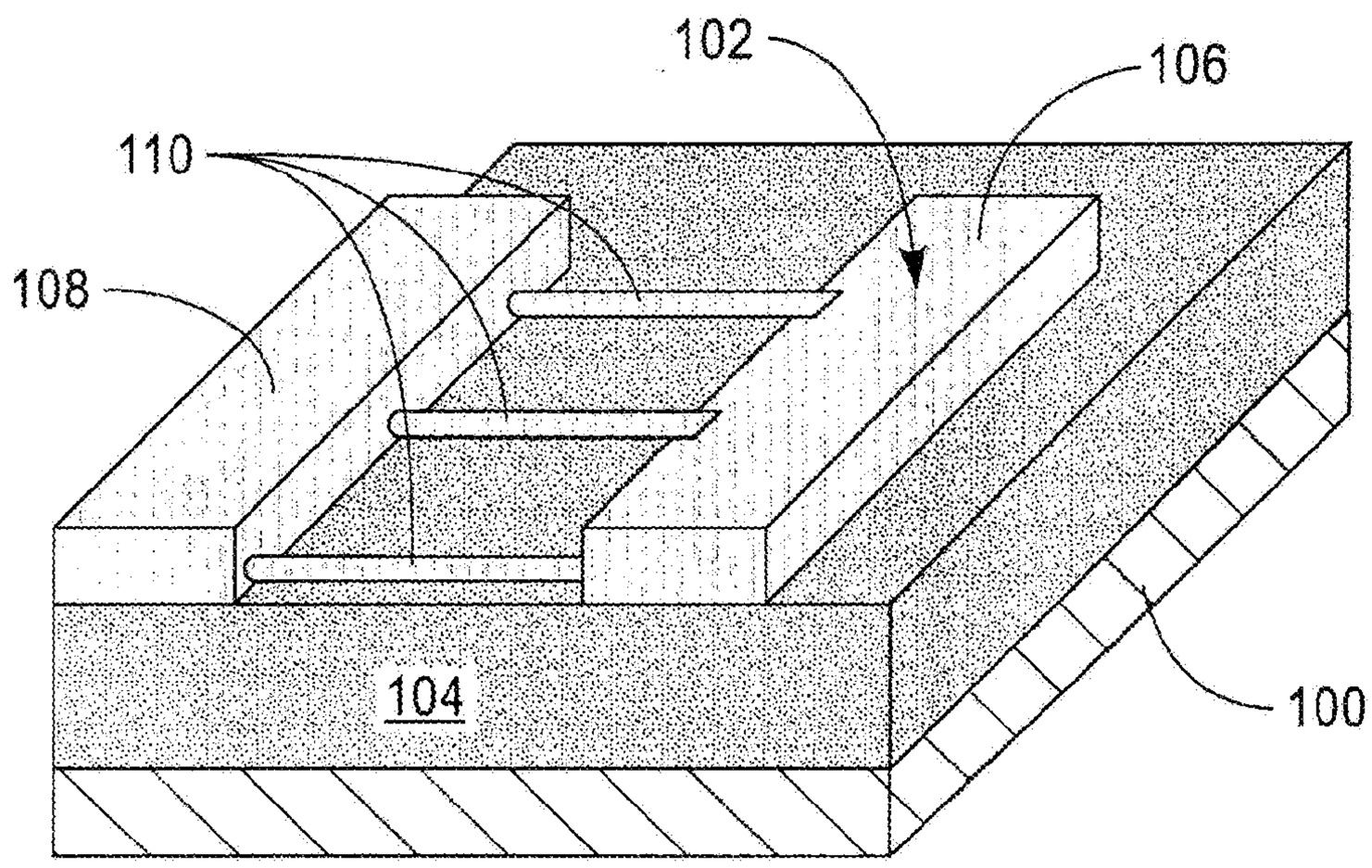


FIG. 1



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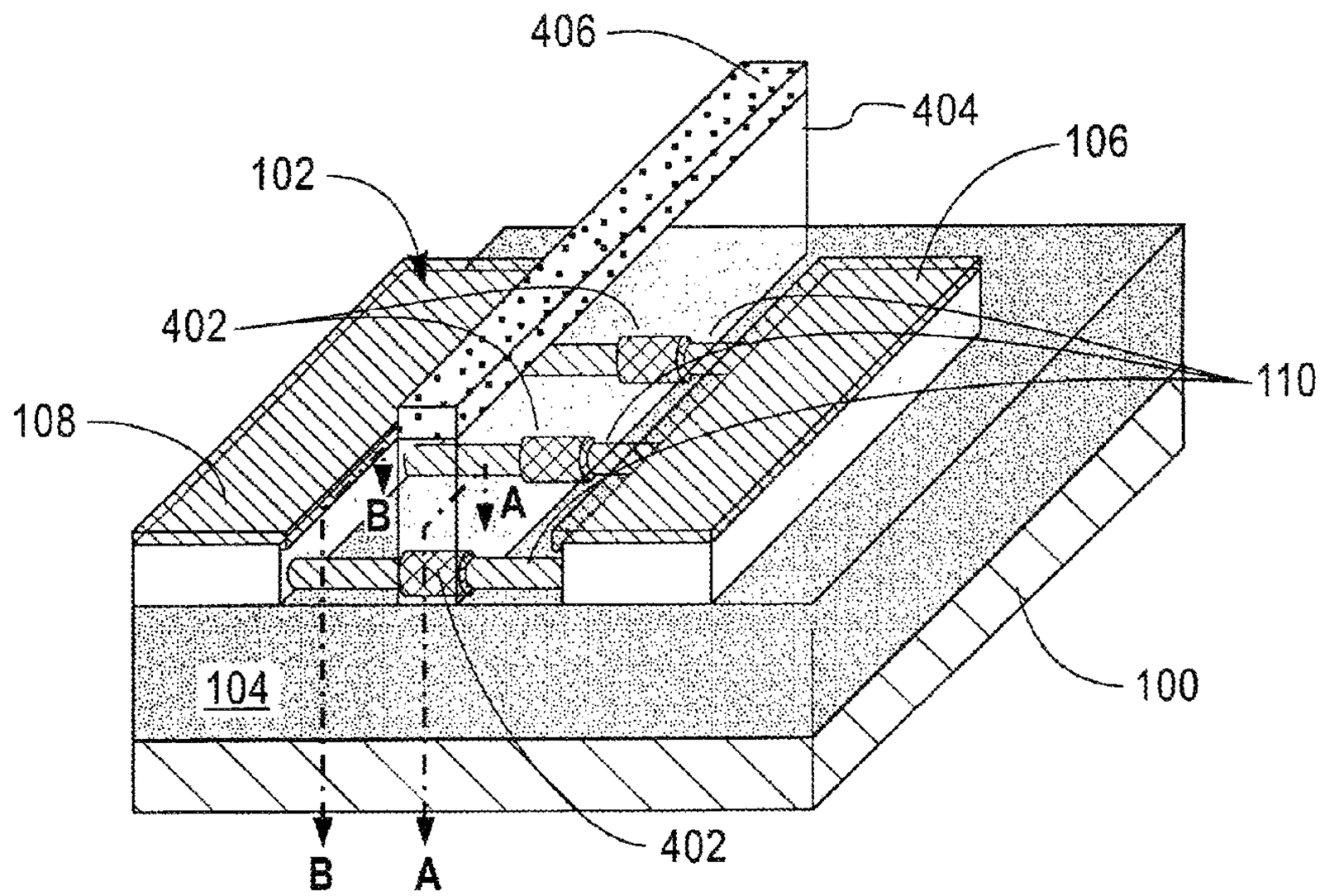

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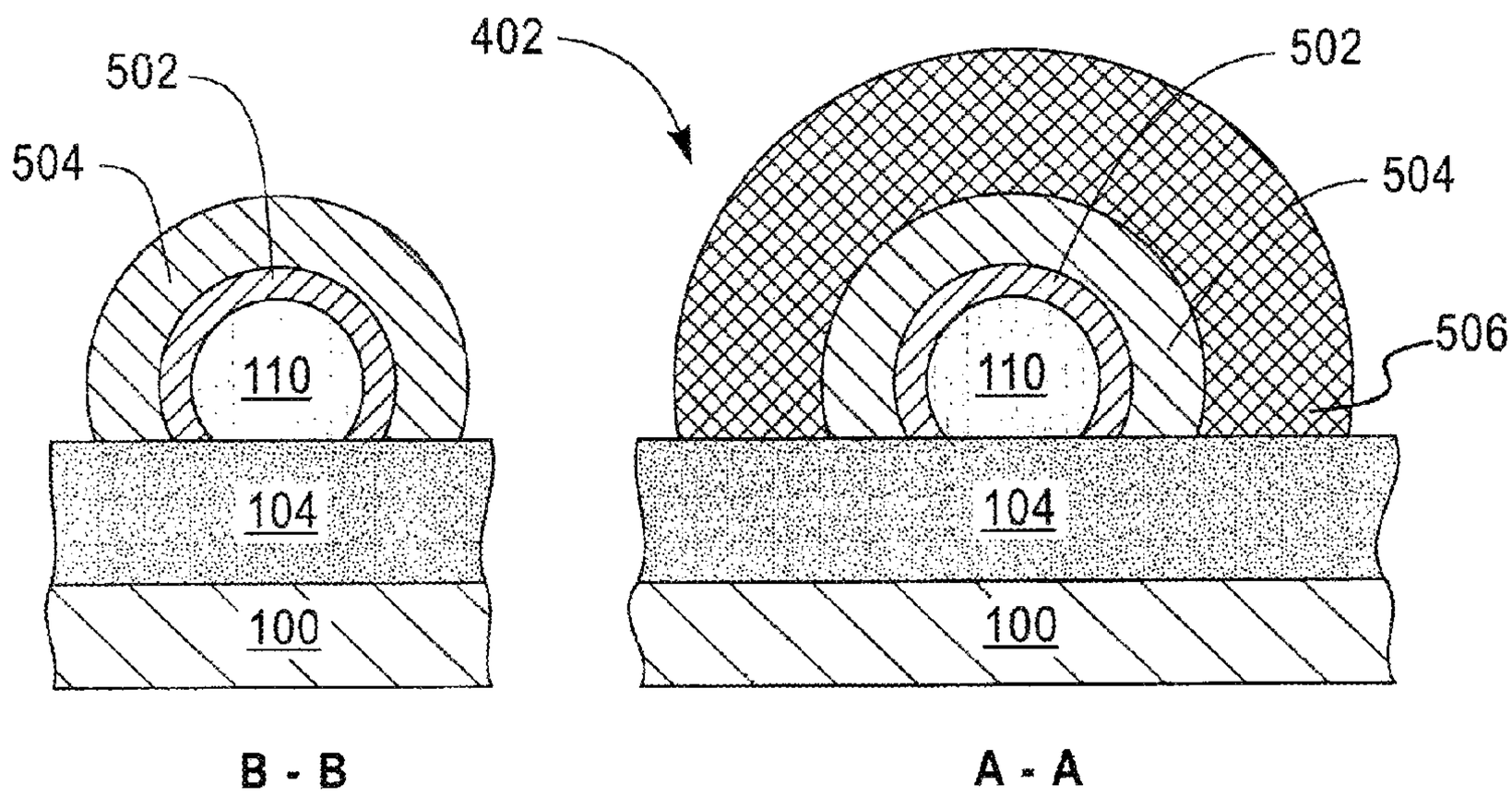
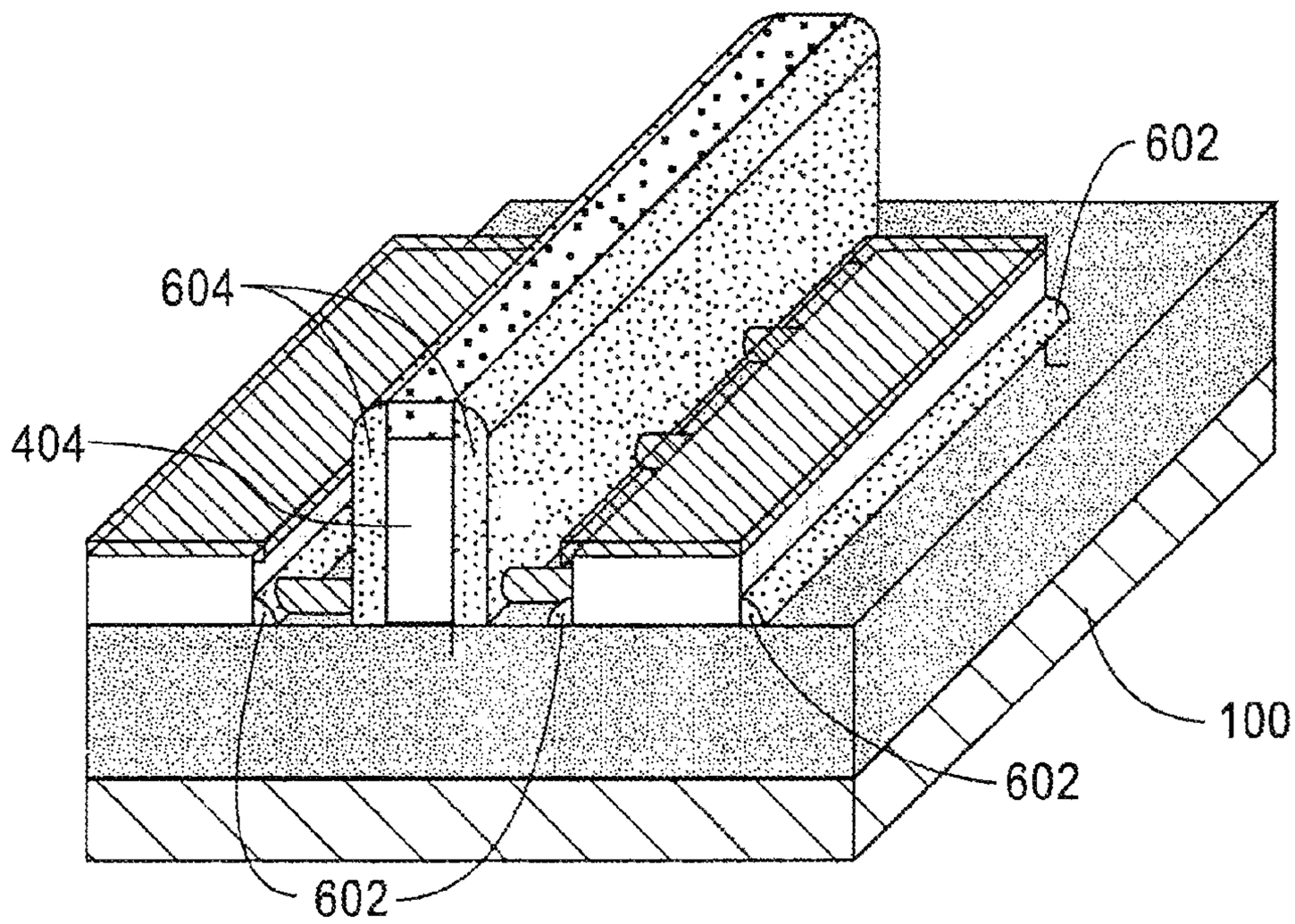


FIG. 4B FIG. 4A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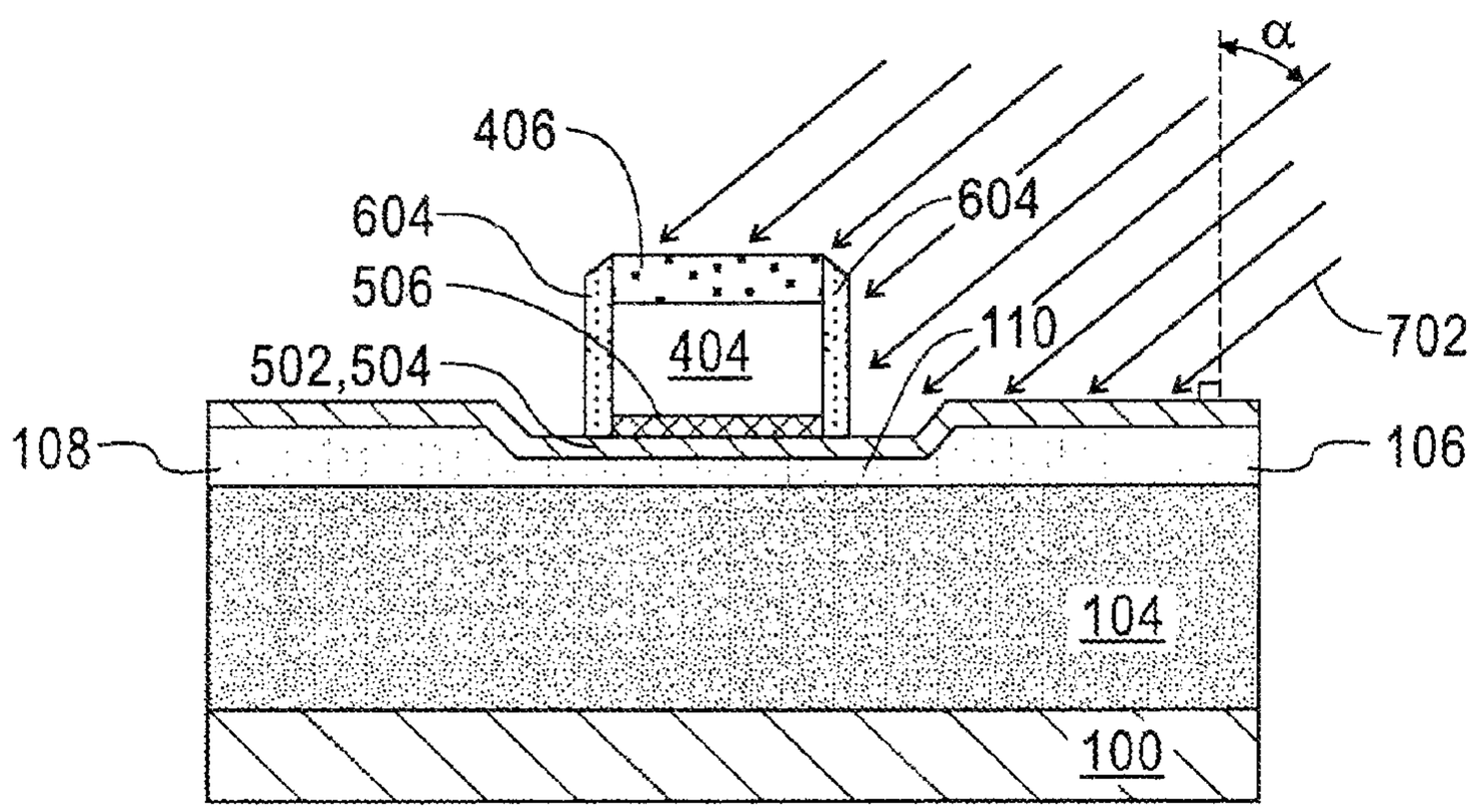
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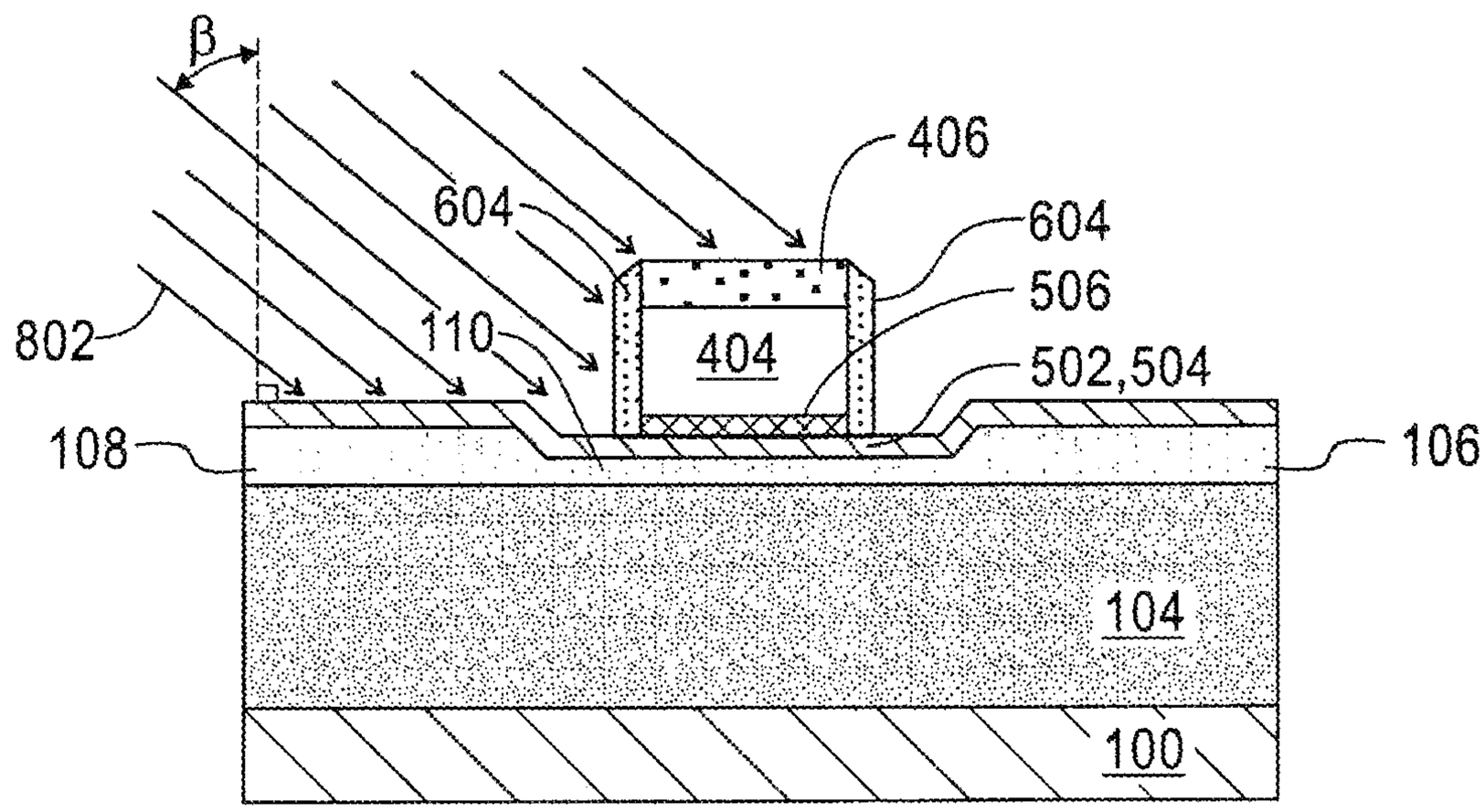
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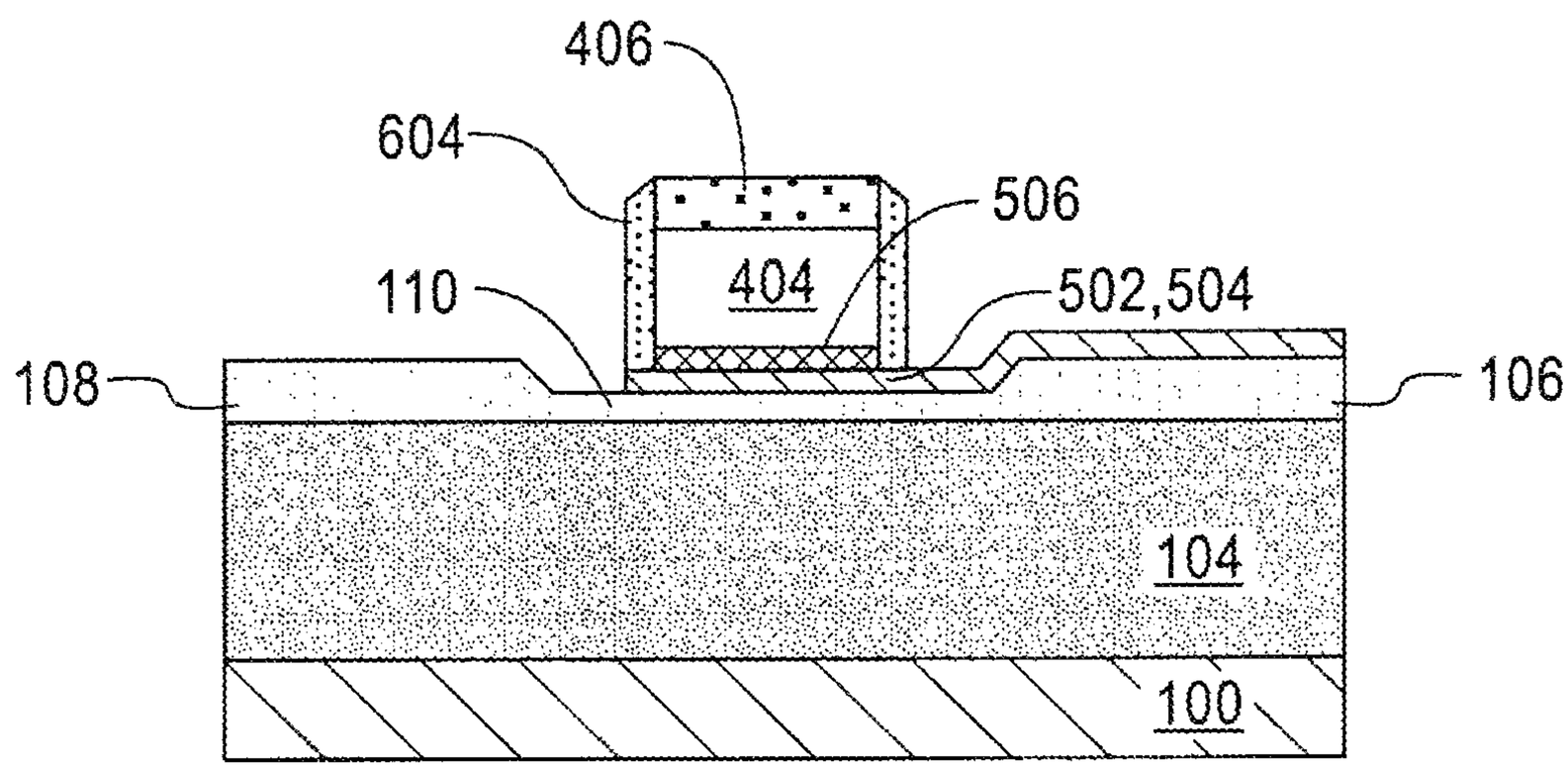
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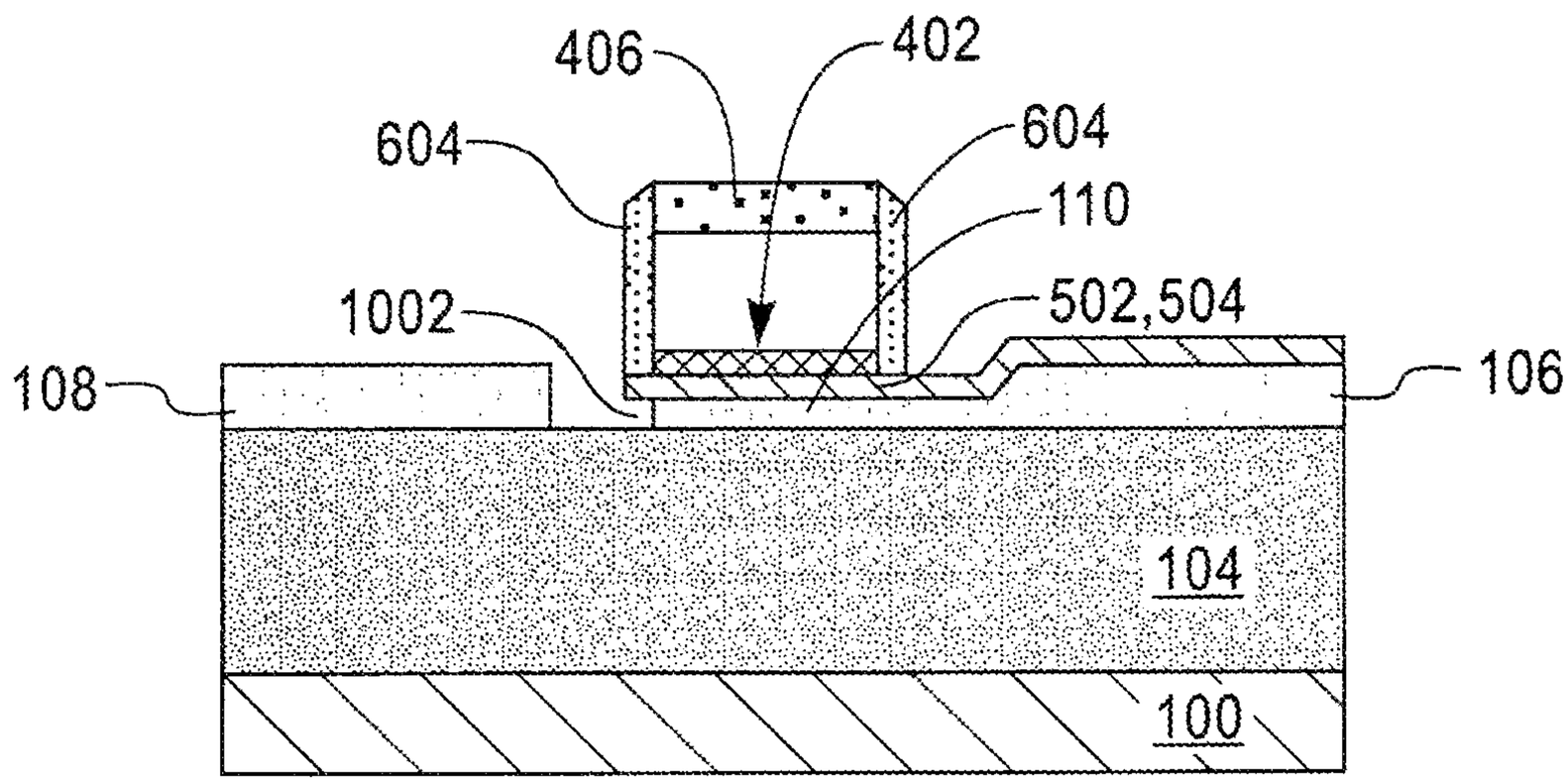
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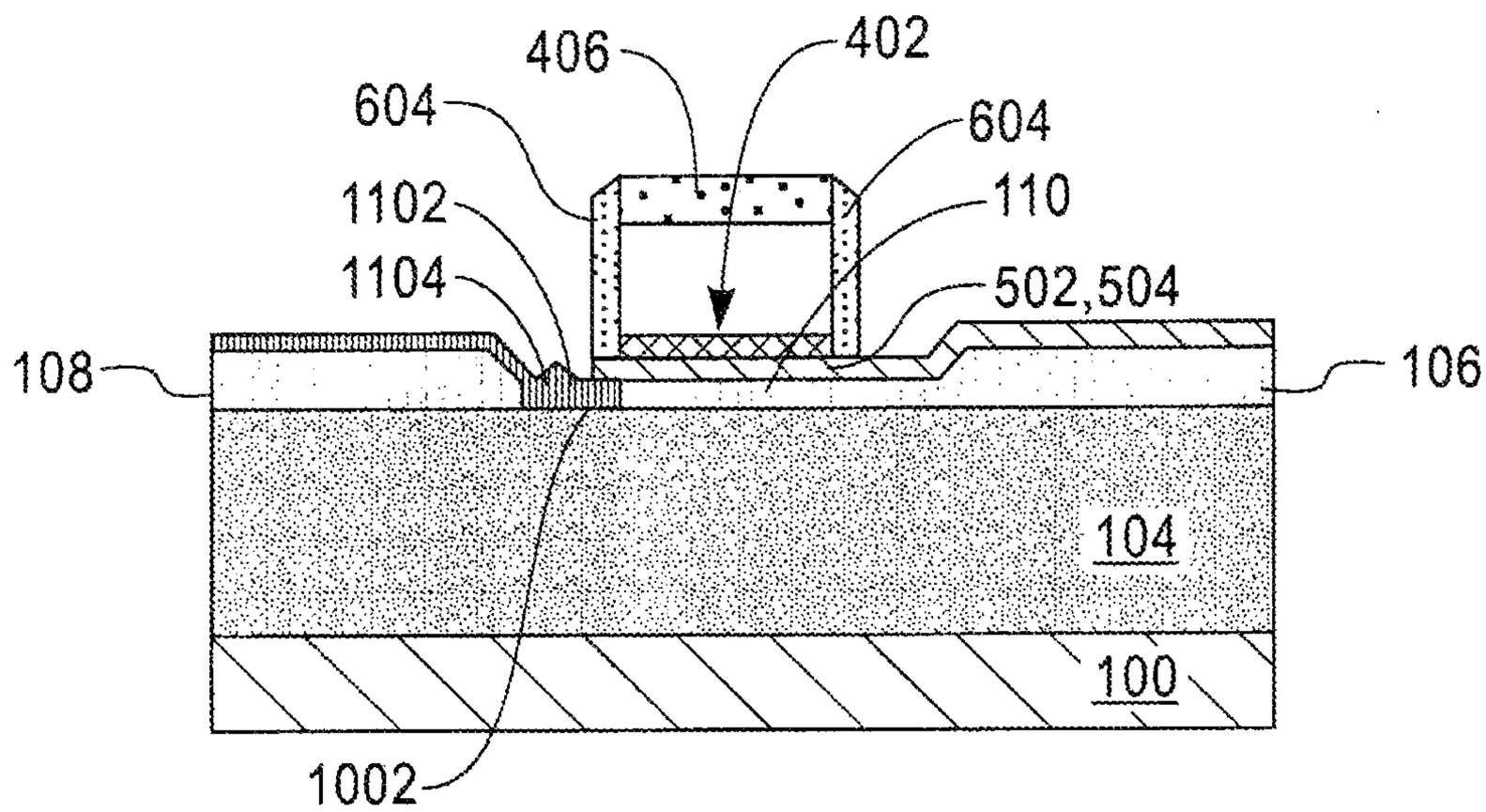
FIG. 9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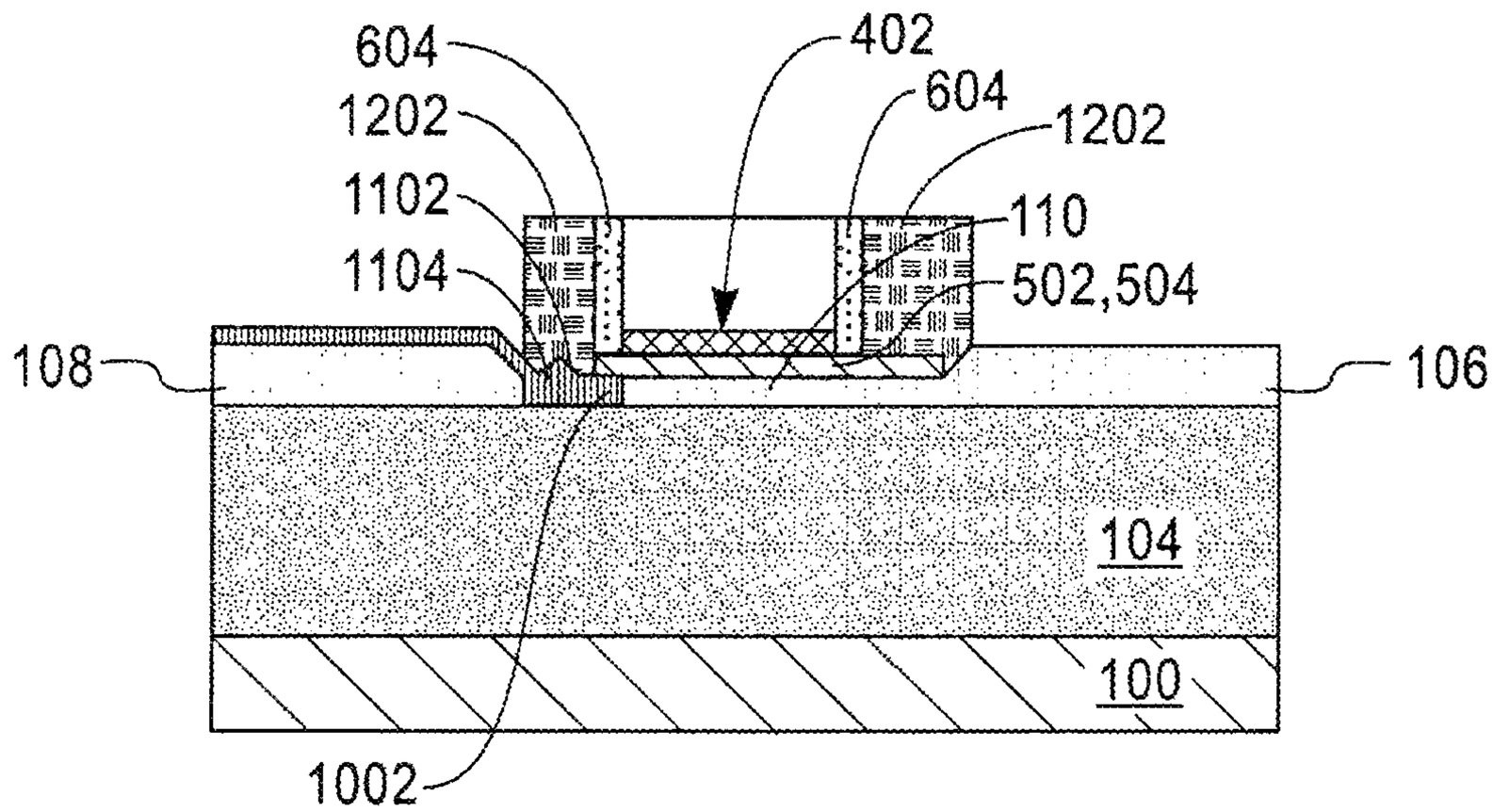
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FIG. 11

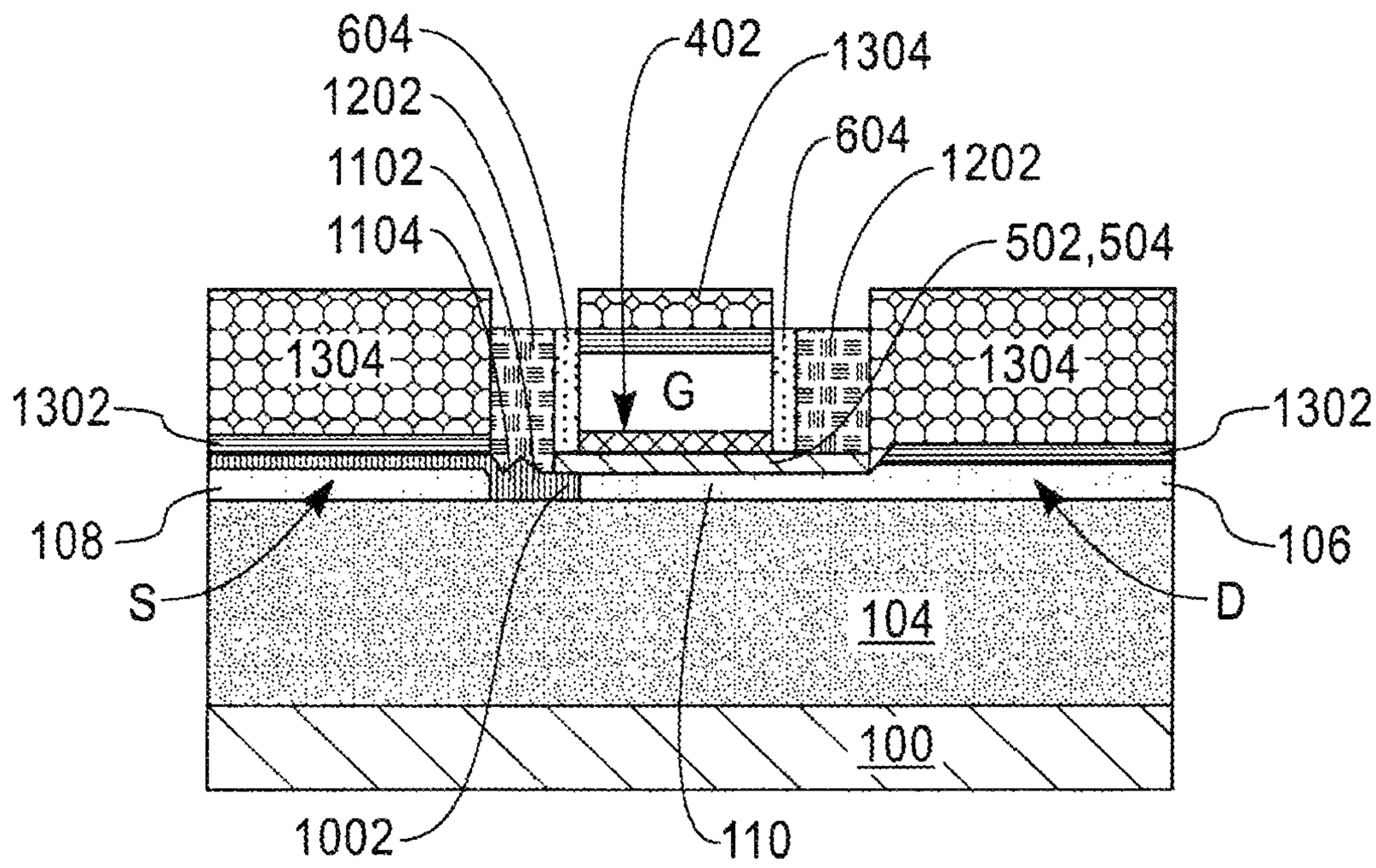
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FIG. 12

OMEGA SHAPED NANOWIRE TUNNEL FIELD EFFECT TRANSISTORS

CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Ser. No. 12/630,939, filed Dec. 4, 2009.

This application is related to co-pending application Ser. No. 12/631,199, filed Dec. 4, 2009, application Ser. No. 12/631,205, filed Dec. 4, 2009, application Ser. No. 12/630,942, filed Dec. 4, 2009, application Ser. No. 12/631,213, filed Dec. 4, 2009 and application Ser. No. 12/631,342, filed Dec. 4, 2009, all of which are incorporated by reference herein.

FIELD OF INVENTION

The present invention relates to semiconductor nanowire tunnel field effect transistors.

DESCRIPTION OF RELATED ART

A nanowire tunnel field effect transistor (FET) includes doped portions of nanowire that contact the channel region and serve as source and drain regions of the device. Previous fabrication methods that used ion-implantation to dope the small diameter nanowire may result in undesirable amorphization of the nanowire or an undesirable junction doping profile.

BRIEF SUMMARY

In one aspect of the present invention, a method for forming a nanowire tunnel field effect transistor (FET) device includes forming a nanowire connected to a first pad region and a second pad region on a semiconductor substrate, the nanowire including a core portion and a dielectric layer on the core portion, the first pad region and the second pad region including a dielectric layer, forming a gate structure on a portion of the dielectric layer of the nanowire, forming a first protective spacer adjacent to sidewalls of the gate structure and on portions of the nanowire extending from the gate structure, implanting a first type of ions in a first portion of the exposed nanowire and the first pad region, implanting a second type of ions in the dielectric layer of a second portion of the exposed nanowire and the second pad region, removing the dielectric layer from the second pad region and the second portion of the exposed nanowire to reveal the core portion of the second portion of the exposed nanowire, removing the core portion of the second portion of the exposed nanowire to form a cavity partially defined by the core portion of the nanowire surrounded by the gate structure and the spacer, and epitaxially growing a doped semiconductor material in the cavity from exposed cross sections of the nanowire and the second pad region to connect the exposed cross sections of the nanowire to the second pad region.

In another aspect of the present invention, a nanowire tunnel field effect transistor (FET) device includes a channel region disposed on a semiconductor substrate including a silicon portion having a first distal end and a second distal end, the silicon portion is surrounded by a gate structure disposed on the silicon portion, a drain region including an n-type doped silicon portion extending from the first distal end, a cavity partially defined by the second distal end of the silicon portion and an inner diameter of the gate structure, a source region including a doped epi-silicon nanowire extension epitaxially extending from the second distal end of the silicon portion in the cavity.

Additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention. For a better understanding of the invention with the advantages and the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIGS. **1-12** illustrate an exemplary method for forming a tunnel field effect transistor (FET) device.

DETAILED DESCRIPTION

With reference now to FIG. **1**, a silicon on insulator (SOI) portion **102** is defined on a buried oxide (BOX) layer **104** that is disposed on a silicon substrate **100**. The SOI portion **102** includes a SOI pad region **106**, a SOI pad region **108**, and nanowire portions **109**. The SOI portion **102** may be patterned by the use of lithography followed by an etching process such as, for example, reactive ion etching (RIE).

FIG. **2** illustrates nanowires **110** disposed on the BOX layer **104** that are smoothed to form elliptical shaped (and in some cases, cylindrical shaped) nanowires **110** on the BOX layer **104**. The smoothing of the nanowires may be performed by, for example, annealing of the nanowires **109** in hydrogen. Example annealing temperatures may be in the range of 600° C.-900° C., and a hydrogen pressure of approximately 600 torr to 7 torr. The diameter of the nanowires **110** may be reduced by an oxidation process. The reduction of the diameter of the nanowires **110** may be performed by, for example, an oxidation of the nanowires **110** followed by the etching of the grown oxide. The oxidation and etching process may be repeated to achieve a desired nanowire **110** diameter. Once the diameters of the nanowires **110** have been reduced, gates are formed over the channel regions of the nanowires **110** (described below).

FIG. **3** illustrates gates **402** that are formed on the nanowires **110**, as described in further detail below, and capped with a polysilicon layer (capping layer) **404**. A hardmask layer **406**, such as, for example silicon nitride (Si_3N_4) is deposited over the polysilicon layer **404**. The polysilicon layer **404** and the hardmask layer **406** may be formed by depositing polysilicon material over the BOX layer **104** and the SOI portion **102**, depositing the hardmask material over the polysilicon material, and etching by RIE to form the polysilicon layer **406** and the hardmask layer **404**. The etching of the gate **402** may be performed by directional etching that results in straight sidewalls of the gate **402**. Following the directional etching, polysilicon **404** remains under the nanowires **110** and outside the region encapsulated by the gate **402**. Isotropic etching may be performed to remove polysilicon **404** from under the nanowires **110**.

FIG. **4**A illustrates a cross sectional view of a gate **402** along the line A-A (of FIG. **3**). The gate **402** is formed by depositing a first gate dielectric layer (high K layer) **502**, such as silicon dioxide (SiO_2) around a channel portion of the

nanowire **110** and on the SOI pad regions **106** and **108**. A second gate dielectric layer (high K layer) **504** such as, for example, hafnium oxide (HfO_2) is formed around the first gate dielectric layer **502**. A metal layer **506** such as, for example, tantalum nitride (TaN) is formed on the second gate dielectric layer **504**. The metal layer **506** is surrounded by polysilicon layer **404** (of FIG. **3**). Doping the polysilicon layer **404** with impurities such as boron (p-type), or phosphorus (n-type) makes the polysilicon layer **404** conductive. The metal layer **506** is removed by an etching process such as, for example, RIE from the nanowire **110** and the SOI pad regions **106** and **108** that are outside of the channel region, and results in the gate **402**. FIG. **4**B illustrates a cross sectional view of a portion of the nanowire **110** along the line B-B (of FIG. **3**).

FIG. **5** illustrates the spacer portions **604** formed along opposing sides of the polysilicon layer **404**. The spacers are formed by depositing a blanket dielectric film such as silicon nitride and etching the dielectric film from all horizontal surfaces by RIE. The spacer walls **604** are formed around portions of the nanowire **110** that extend from the polysilicon layer **404** and surround portions of the nanowires **110**.

FIG. **6** illustrates a cross-sectional view of FIG. **5** following the formation of the spacers **604**. In the illustrated embodiment, the exposed dielectric layers **502** and **504** on one side of the device are doped with n-type ions **702** that are implanted at an angle (α), the angle α may, for example, range from 5-50 degrees. The implantation of the n-type ions **702** at the angle a exposes one side of the device to the n-type ions **702**, while the opposing side remains unexposed due to the height and position of the polysilicon layer **404**. Once the ions **702** are implanted, an annealing process is performed to overlap the device. The annealing process results in a shallow doping gradient of n-type ions in the channel region of the device.

FIG. **7** illustrates a cross-sectional view of the device. In the illustrated embodiment the exposed dielectric layers **502** and **504** on the opposing side of the device (the un-doped side) is implanted with ions **802** at an angle (β). The ions **802** may include, for example, germanium, argon, or xenon. The implantation of the ions **802** at the angle β in the dielectric layers **502** and **504** damages the dielectric layers dielectric layers **502** and **504** on the un-doped side of the device, while the doped side of the device remains unexposed to the ions **802**.

FIG. **8** illustrates a cross-sectional view of the resultant structure following a wet etching process such as, for example, a HF chemical etch that removes the damaged dielectric layers **502** and **504** that were implanted with the ions **802** (of FIG. **8**) from the nanowire **110**. The n-type doped dielectric layers **502** and **505** remain on the nanowire **110**.

FIG. **9** illustrates a cross-sectional view of the resultant structure following an etching process, such as, for example, a wet chemical or vapor etching process that etches exposed silicon, and removes the exposed silicon nanowire **110**. The etching process removes a portion of the nanowire **110** that is surrounded by the spacer wall **604** and the gate **402** to recess the nanowires **110** into the gates **402**, and form a cavity **1002** defined by the gate **402**, the nanowire **110**, the BOX layer **104**, and the spacer wall **604**.

The lateral etching process that forms cavity **1002** may be time based. Width variation in spacer **604** may lead to variations in the position of the edges of the recessed nanowire **110**. The etching rate in the cavity **1002** depends on the size of the cavity, with narrower orifice corresponding to slower etch rates. Variations in the nanowire size will therefore lead to variations in the depth of cavity **1002**.

FIG. **10** illustrates cross-sectional views of the resultant structures following a selective epi-silicon growth to form nanowire extensions **1102** and **1104**. The nanowire extension **1102** is epitaxially grown in the cavity **1022** (of FIG. **9**) from the exposed nanowire **110** in the gate **402** to form the nanowire extension **1102**. The nanowire extension **1104** is epitaxially grown from the SOI pad region **108**. The nanowire extensions **1102** and **1104** are grown until they meet to connect the SOI pad region **108** to the nanowire **110** in the channel region of the gate **402**. The nanowire extensions **1102** and **1104** are formed by epitaxially growing, for example, in-situ doped silicon (Si), a silicon germanium (SiGe), or germanium (Ge) that may be either n-type or p-type doped. As an example, a chemical vapor deposition (CVD) reactor may be used to perform the epitaxial growth. Precursors for silicon epitaxy include $SiCl_4$, SiH_4 combined with HCL. The use of chlorine allows selective deposition of silicon only on exposed silicon surfaces. A precursor for SiGe may be GeH_4, which may obtain deposition selectivity without HCL. Precursors for dopants may include PH_3 or AsH_3 for n-type doping and B_2H_6 for p-type doping. Deposition temperatures may range from 550° C. to 1000° C. for pure silicon deposition, and as low as 300° C. for pure Ge deposition.

Once epi-nanowire extensions **1102** and **1104** are formed, the doping may be activated by, for example, a laser or flash anneal process. The laser or flash annealing may reduce diffusion of ions into the channel region **1105** of the gate **402**, and result in a high uniform concentration of doping in the epi-nanowire extensions **1102** and **1104** with an abrupt junction in the nanowires **110**.

FIG. **11** illustrates a cross-sectional view of the structure following the formation of a spacer **1202**. The spacer **1202** is formed by depositing a layer of spacer material such as, for example, silicon nitride or silicon dioxide and etching the spacer material using, for example, RIE to form the spacers **1202**. The hardmask layer **406** may also be removed in the RIE process.

FIG. **12** illustrates the resultant structure following silicidation where a silicide **1302** is formed on the SOI pad region **106** (the drain region D) and the SOI pad region **108** (the source region S), and over the polysilicon layer **404** (the gate region G). Examples of silicide forming metals include Ni, Pt, Co, and alloys such as NiPt. When Ni is used the NiSi phase is formed due to its low resistivity. For example, formation temperatures include 400-600° C. Once the silicidation process is performed, capping layers and vias for connectivity (not shown) may be formed and a conductive material such as, Al, Au, Cu, or Ag may be deposited to form contacts **1304**.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one ore more other features, integers, steps, operations, element components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and

spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated

The diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the spirit of the invention. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

While the preferred embodiment to the invention had been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

What is claimed is:

1. A nanowire tunnel field effect transistor (FET) device, comprising:

a channel region disposed on a semiconductor substrate including a silicon portion having a first distal end and a second distal end, the silicon portion is surrounded by a gate structure disposed on the silicon portion;

a drain region including an n-type doped silicon portion extending from the first distal end;

a cavity partially defined by the second distal end of the silicon portion and an inner diameter of the gate structure;

a source region including a doped epi-silicon nanowire extension epitaxially extending from the second distal end of the silicon portion in the cavity.

2. The device of claim **1**, wherein the n-type doped silicon portion is connected to a first pad region disposed on the semiconductor substrate.

3. The device of claim **1**, wherein the doped epi-silicon nanowire extension is connected to a second pad region disposed on the semiconductor substrate.

4. The device of claim **2**, wherein the first pad region includes a silicide material.

5. The device of claim **3**, wherein the second pad region includes a silicide material.

6. The device of claim **1**, wherein the epi-silicon nanowire extension fills the cavity.

7. The device of claim **1**, wherein the epi-silicon nanowire extension is uniformly doped.

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