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(54) **DC-DC CONVERTER**

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323/275, 282-290; 315/101, 166, 171, 194,
315/219, 221, 223, 224, 175, 291, 307
See application file for complete search history.

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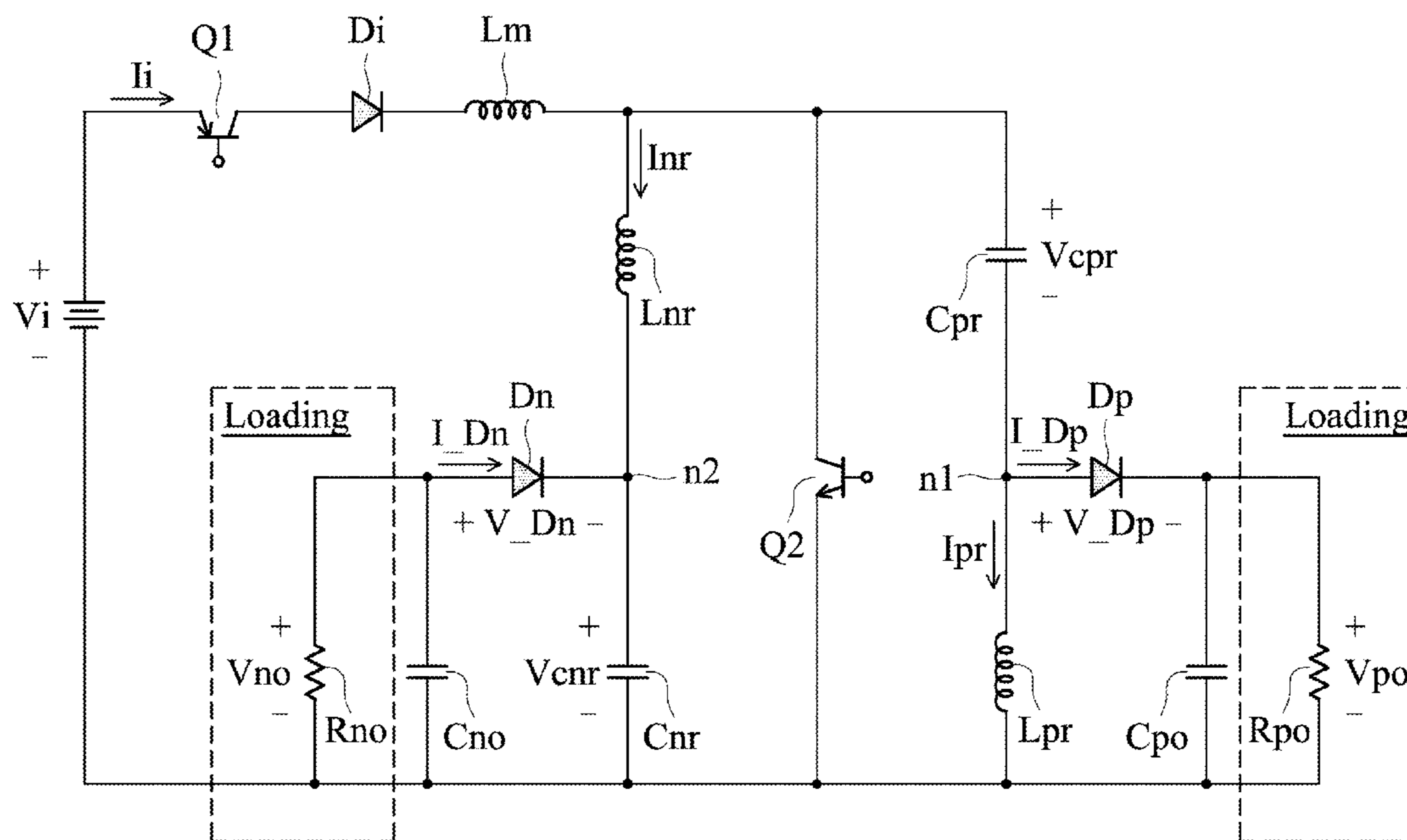
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(57) **ABSTRACT**

A DC-DC converter having a first and a second switch, an input diode, a magnetizing inductor, a resonant capacitor, a resonant inductor, an output diode and an output filter capacitor. The first and second switches are turned on alternatively. When the first switch is turned on, an input voltage is coupled to an anode of the input diode that has a cathode coupled to a first terminal of the magnetizing inductor. The second switch is designed to short a second terminal of the magnetizing inductor to a ground. The resonant capacitor and inductor, which are coupled in series, are disposed between the second terminal of the magnetizing inductor and the ground. A connection node between the resonant capacitor and inductor is coupled to the output filter capacitor, via the output diode, to regulate a voltage of the output filter capacitor. The regulated voltage is used in powering a load.

19 Claims, 4 Drawing Sheets



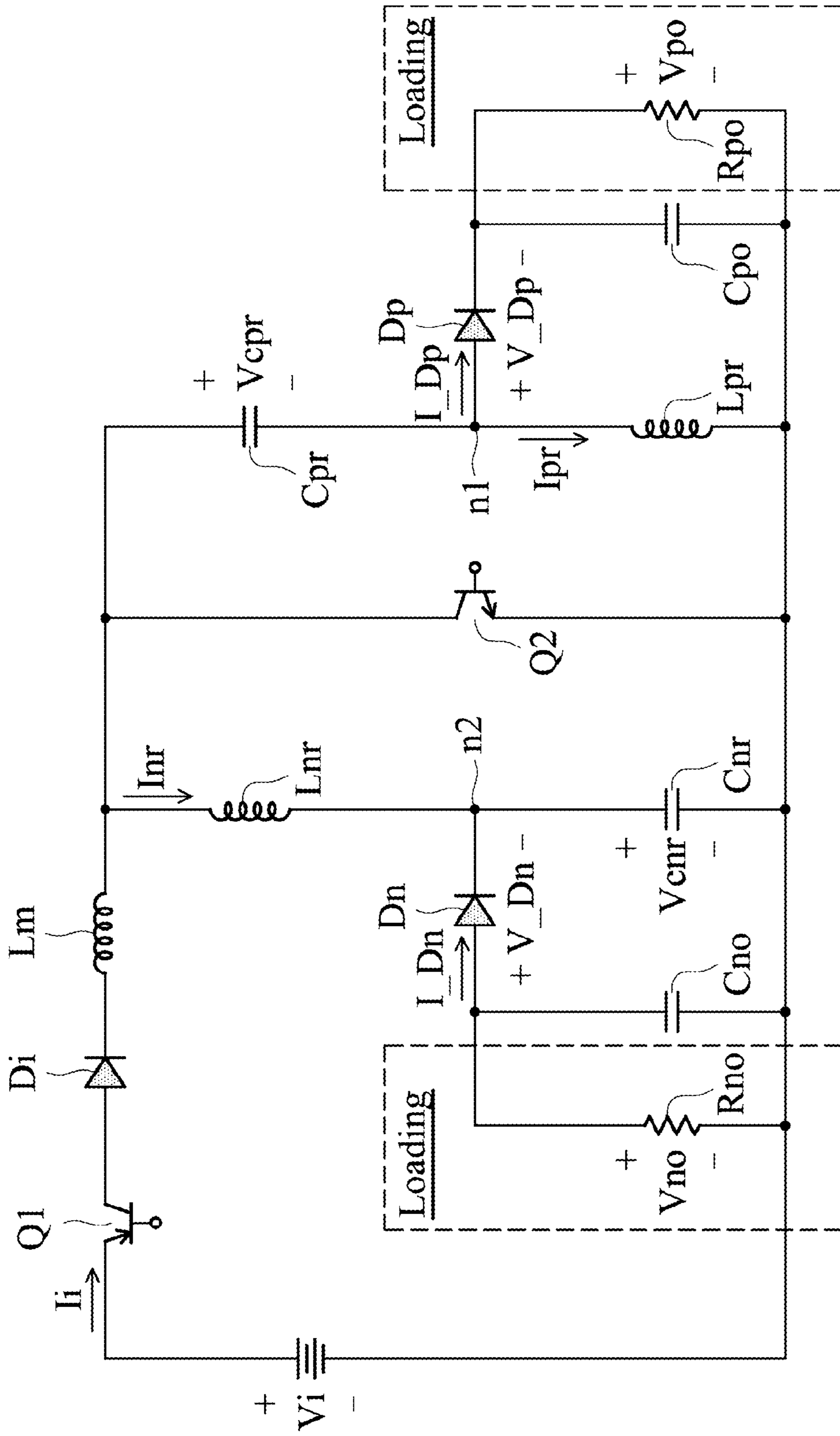


FIG. 1

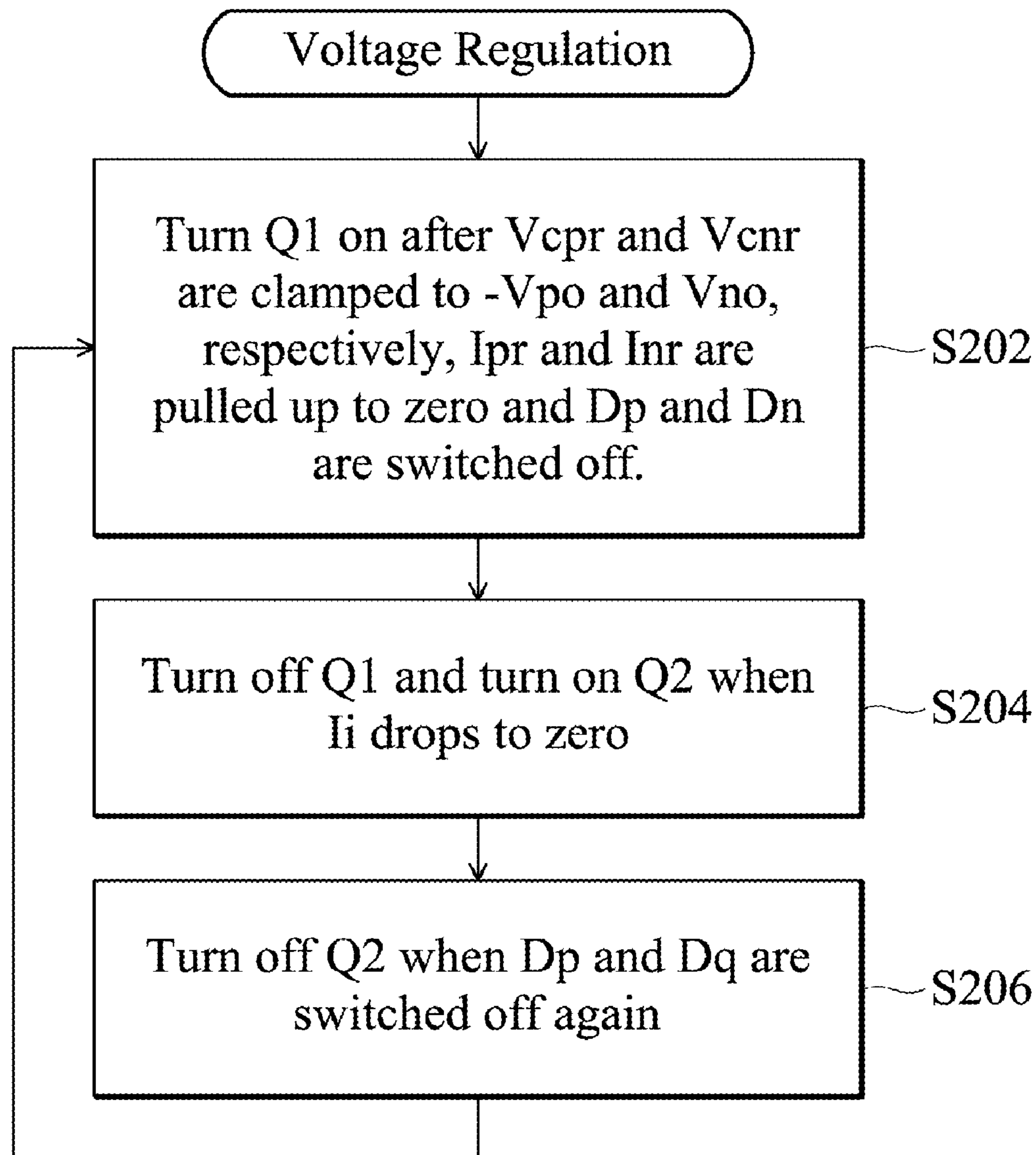


FIG. 2

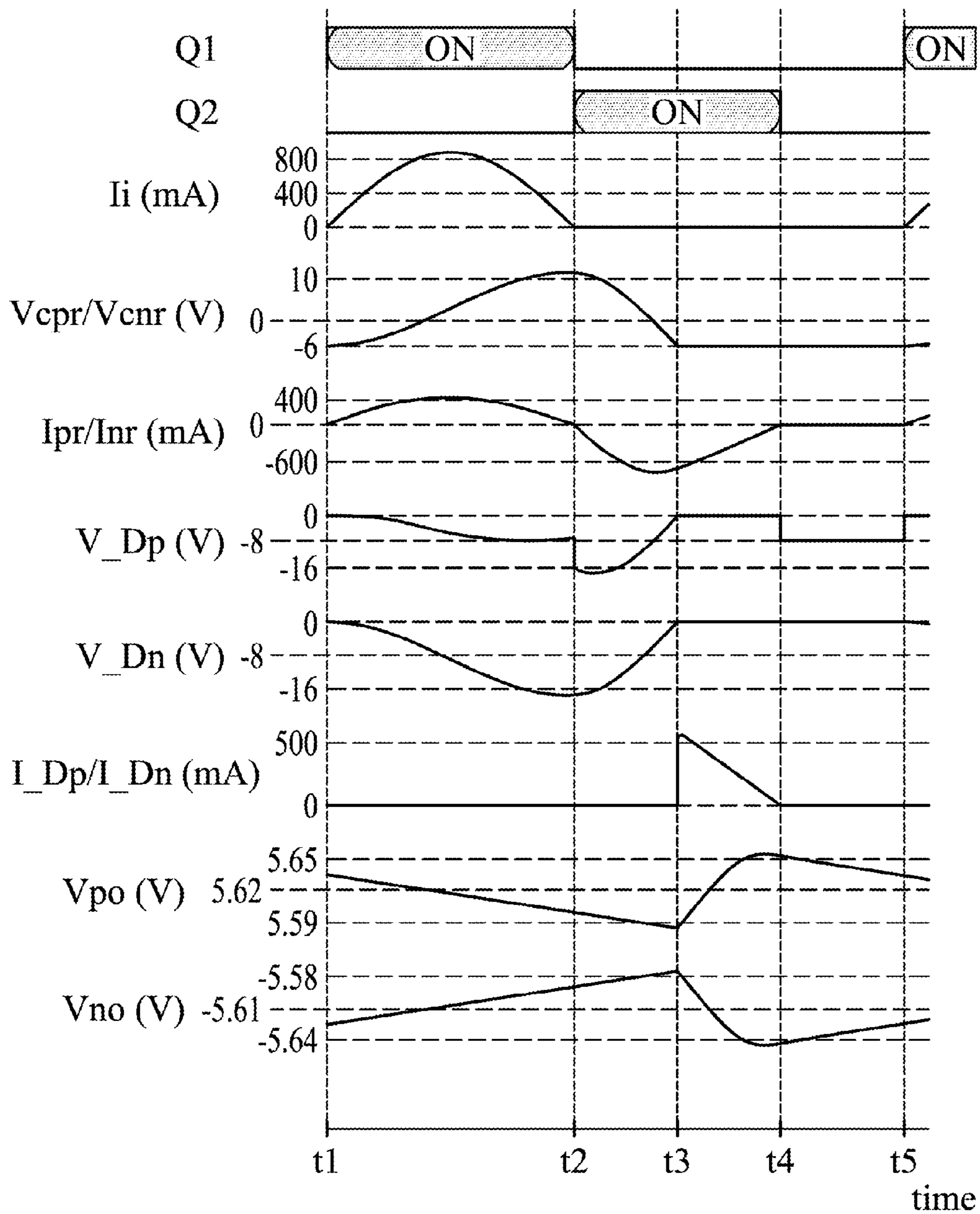


FIG. 3

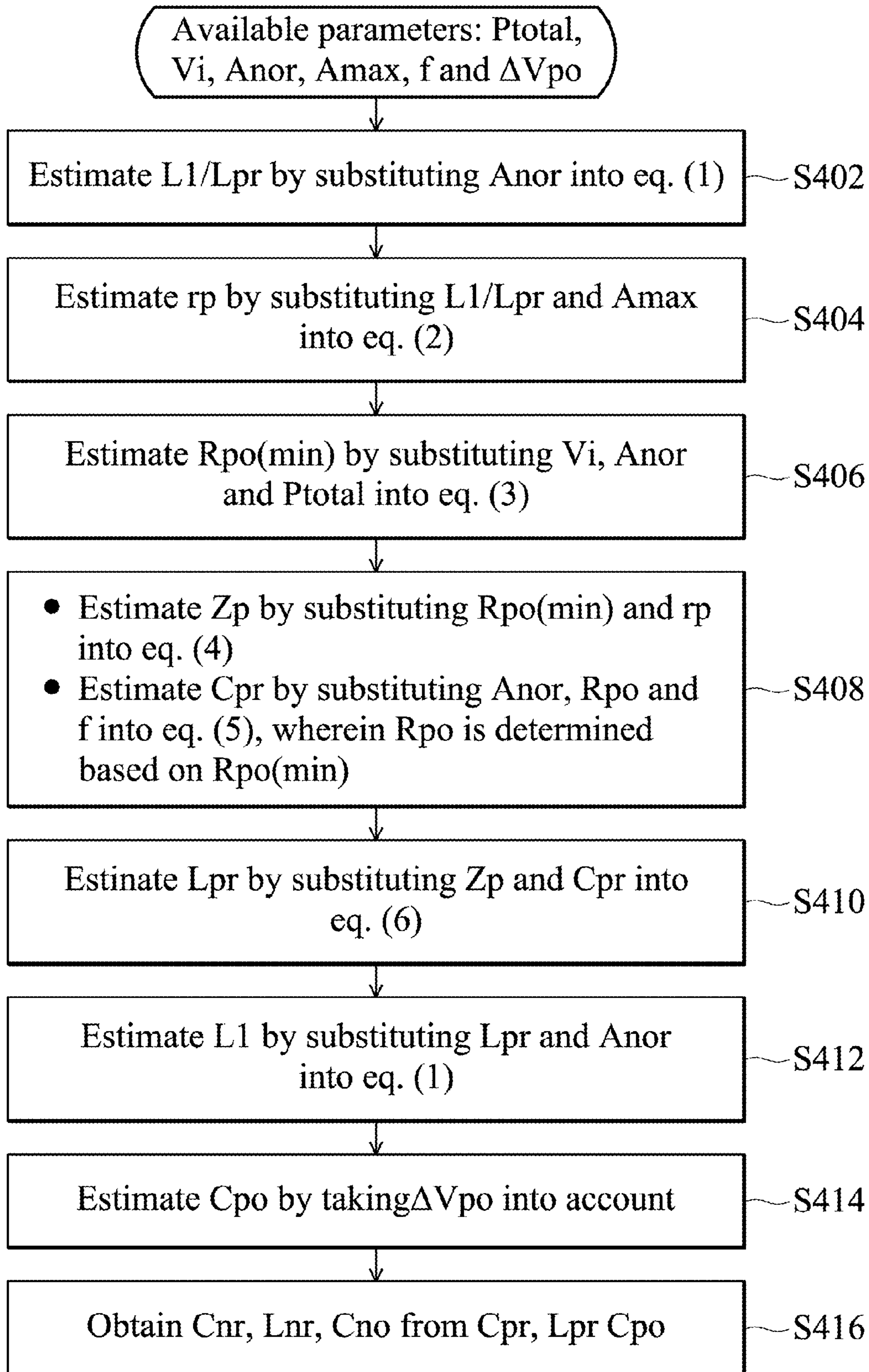


FIG. 4

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DC-DC CONVERTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a DC-DC converter, and in particular relates to a ZCS-PFM (zero current switching and pulse frequency modulation) DC-DC converter in DCM (discontinuous condition mode).

2. Description of the Related Art

A DC-DC converter is an electronic circuit which converts a direct current (DC) source from one voltage level to another. Switched-mode conversion is commonly used to realize a DC-DC converter, which converts one DC voltage level to another by storing the input energy temporarily and then releasing that energy so that it is outputted. The storage component may be a magnetic field storage component (inductors, transformers) or an electric field storage component (capacitors). Switches are provided so that energy may be transmitted into the storage component or be outputted therefrom.

Drawbacks of a switched-mode DC-DC converter include power dissipation caused by the switching operations and EMI (electromagnetic interference).

BRIEF SUMMARY OF THE INVENTION

The invention disclosed DC-DC converters using zero current switching (ZCS) and pulse frequency modulation (PFM) techniques, while being operated in a discontinuous condition mode (DCM).

A DC-DC converter in accordance with an exemplary embodiment of the invention comprises a first switch, a second switch, an input diode, a magnetizing inductor, a first resonant capacitor, a first resonant inductor, a first output diode and a first output filter capacitor. The first and second switches are turned on alternatively. When the first switch is turned on, an input voltage is coupled to an anode of the input diode. A cathode of the input diode is coupled to a first terminal of the magnetizing inductor. The second switch is designed to short a second terminal of the magnetizing inductor to a ground when is turned on. The first resonant capacitor and the first resonant inductor, which are coupled in series, are disposed between the second terminal of the magnetizing inductor and the ground. A first connection node, between the first resonant capacitor and inductor, is coupled to a first terminal of the first output filter capacitor, via the first output diode, to regulate a voltage of the first output filter capacitor. A second terminal of the first output filter capacitor is coupled to the ground. Furthermore, the first terminal of the first output filter capacitor is coupled to a first load to provide the first load with a first output voltage.

In some embodiments, a first terminal of the first resonant capacitor is coupled to the second terminal of the magnetizing inductor while a second terminal of the first resonant capacitor is coupled to the first connection node, and a first terminal of the first resonant inductor is coupled to the first connection node, while a second terminal of the first resonant inductor is coupled to the ground. In such embodiments, an anode and a cathode of the first output diode are coupled to the first connection node and the first terminal of the first output filter capacitor, respectively. The gain between the first output voltage and the input voltage may be positive.

In addition to the aforementioned circuit for a positive gain DC-DC converter, the circuit may further comprise a second resonant inductor, a second resonant capacitor, a second output diode and a second output filter capacitor. The second

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resonant inductor and capacitor are coupled in series between the second terminal of the magnetizing inductor and the ground, wherein a second connection node, between the second resonant inductor and capacitor, is coupled to a first terminal of the second output filter capacitor, via the second output diode, to regulate a voltage of the second output filter capacitor. The first resonant inductor has a first terminal coupled to the second terminal of the magnetizing inductor and a second terminal coupled to the second connection node.

The second resonant capacitor has a first terminal coupled to the second connection node and a second terminal coupled to the ground. An anode of the second output diode is coupled to the first terminal of the second output filter capacitor, while a cathode of the second output diode is coupled to the second connection node. The first terminal of the second output filter capacitor is further coupled to a second load to provide the second node with a second output voltage. The gain between the second output voltage and the input voltage is negative.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. 1 depicts a DC-DC converter in accordance with an exemplary embodiment of the invention;

FIG. 2 illustrates a flowchart depicting an exemplary embodiment of the control schemes;

FIG. 3 depicts waveforms of the signals of FIG. 1; and

FIG. 4 illustrates a flowchart depicting the design guidance.

DETAILED DESCRIPTION OF THE INVENTION

The following description shows several embodiments carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

FIG. 1 depicts a DC-DC converter in accordance with an exemplary embodiment of the invention, which converts an input voltage V_i to a first output voltage V_{po} by a positive gain, or converts the input voltage V_i to a second output voltage V_{no} by a negative gain.

As shown, the DC-DC converter comprises a first switch Q_1 , a second switch Q_2 , an input diode D_i , a magnetizing inductor L_m , a first resonant capacitor C_{pr} , a first resonant inductor L_{pr} , a first output diode D_p , a first output filter capacitor C_{po} , a second resonant inductor L_{nr} , a second resonant capacitor C_{nr} , a second output diode D_n , and a second output filter capacitor C_{no} . The size of the first and second output filter capacitors C_{po} and C_{no} may be greater than the size of the first and second resonant capacitors C_{pr} and C_{nr} by a specific scale factor. The first switch Q_1 and the second switch Q_2 are turned on alternatively to transform the input energy.

The first switch Q_1 is designed to couple the input voltage V_i to an anode of the input diode D_i . A cathode of the input diode D_i is coupled to a first terminal of the magnetizing inductor L_m . The second switch Q_2 is disposed between a second terminal of the magnetizing inductor L_m and a ground. In parallel to the second switch Q_2 , the first resonant capacitor C_{pr} and the first resonant inductor L_{pr} are coupled

in series between the second terminal of the magnetizing inductor L_m and the ground, and the second resonant inductor L_{nr} and the second resonant capacitor C_{nr} are coupled in series between the second terminal of the magnetizing inductor L_m and the ground as well. The circuit, including the first resonant capacitor C_{pr} , the first resonant inductor L_{pr} , the first output diode D_p and the first output filter capacitor C_{po} , is designed to generate the positive gain output voltage V_{po} for a first load R_{po} . The circuit, including the second resonant inductor L_{nr} , the second resonant capacitor C_{nr} , the second output diode D_n and the second output filter capacitor C_{no} , is designed to generate the negative gain output voltage V_{no} for a second load R_{no} .

This paragraph discusses the connections of the components for the positive gain conversion. The first resonant capacitor C_{pr} has a first terminal coupled to the second terminal of the magnetizing inductor L_m and a second terminal coupled to a first connection node n_1 , which is eventually coupled to the first resonant inductor L_{pr} . The first resonant inductor L_{pr} has a first terminal coupled to the first connection node n_1 and a second terminal coupled to the ground. The first output diode D_p has an anode coupled to the first connection node n_1 and a cathode coupled to a first terminal of the first output filter capacitor C_{po} . A second terminal of the first output filter capacitor C_{po} is coupled to the ground. The first load R_{po} is coupled at the first terminal of the first output filter capacitor C_{po} . The first output voltage V_{po} is generated by the disclosed components to supply the first load R_{po} .

This paragraph discusses the connections of the components for the negative gain conversion. The second resonant inductor L_{nr} has a first terminal coupled to the second terminal of the magnetizing inductor L_m and a second terminal coupled to a second connection node n_2 , which is eventually coupled to the second resonant capacitor C_{nr} . The second resonant capacitor C_{nr} has a first terminal coupled to the second connection node n_2 and a second terminal coupled to the ground. The second output diode D_n has a cathode coupled to the second connection node n_2 and an anode coupled to a first terminal of the second output filter capacitor C_{no} . A second terminal of the second output filter capacitor C_{no} is coupled to the ground. The second load R_{no} is coupled at the first terminal of the second output filter capacitor C_{no} . The second output voltage V_{no} is generated by the disclosed components to supply the second load R_{no} .

The following paragraphs discuss exemplary control schemes for the first switch Q_1 and the second switch Q_2 . FIG. 2 illustrates a flowchart depicting an exemplary embodiment of the control schemes.

Referring to the flowchart of FIG. 2, it is shown that the output voltage V_p or V_n is regulated. In step S202, the first switch Q_1 may be switched on after a first resonant voltage difference (V_{cpr} , between the first and second terminals of the first resonant capacitor C_{pr}) is clamped to (reaches and is maintained at) an inverse value of the first output voltage ($-V_{po}$), a second resonant voltage difference (V_{cnr} , between the first and second terminals of the second resonant capacitor C_{nr}) is clamped to the second output voltage (V_{no}), a first resonant current (I_{pr} , flowing through the first resonant inductor L_{pr} from the first terminal to the second terminal thereof) and a second resonant current (I_{nr} , flowing through the second resonant inductor L_{nr} from the first terminal to the second terminal thereof) are pulled up to zero and the first and second output diodes D_p and D_n are switched off. In some embodiments, the first switch Q_1 is switched on in accordance with any dead-time control technique which is familiar to those skilled in the art. In step S204, the first switch Q_1 is switched off and the second switch Q_2 is switched on when an input

current I_i drops to zero. In step S206, the second switch Q_2 is switched off when the first and second output diodes D_p and D_n are switched off again. The three steps S202, S204 and S206 are repeated again and again and the output voltage V_p and V_n are regulated, accordingly.

The flowchart of FIG. 2 is not intended to limit the control scheme of the first and second switches Q_1 and Q_2 . The timing of switching the states of the first and second switches Q_1 and Q_2 may be revised to operate in coordination with the other components of the DC-DC converter.

According to the control scheme of FIG. 2, the DC-DC converter of FIG. 1 is switched between four operation modes repeatedly. FIG. 3 depicts waveforms of the signals of FIG. 1.

During a first time interval t_1 ~ t_2 , the DC-DC converter is operated in a first operation mode. The first switch Q_1 is switched on and the second switch Q_2 is maintained off. At the beginning of the first operation mode (time t_1), the initial values of the first and second resonant currents I_{pr} and I_{nr} are zero, the initial value of the first resonant voltage difference V_{cpr} is $-V_{po}$, the initial value of the second resonant voltage difference V_{cnr} is V_{no} , and the first and second output diodes D_p and D_n are off. With the conduction provided by the first switch Q_1 , the input current I_i is generated and the first and second resonant capacitors C_{pr} and C_{nr} are charged through resonant networks corresponding thereto. When the first and second resonant voltage differences V_{cpr} and V_{cnr} reach zero, the first and second resonant currents I_{pr} and I_{nr} are at their maximum values. The first and second resonant voltage differences V_{cpr} and V_{cnr} keep rising until the first and second resonant currents I_{pr} and I_{nr} and the input current I_i are decreased to zero. As shown, the first and second output diodes D_p and D_n are reversely biased during the first time interval t_1 ~ t_2 , so that the first and second output diodes D_p and D_n are maintained at off during the first operation mode. The loop constructed by the first output filter capacitor C_{po} and the first load R_{po} may cause a slight drop in the first output voltage V_{po} . The loop constructed by the second output filter capacitor C_{no} and the second load R_{no} may cause a slight rise in the second output voltage V_{no} .

At time t_2 (when the input current I_i drops to zero), the first switch Q_1 is switched off and the second is switched on and then the second time interval t_2 ~ t_3 for a second operation mode starts. At this stage, the input current I_i is clamped at zero and the first and second resonant currents I_{pr} and I_{nr} drop to negative values. With the short circuit provided by the turned-on second switch Q_2 , the first and second resonant capacitors C_{pr} and C_{nr} are discharged by the resonant networks corresponding thereto. When the first and second resonant voltage differences V_{cpr} and V_{cnr} drop to zero, the first and second resonant currents I_{pr} and I_{nr} are at their minimum values. At time t_3 , the first and second resonant voltage differences V_{cpr} and V_{cnr} fall to $-V_{po}$ and V_{no} , respectively, and the first and second output diodes D_p and D_n are switched on accordingly to produce currents I_{Dp} and I_{Dn} during the next time interval t_3 ~ t_4 .

During a third time interval t_3 ~ t_4 , a third operation mode is provided. In this stage, the first and second output diodes D_p and D_n are forward biased, so that the first and second resonant voltage differences V_{cpr} and V_{cnr} are clamped at $-V_{po}$ and V_{no} , respectively. Because the size of the first and second output filter capacitors C_{po} and C_{no} are designed to be much greater than that of the first and second resonant capacitors C_{pr} and C_{nr} , the currents I_{Dp} and I_{Dn} through the first and second output diodes D_p and D_n approach the absolute values of the first and the second resonant currents I_{pr} and I_{nr} , respectively. During the third time interval t_3 ~ t_4 , the first output voltage V_{po} is slightly raised back to a higher level and

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the second output voltage V_{no} is slightly pulled down to a lower level. At time t_4 , the first and second resonant currents I_{pr} and I_{nr} are clamped to zero, and the first and second output diodes D_p and D_n are switched off.

At time t_4 , the second switch Q_2 is switched off and the DC-DC converter is switched to a fourth operation mode, accordingly. Note that both of the first and second switches Q_1 and Q_2 are turned off and the first and second output diodes D_p and D_n are also turned off. Again, the first output voltage V_{po} is slightly, pulled down to a lower level because of the loop constructed from the first output filter capacitor C_{po} and the first load R_{po} , and the second output voltage V_{no} is slightly raised back to a higher level because of the loop constructed from the second output filter capacitor C_{no} and the second load R_{no} . Because the first resonant voltage difference V_{cpr} is clamped to an inverse value of the first output voltage ($-V_{po}$), the second resonant voltage difference V_{cnr} is clamped to the second output voltage V_{no} , the first and second resonant currents I_{pr} and I_{nr} are pulled up to zero and the first and second output diodes D_p and D_n are switched off again, the first switch Q_1 may be switched on again at time t_5 , to start another output voltage regulation cycle. The timing to switch on the first switch Q_1 may be based on the loading from the first and second loads R_{po} and R_{no} . Accordingly, herein, the dead-time control technique is a preferred technique choice.

FIG. 3 shows that the first output voltage V_{po} is regulated around a positive value (i.e. about +5.6V), and the second output voltage V_{no} is regulated around a negative value (i.e. about -5.6V). The DC-DC converter introduced in FIG. 1 successfully converts the input voltage V_i into a positive gain output voltage V_{po} and a negative gain output voltage V_{no} .

The control scheme of the first and second switches Q_1 and Q_2 are based on zero current switching (ZCS) techniques and zero voltage switching (ZVS) techniques. At time t_1 , the first switch Q_1 is switched on, while the input current I_i is zero, through zero current switching. At time t_2 , the first switch Q_1 is turned off, when the input current I_i is returned to zero, through zero current switching. At time t_3 , the first and second output diodes D_p and D_n are switched on during a ZVS event, wherein the voltage differences V_{Dp} and V_{Dn} across the first and second output diodes D_p and D_n approximate zero. At time t_4 , the first and second output diodes D_p and D_n are switched off during an ZCS event, wherein the currents I_{Dp} and I_{Dn} through the first and second output diodes D_p and D_n are zero.

In some embodiments, the first and second switches Q_1 and Q_2 are realized by bipolar junction transistors (BJTs) having minimal power consumption. Because tailing-current loss can be eliminated, BJT characteristics are suitable for the zero current switching techniques herein. In order to decrease current stress, unnecessary energy flow should be avoided. Accordingly, unidirectional switches may be employed herein.

In another exemplary embodiment, a DC-DC converter only providing the disclosed positive gain conversion is introduced. This kind of DC-DC converter does not contain the components for the negative gain conversion (for example, does not include the second resonant inductor and capacitor L_{nr} and C_{nr} , the second output diode D_n and the second output filter capacitor C_{no}). In such cases, the first switch Q_1 is switched on after the first resonant voltage difference V_{cpr} is clamped to the inverse value of the first output voltage ($-V_{po}$), the first resonant current I_{pr} is pulled up to zero and the first output diode D_p is switched off. Furthermore, the first switch Q_1 may be switched off and the second switch Q_2 may be switched on when the input current I_i drops to zero. The

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second switch Q_2 may be switched off when the first output diode D_p is switched off again.

In another exemplary embodiment, a DC-DC converter only providing the disclosed negative gain conversion is introduced. This kind of DC-DC converter does not contain the components for the positive gain conversion (for example, does not include the first resonant capacitor and inductor C_{pr} and L_{pr} , the first output diode D_p and the first output filter capacitor C_{po}). In such cases, the first switch Q_1 is switched on after the second resonant voltage difference V_{cnr} is clamped to the second output voltage V_{no} , the second resonant current I_{nr} is pulled up to zero and the second output diode D_n is switched off. Furthermore, the first switch Q_1 may be switched off and the second switch Q_2 may be switched on when the input current I_i drops to zero. The second switch Q_2 may be switched off when the second output diode D_n is switched off again.

The following paragraphs show a design guidance of the DC-DC converter.

FIG. 4 illustrates a flowchart depicting the design guidance for symmetrical positive gain and negative gain voltage conversion. The upper limit of the total power consumption P_{total} , the input voltage V_i , the normal positive voltage gain A_{nor} , the upper limit of the positive voltage gain A_{max} , the output voltage regulation frequency f and the upper limit ΔV_{po} of the ripple in the positive gain output voltage V_{po} are determined by the user as available parameters of the DC-DC converter design. Five equations (1)~(5) are introduced herein.

$$\frac{L_1}{L_{pr}} > \frac{1}{2A_{nor}} \quad \text{Equation (1)}$$

$$r_p = \frac{A_{max}^2}{1 + A_{max}} \cdot \left[\frac{\pi}{2} \cdot \left(1 + \sqrt{1 + \frac{2L_1}{L_{pr}}} \right) + \frac{\sqrt{1 + A_{max}}}{A_{max}} - \frac{1}{2} \cdot \cos^{-1} \left(\frac{A_{max}}{2 + A_{max}} \right) \right] \quad \text{Equation (2)}$$

$$R_{po(\min)} = \frac{(A_{nor} \cdot V_i)^2}{P_{total}/2} \quad \text{Equation (3)}$$

$$Z_p = \frac{R_{po(\min)}}{r_p} \quad \text{Equation (4)}$$

$$\frac{A_{nor}^2}{1 + A_{nor}} = 2 \cdot R_{po} \cdot C_{pr} \cdot f \quad \text{Equation (5)}$$

$$Z_p = \sqrt{\frac{L_{pr}}{C_{pr}}} \quad \text{Equation (6)}$$

The design guidance is discussed in the following for a case wherein P_{total} is 0.5 W, V_i is 2.8V, A_{nor} is 2, A_{max} is 3, f is 5 MHz and ΔV_{po} is $\pm 1\% \cdot V_{po}$. In step S402, a value L_1/L_{pr} is estimated by substituting A_{nor} into equation (1), wherein by further taking the reliable margin into account, L_1/L_{pr} may be set to be 0.5. In step S404, a value r_p is estimated by substituting L_1/L_{pr} and A_{max} into equation (2). r_p is set to 8.989. In step S406, the minimum value of the first load $R_{po(\min)}$ is estimated by substituting V_i , A_{nor} and P_{total} into equation (3). $R_{po(\min)}$ is set to 125 ohm. In step S408, a value Z_p is estimated by substituting $R_{po(\min)}$ and r_p into equation (4), and the first resonant capacitor C_{pr} is estimated by substituting A_{nor} , R_{po} (determined based on $R_{po(\min)}$) and f into equation (5). Z_p is set to be 14 ohm. The first resonant capacitor C_{pr} is set to be 2.2 nF. In step S410, the first resonant inductor L_{pr} is estimated by substituting Z_p and C_{pr} into

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equation (6). The first resonant inductor L_{pr} is set to be 0.47 uH. In step S412, the magnetizing inductor $L1$ is estimated by substituting L_{pr} and A_{nor} into equation (1). The magnetizing inductor $L1$ is set to 0.22 uH. In step S414, the first output filter capacitor C_{po} is estimated by taking the ripple limit ΔV_{po} into account. Based on the following equation:

$$\frac{1}{C_{po}} \int_{t_3}^{t_4} I_{pr}(t) dt \leq \frac{2}{100} V_{po},$$

the first output filter capacitor C_{po} is set to 0/18 uF. In step S416, the second resonant capacitor C_{nr} , the second resonant inductor L_{nr} , and the second output filter capacitor C_{no} are obtained, based on the estimated values of the first resonant capacitor C_{pr} , the first resonant inductor L_{pr} and the first output filter capacitor C_{po} .

The flowchart of FIG. 4 and the estimated values $L1$, C_{pr} , L_{pr} , C_{po} , C_{nr} , L_{nr} and C_{no} are not intended to limit the scope of the invention. The DC-DC converter of FIG. 1 may be realized by other design principles familiar to a person skilled in the art.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A DC-DC converter, comprising
 - an input diode, a first output diode and a first output filter capacitor;
 - a first switch, operative to couple an input voltage to an anode of the input diode;
 - a magnetizing inductor, having a first terminal and a second terminal, wherein the first terminal of the magnetizing inductor is coupled to a cathode of the input diode;
 - a second switch, operative to couple the second terminal of the magnetizing inductor to a ground; and
 - a first resonant capacitor and a first resonant inductor, coupled in series between the second terminal of the magnetizing inductor and the ground, wherein a first connection node, between the first resonant capacitor and the first resonant inductor, is coupled to a first terminal of the first output filter capacitor, via the first output diode, to regulate a voltage of the first output filter capacitor;
 wherein:
 - a second terminal of the first output filter capacitor is coupled to the ground;
 - the first terminal of the first output filter capacitor is further coupled to a first load to provide the first load with a first output voltage; and
 - the first switch and the second switch are turned on alternately.
2. The DC-DC converter as claimed in claim 1, wherein the first output filter capacitor is greater than the first resonant capacitor by a specific scale factor.
3. The DC-DC converter as claimed in claim 1, wherein:
 - the first resonant capacitor has a first terminal coupled to the second terminal of the magnetizing inductor and a second terminal coupled to the first connection node;

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the first resonant inductor has a first terminal coupled to the first connection node and a second terminal coupled to the ground; and

the first output diode has an anode coupled to the first connection node and a cathode coupled to the first terminal of the first output filter capacitor.

4. The DC-DC converter as claimed in claim 3, wherein: the first switch is switched on after a first resonant voltage difference reaches and is maintained at an inverse value of the first output voltage, a first resonant current is pulled up to zero and the first output diode is switched off;

the first resonant voltage difference is measured between the first and second terminals of the first resonant capacitor; and

the first resonant current flows from the first terminal to the second terminal of the first resonant inductor.

5. The DC-DC converter as claimed in claim 4, wherein the first switch is switched on in accordance with a dead-time control technique.

6. The DC-DC converter as claimed in claim 4, wherein the first switch is switched off and the second switch is switched on when an input current drops to zero.

7. The DC-DC converter as claimed in claim 6, wherein the second switch is switched off when the first output diode is switched off again.

8. The DC-DC converter as claimed in claim 1, wherein: the first resonant inductor has a first terminal coupled to the second terminal of the magnetizing inductor and a second terminal coupled to the first connection node;

the first resonant capacitor has a first terminal coupled to the first connection node and a second terminal coupled to the ground; and

the first output diode has a cathode coupled to the first connection node and an anode coupled to the first terminal of the first output filter capacitor.

9. The DC-DC converter as claimed in claim 8, wherein: the first switch is switched on after a first resonant voltage difference reaches and is maintained at a value of the first output voltage, a first resonant current is pulled up to zero and the first output diode is switched off;

the first resonant voltage difference is measured between the first and second terminals of the first resonant capacitor; and

the first resonant current flows from the first terminal to the second terminal of the first resonant inductor.

10. The DC-DC converter as claimed in claim 9, wherein the first switch is switched on in accordance with a dead-time control technique.

11. The DC-DC converter as claimed in claim 9, wherein the first switch is switched off and the second switch is switched on when an input current drops to zero.

12. The DC-DC converter as claimed in claim 11, wherein the second switch is switched off when the first output diode is switched off again.

13. The DC-DC converter as claimed in claim 3, further comprising:

a second output diode and a second output filter capacitor; and

a second resonant inductor and a second resonant capacitor, coupled in series between the second terminal of the magnetizing inductor and the ground, wherein:

a second connection node, between the second resonant inductor and the second resonant capacitor, is coupled to a first terminal of the second output filter capacitor, via the second output diode, to regulate a voltage of the second output filter capacitor;

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the second resonant inductor has a first terminal coupled to the second terminal of the magnetizing inductor and a second terminal coupled to the second connection node; and

the second resonant capacitor has a first terminal 5 coupled to the second connection node and a second terminal coupled to the ground;

wherein:

the second output diode has a cathode coupled to the second connection node and an anode coupled to the 10 first terminal of the second output filter capacitor;

the first terminal of the second output filter capacitor is further coupled to a second load to provide the second load with a second output voltage; and

a second terminal of the second output filter capacitor is 15 coupled to the ground.

14. The DC-DC converter as claimed in claim **13**, wherein the size of the first and second output filter capacitors are greater than the size of the first and second resonant capaci- 20 tors by a specific scale factor.

15. The DC-DC converter as claimed in claim **13**, wherein: the first switch is switched on after a first resonant voltage difference reaches and is maintained at an inverse value of the first output voltage, a second resonant voltage 25 difference reaches and is maintained at the second out- put voltage, a first resonant current and a second reso-

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nant current are pulled up to zero and the first and second output diodes are switched off;

the first resonant voltage difference is measured between the first and second terminals of the first resonant capaci- tor;

the second resonant voltage difference is measured between the first and second terminals of the second resonant capacitor;

the first resonant current flows from the first terminal to the second terminal of the first resonant inductor; and

the second resonant current flows from the first terminal to the second terminal of the second resonant inductor.

16. The DC-DC converter as claimed in claim **15**, wherein the first switch is switched on in accordance with a dead-time control technique.

17. The DC-DC converter as claimed in claim **15**, wherein the first switch is switched off and the second switch is switched on when an input current drops to zero.

18. The DC-DC converter as claimed in claim **17**, wherein the second switch is switched off when the first and second output diodes are switched off again.

19. The DC-DC converter as claimed in claim **1**, wherein: the first and second switches are bipolar junction transis- tors.

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