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**Ramchandran**

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(54) **ADAPTABLE DATAPATH FOR A DIGITAL PROCESSING SYSTEM**

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***G06F 3/00*** (2006.01)

(52) **U.S. Cl.** ..... **710/4**; 710/2; 712/33; 712/201

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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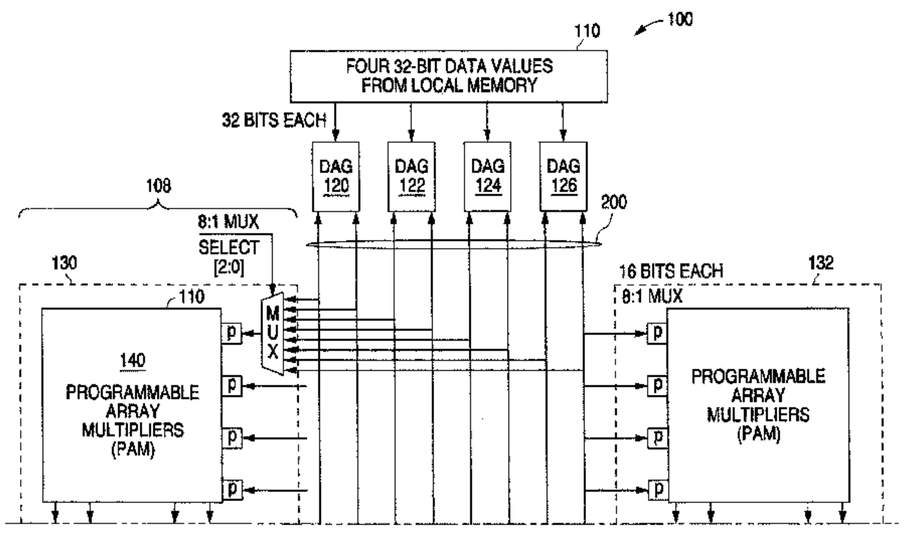
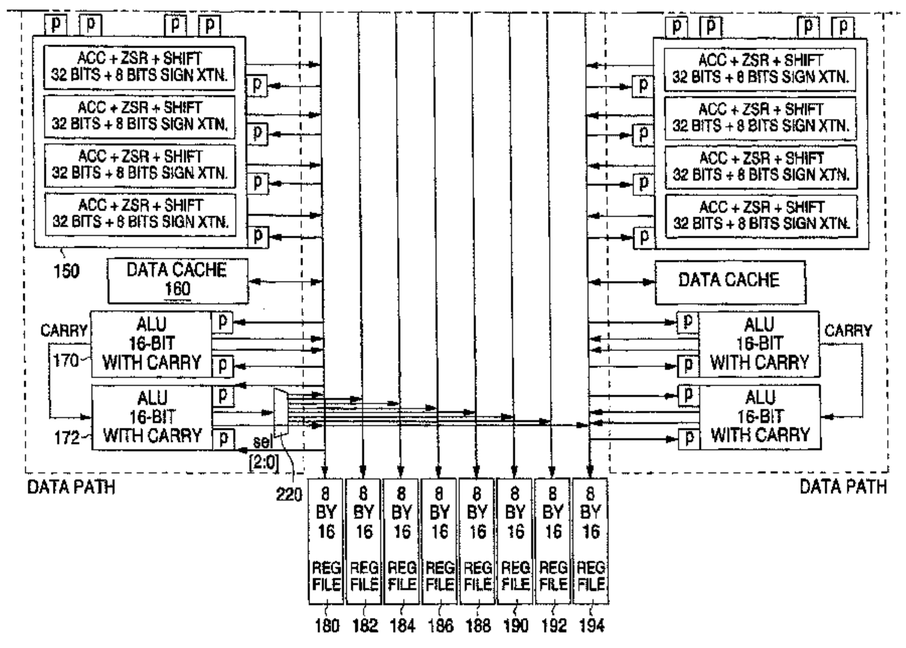
(57) **ABSTRACT**

The present invention includes an adaptable high-performance node (RXN) with several features that enable it to provide high performance along with adaptability. A preferred embodiment of the RXN includes a run-time configurable data path and control path. The RXN supports multi-precision arithmetic including 8, 16, 24, and 32 bit codes. Data flow can be reconfigured to minimize register accesses for different operations. For example, multiply-accumulate operations can be performed with minimal, or no, register stores by reconfiguration of the data path. Predetermined kernels can be configured during a setup phase so that the RXN can efficiently execute, e.g., Discrete Cosine Transform (DCT), Fast-Fourier Transform (FFT) and other operations. Other features are provided.

**33 Claims, 3 Drawing Sheets**



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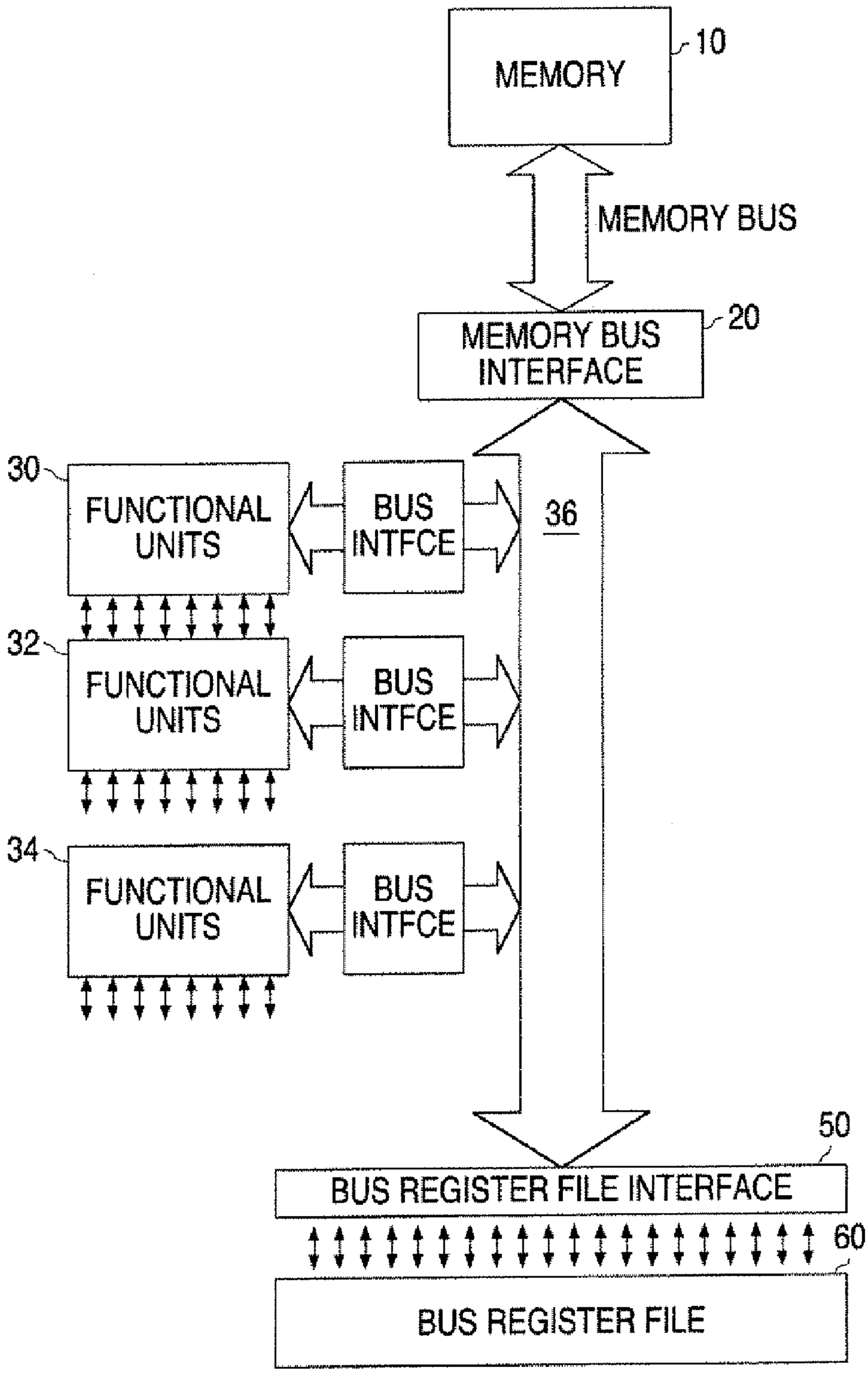



**FIG. 1**
PRIOR ART

FIG. 2A

FIG. 2A-1 | FIG. 2A-2

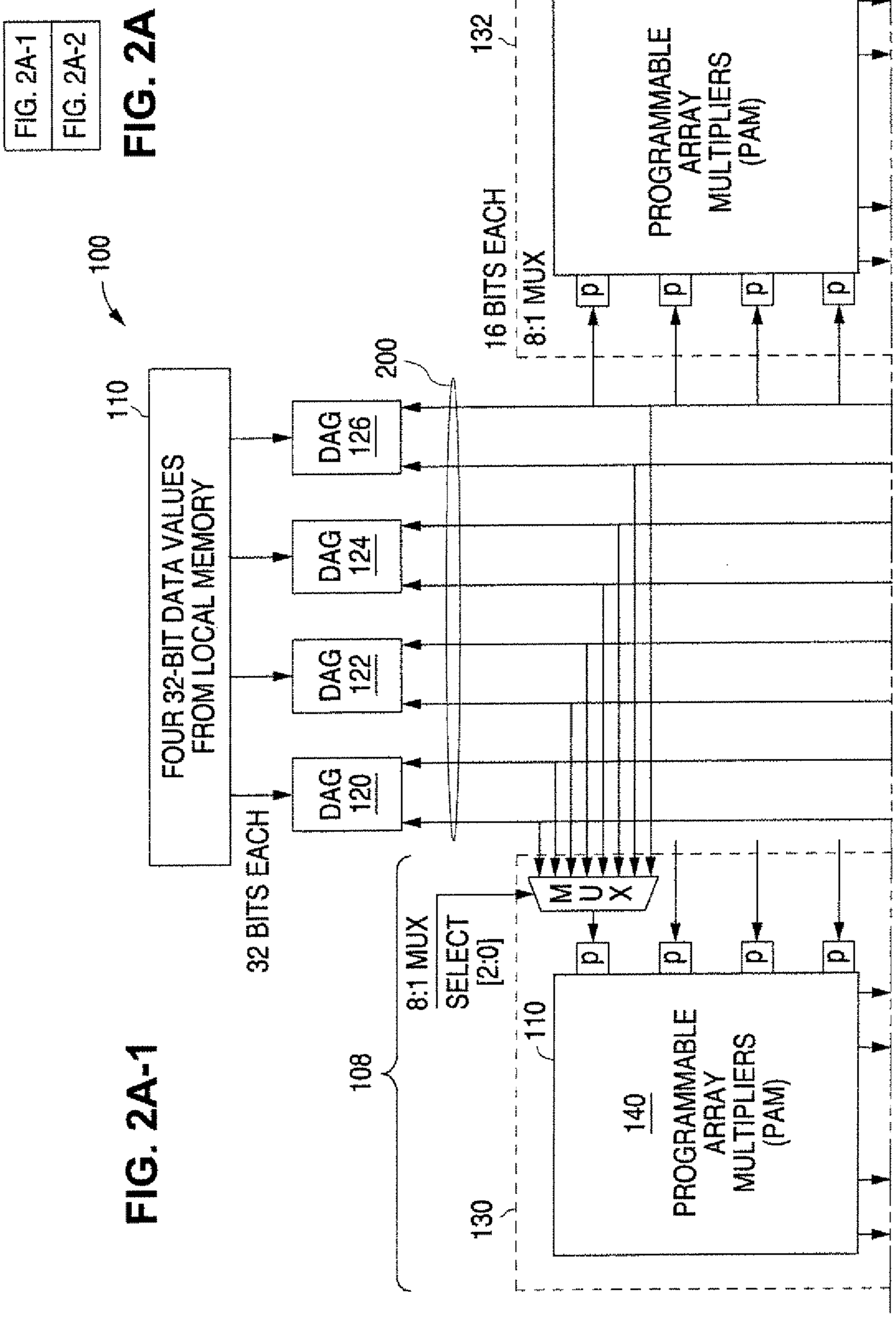



FIG. 2A-1

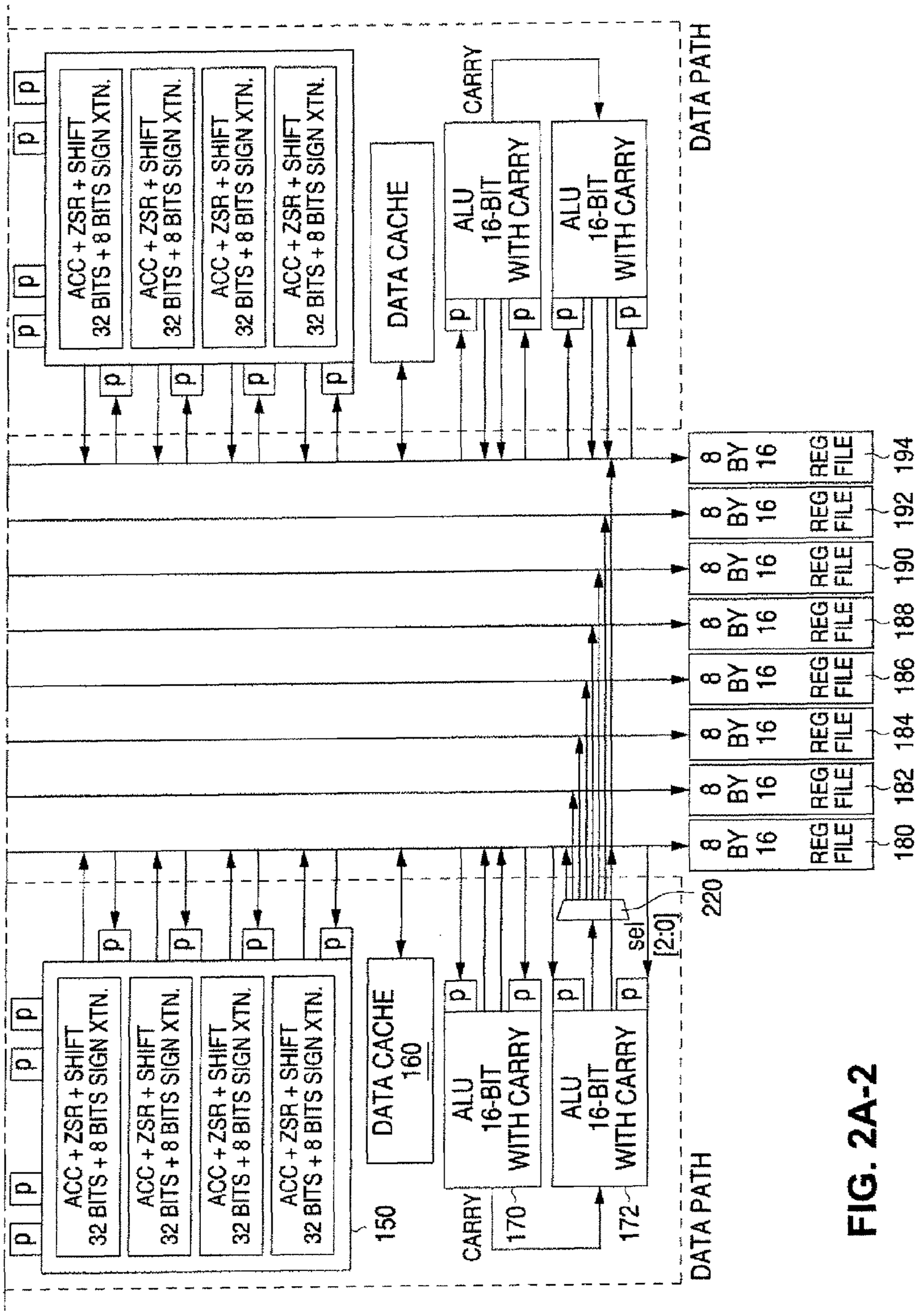

DATA PATH
ACC + ZSR + SHIFT 32 BITS + 8 BITS SIGN XTN.
DATA CACHE
ALU 16-BIT WITH CARRY
CARRY
p
8 BY 16 REG FILE
180
182
184
186
188
190
192
194
220
sel [2:0]
150
160
170
172

FIG. 2A-2

# ADAPTABLE DATAPATH FOR A DIGITAL PROCESSING SYSTEM

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 12/556,894, filed Sep. 10, 2009, which is a continuation of U.S. application Ser. No. 11/800,577, filed May 3, 2007, which is a continuation of U.S. application Ser. No. 10/626,833, filed Jul. 23, 2003, which claims the benefit of U.S. Provisional Application No. 60/422,063, filed Oct. 28, 2002, each of the aforementioned applications are incorporated by reference herein.

This application is related to the following co-pending U.S. Patent Applications that Are each incorporated by reference as if set fourth in full in this application: "Input Pipeline Registers For A Node In An Adaptive Computing Engine, " Ser. No. 10/626,479, filed Jul. 23, 2003; "Cache For Instruction Set Architecture Using Indexes to Achieve Compression", Ser. No. 11/628,083, filed Jul. 24, 2003; "Method For Ordering Operations For Scheduling By A Modulo Scheduler For Processors With A Large Number Of Function Units And Reconfigurable Data Paths", Ser. No. 10/146,857, filed on May 15, 2002; "Uniform interface For A Functional Node In An Adaptive Computing Engine", Ser. No. 10/443,554, filed on May 21, 2003; "Hardware Task Manager For Adaptive Computing ", Ser. No. 10/443,501, filed on May 21, 2003; and "Adaptive Integrated circuitry With heterogeneous And Reconfigurable Matrices Of Diverse And Adaptive Computational Units Having fixed, Application Specific Computational Element", Ser. No. 09/815,122, filed on Mar. 22, 2001.

## BACKGROUND OF THE INVENTION

This invention is related in general to digital processing architectures and more specifically to the use of an adaptable data path using register files to efficiently implement digital signal processing operations.

Digital Signal Processing (DSP) calculations require many iterations of fast multiply-accumulate and other operations. Typically, the actual operations are accomplished by "functional units" such as multipliers, adders, accumulators, shifters, etc. The functional units obtain values, or operands, from a fast main memory such as Random Access Memory (RAM). The DSP system can be included within a chip that resides in a device such as a consumer electronic device, computer, etc.

The design of a DSP chip can be targeted for specific DSP applications. For example, in a cellular telephone, a DSP chip may be optimized for Time-Division Multiple Access (TDMA) processing. A Voice-Over-Internet Protocol (VOIP) application may require vocoding operations, and so on. It is desirable for a chip manufacturer to provide a single chip design that can be adapted to different DSP applications. Such a chip is often described as an adaptable, or configurable, design.

One aspect of an adaptable design for a DSP chip includes allowing flexible and configurable routing between the different functional units, memory and other components such as registers, input/output and other resources on the chip. A traditional approach to providing flexible routing uses a data bus. Such an approach is shown in FIG. **1**.

In FIG. **1**, memory bus **10** interfaces with a memory (not shown) to provide values from the memory to processing components such as functional unit blocks **30**, **32** and **34**.



Values from memory bus **10** are selected and routed through memory bus interface **20** to data path bus **36**. The functional unit blocks are able to obtain values from data path bus **36** by using traditional bus arbitration logic (e.g., address lines, bus busy, etc.). Within a block, such as functional unit block **30** of FIG. **1**, there may be many different components, such as a bank of multipliers, to which the data from data path bus **36** can be transferred. In this manner, any arbitrary value from memory can be provided to any functional unit block, and to components within blocks of functional units.

Values can also be provided between functional unit blocks by using the data path bus. Another resource is register file **60** provided on data path bus **36** by register file interface **50**. Register file **60** includes a bank of fast registers, or fast RAM. Register file interface **50** allows values from data path bus **36** to be exchanged with the register file. Typically, any register or memory location within register file **60** can be placed on data path bus **36** within the same amount of time (e.g., a single cycle). One way to do this is to provide an address to a location in the register file, either on the data path bus, itself, or by using a separate set of address lines. This approach is very flexible in that any value in a component of a functional unit block can be transferred to any location within the register file and vice versa.

However, a drawback with the approach of FIG. **1**, is that such a design is rather expensive to create, slow and does not scale well. A bus approach requires considerable overhead in control circuitry and arbitration logic. This takes up real estate on the silicon chip and increases power consumption. The use of a large, randomly addressable register file also is quite costly and requires inclusion of tens of thousands of additional transistors. The use of such complicated logic often requires bus cycle times to be slower to accommodate all of the switching activity. Finally, such an approach does not scale well since, e.g., adding more and more functional unit blocks will require additional addressing capability that may mean more lines and logic. Additional register file space may also be required. The data path bus would also need to be routed to connect to the added components. Each functional unit block also requires the bus control and arbitration circuitry.

Thus, it is desirable to provide an interconnection scheme for digital processor applications that improves over one or more of the above, or other, shortcomings in the prior art.

## SUMMARY OF THE INVENTION

The present invention uses dedicated groups of configurable data path lines to transfer data values from a main memory to functional units. Each group of data path lines includes a register file dedicated for storage for each group of lines. Functional units can obtain values from, and store values to, main memory and can transfer values among the registers and among other functional units by using the dedicated groups of data path lines and a data address generator (DAG).

DAG circuitry interfaces each group of datapath lines to a main memory bus. Each DAG is controllable to select a value of varying bit width from the memory bus, or to select a value from another group of data path lines. In a preferred embodiment, eight groups of 16 data path lines are used. Each group includes a register file of eight 16-bit words on each group of 16 data path lines. Registers can hold a value onto their associated group of data path lines so that the value is available at a later time on the lines without the need to do a later data fetch.

In one embodiment the invention provides a data path circuit in a digital processing device, wherein the data path

circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising a first plurality of data lines; a first data address generator for coupling the first plurality of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto the first plurality of data lines; one or more functional units for performing a digital operation coupled to the plurality of data lines; and a register coupled to the first plurality of data lines, wherein the register selectively stores a value from the first plurality of data lines so that the value is selectively available on the first plurality of data lines.

Another aspect of the invention provides both general and direct data paths between array multipliers and accumulators. Banks of accumulators are coupled to the groups of configurable data path lines and are also provided with direct lines to the multipliers. An embodiment of the invention provides a digital processing system comprising a multiplier; an accumulator; a configurable data path coupled to the multiplier and the accumulator; and a direct data path coupled between the multiplier and the accumulator.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a prior art approach using a data path bus;

FIG. **2**A comprising FIG. **2**A-**1** and FIG. **2**A-**2** illustrates the configurable data path arrangement of a preferred embodiment of the present invention;

## DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is incorporated into a node referred to as a Adaptable Node (RXN) in a adaptive computing engine (ACE) manufactured by Quicksilver, Inc., of San Jose, Calif. Details of the ACE engine and RXN node can be found in the priority and related patent applications reference above. Aspects of the invention described herein are adaptable for use with any generalized digital processing system, such as a system adapted for digital signal processing or other types of processing.

FIG. **2**A comprising FIG. **2**A-**1** and FIG. **2**A-**2** illustrates the configurable data path arrangement according to a preferred embodiment of the present invention.

In FIG. **2**A, digital processing system **100** is designed for fast DSP-type processing such as in discrete cosine transformation (DCT), fast fourier transformation (FFT), etc. Digital processing system **100** includes four 32-bit data path address generators (DAG) to interface between four groups of configurable data path lines **200** and a main memory bus **110**. Main memory bus **110** is an arbitrated high-speed bus as is known in the art. Other types of main memory accessing can be used.

Each group of 32 lines includes two subgroups of 16 lines each. Each subgroup is connected to a register file of eight 16-bit words. For example, DAG **120** is connected to register files **180** and **182**. DAG **122** is connected to register files **184** and **186**. Similarly, DAGs **124** and **126** are connected to register files **188**, **190** and **192**, **194**, respectively. Naturally, other embodiments can use any number of DAGs, groups, and subgroups register files. Although specific bit widths, numbers of lines, components, etc., and specific connectivity are described, many variations are possible and are within the scope of the invention. Although the DAGs play a major role in the preferred embodiment, other embodiments can use other types of interfacing to the main memory bus. Although the DAGs provide a high degree of configurable routing options (as discussed below), other embodiments can vary in the degree of configurability, and in the specific configuration options and control methods. In some cases, simple registers, register files, multiplexers or other components might be used in place of the DAGs of the present invention.

The use of register files on each of the discrete subgroup lines simplifies the interconnection architecture from that of the more generalized bus and multiport register file shown in FIG. **1** of the prior art. This approach can also provide benefits in reduced transistor count, power consumption, improved scalability, efficient data access and other advantages. Although configuring the data path of the present invention may be more complex than with generalized approaches, in practice, a compiler is able to automatically handle the configuration transparently to a human programmer. This allows creation of faster-executing code for a variety of DSP applications by using the same hardware architecture without placing any undue burden on the programmer. If desired, a programmer can customize the data path configuration in order to further optimize processing execution.

Groups of data path lines **200** are used to transfer data from memory bus **110** to functional units within blocks **130** and **132**, and also to transfer data among the functional units, themselves. The functional unit blocks are essentially the same so only block **130** is discussed in detail. Functional units include Programmable Array Multipliers (PAMs) **140**, accumulators (and shift registers) **150**, data cache **160** and Arithmetic/Logic Units (ALUs) **170** and **172**. Naturally, the functional units used in any specific embodiment can vary in number and type from that shown in FIG. **2**A.

Functional units are connected to the data path line groups via multiplexers and demultiplexers such as **210** and **220**, respectively. Inputs and Outputs (I/Os) from the functional units can, optionally, use multiplexing to more than one subgroup of data path lines; or an I/O can be connected directly to one subgroup. A preferred embodiment uses pipeline registers between I/O ports and data path lines, as shown by boxes labeled "p" in FIG. **2**A. Pipeline registers allow holding data at I/O ports, onto data lines, or for other purposes. The pipeline registers also allow obtaining a zero, 1, or other desired binary values and provide other advantages. Pipeline registers are described in more detail in the co-pending patent application "Input Pipeline Registers For A Node In An Adaptive Computing Engine" referenced above.

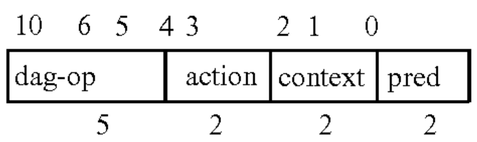
Table I, below, shows DAG operations. The configuration of the data path from cycle to cycle is set by a control word, or words obtained from the main memory bus in accordance with controller modules such as a hardware task manager, scheduler and other processes and components not shown in FIG. **2**A but discussed in related patent applications. Part of the configuration information includes fields for DAG operations. A DAG operation can change from cycle to cycle and includes reading data of various widths from memory or from another DAG. DAG operations other than those shown in Table I can be used. Each DAG has one 5-bit 'dag-op' field and one 4-bit 'address' field. There is a single 'pred' field that defines non-sequencing operations.

TABLE I

| Dag-op | Mnemonic | Description | Cycles |
|---|---|---|---|
| 0x00 | read8 | Read 8-bits from memory | 1 |
| 0x01 | read8x | Read 8-bits from memory and sign extend to 32-bits | 1 |
| 0x02 | read16 | Read 16-bits from memory | 1 |
| 0x03 | read16x | Read 16-bits from memory and sign extend to 32-bits | 1 |
| 0x04 | read24 | Read 24-bits from memory | 1 |
| 0x05 | read24x | Read 24-bits from memory and sign extend to 32-bits | 1 |
| 0x06 | read32 | Read 32-bits from memory | 1 |
| 0x07 | write8 | Write 8-bits to memory | 1 |
| 0x08 | write16 | Write 16-bits to memory | 1 |
| 0x09 | write24 | Write 24-bits to memory | 1 |
| 0x0A | write32 | Write 32-bits to memory | 1 |
| 0x0B | writeMindp | Write 32-bits (only mode supported) to MIN write queue from the data path buses | 1 |
| 0x0C | writeMinM | Write 32-bits (only mode supported) to MIN write queue from a 32-bit memory read. | 1 (pipelined) |
| 0x0D | readdag16 | Read a 16 bit value from one DAG register | 0 |
| 0x0E | readdag32 | Read a 32 bit value from two DAG registers | 0 |
| 0x0F | load32dp | Load two 16-bit DAG registers or 32-bit write buffer using 32-bit data in dp2n:dp2n+1 connecting to DAGn | 1 |
| 0x10 | load16dpn | Load a DAG register from an even data path bus | 1 |
| 0x11 | load16dpn+1 | Load a DAG register from an odd data path bus 1 | |
| 0x12 | modify | Modify address but do not do a memory access. | 1 |
| 0x13 | Dagnoop | Do nothing. All DAG operations execute every clock cycle until this operation is chosen | 1 |
| 0x14 | Dagcont | Continue the previous operation | 1 |
| 0x15 | writePA | Writes 32-bits of data from memory into 'tfrl' or 'tbrl' | 1 |
| 0x16 | writeMinbuf | Write 32-bits to MIN write queue from buffer | 1 |

For dag-op: 0x00 to 0x0A, 0x0C and 0x12 the DAG operation format of Table II applies. The address field is divided into action and context as shown.

TABLE II




Action

The 'action' field describes the address modification/generation process using a set of registers (base, limit, index and delta) pointed to by the 'context' field.

TABLE 1

DAG address calculation

| action | Operation | Description |
|---|---|---|
| 00 | Supply an address and post modify | Address = Base + Index<br>Index = Index + delta (delta is a signed value)<br>If Index >= limit, Index = Index − limit<br>If Index <0, Index = limit + Index |
| 01 | Supply a pre-modified address | Index = Index + delta (delta is a signed value)<br>If Index >= limit, Index = Index − limit<br>If Index <0, Index = limit + Index<br>Address = Base + Index |
| 11 | Supply a bit-reversed address | Address = Base + B-Index<br>B-Index = reverse carry add (Index + delta)<br>(delta is a signed value)<br>If Index >= limit, Index = Index − Limit<br>If Index <0, Index = limit + Index |

Context

The 'context' field is used to point at a specific DAG setting (base, limit, index and delta) on which an 'action' is performed or a DAG register is accessed (II)

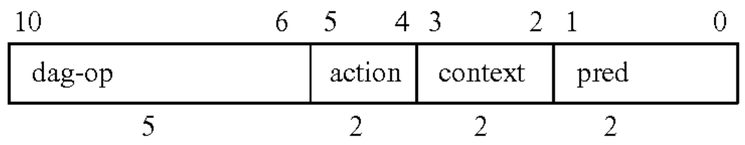
TABLE 2

context encoding

| Context | Operation |
|---|---|
| 00 | Use setting - basen.0, limitn.0, indexn.0, deltan.0 for DAGn |
| 01 | Use setting - basen.1, limitn.1, indexn.1, deltan.1 for DAGn |
| 10 | Use setting - basen.2, limitn.2, indexn.2, deltan.2 for DAGn |
| 11 | Use setting - basen.3, limitn.3, indexn.3, deltan.3 for DAGn |

For convenience, an ACTION function is defined according to the action table—ACTION (action, context) where 'action' and 'context' refer to the DAG operation fields. This function is used in the individual DAG operation descriptions.

(II) For dag-op: 0x0D to 0x11 the following DAG operation format applies:




The 'dag-reg' field is used to identify a specific 16-bit register (base or limit or index or delta) within a DAG 'context' as specified by the dag-reg table (below)

TABLE 3

dag-reg encoding for dag-op 0x0D, 0x10 and 0x11

| dag-reg | Register |
|---|---|
| 00 | base |
| 01 | limit |
| 10 | index |
| 11 | delta |

For operations 0x0E and 0x0F, the dag-reg field is used to address 2 DAG registers—base and limit or index and delta or a write buffer location. In this case, the 'dag-reg' table is as follows:

TABLE 4

dag-reg encoding for dag-op 0x0E

| dag-reg | Register |
|---|---|
| 0X | Base and limit |
| 1X | Index and delta |

X - don't care

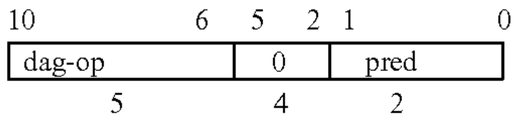
TABLE 5

dag-reg encoding for dag-op 0x0F

| dag-reg | Register |
|---|---|
| 00 | Base and limit |
| 10 | Index and delta |
| 11 | Location 'n' of write buffer for DAGn |

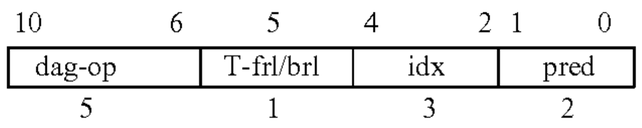
01 - undefined

(III) For dag-op: 0x0B, 0x13, 0x14, and 0x16 the following DAG operation format applies:




The address field in this case is unused, which is represented as "0" in the RXN.

(IV) For dag-op: 0x15 the following DAG operation format applies:




The 'T-frl/brl' field is used to choose between the translation frl and the translation brl

| T-frl/brl | Operation |
|---|---|
| 0 | The 'idx' field points to T-frl |
| 1 | The 'idx' field points to T-brl |

The T-frl and T-brl each have 5 32-bit locations. The 'idx' field is used to address these five locations

| add | Operation |
|---|---|
| 000 | Location 0 |
| 001 | Location 1 |
| 010 | Location 2 |
| 011 | Location 3 |
| 100 | Location 4 |
| 101 | Location 5 |

Pred

The universal 'pred' field along with the 's' bit determines whether a DAG operation is executed or not executed. When a DAG operation is 'not executed' due to its predication, the last executed DAG operation executes again.

TABLE 6

Pred field encoding

| Pred | Description |
|---|---|
| 00 | Never execute |
| 01 | Always execute (execute specified operations) |
| 10 | Execute if condition is true ("s" bit is set) (execute specified operation)<br>If condition is false ("s" bit is not set) (do not execute the DAG operation) |
| 11 | Execute if condition is false ("s" bit is not set) (execute specified operation)<br>If condition is true ("s" bit is set) (do not execute the DAG operation) |

Note:
All DAG operations execute every clock cycle until "dagnoop" operation is chosen.

Although the invention has been discussed with respect to specific embodiments thereof, these embodiments are merely illustrative, and not restrictive, of the invention. For example, although the node has been described as part of an adaptive computing machine, or environment, aspects of the filter node design, processing and functions can be used with other types of systems. In general, the number of lines and specific interconnections can vary in different embodiments. Specific components, e.g., the data address generator, can be implemented in different ways in different designs. Components may be omitted, substituted or implemented with one or more of the same or different components. For example, a data address generator can be substituted with a general register, or it can be a different component responsive to a control word. Many variations are possible.

Thus, the scope of the invention is to be determined solely by the claims.

What is claimed is:

**1**. A reconfigurable data path circuit coupled to a memory bus for obtaining data from a memory, the reconfigurable data path circuit comprising:

a plurality of functional units configured to perform a digital operation;

one or more data address generators coupled to the memory bus;

a configurable data path configurably coupled to the one or more data address generators and the plurality of functional units, the configurable data path being configurable in response to a first configuration information by configuring or reconfiguring at least one interconnection between the one or more data address generators and the plurality of functional units;

wherein the one or more data address generators are coupled to the memory bus and the configurable data path, each of the one or more data address generators being configurable in response to a second configuration information that is different from the first configuration information to generate memory addresses from which data is to be read from or written to the memory for the data path configuration; and

wherein the second configuration information includes predication information, the generation of the memory addresses in response to the second configuration information being conditioned upon the predication information.

2. A reconfigurable data path circuit of claim 1, wherein each of the one or more data address generators is configurable as a function of both the predication information and other information in the second configuration information to determine whether to generate one of the memory addresses in response to the second configuration information.

3. The reconfigurable data path circuit of claim 2, wherein each of the one or more data address generators is configurable as a function of the predication information to operate other than generating one of the memory addresses.

4. The reconfigurable data path circuit of claim 1, wherein each of the one or more data address generators is configurable for non-sequential operation as a function of the predication information.

5. The reconfigurable data path circuit of claim 1, wherein the first and second configuration information each comprises a separate control word.

6. The reconfigurable data path circuit of claim 5, wherein each separate control word includes an operation field including the predication information.

7. The reconfigurable data path circuit of claim 6, wherein each separate control word further comprises an address field designating one of the memory addresses.

8. The reconfigurable data path circuit of claim 1, wherein the one or more data address generators are further configurable or reconfigurable in response to the second configuration information to read data of one or more widths from the memory bus consistent with and for the data path configuration.

9. The reconfigurable data path circuit of claim 1, wherein the one or more data address generators are configurable in response to the second configuration information to split data received from the memory bus onto the configurable data path.

10. The reconfigurable data path circuit of claim 9, wherein the one or more data address generators transfer data to the configurable data path for processing by the functional units in parallel.

11. The reconfigurable data path circuit of claim 1, wherein the configurable data path is reconfigurable to change from a first data path configuration having one 16 bit path to a second data path configuration having two 8 bit paths in response to the first configuration information; and each of the one or more data address generators is configurable in response to the second configuration information to generate two memory addresses for writing and reading two 8 bit words for the second data path configuration, and wherein the generation of the two memory addresses is conditioned upon the predication information.

12. The reconfigurable data path circuit of claim 1, wherein the one or more data address generators are further configurable in response to the second configuration information for transferring data to the memory bus for writing to the memory, the generation of a respective memory address for the writing of the data being conditioned upon the predication information.

13. The reconfigurable data path circuit of claim 1, wherein the plurality of functional units include a multiplier and an accumulator, the accumulator being adapted to accumulate outputs from the multipliers into a register, the reconfigurable data path circuit further comprising a direct data path coupling the multiplier and the accumulator.

14. The reconfigurable data path circuit of claim 13, wherein the plurality of functional units further includes an Arithmetic Logic Unit (ALU).

15. The reconfigurable data path circuit of claim 1, further comprising a plurality of register files each configurably interconnected by the configurable data path to the plurality of functional units and to one of the one or more data address generators.

16. The reconfigurable data path circuit of claim 1, wherein the configurable data path further comprises a reconfigurable interconnection network configurable for configuring or reconfiguring the interconnections between the one or more data address generators and the plurality of functional units for the data path configuration.

17. The reconfigurable data path circuit of claim 16, wherein the reconfigurable interconnection network includes a plurality of groups of data lines configurably coupled to the one or more data address generators and the plurality of functional units.

18. The reconfigurable data path circuit of claim 17, wherein the reconfigurable interconnection network is configurable or reconfigurable to create portions of the reconfigurable data path having different widths, the portions being coupled between the one or more data address generators and the plurality of functional units.

19. The reconfigurable data path circuit of claim 15, wherein the configurable data path further comprises a reconfigurable interconnection network comprising a plurality of groups of data lines configurably coupled to the one or more data address generators, the functional units, and the plurality of register files in the configurable data path, wherein each register file of the plurality of register files is coupled to a group of data lines of the plurality of groups of data lines in the configurable data path in a one-to-one correspondence, the plurality of register files being adapted for storing data from the respective group of data lines to which the respective ones of the plurality of register files is coupled.

20. The reconfigurable data path circuit of claim 1, wherein the interconnections between the configurable data path and the one or more data address generators are configurable in real time.

21. The reconfigurable data path circuit of claim 1, wherein at least one of the plurality of functional units is configurable to provide at least two different functions.

22. The reconfigurable data path circuit of claim 16, wherein the plurality of functional units are configurable to provide a second plurality of configurable data paths between respective ones of the plurality of functional units and the reconfigurable interconnection network.

23. The reconfigurable data path circuit of claim 22, wherein the second plurality of configurable data paths are configurable for a plurality of data widths.

24. The reconfigurable data path circuit of claim 1, wherein each of the functional units of the plurality of functional units comprises one of a multiplier, an accumulator, a data cache, an Arithmetic Logic Unit (ALU), or a register file.

25. The reconfigurable data path circuit of claim 24, wherein the reconfigurable data path includes the multiplier, the accumulator, the data cache, the Arithmetic Logic Unit (ALU), the register file, and the reconfigurable data path includes interconnects between the functional units of the reconfigurable data path.

26. The reconfigurable data path circuit of claim 1, wherein each of the one or more data address generators is further configurable in response to the second configuration information to control memory addresses from which data is to be read from or written to the memory for the data path configuration, the control of the memory addresses in response to the second configuration information being conditioned upon the predication information.

27. A digital processing system comprising:
a memory bus coupled to a memory; and
a reconfigurable data path circuit coupled to the memory bus for obtaining data from the memory, the reconfigurable data path circuit comprising:
a plurality of functional units configurable to perform a digital operation; and
one or more data address generators coupled to the memory bus;
a configurable data path configurably coupled to the one or more data address generators and the plurality of functional units, the configurable data path being configurable in response to a first configuration information by configuring or reconfiguring at least one interconnection between the one or more data address generators and the plurality of functional units;
wherein the one or more data address generators are coupled to the memory bus and the configurable data path, each of the one or more data address generators being configurable in response to a second configuration information that is different from the first configuration information to generate memory addresses from which data is to be read from or written to the memory for the data path configuration; and
wherein the second configuration information includes predication information, the generation of the memory addresses in response to the second configuration information being conditioned upon the predication information.

28. The digital processing system of claim 27, wherein each of the one or more data address generators is further configurable in response to the second configuration information to control memory addresses from which data is to be read from or written to the memory for the data path configuration, the control of the memory addresses in response to the second configuration information being conditioned upon the predication information.

29. The digital processing system of claim 27, wherein each of the one or more data address generators is configurable as a function of both the predication information and other information in the second configuration information to determine whether to generate one of the memory addresses in response to the second configuration information.

30. The digital processing system of claim 27, wherein the configurable data path further comprises a reconfigurable interconnection network comprising the plurality of groups of data lines and being configurable for configuring or reconfiguring the interconnections between or among the one or more data address generators and the plurality of functional units for the data path configuration.

31. The digital processing system of claim 30, wherein the reconfigurable interconnection network is configurable or reconfigurable to create portions of the reconfigurable data paths having different widths, the portions being coupled between the one or more data address generators and the plurality of functional units.

32. The digital processing system of claim 30, wherein the plurality of functional units include a multiplier, an accumulator, and an Arithmetic Logic Unit (ALU), the reconfigurable data path circuit further comprising a direct data path coupling the multiplier and the accumulator.

33. The digital processing system of claim 27, wherein at least one of the plurality of functional units is configurable to provide two different functions.

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