US008368193B2

(12) United States Patent
Lin et al.

(10) Patent No.: US 8,368,193 B2
(45) Date of Patent: Feb. 5, 2013

(54) **CHIP PACKAGE**

(75) Inventors: **Mou-Shiung Lin**, Hsinchu (TW); **Shih-Hsiung Lin**, Hsinchu (TW); **Hsin-Jung Lo**, Taipei County (TW)

(73) Assignee: **Megica Corporation**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/236,507**

(22) Filed: **Sep. 19, 2011**

(65) **Prior Publication Data**

US 2012/0007237 A1 Jan. 12, 2012

Related U.S. Application Data

(63) Continuation of application No. 12/353,250, filed on Jan. 13, 2009, now Pat. No. 8,044,475, which is a continuation of application No. 11/422,337, filed on Jun. 6, 2006, now Pat. No. 7,495,304.

(30) **Foreign Application Priority Data**

Jun. 6, 2005 (TW) .... 94118540 A

(51) **Int. Cl.**
H01L 23/02 (2006.01)

(52) **U.S. Cl.** **257/678**; 257/737; 257/E31.117

(58) **Field of Classification Search** 257/432–436, 257/680, E23.009, E23.01, E23.011; 438/69, 438/70, 116, 121

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,148,265	A	9/1992	Khandros et al.
5,148,266	A	9/1992	Khandros et al.
5,258,330	A	11/1993	Khandros et al.
5,346,861	A	9/1994	Khandros et al.
5,347,159	A	9/1994	Khandros et al.
5,632,631	A	5/1997	Fjelstad et al.
5,679,977	A	10/1997	Khandros et al.
5,682,061	A	10/1997	Khandros et al.
5,685,885	A	11/1997	Khandros et al.
5,848,467	A	12/1998	Khandros et al.
5,852,326	A	12/1998	Khandros et al.
5,934,914	A	8/1999	Fjelstad et al.
5,950,304	A	9/1999	Khandros et al.
6,133,627	A	10/2000	Khandros et al.
6,168,965	B1	1/2001	Malinovich
6,169,319	B1	1/2001	Malinovich
6,177,293	B1	1/2001	Netzer
6,200,712	B1	3/2001	Fan et al.
6,221,687	B1	4/2001	Abramovich
6,225,013	B1	5/2001	Cohen
6,239,386	B1	5/2001	DiStefano et al.
6,247,228	B1	6/2001	Distefano et al.
6,274,820	B1	8/2001	DiStefano et al.
6,285,065	B1	9/2001	Levy
6,288,434	B1	9/2001	Levy
6,339,247	B1	1/2002	Taguchi
6,362,498	B2	3/2002	Abramovich

(Continued)

OTHER PUBLICATIONS

Mistry, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pp. 247-250.

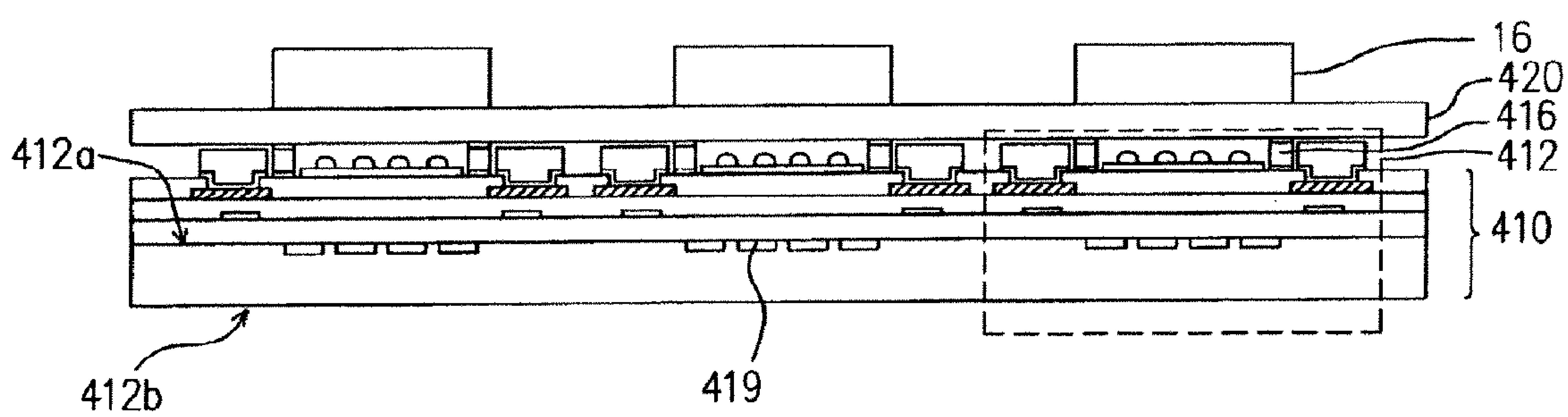
(Continued)

Primary Examiner — Zandra Smith
Assistant Examiner — Paul Patton
(74) *Attorney, Agent, or Firm* — McDermott Will & Emery LLP

(57) **ABSTRACT**

A chip package includes a bump connecting said semiconductor chip and said circuitry component, wherein the semiconductor chip has a photosensitive area used to sense light. The chip package may include a ring-shaped protrusion connecting a transparent substrate and the semiconductor chip.

39 Claims, 20 Drawing Sheets



U.S. PATENT DOCUMENTS

6,372,527	B1	4/2002	Khandros et al.	
6,387,732	B1	5/2002	Akram	
6,392,306	B1	5/2002	Khandros et al.	
6,429,036	B1	8/2002	Nixon	
6,433,419	B2	8/2002	Khandros et al.	
6,465,893	B1	10/2002	Khandros et al.	
6,617,174	B2	9/2003	Rotstein	
6,744,109	B2	6/2004	Barton et al.	
6,831,000	B2 *	12/2004	Murayama	438/613
6,872,984	B1	3/2005	Leung	
6,885,107	B2	4/2005	Kinsman	
7,098,078	B2	8/2006	Khandros et al.	
7,122,874	B2 *	10/2006	Kim	257/433
7,141,869	B2	11/2006	Kim et al.	
7,172,922	B2	2/2007	Benjamin	
7,198,969	B1	4/2007	Khandros et al.	
7,221,051	B2	5/2007	Ono et al.	
7,259,438	B2 *	8/2007	Yamamoto et al.	257/433
7,271,481	B2	9/2007	Khandros et al.	
7,291,910	B2	11/2007	Khandros et al.	
7,495,304	B2	2/2009	Lin et al.	
8,044,475	B2	10/2011	Lin et al.	
2001/0030370	A1	10/2001	Khandros et al.	
2002/0011663	A1	1/2002	Khandros et al.	
2002/0155728	A1	10/2002	Khandros et al.	
2003/0168253	A1	9/2003	Khandros et al.	
2004/0084741	A1	5/2004	Boon	
2005/0087855	A1	4/2005	Khandros et al.	
2005/0218495	A1	10/2005	Khandros et al.	
2006/0244135	A1	11/2006	Khandros et al.	

OTHER PUBLICATIONS

Edelstein, D.C., “Advantages of Copper Interconnects,” Proceedings of the 12th International IEEE VLSIi Multilevel Interconnection Conference (1995) pp. 301-307.

Theng, C. et al. “An Automated Tool Deployment for ESD (Electro-Static-Discharge) Correct-by-Construction Strategy in 90 nm Process,” IEEE International Conference on Semiconductor Electronics (2004) pp. 61-67.

Gao, X. et al. “An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance,” Solid-State Electronics, 27 (2003), pp. 1105-1110.

Yeoh, A. et al. “Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing,” Electronic Components and Technology Conference (2006) pp. 1611-1615.

Hu, C-K. et al. “Copper-Polyimide Wiring Technology for VLSI Circuits,” Materials Research Society Symposium Proceedings VLSI V (1990) pp. 369-373.

Roesch, W. et al. “Cycling copper flip chip interconnects,” Microelectronics Reliability, 44 (2004) pp. 1047-1054.

Lee, Y-H. et al. “Effect of ESD Layout on the Assembly Yield and Reliability,” International Electron Devices Meeting (2006) pp. 1-4.

Yeoh, T-S. “ESD Effects on Power Supply Clamps,” Proceedings of the 6th International Symposium on Physical & Failure Analysis of Integrated Circuits (1997) pp. 121-124.

Edelstein, D. et al. “Full Copper Wiring in a Sub-0.25 pm CMOS ULSI Technology,” Technical Digest IEEE International Electron Devices Meeting (1997) pp. 773-776.

Venkatesan, S. et al. “A High Performance 1.8V, 0.20 pm CMOS Technology with Copper Metallization,” Technical Digest IEEE International Electron Devices Meeting (1997) pp. 769-772.

Jenei, S. et al. “High Q Inductor Add-on Module in Thick Cu/SiLK™ single damascene,” Proceedings from the IEEE International Interconnect Technology Conference (2001) pp. 107-109.

Groves, R. et al. “High Q Inductors in a SiGe BiCMOS Process Utilizing a Thick Metal Process Add-on Module,” Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting (1999) pp. 149-152.

Sakran, N. et al. “The Implementation of the 65nm Dual-Core 64b Merom.Processor,” IEEE International Solid-State Circuits Conference, Session 5, Microprocessors, 5.6 (2007) pp. 106-107, p. 590.

Kumar, R. et al. “A Family of 45nm IA Processors,” IEEE International Solid-State Circuits Conference, Session 3, Microprocessor Technologies, 3.2 (2009) pp. 58-59.

Bohr, M. “The New Era of Scaling in an SoC World,” International Solid-State Circuits Conference (2009) Presentation Slides 1-66.

Bohr, M. “The New Era of Scaling in an SoC World,” International Solid-State Circuits Conference (2009) pp. 23-28.

Ingerly, D. et al. “Low-K Interconnect Stack with Thick Metal 9 Redistribution Layer and Cu Die Bump for 45nm High Volume Manufacturing,” International Interconnect Technology Conference (2008) pp. 216-218.

Kurd, N. et al. “Next Generation Intel® Micro-architecture (Nehalem) Clocking.Architecture,” Symposium on VLSI Circuits Digest of Technical Papers (2008) pp. 62-63.

Maloney, T. et al. “Novel Clamp Circuits for IC Power Supply Protection,” IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part C, vol. 19, No. 3 (Jul. 1996) pp. 150-161.

Geffken, R. M. “An Overview of Polyimide Use in Integrated Circuits and Packaging,” Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology (1991) pp. 667-677.

Luther, B. et al. “Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices,” Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference (1993) pp. 15-21.

Master, R. et al. “Ceramic Mini-Ball Grid Array Package for High Speed Device,” Proceedings from the 45th Electronic Components and Technology Conference (1995) pp. 46-50.

Maloney, T. et al. “Stacked PMOS Clamps for High Voltage Power Supply Protection,” Electrical Overstress/Electrostatic Discharge Symposium Proceedings (1999) pp. 70-77.

Lin, M.S. et al. “A New System-on-a-Chip (SOC) Technology—High Q Post Passivation Inductors,” Proceedings from the 53rd Electronic Components and Technology Conference (May 30, 2003) pp. 1503-1509.

Megic Corp. “MEGIC way to system solutions through bumping and redistribution,” (Brochure) (Feb. 6, 2004) pp. 1-3.

Lin, M.S. “Post Passivation Technology™—MEGIC® Way to System Solutions,” Presentation given at TSMC Technology Symposium, Japan (Oct. 1, 2003) pp. 1-32.

Lin, M.S. et al. “A New IC Interconnection Scheme and Design Architecture for High Performance ICs at Very Low Fabrication Cost—Post Passivation Interconnection,” Proceedings of the IEEE Custom Integrated Circuits Conference (Sep. 24, 2003) pp. 533-536.

* cited by examiner

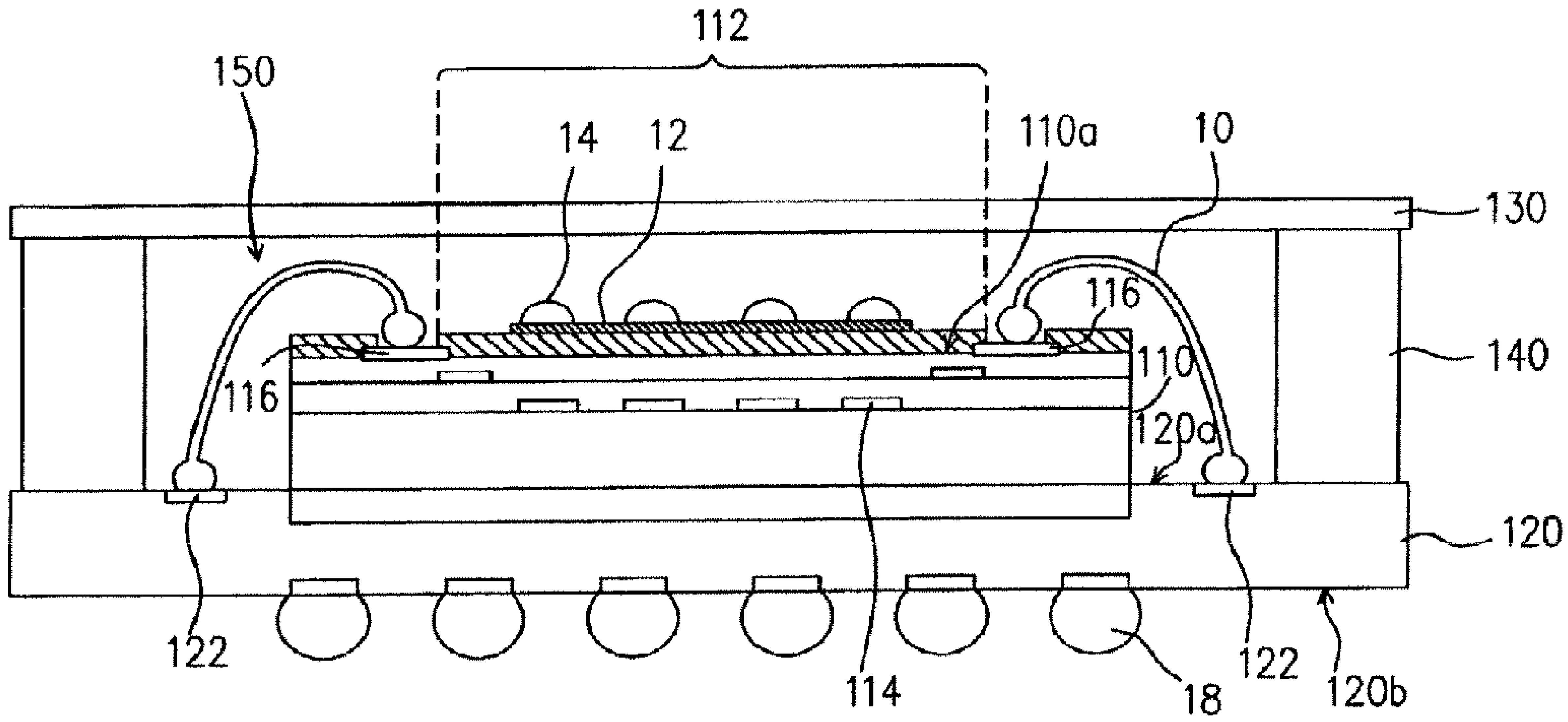


FIG. 1A (PRIOR ART)

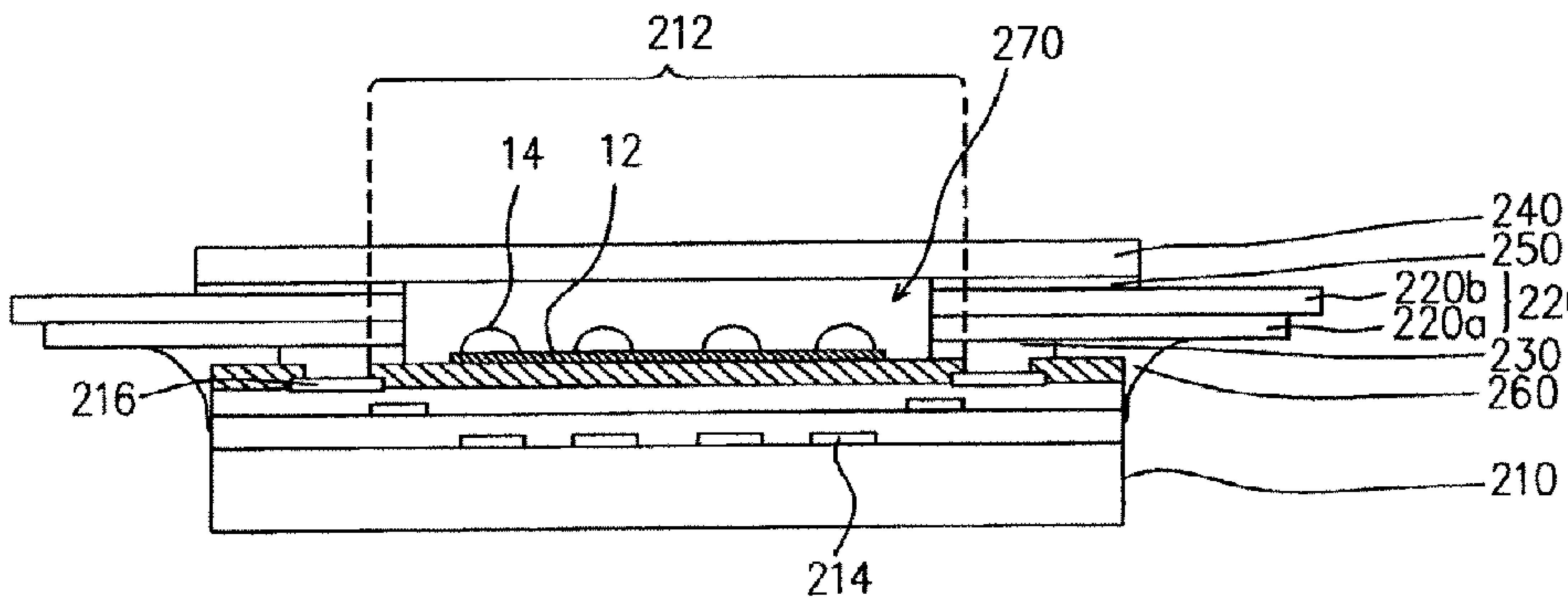


FIG. 1B (PRIOR ART)

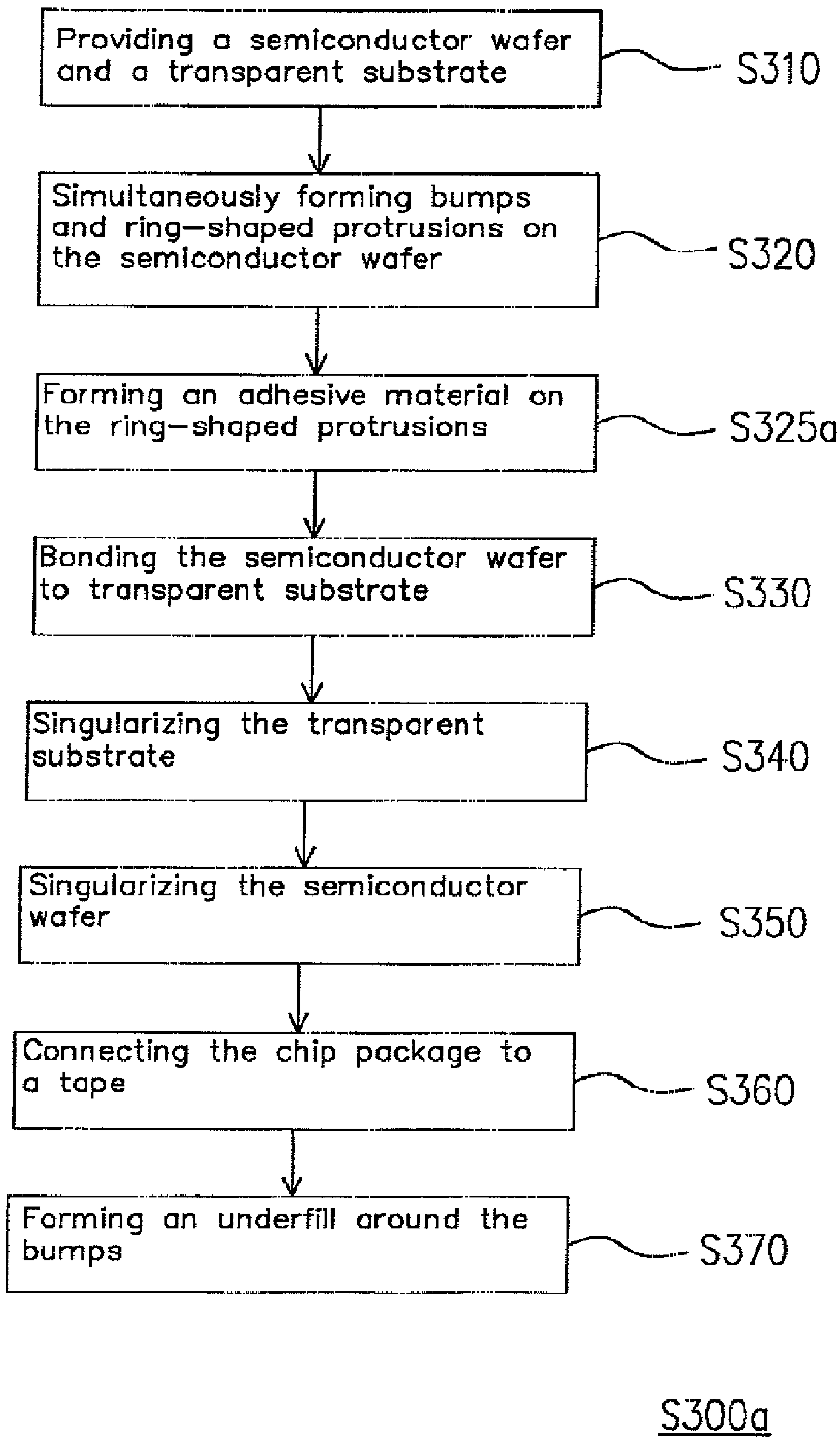

Providing a semiconductor wafer and a transparent substrate
S310
Simultaneously forming bumps and ring—shaped protrusions on the semiconductor wafer
S320
Forming an adhesive material on the ring—shaped protrusions
S325a
Bonding the semiconductor wafer to transparent substrate
S330
Singularizing the transparent substrate
S340
Singularizing the semiconductor wafer
S350
Connecting the chip package to a tape
S360
Forming an underfill around the bumps
S370
S300a

FIG.2A

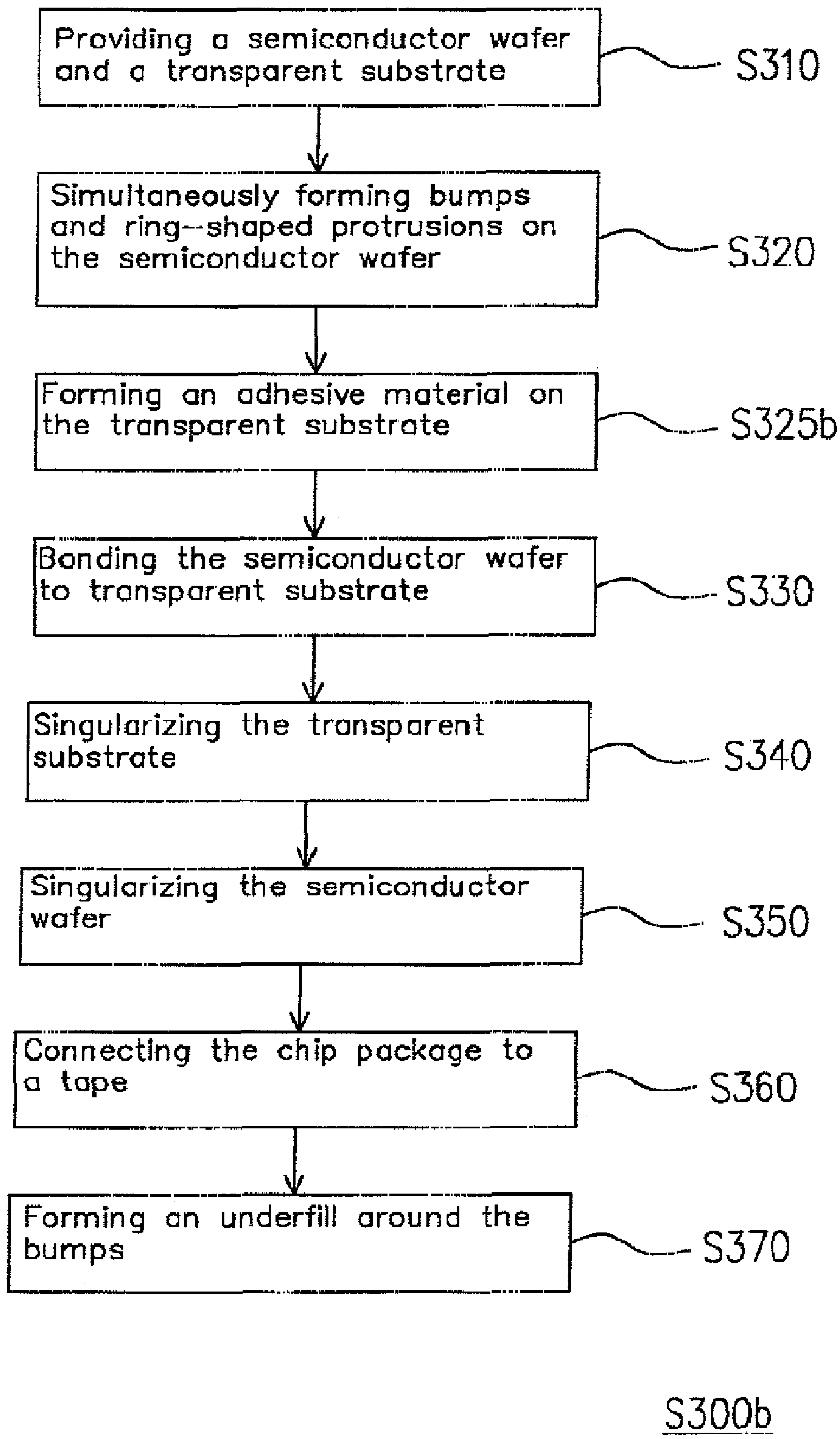

Providing a semiconductor wafer and a transparent substrate
S310
Simultaneously forming bumps and ring--shaped protrusions on the semiconductor wafer
S320
Forming an adhesive material on the transparent substrate
S325b
Bonding the semiconductor wafer to transparent substrate
S330
Singularizing the transparent substrate
S340
Singularizing the semiconductor wafer
S350
Connecting the chip package to a tape
S360
Forming an underfill around the bumps
S370
S300b

FIG.2B

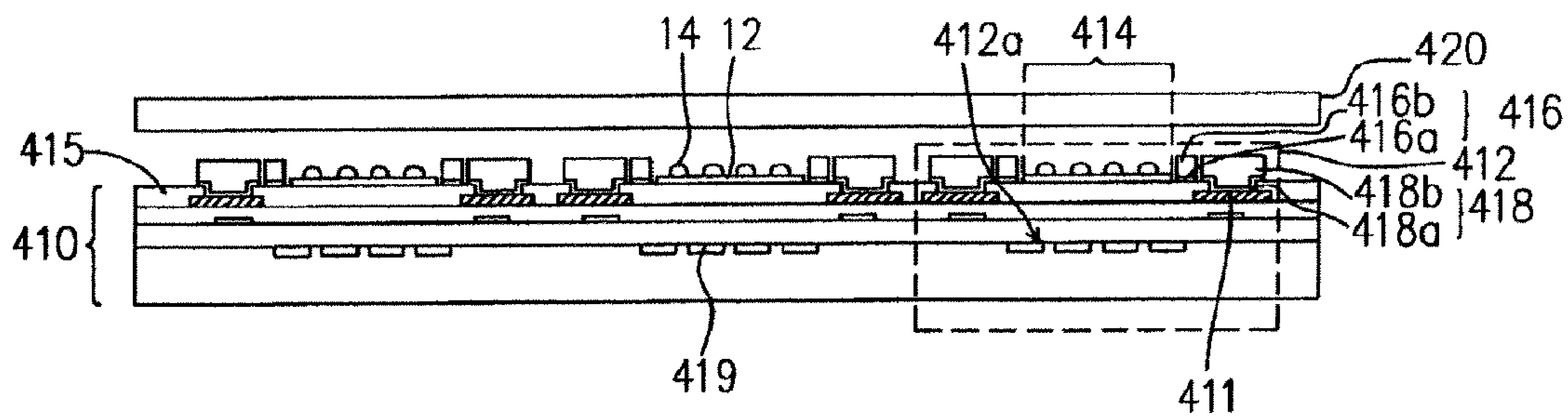

14
12
412a
414
420
416b
416
416a
412
415
418b
418
410
418a
419
411

FIG.3A

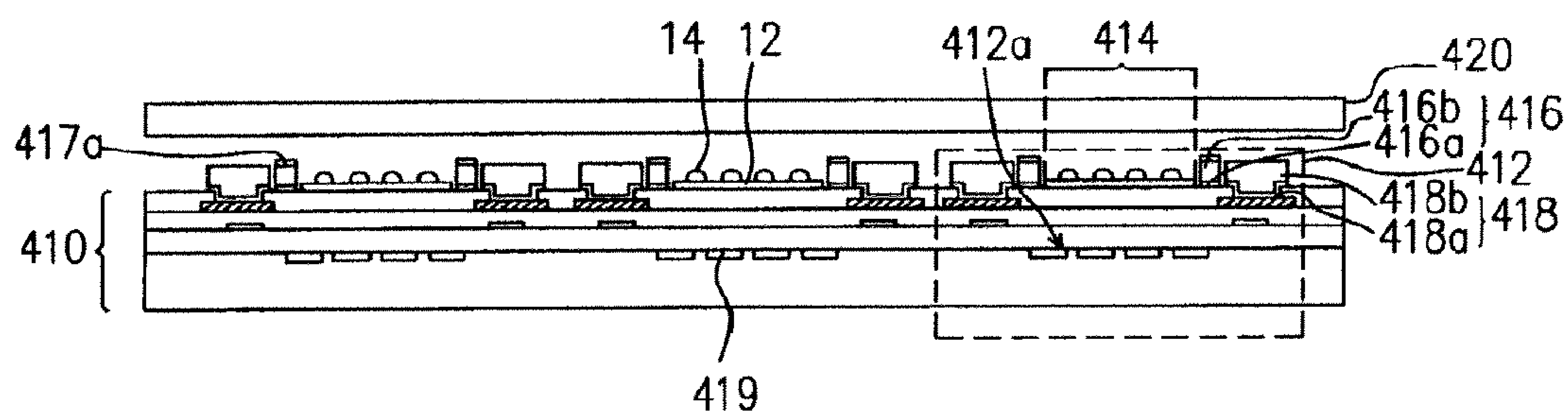

14
12
412a
414
420
416b
416
417a
416a
412
418b
418
410
418a
419

FIG.3B

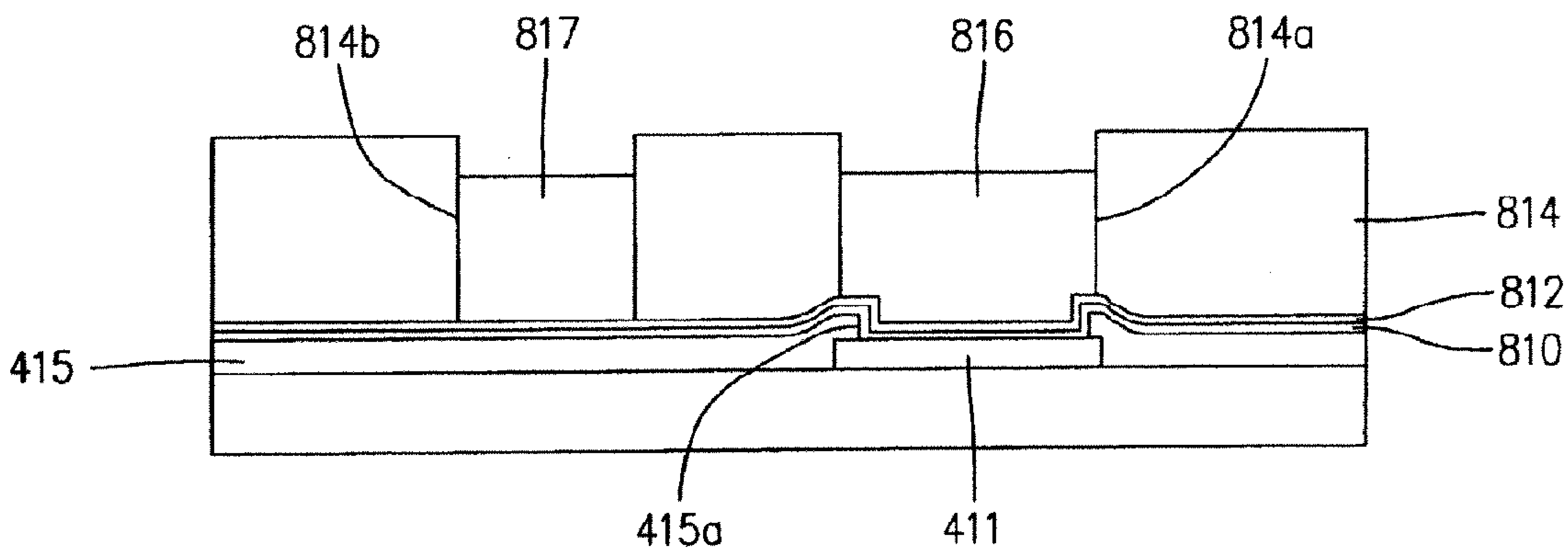


FIG. 3AA

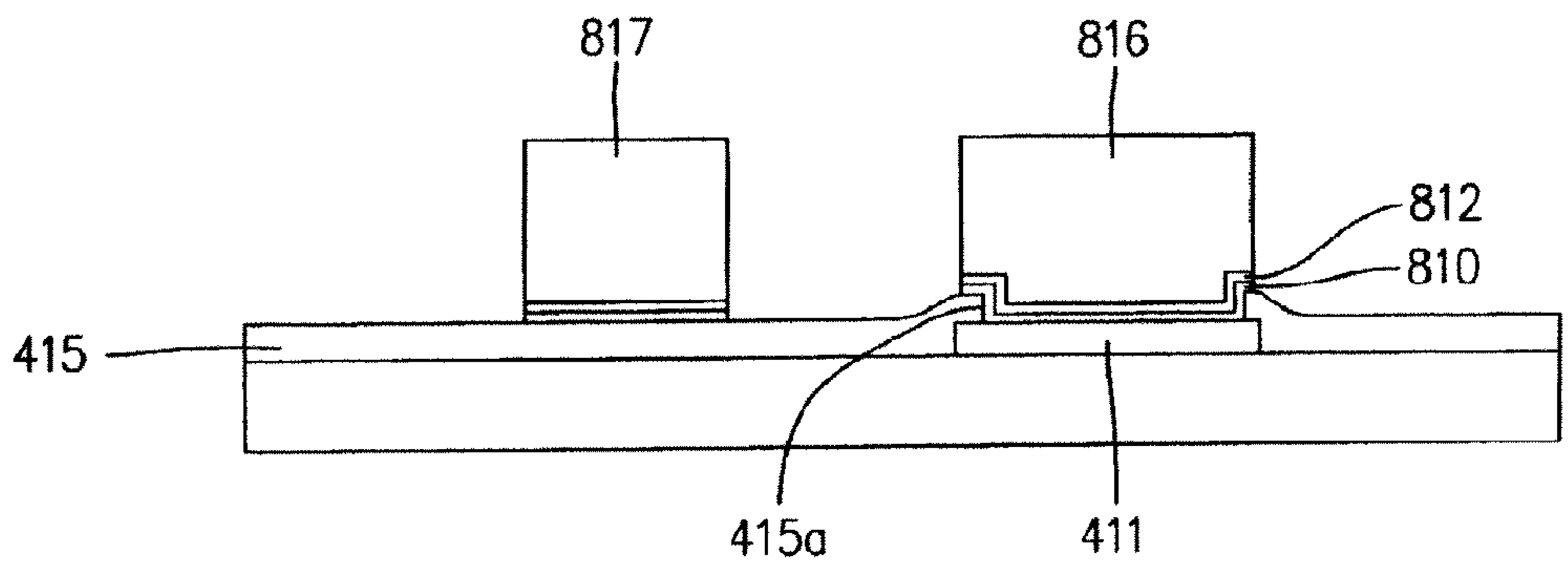


FIG. 3AB

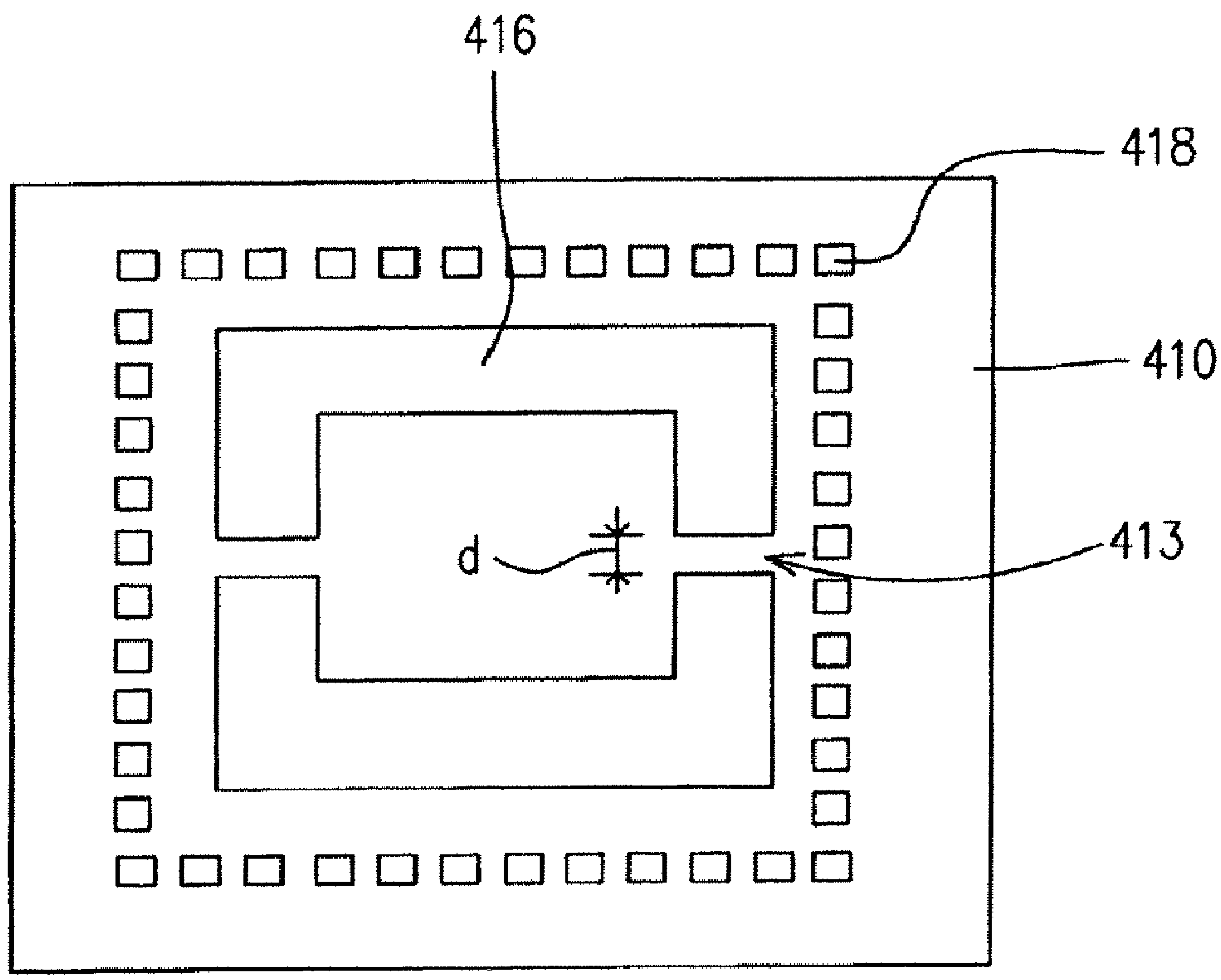


FIG.3AC

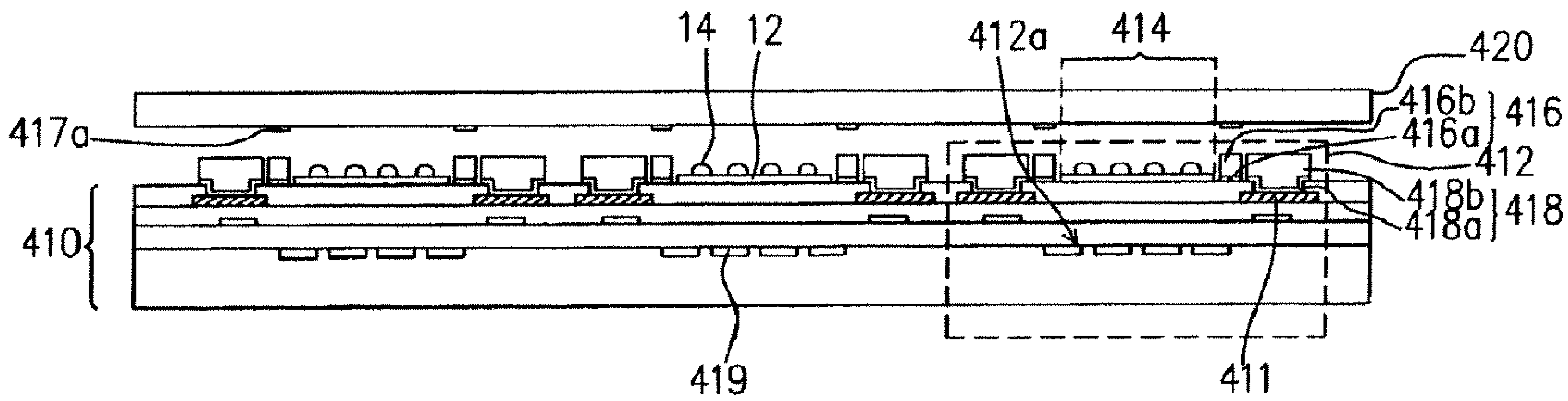

14
12
412a
414
420
417a
416b
416a
416
412
418b
418a
418
410
419
411

FIG.3B'

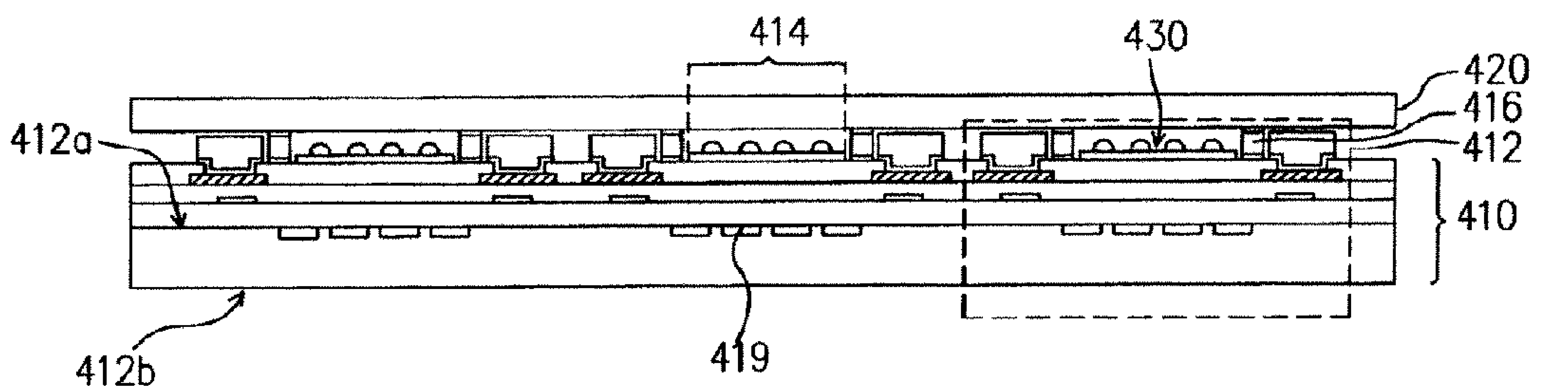

414
430
420
416
412
412a
410
412b
419

FIG.3C

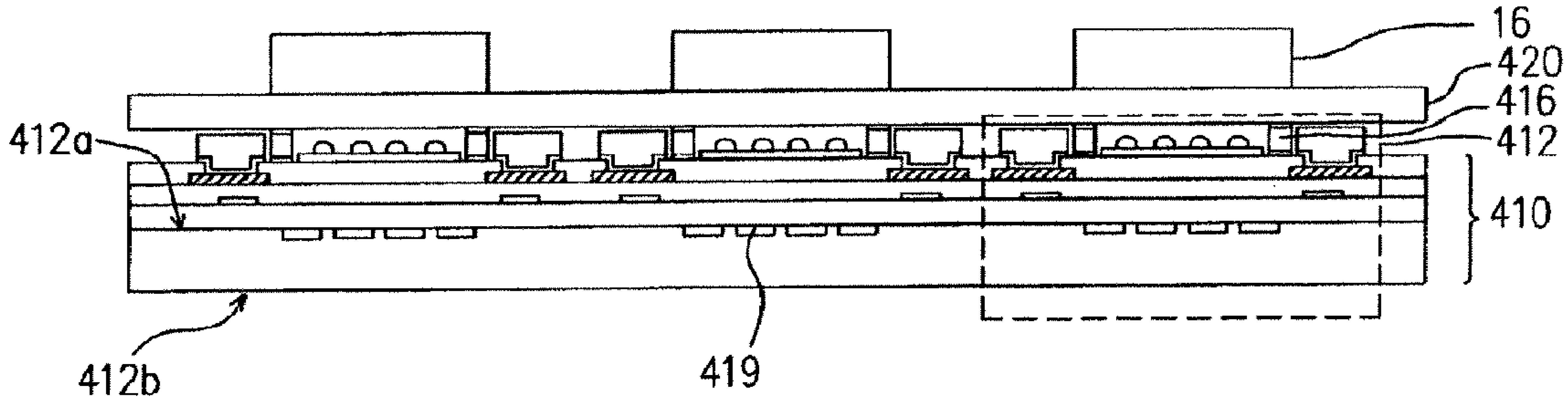


FIG.3D

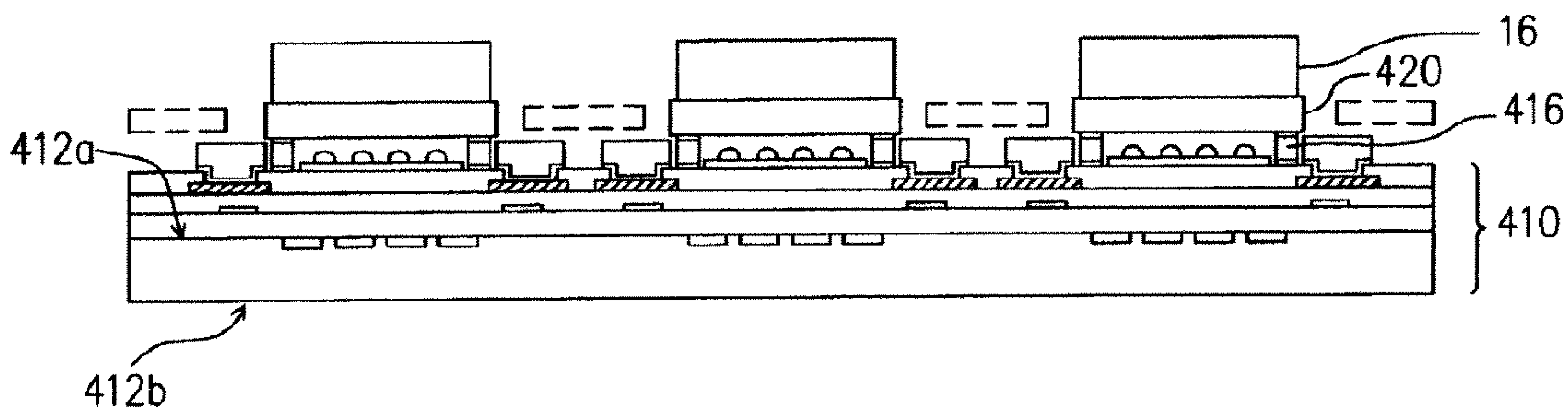


FIG.3E

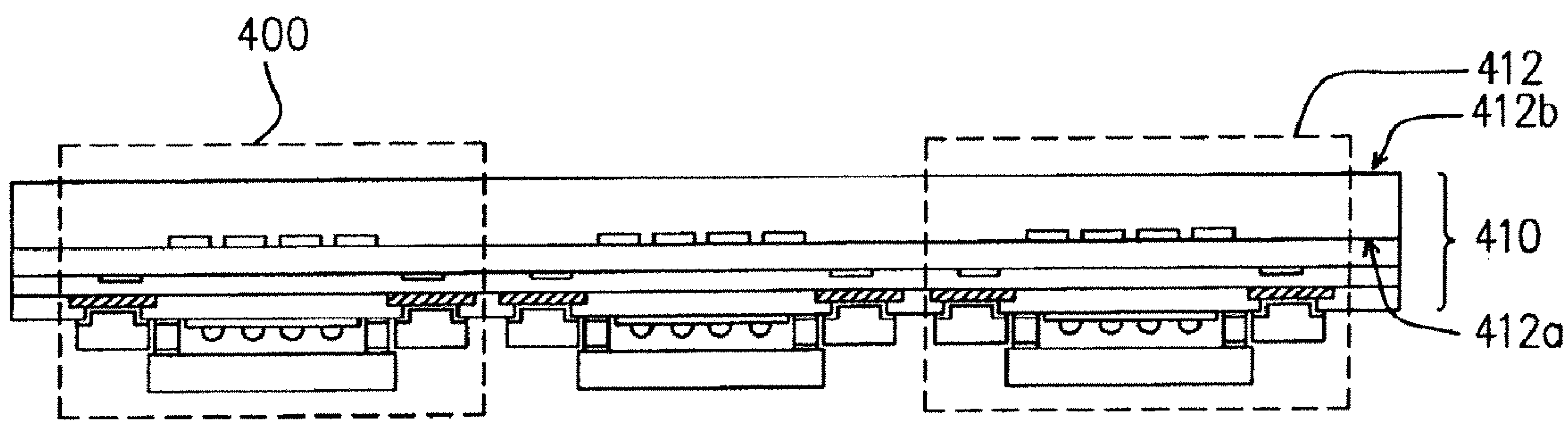


FIG.3F

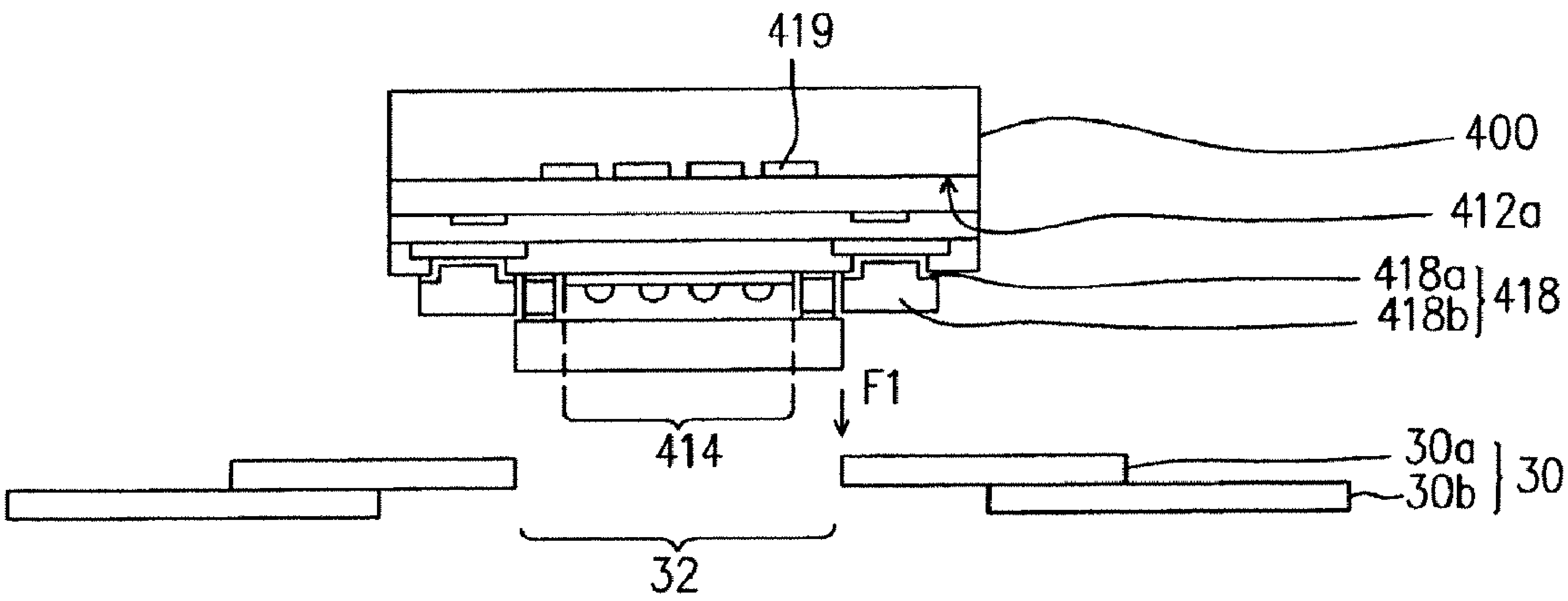

419
400
412a
418a
418b
418
F1
414
30a
30b
30
32

FIG.3G

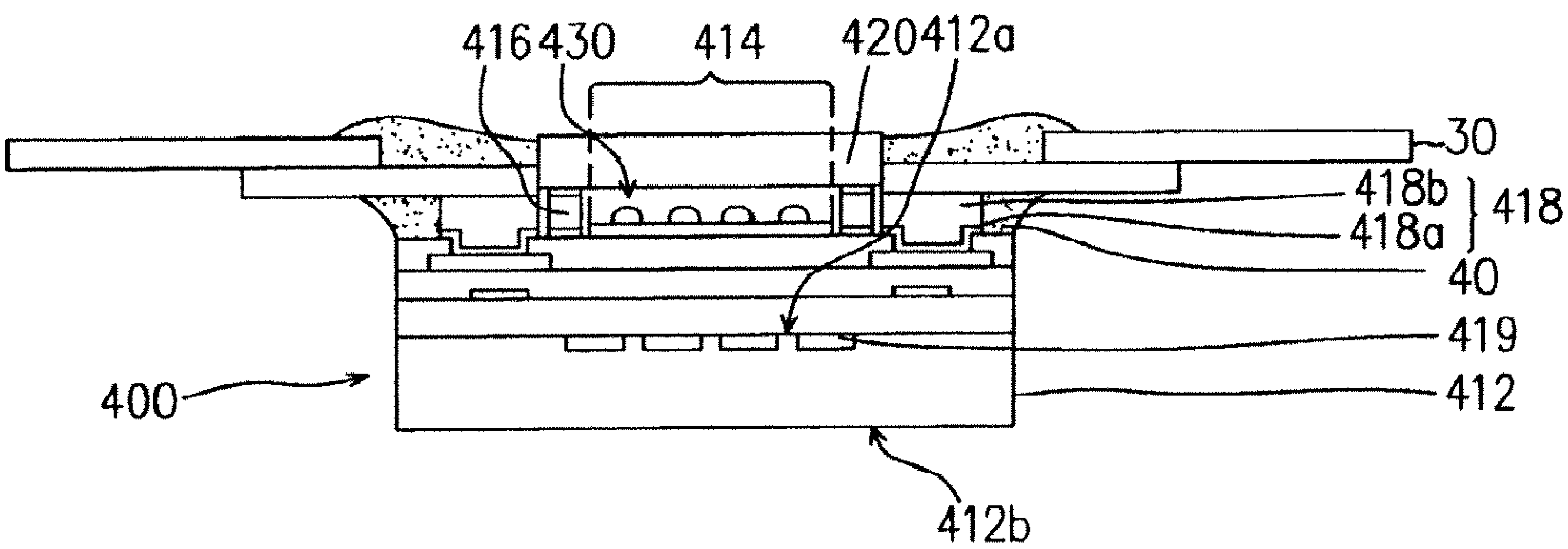
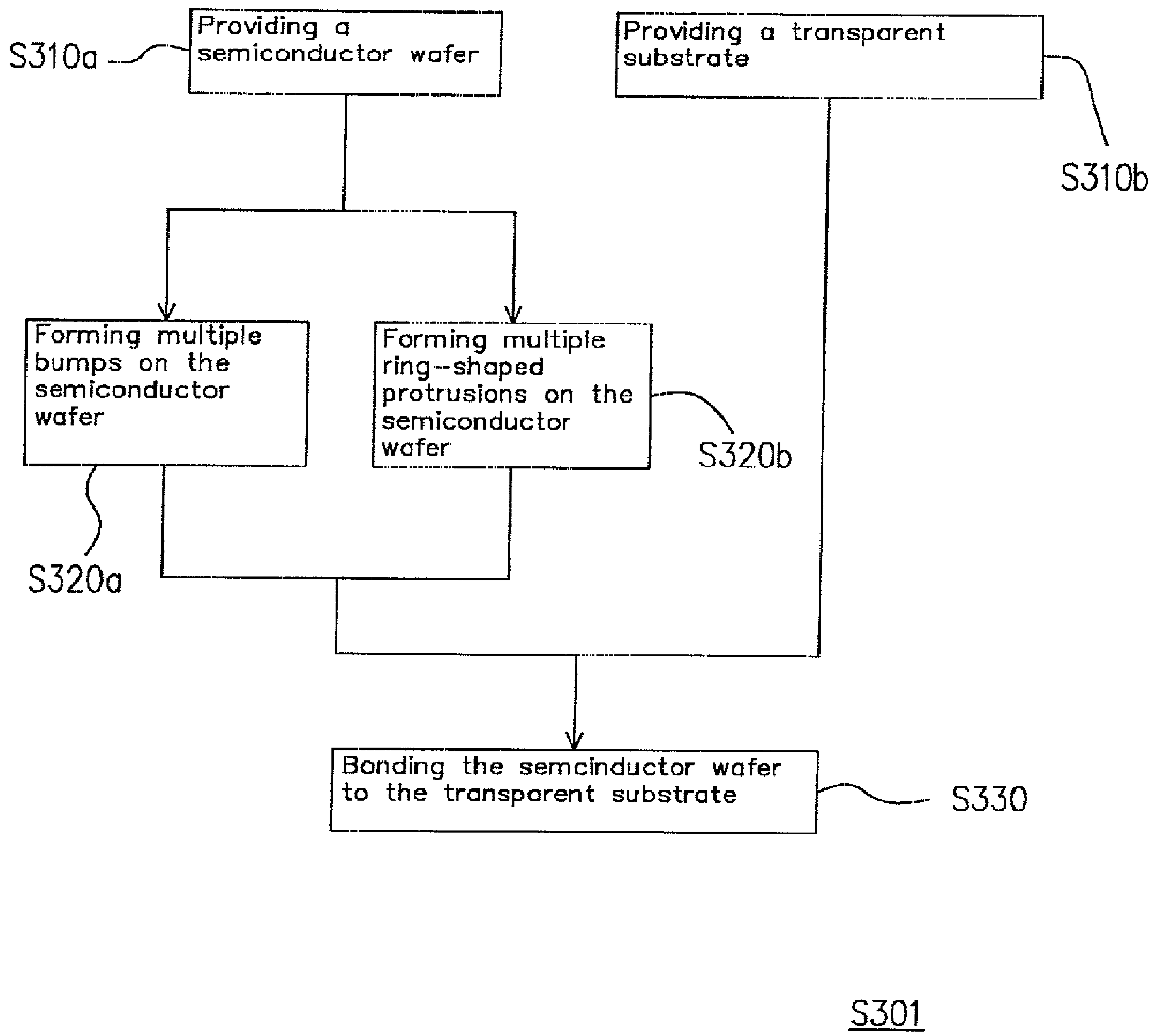

416
430
414
420
412a
30
418b
418a
418
40
419
400
412
412b

FIG.3H



Providing a semiconductor wafer
S310a
Providing a transparent substrate
S310b
Forming multiple bumps on the semiconductor wafer
S320a
Forming multiple ring-shaped protrusions on the semiconductor wafer
S320b
Bonding the semcinductor wafer to the transparent substrate
S330
S301

FIG.4A

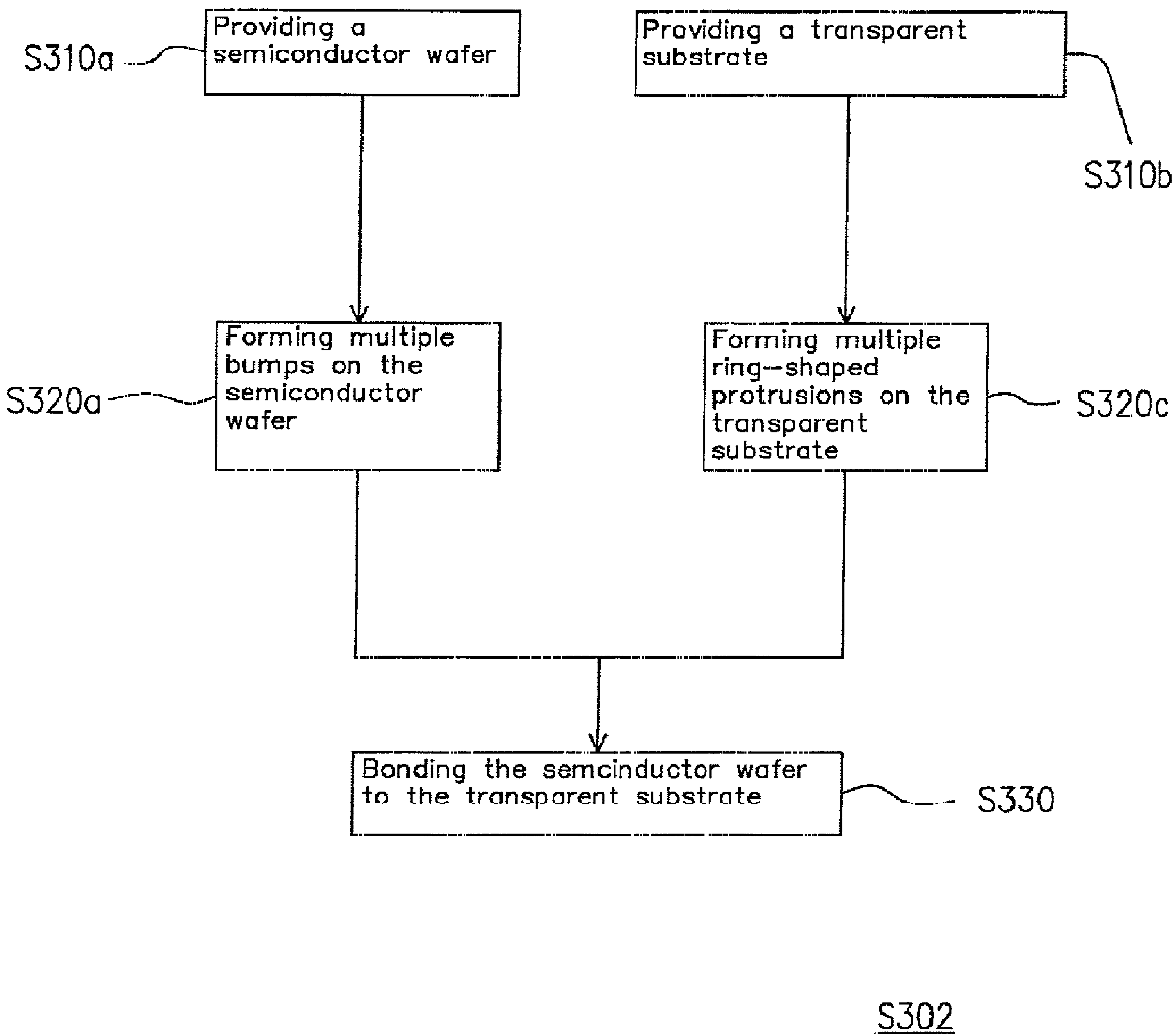

Providing a semiconductor wafer
S310a
Providing a transparent substrate
S310b
Forming multiple bumps on the semiconductor wafer
S320a
Forming multiple ring-shaped protrusions on the transparent substrate
S320c
Bonding the semcinductor wafer to the transparent substrate
S330
S302

FIG.4B

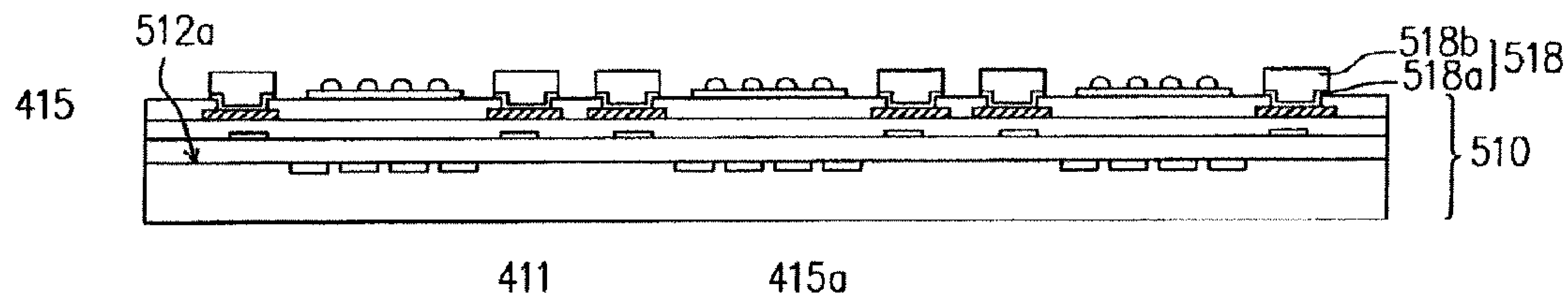

512a
518b
518
518a
415
510
411
415a

FIG.5A

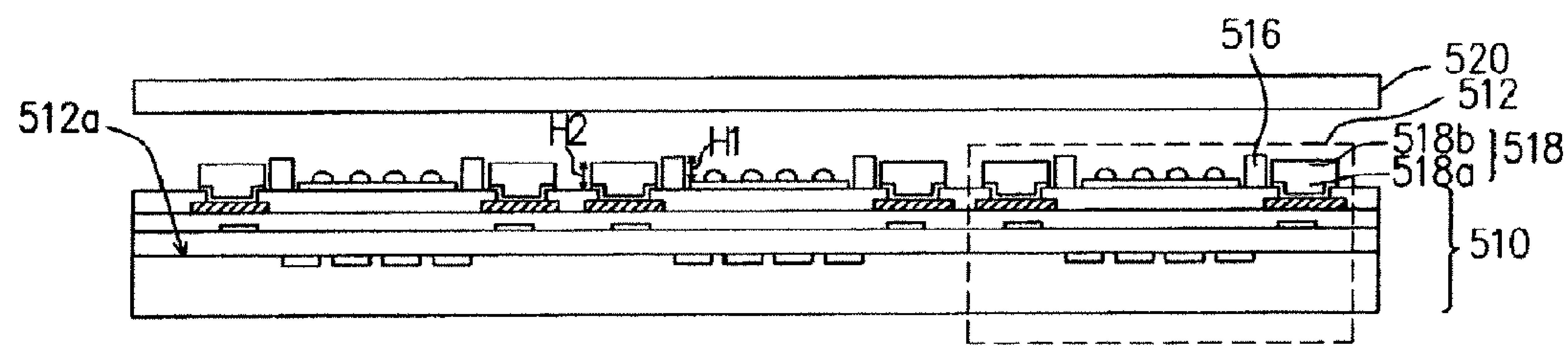

516
520
512
512a
H2
H1
518b
518
518a
510

FIG.5B

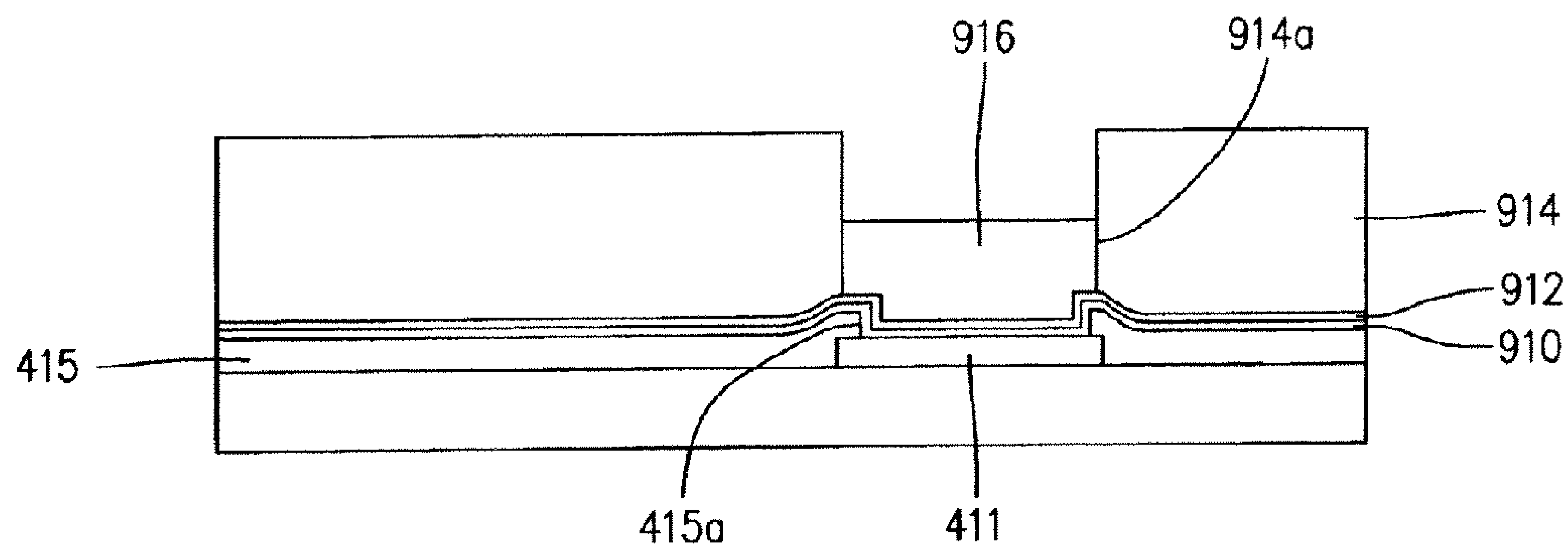


FIG. 5BA

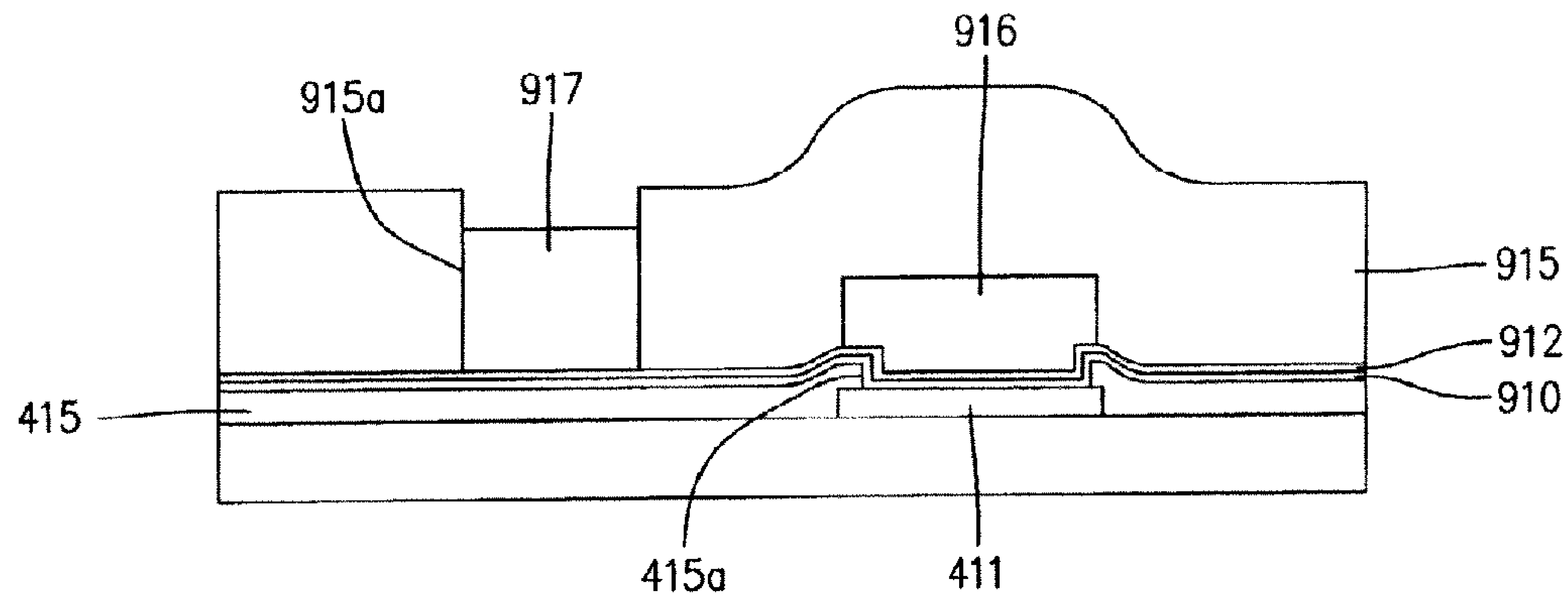


FIG. 5BB

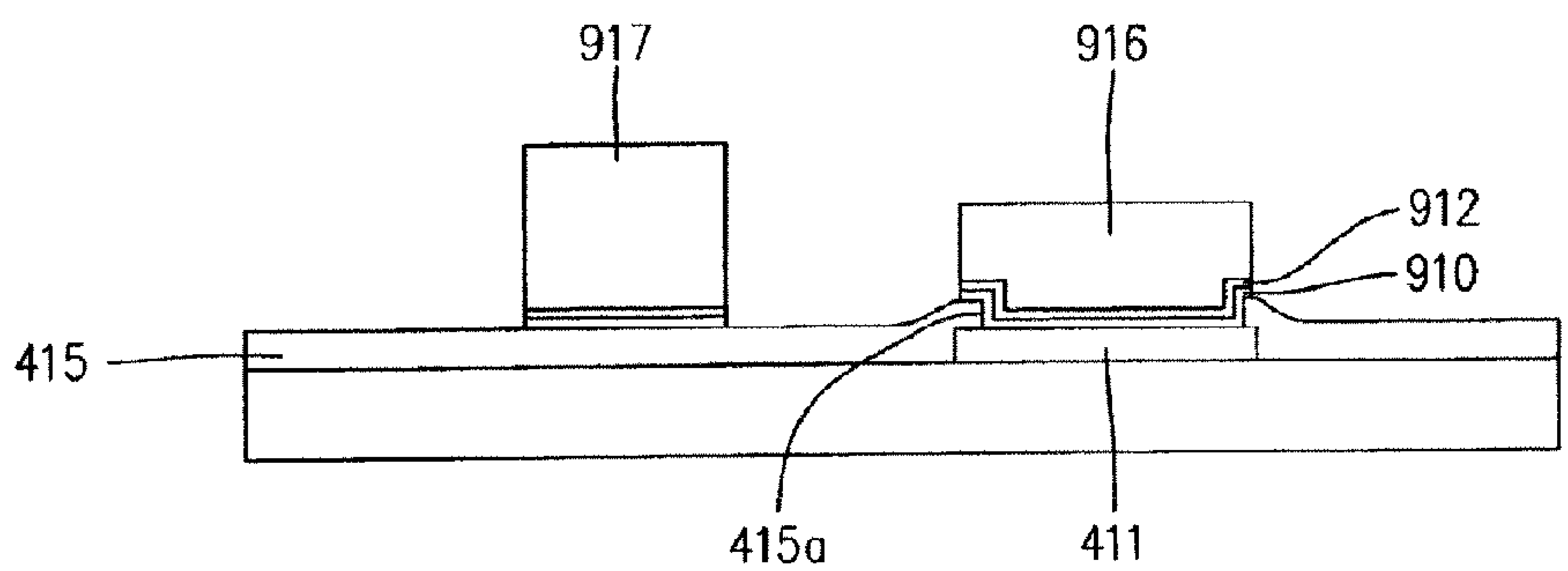


FIG. 5BC

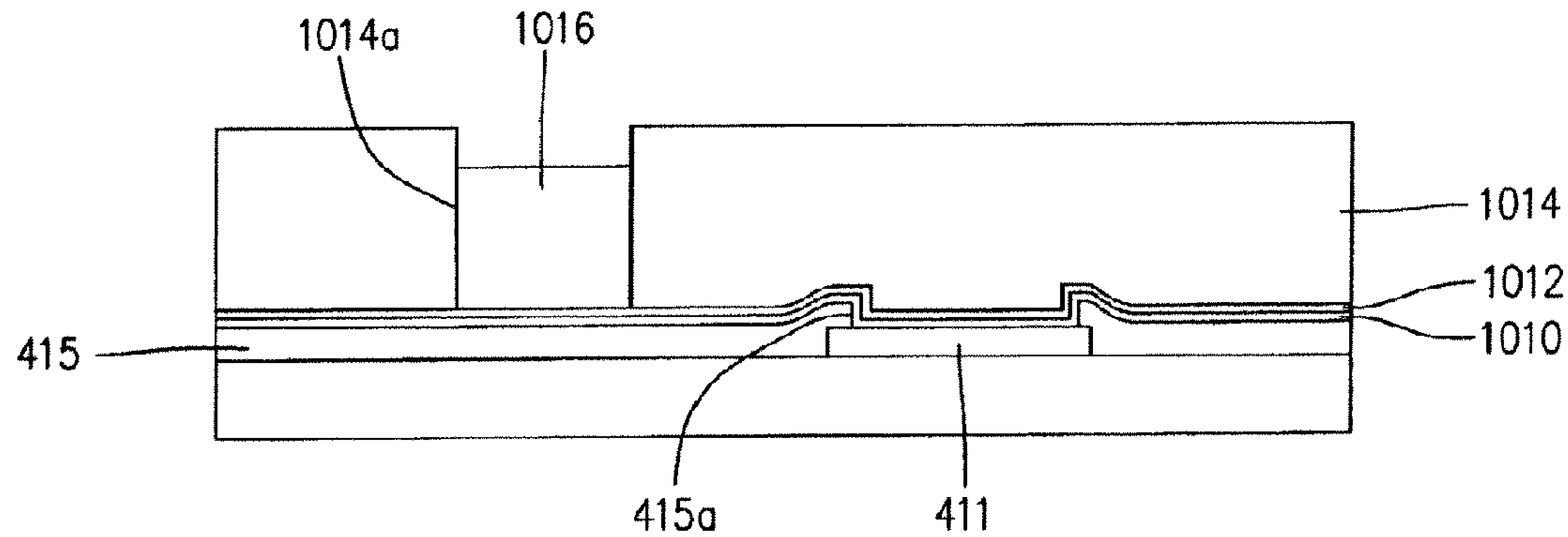


FIG. 5BD

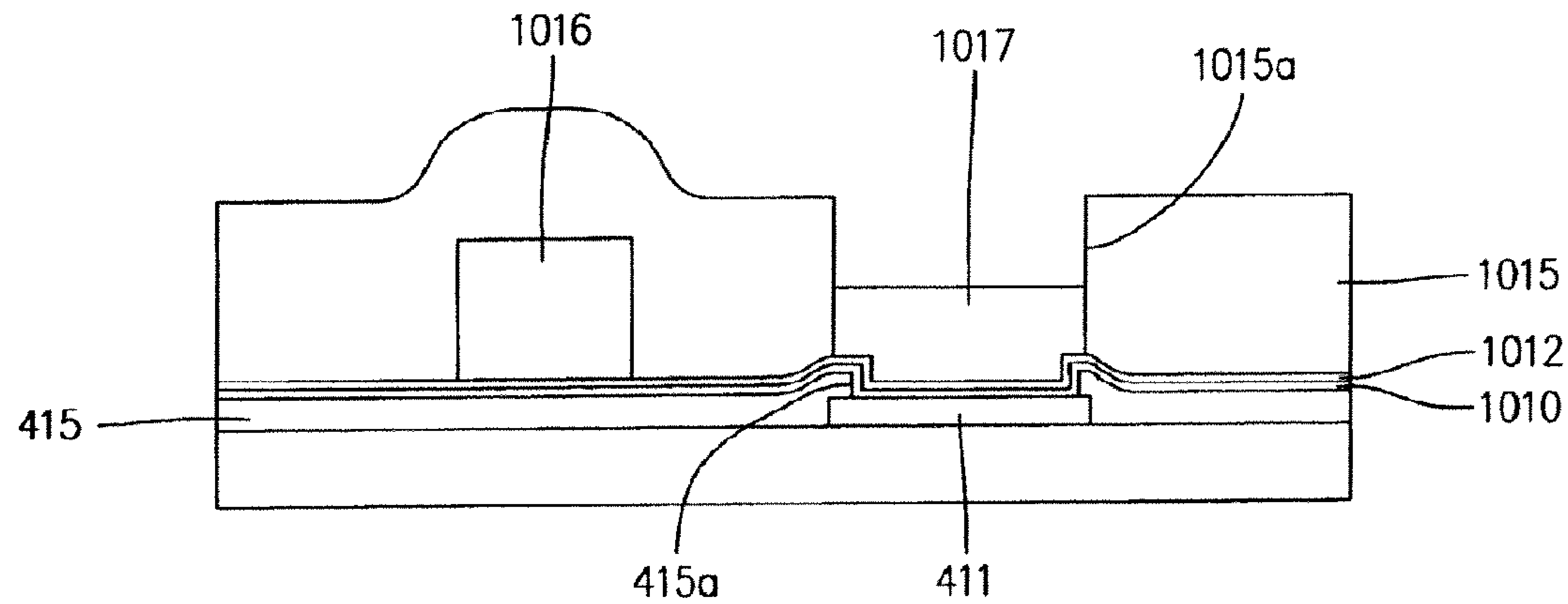


FIG. 5BE

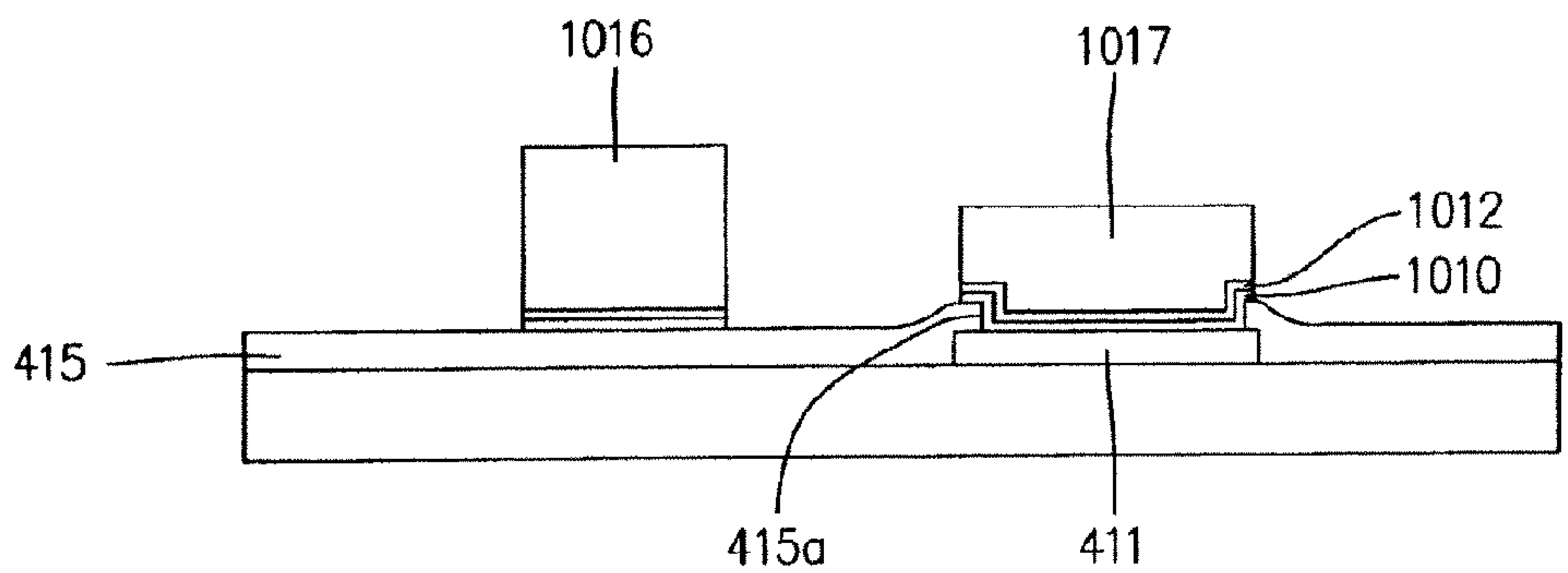


FIG. 5BF

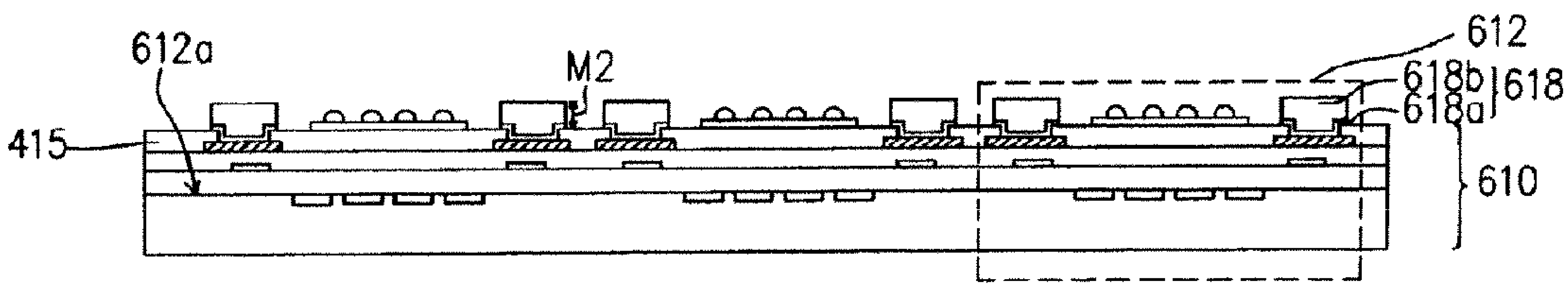


FIG.6A

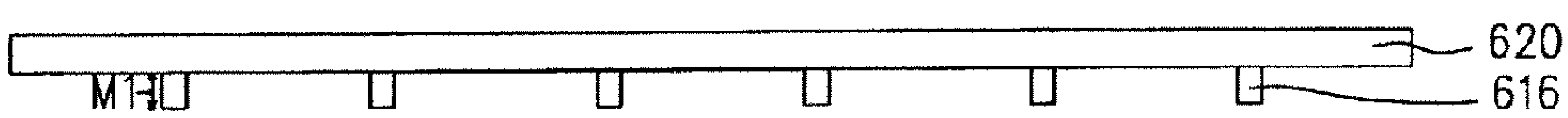


FIG.6B

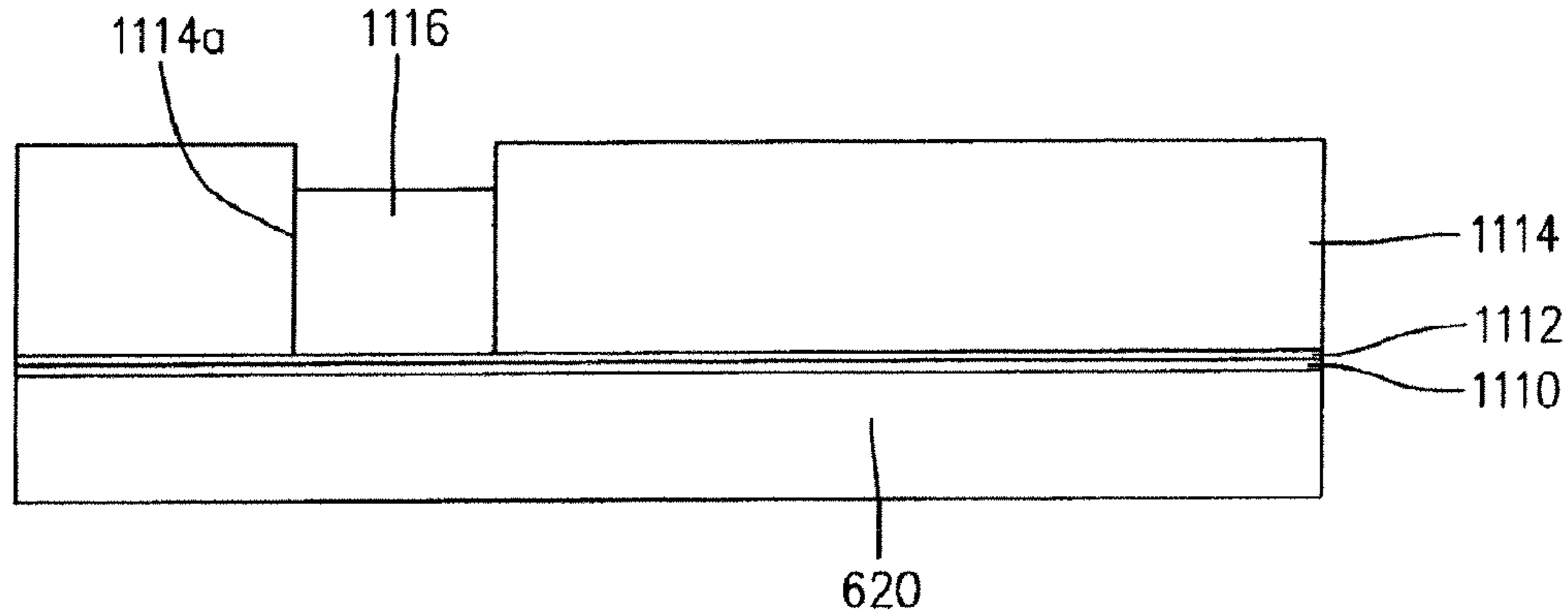


FIG. 6BA

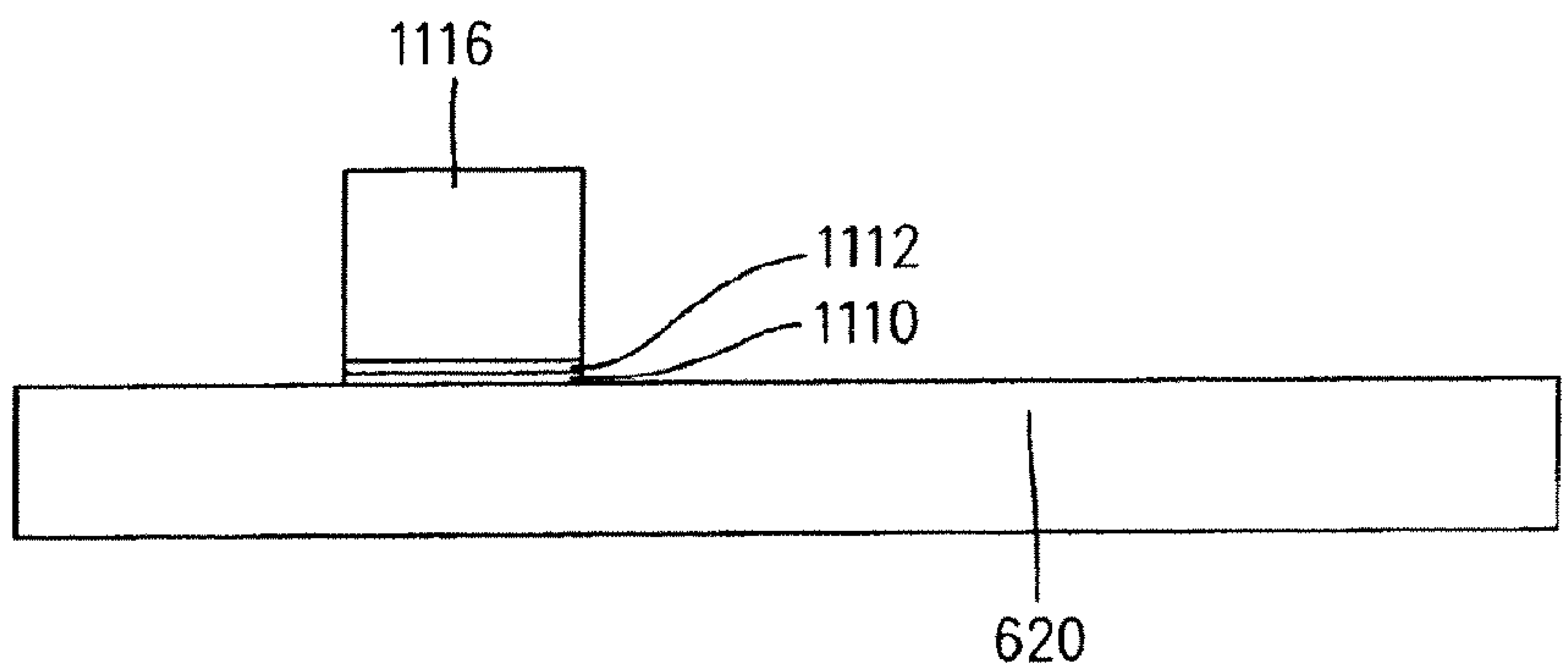
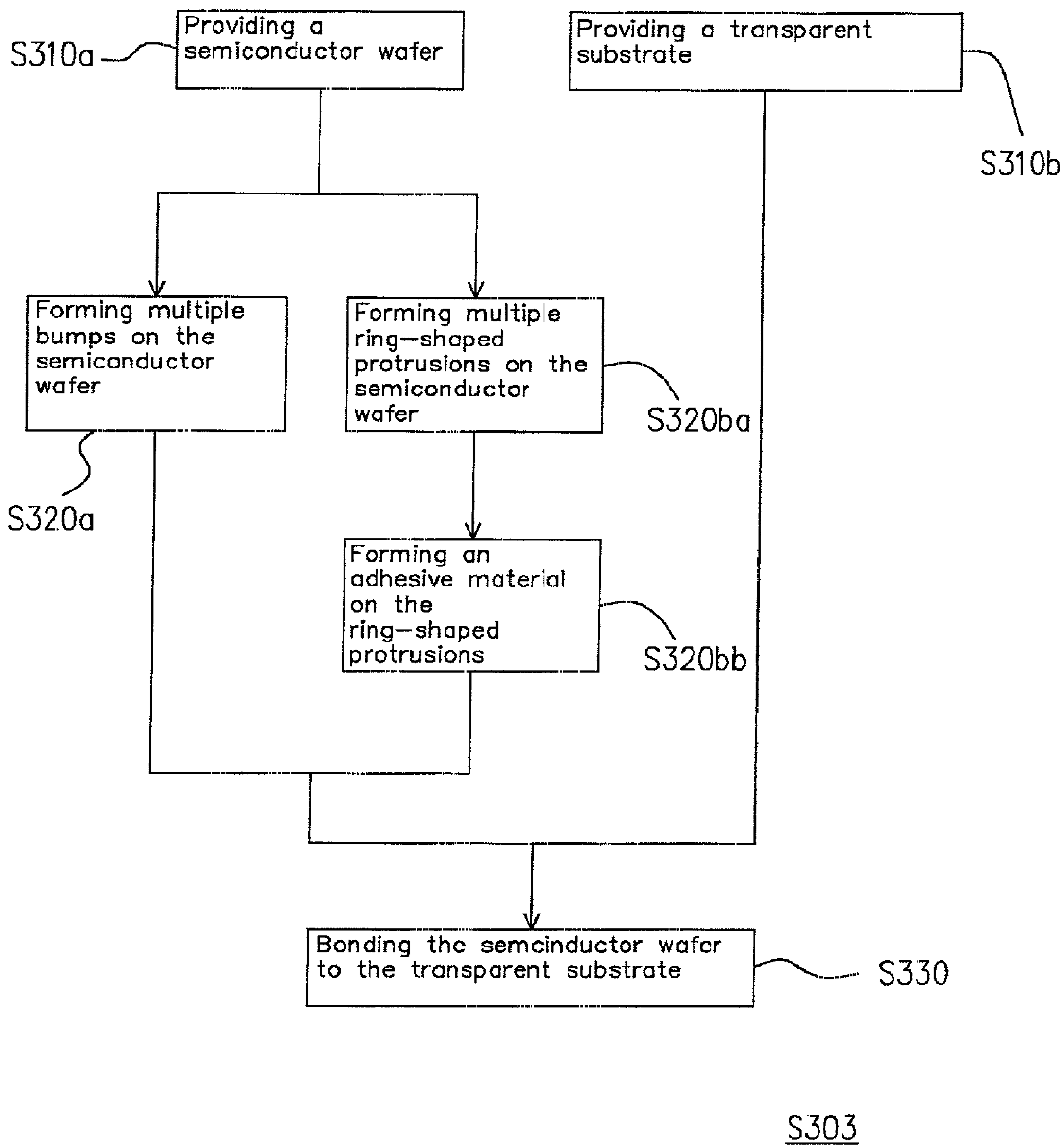


FIG. 6BB



Providing a semiconductor wafer
S310a
Providing a transparent substrate
S310b
Forming multiple bumps on the semiconductor wafer
S320a
Forming multiple ring-shaped protrusions on the semiconductor wafer
S320ba
Forming an adhesive material on the ring-shaped protrusions
S320bb
Bonding the semcinductor wafer to the transparent substrate
S330
S303

FIG.7

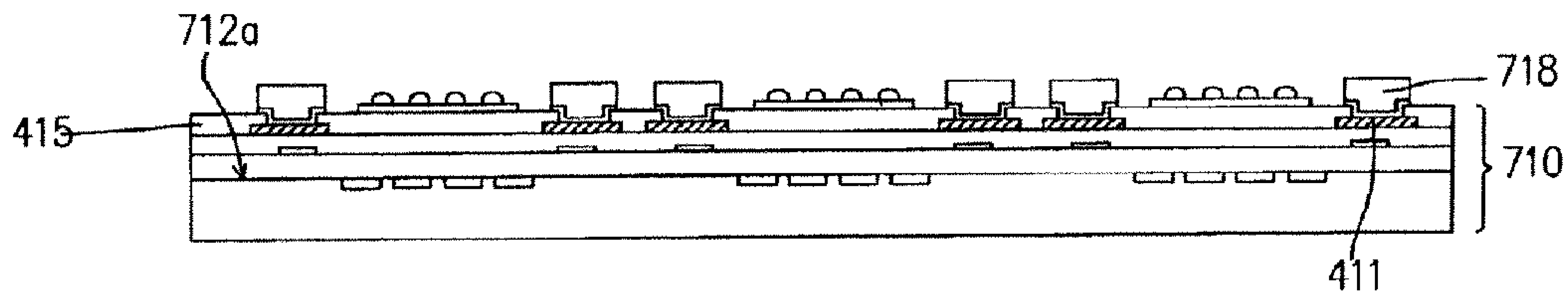


FIG.8A

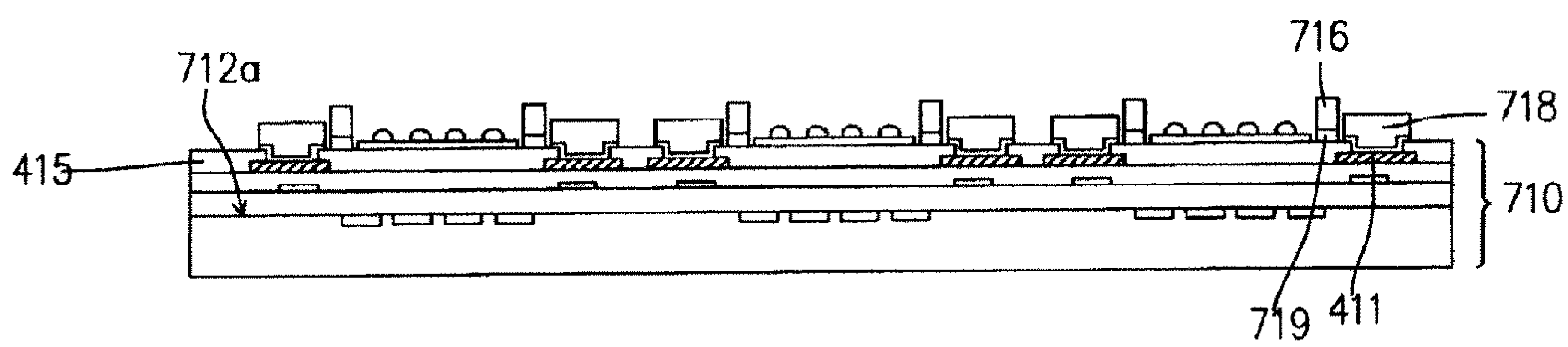


FIG.8B

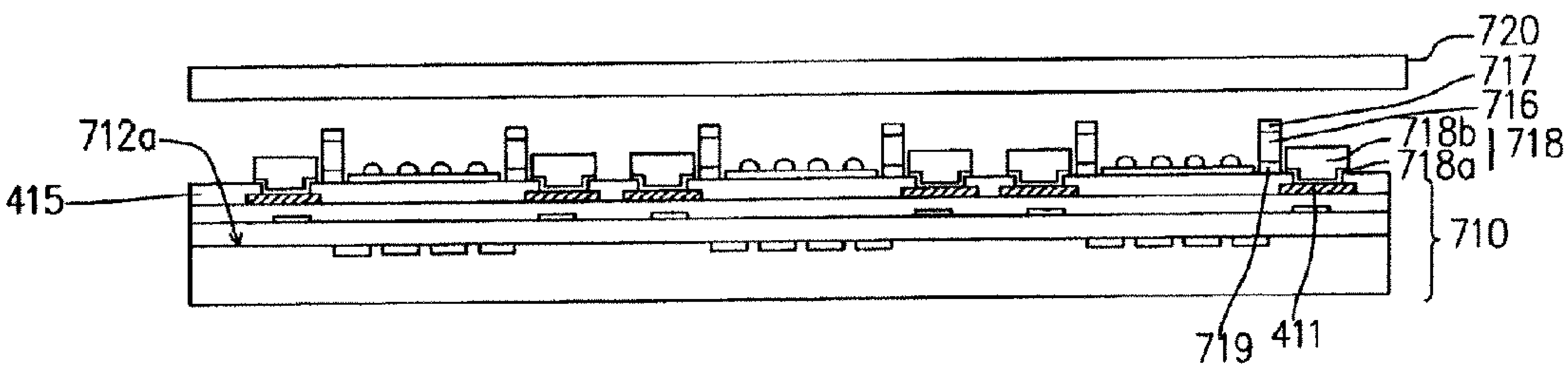


FIG.8C

CHIP PACKAGE

This application is a continuation of application Ser. No. 12/353,250, filed on Jan. 13, 2009, now U.S. Pat. No. 8,044, 475, which is a continuation of application Ser. No. 11/422, 337, filed on Jun. 6, 2006, now U.S. Pat. No. 7,495,304, which claims priority benefit of Taiwan Application Ser. No. 094118540, filed Jun. 6, 2005.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a chip package and a process for fabricating the same, and more particularly to a photo-sensitive chip package and a process for fabricating the same.

2. Description of the Prior Art

In the recent years, the electronic technology is advanced with each passing day and more new high-tech electronic products are presented to the public as well with more humanity, more convenience in the functions. However, all those products come into a trend toward lighter, thinner, and handier in order to provide more convenient and comfortable usage. Electronic packaging plays an important role in the fulfillment in communication industry and digital technology. Electronic consumer products such as PDA, Pocket PC, Portable PC and mobile phone accompanied with the digital image products such as digital camera and digital video cameras have become a trend.

The key component that makes a digital camera and a digital video camera capable of sensing images is a photo-sensitive device. The photo-sensitive device is able to sense the intensity of light and transfer electrical signals based on the light intensity for further processing. Furthermore, the packaging process is necessary to make the photo-sensitive chip connectable to outer electrical circuit through the substrate and protect the photo-sensitive chip from impurity and moisture contacting the sensitive area.

FIG. **1**A is schematically cross-sectional view of a conventional chip package. Referring to FIG. **1**A, a chip package **101** comprises a semiconductor chip **110**, a circuitry board **120**, a transparent substrate **130** and an adhesive material **140**. The semiconductor chip **110** is formed by cutting and separating a wafer (not shown). The semiconductor chip **110** has a photo-sensitive area **112**, multiple electronic components **114** and multiple connecting points. The photo-sensitive area **112** and the connecting points **116** are located on an active surface **110***a* of the semiconductor chip **110**. The connecting points **116** are distributed around the photo-sensitive area **112**. The electronic components **114**, such as MOS devices or transistors, are allocated inside the semiconductor chip **110**. In the photo-sensitive area **112** are an optical filter **12** and multiple micro-lenses **14** to filter and concentrate the light from the outside, respectively. The electronic components **114** in the photo-sensitive area **112** can sense the intensity of the light filtered and concentrated by the optical filter **12** and the micro-lenses **14** to generate electrical signals corresponding with the intensity of the light.

Referring to FIG. **1**A, the semiconductor chip **110** is mounted on the circuitry board **120**. The circuitry board **120** may comprises a hard core insulating layer, multiple polymer layers and multiple patterned metal layers. The polymer layers and patterned metal layers are formed on the top and bottom sides of the hard core insulating layer. The hard core insulating layer, such as FR-4 or FR-5, may comprise polymer and glass. The circuitry board **120** may includes multiple connecting points **122** on a top surface thereof and surrounding an area used to be joined with the semiconductor chip **110**.

After joining the semiconductor chip **110** and the circuitry board **120**, multiple wires are formed by a wirebonding process to connect the connecting points **116** of the semiconductor chip **110** to the connecting points **122** of the circuitry board **120**.

Referring to FIG. **1**A, after the semiconductor chip **110** is mounted on the circuitry board **120** and multiple wires **10** are formed by a wirebonding process to connect the connecting points **116** of the semiconductor chip **110** to the connecting points **122** of the circuitry board **120**, one of the transparent substrates **130** divided from a large plane piece of transparent material (not shown) is joined to the circuitry board **120** using the adhesive material **140**. The material of the transparent substrate **130** is glass. The adhesive material **140** is epoxy resin. The adhesive material **140** surrounds the semiconductor chip **110** and the wires **10**. The circuitry board **120**, transparent substrate **130** and adhesive material **140** construct an airtight space **150** accommodating the semiconductor chip **110**. Next, multiple solder balls **18** are formed on the bottom surface of the circuitry board **120** to form an electrical connection from the circuitry board **120** to a next-level printed circuit board (PCB, not shown). Thereafter, cutting the circuitry board **120** is performed and then multiple individual chip packages are completed.

FIG. **1**B is a schematically cross-sectional view of another conventional chip package. Referring to FIG. **1**B, the chip package **201** comprises of a semiconductor chip **201**, a flexible circuitry substrate **220**, multiple bumps **230**, a transparent substrate **240**, an adhesive material **250** and an underfill **260**. The semiconductor chip **210** has a photo-sensing function and the detail structure of the semiconductor chip **210** can refer to the structure of the above-mentioned semiconductor chip **110** in FIG. **1**A.

Referring to FIG. **1**B, the bumps **230** are formed on multiple connecting points **216** of the semiconductor chip **210**. Next, the semiconductor chip **210** is bonded to a metal layer **220***a* of the flexible circuitry substrate **220** through the bumps **230**. The flexible circuitry substrate **220** further comprises an insulating polymer layer **220***b* joined to the metal layer **220***a*. Thereafter, the underfill **260** is provided to fill the space between the semiconductor chip **210** and the flexible circuitry substrate **220** and to cover the bumps **230**. One of the transparent substrates **130** divided from a large plane piece of transparent material (not shown) is joined to the flexible circuitry substrate **120** using the adhesive material **250**, wherein the transparent substrates **240** are glass, for example. At this time, the semiconductor chip **210**, transparent substrate **240**, flexible circuitry substrate **220**, bumps **230** and underfill **260** construct an airtight space **270**. Thereafter, the flexible circuitry substrate **220** is cut to form multiple individual chip packages **201**.

It is worthy to notice that the fabrication of the package structures **101** and **201** as above-mentioned in FIGS. **1**A and **1**B is performed to attach the transparent substrate **130** or **240** onto the semiconductor chip **110** or **210** in a packaging fab. Therefore, the photo-sensitive areas of the semiconductor chips **110** and **210** will be exposed in a clean room in the packaging fab. Because the class of the clean room in the packaging fab is typically **100-100**, many tiny dust particles in the air will fall on the photo-sensitive areas **112** and **212** of the chips **110** and **210**. This affects their sensitivity.

Besides, in the prior art, such a process that the transparent substrate **130** or **240** after cut is joined piece by piece to the semiconductor chip **110** or **210** is joined to the transparent substrate **130** or **240** through the adhesive material **140** or **250** is not efficient.

SUMMARY OF THE INVENTION

Therefore, one objective of the present invention is to provide a chip package having an improved yield.

In order to reach the above objectives, the present invention provides a chip package including a bump connecting said semiconductor chip and said circuitry component, wherein the semiconductor chip has a photosensitive area used to sense light. The chip package may include a ring-shaped protrusion connecting a transparent substrate and the semiconductor chip.

Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive to the invention, as claimed. It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated as a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

FIG. **1**A is schematically cross-sectional view of a conventional chip package.

FIG. **1**B is a schematically cross-sectional view of another conventional chip package.

FIG. **2**A is a flowchart of fabricating a chip package according to the first embodiment of this invention.

FIG. **2**B is another flowchart of fabricating a chip package according to the first preferred embodiment of this invention.

FIG. **3**A is a schematically cross-sectional view including a wafer and a transparent substrate before being joined together according to the first embodiment of this invention.

FIGS. **3**AA and **3**AB are schematically cross-sectional views showing a process for forming a ring-shaped protrusion **416** and bump **418**.

FIG. **3**AC is a schematically top view showing the arrangement of the ring-shaped protrusion **416** and bumps **418**.

FIGS. 3B, 3B', and 3C-3H are schematically cross-sectional views showing a process for fabricating a semiconductor chip package according to the first embodiment of this invention.

FIG. **4**A is a flowchart of fabricating a semiconductor chip package according to the second embodiment of this invention.

FIG. **4**B is another flowchart of fabricating a semiconductor chip package according to the third embodiment of this invention.

FIGS. **5**A and **5**B are schematically cross-sectional views showing a process for fabricating a semiconductor chip package according to the second embodiment of this invention.

FIGS. **5**BA-**5**BC are schematically cross-sectional views showing a process for forming a ring-shaped protrusion **917** and bump **916**.

FIGS. **5**BD-**5**BF are schematically cross-sectional views showing a process for forming a ring-shaped protrusion **1016** and bump **1017**.

FIGS. **6**A and **6**B are schematically cross-sectional views showing a process for fabricating a semiconductor chip package according to the third embodiment of this invention.

FIGS. **6**BA-**6**BB are schematically cross-sectional views showing a process for forming multiple ring-shaped protrusions on a transparent substrate according to the third embodiment of this invention.

FIG. **7** is a flowchart of fabricating a semiconductor chip package according to the fourth embodiment of this invention.

FIGS. **8**A-**8**C are schematically cross-sectional views showing a process of fabricating a semiconductor chip package according to the fourth embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

FIG. **2**A is a flowchart of fabricating a chip package according to the first embodiment of this invention. FIG. **3**A is a schematically cross-sectional view including a wafer and a transparent substrate before being joined together according to the first embodiment of this invention. Referring to FIGS. **2**A and **3**A, the process S**300***a* for fabricating a semiconductor chip package comprises several steps as follows. First, in step S**310**, a semiconductor wafer **410** and a transparent substrate **420** are provided. The semiconductor wafer **410** comprises multiple semiconductor chips **412** each having a photosensitive area **414** on an active surface **412***a* of the semiconductor chip **412** to sense the external light. The material of the transparent substrate **420** contains, for example, glass. There are an optical filter **12** and multiple micro-lenses **14** on the photo-sensitive area **414** where the external light can be focused and filtered. The intensity of the light illuminating on the photo-sensitive area **414** can be sensed by semiconductor devices **419** to generate electrical signals corresponding to the light intensity. The semiconductor devices **419** may be CMOS light sensors, photo-sensitive P/N junctions or charge coupled devices (CCD), which is connected to sense amplifier, CMOS circuits or other integrated circuits.

Next, in step S**320**, multiple ring-shaped protrusions **416** and bumps **418** are formed over the active surface **412***a* of the semiconductor wafer **410** simultaneously. The protrusions **416** from a top view are ring shaped. In the semiconductor chip **412**, the ring-shaped protrusion **416** surrounds the photosensitive area **414** and the bumps **418** surround the ring-shaped protrusion **416**. The ring-shaped protrusions **416** and bumps **418** contain an adhesion/barrier layer **416***a* or **418***a* and a gold layer **416***b* or **418***b*, for example. For the ring-shaped protrusions **416**, the adhesion/barrier layer **416***a* is formed on a topmost insulating layer **415** of the semiconductor wafer **410**, and the gold layer **416***b* is formed on the adhesion/barrier layer **416***a*. For the bumps **418**, the adhesion/barrier layer **418***a* is formed on contact pads exposed by openings in a topmost insulating layer **415** of the semiconductor wafer **410**, and the gold layer **416***b* is formed on the adhesion/barrier layer **416***a*. The material of the adhesion/barrier layer **416***a* or **418***a* contains, for example, Ti—W alloy, titanium nitride or tantalum nitride, etc. The topmost insulating layer **415** may be a passivation layer. Multiple openings in the passivation layer **415** expose multiple bonding pads. The bonding pads **411** may contain more than 90 weight percent of aluminum. The bonding pads **411** may be aluminum-copper alloy having a thickness of between 0.1 and 1 microns, formed by a sputtering process. Alternatively, the bonding pads **411** may include a copper layer having a thickness of between 0.1 and 1 micron, formed by a sputtering, electroplating or CVD process, and an adhesion/barrier layer covering the sidewalls and the bottom of the copper layer, wherein the adhesion/barrier layer, such as tantalum nitride, tantalum, titanium nitride or titanium, may have a thickness of between 500 and 3000 angstroms.

In a first case, the passivation layer **415** can be formed by first depositing a silicon-oxide layer with a thickness of between 0.2 and 0.7 microns using a PECVD process, then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxide layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a silicon-oxide layer with a thickness of between 0.2 and 0.7 microns using a PECVD process, then depositing a silicon-oxynitride layer with a thickness of between 0.05 and 0.15 microns on the silicon-oxide layer using a PECVD process, and then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxynitride layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a silicon-oxynitride layer with a thickness of between 0.05 and 0.15 microns using a PECVD process, then depositing a silicon-oxide layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxynitride layer using a PECVD process, and then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxide layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a silicon-oxide layer with a thickness of between 0.2 and 0.5 microns using a PECVD process, then depositing a silicon-oxide layer with a thickness of between 0.5 and 1 microns on the PECVD silicon-oxide layer using a spin-coating process, then depositing a silicon-oxide layer with a thickness of between 0.2 and 0.5 microns on the spin-coated silicon-oxide layer using a PECVD process, and then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the PECVD silicon-oxide layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a silicon-oxide layer with a thickness of between 0.5 and 2 microns using a HDP-CVD process, and then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxide layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a USG layer with a thickness of between 0.2 and 3 microns, then depositing a layer of TEOS, BPSG or PSG with a thickness of between 0.5 and 3 microns on the USG layer, and then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the layer of TEOS, BPSG or PSG using a PECVD process.

In another case, the passivation layer **415** can be formed by optionally first depositing a first silicon-oxynitride layer with a thickness of between 0.05 and 0.15 microns using a PECVD process, then depositing a silicon-oxide layer with a thickness of between 0.2 and 0.7 microns optionally on the first silicon-oxynitride layer using a PECVD process, then optionally depositing a second silicon-oxynitride layer with a thickness of between 0.05 and 0.15 microns on the silicon-oxide layer using a PECVD process, then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the second silicon-oxynitride layer or on the silicon-oxide layer using a PECVD process, then optionally depositing a third silicon-oxynitride layer with a thickness of between 0.05 and 0.15 microns on the silicon-nitride layer using a PECVD process, and then depositing a silicon-oxide layer with a thickness of between 0.2 and 0.7 microns on the third silicon-oxynitride layer or on the silicon-nitride layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a first silicon-oxide layer with a thickness of between 0.2 and 0.7 microns using a PECVD process, then depositing a second silicon-oxide layer with a thickness of between 0.5 and 1 microns on the first silicon-oxide layer using a spin-coating process, then depositing a third silicon-oxide layer with a thickness of between 0.2 and 0.7 microns on the second silicon-oxide layer using a PECVD process, then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the third silicon-oxide layer using a PECVD process, and then depositing a fourth silicon-oxide layer with a thickness of between 0.2 and 0.7 microns on the silicon-nitride layer using a PECVD process.

In another case, the passivation layer **415** can be formed by first depositing a silicon-oxide layer with a thickness of between 0.5 and 2 microns using a HDP-CVD process, then depositing a silicon-nitride layer with a thickness of between 0.2 and 0.7 microns on the silicon-oxide layer using a PECVD process, and then depositing another silicon-oxide layer with a thickness of between 0.5 and 2 microns on the silicon-nitride layer using a HDP-CVD process.

FIGS. **3**AA and **3**AB are schematically cross-sectional views showing a process for forming a ring-shaped protrusion **416** and bump **418**. Referring FIGS. **3**AA and **3**AB, the ring-shaped protrusions **416** and bumps **418** can be formed by first sputtering an adhesion/barrier layer **810**, such as titanium, a titanium-tungsten alloy, chromium, titanium-nitride, tantalum, tantalum-nitride, with a thickness of between 100 and 5000 angstroms, for example, on the passivation layer **415** and the bonding pad **411** exposed by the opening **415***a* in the passivation layer **415**, then sputtering, electroless plating or electroplating a seed layer **812**, such as gold or copper, with a thickness of between 1000 angstroms and 2 microns, for example, on the adhesion/barrier layer **810**, next forming a photoresist layer **814** on the seed layer **812**, multiple bump-shaped openings **814***a* and ring-shaped openings **815***a* (from a top view) in the photoresist layer **814** exposing the seed layer **812**, then electroplating a bulk metal layer having multiple bump-shaped structure **816** and multiple loop-shaped structure **817** (from a top view), on the seed layer **812** exposed by the openings **814***a* and **814***b* in the photoresist layer **814**, then removing the photoresist layer **814**, then etching the seed layer **812** not under the bulk metal layer **816** and **817**, and then etching the adhesion/barrier layer **810** not under the bulk metal layer **816** and **817**. The bulk metal layer **816** and **817** may contain more than 95 weight percent of gold and may have a thickness of between 1 and 50 microns; in this case, the seed layer **812** is preferably gold. Alternatively, the bulk metal layer **816** and **817** may be formed by first electroplating a copper layer on the seed layer **812** exposed by the openings **815***a* and **815***b* in the photoresist layer **814**, next electroplating a nickel layer on the copper layer in the openings **815***a* and **815***b* in the photoresist layer **814**, and then electroplating a solder layer on the nickel layer in the openings **815***a* and **815***b* in the photoresist layer **814**. The copper layer contains more than 95 weight percent of copper and has a thickness of between 1 and 100 microns, and preferably between 50 and 100 microns; in this case, the seed layer **812** is preferably copper. The nickel layer contains more than 95 weight percent of nickel and has a thickness of between 1 and 100 microns, and preferably between 1 and 10 microns. The solder layer contains a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, and has a thickness of between 1 and 300 microns, and preferably between 10 and 50 microns.

FIG. **3**AC is a schematically top view showing the arrangement of the ring-shaped protrusion **416** and bumps **418**. Referring FIG. **3**AC, the bumps **418** surround the ring-shaped protrusion **416**. Each ring-shaped protrusion **416** may have four sides and an opening or gap **413** may be formed at the middle part of one or more of the four sides. The opening or gap **413** may have a least lateral transverse dimension d of between 5 and 100 microns, and preferably between 5 and 50 microns.

FIG. **3**B is a schematically cross-sectional view showing a process of fabricating a semiconductor chip according to the first embodiment of this invention. Referring to FIGS. **2**A and **3**B, in step S**325***a*, an adhesive material **417***a* with a ring-shaped pattern is deposited on the ring-shaped protrusion **416**, wherein the adhesive material **417***a* is, for example, a solder paste, an epoxy resin, polyimide, benzocyclobutene (BCB), or a material used as a solder mask layer of a printed circuit board and can be formed by screen printing. Alternatively, the top surface of the ring-shaped protrusion **416** can be dipped in an adhesive material to have the adhesive material **417***a* formed thereon. Preferably, the height of the adhesive material **417***a* plus the ring-shaped protrusions **416** is higher than the height of the bumps **418**.

Alternatively, the adhesive material **417***a* may comprise solder, such as tin-lead alloy or tin-silver alloy. In this case, the adhesive material **417***a* can be formed by screen printing a solder paste mixed with flux on the ring-shaped protrusion **416**. Alternatively, an adhesion layer with a ring-shaped pattern, such as chromium, titanium, copper, gold or nickel, having a thickness of between 3000 angstroms and 5 microns may be formed on all bottom surface of the transparent substrate **420** by sputtering or evaporating; then, patterning the adhesion layer using a photolithography and etching process to be formed with a ring shape (from a top view). Next, the adhesive material **417***a* of solder is readily bonded onto the adhesion layer formed on the transparent substrate **420**.

FIG. **2**B is another flowchart of fabricating a chip package according to the first preferred embodiment of this invention. FIG. **3**B' is a schematically cross-sectional view of the chip package process according to the first embodiment of this invention. Referring to FIGS. **2**A, **2**B and **3**B', the above-mentioned step S**325***a* can be replaced by choosing to carry out the step **325***b* of a semiconductor chip package process S**300***b* shown in FIG. **2**B. An adhesive material **417***b* can be formed on the transparent substrate **420**, wherein the height of the adhesive material **417***b* plus the ring-shaped protrusions **416** is higher than the height of the bumps **418**. The transparent substrate **420** may be made of silicon oxide, glass or transparent plastic sheet, for example. The adhesive material **417***b* is, for example, an epoxy resin, polyimide, benzocyclobutene (BCB) or a material used as a solder mask layer of a printed circuit board.

Alternatively, the adhesive material **417***b* may comprise solder, such as tin-lead alloy or tin-silver alloy. In this case, the adhesive material **417***b* can be formed by first sputtering an adhesion layer (not shown), such as titanium, a titanium-tungsten alloy, chromium, copper or nickel, can be on the transparent substrate **420**, then patterning the adhesion layer to be formed with a ring shape (from a top view) using a photolithography and etching processes, and then screen printing a solder paste with flux, having a ring shape, on the patterned adhesion layer. Using a reflow process, the ring-shaped solder paste may bond the ring-shaped protrusion **416** to the transparent substrate **420**. Alternatively, the adhesive material **417***b* can be formed by first sputtering an adhesion layer (not shown), such as titanium, a titanium-tungsten alloy, chromium, copper or nickel, can be on the transparent substrate **420**, then forming a photoresist layer on the adhesion layer, multiple ring-shaped openings in the photoresist layer exposing the adhesion layer, then electroplating a ring-shaped copper layer with a thickness of between 1 and 10 microns on the adhesion layer, next electroplating a ring-shaped nickel layer with a thickness of between 0.5 and 5 microns on the ring-shaped copper layer, next electroplating a ring-shaped solder layer, such as tin-lead alloy, tin-silver alloy or tin-silver-copper alloy, with a thickness of between 5 and 50 microns on the ring-shaped nickel layer, then removing the photoresist layer, and then removing the adhesion layer not under the solder layer. Using a reflow process, the ring-shaped solder paste may bond the ring-shaped protrusion **416** to the transparent substrate **420**. The rest steps of the chip package process S**300***b* are similar to those of the chip package process S**300***a*.

FIG. **3**C is a schematically cross-sectional view showing a process of fabricating a chip package according to the first embodiment of this invention. In step S**330**, the transparent substrate **420** is joined to the wafer **410** through the adhesive material **417**. The semiconductor chip **412**, transparent substrate **420** and ring-shaped protrusions **416** may construct multiple cells **430**. As shown in FIG. **3**AC, the opening or gap **413** connects the cell **430** and the ambient space outside the cell **430**. Alternatively, no opening or gap may be formed to connect the cell **430** and the ambient space outside the cell **430**. Therefore, external particles falling onto the photo-sensitive area **414** may be avoided.

FIGS. **3**D and **3**E are schematically cross-sectional views showing a process of fabricating a chip package according to the first embodiment of this invention. Referring to FIGS. **2**A, and **3**D, in step S**340**, the transparent substrate **420** is patterned using photolithography and etching processes, depicted as follows. First, referring to FIG. **3**D, a photoresist layer **16** is coated on the transparent substrate **420**. Next, the pattern of the photoresist layer **16** is defined using a photolithography process. Referring to FIG. **3**E, using the patterned photoresist layer **16** as an etching mask, the transparent substrate **420** is etched using an etchant, such as hydrofluoric acid, to define the pattern of the transparent substrate **420**. Afterwards, the photoresist layer **16** is removed from the transparent substrate **420**.

Alternatively, the transparent substrate **420** can be previously cut into multiple pieces with a predetermined size and then the separated pieces are joined with the ring-shaped protrusions **416**.

FIG. **3**F is a schematically cross-sectional view showing a process of fabricating a chip package according to the first embodiment of this invention. Referring to FIGS. **2**A, **28** and **3**F, in step S**350**, the semiconductor wafer **410** is segmented into multiple individual semiconductor chip packages **400** using a cutting tool (not shown).

FIG. **3**G is a schematically cross-sectional view showing a process of fabricating a chip package according to the first embodiment of this invention. Referring to FIGS. **2**A, **2**B and **3**G, in step S**360**, the bumps **418** of the individual semiconductor chip package **400** are bonded to a flexible tape **30** in an F**1** direction. The flexible tape **30** comprises metal traces **30***a* and a polymer layer **30***b*, wherein the metal traces **30***a* is formed on the polymer layer **30***b*. An opening **32** through the flexible tape **30** exposes the photo-sensitive area **414** of the semiconductor chip package **400**. Thus, light can pass through the opening **32** and can be sensed by the photo-sensitive area **414** of the semiconductor chip package **400**. A signal can be transmitted between the semiconductor devices **419** of the semiconductor chip package **400** and an external circuitry, such as printed circuit board, through the flexible tape **30**.

FIG. **3**H is a schematically cross-sectional view showing a process of a chip package process according to the first embodiment of this invention. Referring to FIGS. **2**A, **2**B and **3**H, in step S**370**, an underfill **40**, such as polymer, is provided to cover the bumps **418** and the metal traces **30***a* of the flexible circuit substrate **30**.

Referring to FIGS. **2**A, **2**B and **3**C, it is worthy to notice that, the steps prior to above-mentioned step S**330**, that is, the steps for constructing the airtight space **430** enclosed by the semiconductor chip **412**, transparent substrate **420** and ring-shaped protrusion **416** can be carried out in a high class clean room in a wafer fab. This can efficiently reduce particles existing in the airtight space **430** and increase the sensitivity of the photo-sensitive area **414**. Therefore, the yield rate of fabricating the semiconductor chip package **400** can be improved. As to the step after the above-mentioned step S**340**, that is, the step of patterning the transparent substrate **420**, cutting the semiconductor wafer **410** and bonding the tape **30** to the bumps **418** can be carried out in a low class clean room in a packaging fab.

In the steps S**300***a* and S**300***b* for fabricating the semiconductor chip packages, the semiconductor wafer **410** and transparent substrate **420** are first joined and the transparent substrate **420** is then patterned using photolithography and etching processes, whereby the duration of manufacturing the semiconductor chip package **400** can be efficiently retrenched.

Second Embodiment

FIG. **4**A is a flowchart of fabricating a semiconductor chip according to the second embodiment of this invention. FIG. **5**A is a schematically cross-sectional view showing a process of fabricating a semiconductor chip according to the second embodiment of this invention. Referring to FIGS. **4**A and **5**A, the process S**301** of forming a semiconductor chip package comprises the following steps. First, in step S**310***a*, a semiconductor wafer **510** is provided and has a similar structure to the above-mentioned semiconductor wafer **410** in the first embodiment. Then, in step S**320***a*, multiple bumps **518** are formed over the active surface **512***a* of the semiconductor wafer **510**. Each of the bumps **518** comprises an adhesion/barrier layer **518***a* and a gold layer **518***b*, wherein the gold layer **518***b* is on the adhesion/barrier layer **518***a*. The material of the adhesion/barrier layer **518***a* is, for example, a Ti/W alloy, titanium, titanium nitride or tantalum nitride, etc. The gold layer **518***b* may have a thickness of between 10 and 50 microns, for example.

The bumps **518** can be formed by first sputtering an adhesion/barrier layer, such as titanium, a titanium-tungsten alloy, chromium, titanium-nitride, tantalum, tantalum-nitride, with a thickness of between 100 and 5000 angstroms, for example, on the passivation layer **415** and the bonding pad **411** exposed by the opening **415***a* in the passivation layer **415**, then sputtering, electroless plating or electroplating a seed layer, such as gold or copper, with a thickness of between 1000 angstroms and 2 microns, for example, on the adhesion/barrier layer, next forming a photoresist layer on the seed layer, multiple openings in the photoresist layer exposing the seed layer, then electroplating a bulk metal layer on the seed layer exposed by the openings in the photoresist layer, then removing the photoresist layer, then etching the seed layer not under the bulk metal layer, and then etching the adhesion/barrier layer not under the bulk metal layer. The bulk metal layer may contain more than 95 weight percent of gold and may have a thickness of between 1 and 50 microns; in this case, the seed layer is preferably gold. Alternatively, the bulk metal layer may be formed by first electroplating a copper layer on the seed layer exposed by the openings in the photoresist layer, next electroplating a nickel layer on the copper layer in the openings in the photoresist layer, and then electroplating a solder layer on the nickel layer in the openings in the photoresist layer. The copper layer contains more than 95 weight percent of copper and has a thickness of between 1 and 100 microns, and preferably between 50 and 100 microns; in this case, the seed layer is preferably copper. The nickel layer contains more than 95 weight percent of nickel and has a thickness of between 1 and 100 microns, and preferably between 1 and 10 microns. The solder layer contains a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, and has a thickness of between 1 and 300 microns, and preferably between 10 and 50 microns.

FIG. **5**B is a schematically cross-sectional view showing a process for fabricating a semiconductor chip according to the second embodiment of this invention. Referring to FIGS. **4**A and **5**B, in step S**320***b*, after forming the bumps **518**, multiple ring-shaped protrusions **516** are formed over the active surface **512***a* of the wafer **510**, wherein the height H**1** of the ring-shaped protrusion **516** is higher than the height H**2** of the bumps **518**. The principal material of the ring-shaped protrusion **516** is, for example, an adhesive polymer, epoxy resin, polyimide, benzocyclobutene (BCB), or the material used for a solder mask layer of a printed circuit board. Alternatively, the step S**320***b* can be followed by the step **320***a*. After forming the bumps **518** and ring-shaped protrusion **516**, in step S**310***b*, the transparent substrate **520** is provided and in step S**330**, the ring-shaped protrusion **516** on the semiconductor wafer **510** is joined with the transparent substrate **520**. The transparent substrate **520** may be made of silicon oxide, glass or transparent plastic sheet, for example. The bumps **518** may have a thickness of between 5 and 50 microns; the ring-shaped protrusion **516** may have a thickness of between 10 and 500 microns. After forming the bumps **518** and ring-shaped protrusion **516** on the semiconductor wafer **510**, the semiconductor wafer **510** and the transparent substrate **520** can be joined with the ring-shaped protrusion **516** bonded to the transparent substrate **520**. As to the rest steps, they can refer to the above-mentioned process S**300***a* of fabricating the semiconductor chip package.

Alternatively, the bumps **518** and ring-shaped protrusion **516** can be formed using other ways, as shown in FIGS. **5**BA through **5**BC. The bumps **518** and ring-shaped protrusion **516** can be formed by first, referring to FIG. **5**BA, sputtering an adhesion/barrier layer **910**, such as titanium, titanium-tungsten alloy, tantalum nitride, tantalum, titanium nitride, chromium, on the passivation layer **415** and the bonding pads **411** exposed by the openings **415***a* in the passivation layer **415**, then sputtering, electroless plating or electroplating a seed layer **912**, such as copper, gold, silver, palladium or platinum, on the adhesion/barrier layer **910**, next forming a photoresist layer **914** on the seed layer **912**, multiple openings **914***a* for the bumps **518** in the photoresist layer **914** exposing the seed layer **912**, then electroplating a bulk metal layer **916** for the bumps **518** on the seed layer **912** exposed by the openings **914***a* in the photoresist layer **914**, then removing the photoresist layer **914**, next, referring to FIG. **5**BB, forming another photoresist layer **915** on the seed layer **912** and on the bulk metal layer **916**, multiple ring-shaped openings **915***a* in the photoresist layer **915** exposing the seed layer **912** then electroplating a bulk metal layer **917** for the ring-shaped protrusions **516** on the seed layer **912** exposed by the openings **915***a* in the photoresist layer **915**, then removing the photoresist layer **915**, and then removing the seed layer **912** not under the bulk metal layers **916** and **917** respectively for the bumps **518** and for the ring-shaped protrusions **516**, next removing the adhesion/barrier layer **910** not under the bulk metal layers **916** and **917** respectively for the bumps **518** and for the ring-shaped protrusions **516**, as shown in FIG. **5**BC.

The bulk metal layer **916** may have a thickness different from that of the bulk metal layer **917**. Preferably, the bulk metal layer **917** for the ring-shaped protrusions **516** is higher than the bulk metal layer **916** for the bumps **518**.

As to a first case, both or either of the bulk metal layers **916** and/or **917** may contain more than 95 weight percent of gold and may have a thickness of between 1 and 50 microns, and preferably between 5 and 30 microns. As to a second case, both or either of the bulk metal layers **916** and/or **917** may be formed by first electroplating a copper layer on the seed layer **912** exposed by the openings **914***a* and/or **915***a* in the photoresist layer **914** and/or **915**, next electroplating a nickel layer on the copper layer in the openings **914***a* and/or **915***a* in the photoresist layer **914** and/or **915**, and then electroplating a solder layer on the nickel layer in the openings **914***a* and/or **915***a* in the photoresist layer **914** and/or **915**. The copper layer contains more than 95 weight percent of copper and has a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. The nickel layer contains more than 95 weight percent of nickel and has a thickness of between 1 and 100 microns, and preferably between 1 and 10 microns. The solder layer contains a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, and has a thickness of between 1 and 300 microns, and preferably between 10 and 50 microns. Alternatively, the copper layer can be substituted with electroplated gold layer containing more than 95 weight percent of gold and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated silver layer containing more than 95 weight percent of silver and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated platinum layer containing more than 95 weight percent of platinum and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated palladium layer containing more than 95 weight percent of palladium and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns.

Both of the bumps **518** and ring-shaped protrusion **516** can be formed following the first case; alternatively, both of the bumps **518** and ring-shaped protrusion **516** can be formed following the second case; alternatively, the bumps **518** can be formed following the first case, but the ring-shaped protrusion **516** can be formed following the second case; alternatively, the bumps **518** can be formed following the second case, but the ring-shaped protrusion **516** can be formed following the first case. Using a heating process, the ring-shaped protrusion **516** formed following the first case can be bonded to a ring-shaped solder paste or an adhesive polymer, such as epoxy, (not shown) previously screen printed on the transparent substrate **520**, as shown in FIG. **5**B. Using a heating process, the ring-shaped protrusion **516** formed following the second case can be bonded to a ring-shaped pad (not shown), such as gold or copper, previously sputtered on the transparent substrate **520** or bonded to a ring-shaped solder paste or lump (not shown) previously screen printed or electroplated on the transparent substrate **520**, as shown in FIG. **5**B.

Alternatively, the bumps **518** and ring-shaped protrusion **516** can be formed using other ways, as shown in FIGS. **5**BD through **5**BF. The bumps **518** and ring-shaped protrusion **516** can be formed by first, referring to FIG. **5**BD, sputtering an adhesion/barrier layer **1010**, such as titanium, titanium-tungsten alloy, tantalum nitride, tantalum, titanium nitride, chromium, on the passivation layer **415** and the bonding pads **411** exposed by the openings **415***a* in the passivation layer **415**, then sputtering, electroless plating or electroplating a seed layer **1012**, such as copper, gold, silver, palladium or platinum, on the adhesion/barrier layer **1010**, next forming a photoresist layer **1014** on the seed layer **1012**, multiple openings **1014***a* for the ring-shaped protrusions **516** in the photoresist layer **1014** exposing the seed layer **1012**, then electroplating a bulk metal layer **1016** for the ring-shaped protrusions **516** on the seed layer **1012** exposed by the openings **1014***a* in the photoresist layer **1014**, then removing the photoresist layer **1014**, next, referring to FIG. **5**BE, forming another photoresist layer **1015** on the seed layer **1012** and on the bulk metal layer **1016**, multiple ring-shaped openings **1015***a* in the photoresist layer **1015** exposing the seed layer **1012**, then electroplating a bulk metal layer **1017** for the bumps **518** on the seed layer **1012** exposed by the openings **1015***a* in the photoresist layer **1015**, then removing the photoresist layer **1015**, and then removing the seed layer **1012** not under the bulk metal layers **1016** and **1017** respectively for the ring-shaped protrusions **516** and for the bumps **518**, next removing the adhesion/barrier layer **1010** not under the bulk metal layers **1016** and **1017** respectively for the ring-shaped protrusions **516** and for the bumps **518**, as shown in FIG. **5**BF.

The bulk metal layer **1016** may have a thickness different from that of the bulk metal layer **1017**. Preferably, the bulk metal layer **1016** for the ring-shaped protrusions **516** is higher than the bulk metal layer **1017** for the bumps **518**.

As to a first case, both or either of the bulk metal layers **1016** and/or **1017** may contain more than 95 weight percent of gold and may have a thickness of between 1 and 50 microns, and preferably between 5 and 30 microns. As to a second case, both or either of the bulk metal layers **1016** and/or **1017** may be formed by first electroplating a copper layer on the seed layer **1012** exposed by the openings **1014***a* and/or **1015***a* in the photoresist layer **1014** and/or **1015**, next electroplating a nickel layer on the copper layer in the openings **1014***a* and/or **1015***a* in the photoresist layer **1014** and/or **1015**, and then electroplating a solder layer on the nickel layer in the openings **1014***a* and/or **1015***a* in the photoresist layer **1014** and/or **1015**. The copper layer contains more than 95 weight percent of copper and has a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. The nickel layer contains more than 95 weight percent of nickel and has a thickness of between 1 and 100 microns, and preferably between 1 and 10 microns. The solder layer contains a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, and has a thickness of between 1 and 300 microns, and preferably between 10 and 50 microns. Alternatively, the copper layer can be substituted with electroplated gold layer containing more than 95 weight percent of gold and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated silver layer containing more than 95 weight percent of silver and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated platinum layer containing more than 95 weight percent of platinum and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns. Alternatively, the copper layer can be substituted with electroplated palladium layer containing more than 95 weight percent of palladium and having a thickness of between 5 and 100 microns, and preferably between 5 and 50 microns.

Both of the bumps **518** and ring-shaped protrusion **516** can be formed following the first case; alternatively, both of the bumps **518** and ring-shaped protrusion **516** can be formed following the second case; alternatively, the bumps **518** can be formed following the first case, but the ring-shaped protrusion **516** can be formed following the second case; alternatively, the bumps **518** can be formed following the second case, but the ring-shaped protrusion **516** can be formed following the first case. Using a heating process, the ring-shaped protrusion **516** formed following the first case can be bonded to a ring-shaped solder paste or an adhesive polymer, such as epoxy, (not shown) previously screen printed on the transparent substrate **520**, as shown in FIG. **5**B. Using a reflow process, the ring-shaped protrusion **516** formed following the second case can be bonded to a ring-shaped pad (not shown), such as gold or copper, previously sputtered on the transparent substrate **520** or bonded to a ring-shaped solder paste or lump (not shown) previously screen printed or electroplated on the transparent substrate **520**, as shown in FIG. **5**B.

Third Embodiment

FIG. **4**B is a flowchart S**302** of fabricating a semiconductor chip package according to the third embodiment of this invention. FIGS. **6**A and **6**B are schematically cross-sectional views showing a process for fabricating a semiconductor chip package according to the third embodiment of this invention. Referring to FIG. **4**B and **6**A, in step S**320***a*, multiple bumps **618** are formed over the active surface **612***a* of the semiconductor wafer **610**. The detail of the bumps **618** can refer to the bumps **418** or **518** described in the first or second embodiment of this invention. Referring to FIGS. **4**B, **6**A and **6**B, in step S**320***c*, multiple protrusions **616** are formed on a bottom surface of the transparent substrate **620**, wherein the protrusions **616** are ring shaped (from a bottom view), for example. The height M1 of the ring-shaped protrusions **616** is higher than the height M2 of the bumps **618**. The transparent substrate **620** may be made of silicon oxide, glass or transparent plastic sheet, for example. The ring-shaped protrusion **616** is, for example, an adhesive polymer, epoxy resin, polyimide, benzocyclobutene (BCB), or a material used as a solder mask layer of a printed circuit board and can be formed by screen printing.

FIGS. **6**BA-**6**BB are schematically cross-sectional views showing a process for forming ring-shaped protrusions on a transparent substrate according to the third embodiment. The transparent substrate **620** may be silicon oxide, transparent polymer material or glass. Alternatively, the ring-shaped protrusion **616** can be formed by, referring to FIG. **6**BA, sputtering an adhesion/barrier layer **1110**, such as a titanium-tungsten alloy, titanium, titanium nitride, tantalum nitride, or tantalum, on the transparent substrate **620**, then sputtering, electroless plating or electroplating a seed layer **1112**, such as gold or copper, on the adhesion/barrier layer **1110**, next forming a photoresist layer **1114** on the seed layer **1112**, multiple ring-shaped openings **1114***a* in the photoresist layer **1114** exposing the seed layer **1112**, then electroplating a bulk metal layer **1116** with a thickness of between 10-200 microns on the seed layer **1112** exposed by the ring-shaped openings **1114***a* in the photoresist layer **1114**, then, referring to FIG. **6**BB, removing the photoresist layer **1114**, next removing the seed layer **1112** not under the bulk metal layer **1116**, and next removing the adhesion/barrier layer **1110** not under the bulk metal layer **1116**.

As to a first case, the bulk metal layer **1116** may contain more than 95 weight percent of gold and may have a thickness of between 1 and 50 microns. Using a reflow process, the ring-shaped protrusion **616** formed following the first case can be bonded to a ring-shaped solder paste or an adhesive polymer, such as epoxy, previously screen printed on the passivation layer **415**. As to a second case, the bulk metal layer **1116** may be formed by first electroplating a copper layer on the seed layer **1112** exposed by the openings **1114***a* in the photoresist layer **1114**, next electroplating a nickel layer on the copper layer in the opening **1114***a* in the photoresist layer **1114**, and then electroplating a solder layer on the nickel layer in the opening **1114***a* in the photoresist layer **1114**. The copper layer contains more than 95 weight percent of copper and has a thickness of between 1 and 100 microns, and preferably between 50 and 100 microns. The nickel layer contains more than 95 weight percent of nickel and has a thickness of between 1 and 100 microns, and preferably between 1 and 10 microns. The solder layer contains a tin-lead alloy, a tin-silver alloy or a tin-silver-copper alloy, and has a thickness of between 1 and 300 microns, and preferably between 10 and 50 microns. Using a reflow process, the ring-shaped protrusion **616** formed following the second case can be bonded to a ring-shaped pad (not shown), such as gold or copper, previously sputtered on the passivation layer **415** or bonded to a ring-shaped solder paste or lump (not shown) previously screen printed or electroplated on the passivation layer **415**.

After forming the bumps **618** on the semiconductor wafer **610** and forming the ring-shaped protrusion **616** on the transparent substrate **620**, the semiconductor wafer **610** and the transparent substrate **620** can be joined with the ring-shaped protrusion **616** bonded to the semiconductor wafer **610** using a reflow process. As to the rest steps, they can refer to the above-mentioned process S**300***a* of fabricating the semiconductor chip package.

Alternatively, the ring-shaped protrusion **616**, such plastic, rubber, copper, aluminum or gold, can be preformed. The preformed ring-shaped protrusion **616** can be bonded to the transparent substrate **620** using a first adhesive material, such as epoxy. When the transparent substrate **620** is bonded to the semiconductor wafer **610**, the bottom surface of the ring-shaped protrusion **616** can be dipped in a second adhesive material (not shown), such as epoxy or solder paste, to have the second adhesive material formed thereon. Using a heating process, the second adhesive material bond the ring-shaped protrusion **616** to the passivation layer **415** or to a metal pad (not shown) previously aimed on the passivation layer **415**.

Alternatively, before the preformed ring-shaped protrusion **616** is bonded to the transparent substrate **620**, an adhesive material, such as solder material or thermoplastic polymer, is formed on the bottom surface of the ring-shaped protrusion **616**. Using a heating process, the adhesive material bond the ring-shaped protrusion **616** to the passivation layer **415** or to a metal pad (not shown) previously formed on the passivation layer **415**.

Fourth Embodiment

FIG. **7** is a flowchart of fabricating a semiconductor chip package according to the fourth embodiment of this invention. FIGS. **8**A-**8**C are schematically cross-sectional views showing a process of fabricating a semiconductor chip package according to the fourth embodiment of this invention. Referring to FIGS. **7** and **8**A, the method S**303** of fabricating a semiconductor chip package comprises several steps as follows. First, in step S**310***a*, a semiconductor wafer **710** is provided and can be referred to as the semiconductor wafer **410** mentioned in the first embodiment. Next, in step S**320***a*, multiple bumps **718** are formed over the active surface **712***a* of the semiconductor wafer **710**.

Referring to FIG. **8**B, in step S**320***ba*, multiple non-adhesive ring-shaped protrusions **716**, such as polymer, plastic, rubber, glass or metal, are preformed. After forming the bumps **718** on the bonding pads **411** exposed by the openings **411** in the passivation layer **415**, as shown in FIG. **8**A, the preformed ring-shaped protrusions **716** can be attached to the passivation layer **415** of the wafer **710** using an adhesive material **719** with a ring-shaped pattern, such as epoxy, polyimide or benzocyclobuteme (BCB), as shown in FIG. **8**B. Preferably, the height of the preformed ring-shaped protrusions **716** plus the adhesive material **719** is greater than the height of the bumps **718**. Thereafter, the top surface of the ring-shaped protrusions **716** may be dipped in an adhesive material **717**, such as epoxy polyimide, benzocyclobuteme (BCB) or solder paste, to have the adhesive material **717** with a ring-shaped pattern formed on the top surface of the ring-shaped protrusions **716**, as shown in FIG. **8**C. Next, the ring-shaped protrusions **716** can be joined with the transparent substrate **720**, such as silicon oxide, glass or transparent plastic sheet, using the adhesive material **713**. Alternatively, the steps S**320***ba* and S**320***bb* can be followed by the step **320***a*. Alternatively, the step S**320***ba* can be followed by the step **320***a* followed by the step S**320***bb*.

In another case, the adhesive material **717**, such as thermoplastic polymer material or solder material, can be previously formed on the top surface of the ring-shaped protrusions **716**, and then the bottom surface of the ring-shaped protrusions **716** is attached to the passivation layer **415** of the semiconductor wafer using the adhesive material **719**. Therefore, the step S**320***bb* can be followed by the step S**320***ba*. In combination with the step S**320***a* for forming the bumps, the step S**320***a* can be followed by the step S**320***bb* followed by the step S**320***ba*; alternatively, the step S**320***a* can be performed after the step S**320***ba* following the step S**320***bb* is performed.

CONCLUSION

The steps for constructing the airtight space enclosed by a semiconductor chip, transparent substrate and ring-shaped protrusion can be carried out in a high class clean room in a wafer fab. This can efficiently reduce particles existing in the airtight space and increase the sensitivity of the photo-sensitive area. Therefore, the yield rate of fabricating the semiconductor chip package can be improved. After forming the airtight space, the steps of patterning the transparent substrate, cutting the semiconductor wafer and bonding the tape to the bumps can be carried out in a low class clean room in a packaging fab. Besides, in the above embodiments, the semiconductor wafer and transparent substrate are first joined and the transparent substrate is then patterned using photolithography and etching processes, whereby the duration of manufacturing the semiconductor chip package can be efficiently retrenched.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. Therefore, the protection area of the present invention depends on the claims attached in the patent.

What is claimed is:

1. A circuit component comprising:

a semiconductor chip comprising multiple transistors, a passivation layer over said multiple transistors, wherein said passivation layer comprises a nitride layer, and a metal pad having a contact point at a bottom of an opening in said passivation layer, wherein said opening is over said contact point;

a flexible substrate;

a first metal bump between said contact point and a metal trace of said flexible substrate, wherein said first metal bump is connected to said contact point through said opening, wherein said metal trace of said flexible substrate is connected to said contact point through said first metal bump, wherein said first metal bump comprises a first copper layer having a thickness between 5 and 50 micrometers;

a substrate component comprising a glass substrate; and

a polymer over said flexible substrate, wherein said polymer joins said metal trace and joins said substrate component.

2. The circuit component of claim **1** further comprising a second metal bump joining said substrate component, wherein said second metal bump comprises a gold layer having a thickness between 1000 angstroms and 2 micrometers.

3. The circuit component of claim **1** further comprising a second metal bump joining said substrate component, wherein said second metal bump comprises a gold layer having a thickness between 1 and 50 micrometers.

4. The circuit component of claim **1** further comprising a second metal bump joining said substrate component, wherein said second metal bump comprises a second copper layer having a thickness between 5 and 50 micrometers.

5. The circuit component of claim **1** further comprising a second metal bump joining said substrate component, wherein said second metal bump comprises a nickel layer having a thickness between 1 and 100 micrometers.

6. The circuit component of claim **1**, wherein said first metal bump further comprises a titanium-containing layer under said first copper layer.

7. The circuit component of claim **1**, wherein said first metal bump further comprises a tin-containing solder at a top of said metal bump.

8. The circuit component of claim **7**, wherein said tin-containing solder comprises silver.

9. The circuit component of claim **1**, wherein said first metal bump further comprises a nickel-containing layer on said first copper layer.

10. The circuit component of claim **9**, wherein said nickel-containing layer has a thickness between 1 and 100 micrometers.

11. A circuit component comprising:

a semiconductor chip comprising multiple transistors, a passivation layer over said multiple transistors, wherein said passivation layer comprises a nitride layer, and a metal pad having a contact point at a bottom of an opening in said passivation layer, wherein said opening is over said contact point;

a substrate component comprising a glass substrate over said semiconductor chip;

a first metal bump between said contact point and said glass substrate, wherein said first metal bump is connected to said contact point through said opening, wherein said first metal bump comprises a first copper layer having a thickness between 5 and 50 micrometers;

a flexible substrate; and

a polymer joining said substrate component and joining a metal trace of said flexible substrate.

12. The circuit component of claim **11** further comprising a second metal bump joining said flexible substrate, wherein said second metal bump comprises a gold layer having a thickness between 1000 angstroms and 2 micrometers.

13. The circuit component of claim **11** further comprising a second metal bump joining said flexible substrate, wherein said second metal bump comprises a gold layer having a thickness between 1 and 50 micrometers.

14. The circuit component of claim 11 further comprising a second metal bump joining said flexible substrate, wherein said second metal bump comprises a second copper layer having a thickness between 5 and 50 micrometers.

15. The circuit component of claim 11 further comprising a second metal bump joining said flexible substrate, wherein said second metal bump comprises a nickel layer having a thickness between 1 and 100 micrometers.

16. The circuit component of claim 11, wherein said first metal bump further comprises a titanium-containing layer under said first copper layer.

17. The circuit component of claim 11, wherein said first metal bump further comprises a tin-containing solder at a top of said first metal bump.

18. The circuit component of claim 17, wherein said tin-containing solder comprises silver.

19. The circuit component of claim 11, wherein said first metal bump further comprises a nickel-containing layer on said first copper layer.

20. The circuit component of claim 19, wherein said nickel-containing layer has a thickness between 1 and 100 micrometers.

21. A chip package comprising:

a semiconductor chip comprising multiple CMOS devices, an insulating layer over said multiple CMOS devices, a metal pad having a contact point under a first opening in said insulating layer, an optical filter over said insulating layer and said multiple CMOS devices, and multiple microlenses over said optical filter, said insulating layer and said multiple CMOS devices;

a circuit component joining said semiconductor chip, wherein a second opening through said circuit component is vertically over said semiconductor chip;

a metal bump between said circuit component and said contact point, wherein said metal bump has a bottom end joining said contact point and a top end joining said circuit component, wherein said metal bump comprises gold; and

a transparent substrate over said semiconductor chip, said multiple microlenses and said optical filter, wherein a cell is between said semiconductor chip and said transparent substrate and vertically over a photo-sensitive area of said semiconductor chip.

22. The chip package of claim 21, wherein said transparent substrate comprises a glass substrate.

23. The chip package of claim 21 further comprising a spacer between said semiconductor chip and said transparent substrate.

24. The chip package of claim 23, wherein said spacer comprises a polymer.

25. The chip package of claim 21, wherein said insulating layer comprises an oxide layer.

26. The chip package of claim 25, wherein said oxide layer has a thickness between 0.2 and 0.7 micrometers.

27. The chip package of claim 21, wherein said metal pad comprises a copper layer.

28. The chip package of claim 21, wherein said metal pad comprises aluminum.

29. A circuit component comprising:

a first substrate;

a second substrate over said first substrate;

a flexible substrate connected to said first substrate; and

a first metal bump between said first and second substrates, wherein said first metal bump comprises a first copper layer having a thickness between 5 and 50 micrometers.

30. The circuit component of claim 29 further comprising a second metal bump between said flexible substrate and said first substrate, wherein said second metal bump comprises a gold layer having a thickness between 1000 angstroms and 2 micrometers.

31. The circuit component of claim 29 further comprising a second metal bump between said flexible substrate and said first substrate, wherein said second metal bump comprises a gold layer having a thickness between 1 and 50 micrometers.

32. The circuit component of claim 29 further comprising a second metal bump between said flexible substrate and said first substrate, wherein said second metal bump comprises a second copper layer having a thickness between 5 and 50 micrometers.

33. The circuit component of claim 29 further comprising a second metal bump between said flexible substrate and said first substrate, wherein said second metal bump comprises a nickel layer having a thickness between 1 and 100 micrometers.

34. The circuit component of claim 29, wherein said first metal bump further comprises a titanium-containing layer under said first copper layer.

35. The circuit component of claim 29, wherein said first metal bump further comprises a tin-containing solder at a top of said first metal bump.

36. The circuit component of claim 35, wherein said tin-containing solder comprises silver.

37. The circuit component of claim 29, wherein said first metal bump further comprises a nickel-containing layer on said copper layer.

38. The circuit component of claim 37, wherein said nickel-containing layer has a thickness between 1 and 100 micrometers.

39. The circuit component of claim 29, wherein said second substrate comprises a glass substrate.

* * * * *