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(54) **FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE**

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(51) **Int. Cl.**
H01L 23/525 (2006.01)

(52) **U.S. Cl.** **257/530**; 257/529; 257/E29.149; 257/E23.147

(58) **Field of Classification Search** 257/530
See application file for complete search history.

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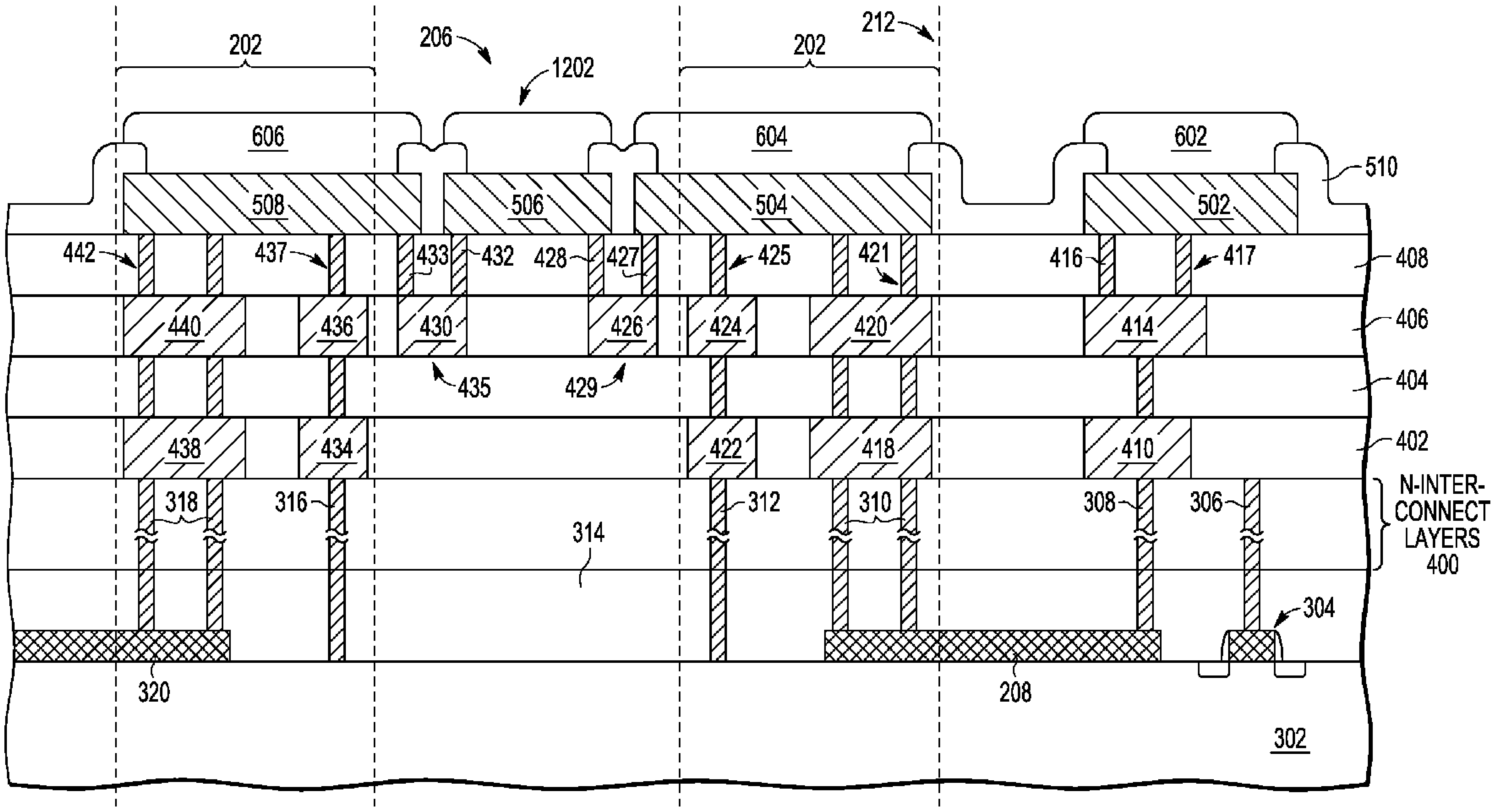
(57) **ABSTRACT**

A semiconductor structure includes a semiconductor substrate; a semiconductor device formed in and over the substrate; a plurality of interconnect layers over the semiconductor device; an interconnect pad over a top surface of the plurality of interconnect layers, wherein the interconnect pad is coupled to the semiconductor device through the plurality of interconnect layers; a contiguous seal ring surrounding the semiconductor device and extending vertically from the substrate to the top surface of the plurality of interconnect layers; and a fuse coupled between the interconnect pad and the seal ring, wherein the fuse is in a non-conductive state.

20 Claims, 11 Drawing Sheets



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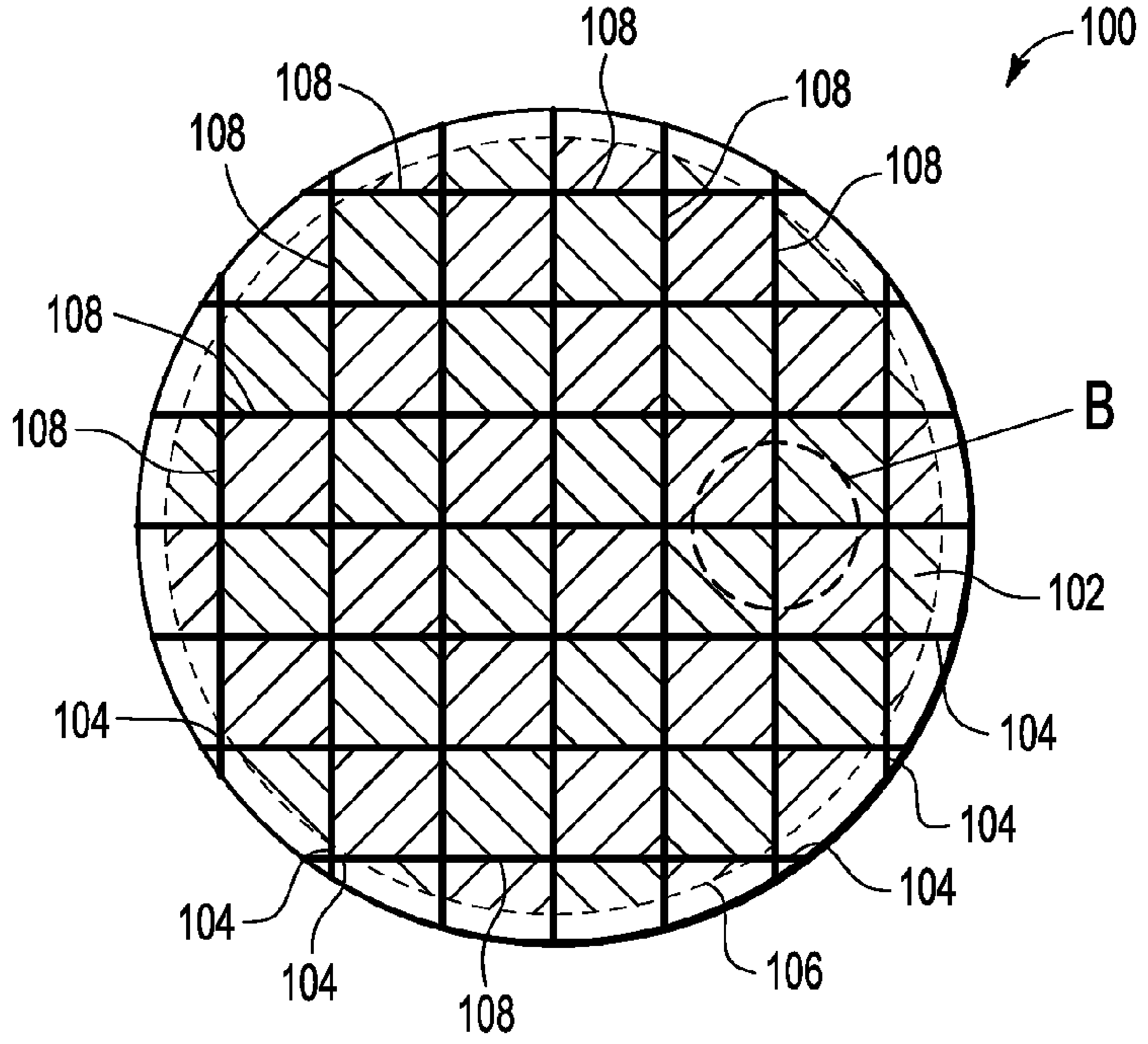
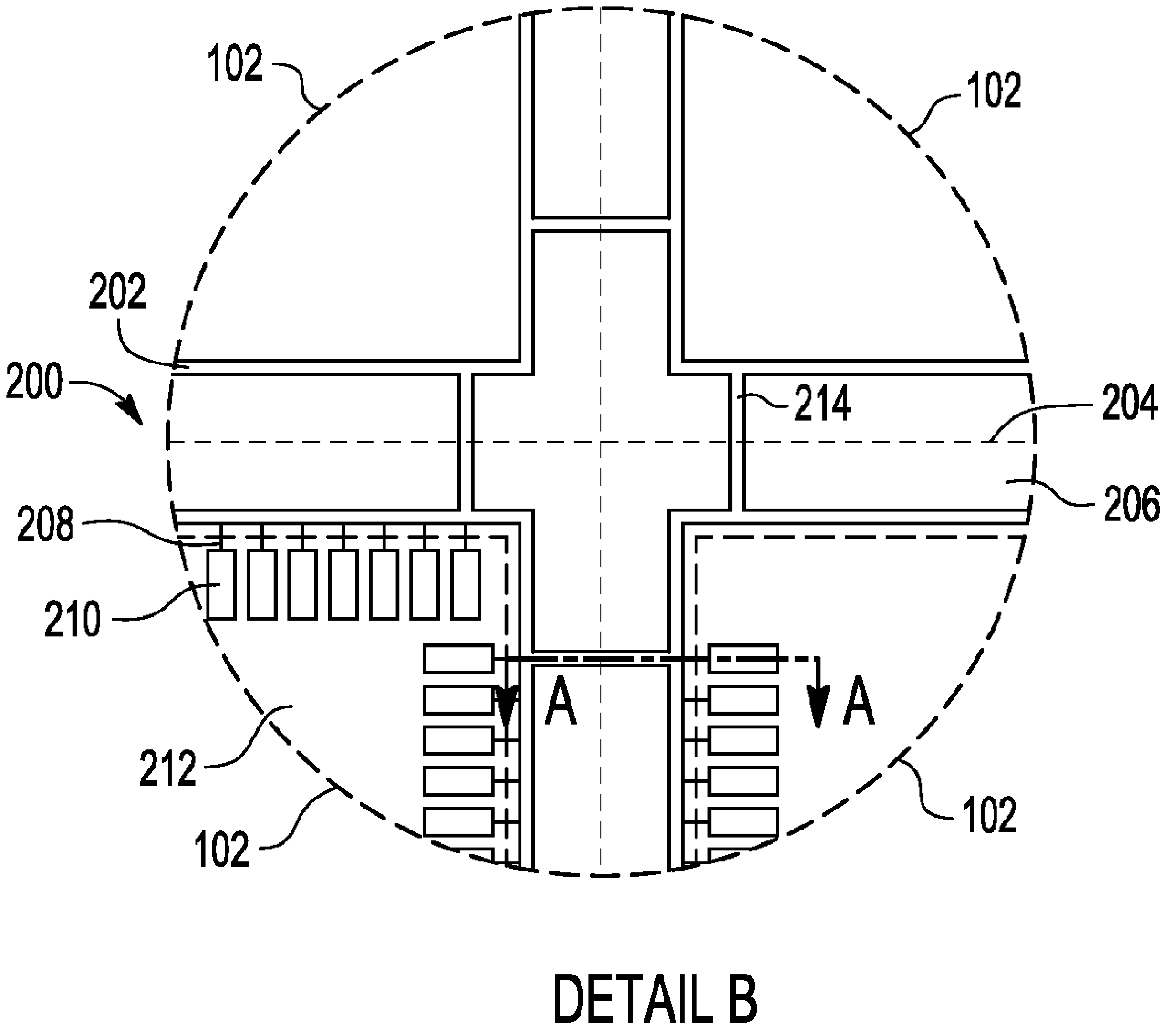


FIG. 1



DETAIL B

FIG. 2

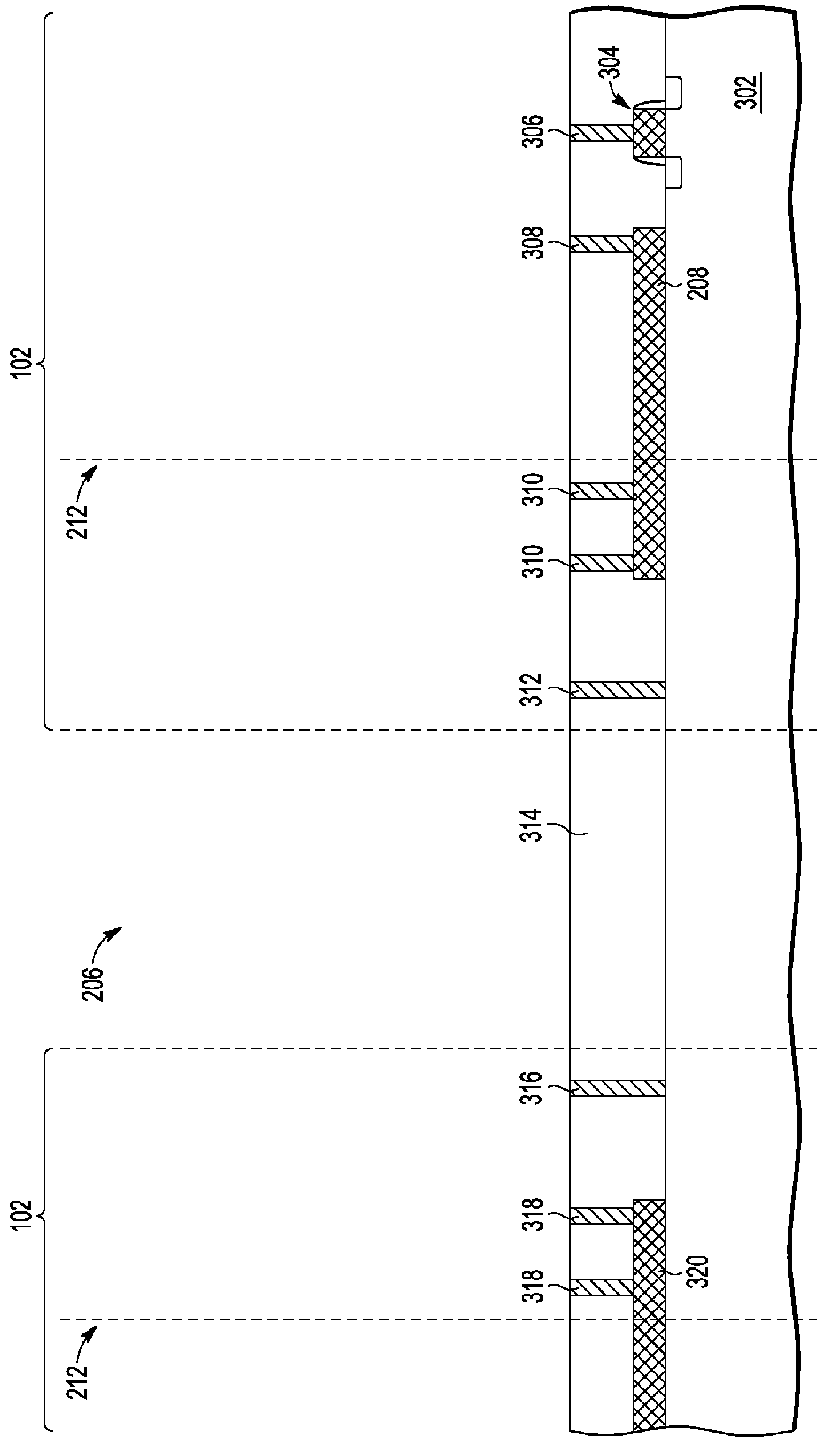


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FIG. 3

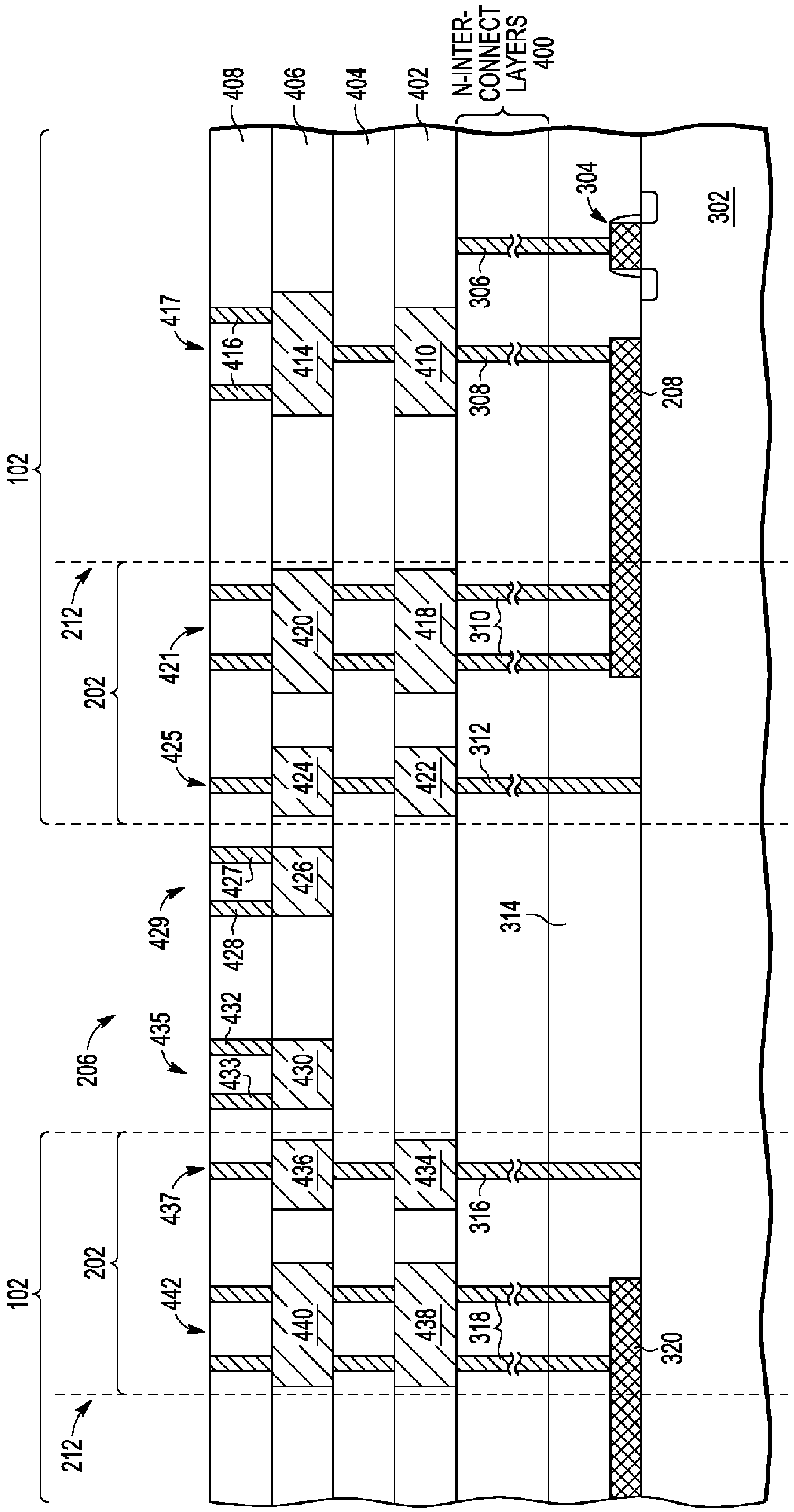

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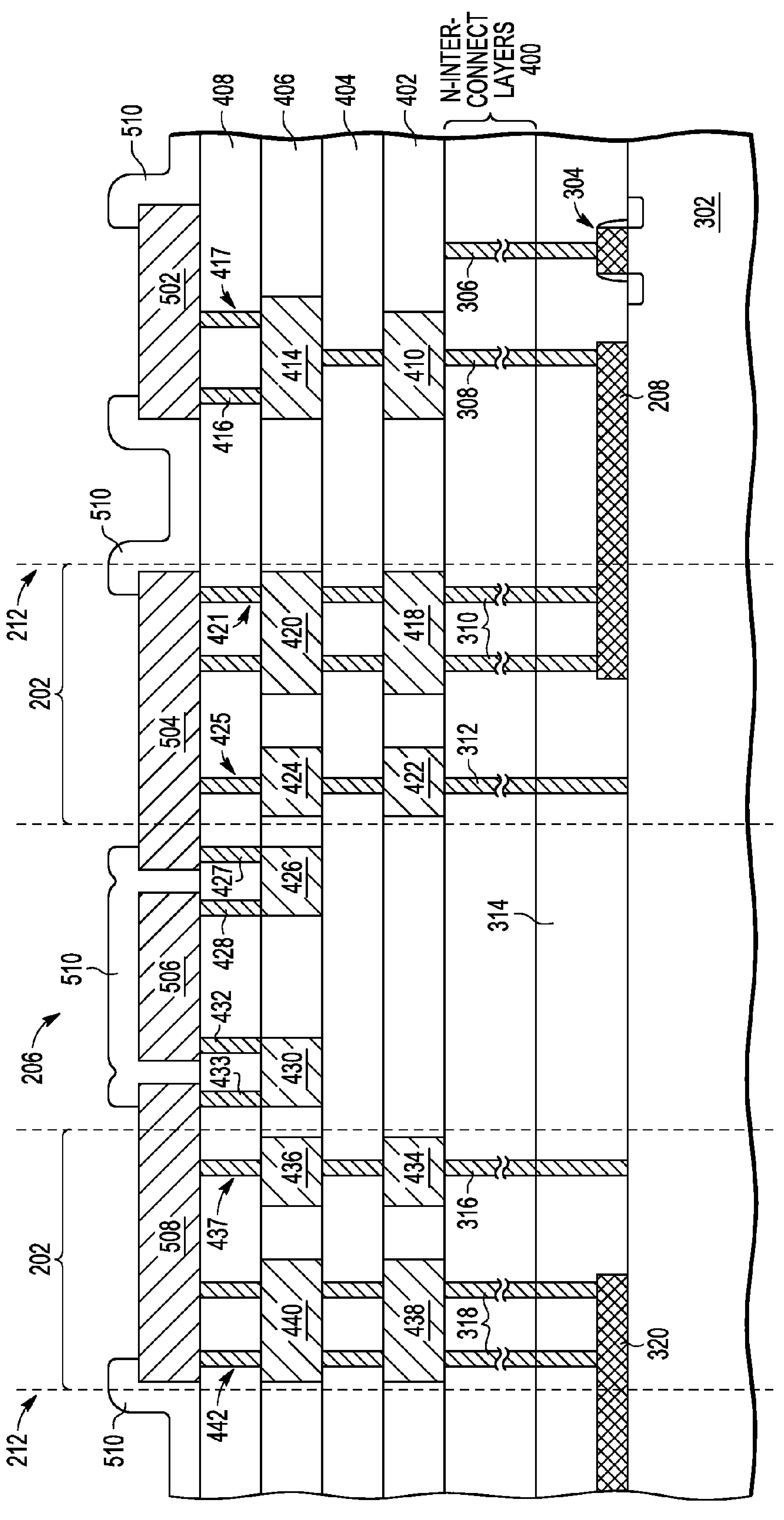
FIG. 4



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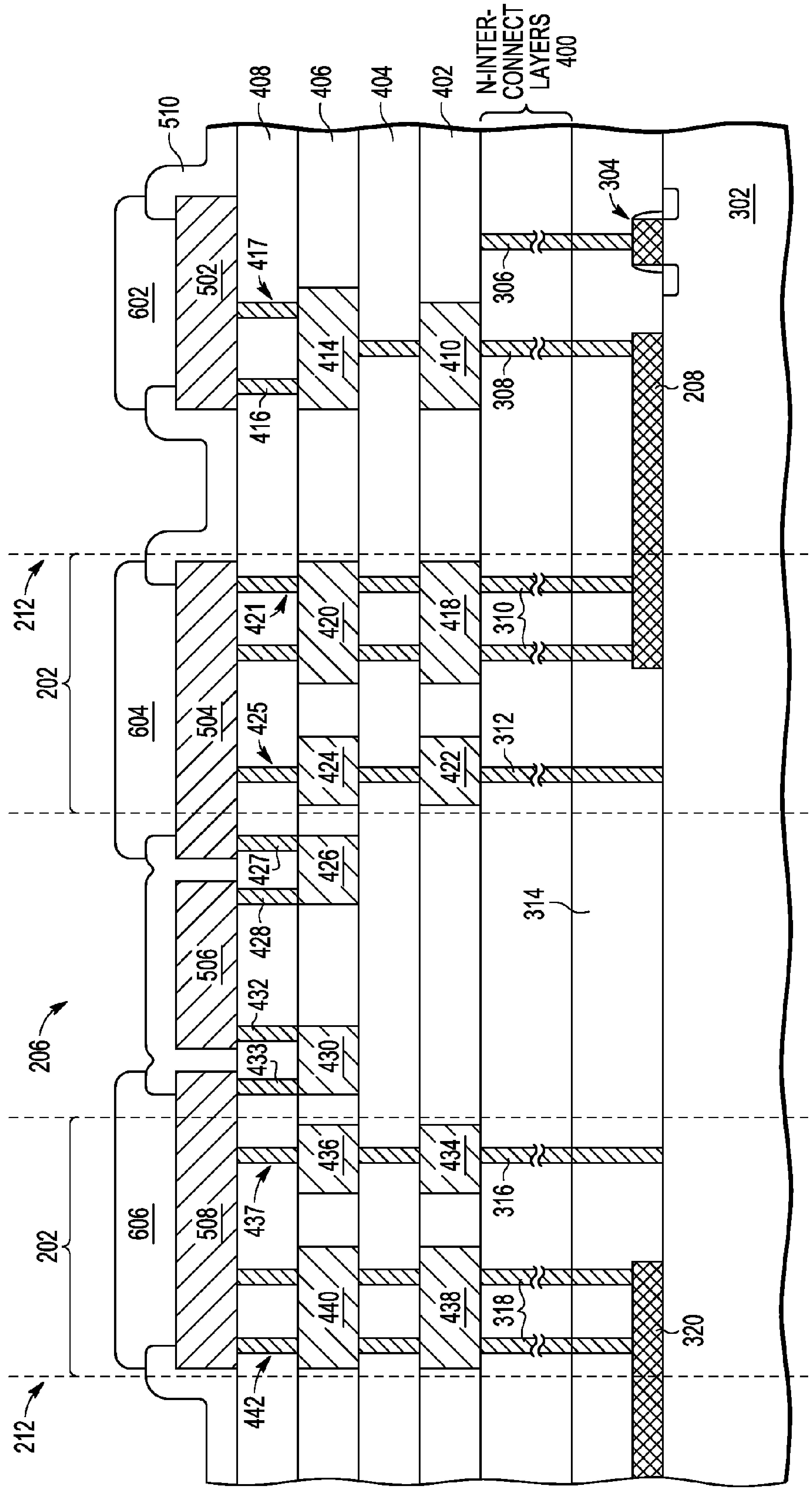

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FIG. 6

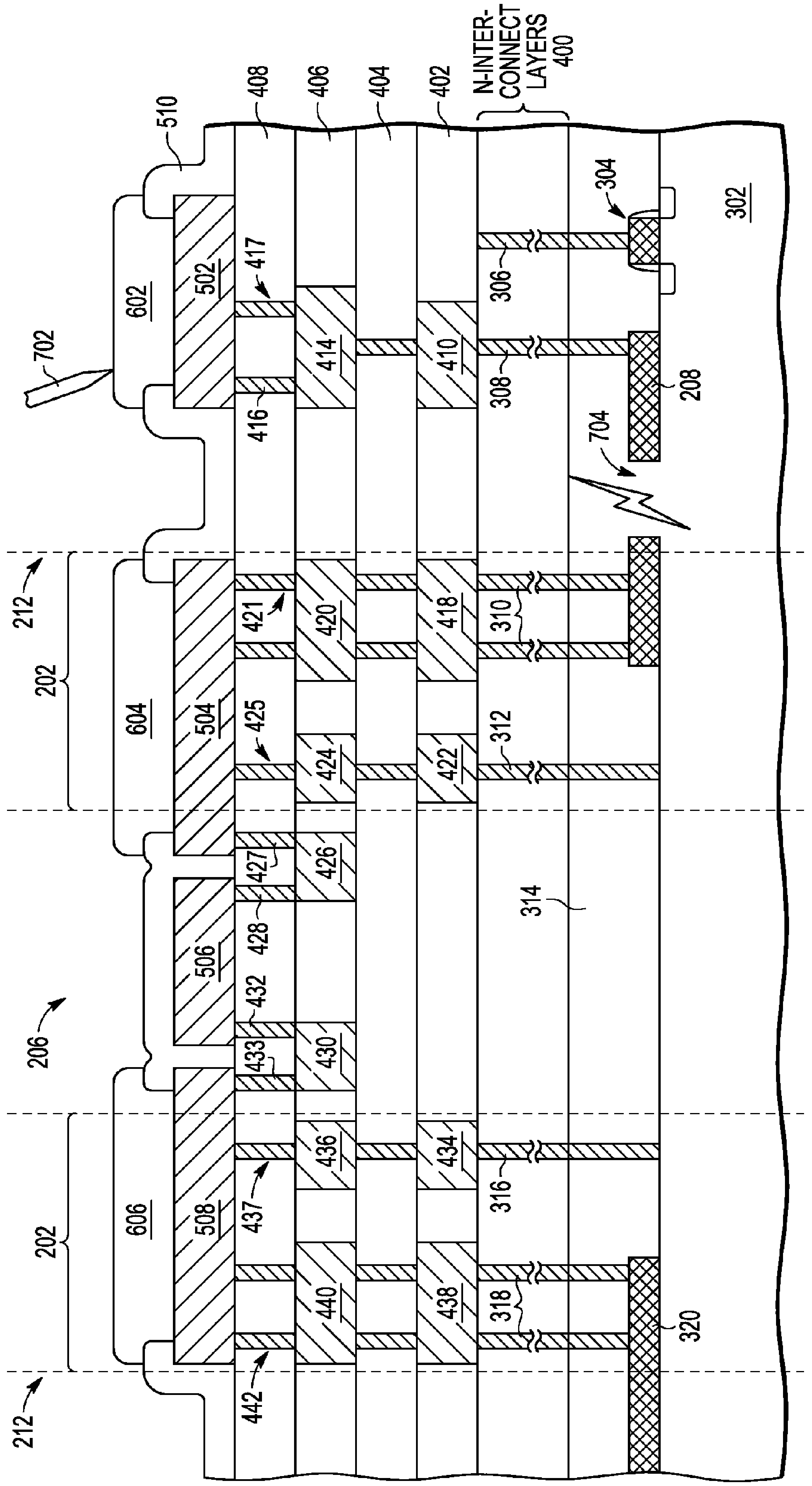

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FIG. 7

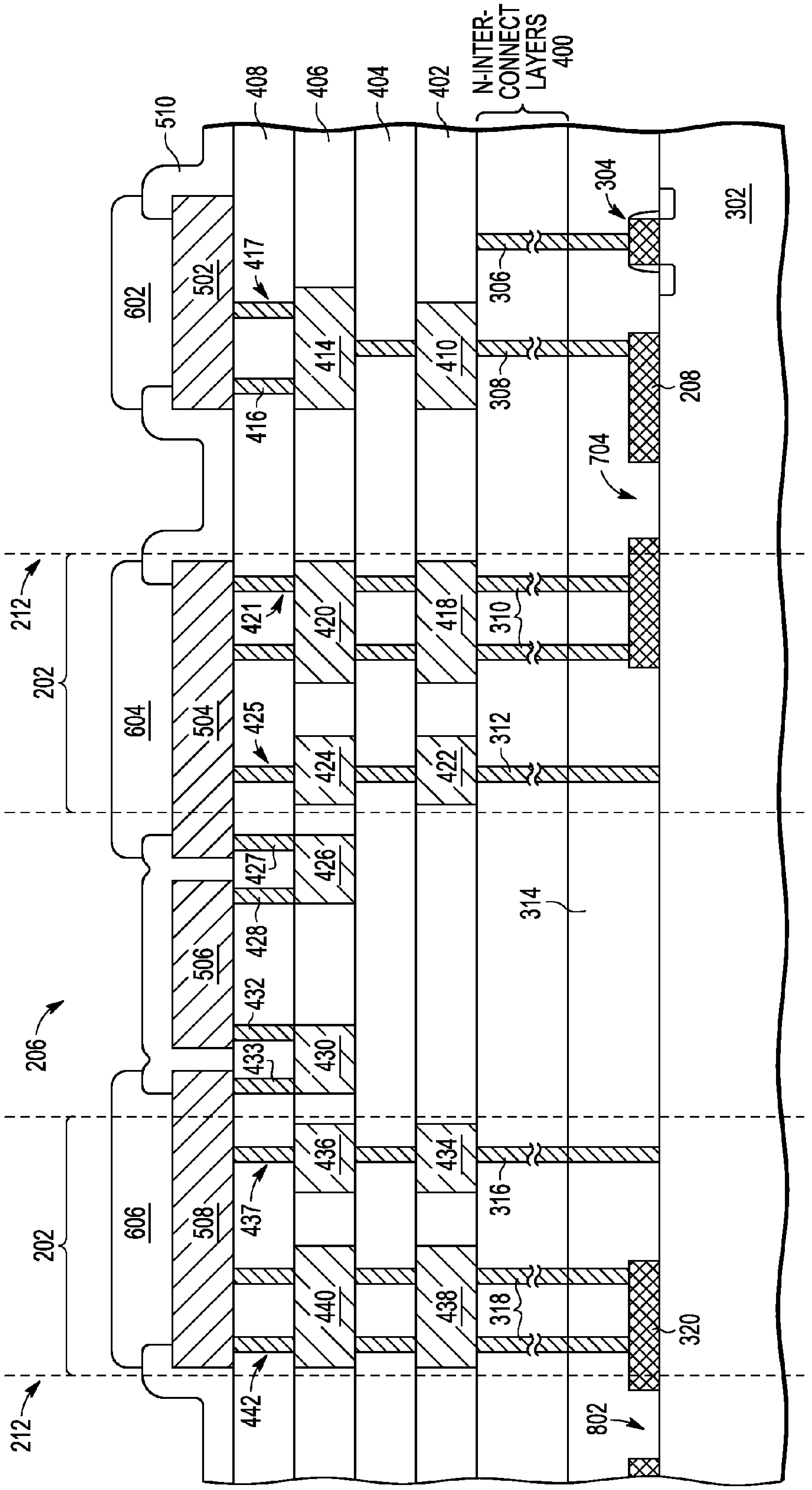

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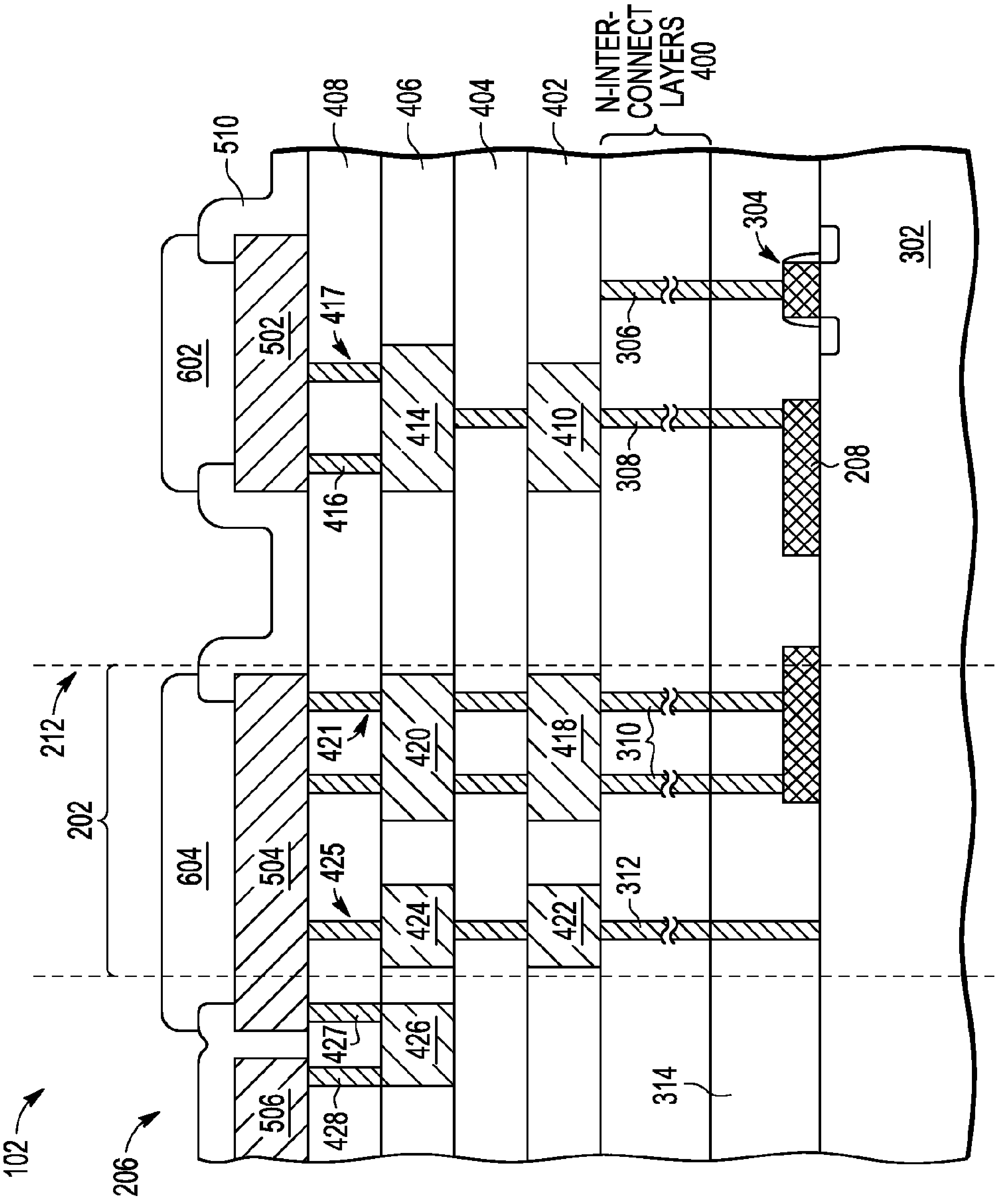
FIG. 8



SECTION A - A

FIG. 9

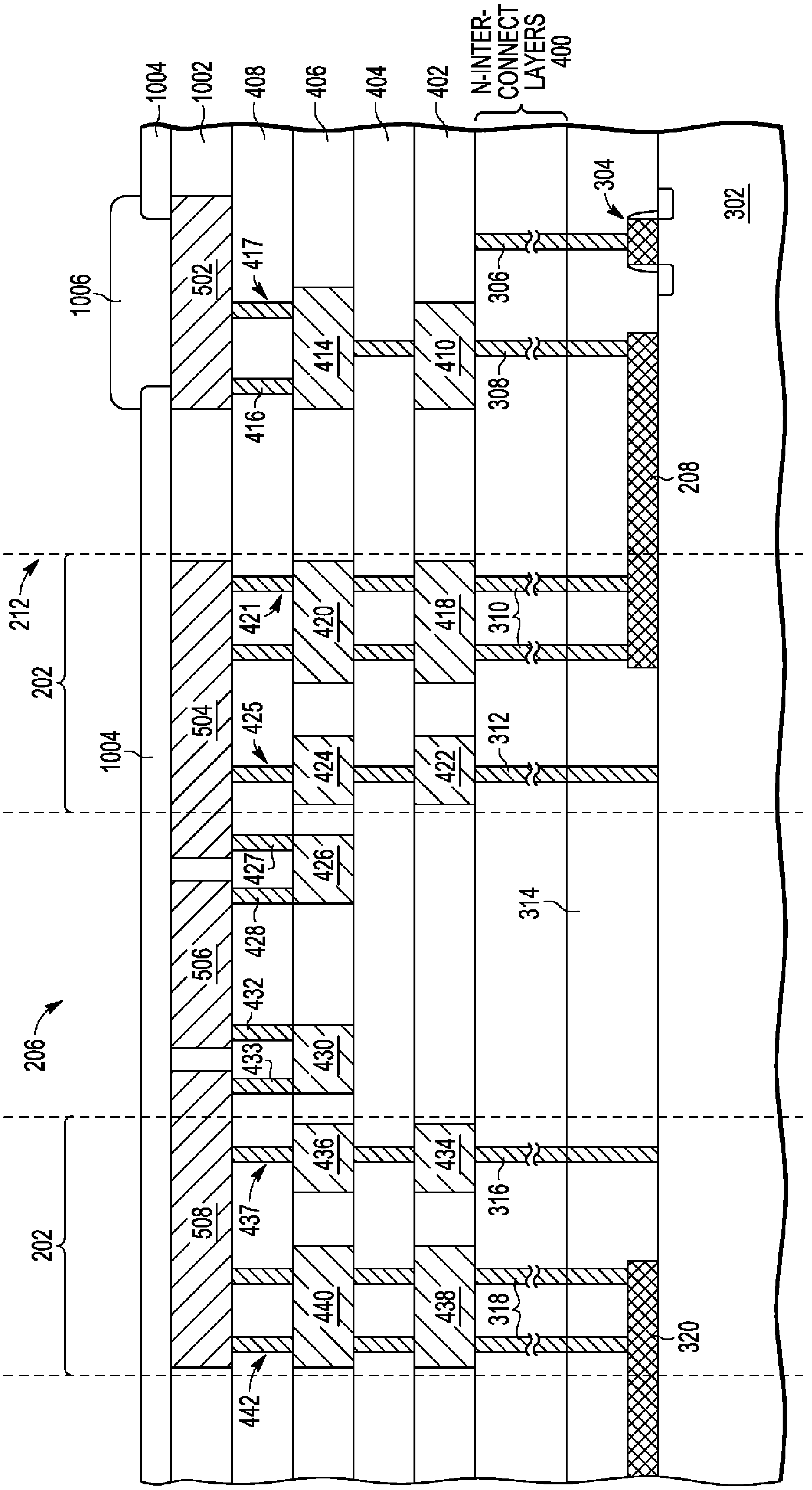


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FIG. 10

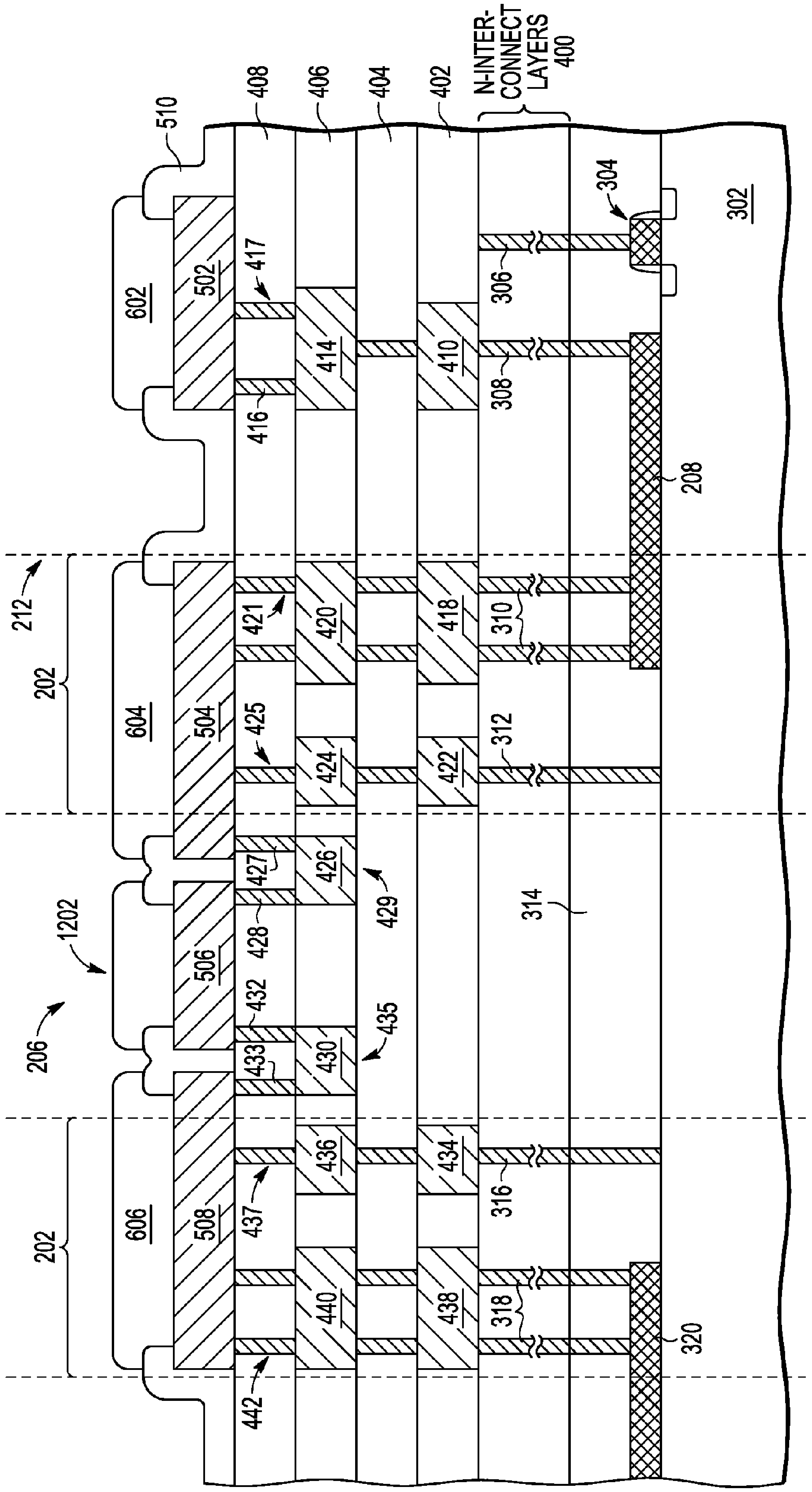

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FIG. 11

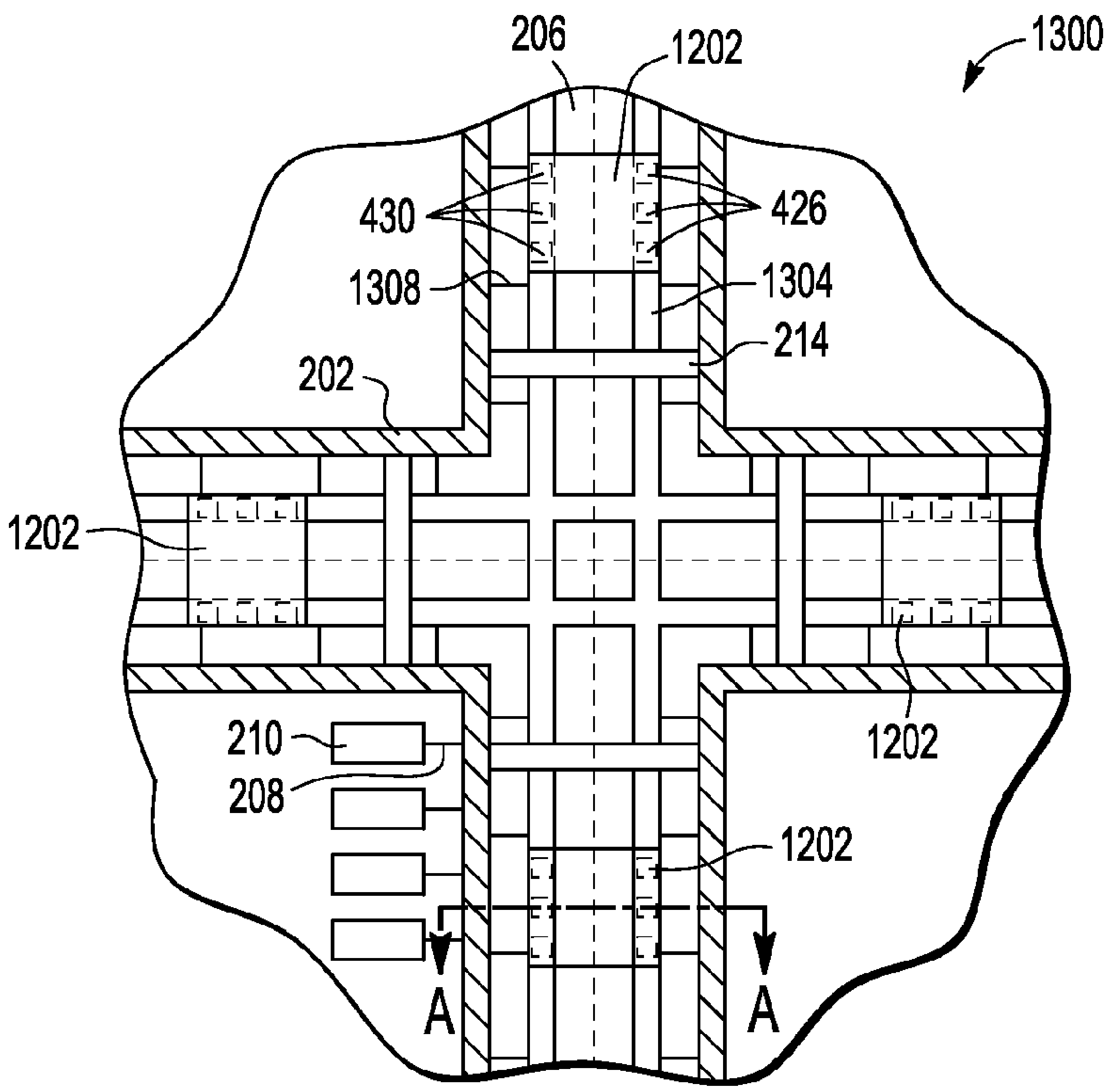
1300
206
1202
430
426
1308
1304
214
202
1202
210
208
1202
1202
A
A

FIG. 12

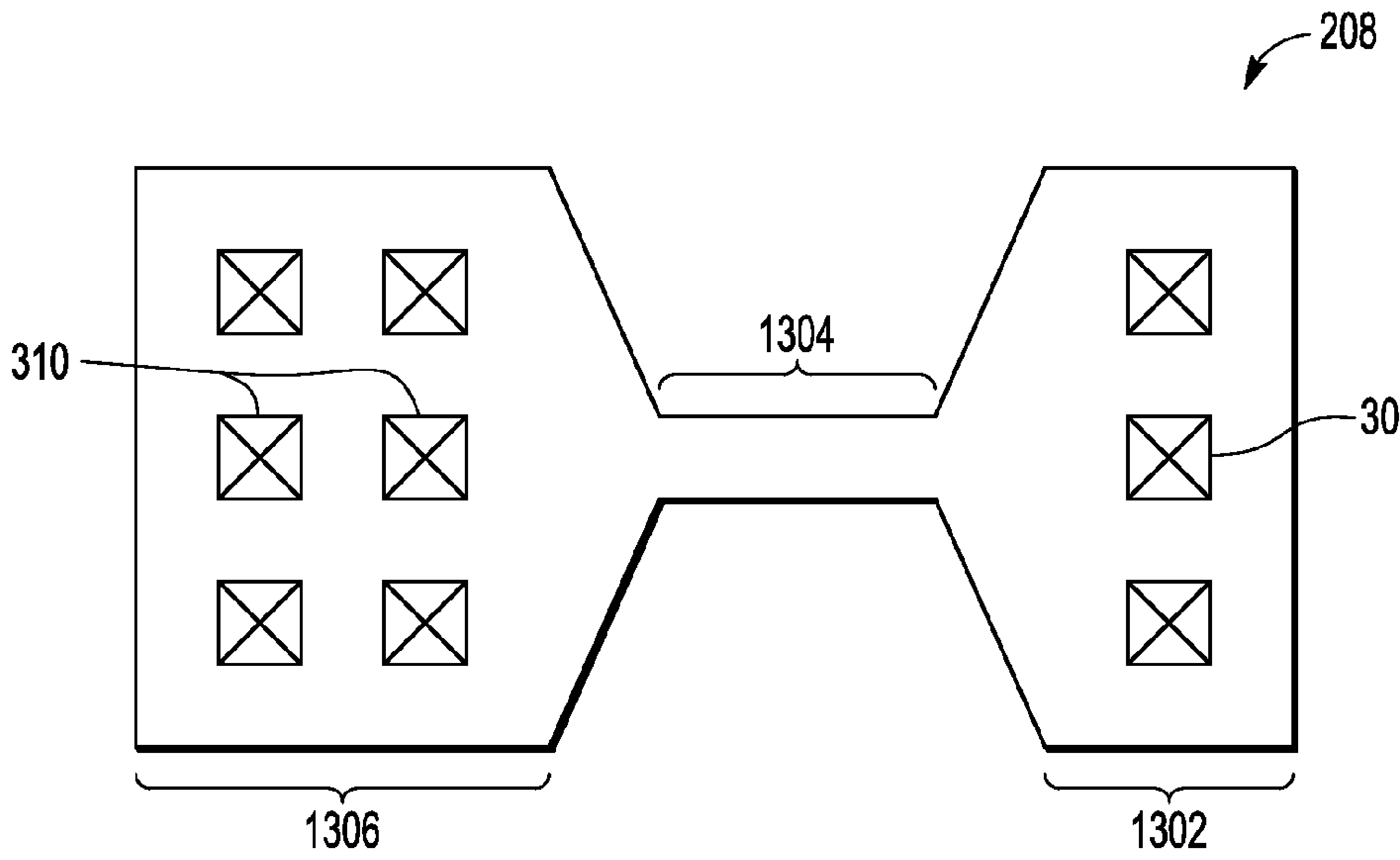
208
1304
310
308
1306
1302

FIG. 13

FUSED BUSS FOR PLATING FEATURES ON A SEMICONDUCTOR DIE

BACKGROUND

1. Field of the Invention

This invention relates in general to semiconductor devices and more specifically to electroplating interconnect pads for semiconductor devices.

2. Description of the Related Art

To electroplate features such as interconnect or bond pads on a semiconductor wafer, plating buses must be added to the top surface of the wafer and then removed after the plating process is complete. The application and removal of the buses add cost.

A replacement for Au—Al wirebonding has been sought. The Over Pad Metallurgy (OPM) process for bond pads was developed to enable Au—Au and Cu—Au bonding. The OPM deposition is currently limited to electroless plating processes because a method for connecting the individual bond pads to a plating bus has not been conceived and traditional pattern (electro) plating processes are cost prohibitive.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

FIG. **1** illustrates a top view of an embodiment of semiconductor wafer.

FIG. **2** is a partial top view of additional detail of the wafer of FIG. **1** according to an embodiment.

FIG. **3** is a partial side cross-sectional view of a wafer after a phase of manufacture in accordance with an embodiment of the present invention.

FIG. **4** is a partial side view of the wafer of FIG. **3** after several other phases of manufacture.

FIG. **5** is a partial side view of the wafer of FIG. **4** after another phase of manufacture.

FIG. **6** is a partial side view of the wafer of FIG. **5** after another phase of manufacture.

FIG. **7** is a partial side view of the wafer of FIG. **6** after another phase of manufacture.

FIG. **8** is a partial side view of the wafer of FIG. **7** after another phase of manufacture.

FIG. **9** is a partial side view of the wafer of FIG. **8** after another phase of manufacture.

FIG. **10** is a partial cross-sectional side view of another embodiment the wafer of FIG. **4** after another phase of manufacture.

FIG. **11** is a partial cross-sectional side view of another embodiment the wafer of FIG. **4** after another phase of manufacture.

FIG. **12** is a partial top view of the wafer of FIG. **11** after another phase of manufacture.

FIG. **13** illustrates a top-down layout schematic view of an embodiment of a fuse that can be used in the wafer of FIGS. **2**-**12**.

The use of the same reference symbols in different drawings indicates identical items unless otherwise noted. The features shown in the Figures are not necessarily drawn to scale.

DETAILED DESCRIPTION

The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

Embodiments of a fused plating bus connection between a seal ring or other continuous die or wafer structure and the individual bond pads on the top surface of the die are disclosed. One embodiment comprises a polysilicon fuse at the active layer of the wafer proximal to the seal ring structure. The contacts of the seal ring are directly connected to the first end of the poly fuse. A metal/via stack electrically coupled to the topmost pad conductive layer is connected to the second end of the fuse link. The metal/via stack can be placed between the bond pad footprint and the seal ring or directly under the bond pad. Seal rings of multiple die on the wafer may be grouped together via an electrical connection to a common metal tracing placed in the scribe street that is later removed during the sawing process.

The current for plating flows through the common metal trace in the scribe street, the seal ring, poly fuse, metal stack, and to the bond pad. Once the plating process is completed, the fuse can be blown by overdriving the fuse with a current higher than that used for the plating process. Thus, bond pads can be electrolytically plated and then isolated from the plating bus. The fuse overdriving process can be performed during wafer probe test where the fuse blowing process can be staged or sequenced to further limit total current needed.

FIG. **1** illustrates a top view of an embodiment of semiconductor wafer **100** with a plurality of integrated circuit (IC) die **102** formed thereon. IC die **102** are shown cross-hatched in FIG. **1** to distinguish IC die **102** from unused portions of around the circular edge of wafer **100**. Plating traces **104** are connected to seal rings **108** formed around the edge of each IC die **102** in a grid pattern on wafer **100**. The end of each trace **104** can extend into and beyond edge bead region **106** to the edge of wafer **100**. Metal interconnect layers in the edge bead region **106** can be exposed by selectively removing dielectric material using processes and tools known in the art. Referring to FIG. **2**, a partial top view of additional detail of a portion delineated by area B of wafer **100** in FIG. **1** according to an embodiment is shows corner portions at an intersection of four IC dies **102** having seal rings **202**, singulation path **204**, scribe streets **206**, fuses **208**, interconnect pads **210**, active regions **212**, and seal ring interconnects **214**.

Seal rings **202** are placed around the perimeter of IC dies **102** to seal the edge of IC dies **102** from contaminating ions that affect the yield during processing and affect performance of IC die **102** after IC die **102** has been fabricated. In addition, seal ring **202** is grounded to a substrate (not shown) of wafer **200**. In another embodiment, the seal ring **202** is connected to the substrate through a well implant (not shown). Singulation paths **204** are shown by dashed lines in scribe streets **206** to indicate the location where a saw and/or laser may be used to separate IC die **102** from one another.

Active regions **212** of IC die **102** are delineated by a dashed line inside the perimeter of seal ring **202** and include circuitry (not shown) that is used for the functionality of a semiconductor device. For example, active regions **212** may include circuitry used for logic or memory functions. Interconnect pads **210** are coupled to the circuitry in active regions **212** and are typically arranged in one or more rows around the inside perimeter of active regions **212**. Each of fuses **208** are coupled between a corresponding interconnect pad **210** and seal ring **202**. One end of each seal ring interconnect **214** is coupled to a first seal ring **202** and another end of seal ring interconnect **214** is coupled to another seal ring **202** across scribe street **206**. Seal rings **202** are thus interconnected with one another either directly or indirectly by seal ring interconnects **214**.

FIG. **3** is a partial side cross-sectional view of wafer **200** after a phase of manufacture in accordance with an embodiment of the present invention. Scribe street **206** and first and second active regions **212** are delineated by vertical dashed lines. Wafer **200** includes dielectric layer **314** formed over substrate **302**, transistor having a gate electrode **304** and contact **306**, and fuses **208**, **320**. Electrical interconnections including gate contact **306**, conductive vias **308**, **310**, **312**, **316**, **318** are formed though dielectric layer **314** to corresponding components as further describe herein. Gate electrode **304** is shown as an example of one of various types of active circuitry that may be included in active regions **212**. Substrate **302** can be any suitable silicon or silicon-on-insulator (SOI) substrate, such as bulk silicon substrate, a gallium arsenide substrate, or the like, having an active region **212**.

A first end portion of fuses **208**, **320** are positioned in respective active regions **212** and a second end portion of fuses **208**, **320** are positioned between respective active regions **212** and scribe street **206**. Via **308** is coupled to fuse **208** inside first active region **212**, while a pair of vias **310** are coupled to fuse **208** between first active region **212** and scribe street **206**. Another via (not shown) is coupled to fuse **320** inside second active region **212**, while a pair of vias **318** are coupled to fuse **320** between second active region **212** and scribe street **206**. As additional layers are formed on substrate **302**, vias **310** will form part of first seal ring **202** (FIG. **2**) and via **312** will form part of a crack stop for first IC die **102**. Similarly, vias **318** will form part of second seal ring **202** (FIG. **2**) and another via **316** will form part of a crack stop for second IC die **102**.

FIG. **4** is a partial side view of the wafer of FIG. **3** after several other phases of manufacture including forming a number (N) of interconnect layers **400**, which are not shown in detail in FIG. **4**, but include alternating metal interconnect layers and via layers that may be similar to metal interconnect layer **402** and via layer **404**. In one embodiment, conductive portions of metal interconnect and via layers include copper. In another embodiment, the conductive portions of metal interconnect layers include aluminum and conductive portions of via layers include tungsten. Any number of vias may be formed between conductive portions of adjacent metal interconnect layers.

Stacked vias **306**, **308**, **310**, **312**, **316**, **318** are formed vertically through dielectric layers in interconnect layers **400**, as well as in via layers **404**, **408**. In the embodiment shown, layer **402** includes metal interconnect **410** coupled to stacked via **308** in active region **212**. In the region between active region **212** and scribe street **206**, layer **402** further includes metal interconnect **418** coupled to a pair of stacked vias **310**; metal interconnect **422** coupled to via stack **312**; metal interconnect **434** coupled to stacked via **316**; and metal interconnect **438** coupled to a pair of stacked vias **318**.

Layer **406** includes metal interconnect **414** coupled to stacked via **308** in active region **212**. In the region between active region **212** and scribe street **206**, layer **406** further includes metal interconnect **420** coupled to stacked via **310**; metal interconnect **424** coupled to stacked via **312**; metal interconnect **436** coupled to stacked via **316**; and metal interconnect **440** coupled to a pair of stacked vias **318**.

Additionally, layer **406** includes first and second metal interconnects **426**, **430** in scribe street **206**. Layer **408** includes vias **427**, **428**, **432**, **433** coupled to respective metal interconnects **426**, **430** in layer **406**. Metal interconnect **426** and vias **427**, **428** form a first scribe street contact **429** for seal ring interconnect **214** (FIG. **2**). Metal interconnect **430** and vias **432**, **433** form a second scribe street contact **435** for seal ring interconnect **214**.

Plating bus portion **417** is thus formed in active region **212** by stacked vias **308** coupled between fuse **208**, metal interconnects **410**, **414**, and a pair of vias **416** coupled to metal interconnect **414**. Plating bus portion **417** couples interconnect pad **210** (FIG. **2**) to the first end portion of fuse **208** in active region **212**. Additional plating bus portions **417** are formed in active region **212** for other interconnect pads of IC die **102**, but are not shown in the figures. Further, plating bus portions **417** are formed in active regions **212** for other IC die **102**, but are not shown in the figures.

First edge seal **421** is formed in the region between first active region **212** and scribe street **206** by the pair of stacked vias **310** connected to fuse **208** in layer **314** and extending through layers **400**, **404**, **408**. The pair of stacked vias **310** are further connected to metal interconnects **418**, **420** in respective layers **402**, **406**.

First crack stop **425** is thus formed in the region between edge seal **421** and scribe street **206** by stacked via **312** extending from the bottom of dielectric layer **314** to the top of dielectric layer **408** and coupled to metal interconnects **422**, **424** in respective conductive layers **402**, **406**.

Second edge seal **442** is thus formed in the region between second active region **212** and scribe street **206** by the pair of stacked vias **318** connected to fuse **320** in dielectric layer **314** extending through layers **400**, **404**, **408**. The pair of stacked vias **318** are further connected to metal interconnects **438**, **440** in respective layers **402**, **406**.

Second crack stop **437** is thus formed in the region between edge seal **442** and scribe street **206** by stacked via **316** extending from the bottom of dielectric layer **314** to the top of dielectric layer **408** and coupled to metal interconnects **434**, **436** in respective conductive layers **402**, **406**.

Seal rings **202** surround the periphery of respective active regions **212** and can include a respective edge seal **421**, **442** and, optionally, crack stop **425**, **437**. Although example seal rings **202** for two adjacent IC die **102** on wafer **100** have been described, additional seal rings **202** are formed around the periphery of IC die **102** to prevent moisture from penetrating into active regions **212** of respective IC dies **102** as well as to provide conductive interconnects to fuses **208** and **320**. Additional crack stops **425**, **437** may be formed to prevent cracks created when respective IC dies **102** are singulated (e.g., by a saw or laser) from penetrating into active regions **212**.

FIG. **5** is a partial side view of the wafer of FIG. **4** after another phase of manufacture during which conductive interconnect pad **502** is formed in active region **212** over vias **416** of plating bus portion **417**. During the same process, plating bus contacts **504**, **508** are formed over respective seal rings **202** and vias **427**, **433**; and seal ring interconnect **506** is formed over vias **428** and **432**, thereby conductively interconnecting seal rings **202**, fuses **208**, **320**, plating bus portions **417**, and interconnect pad **502**.

Passivation layer **510** is then formed over dielectric layer **408** and interconnect pad **502**, plating bus contacts **504**, **508**, and seal ring interconnect **506**. Passivation layer **510** is removed over portions of interconnect pad **502** and plating bus contacts **504**, **508**, but is left over seal ring interconnect **506**.

FIG. **6** is a partial side view of the wafer of FIG. **5** after another phase of manufacture in which conductive layers **602**, **604**, **606** are formed or electroplated on interconnect pad **502** and plating bus contacts **504**, **508** using conventional electroplating methods. In some embodiments, conductive layers **602**, **604**, **606** are formed by electroplating interconnect pad **502** and plating bus contacts **504**, **508**. A potential is applied to seal rings **202** (also referred to as traces **104** in FIG. **1**) to provide the required electric current for the electroplating process. The electroplating process can be used to plate metals such as Ni, Ni—Au, Ni—Pd—Au, Cu, Cu—Pd or other metals in various embodiments. A metal ring for contacting the electroplating tooling can be formed in the wafer fab process using commonly practiced wafer edge processing methods known to one skilled in the art. Interconnect pad **502** and seal rings **202** are electrically coupled. The current used during the electroplating process is less than the current required to overload fuses **208**, **320**. For example, for 90 nm CMOS technology, current in the range of 2 to 10 microAmps can be used during electroplating a single contact pad whereas a current in the range of 40-150 milliAmps is required to blow fuses **208**, **320**.

FIG. **7** is a partial side view of the wafer of FIG. **6** after another phase of manufacture in which current is supplied to interconnect pad **502** through test probe **702** which contacts conductive layer **602**. A ground connection to enable current flow through fuse **208** can be made by contacting conductive layer **604** in the seal ring **202**. The current is greater than the current required to overload fuse **208**, thus causing fuse **208** to fail and create an open circuit **704** between circuitry in active region **212** and seal ring **202**. For example, for 45 nm CMOS technology, a fuse with body dimensions of 0.15 um width and 1.0 um length can be overloaded by 100 milliAmps of current applied by a 5 microsecond pulse at 1.5 Volts.

FIG. **8** is a partial side view of the wafer of FIG. **7** after another phase of manufacture during which overload current was applied to an interconnect pad (not shown) connected to fuse **320**. The failure of fuse **320** creates an open circuit **802** between circuitry in respective active region **212** and seal ring **202**.

Overload current can be applied to each interconnect pad **502** in sequence via a respective conductive layer **602**. The amount of current required to overload fuses **208**, **320** is less than the current required to damage active circuitry on IC die **102**.

FIG. **9** is a partial side view of the wafer of FIG. **8** after another phase of manufacture after which IC die **102** have been singulated and are ready to package including attaching IC die **102** to a lead frame or other package substrate (not shown), adding wire bonds between conductive layer **602** and conductive leads on the lead frame or other package substrate, and encapsulating IC die **102** in a protective coating, for example.

FIG. **10** is a partial cross-sectional side view of another embodiment of the wafer of FIG. **6** after another phase of manufacture during which conductive interconnect pad **502** is formed in active region **212** over vias **416** of plating bus portion **417**. During the same process, plating bus contacts **504**, **508** are formed over respective seal rings **202** and vias **427**, **433**; and seal ring interconnect **506** is formed over vias **428** and **432**, thereby conductively interconnecting seal rings **202**, fuses **208**, **320**, plating bus portions **417**, and interconnect pad **502**.

Passivation layer **1004** is then formed over dielectric layer **408** and metal interconnect layer **1002** including interconnect pad **502**, plating bus contacts **504**, **508**, and seal ring interconnect **506**. Passivation layer **1004** is removed over a portion of interconnect pad **502** but is left over plating bus contacts **504**, **508**, and seal ring interconnect **506**. Thus, the surface of seal ring interconnect **506** is not exposed during the plating process. The advantage of not plating metal onto the surface of seal ring interconnect **506** is that no additional metal is formed in the scribe street. Metal in the scribe street can cause damage to the die during the wafer sawing process.

A conductive layer **1006** can then be formed on interconnect pad **502** by electroplating interconnect pad **502**. Direct potential is applied to seal rings **202** to provide the required electric current for the electroplating process. The interconnect pad **502** is electrically coupled to the seal rings **202**. The current used during the electroplating process is less than the current required to overload fuses **208**, **320**.

Once the electroplating process is complete, current is applied to interconnect pad **502** through a wafer test probe, such as probe **702** (FIG. **7**) which contacts conductive layer **1006**, as well as to other interconnect pads (not shown). The current is applied to the interconnect pads in a sequence such that the maximum instantaneous current applied to the wafer can be controlled. A current greater than the current required to overload fuse **208** is applied to cause fuse **208** to fail and create an open circuit between circuitry in active region **212** and seal ring **202**. A ground connection to enable current flow through fuse **208** can be made by contacting conductive layer **1006** of another interconnect pad electrically coupled to seal ring **202** that is not coupled to the seal ring through an intervening fuse **208**. The testing and subsequent induced fuse failure processes are repeated for each interconnect pad/fuse combination for each die **102**. IC die **102** can then be singulated and packaged as previously described.

FIG. **11** is a partial cross-sectional side view of another embodiment of the wafer of FIG. **6** after an electroplating phase of manufacture during which metal interconnect **602** is formed over interconnect pad **502**, metal interconnects **604**, **606** are formed over plating bus contacts **504**, **508**, and scribe street plating buss contact **1202** is formed over seal ring interconnect **506**.

FIG. **12** is a partial top view of the wafer of FIG. **1** showing scribe street plating buss contacts **1202** spaced at intervals along continuous seal rings **202**. Plating buss contacts **1202** provide a plurality of contacts for applying the plating current uniformly across the wafer during the electroplating process.

Once the electroplating process is complete, a current greater than the current required to overload fuse **208** is applied to conductive layer **602** via wafer test probe, such as probe **702** of FIG. **7**, as well as to other interconnect pads (not shown) in a sequence such that the maximum instantaneous current applied to the wafer can be controlled. A ground connection to scribe street plating buss contact **1202** can be made to enable current flow through fuse **208**. The testing and subsequent induced fuse failure processes are repeated for each interconnect pad/fuse combination for each die **102**. IC die **102** can then be singulated and packaged as specified.

FIG. **13** illustrates a top-down layout view of an embodiment of fuse **208** that can be used in the wafer of FIGS. **2-12**. Fuse **208** includes first end portion **1302**, center portion **1304**, and second end portion **1306**. Center portion **1304** has a narrower cross-section than end portions **1302**, **1306**. First and second end portions **1302**, **1306** include respective contacts **308**, **310** to provide an electrical connection between interconnect pad plating bus portion **417** and edge seal plating buss portion **421** (FIG. **4**). Note that although six contacts **310** and three contacts **308** are shown to form each electrical connection, any number and shape of contacts can be used to provide the electrical connections. For example, in another embodiment, the electrical connections to the one or more end portions may be made by bar contacts. Fuse **208** is blown by driving a high enough current through it to result in fuse **208** being changed to a nonconductive state, thereby eliminating the electrical connection between end portions **1302**, **1306**.

By now it should be appreciated that there has been provided methods and structures for forming and using polysilicon fuses **208**, **320** coupled to seal rings **202** and interconnect pads **502-508** as electroplating busses for semiconductor devices. One end of fuses **208**, **320** is coupled to respective edge seals **421**, **442** and another end of fuses **208**, **320** is coupled to respective interconnect pads **502**. In one embodiment, one end of fuses **208**, **320** is located under respective edge seals **421**, **442** and another end of fuses **208**, **320** is located under respective interconnect pads **502**. The addition of fuses **208**, **320** therefore should not affect the size of IC die **102**. In another embodiment, one end of the fuses **208**, **320** is coupled to respective edge seals **421**, **442** but not located below the seal ring **202**. In still another embodiment, another end of fuses **208**, **320** is coupled to the respective interconnect pad **502**, but is not located below the interconnect pad **502**. In yet another embodiment, the fuses **208**, **320** may be formed within a layer of the plurality of interconnect layers **400**.

Currently known electroplating processes use a large number of steps that are not required in the methods and structures disclosed herein. For example, with currently known methods, the steps include fabricating a wafer, applying an electroplating buss, applying photoresist, exposing and developing the elements to be electroplated, electroplating the elements, stripping the photoresist, removing the plating buss, testing electrical connections and functionality of the wafer, and singulating the IC die.

In contrast, embodiments of the electroplating process for the present disclosure include fabricating the wafer with fuses **208**, **320** coupled to seal rings **202**, electroplating the exposed elements, applying current to blow fuses **208**, **320** coupled to an electroplated element, testing electrical connections and functionality of the IC die on the wafer and singulating the wafer into individual IC die. Embodiments of the novel fused electroplating buss structure can be fabricated using the same processes as required to create active circuitry and seal rings **202** currently being performed and requires no additional area on the IC die. The novel process of blowing the fuses after interconnect pads **502** are electroplated disconnects active circuitry and interconnect pads **502** from the seal rings **202**. Thus embodiments of structures and methods disclosed herein provide the advantages of electroplating while eliminating most of the process steps and cost associated with electroplating.

Accordingly, in some embodiments, as shown in FIGS. **1-13** and described herein, a semiconductor structure can comprise a semiconductor substrate; a semiconductor device formed in and over the substrate; a plurality of interconnect layers over the semiconductor device; an interconnect pad over a top surface of the plurality of interconnect layers, wherein the interconnect pad is coupled to the semiconductor device through the plurality of interconnect layers; a contiguous seal ring surrounding the semiconductor device and extending vertically from the substrate to the top surface of the plurality of interconnect layers; and a fuse coupled between the interconnect pad and the seal ring, wherein the fuse is in a non-conductive state.

In some aspects, the fuse can be on the substrate.

In other aspects, a dielectric layer can be included over the fuse and the semiconductor device, wherein the plurality of interconnect layers is over the dielectric layer.

In further aspects, the fuse can be further characterized as a polysilicon fuse.

In further aspects, the fuse can be within an interconnect layer of the plurality of interconnect layers.

In further aspects, a plated conductive layer can be included on the interconnect pad.

In further aspects, a first terminal of the fuse can be connected to the interconnect pad through the plurality of interconnect layers and a second terminal of the fuse is connected to the seal ring through at least one interconnect layer of the plurality of interconnect layers.

In further aspects, the contiguous seal ring can comprise a contiguous edge seal surrounding the semiconductor device; and a contiguous crack stop surrounding the contiguous edge seal, wherein the fuse is coupled between the interconnect pad and the contiguous edge seal.

In further aspects, a plurality of interconnect pads can be included over the top surface of the plurality of interconnect layers; and a plurality of fuses can be coupled between a corresponding interconnect pad of the plurality of interconnect pads and the seal ring.

In further aspects, each fuse of the plurality of fuses can be in a non-conductive state.

In further aspects, each of the plurality of interconnect layers can comprise conductive portions, wherein the interconnect pad comprises a conductive material that is different from a conductive material of the conductive portions.

In further aspects, a plated conductive layer can be included on an exposed top surface of the contiguous seal ring and on the interconnect pad.

In other embodiments, a semiconductor structure can include a semiconductor substrate; active circuitry in and on the semiconductor substrate; a plurality of interconnect layers over the active circuitry; a plurality of interconnect pads over a top surface of the plurality of interconnect layers, wherein each interconnect pad is coupled to the active circuitry through the plurality of interconnect layers; a contiguous seal ring surrounding the active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers; a plurality of fuses, wherein each fuse of the plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the seal ring through at least one interconnect layer of the plurality of interconnect layers; and a plated conductive layer on each interconnect pad of the plurality of interconnect pads.

In further aspects, each fuse of the plurality of fuses can be further characterized as a polysilicon fuse.

In further aspects, each fuse of the plurality of fuses can be in a non-conductive state.

In further aspects, each fuse of the plurality of fuses can be on the semiconductor substrate.

In further aspects, at least one fuse of the plurality of fuses can be within an interconnect layer of the plurality of interconnect layers.

In further aspects, the contiguous seal ring can comprise: a contiguous edge seal surrounding the semiconductor device; and a contiguous crack stop surrounding the contiguous edge seal, wherein each fuse of the plurality of fuses is coupled between the corresponding interconnect pad and the contiguous edge seal.

In further aspects, a plated conductive layer on an exposed top surface of the contiguous seal ring can be included.

In still other embodiments, a semiconductor structure can comprise a semiconductor substrate; a plurality of interconnect layers over the semiconductor substrate; in a first die: first active circuitry in and on the semiconductor substrate, wherein the plurality of interconnect layers is over the first active circuitry; a first plurality of interconnect pads over a top surface of the plurality of interconnect layers, wherein each interconnect pad of the first plurality of interconnect pads is coupled to the first active circuitry through the plurality of interconnect layers; a first contiguous seal ring surrounding the first active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers; a first plurality of fuses, wherein each fuse of the first plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the first plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the first seal ring through at least one interconnect layer of the plurality of interconnect layers; and a plated conductive layer on each interconnect pad of the first plurality of interconnect pads; and in a second die, adjacent the first die: second active circuitry in and on the semiconductor substrate, wherein the plurality of interconnect layers is over the second active circuitry; a second plurality of interconnect pads over the top surface of the plurality of interconnect layers, wherein each interconnect pad of the second plurality of interconnect pads is coupled to the second active circuitry through the plurality of interconnect layers; a second contiguous seal ring surrounding the second active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers; a second plurality of fuses, wherein each fuse of the second plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the second plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the second seal ring through at least one interconnect layer of the plurality of interconnect layers; a plated conductive layer on each interconnect pad of the second plurality of interconnect pads; and a seal ring interconnect which connects the first contiguous seal ring to the second contiguous seal ring through at least one interconnect layer of the plurality of interconnect layers in a scribe street between the first and second die.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, polysilicon fuses may be coupled between a seal ring and bumps to serve as electroplating busses for flipchip semiconductor devices. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

The term "coupled," as used herein, is not intended to be limited to a direct coupling or a mechanical coupling. Moreover, the terms "front," "back," "top," "bottom," "over," "under" and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

What is claimed is:

1. A semiconductor structure, comprising:

a semiconductor substrate;

a semiconductor device formed in and over the substrate;

a plurality of interconnect layers over the semiconductor device;

an interconnect pad over a top surface of the plurality of interconnect layers, wherein the interconnect pad is coupled to the semiconductor device through the plurality of interconnect layers;

a contiguous seal ring surrounding the semiconductor device and extending vertically from the substrate to the top surface of the plurality of interconnect layers; and

a fuse coupled between the interconnect pad and the seal ring, wherein the fuse is in a non-conductive state.

2. The semiconductor structure of claim **1** wherein the fuse is on the substrate.

3. The semiconductor structure of claim **2**, further comprising a dielectric layer over the fuse and the semiconductor device, wherein the plurality of interconnect layers is over the dielectric layer.

4. The semiconductor structure of claim **2**, wherein the fuse is further characterized as a polysilicon fuse.

5. The semiconductor structure of claim **1**, wherein the fuse is within an interconnect layer of the plurality of interconnect layers.

6. The semiconductor structure of claim **1**, further comprising a plated conductive layer on the interconnect pad.

7. The semiconductor structure of claim **1**, wherein a first terminal of the fuse is connected to the interconnect pad through the plurality of interconnect layers and a second terminal of the fuse is connected to the seal ring through at least one interconnect layer of the plurality of interconnect layers.

8. The semiconductor structure of claim **1**, wherein the contiguous seal ring comprises:

a contiguous edge seal surrounding the semiconductor device; and

a contiguous crack stop surrounding the contiguous edge seal, wherein the fuse is coupled between the interconnect pad and the contiguous edge seal.

9. The semiconductor structure of claim **1**, further comprising:

a plurality of interconnect pads over the top surface of the plurality of interconnect layers; and

a plurality of fuses, each fuse of the plurality of fuses coupled between a corresponding interconnect pad of the plurality of interconnect pads and the seal ring.

10. The semiconductor structure of claim **9**, wherein each fuse of the plurality of fuses is in a non-conductive state.

11. The semiconductor structure of claim **1**, wherein each of the plurality of interconnect layers comprises conductive portions, and wherein the interconnect pad comprises a conductive material that is different from a conductive material of the conductive portions.

12. The semiconductor structure of claim **1**, further comprising a plated conductive layer on an exposed top surface of the contiguous seal ring and on the interconnect pad.

13. A semiconductor structure, comprising:

a semiconductor substrate;

active circuitry in and on the semiconductor substrate;

a plurality of interconnect layers over the active circuitry;

a plurality of interconnect pads over a top surface of the plurality of interconnect layers, wherein each interconnect pad is coupled to the active circuitry through the plurality of interconnect layers;

a contiguous seal ring surrounding the active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers;

a plurality of fuses, wherein each fuse of the plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the seal ring through at least one interconnect layer of the plurality of interconnect layers; and

a plated conductive layer on each interconnect pad of the plurality of interconnect pads.

14. The semiconductor structure of claim **13**, wherein each fuse of the plurality of fuses is further characterized as a polysilicon fuse.

15. The semiconductor structure of claim **13**, wherein each fuse of the plurality of fuses is in a non-conductive state.

16. The semiconductor structure of claim **13**, wherein each fuse of the plurality of fuses is on the semiconductor substrate.

17. The semiconductor structure of claim **13**, wherein at least one fuse of the plurality of fuses is within an interconnect layer of the plurality of interconnect layers.

18. The semiconductor structure of claim **13**, wherein the contiguous seal ring comprises:

a contiguous edge seal surrounding the semiconductor device; and

a contiguous crack stop surrounding the contiguous edge seal, wherein each fuse of the plurality of fuses is coupled between the corresponding interconnect pad and the contiguous edge seal.

19. The semiconductor structure of claim **13**, further comprising a plated conductive layer on an exposed top surface of the contiguous seal ring.

20. A semiconductor structure, comprising:

a semiconductor substrate;

a plurality of interconnect layers over the semiconductor substrate;

in a first die:

first active circuitry in and on the semiconductor substrate, wherein the plurality of interconnect layers is over the first active circuitry;

a first plurality of interconnect pads over a top surface of the plurality of interconnect layers, wherein each interconnect pad of the first plurality of interconnect pads is coupled to the first active circuitry through the plurality of interconnect layers;

a first contiguous seal ring surrounding the first active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers;

a first plurality of fuses, wherein each fuse of the first plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the first plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the first seal ring through at least one interconnect layer of the plurality of interconnect layers; and

a plated conductive layer on each interconnect pad of the first plurality of interconnect pads; and

in a second die, adjacent the first die:

second active circuitry in and on the semiconductor substrate, wherein the plurality of interconnect layers is over the second active circuitry;

a second plurality of interconnect pads over the top surface of the plurality of interconnect layers, wherein each interconnect pad of the second plurality of interconnect pads is coupled to the second active circuitry through the plurality of interconnect layers;

a second contiguous seal ring surrounding the second active circuitry and extending vertically from the substrate to the top surface of the plurality of interconnect layers;

a second plurality of fuses, wherein each fuse of the second plurality of fuses has a first terminal coupled to a corresponding interconnect pad of the second plurality of interconnect pads through the plurality of interconnect layers and a second terminal coupled to the second seal ring through at least one interconnect layer of the plurality of interconnect layers; and

a plated conductive layer on each interconnect pad of the second plurality of interconnect pads; and

a seal ring interconnect which connects the first contiguous seal ring to the second contiguous seal ring through at least one interconnect layer of the plurality of interconnect layers in a scribe street between the first and second die.

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