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(54) OFFSET COMPENSATION FOR SENSE AMPLIFIERS

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H03F 3/45 (2006.01)

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(58) **Field of Classification Search** 327/51, 327/52; 365/156
See application file for complete search history.

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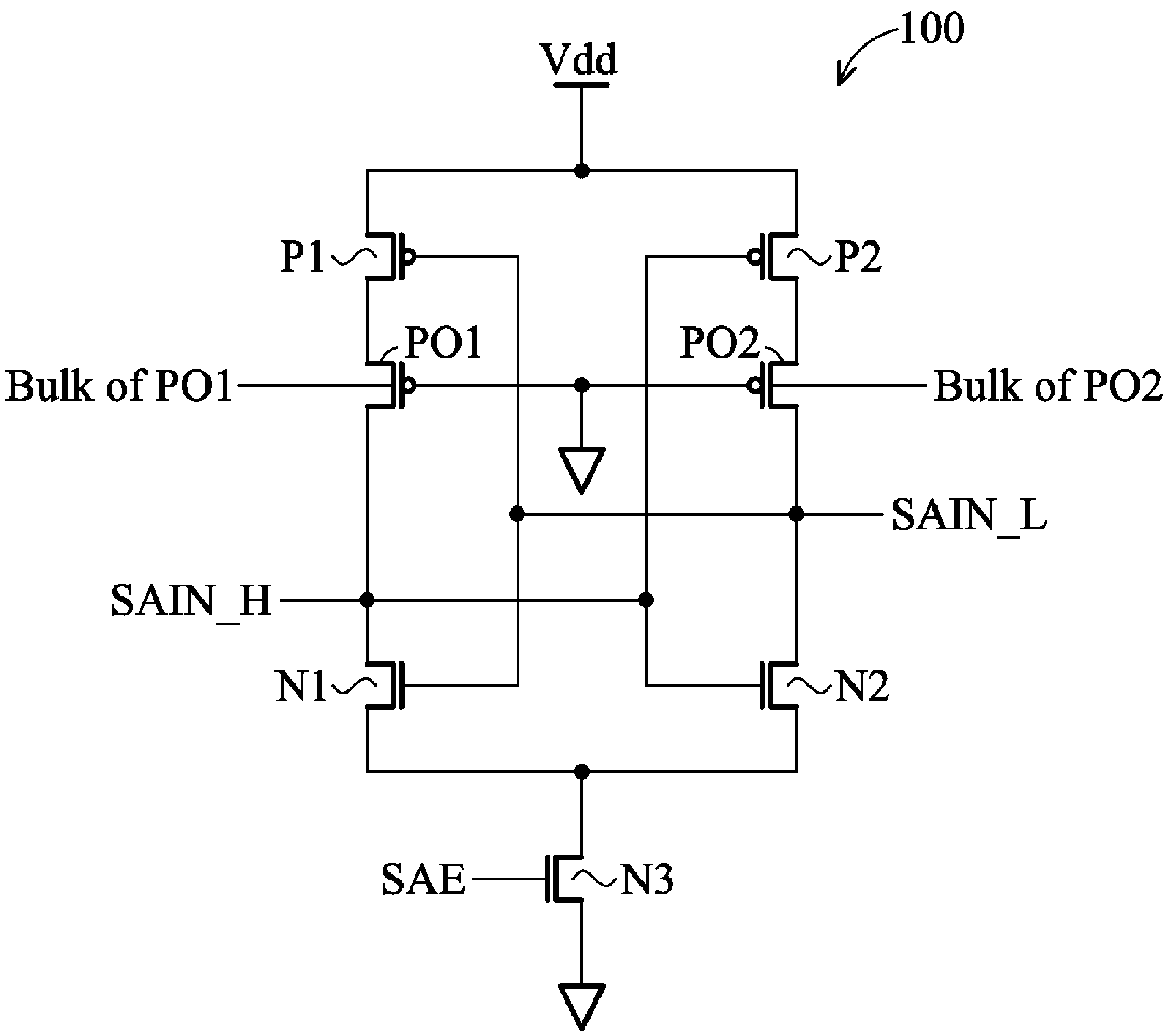
(57) ABSTRACT

A sense amplifier having compensation circuitry is described. The compensation circuitry includes at least one pair of compensation transistors. When compensation is desired, one or a combination of the bulk of the at least one pair of compensation transistors is provided with one or a combination of compensation voltages.

15 Claims, 5 Drawing Sheets



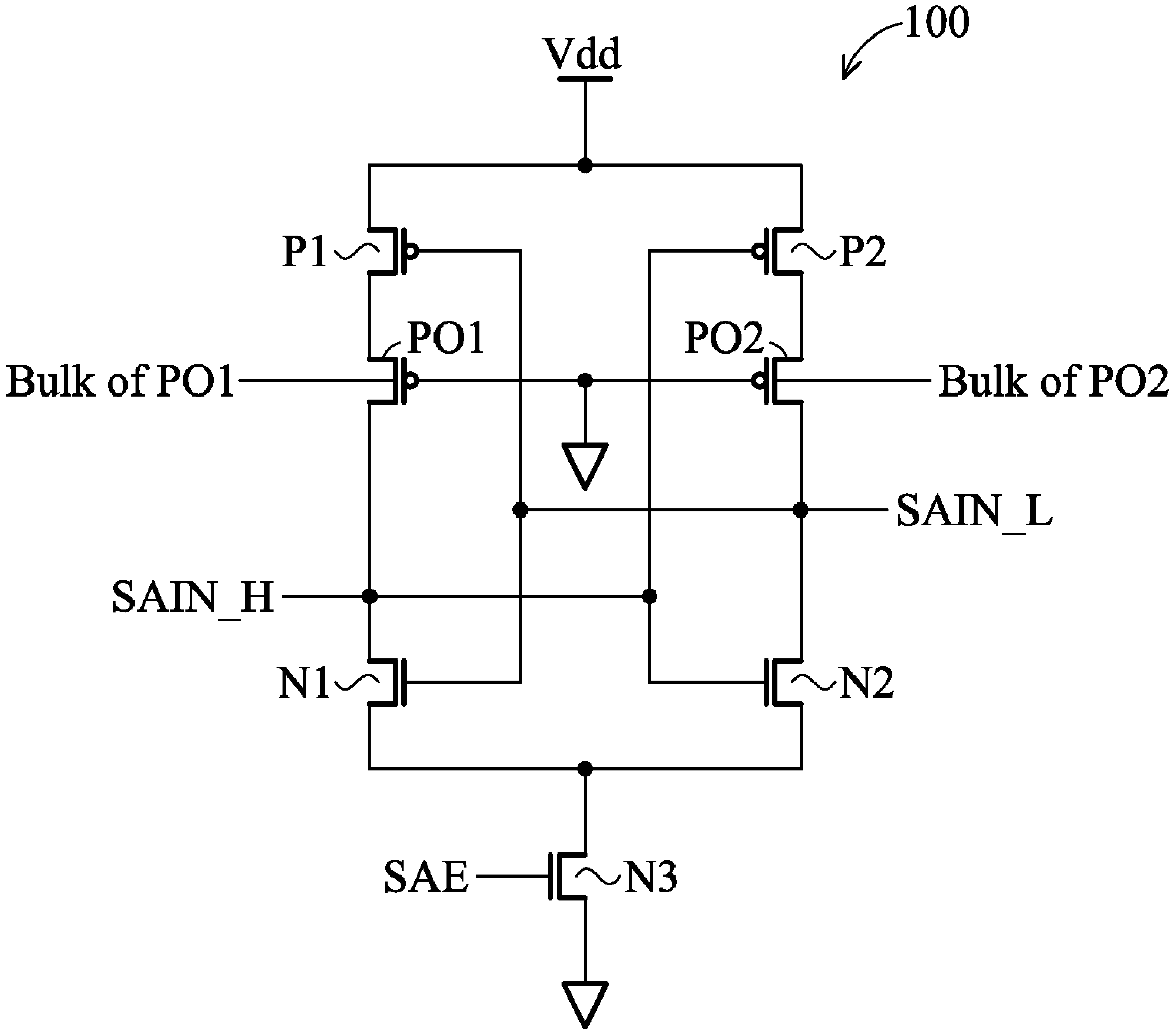

100
Vdd
P1
P2
PO1
PO2
Bulk of PO1
Bulk of PO2
SAIN_L
SAIN_H
N1
N2
SAE
N3

Fig. 1

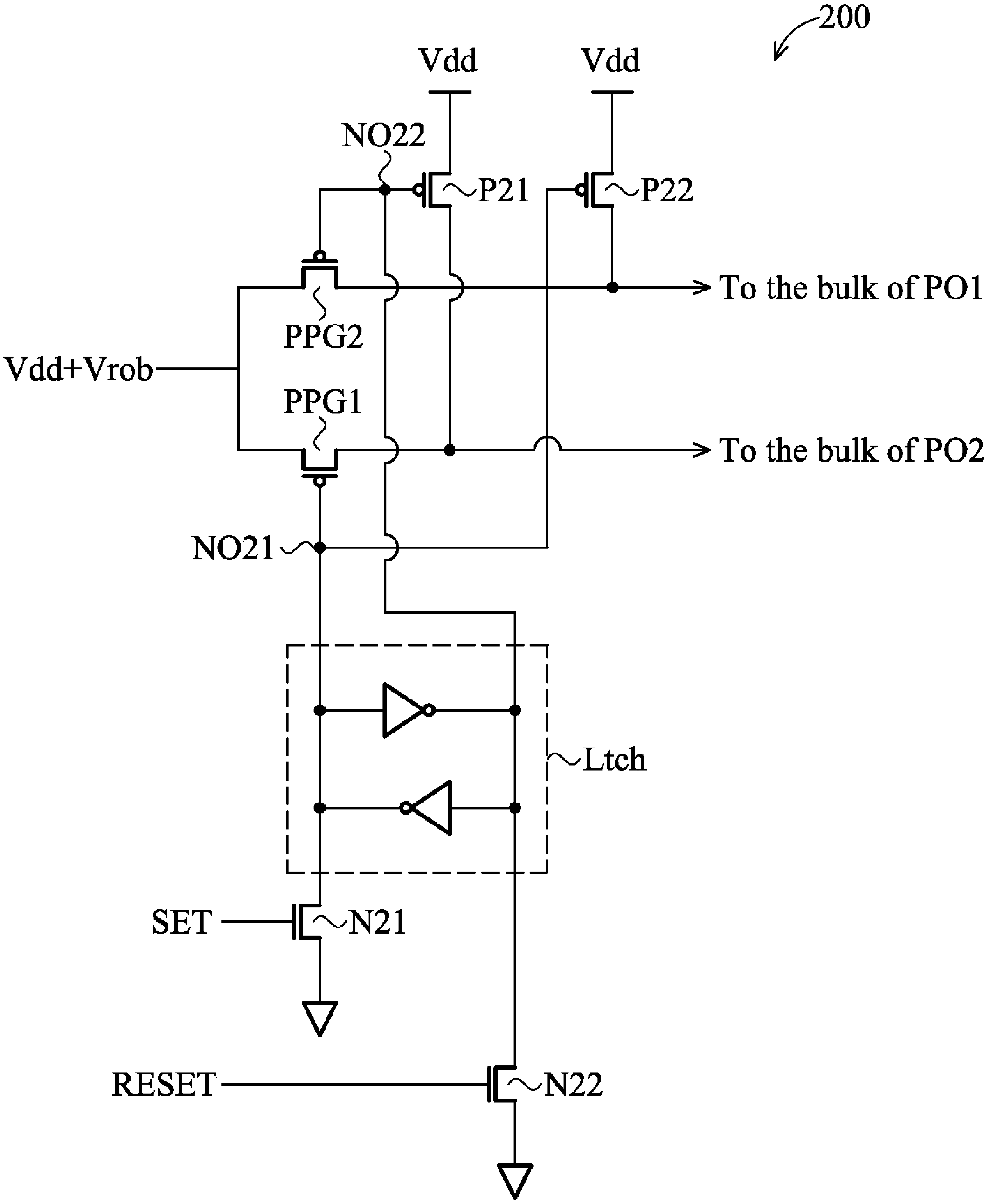

200
Vdd
Vdd
NO22
P21
P22
To the bulk of PO1
PPG2
Vdd+Vrob
PPG1
To the bulk of PO2
NO21
Ltch
SET
N21
RESET
N22

Fig. 2

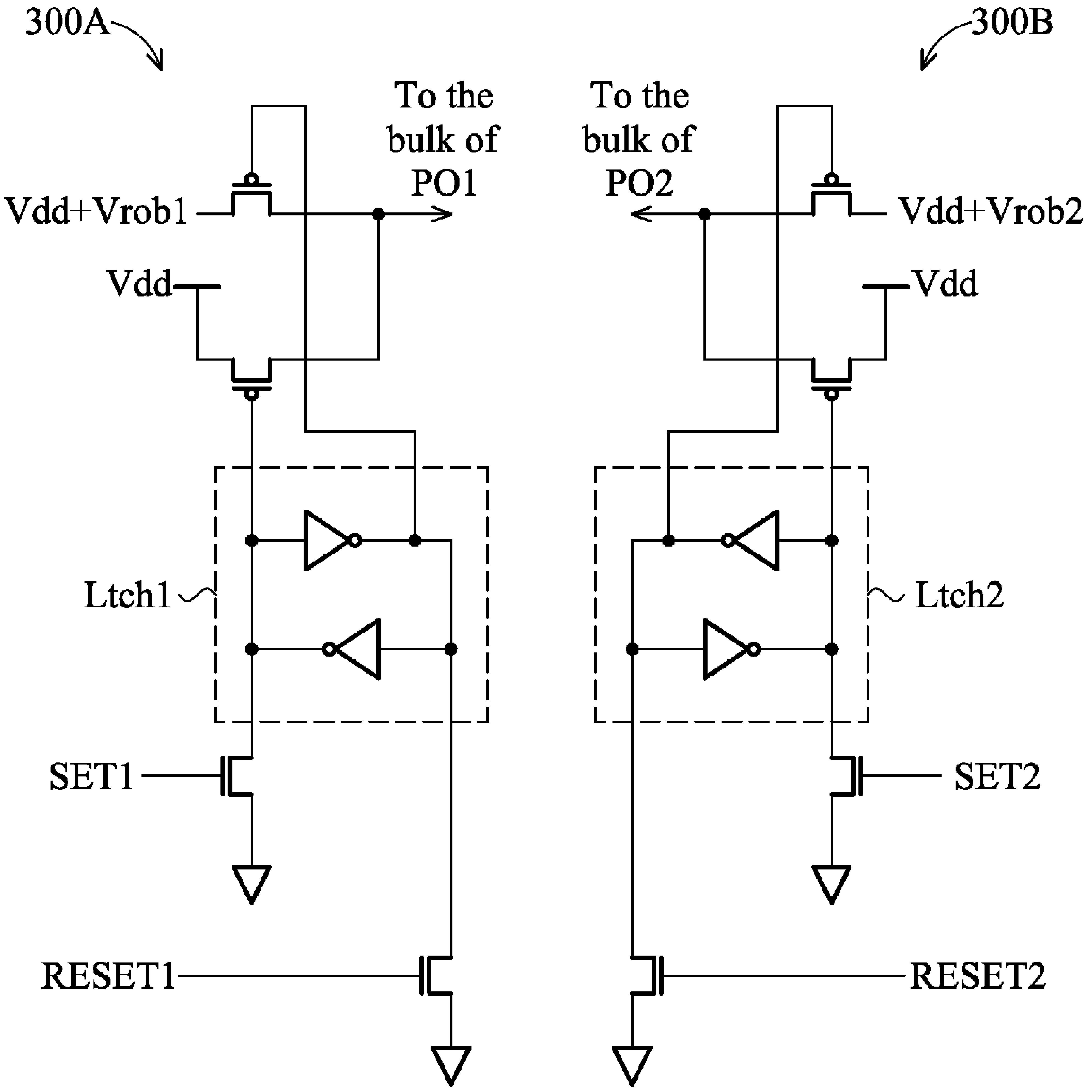

300A
300B
To the bulk of PO1
To the bulk of PO2
Vdd+Vrob1
Vdd+Vrob2
Vdd
Vdd
Ltch1
Ltch2
SET1
SET2
RESET1
RESET2

Fig. 3

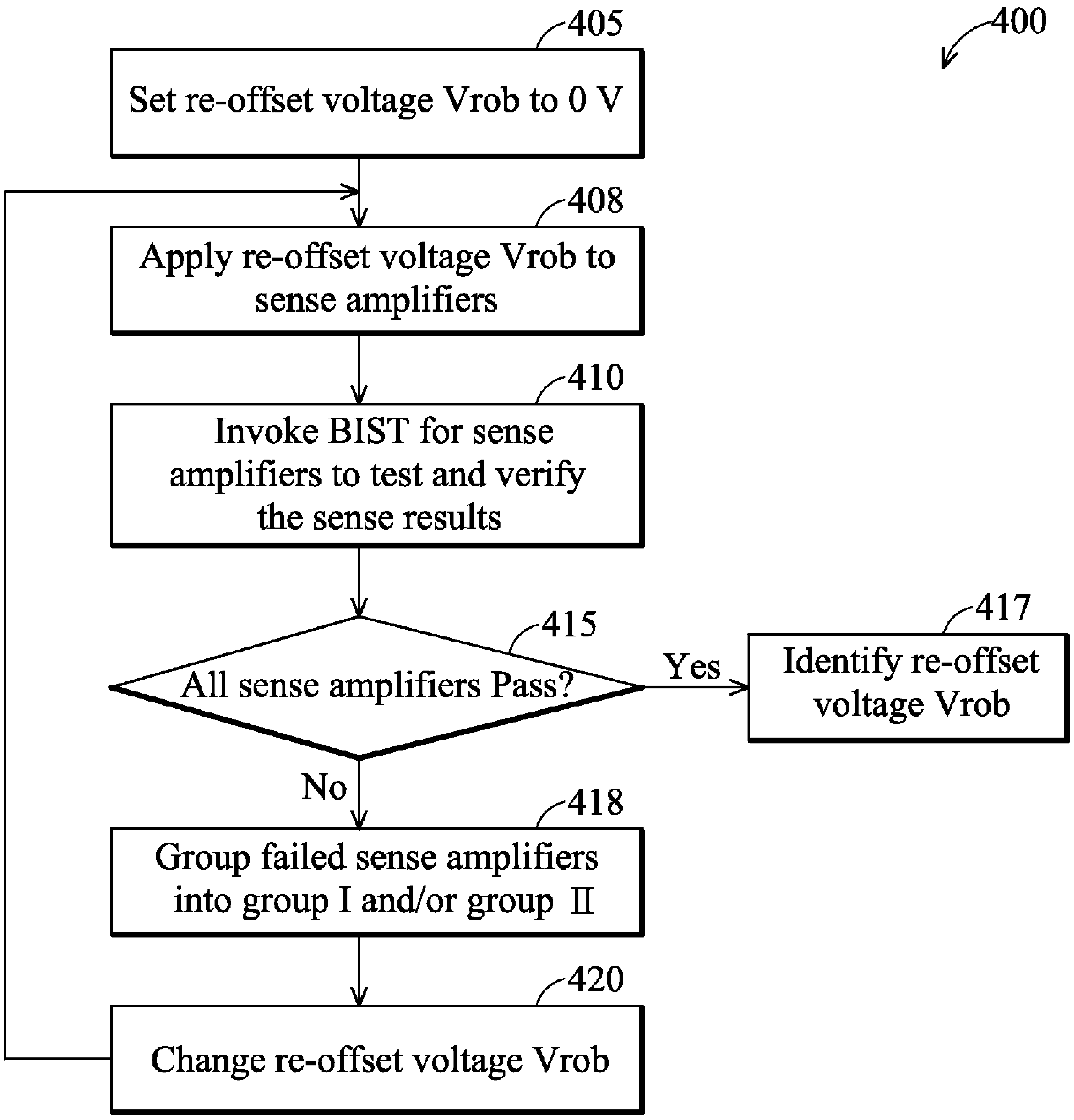

400
405
Set re-offset voltage Vrob to 0 V
408
Apply re-offset voltage Vrob to sense amplifiers
410
Invoke BIST for sense amplifiers to test and verify the sense results
415
All sense amplifiers Pass?
Yes
417
Identify re-offset voltage Vrob
No
418
Group failed sense amplifiers into group I and/or group II
420
Change re-offset voltage Vrob

Fig. 4

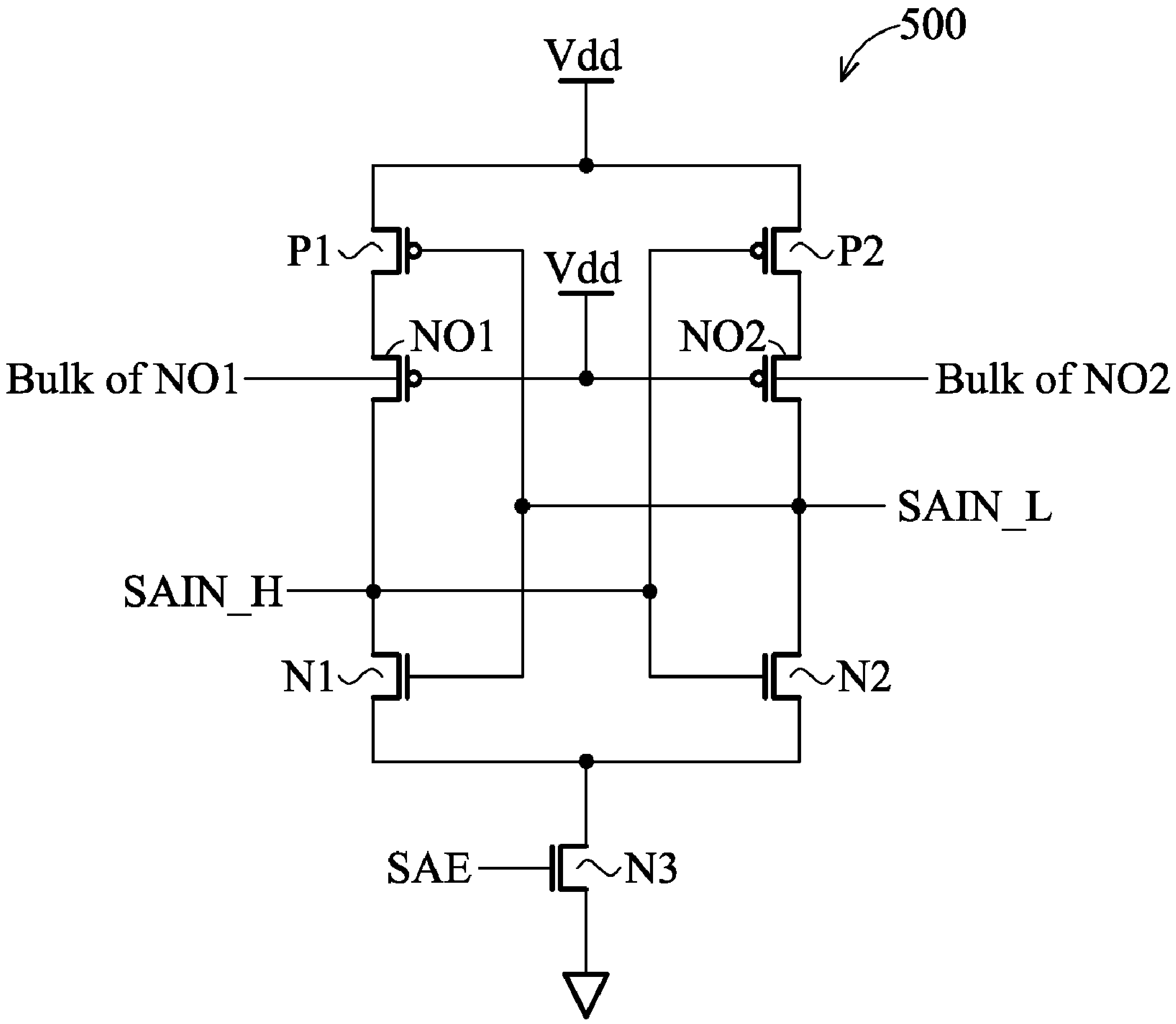

500
Vdd
P1
Vdd
P2
NO1
NO2
Bulk of NO1
Bulk of NO2
SAIN_L
SAIN_H
N1
N2
SAE
N3

Fig. 5

OFFSET COMPENSATION FOR SENSE AMPLIFIERS

TECHNICAL FIELD

The present disclosure is generally related to sense amplifiers, and, more particularly, to offset compensation for sense amplifiers.

BACKGROUND

A sense amplifier (SA) is used to sense the difference between two signals at two inputs of the sense amplifier, and amplify the difference or, commonly stated, amplify the differential signal across the inputs. To sense correctly, a sense margin, which is the minimum difference between the two signals, or the minimum differential signal, is required.

In many situations, process variation causes two different threshold voltages to be present in two transistors that are supposed to be the same (e.g., two NMOS transistors of a cross latch of an amplifier). In that situation, the sense amplifier is said to have an offset at the two inputs caused by the mismatch of the two transistors. As a result, the sense amplifier favors reading one logic state versus another logic state, instead of neutrally providing the sensed data. For example, some sense amplifiers, when sensing the differential signal across two inputs, tend to favor a high logic level, (e.g., a High) while some other sense amplifiers tend to favor a low logic level (e.g., a Low). A sense amplifier tending to favor a High quickly provides the High as the read data at the output when the actual High data is sensed, but slowly provides a Low as the read data at the output when the actual Low data is sensed. Similarly, a sense amplifier tending to favor a Low quickly provides the Low when the actual Low data is sensed, but slowly provides a High when the actual High data is sensed.

In effect, because of the process variation, the mismatch manifests as an additional offset, which causes the sense amplifier to require a larger sense margin to correctly sense the data. In applications where one sense margin is used for many amplifiers, a larger value for the sense margin is utilized so that a very high percentage, or all, of the sense amplifiers function correctly. As the large sense margin is used, the time required for the differential signal to develop increases, making the overall memory access speed slower.

BRIEF DESCRIPTION OF THE DRAWINGS

The details of one or more embodiments of the disclosure are set forth in the accompanying drawings and the detailed description below. Other features and advantages will be apparent from the detailed description, drawings, and claims.

FIG. **1** is a diagram of a sense amplifier having compensation circuitry, in accordance with some embodiments.

FIG. **2** is a diagram of a circuit illustrating a first mechanism to compensate for the offset of the sense amplifier in FIG. **1**, in accordance with some embodiments.

FIG. **3** is a diagram of a circuit illustrating a second mechanism to compensate for the offset of the sense amplifier in FIG. **1**, in accordance with some embodiments.

FIG. **4** is a flow chart illustrating a method of compensating the offset for a plurality of the sense amplifiers used in a memory, in accordance with some embodiments.

FIG. **5** is a diagram of a sense amplifier having compensation circuitry, in accordance with some further embodiments.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Embodiments, or examples, illustrated in the drawings are disclosed below using specific language. It will nevertheless be understood that the embodiments and examples are not intended to be limiting. Any alterations and modifications in the disclosed embodiments, and any further applications of the principles disclosed in this document are contemplated as would normally occur to one of ordinary skill in the pertinent art. Reference numbers may be repeated throughout the embodiments, but they do not require that feature(s) of one embodiment apply to another embodiment, even if they share the same reference number.

Some embodiments can have one or a combination of the following features and/or advantages. The re-offset voltage provided to the bulks of the compensation transistors reduces the sense margin. As a result, the memory access time is improved.

Exemplary Sense Amplifiers with Compensation Mechanisms

FIG. **1** is a diagram of a sense amplifier (SA) **100**, in accordance with some embodiments. In some embodiments, sense amplifier **100** is used in memory arrays, but SA **100** can be used in other circuits where a small signal difference is to be amplified, including, for example, an IO interface. In some memory applications, multiple memory cells on a column share the same amplifier.

SA **100** senses a high logic level (e.g., a High) at output Out when the voltage value at input SAIN_H is greater than the voltage value at input SAIN_L. Similarly, SA **100** senses a low logic level (e.g., a Low) at output Out when the voltage value at input SAIN_H is lower than the voltage value at input SAIN_L. Transistor N**3** operates as a switch and serves as a current path for SA to be turned on/off. For example, when signal SAE is applied with a High, transistor N**3** turns on, and provides a current path for SA **100** to turn on. In contrast, when signal SA is applied with a Low, transistor N**3** turns off, and SA **100** turns off because there is no current path.

In some embodiments, for various reasons, including device manufacturing process variations, transistor N**1** and transistor N**2** are not exactly the same (i.e., mismatched). As a result, transistor N**1** has a threshold voltage (e.g., threshold voltage Vthn**1**) different from that of transistor N**2** (e.g., threshold voltage Vthn**2**), which causes an offset at inputs SAIN_H and SAIN_L. Because of the mismatch in the transistors, or the offset, at inputs SAIN_H and SAIN_L, sense amplifier **100** favors reading a logic state versus another logic state, instead of neutrally providing the sensed data. For example, if voltage Vthn**1** is greater than voltage Vthn**2**, then SA **100** favors reading a Low on node SAIN_H when node SAIN_H serves as an output. If voltage Vthn**1** is less than voltage Vthn**2**, then SA **100** favors reading a High on node SAIN_H when node SAIN_H serves as an output. For illustration, voltage ΔVth represents the difference between threshold voltage Vthn**1** and threshold voltage Vthn**2**. Voltage ΔVth is positive if voltage Vthn**1** is greater than voltage Vthn**2**, and voltage ΔVth is negative if voltage Vthn**1** is less than voltage Vthn**2**. Further, voltage ΔInput represents the offset at inputs SAIN_H and SAIN_L corresponding to voltage ΔVth. In some embodiments, mechanisms are provided to compensate (e.g., reduce, cancel, re-offset, etc.) the effect of the threshold voltage offset (e.g., the voltage difference)

ΔVth, and after the threshold offset ΔVth is re-offset, the input voltage offset caused by the threshold offset is reduced or canceled (e.g., re-offset). For simplicity of illustration, reducing or re-offsetting the offset described in this document could cancel the offset altogether.

PMOS transistors **PO1** and **PO2** are commonly called compensation transistors, and serve to re-offset (e.g., cancel, reduce, compensate, etc.) the offset caused by the mismatch between transistors **N1** and **N2**. When compensation is desired, one or a combination of the bulk of transistor **PO1** and **PO2** is provided with one or a combination of bulk re-offset voltages (e.g., Vrob, Vrob**1**, Vrob**2** illustrated below) that compensates for the mismatch. Alternatively stated, the bulk re-offset voltage(s) cancels the input offset at the corresponding input SAIN_H and/or SAIN_L. In some embodiments, the gates of transistors PO1 and PO2 are coupled together and to ground (e.g., Low) so that transistors PO1 and PO2 are turned on for re-offsetting. In the following explanation, for ease of discussion, when one re-offset voltage is provided to the bulk of one PMOS transistor (e.g., transistor PO**2**), the bulk of the other PMOS transistor (e.g., transistor PO**1**) remains the same (e.g., at voltage Vdd).

In some embodiments, if voltage Vthn**1** is greater than voltage Vthn**2** (e.g., voltage ΔVth is positive, and sense amplifier **100** favors reading a Low), a negative bulk re-offset voltage Vrob is provided to the bulk of transistor PO**2**, which cancels the offset at inputs SAIN_L and SAIN_H that corresponds to the threshold voltage difference ΔVth. But if voltage Vthn**1** is less than voltage Vthn**2** (e.g., voltage ΔVth is negative, and sense amplifier **100** favors reading a Low), a negative bulk re-offset voltage Vrob is provided to the bulk of transistor PO**1**, which also cancels the offset at inputs SAIN_L and SAIN_H corresponding to the threshold voltage difference ΔVth. Once voltage Vrob is provided to the bulk of transistor PO**2** or transistor PO**1**, the threshold voltage of the corresponding transistor (e.g., voltage Vthp**2** or voltage Vthp**1**) changes, which re-offsets the offset caused by the mismatch (e.g., the difference in the threshold voltages) between transistors N**1** and N**2**.

In some embodiments, the mismatch between transistors N**1** and N**2** causing the offset exists after sense amplifier **100** is manufactured, and the difference in the threshold voltage ΔVth is identified by a Monte Carlos simulation. Based on the identified ΔVth, the re-offset voltage Vrob is determined and provided to the bulk of the corresponding transistor PO**1** or PO**2**.

In some embodiments, a plurality of sense amplifiers (e.g., sense amplifiers **100**) is used in a circuit (e.g., in a memory array), and the minimum sense margin (e.g., Smin) for the plurality of sense amplifiers is known. For example, the minimum sense margin Smin is the mean of the sense margins of all sense amplifiers plus three sigma. The sense amplifiers are then configured to sense some known data based on the known (i.e., pre-determined) sense margin. In some embodiments related to a memory array, a built-in self test (BIST) is used to test the sense amplifiers used in the memory array. For example, for each sense amplifier the minimum read margin is set for the sense amplifier, the BIST is invoked for the sense amplifier to test itself using a specific input data (e.g., a Low or a High). The test result is compared against the expected test data from which the sense amplifiers are classified into a group of sense amplifiers favoring reading a High (e.g., group I) and/or another group of sense amplifiers favoring reading a Low (e.g., group II).

For example, sense amplifiers that are supposed to provide a Low after sensing, but provide the failed data, reveal that the sense amplifiers favor reading a High and thus are classified into group I. Similarly, sense amplifiers that are supposed to provide a High after sensing but failed the sensing reveal that those amplifiers favor reading a Low and are classified into group II. For each sense amplifier in group I, a corresponding positive bulk re-offset voltage Vrob is provided to the bulk of transistor PO**2**, which, in effect, provides the input re-offset to input SAIN_L. At the same time, the bulk of each transistor PO**2** in group I remains unchanged, e.g., at voltage Vdd. Similarly, for each sense amplifier in group II, a corresponding bulk re-offset voltage Vrob is provided to the bulk of transistor PO**1**, which, in effect, provides the input re-offset to input SAIN_H. At the same time, the bulk of each transistor PO**1** in group II remains unchanged, e.g., at voltage Vdd.

In some embodiments, re-offset voltage Vrob is calculated based on the difference in the threshold voltage of transistor N**1** (e.g., Vthn**1**) and that of transistor N**2** (e.g., Vthn**2**), e.g., voltage ΔVt. If voltage ΔVt is 0, then the offset is 0, and re-offset voltage Vrob is 0 V. But if voltage ΔVt is not 0, voltage ΔVt is used to generate the difference in threshold voltages of transistors PO**1** and PO**2** (e.g., ΔVtp) to re-offset the voltage difference ΔVt of transistors N**1** and N**2**, by, for example, changing one or a combination of the threshold voltage of transistors PO**1** and PO**2**. For example, if ΔVt is 100 mV, then the threshold voltage of transistor PO**1** (e.g., voltage Vthpo**1**) is configured to change by 100 mV, while the threshold voltage of transistor PO**2** (e.g., voltage Vthpo**2**) remains unchanged, or voltage Vthpo**2** of transistor PO**2** is configured to change by −100 mV while voltage Vthpo**1** of transistor PO**1** remains unchanged. Alternatively, voltage Vthpo**1** is configured to change by 40 mV, 50 mV, or 60 mV, and voltage Vthpo**2** is configured to change by −60 mV, −50 mV, and −40 mV, etc., respectively. For illustration, the threshold voltage of transistors PO**2** is adjusted. In other words, threshold voltage Vthpo**2** is changed by −ΔVtp where ΔVtp=ΔVt. In some embodiments, ΔVtp is generated by providing negative voltage Vrob to the bulk of transistor PO**2**. Further, voltage Vrob is calculated based on the equation:

$$V_{TN}=V_{TO}+\gamma(\sqrt{V_{SB}+2\phi_F}-\sqrt{2\phi_F})$$

where V_{TN} is the threshold voltage of transistor PO**2** when the substrate bias is present, V_{SB} is the source-to-body substrate bias (e.g., Vrob), $2\phi_F$ is the surface potential, and V_{TO} is the threshold voltage for zero substrate bias and γ is the body effect parameter.

FIG. **1** is illustrated with the transistor PO**1** coupled between transistors P**1** and N**1**, and transistor PO**2** coupled between transistors P**2** and N**2**. Various embodiments are not so limited. Transistor PO**1** can be coupled between voltage Vdd and transistor P**1** while transistor PO**2** can be coupled between voltage Vdd and transistor P**2**. The sign of re-offset voltage Vrob, however, is changed accordingly, as recognizable by persons of ordinary skilled in the art. For example, when voltage Vthn**1** is greater than voltage Vthn**2** (e.g., voltage ΔVth is positive), a corresponding positive re-offset voltage Vrob is applied at the bulk of transistor PO**2**, and when voltage Vthn**2** is less than voltage Vthn**2** (e.g., voltage ΔVth is negative), a corresponding positive re-offset voltage Vrob is applied at the bulk of transistor PO**1**, etc.

Exemplary Offset Circuits

FIG. **2** is a diagram of a circuit **200** illustrating offset compensation for SA **100**, in accordance with some embodiments. In this illustration, the bulk of one transistor (e.g., transistor PO**1** or PO**2**) remains the same (e.g., at voltage Vdd) while the bulk of the other transistor is provided with bulk re-offset voltage Vrob. In some embodiments, the bulk of PMOS transistors without a re-offset is set at voltage Vdd, and the bulk of the transistor receiving the offset is provided with voltage Vdd+Vrob to provide the re-offset voltage Vrob. For example, if the re-offset is for transistor PO**2**, then the bulk of transistor PO**2** is provided with Vdd+Vrob, while the bulk of transistor PO**1** remains the same at voltage Vdd. Similarly, if the re-offset is to transistor PO**1**, then the bulk of transistor PO**1** is provided with Vdd+Vrob, while the bulk of transistor PO**2** remains the same at voltage Vdd. In some embodiments, re-offsetting to the bulk of transistor PO**2** with a re-offset voltage value Vrob results in a re-offset at input SAIN_L with a corresponding voltage value Vroi. Similarly, re-offsetting to the bulk of transistor PO**1** with a re-offset voltage value results in a re-offset at input SAIN_H with a corresponding voltage value Vroi.

In FIG. **2**, when signal SET is activated (e.g., applied with a High), NMOS transistor N**21** turns on, which pulls node NO**21**, which is the drain of transistor N**21**, to ground (e.g., Low). As a result, transistor PPG**1** is turned on, and voltage Vdd+Vrob is passed through transistor PPG**1** to the bulk of transistor PO**2**. In effect, the bulk of transistor PO**2** is provided with a re-offset voltage value of Vrob. Node NO**21** pulled low also causes transistor P**22** to turn on, which transfers voltage Vdd at the source of transistor P**22** to the drain of transistor P**22** or to the bulk of transistor PO**1**.

Similarly, when signal RESET is activated (e.g., applied with a High), NMOS transistor N**22** turns on, which pulls node NO**22**, which is the drain of transistor N**22**, to ground (e.g., Low). As a result, transistor PPG**2** is turned on, and voltage Vdd+Vrob is passed through transistor PPG**2** to the bulk of transistor PO**1**. In effect, the bulk of transistor PO**1** is provided with a re-offset voltage value of Vrob. Node NO**22** being Low also causes transistor P**21** to turn on, which transfers voltage Vdd at the source of transistor P**21** to the drain of transistor P**21** or to the bulk of transistor PO**2**.

Latch Ltch stores the value passed through transistors PPG**1** and PPG**2** at nodes NO**21** and NO**22**, respectively.

In the above illustration, the bulk of one transistor (e.g., transistor PO**1** or PO**2**) is re-offset and the bulk of the other transistor remains the same. In some embodiments, the bulks of both transistors PO**1** and PO**2** are re-offset. FIG. **3** is a diagram of a circuit **300** illustrating re-offsetting to the bulk of both transistors PO**1** and PO**2**. In this illustration, the bulk of transistor PO**1** is re-offset with a first value, e.g., voltage Vrob**1**, by a sub-circuit **300**A, and the bulk of transistor PO**2** is re-offset with a second value, e.g., voltage Vrob**2**, by a sub-circuit **300**B. Circuits **300**A and **300**B include similar components and operate in the same manner except circuit **300**A is used to re-offset the bulk of transistor PO**1** while circuit **300**B is used re-offset the bulk of transistor PO**2**. Further, a circuit **300**A or **300**B operates substantially the same as circuit **200**. For simplicity, only one circuit, e.g., circuit **300**A is described, and the operation of the other circuit, e.g., circuit **300**B, can be understood by a person of ordinary skill in the art. When there is no compensation or re-offset, signal SET**1** is activated, transistor PPG**1** is turned on and voltage Vdd is passed to the bulk of transistor PO**1**. But when a re-offset value, e.g., voltage Vrob**1** is desired, signal RESET**1** is activated, transistor PPG**2** is activated, and voltage Vdd+Vrob**1** is passed to the bulk of transistor PO**1**. In effect, the bulk of transistor PO**1** is re-offset with voltage Vrob**1**.

In circuit **300**, voltage Vrob**1** or voltage Vrob**2** is negative or positive, and the total re-offset by voltage Vrob**1** to the bulk of transistor PO**1** and voltage Vrob**2** to the bulk of transistor PO**2** is to reduce the effect of the mismatch between transistor N**1** and N**2**.

Exemplary Method of Re-Offsetting a Plurality of Sense Amplifiers

FIG. **4** is a flowchart illustrating a method **400** of re-offsetting a plurality of sense amplifiers used in a memory array, in accordance with some embodiments. Method **400**, however, can be used for sense amplifiers in other circuits.

In step **405**, re-offset voltage Vrob is set to 0 V.

In step **408**, re-offset voltage Vrob is applied to all sense amplifiers.

In step **410**, a BIST is invoked for the sense amplifiers to sense and verify the sense results of the sense amplifiers.

In step **415**, if all sense amplifiers pass, the applied voltage Vrob is identified as the desired re-offset voltage in step **417**. If, however, any of the amplifiers fails, the failed amplifiers are grouped into a first group favoring reading a High (e.g., group I) and/or a second group favoring reading a Low (e.g., group II) in step **418**.

In step **420**, re-offset voltage Vrob is changed (e.g., is decreased, for example, by −100 mV, in some embodiments), and the new re-offset voltage (e.g., voltage Vrobn) is applied in step **410**, in accordance with the identified groups. For example, for amplifiers in group I, voltage Vrobn is applied to the bulk of transistor PO**1** while, for amplifiers in group II, voltage Vrobn is applied to the bulk of transistors PO**2**. When all amplifiers pass (e.g., in step **415**), a first re-offset voltage (e.g., voltage Vrob**1**) is identified for group I, and a second re-offset voltage (e.g., voltage VrobII) is identified for group II, in step **417**.

In flow chart **400**, a sequential search (e.g., voltage Vrobn keeps decreasing) is used for illustration. However, other searches, including a binary search are within the scope of various embodiments.

Exemplary Sense Amplifier with Compensation Mechanisms—Some Further Embodiments

FIG. **5** is a diagram of a sense amplifier (SA) **500** having offset compensation circuitry, in accordance with some further embodiments. Compared with SA **100**, SA **500** includes two NMOS transistors NO**1** and NO**2** that replace PMOS transistors PO**1** and PO**2**, respectively. The gates of transistors NO**1** and NO**2**, however, are coupled to voltage Vdd (e.g., a High) plus Vthn, the threshold voltage of transistors NO**1** and NO**2**, so that transistors NO**1** and NO**2** are turned on for re-offsetting. Further, the drains of transistors NO**1** and NO**2** are coupled to the drains of transistors P**1** and P**2**, respectively, and the source of transistors NO**1** and NO**2** are coupled to the drains of transistor N**1** and N**2**, respectively.

The re-offset operation of transistors NO**1** and NO**2** is substantially the same as that of transistors P**01** and P**02**. For example, when voltage Vthn**1** is greater than voltage Vthn**2** (e.g., voltage ΔVth is positive), a corresponding positive re-offset voltage Vrob is applied at the bulk of transistor NO**2**, and when voltage Vthn**1** is less than voltage Vthn**2** (e.g., voltage ΔVth is negative), a corresponding positive re-offset voltage Vrob is applied at the bulk of transistor N**01**, etc. Different techniques (e.g., having one or two re-offset voltages, negative and/or positive re-offset voltages, etc.) applicable to SA **100** are applicable to SA **500** as would be recognizable by a person of ordinary skill in the art.

FIG. **5** is illustrated with the transistor NO**1** coupled between transistors P**1** and N**1**, and transistor NO**2** coupled between transistors P**2** and N**2**. Various embodiments are not so limited. Transistor NO**1** can be coupled between transistor N**1** and transistor N**3** while transistor NO**2** can be coupled between transistor N**2** and transistor N**3**. The sign of re-offset voltage Vrob, however, is changed accordingly, as recognizable by persons of ordinary skilled in the art. For example, when voltage Vthn**1** is greater than voltage Vthn**2** (e.g., voltage ΔVth is positive), a corresponding negative re-offset voltage Vrob is applied at the bulk of transistor NO**2**, and when voltage Vthn**1** is less than voltage Vthn**2** (e.g., voltage ΔVth is negative), a corresponding negative re-offset voltage Vrob is applied at the bulk of transistor NO**1**, etc.

In the above illustration (e.g., FIG. **1** and FIG. **5**), one pair of transistors (e.g., the pair of transistor PO**1** and PO**2** or the pair of transistor NO**1** and NO**2**) is used. Combinations of pairs of transistors are within the scope of various embodiments, and are recognizable by persons of ordinary skill in the art. For example, a pair of NMOS transistors NO**1** and NO**2** can be added to circuit **100** by having transistor NO**1** coupled between transistor PO**1** and transistor N**1** or between transistor N**1** and transistor N**3**, and transistor NO**2** coupled between transistor PO**2** and transistor N**2** or between transistor N**2** and transistor N**3**. Similarly, a pair of PMOS transistors PO**1** and PO**2** can be added to circuit **500** by having transistor PO**1** coupled between transistor P**1** and voltage Vdd node and transistor PO**2** coupled between transistor P**2** and voltage Vdd node, etc.

A number of embodiments have been described. It will nevertheless be understood that various modifications may be made without departing from the spirit and scope of the disclosure. For example, the various transistors being shown as a particular dopant type (e.g., NMOS and PMOS) are for illustration purposes, embodiments of the disclosure are not limited to a particular type, but the dopant type selected for a particular transistor is a design choice and is within the scope of various embodiments. The logic level (e.g., low or high) of the various signals used in the above description is also for illustration purposes, various embodiments are not limited to a particular level when a signal is activated and/or deactivated, but, rather, selecting such a level is a matter of design choice. In some embodiments, a source/drain is used for either a source or a drain of a transistor.

Some embodiments are described as having one bulk voltage re-offset applied at a bulk of one transistor PO**1** or PO**2**, and some embodiments are described as having two bulk re-offset voltages applied at the bulks of both transistors PO**1** and PO**2**. Various embodiments of the invention are not limited to a particular mechanism of re-offsetting by using one or two bulk re-offset voltages. Selecting one or two re-offset voltages is a design choice and is within the scope of the various embodiments. In various embodiments, when a re-offset is applied, the re-offset value is either positive or negative and can be applied to a corresponding transistor. For example, in the above illustration, when voltage Vthn**1** is greater than voltage Vthn**2**, a negative re-offset voltage Vrob is applied to the bulk of transistor PO**2**. Alternatively, a positive re-offset of the same value can be applied to the bulk of transistor PO**1**. Various embodiments are not limited to a positive or a negative value, nor applying to one particular transistor. For example, when a bulk re-offset voltage corresponding to voltage ΔVth is identified, the re-offset voltage can be applied to a particular transistor, or the same negative offset can be applied to the other transistor, or the bulk re-offset can be split into two and applied to both transistors. For example, the bulk re-offset is Vrob identified, from which ½ Vrob can be applied to the bulk of a transistor (e.g., transistor PO1) and −½ Vrob can be applied to the bulk of the other transistor (e.g., transistor PO2), etc.

Some embodiments regard an amplifier that comprises a first PMOS transistor having a first PMOS drain, a first PMOS gate, and a first PMOS source; a second PMOS transistor having a second PMOS drain, a second PMOS gate, and a second PMOS source; a first NMOS transistor having a first NMOS drain, a first NMOS gate, and a first NMOS source; a second NMOS transistor having a second NMOS drain, a second NMOS gate, and a second NMOS source; a first compensation transistor having a first compensation drain, a first compensation gate, a first compensation source, and a first compensation bulk; a second compensation having a second compensation drain, a second compensation gate, a second compensation source, and a second compensation bulk. The first compensation transistor is coupled to the first PMOS drain and the first NMOS drain. The second compensation transistor is coupled to the second PMOS drain and the second NMOS drain. The second PMOS gate, the second NMOS gate, and the first NMOS drain are coupled together, and serve as a first data input for the sense amplifier. The first PMOS gate, the first NMOS gate, and the second NMOS drain are coupled together, and serve as a second data input for the sense amplifier. The first compensation transistor bulk serves as a first compensation input for the sense amplifier and the second compensation transistor bulk serves as a second compensation input for the sense amplifier.

Some embodiments regard a method of compensating a sense amplifier. The method includes the following steps: determining whether there is a mismatch between a first transistor N**1** of the amplifier and a second transistor N**2** of the amplifier; and applying a compensation voltage value to one or a combination of a first bulk of a first compensation transistor PO**1** of the amplifier and a second bulk of a second compensation transistor PO**2** of the amplifier, if there is the mismatch and while the first compensation transistor and the second compensation transistor are on. The first compensation transistor PO**1** is coupled between the first transistor N**1** and a third transistor P**1** of the amplifier. The second compensation transistor PO**2** is coupled between the second transistor N**2** and a fourth transistor P**2** of the amplifier. A gate of the second transistor and a gate of the fourth transistor are coupled together and form a first data input for the amplifier. A gate of the third transistor and a gate of the first transistor are coupled together and form a second data input for the amplifier. Applying the compensation voltage value causes a reduction in a voltage difference between a first threshold voltage of the first transistor and a second threshold voltage of the second transistor.

Some embodiments regard a method of re-offsetting a plurality of amplifier. The method includes testing the plurality of amplifiers based on a re-offset value at bulks of compensation transistors of the plurality of amplifiers; identifying a first group of first amplifiers of the plurality of amplifiers favoring reading a first logic level and/or a second group of second amplifiers of the plurality of amplifiers favoring reading a second logic level different from the first logic level, based on results of the testing step; changing the re-offset value to a new re-offset value; re-offsetting the first group of first amplifiers and/or the second group of second amplifiers based on the new re-offset value; and re-testing the first group of first amplifiers and the second group of second amplifiers.

The above methods show exemplary steps, but they are not necessarily performed in the order shown. Steps may be added, replaced, changed order, and/or eliminated as appropriate, in accordance with the spirit and scope of disclosed embodiments.

What is claimed is:

1. A sense amplifier comprising:

a first PMOS transistor having a first PMOS drain, a first PMOS gate, and a first PMOS source; a second PMOS transistor having a second PMOS drain, a second PMOS gate, and a second PMOS source;

a first NMOS transistor having a first NMOS drain, a first NMOS gate, and a first NMOS source; a second NMOS transistor having a second NMOS drain, a second NMOS gate, and a second NMOS source;

a first compensation transistor having a first compensation drain, a first compensation gate, a first compensation source, and a first compensation bulk; and

a second compensation transistor having a second compensation drain, a second compensation gate, a second compensation source, and a second compensation bulk, wherein

the second PMOS gate, the second NMOS gate, and the first NMOS drain are coupled together, and serve as a first data input for the sense amplifier;

the first PMOS gate, the first NMOS gate, and the second NMOS drain are coupled together, and serve as a second data input for the sense amplifier;

the first compensation transistor is coupled between a power supply voltage node and the first PMOS transistor or between the first PMOS transistor and the first NMOS transistor or between the first NMOS transistor and a first node;

the second compensation transistor is coupled between the power supply voltage node and the second PMOS transistor or between the second PMOS transistor and the second NMOS transistor or between the second NMOS transistor and the first node;

the first compensation bulk serves as a first compensation input for the sense amplifier and the second compensation bulk serves as a second compensation input for the sense amplifier; and

a compensation voltage value is applied to one or a combination of the first compensation bulk and the second compensation bulk causing a voltage change between a first threshold voltage of the first compensation transistor and a second threshold voltage of the second compensation transistor.

2. The amplifier of claim **1**, wherein:

the first compensation transistor and the second compensation transistor are PMOS transistors; the first compensation transistor is coupled between the power supply voltage node and the first PMOS transistor or between the first PMOS transistor and the first NMOS transistor; and

the second compensation transistor is coupled between the power supply voltage node and the second PMOS transistor or between the second PMOS transistor and the second NMOS transistor.

3. The amplifier of claim **1**, wherein:

the first compensation transistor and the second compensation transistor are NMOS transistors; the first compensation transistor is coupled between the first PMOS transistor and the first NMOS transistor or between the first NMOS transistor and the first node; and

the second compensation transistor is coupled between the second PMOS transistor and the second NMOS transistor or between the second NMOS transistor and the first node.

4. The amplifier of claim **1**, wherein the first compensation input is configured to receive a first compensation value and the second compensation input is configured to receive a second compensation value, based on one or a combination of:

a voltage difference between a first NMOS threshold voltage of the first NMOS transistor and a second NMOS threshold voltage of the second NMOS transistor; a voltage difference between the first data input of the amplifier and the second data input of the amplifier; and first data sensed by the amplifier based on second data fed to the amplifier.

5. The amplifier of claim **4**, wherein the first compensation value or the second compensation value is zero.

6. The amplifier of claim **1** configured to satisfy at least one of the following conditions: the second compensation input is configured to receive a negative compensation voltage when a first NMOS threshold voltage of the first NMOS transistor is greater than a second NMOS threshold voltage of the second NMOS transistor, and the first compensation input is configured to receive a negative compensation voltage when the first NMOS threshold voltage of the first NMOS transistor is less than the second NMOS threshold voltage of the second NMOS transistor.

7. The amplifier of claim **1** configured to satisfy at least one of the following conditions: the first compensation input is configured to receive a positive compensation voltage, when a first NMOS threshold voltage of the first NMOS transistor is greater than a second NMOS threshold voltage of the second NMOS transistor, and the second compensation input is configured to receive a positive compensation voltage, when the first NMOS threshold voltage of the first NMOS transistor is less than the second NMOS threshold voltage of the second NMOS transistor.

8. The amplifier of claim **1**, wherein one or a combination of the first compensation input and the second compensation input is configured to receive a compensation voltage to reduce a voltage difference between a first threshold voltage of the first NMOS transistor and a second threshold voltage of the second NMOS transistor.

9. A method for compensating a sense amplifier, comprising:

turning on a first compensation transistor and a second compensation transistor of the sense amplifier; and

applying a compensation voltage value to one or a combination of a first bulk of the first compensation transistor and a second bulk of the second compensation transistor, if there is a mismatch between a first transistor of the amplifier and a second transistor of the amplifier; and wherein:

the first compensation transistor is electrically coupled to a first drain or a first source of the first transistor;

the second compensation transistor is electrically coupled to a second drain or a second source the second transistor;

a gate of a second transistor of the amplifier and a gate of the fourth transistor are coupled together and form a first data input for the amplifier; and

a gate of a third transistor of the amplifier and a gate of the first transistor are coupled together and form a second data input for the amplifier; and

applying the compensation voltage value causes a voltage change between a first threshold voltage of the first compensation transistor and a second threshold voltage of the second compensation transistor.

10. The method of claim **9** further comprising determining if there is a mismatch by having the sense amplifier provide first sensed data based on second data fed to the sense amplifier.

11. The method of claim **10**, wherein there is a mismatch if the first sensed data differs from the second fed data.

12. The method of claim **9**, wherein whether there is the mismatch is determined by using a built-in self test to determine if the amplifier provides expected data.

13. The method of claim **9**, wherein whether there is the mismatch is determined by determining whether there is the voltage difference between the first threshold voltage and the second threshold voltage.

14. The method of claim **9**, wherein applying a compensation voltage value to one or a combination of the first bulk and the second bulk includes applying a positive compensation voltage value to the second bulk while maintaining the first bulk at a same first bulk voltage level or applying a negative compensation voltage value to the first bulk and maintaining the second bulk at a same second bulk voltage level, if a voltage threshold of the first transistor is greater than a voltage threshold of the second transistor; or

applying a positive compensation voltage value to the first bulk and maintaining the second bulk at the same second bulk voltage level or applying a negative compensation voltage value to the second bulk and maintaining the first bulk at the same first bulk voltage level, if the voltage threshold of the first transistor is less than the voltage threshold of the second transistor.

15. The method of claim **9**, wherein:

the first transistor and the second transistor are NMOS transistors;

the third transistor and the fourth transistor are PMOS transistors; and the first compensation transistor and the second compensation transistor are NMOS transistors or PMOS transistors.

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