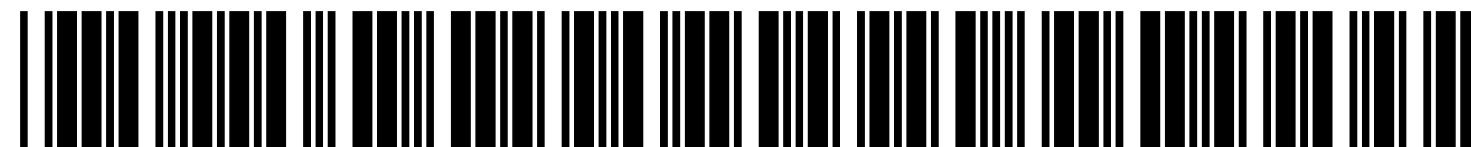
US008258570B2

(12) **United States Patent**
Anezaki

(10) **Patent No.: US 8,258,570 B2**
(45) **Date of Patent: Sep. 4, 2012**

(54) **SEMICONDUCTOR DEVICE**

(75) Inventor: **Toru Anezaki**, Kawasaki (JP)

(73) Assignee: **Fujitsu Semiconductor Limited**, Yokohama (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/179,038**

(22) Filed: **Jul. 8, 2011**

(65) **Prior Publication Data**

US 2011/0278659 A1 Nov. 17, 2011

Related U.S. Application Data

(62) Division of application No. 12/187,851, filed on Aug. 7, 2008, now Pat. No. 7,998,806.

(30) **Foreign Application Priority Data**

Aug. 10, 2007 (JP) 2007-209410

(51) **Int. Cl.**
H01L 29/788 (2006.01)

(52) **U.S. Cl.** **257/321**; 257/315; 257/316; 257/324; 257/E21.625; 257/E21.628

(58) **Field of Classification Search** 257/315, 257/316, 321, 324, E21.625, E21.628
See application file for complete search history.

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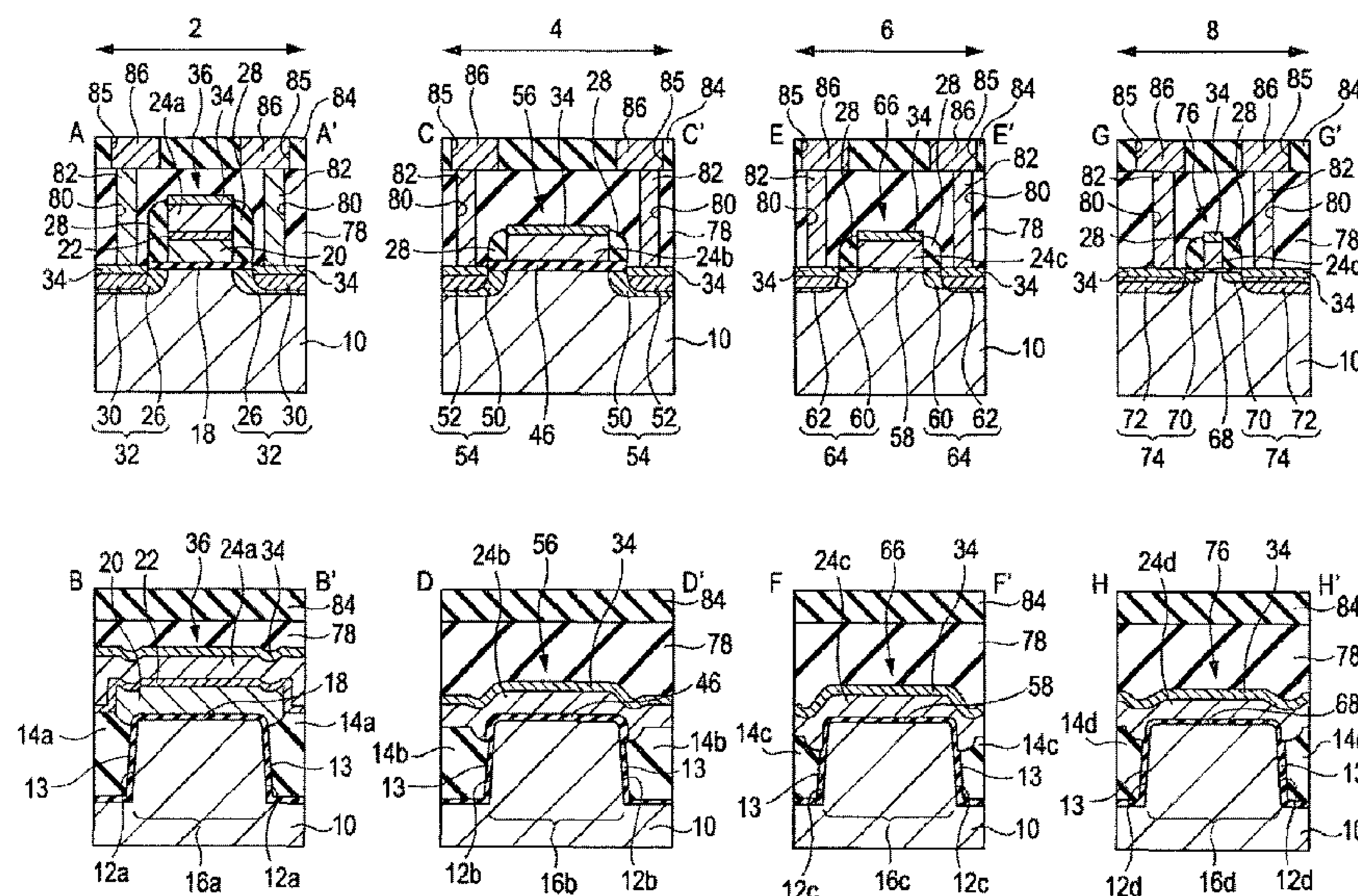
Primary Examiner — Andy Huynh
(74) *Attorney, Agent, or Firm* — Westerman, Hattori, Daniels & Adrian, LLP

(57) **ABSTRACT**

A semiconductor device includes a first gate insulating film over a first device region, a second gate insulating film over a second device region, a first gate electrode over the first gate insulating film, a second gate electrode over the second gate insulating film, first source and drain regions in the first device region at both sides of the first gate electrode, second source and drain regions in the second device region at both sides of the second gate electrode, and a memory cell memory cell that further includes a tunnel insulating film formed over a third device region, a floating gate formed over the tunnel insulating film, an insulating film formed over the floating gate, a control gate formed over the tunnel insulating film, and third source and drain regions formed in third device region at both sides of the floating gate and the control gate.

3 Claims, 59 Drawing Sheets



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Japanese Office Action dated Jul. 3, 2012 (mailing date), issued in corresponding Japanese Application No. 2007-209410, with English Translation (total 4 pages).

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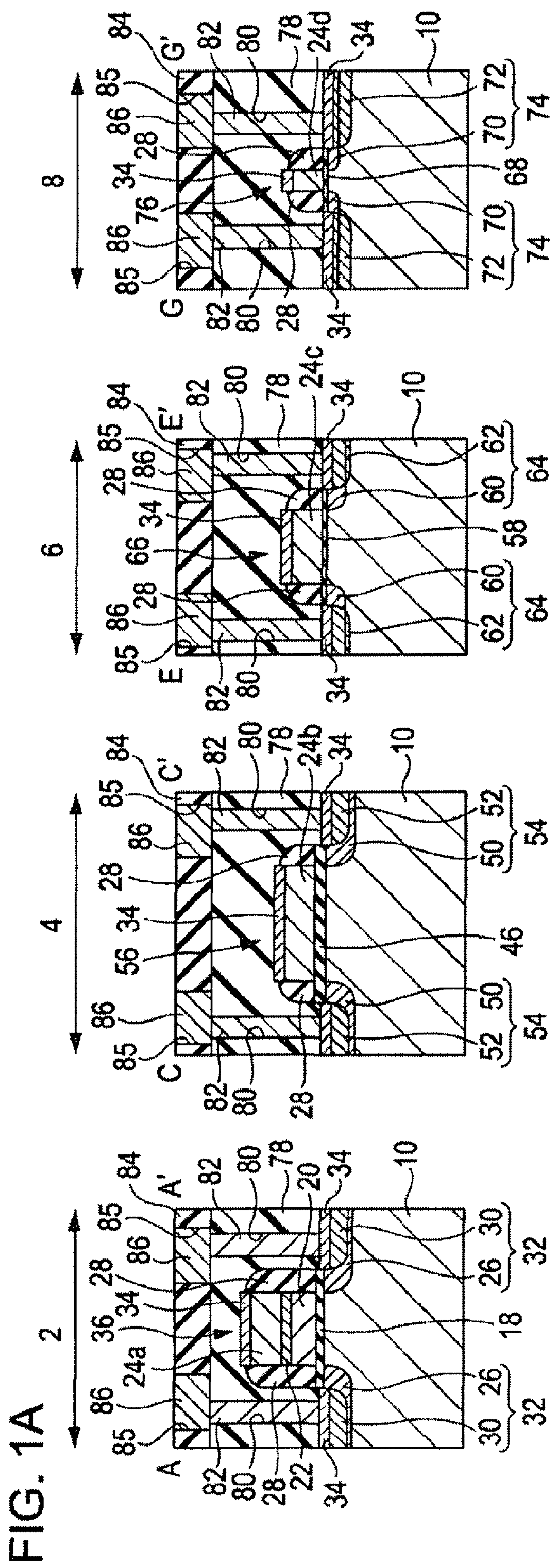


FIG. 1A

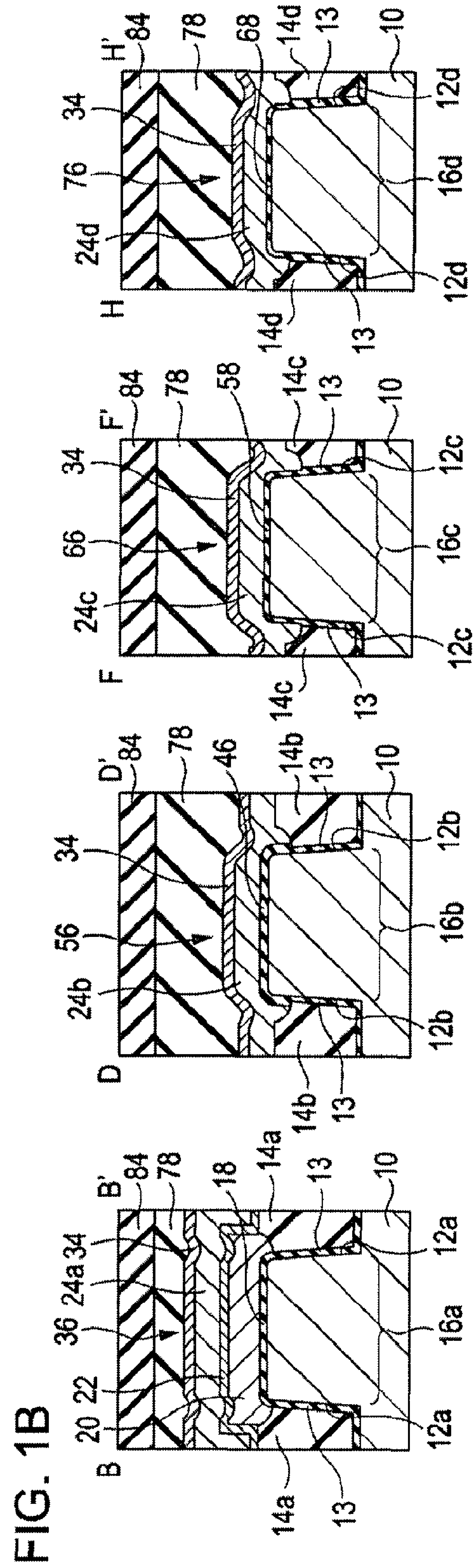


FIG. 1B

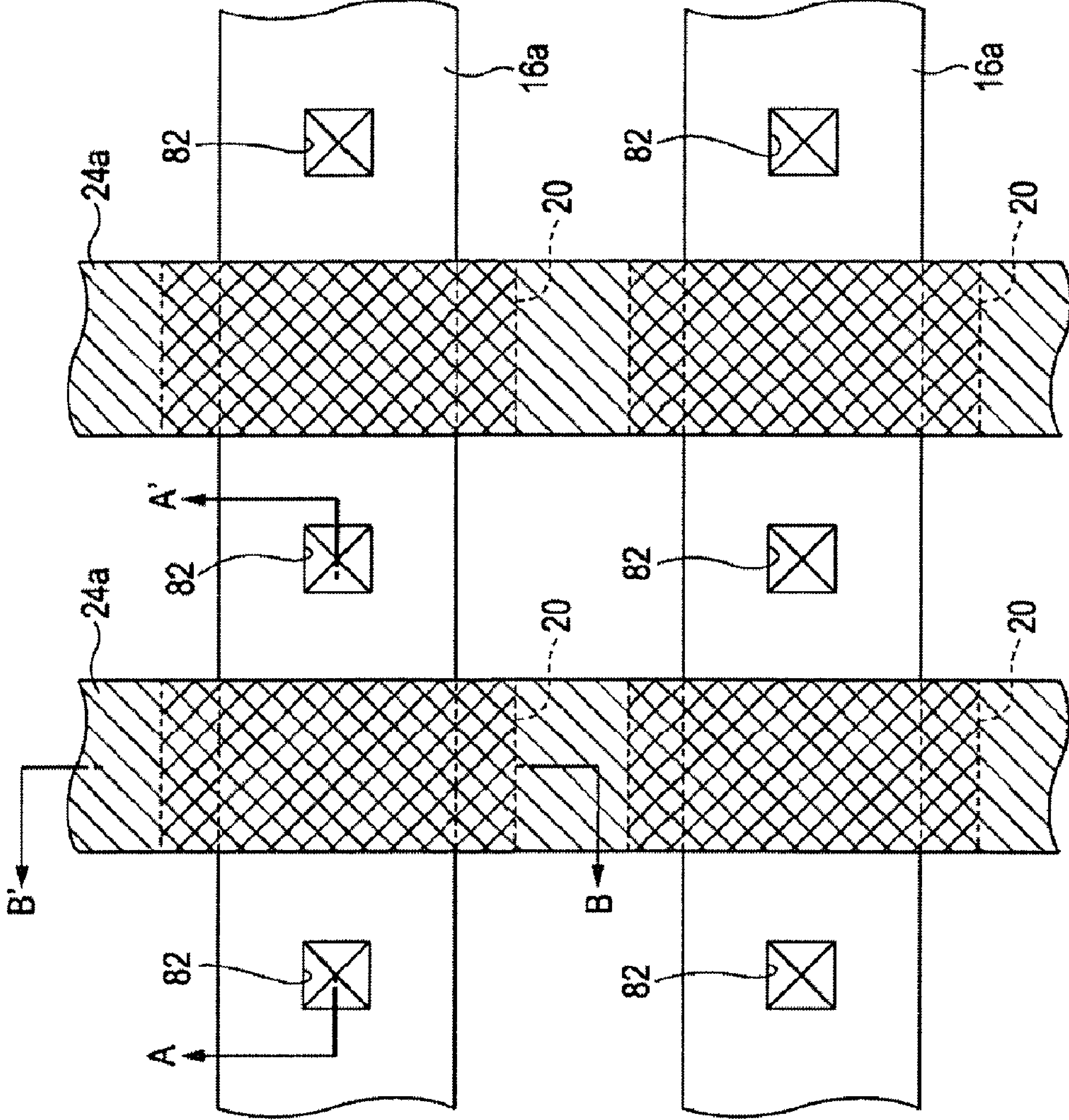


FIG. 2
16a
16a
82
82
82
82
82
82
24a
24a
20
20
20
20
A
A'
B
B'

FIG. 3A

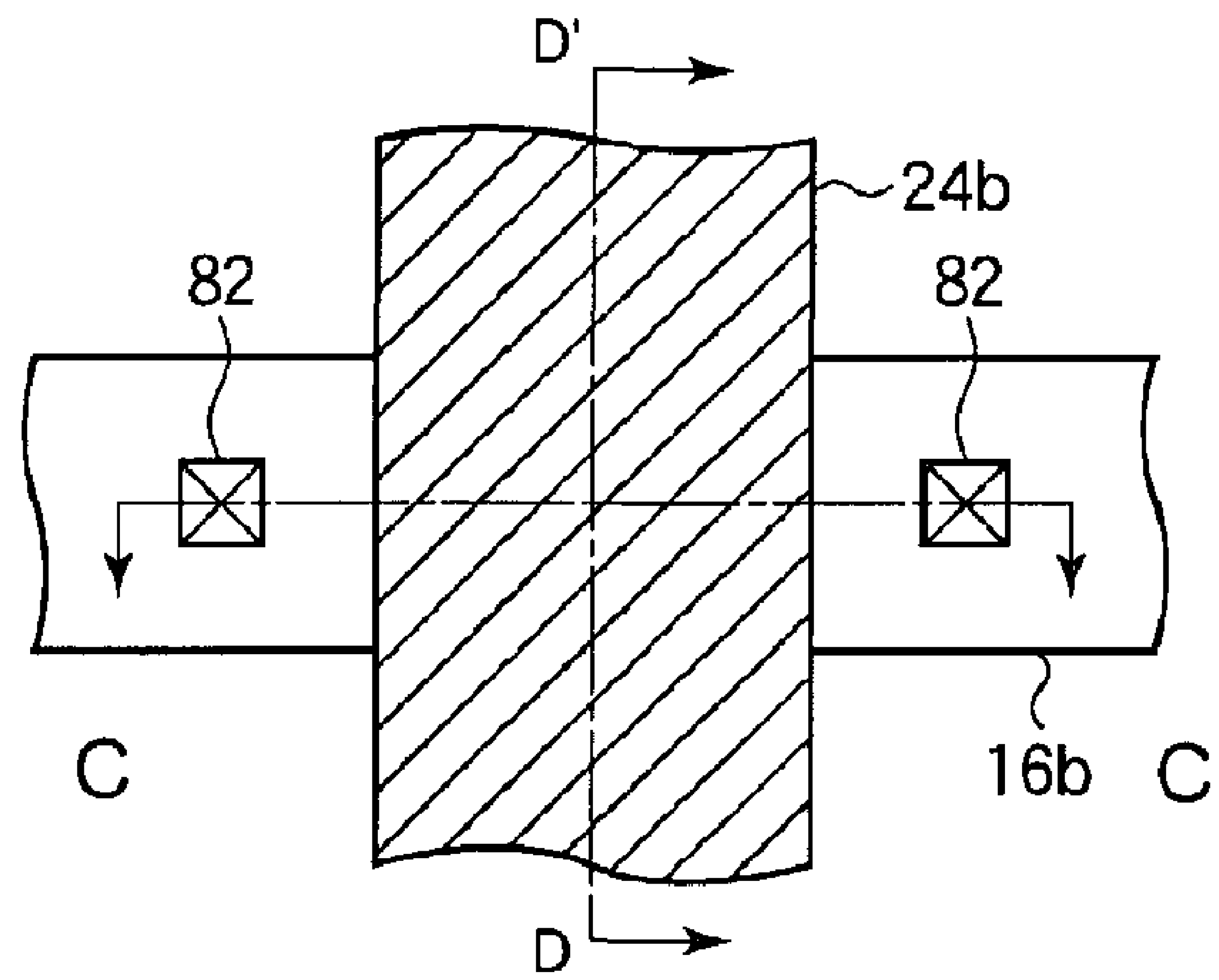


FIG.3B

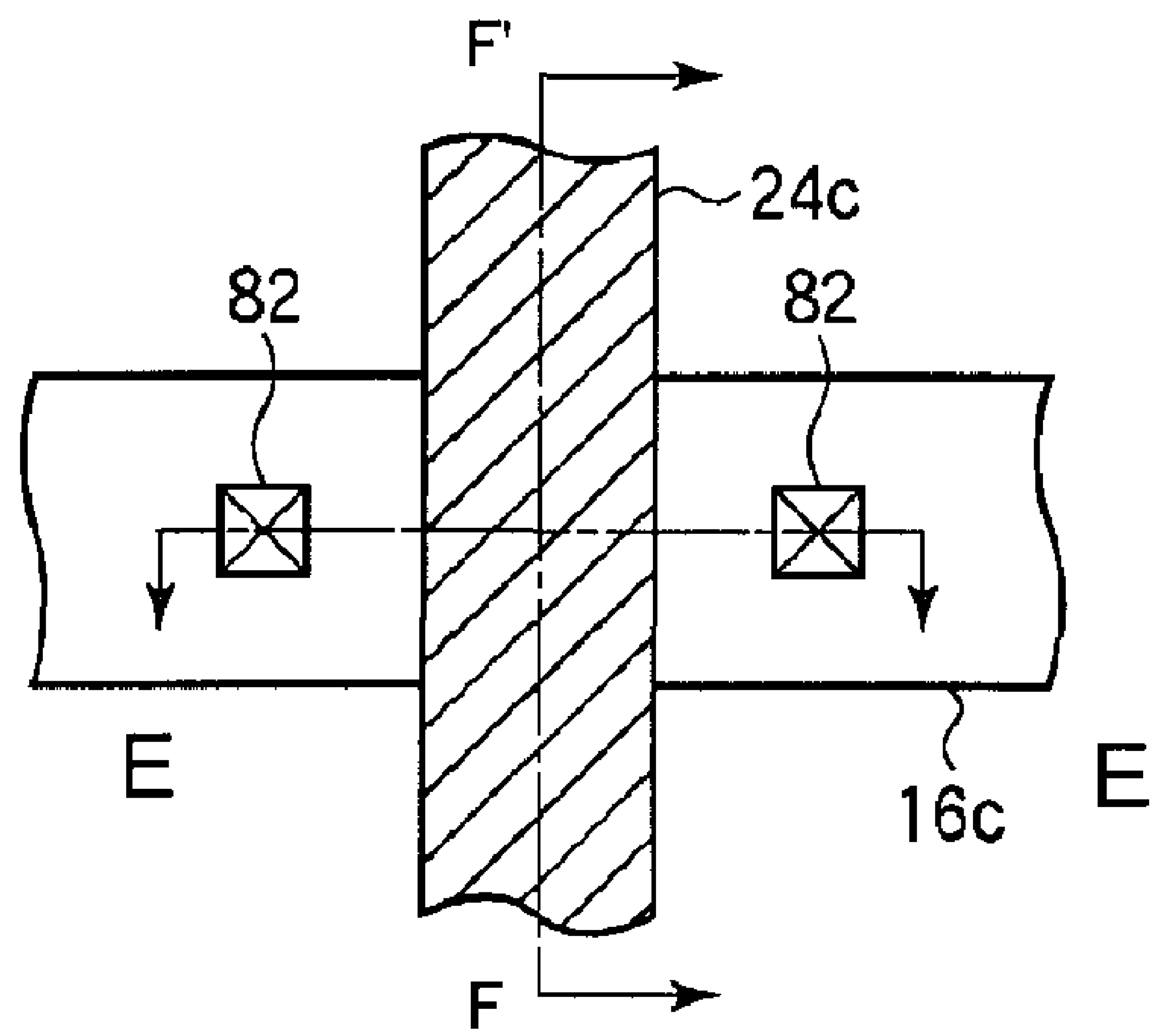
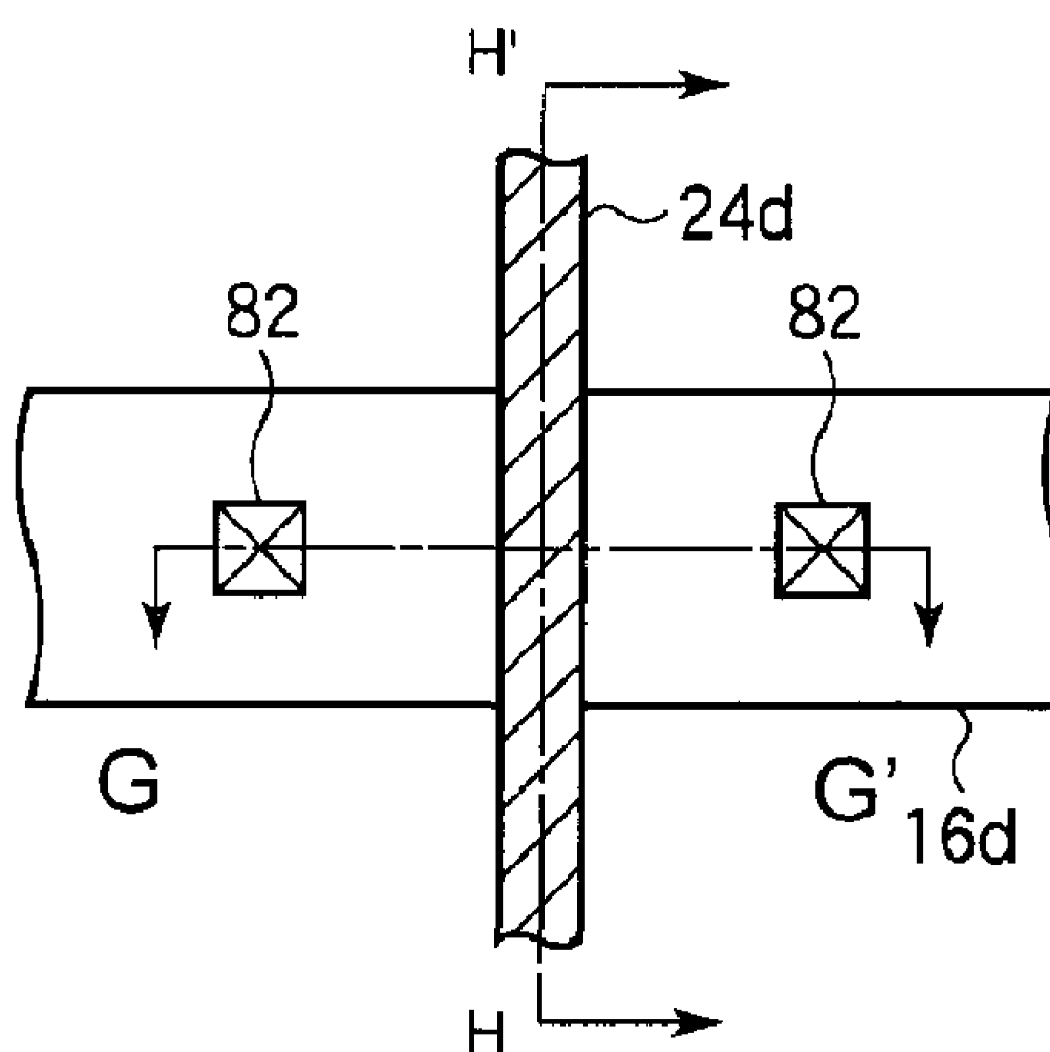


FIG.3C



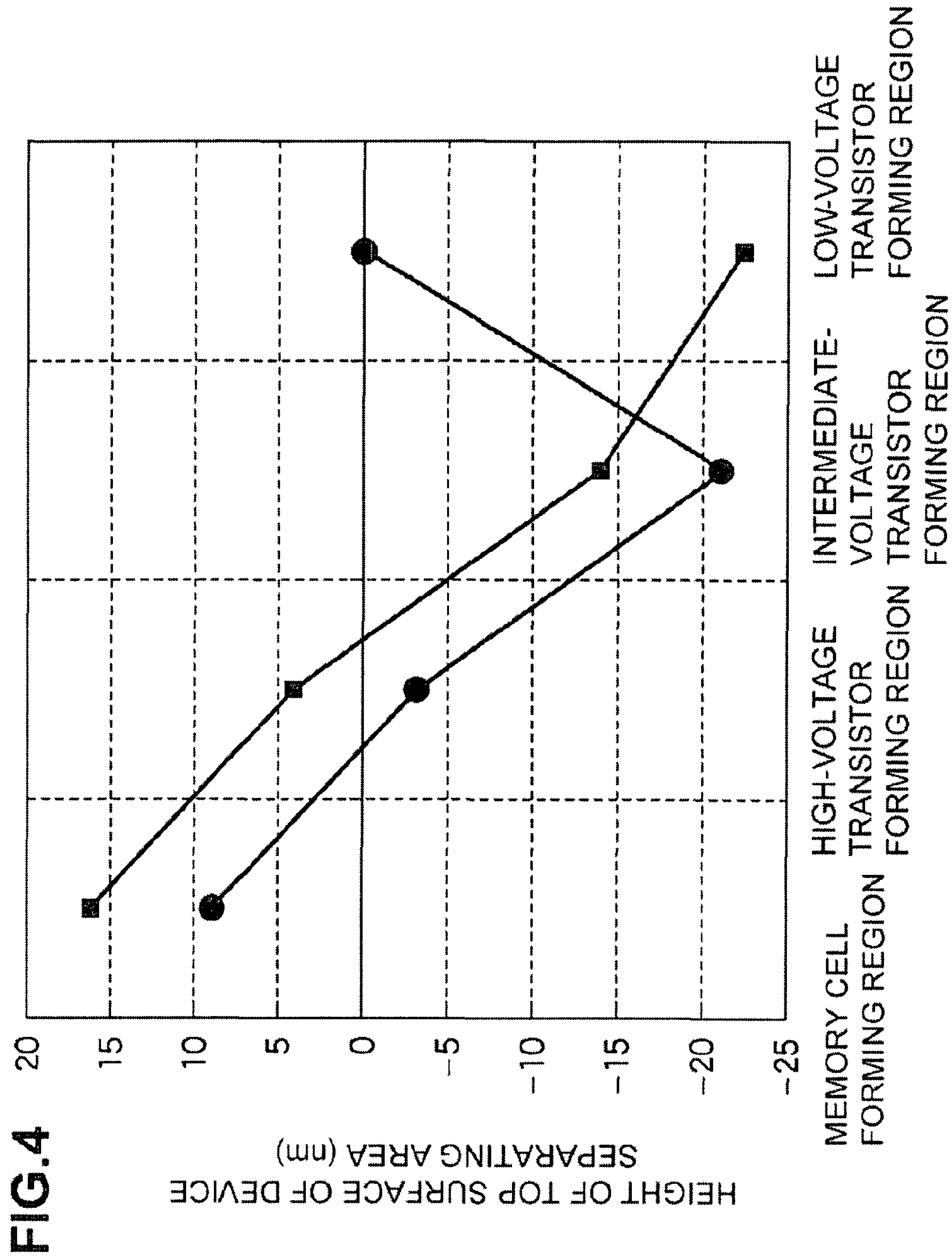


FIG.4
HEIGHT OF TOP SURFACE OF DEVICE SEPARATING AREA (nm)
20
15
10
5
0
−5
−10
−15
−20
−25
MEMORY CELL FORMING REGION
HIGH-VOLTAGE TRANSISTOR FORMING REGION
INTERMEDIATE-VOLTAGE TRANSISTOR FORMING REGION
LOW-VOLTAGE TRANSISTOR FORMING REGION

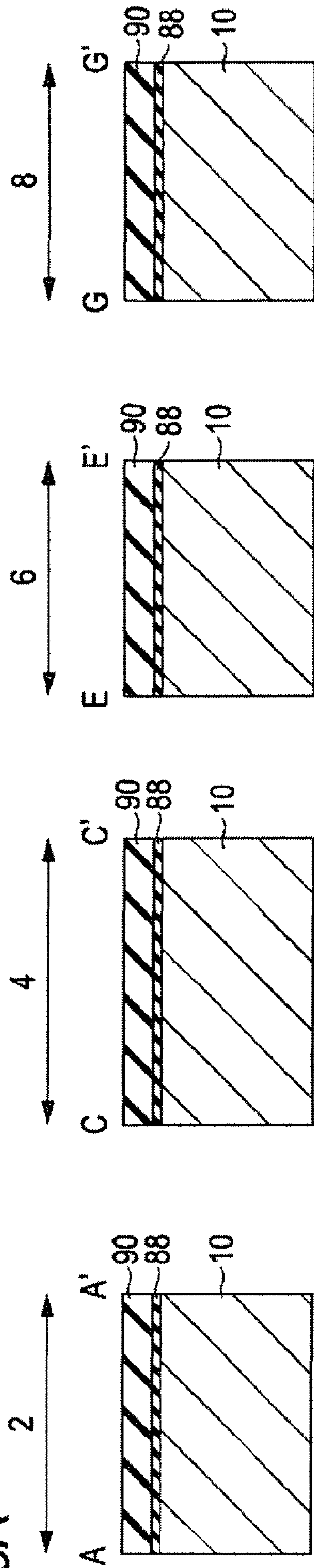


FIG. 5A

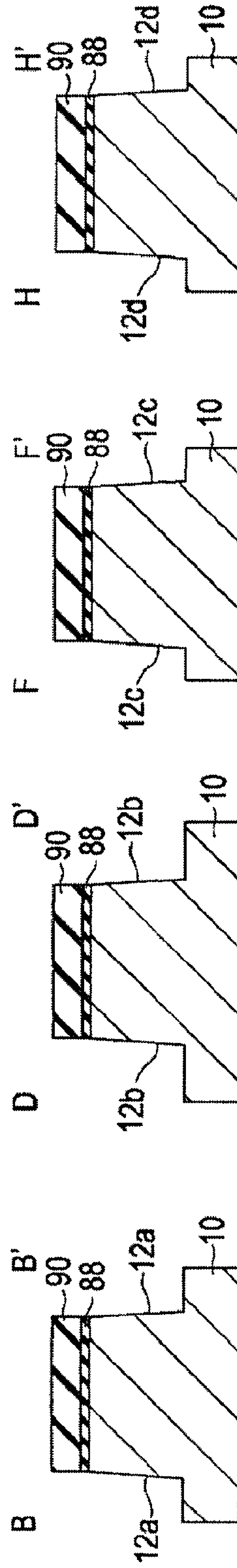


FIG. 5B

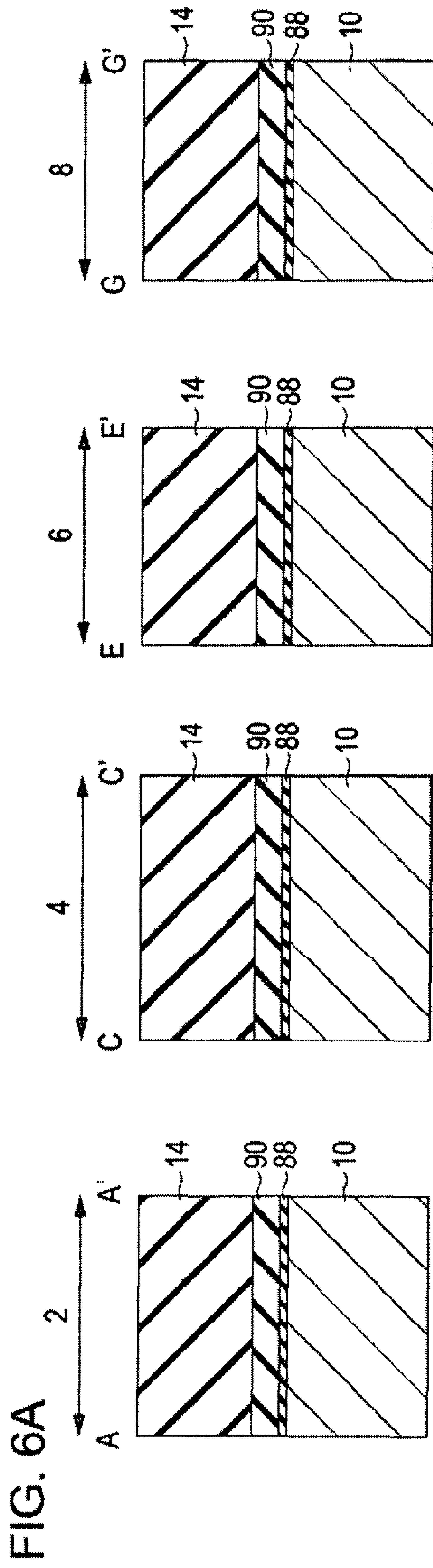


FIG. 6A
A
A'
2
14
90
88
10
C
C'
4
E
E'
6
G
G'
8

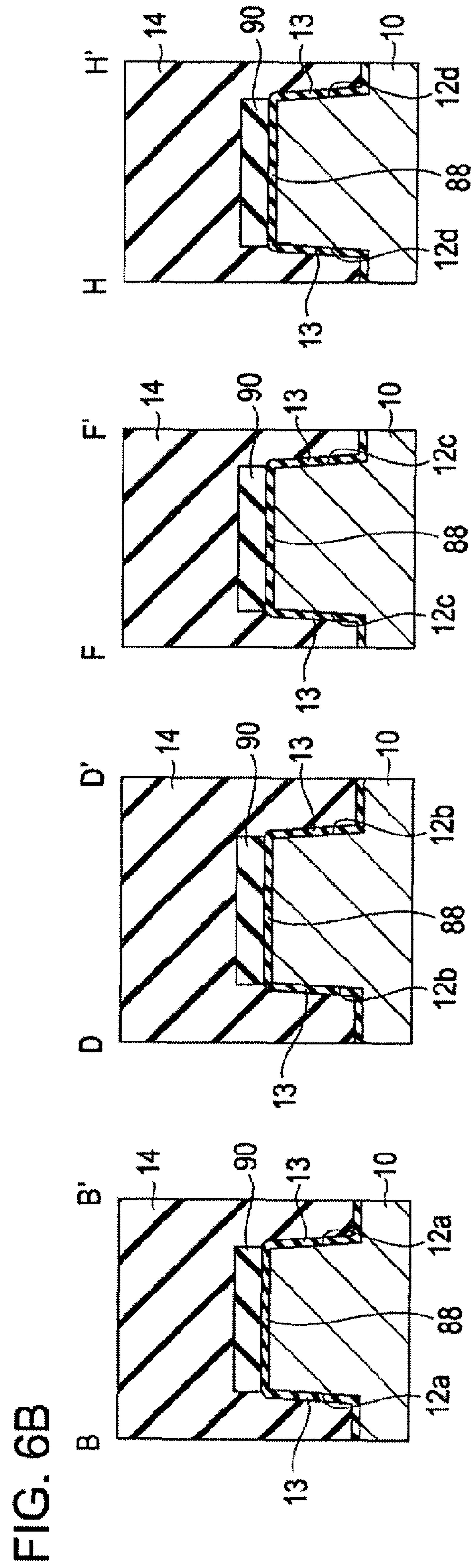


FIG. 6B
B
B'
14
90
13
10
12a
88
D
D'
12b
F
F'
12c
H
H'
12d

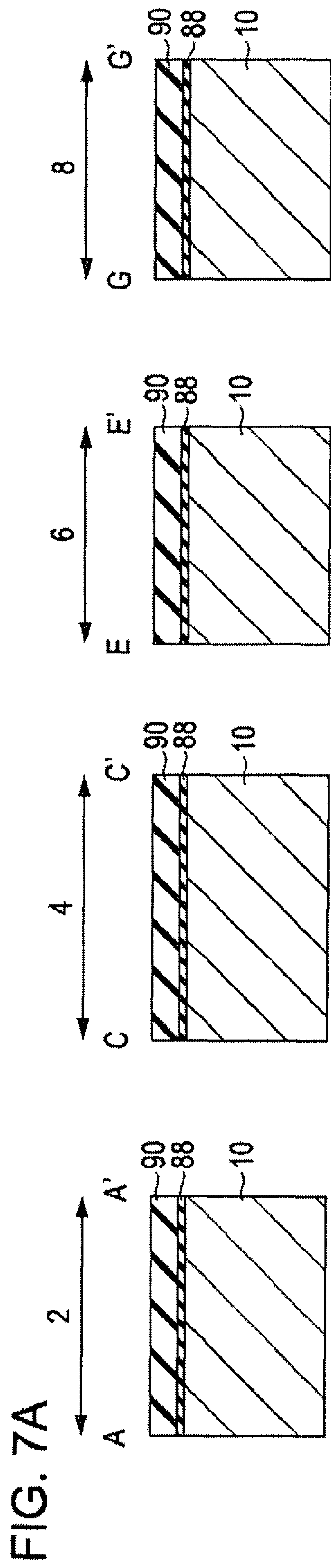


FIG. 7A

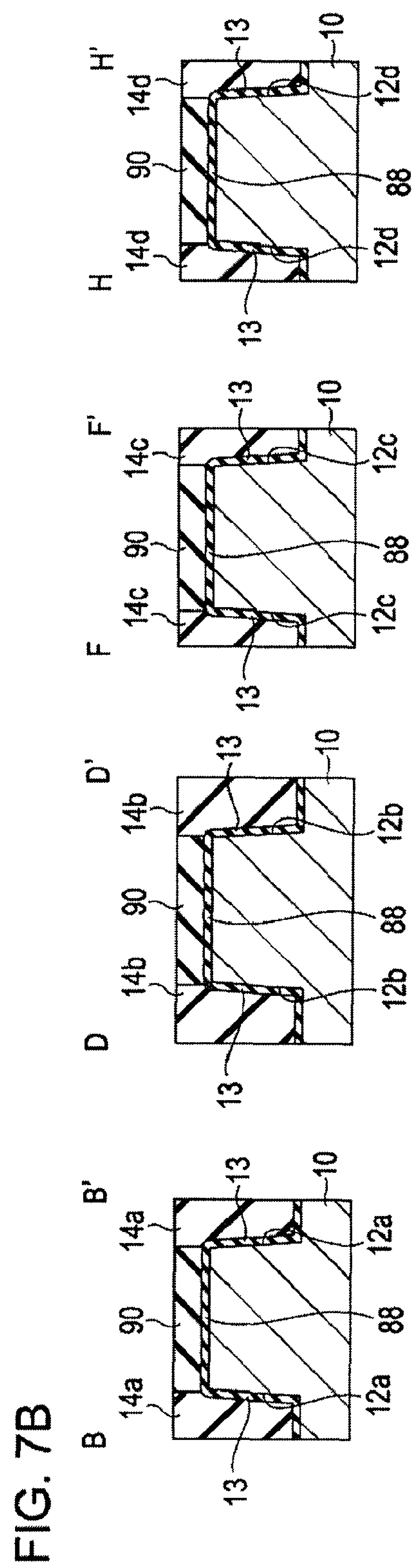


FIG. 7B

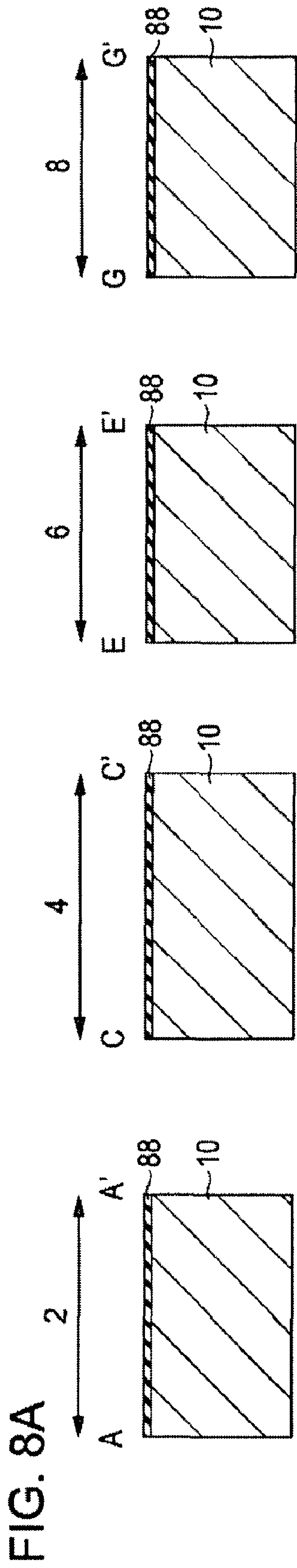


FIG. 8A

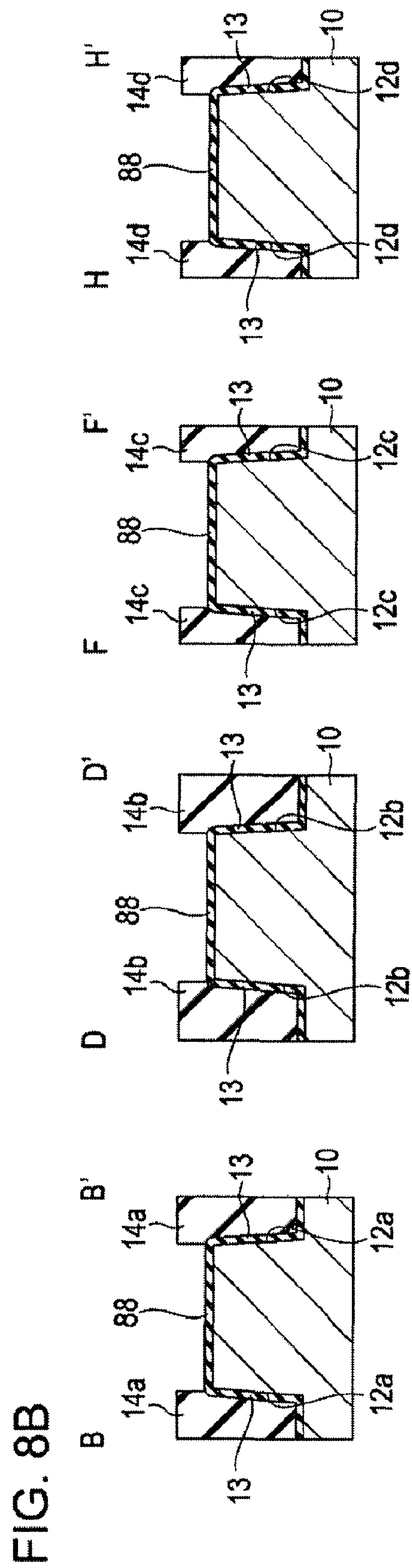


FIG. 8B

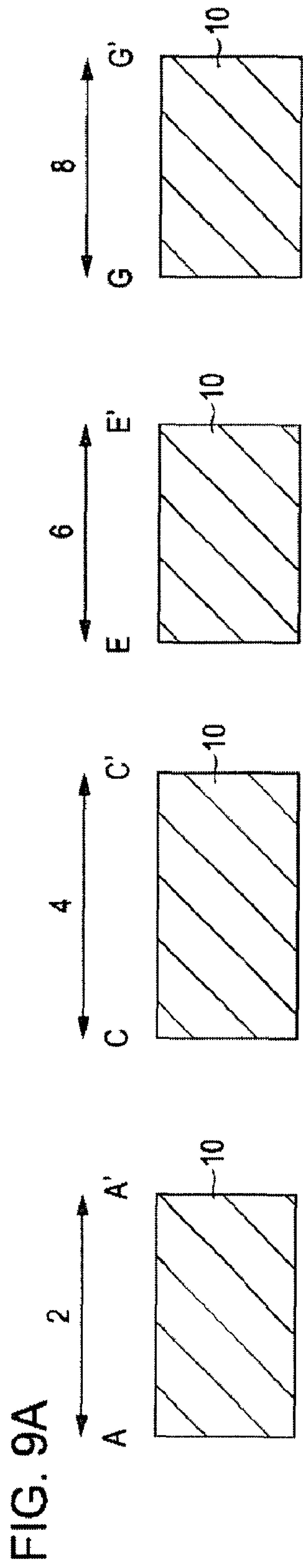


FIG. 9A

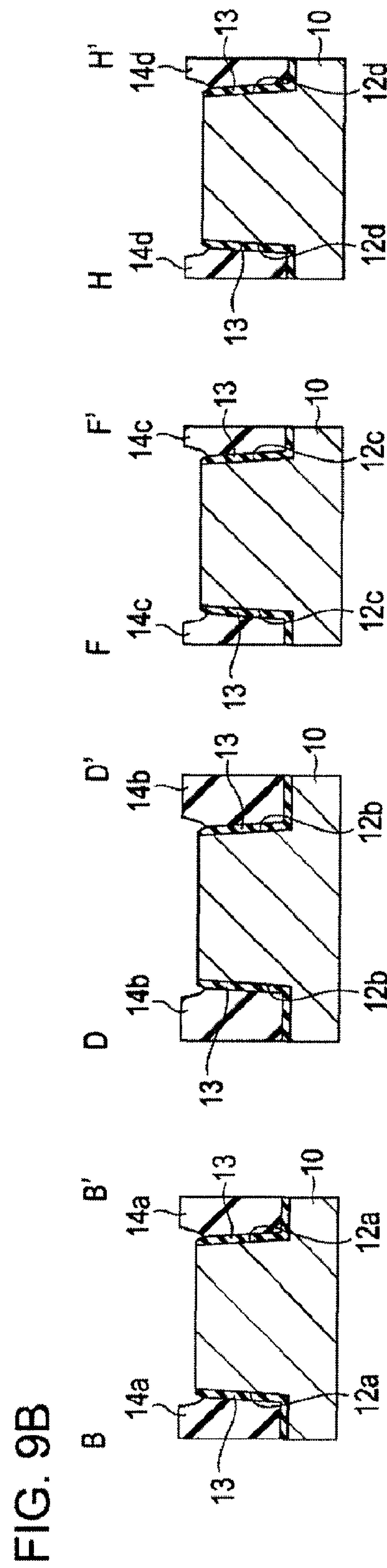


FIG. 9B

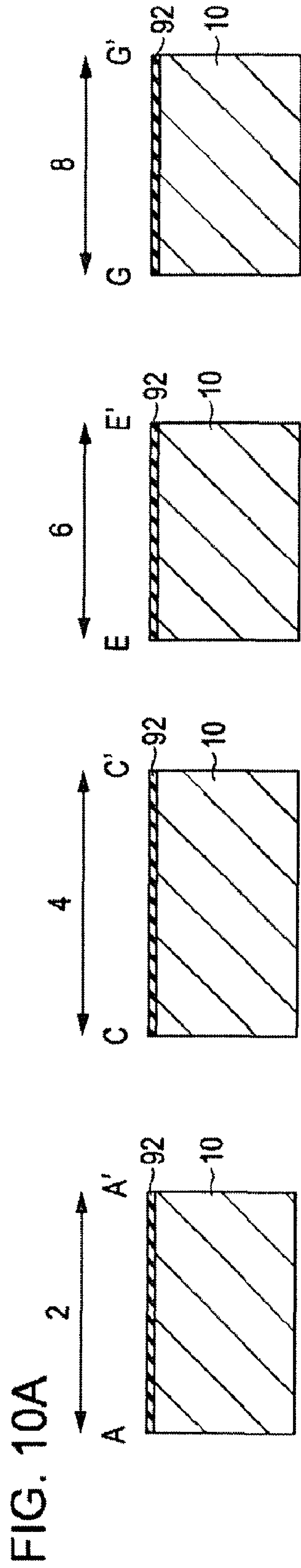


FIG. 10A

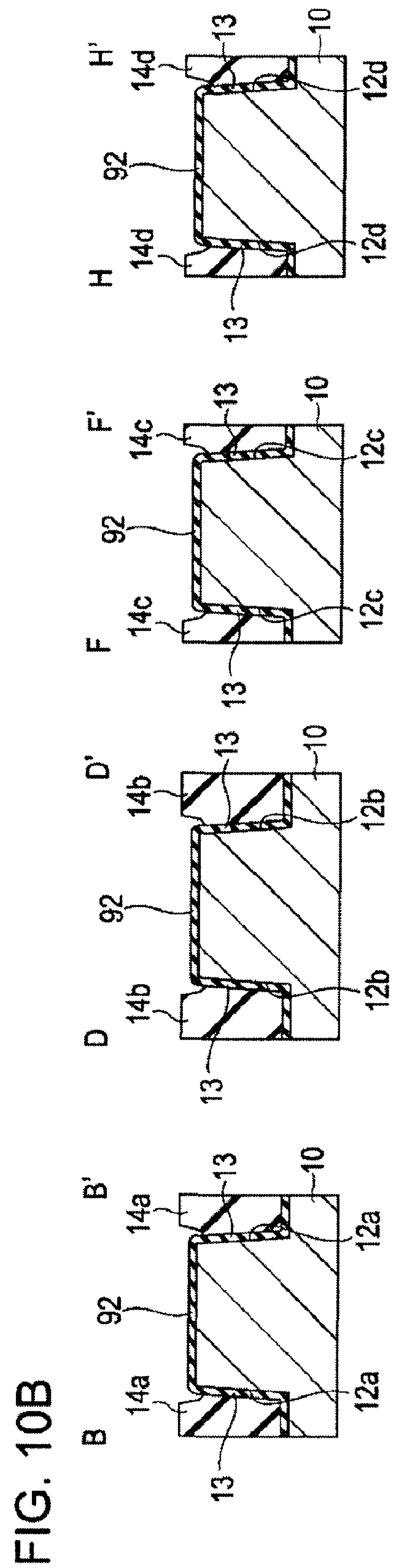


FIG. 10B

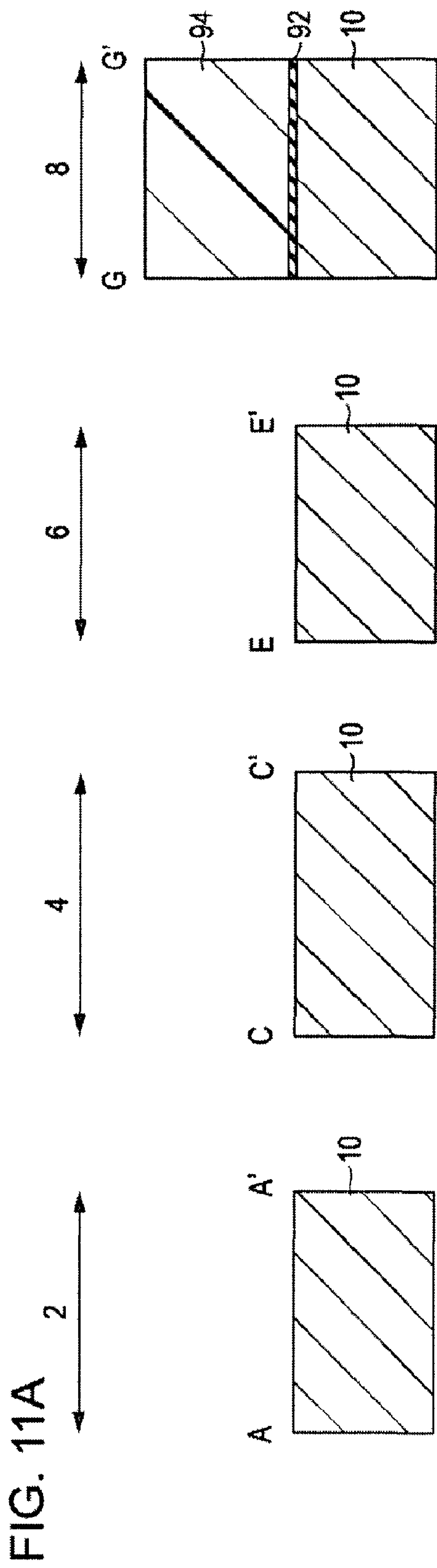


FIG. 11A
2
4
6
8
A
A'
C
C'
E
E'
G
G'
10
92
94

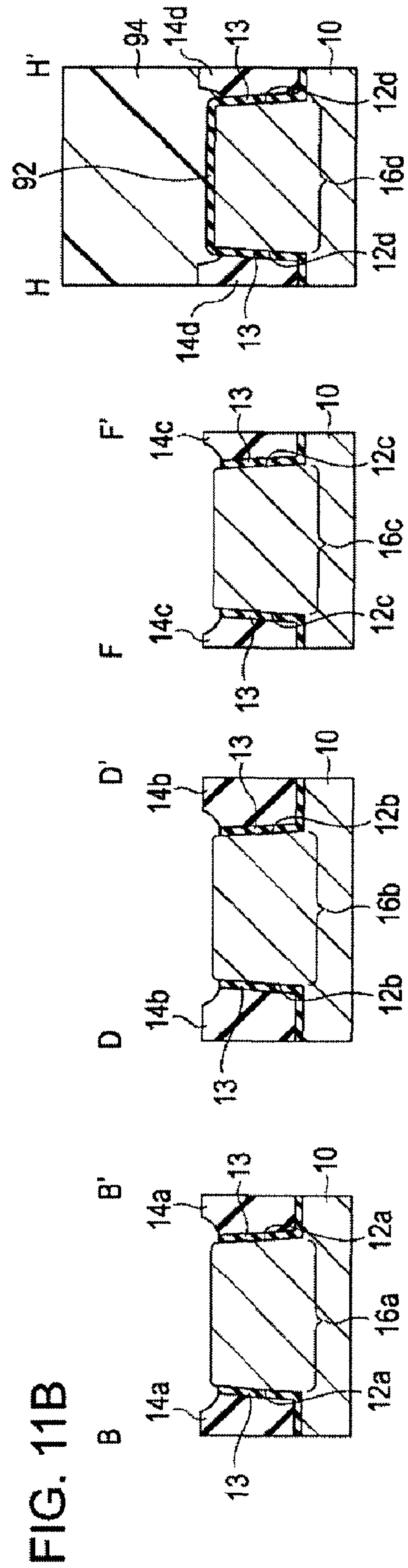


FIG. 11B
B
B'
D
D'
F
F'
H
H'
10
13
14a
14b
14c
14d
12a
12b
12c
12d
16a
16b
16c
16d
92
94

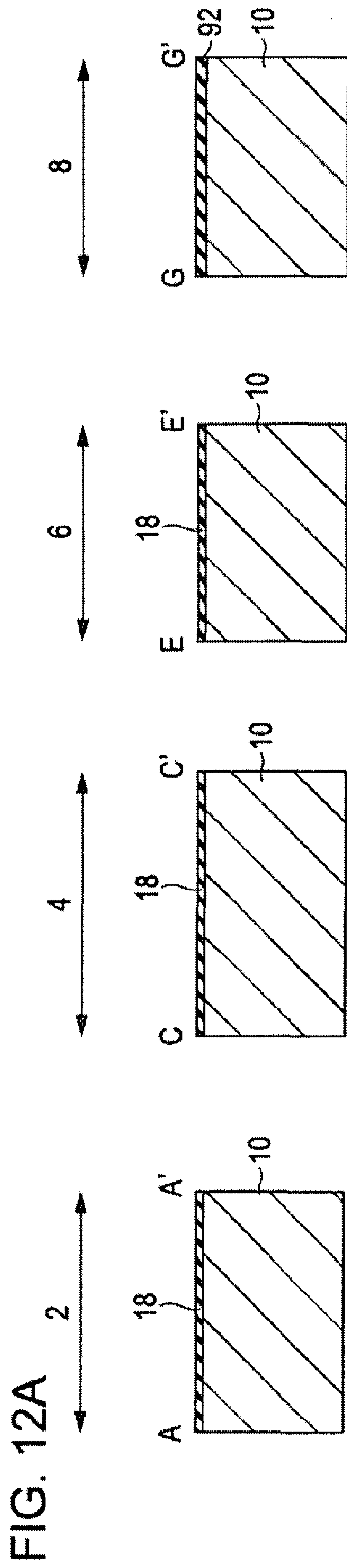


FIG. 12A
2
4
6
8
A
A'
C
C'
E
E'
G
G'
18
92
10

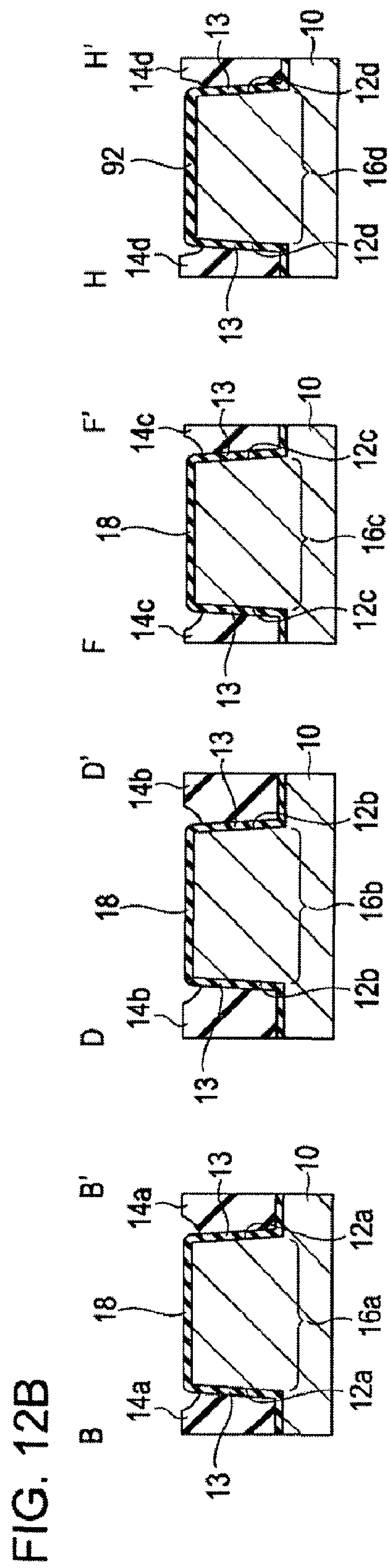


FIG. 12B
B
B'
D
D'
F
F'
H
H'
18
92
13
14a
14b
14c
14d
12a
12b
12c
12d
16a
16b
16c
16d
10

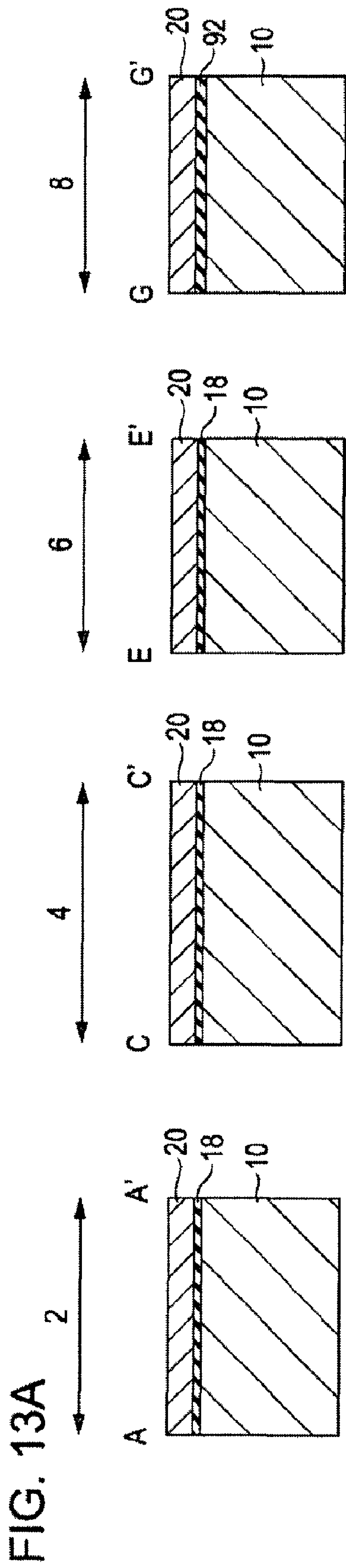


FIG. 13A

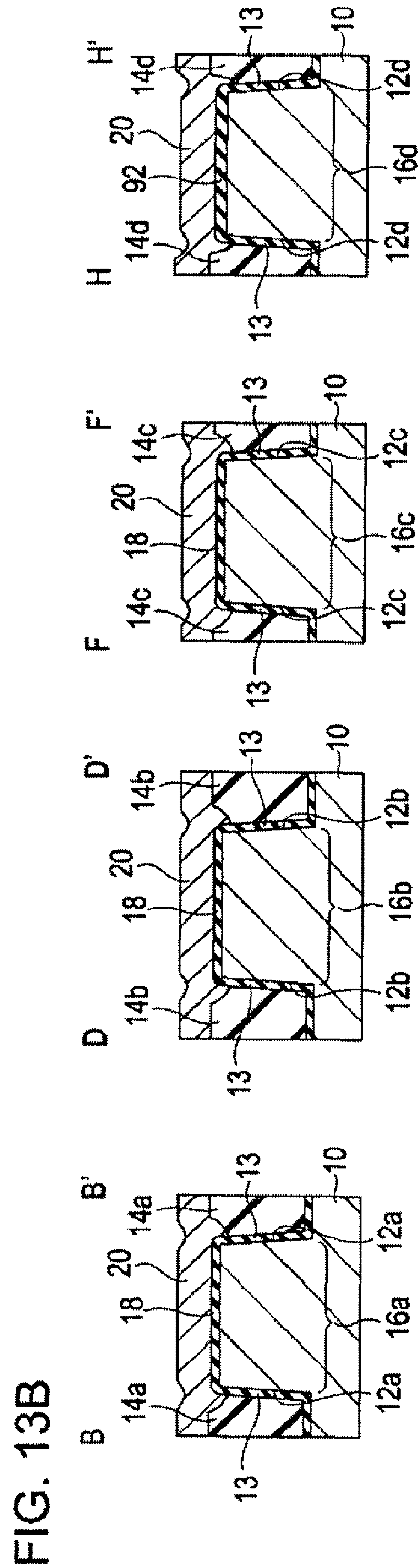


FIG. 13B

FIG. 14A

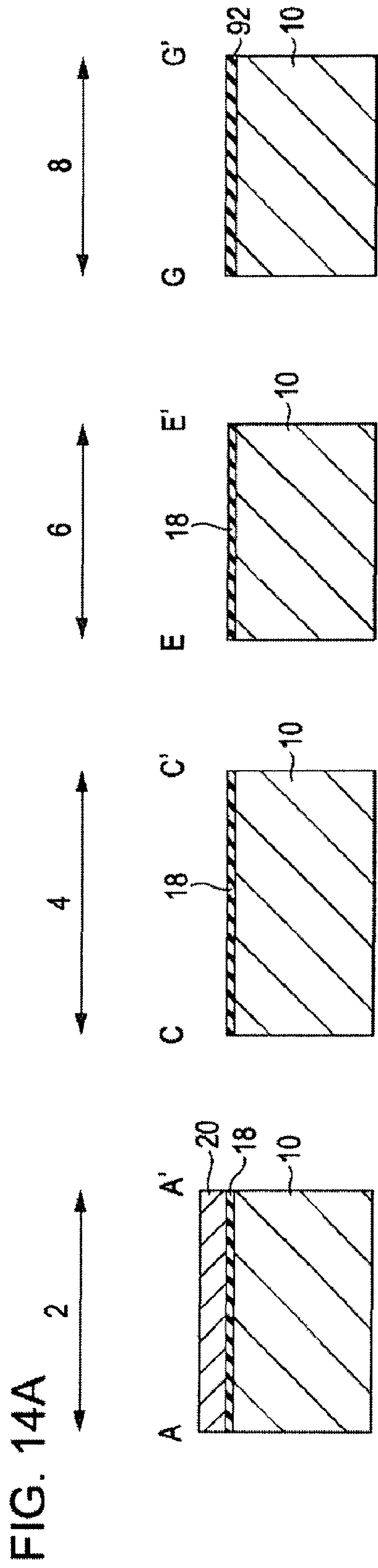
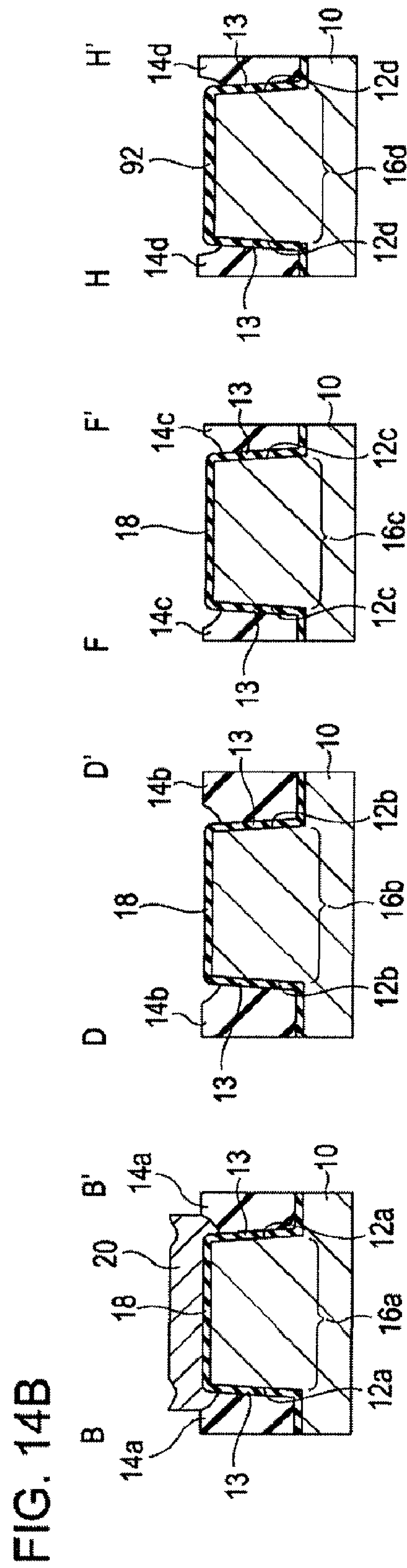


FIG. 14B



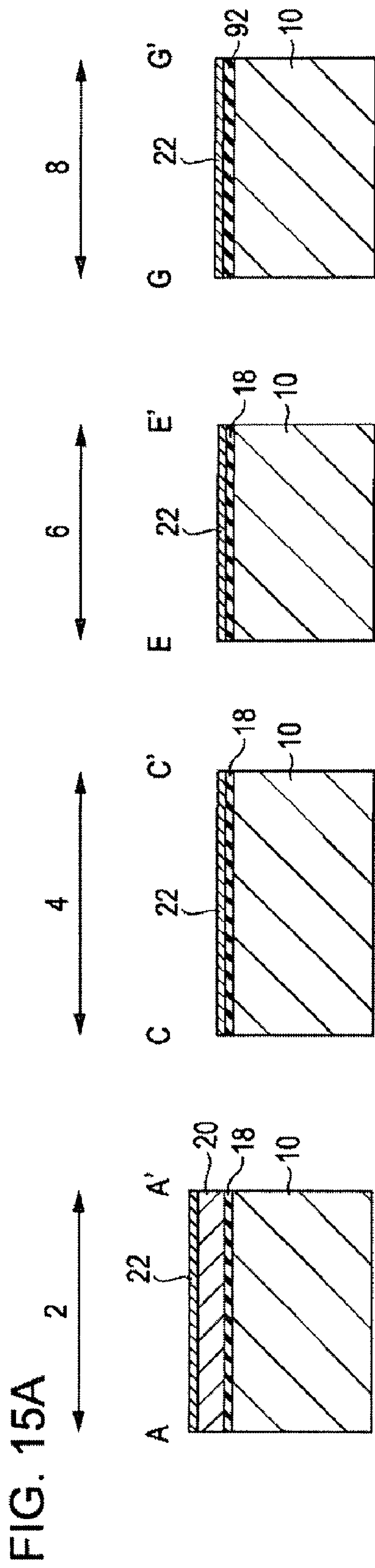


FIG. 15A
2
4
6
8
A
A'
C
C'
E
E'
G
G'
22
20
18
10
92

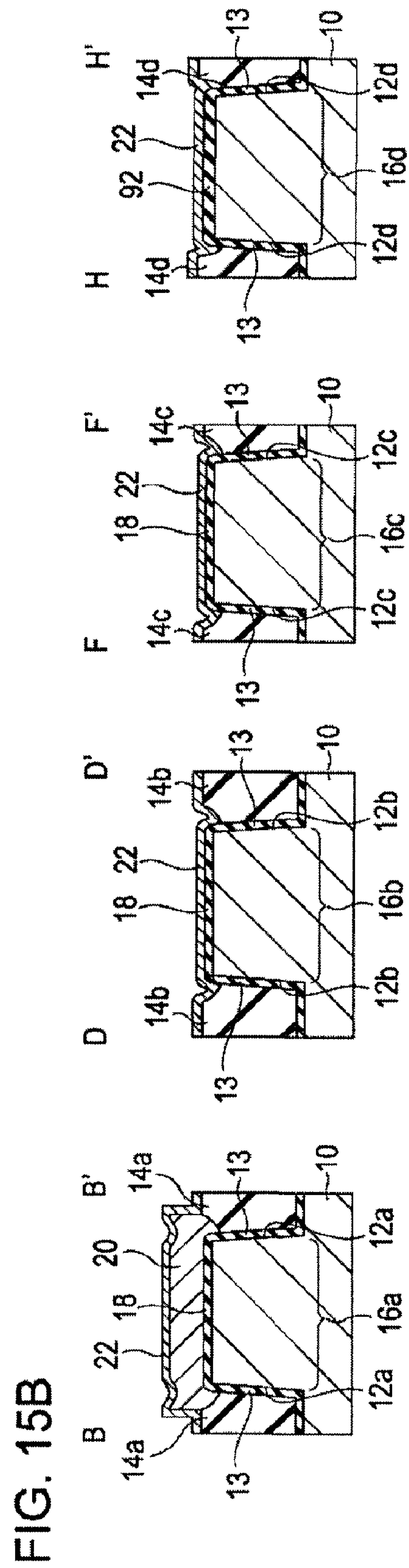


FIG. 15B
B
B'
D
D'
F
F'
H
H'
22
20
18
92
13
10
14a
14b
14c
14d
12a
12b
12c
12d
16a
16b
16c
16d

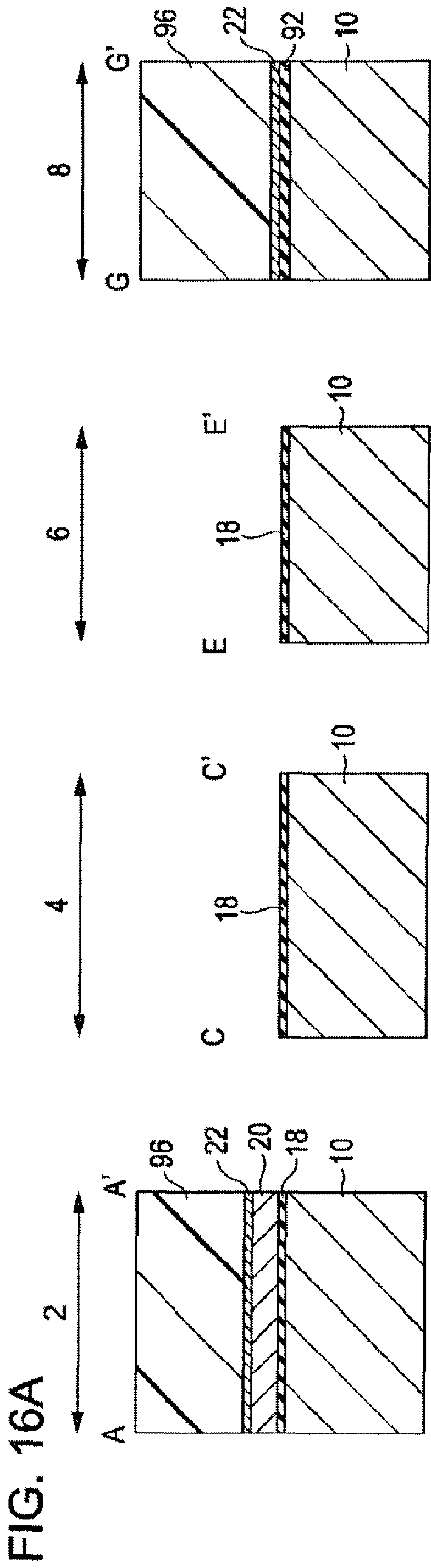


FIG. 16A

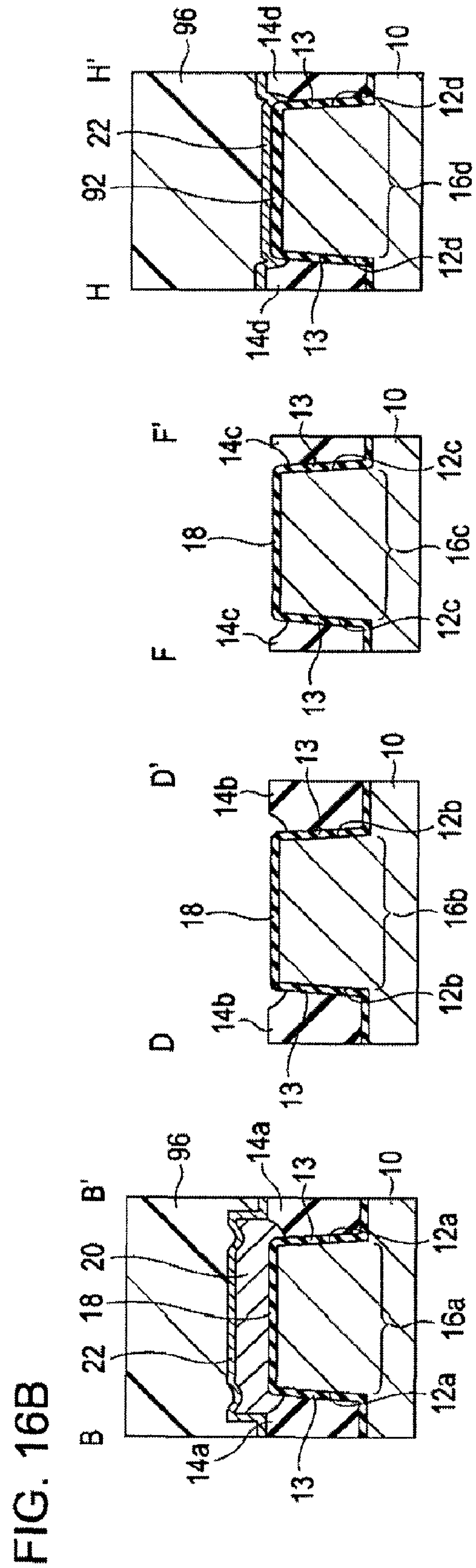


FIG. 16B

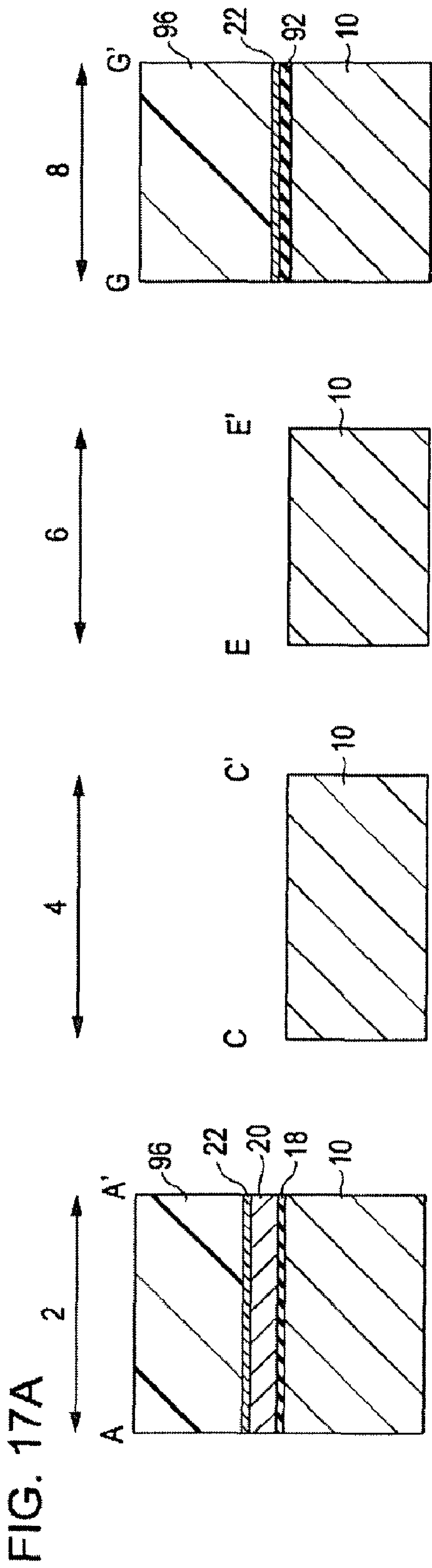


FIG. 17A

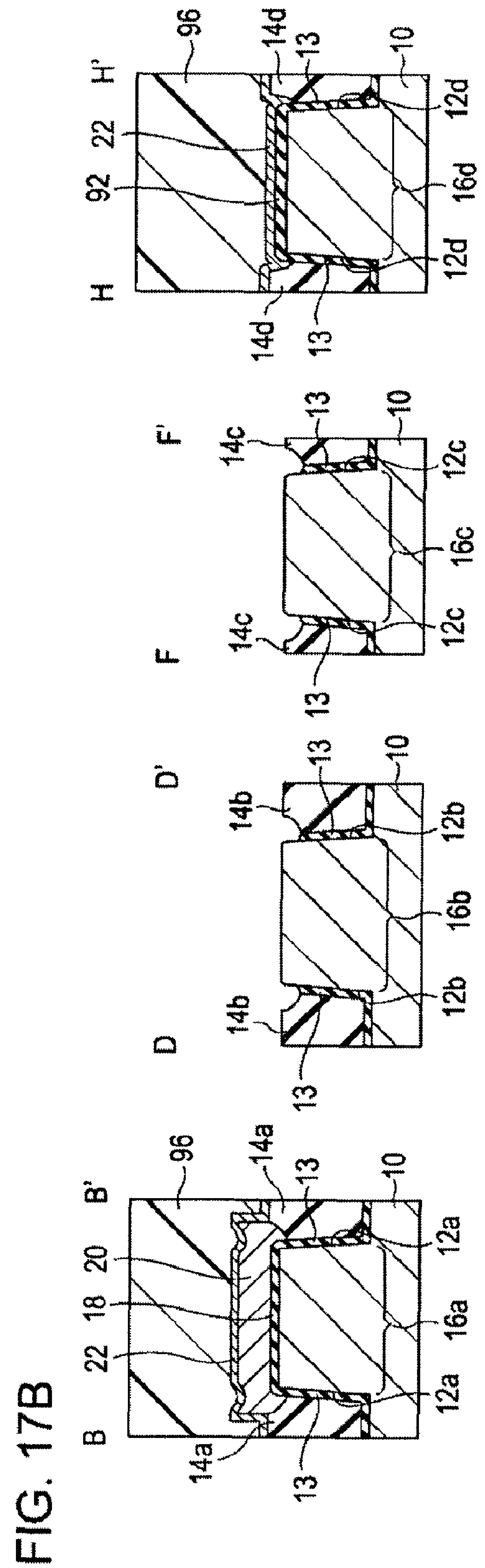


FIG. 17B

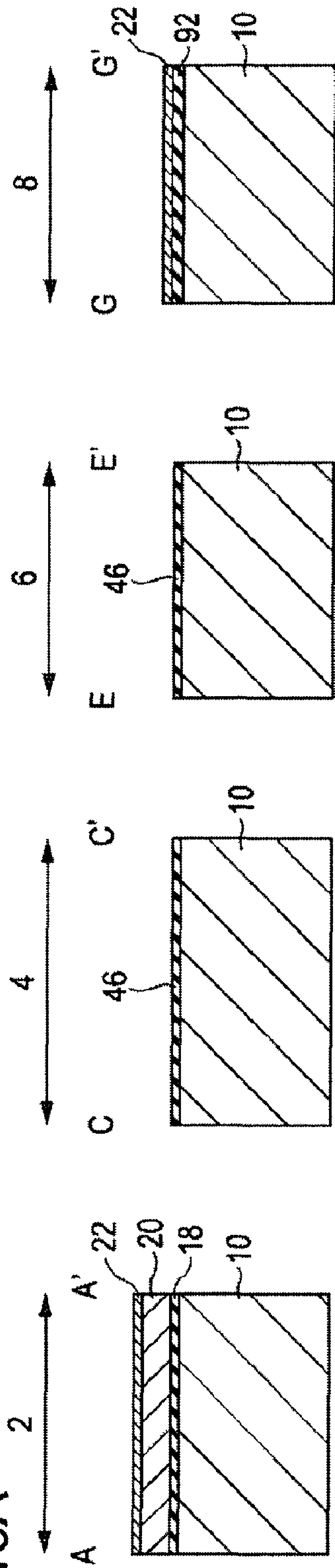


FIG. 18A

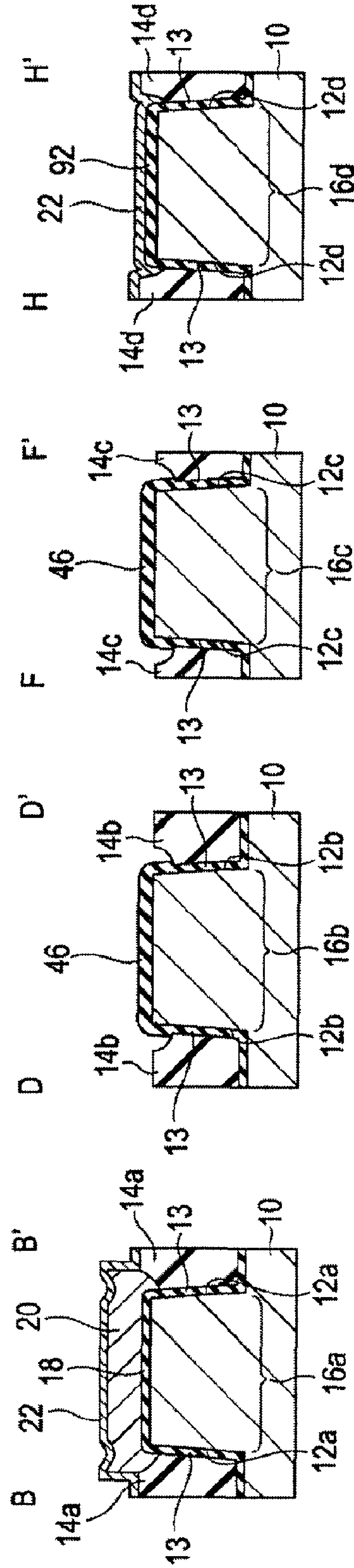


FIG. 18B

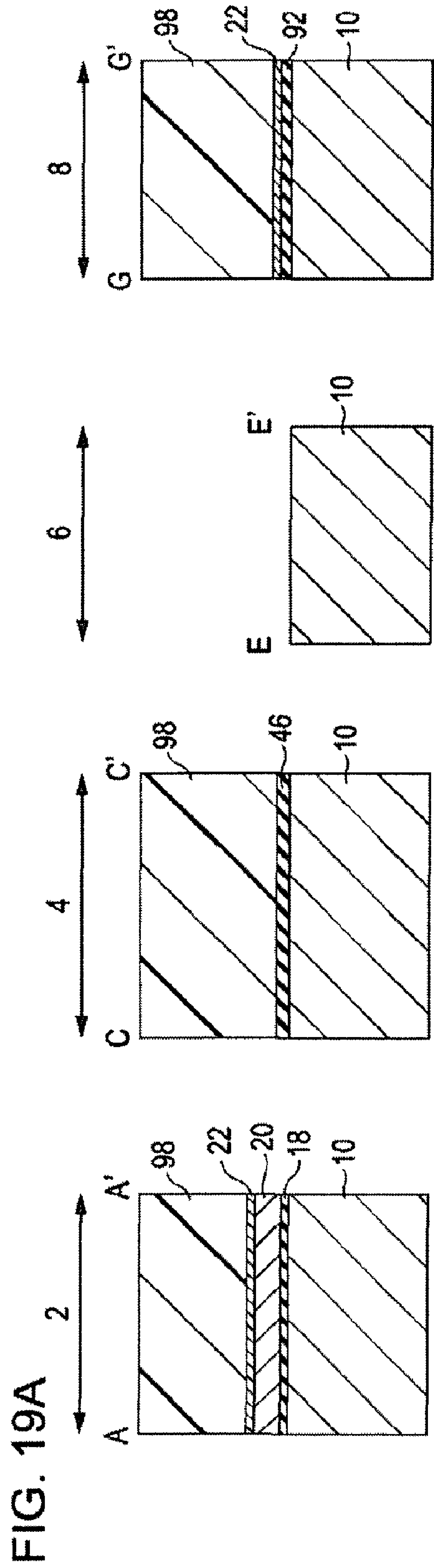


FIG. 19A

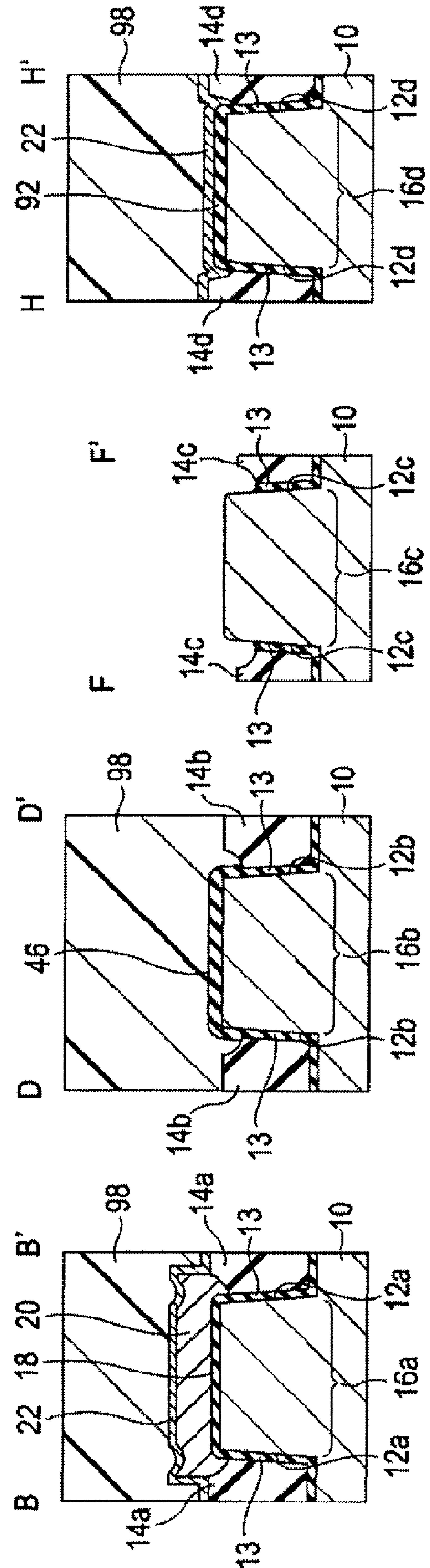


FIG. 19B

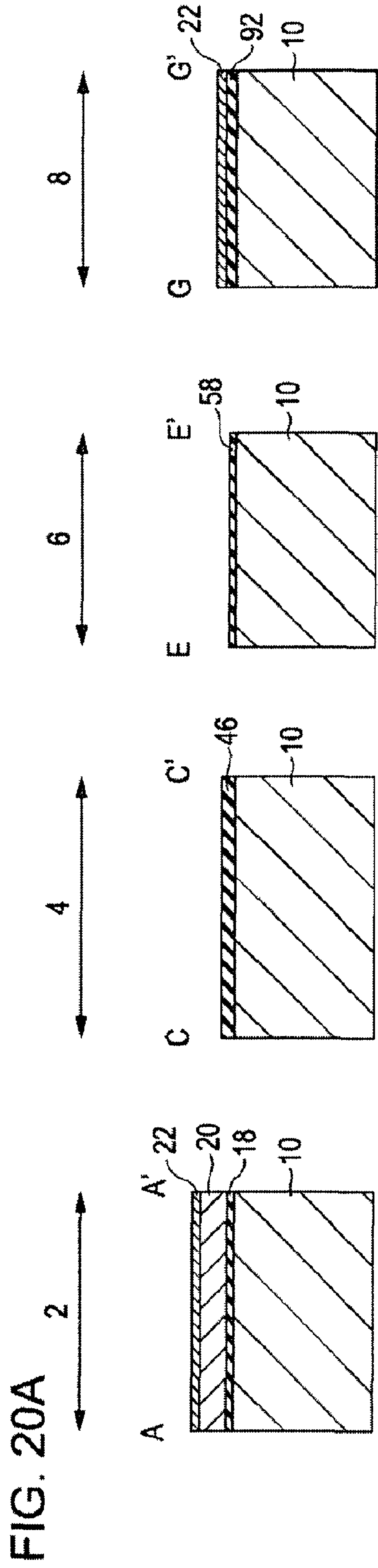


FIG. 20A

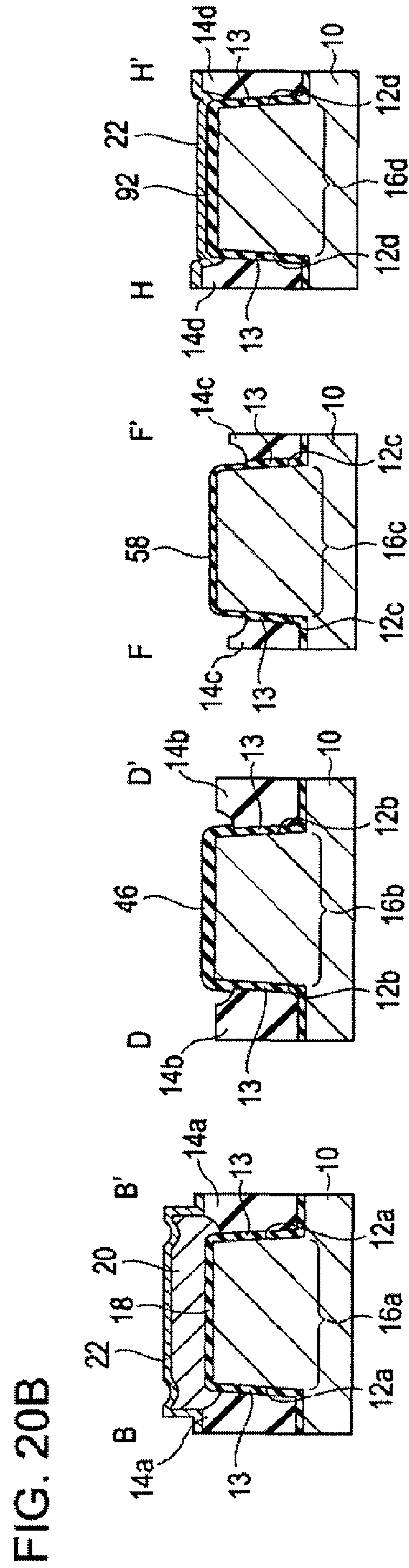


FIG. 20B

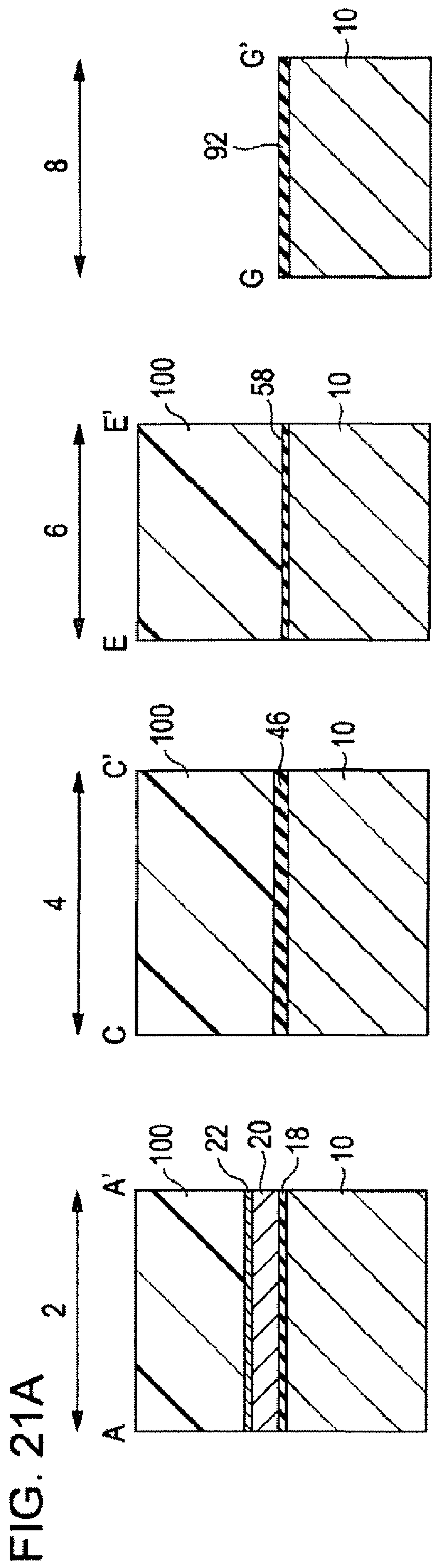


FIG. 21A

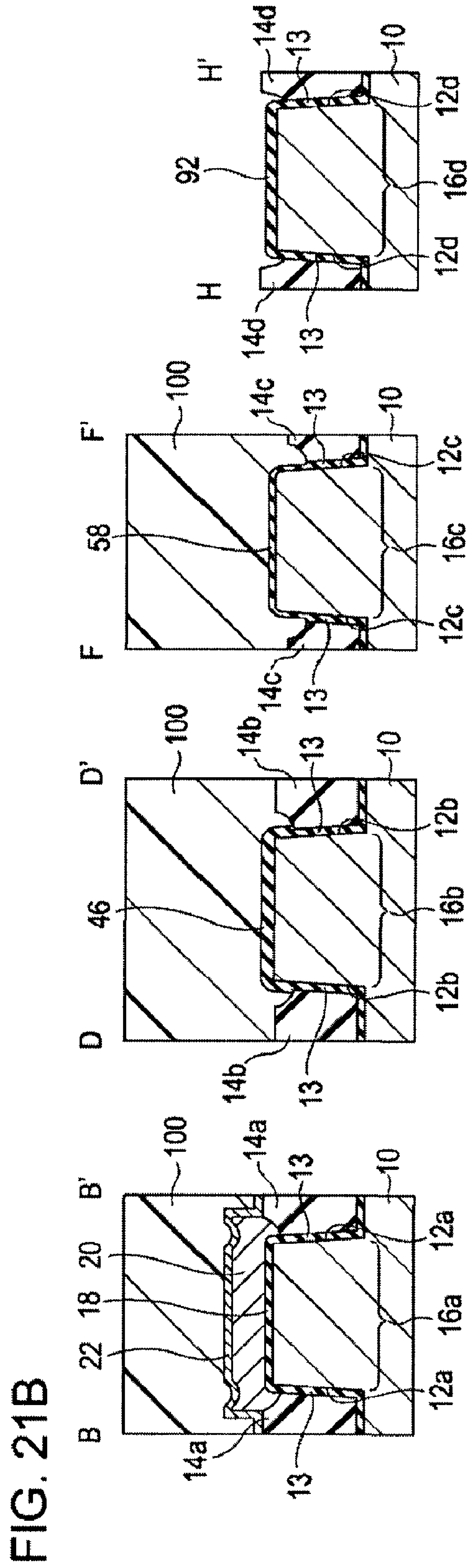


FIG. 21B

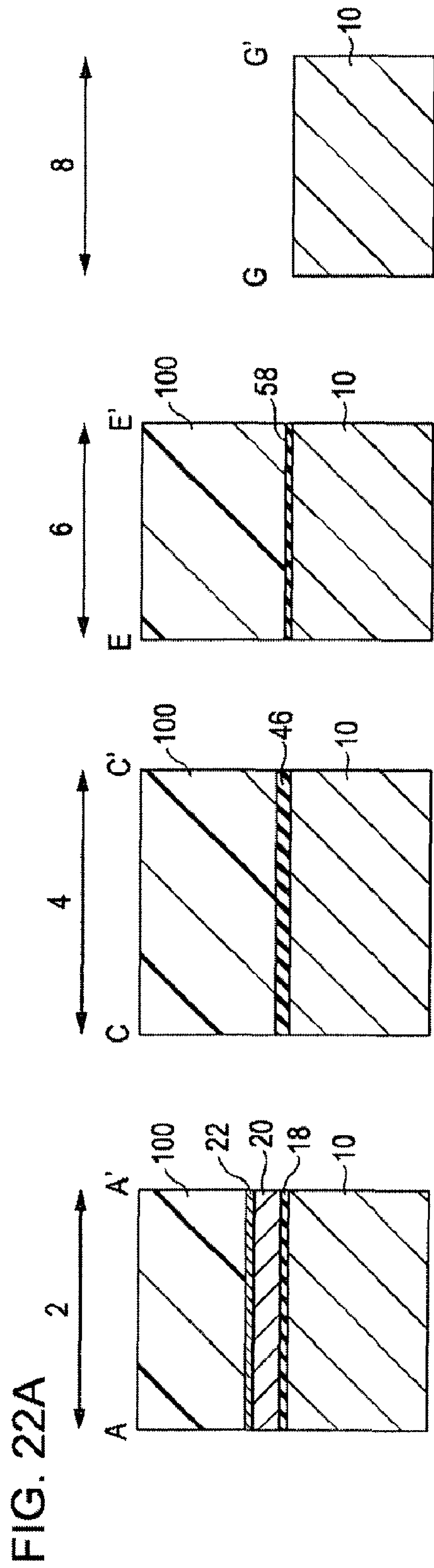


FIG. 22A

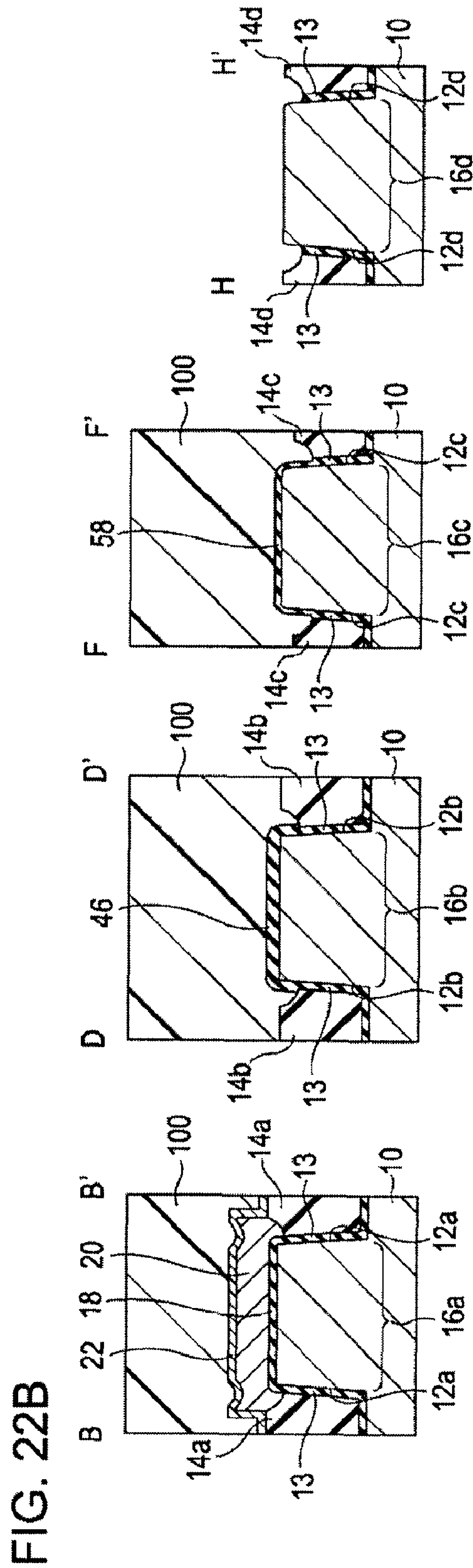


FIG. 22B

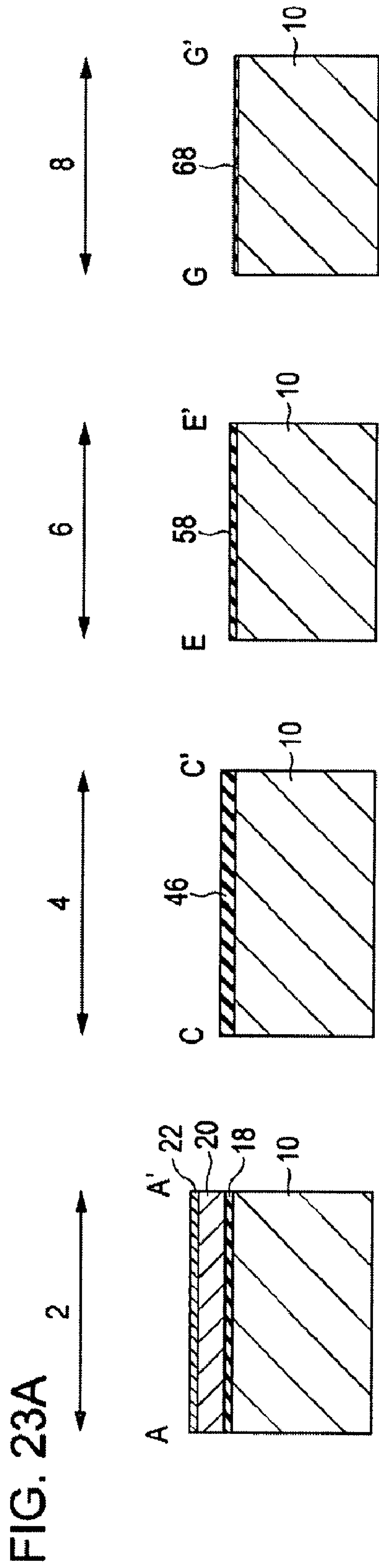


FIG. 23A

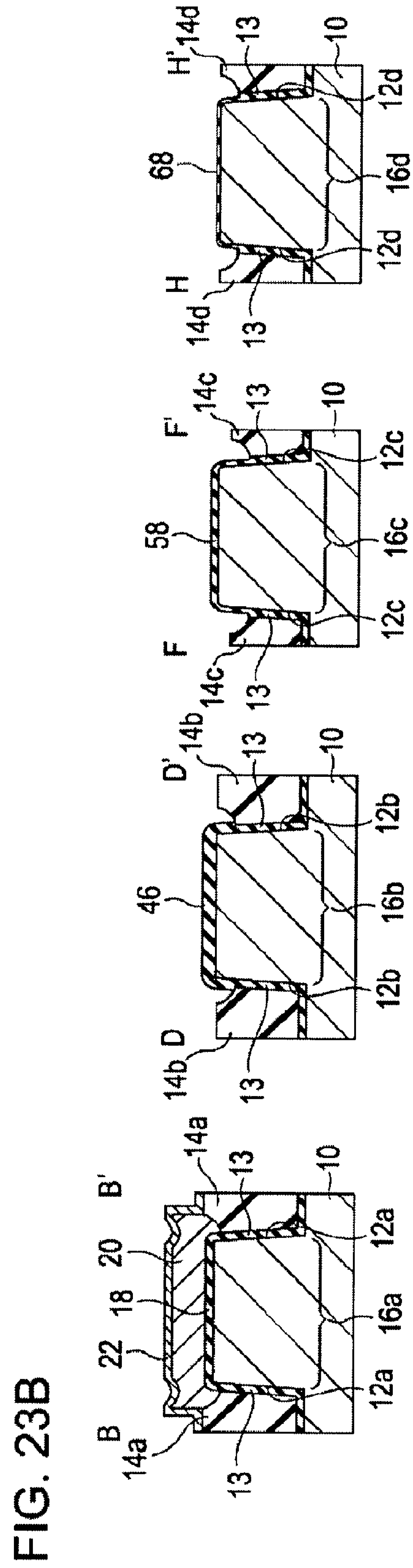


FIG. 23B

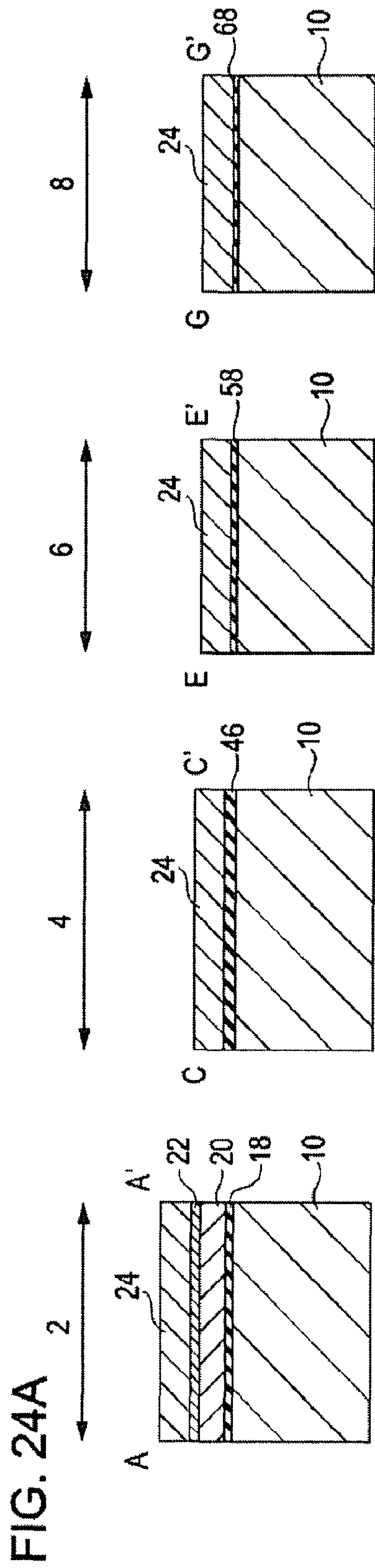


FIG. 24A

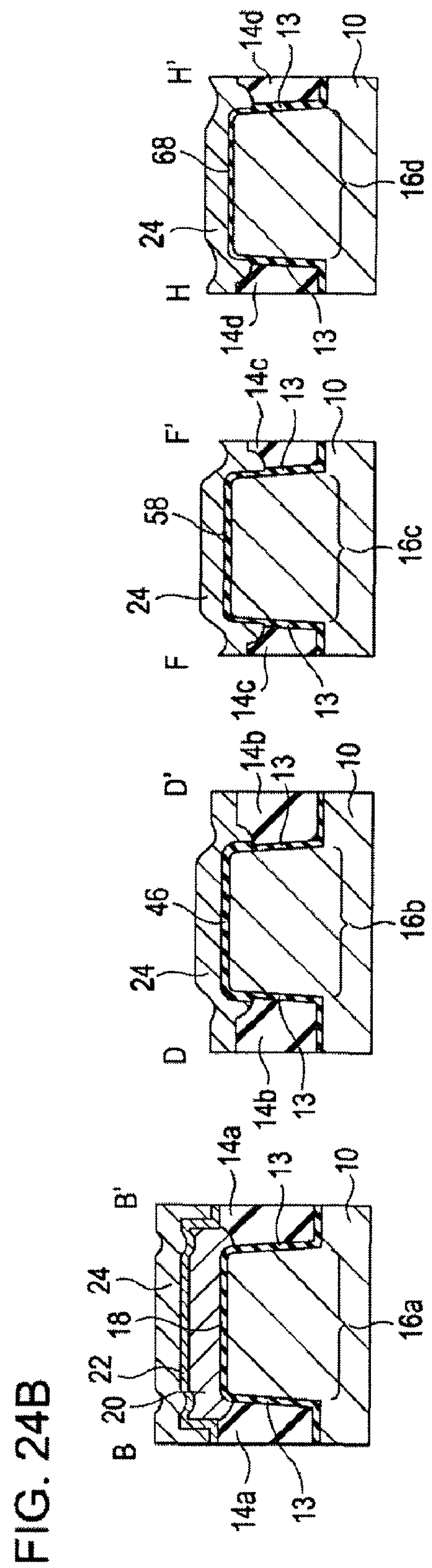


FIG. 24B

FIG. 25A

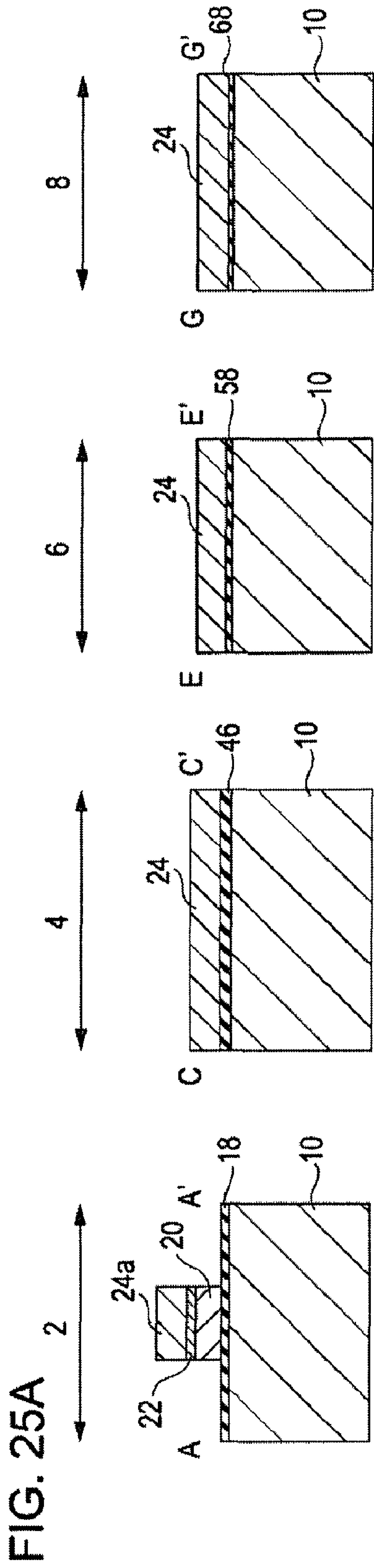
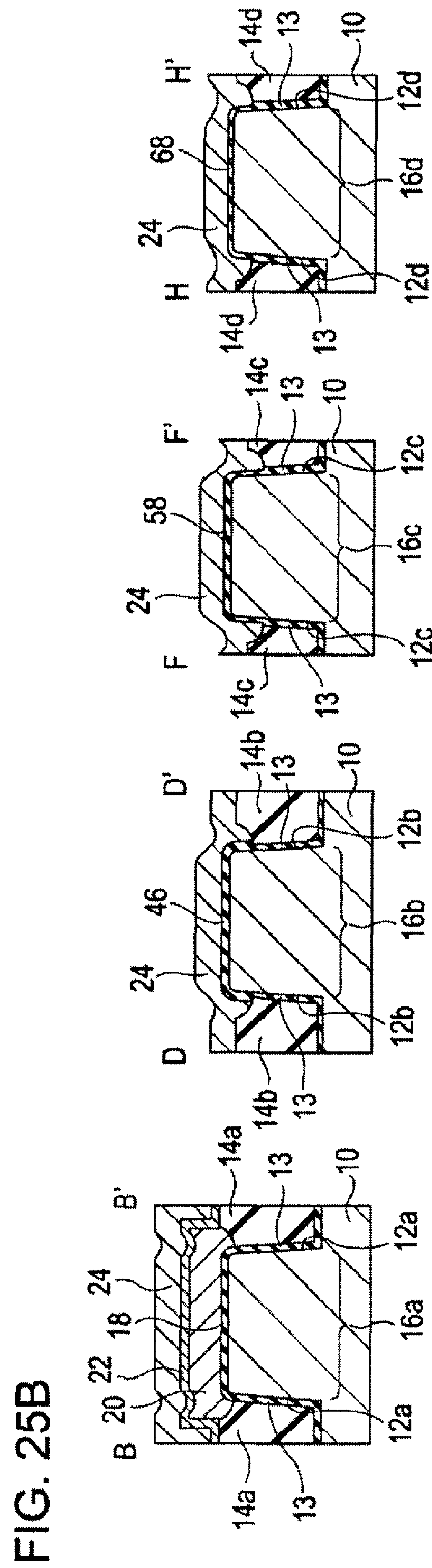


FIG. 25B



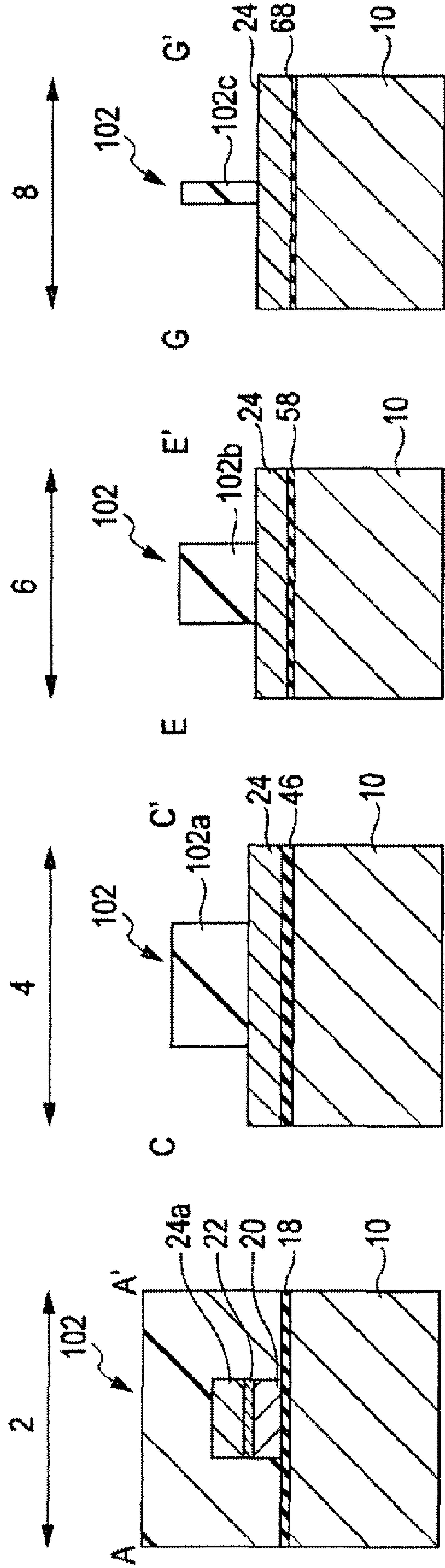


FIG. 26A

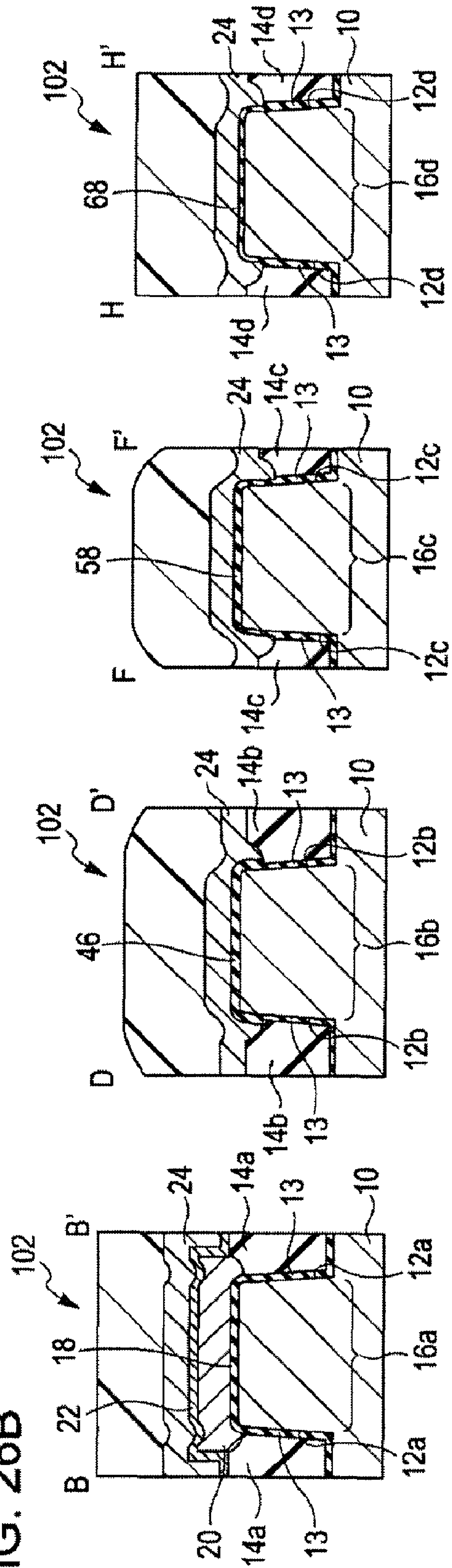


FIG. 26B

FIG. 27A

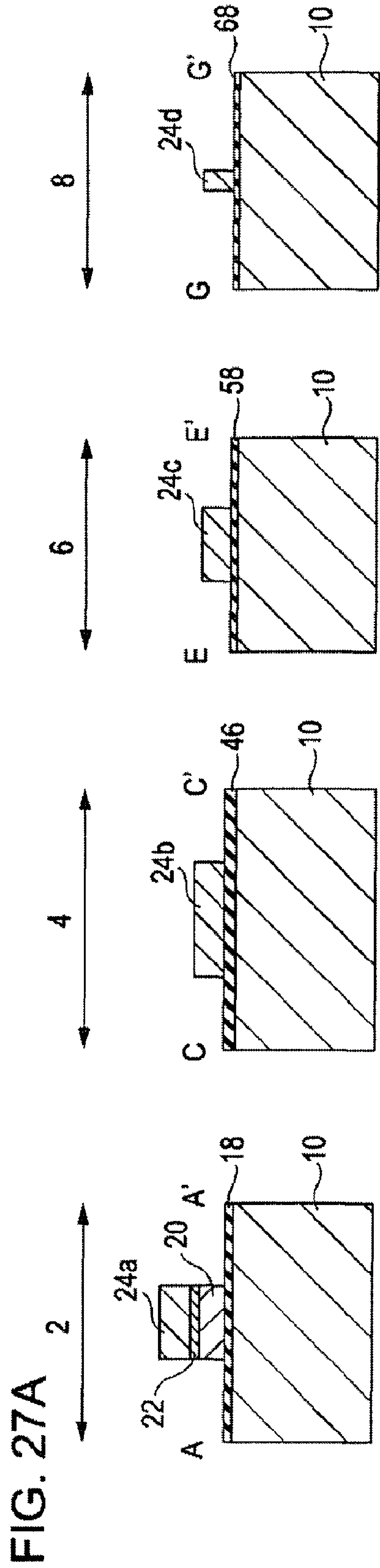
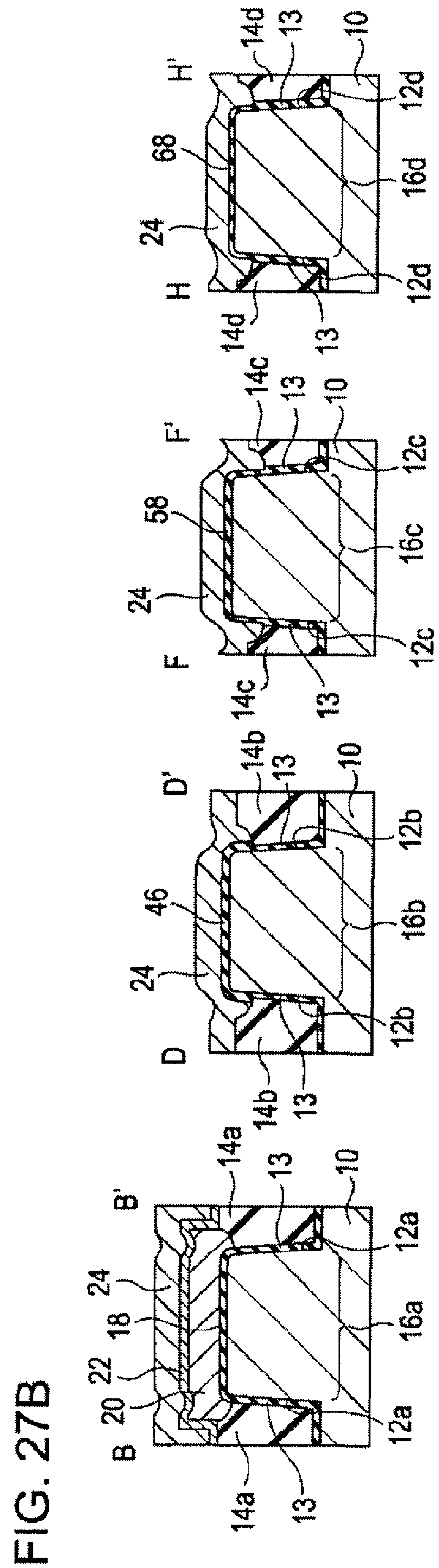


FIG. 27B



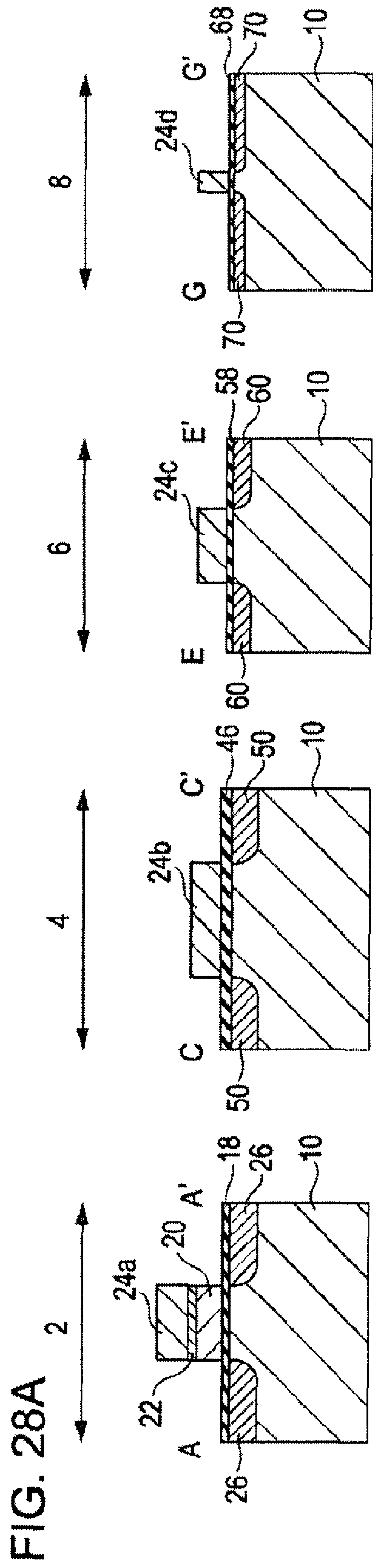


FIG. 28A
2
A
A'
24a
22
20
18
26
10
4
C
C'
24b
46
50
6
E
E'
24c
58
60
8
G
G'
24d
68
70

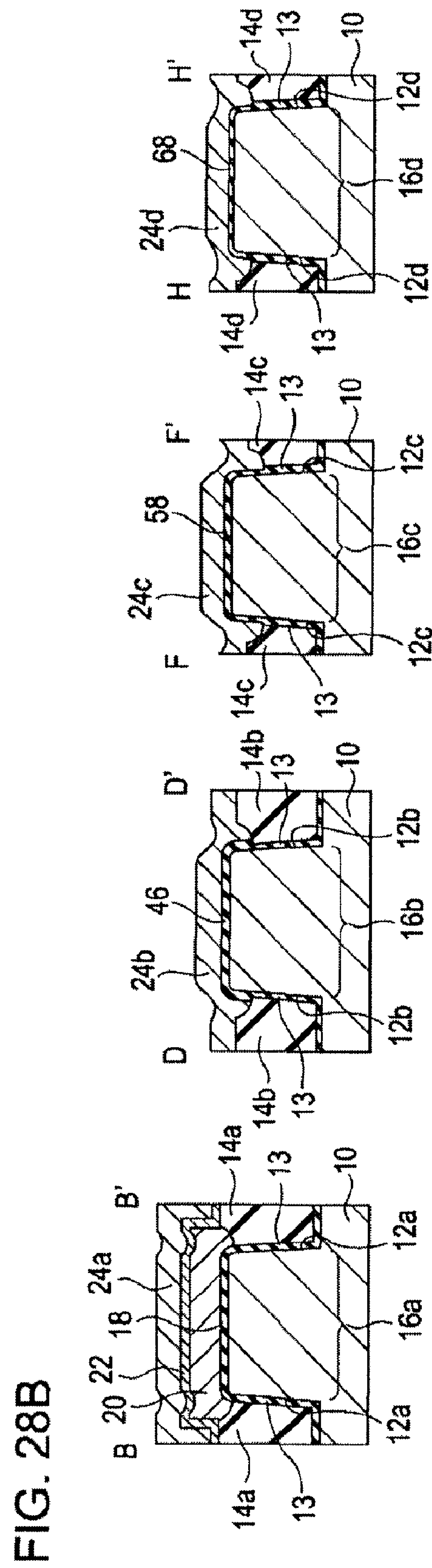


FIG. 28B
B
B'
24a
22
20
18
14a
13
12a
16a
10
D
D'
24b
46
14b
12b
16b
F
F'
24c
58
14c
12c
16c
H
H'
24d
68
14d
12d
16d

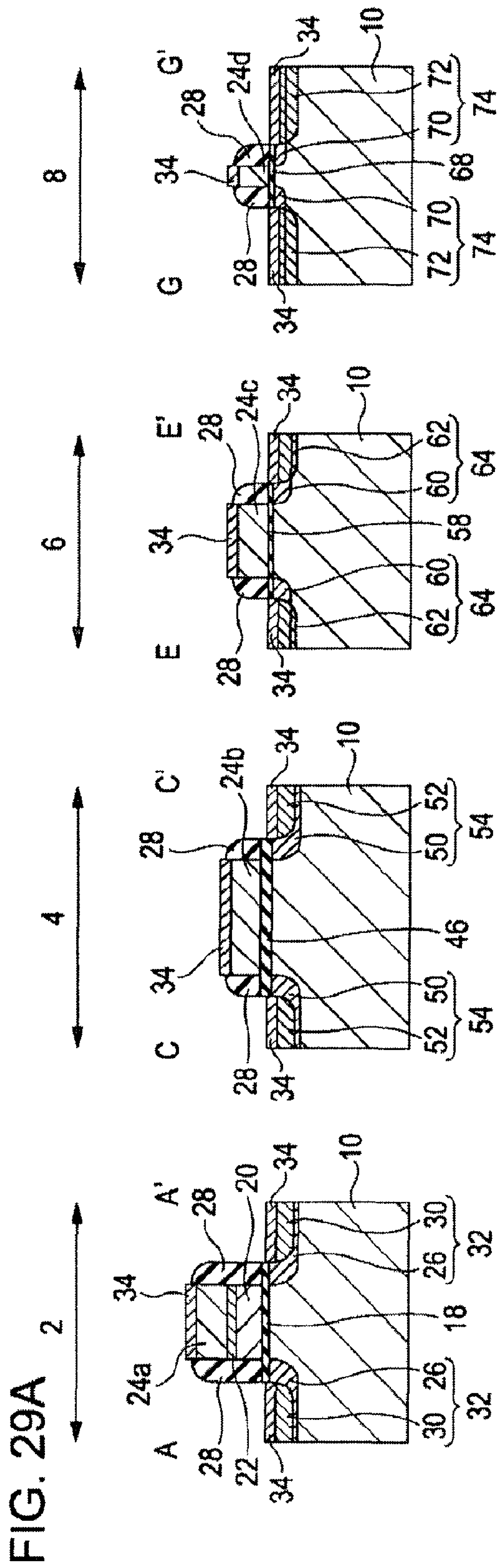


FIG. 29A

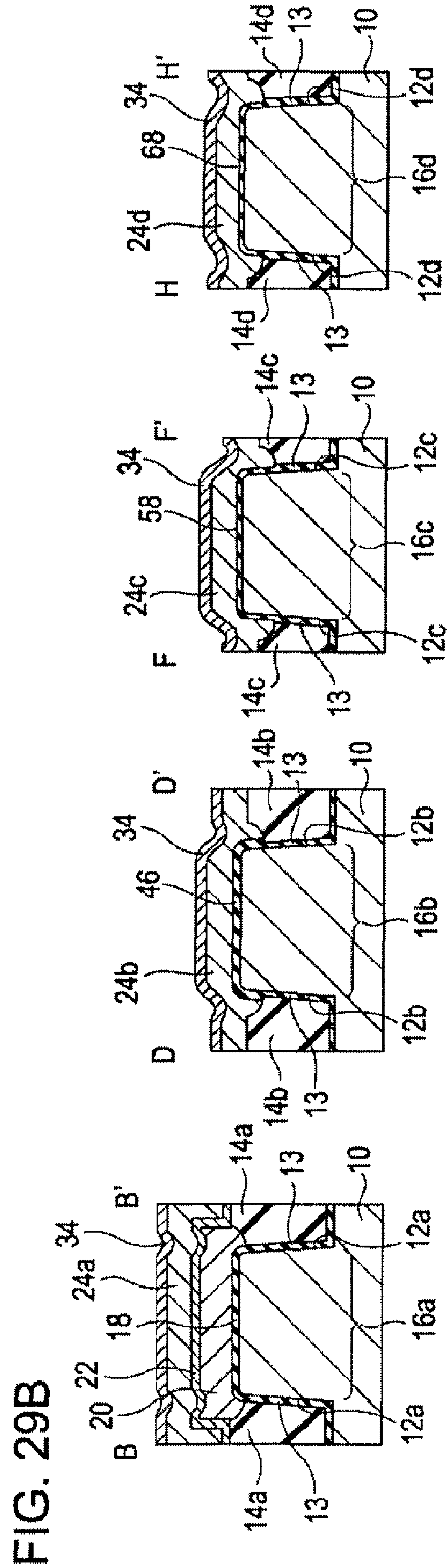


FIG. 29B

FIG. 30A

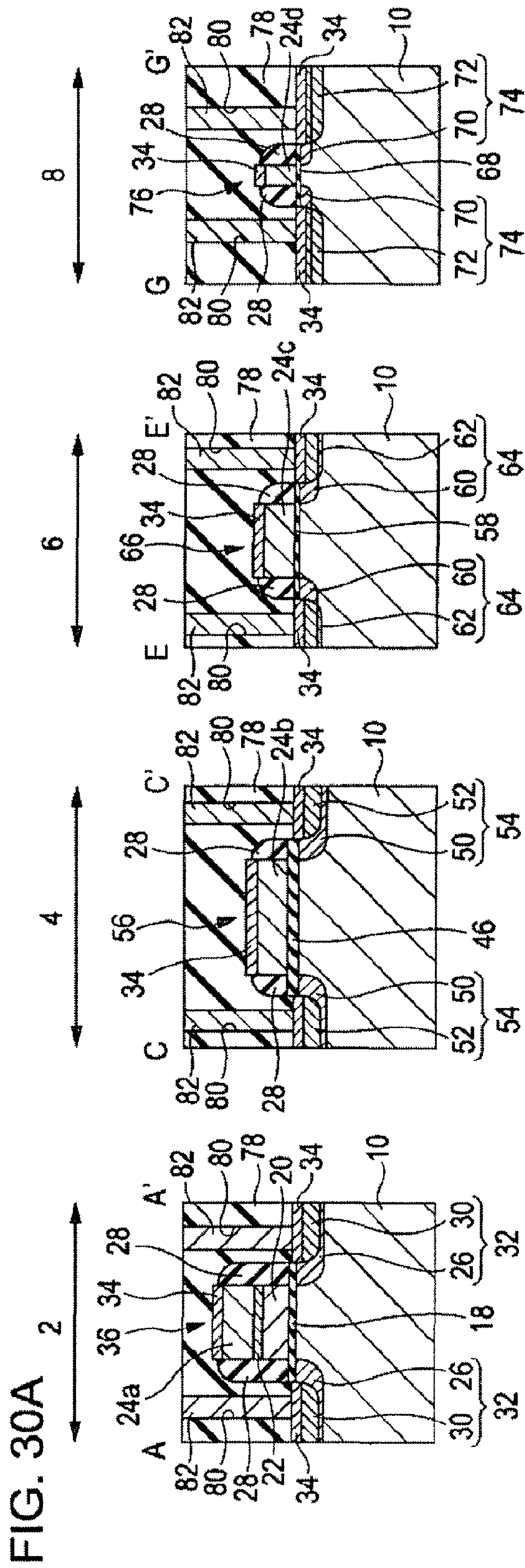
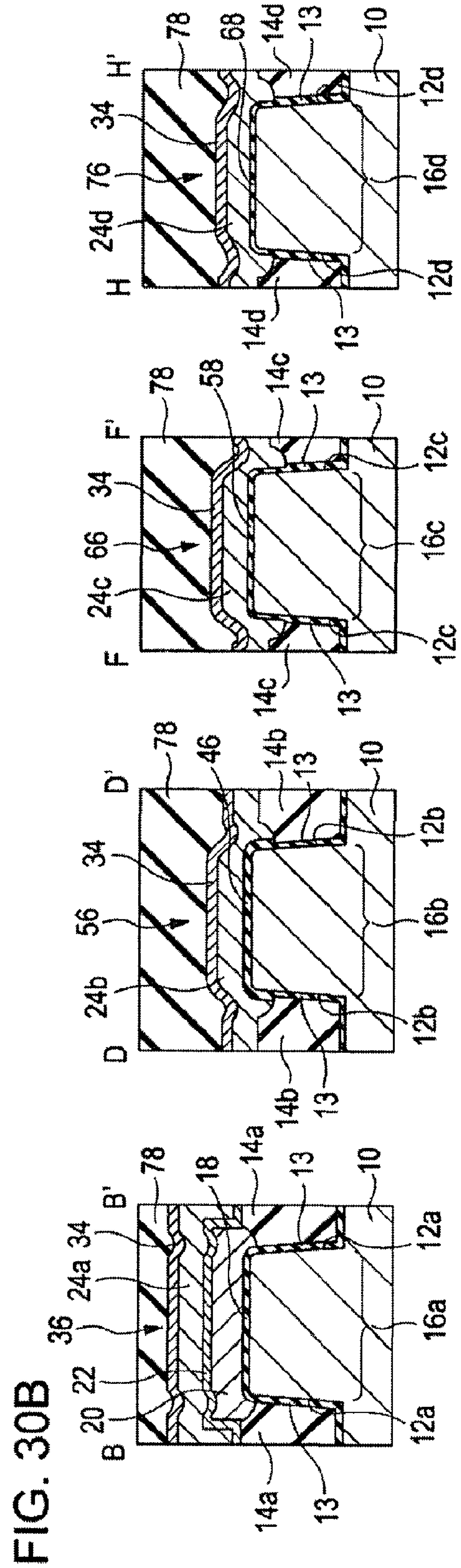


FIG. 30B



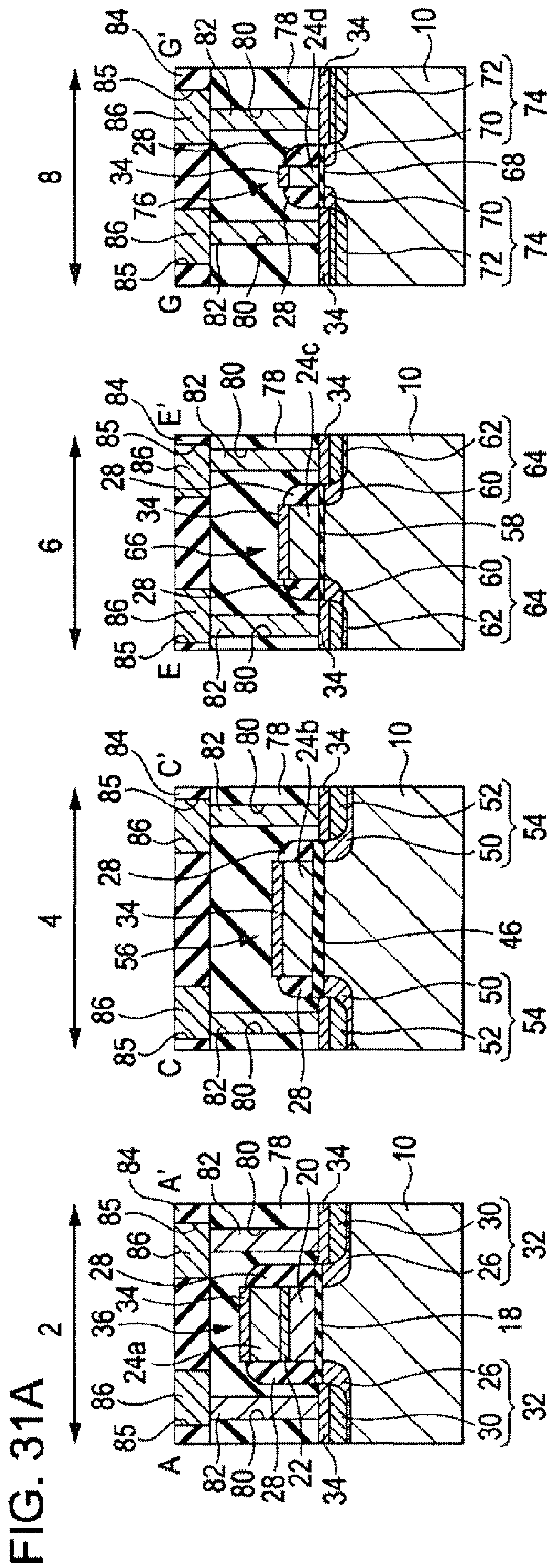


FIG. 31A

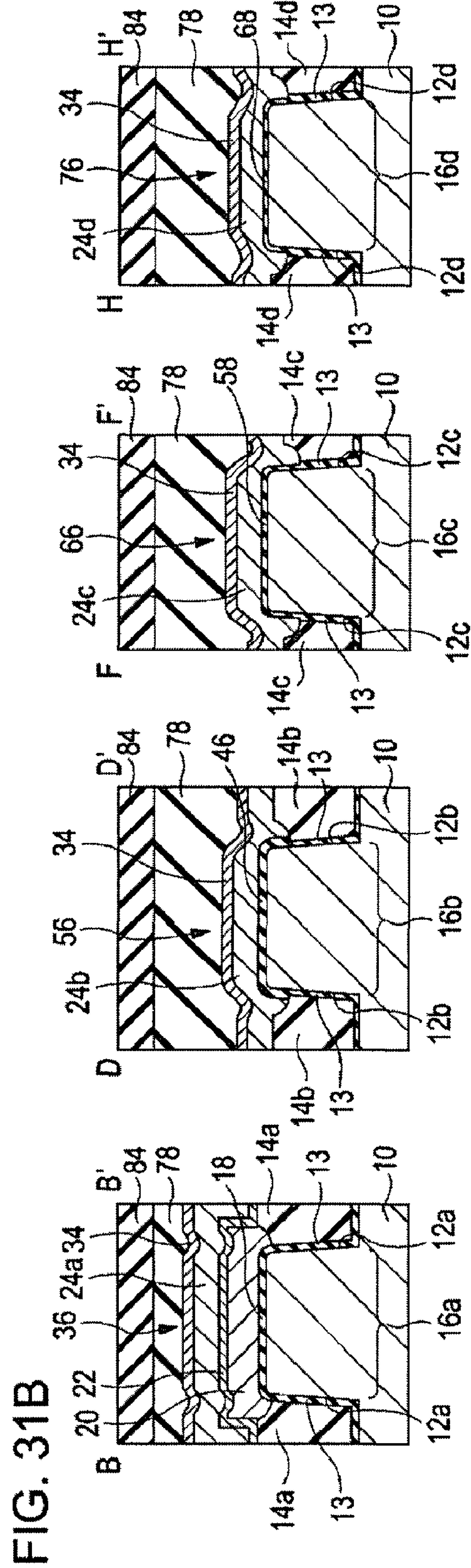


FIG. 31B

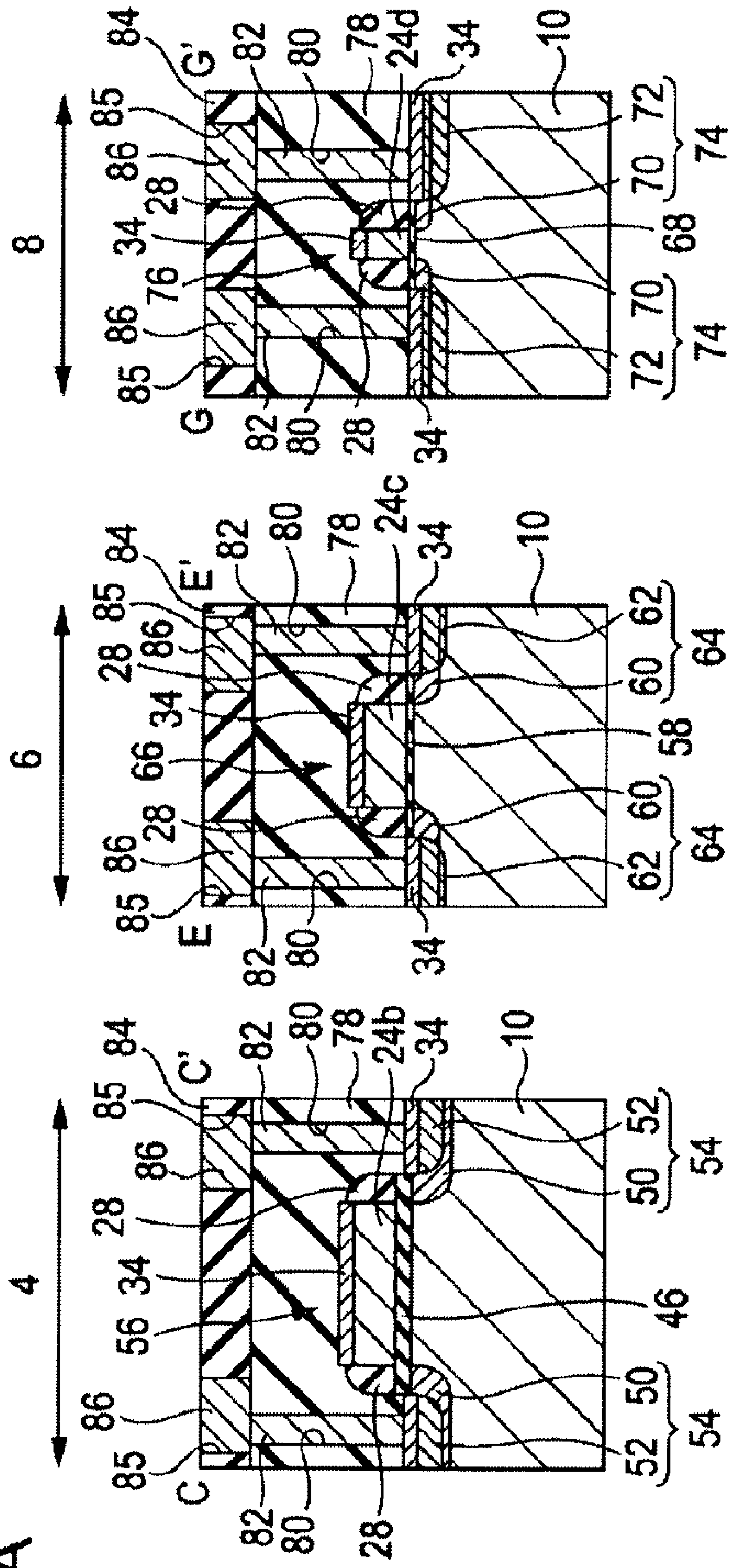


FIG. 32A

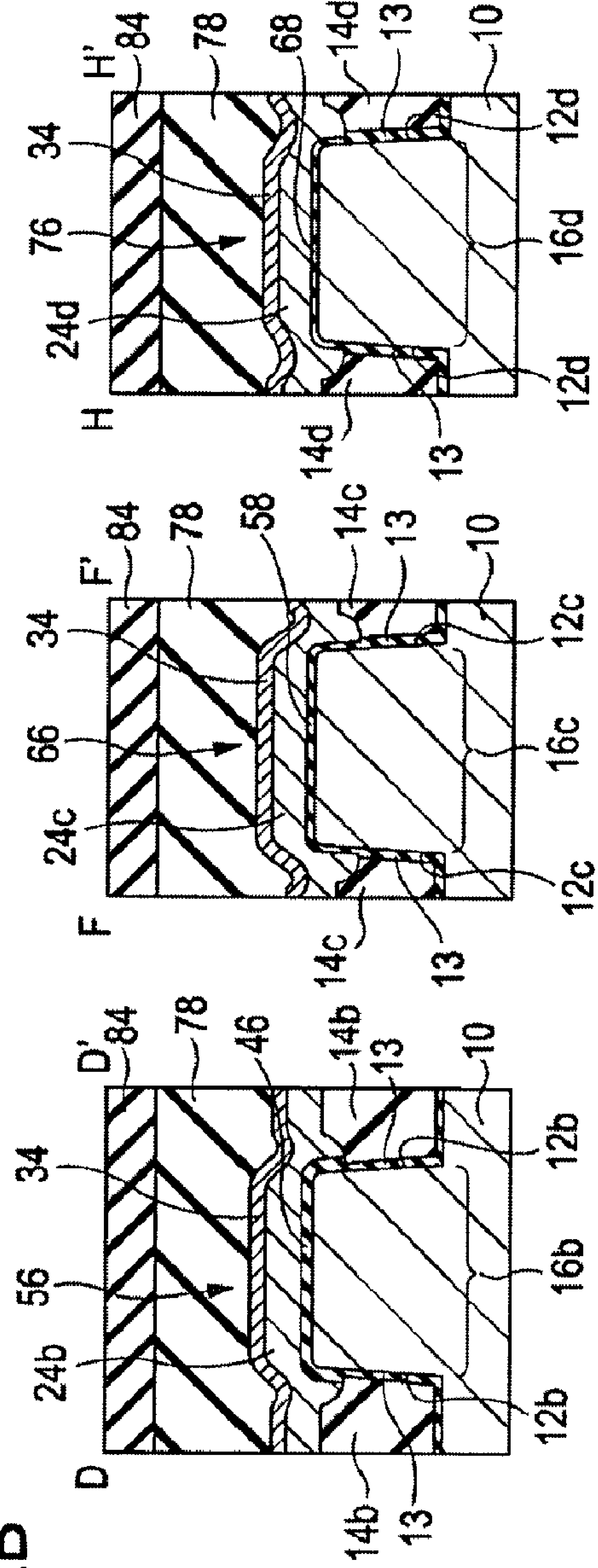


FIG. 32B

FIG.33A

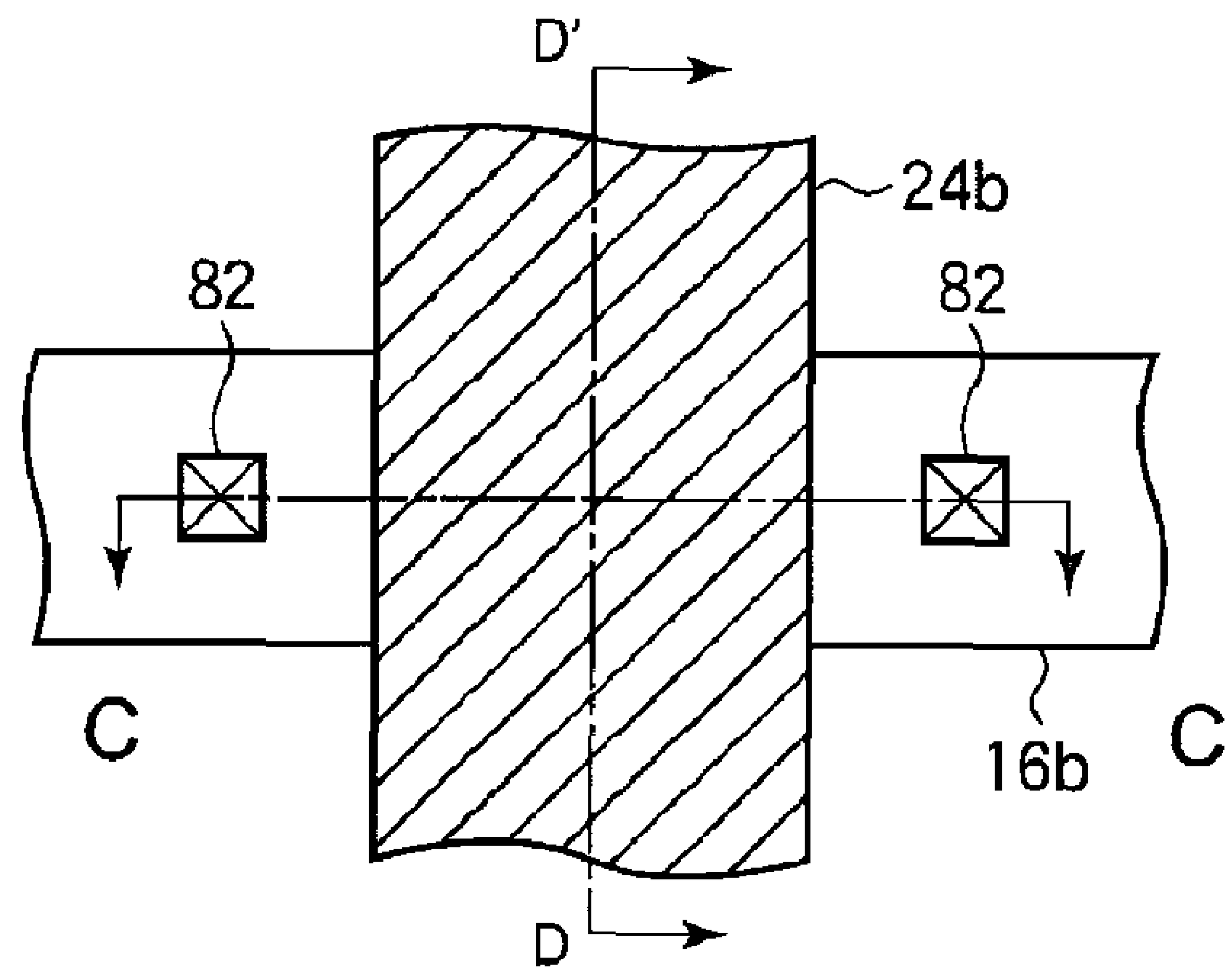


FIG.33B

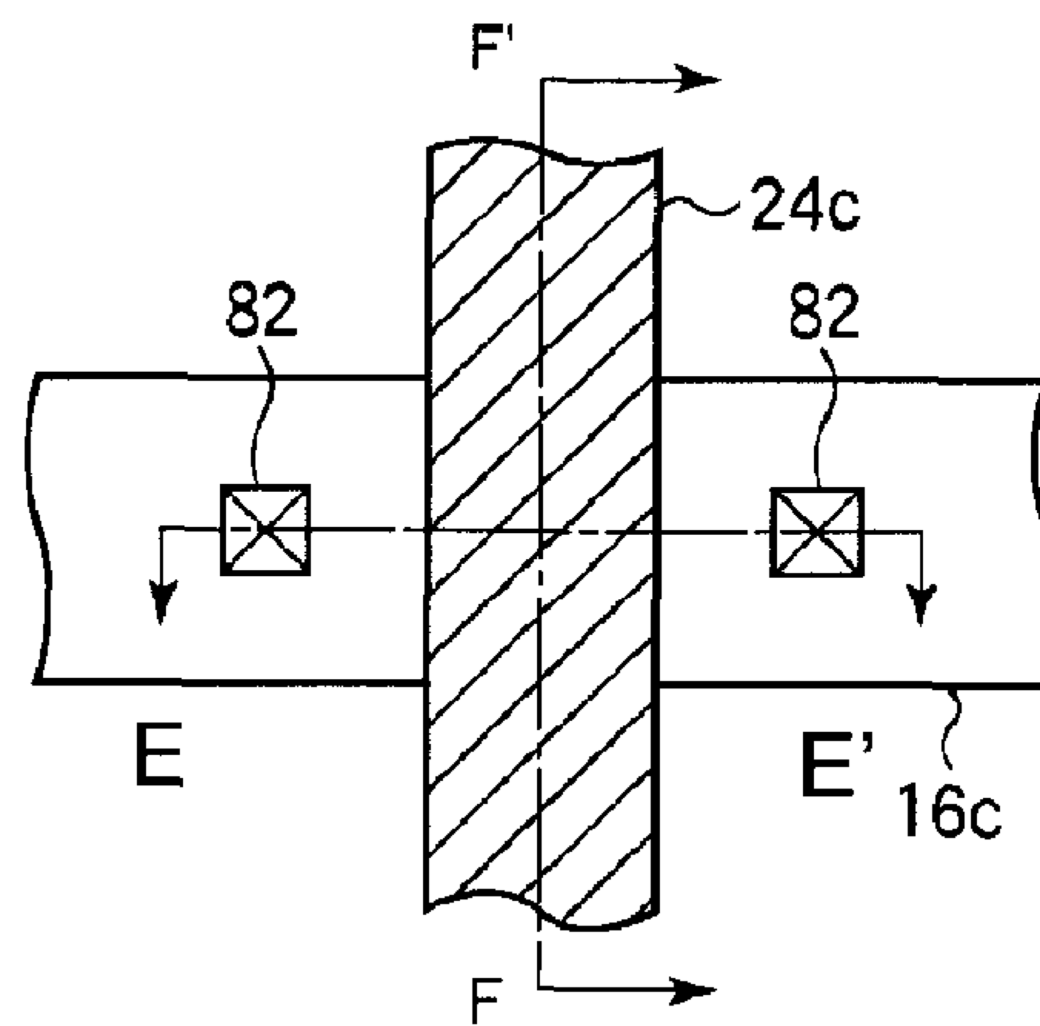
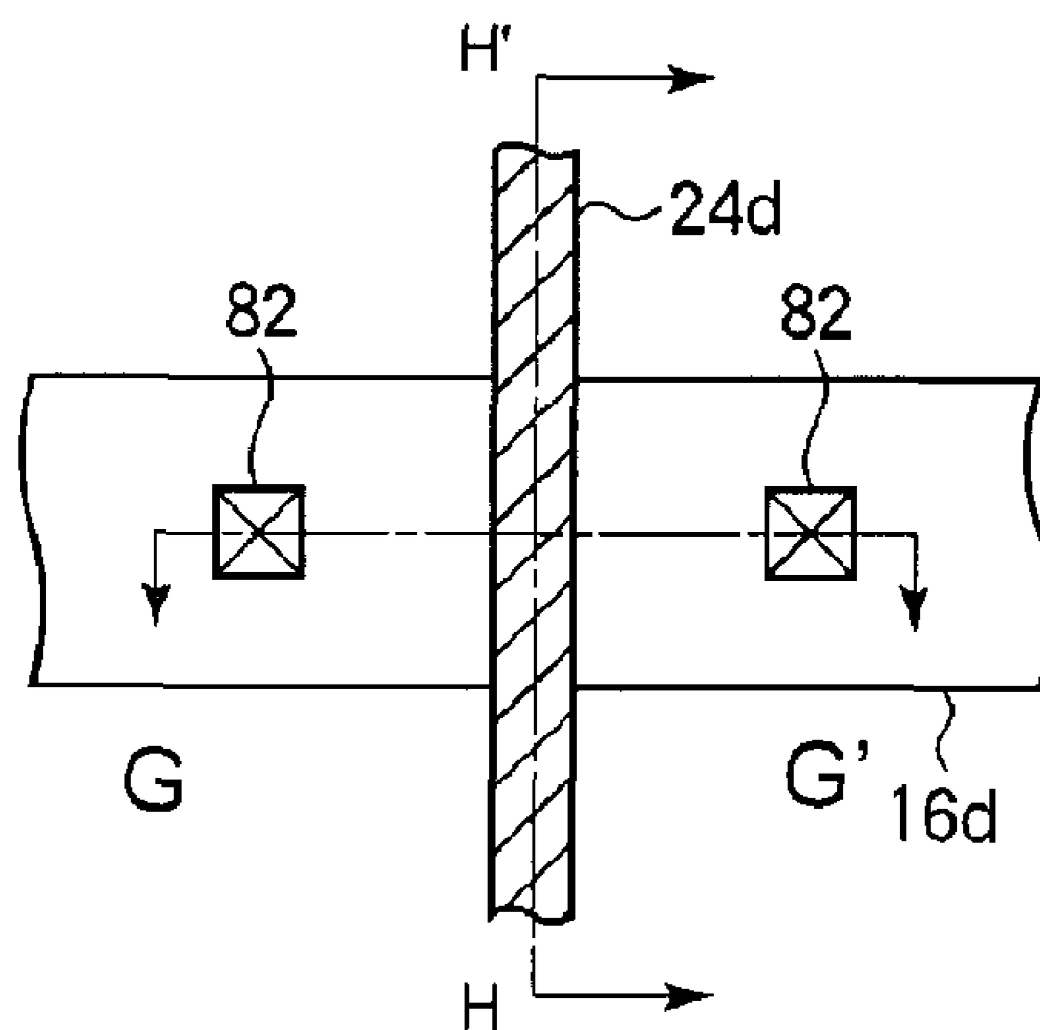


FIG.33C



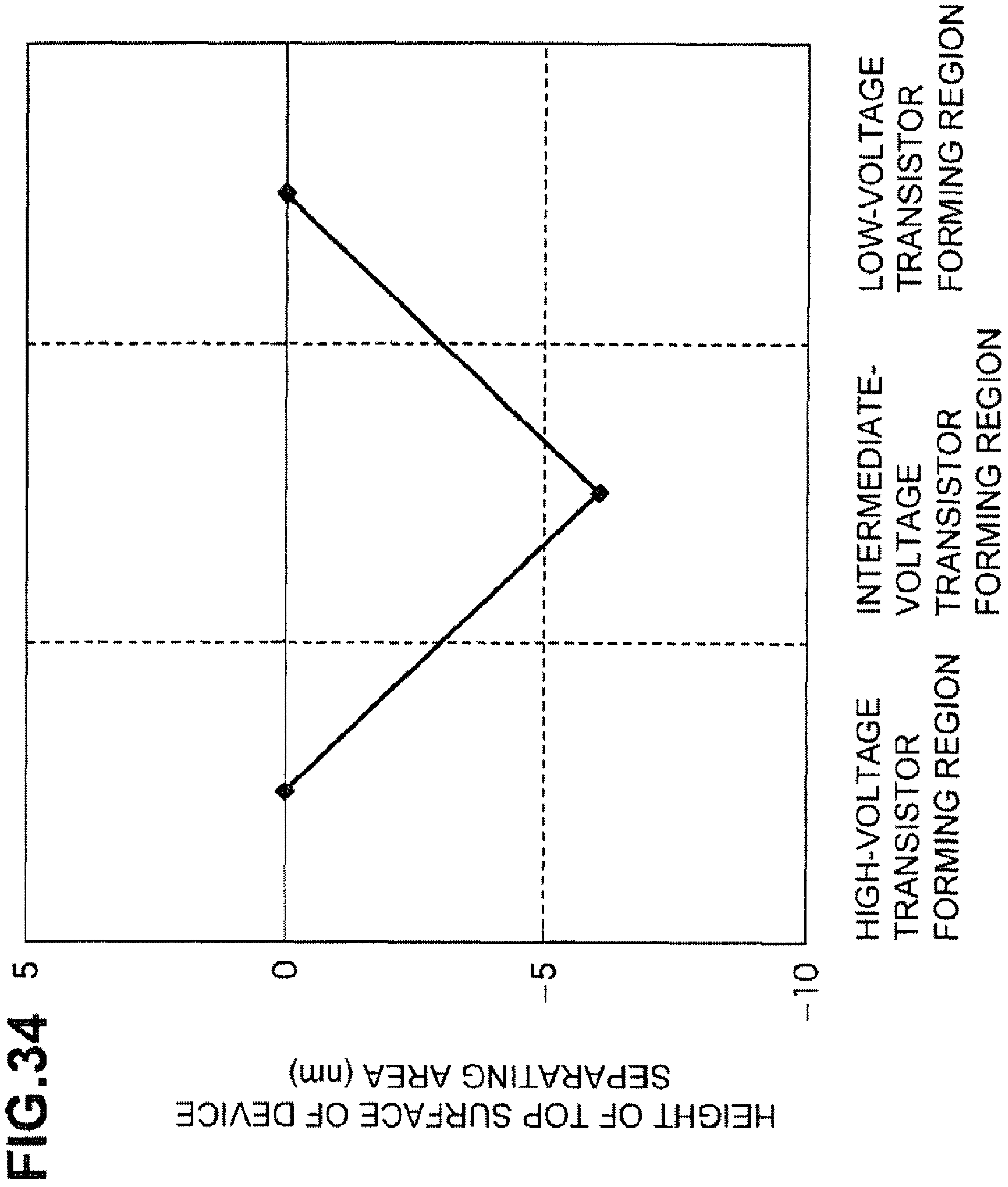


FIG.34

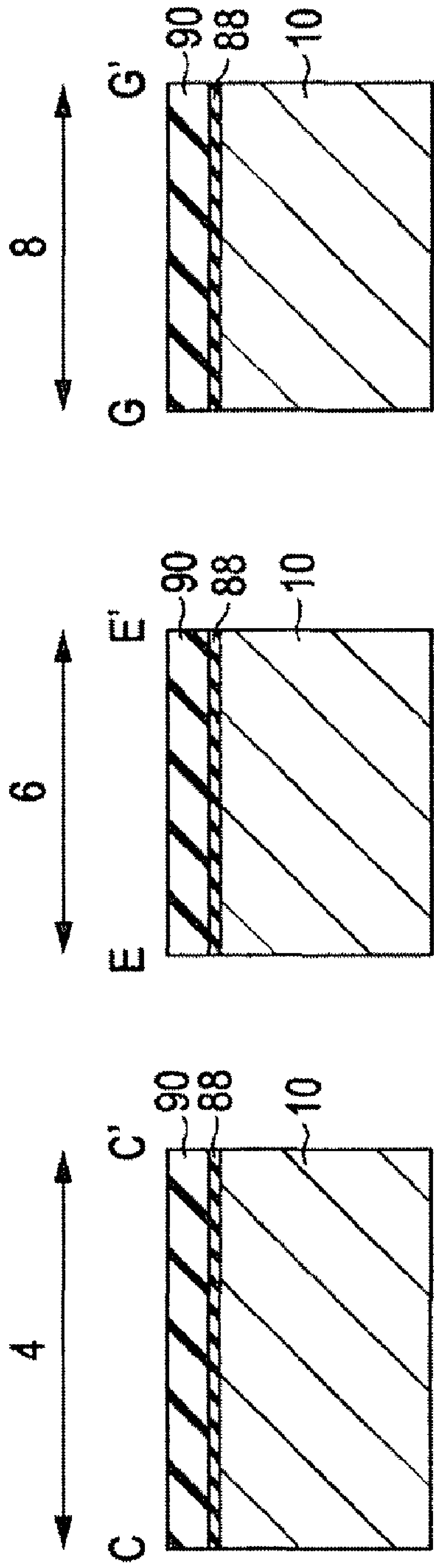


FIG. 35A

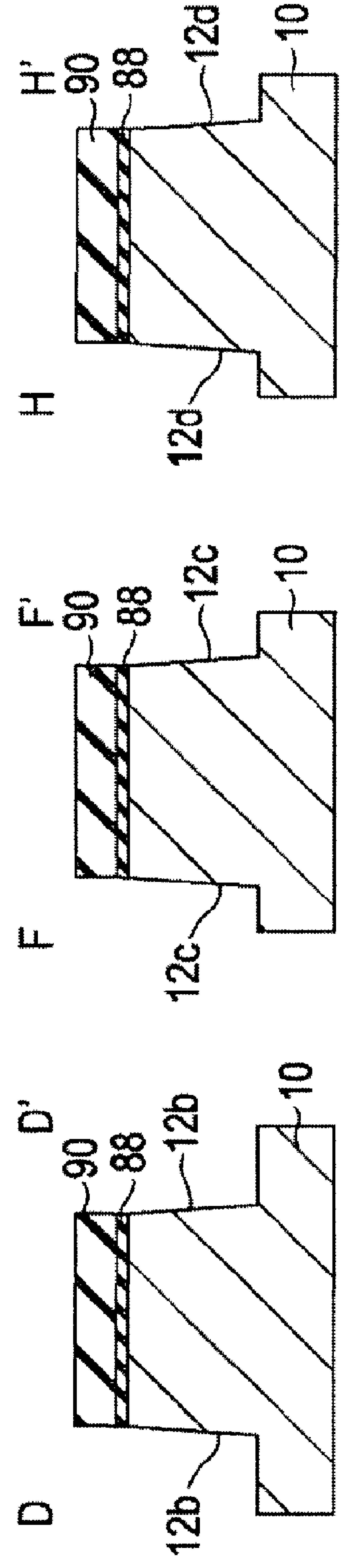


FIG. 35B

FIG. 36A

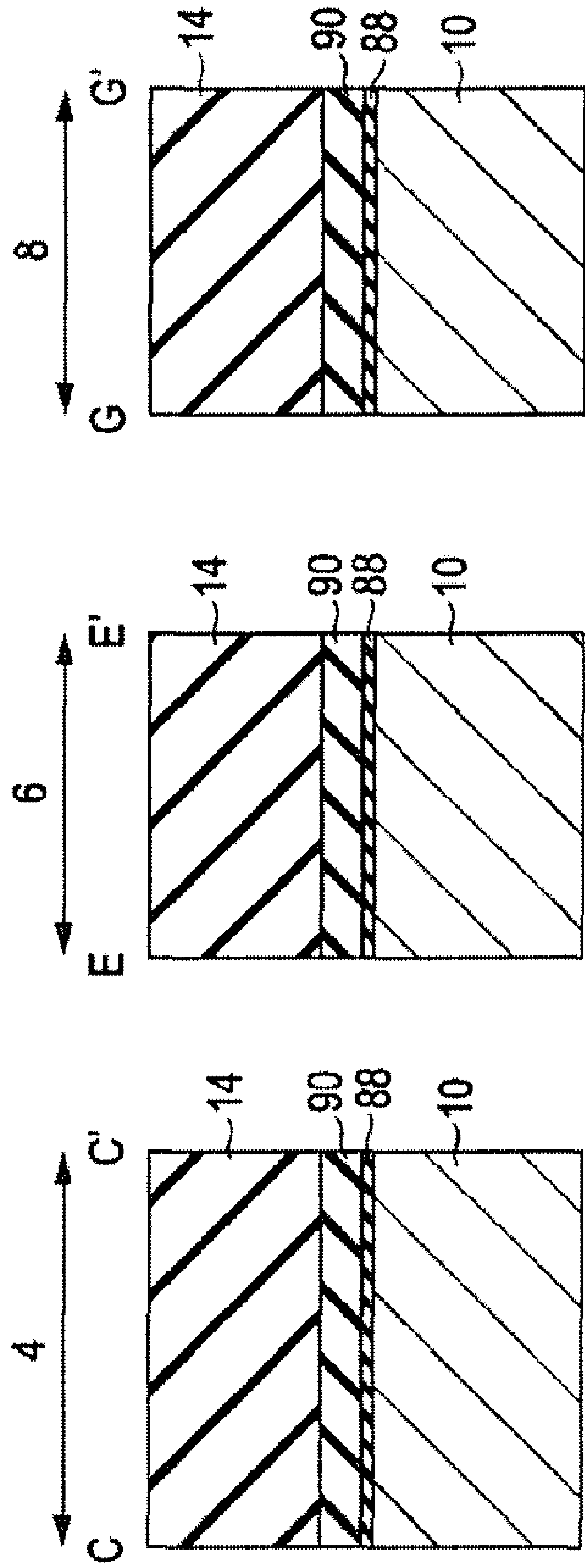


FIG. 36B

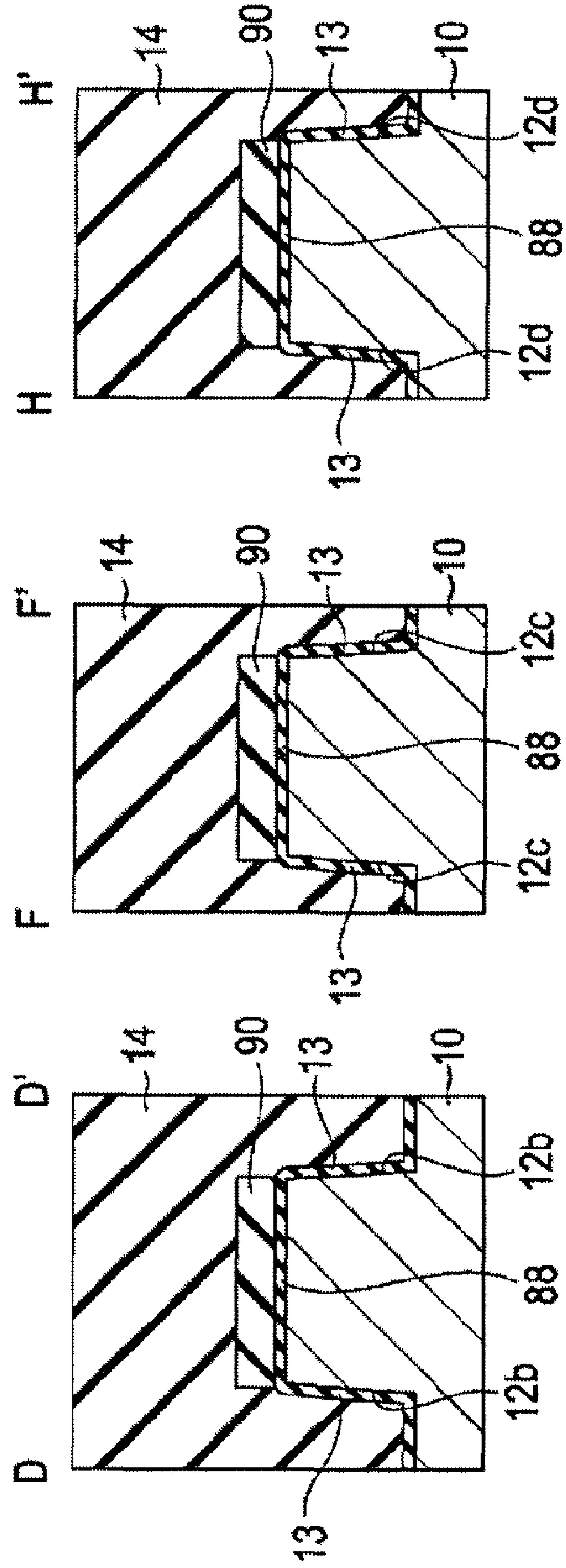


FIG. 37A

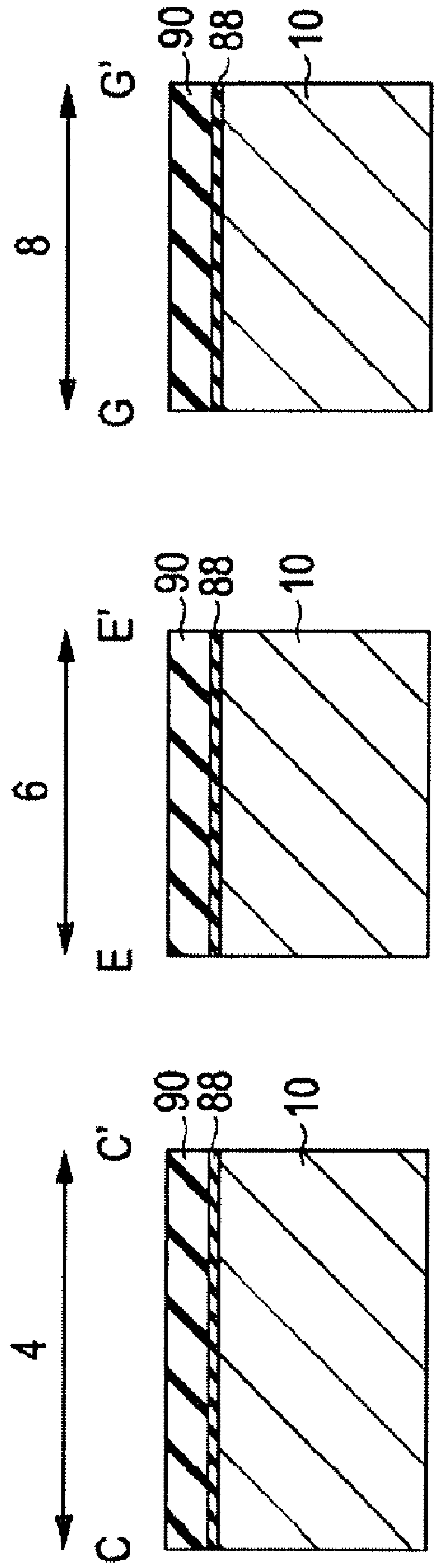


FIG. 37B

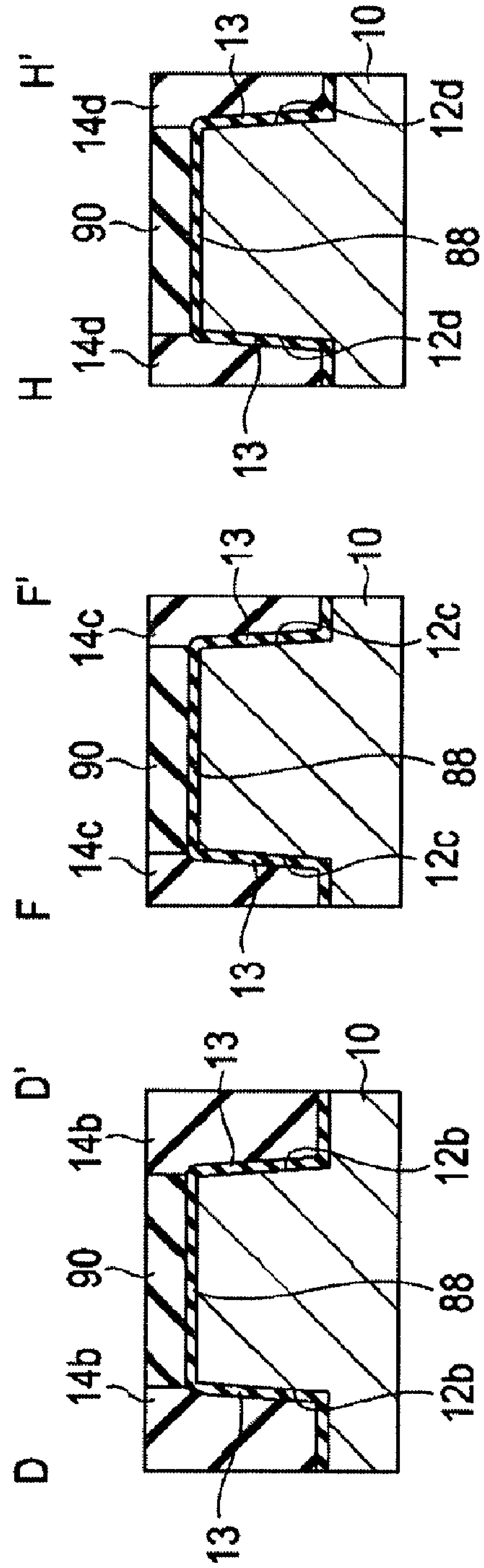


FIG. 38A

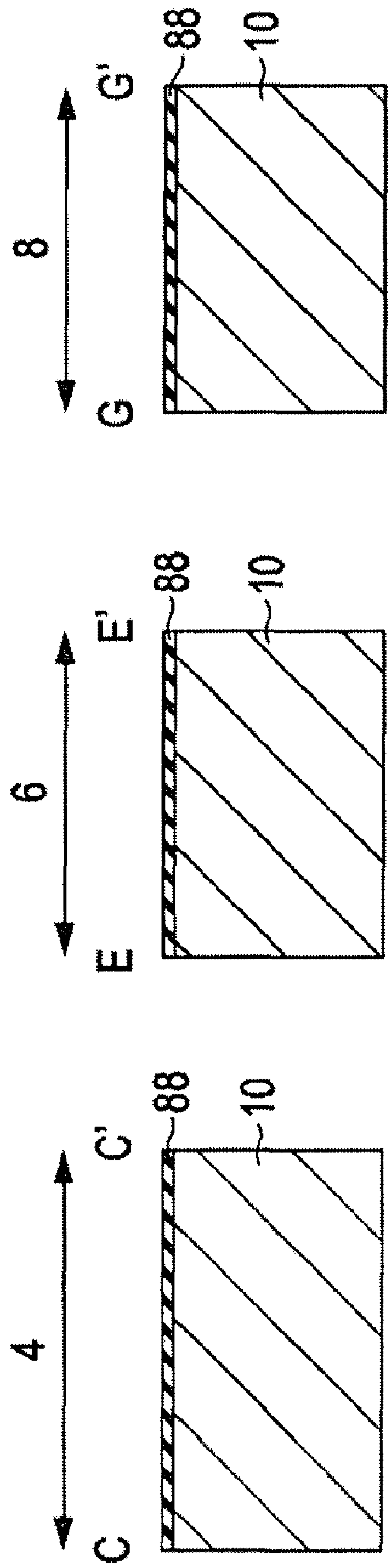
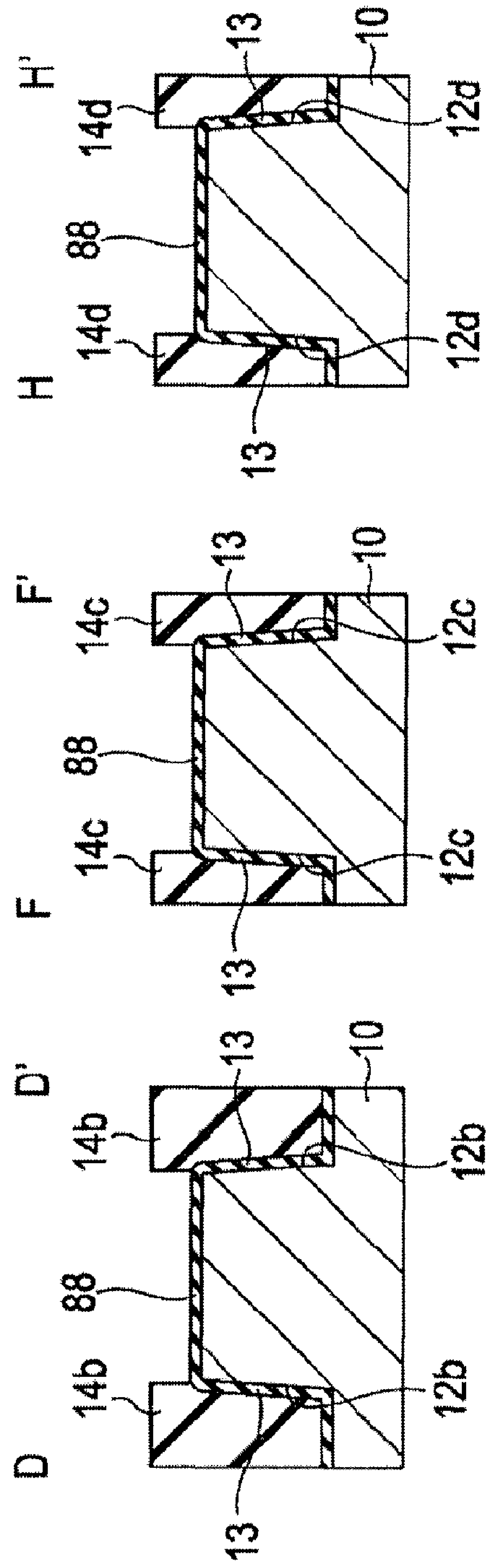


FIG. 38B



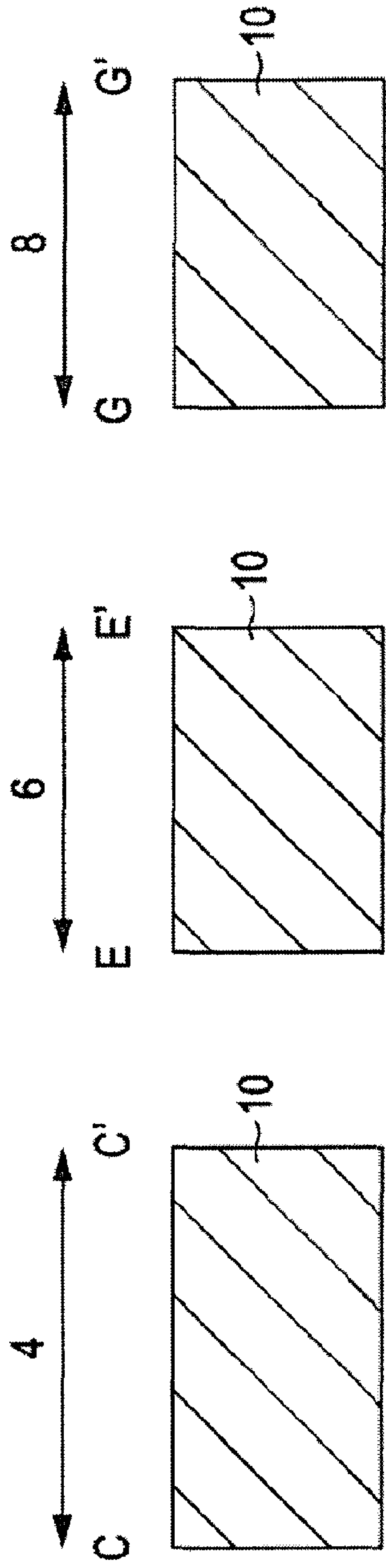


FIG. 39A

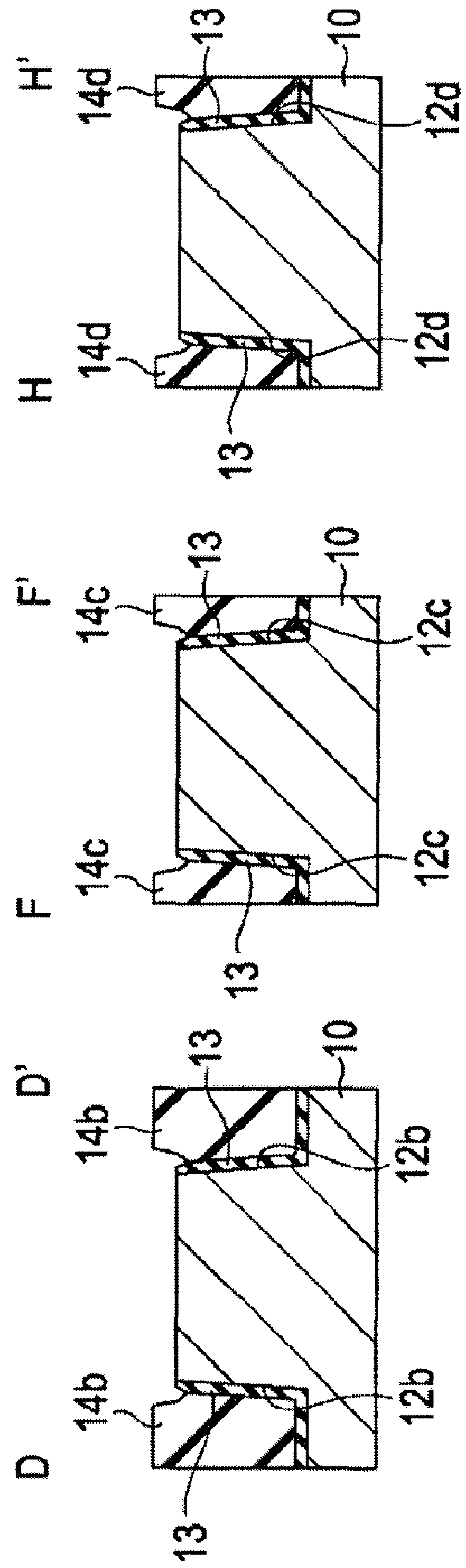


FIG. 39B

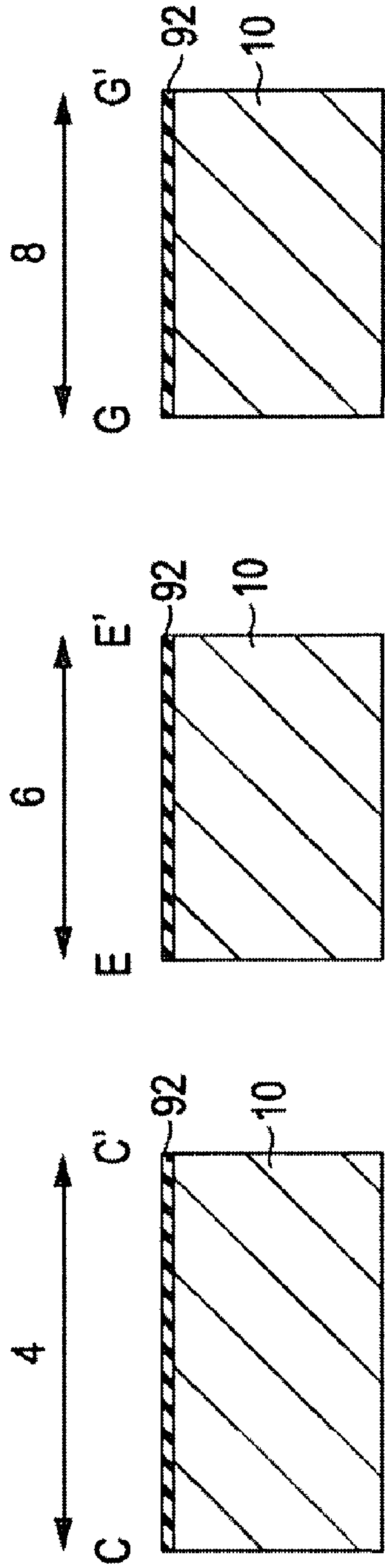


FIG. 40A

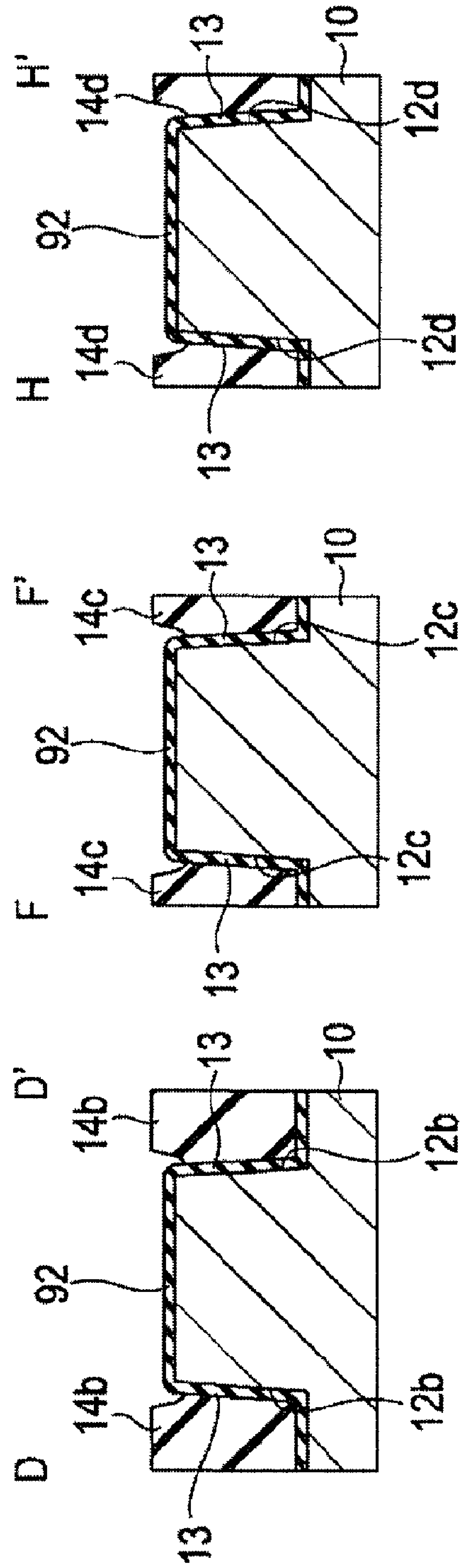


FIG. 40B

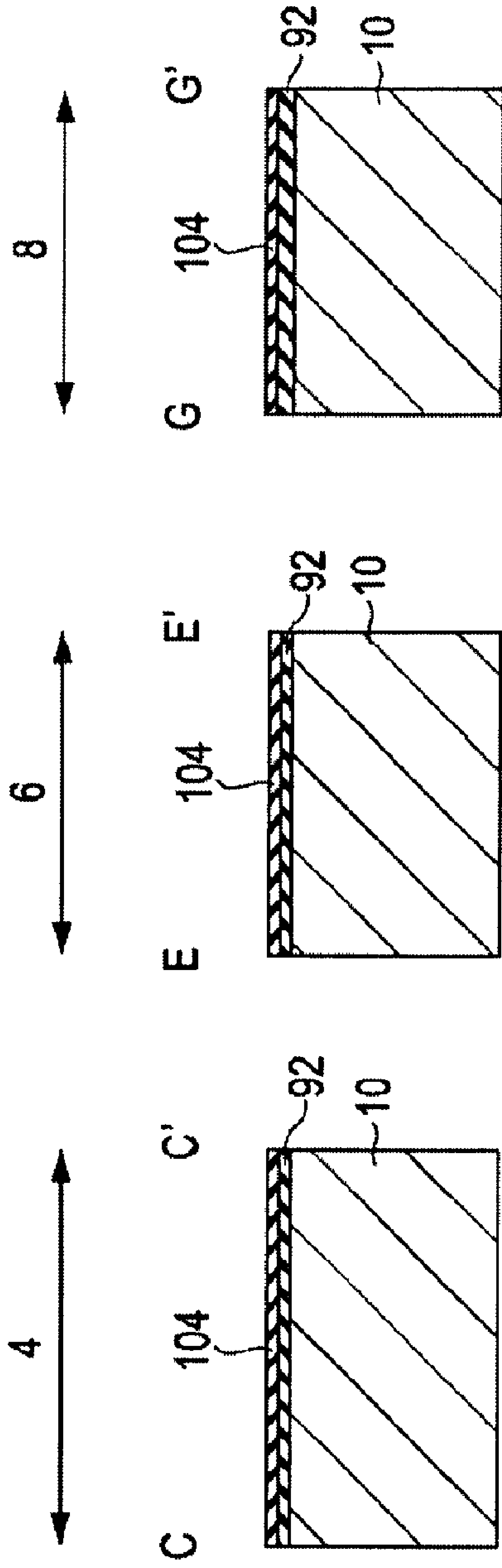


FIG. 41A

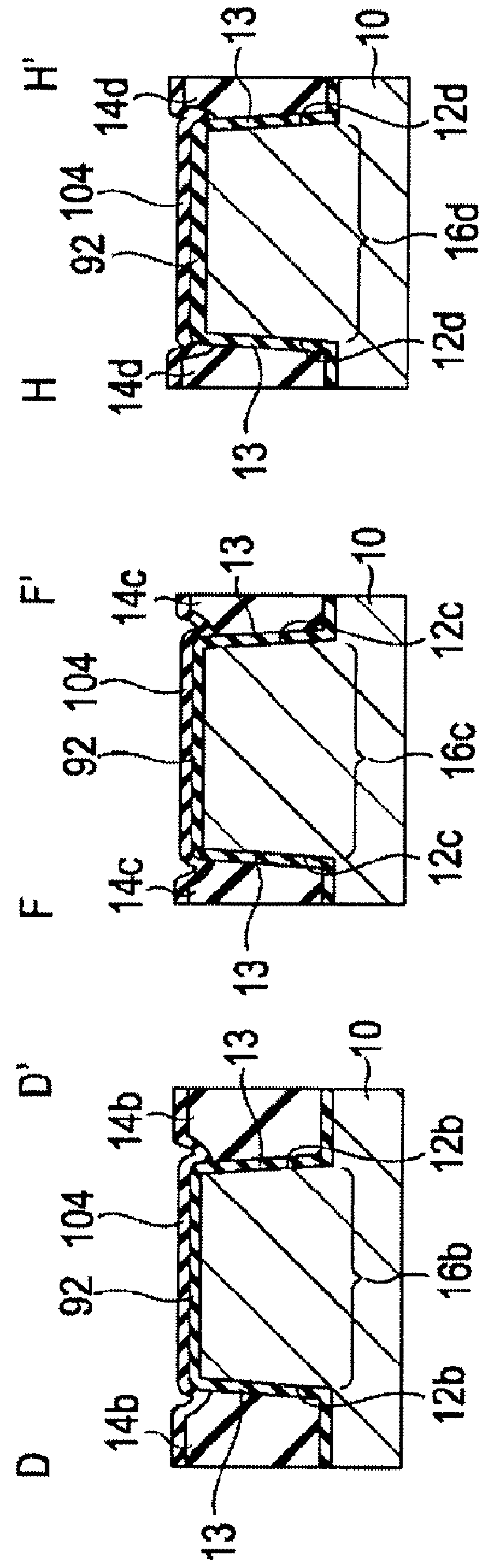


FIG. 41B

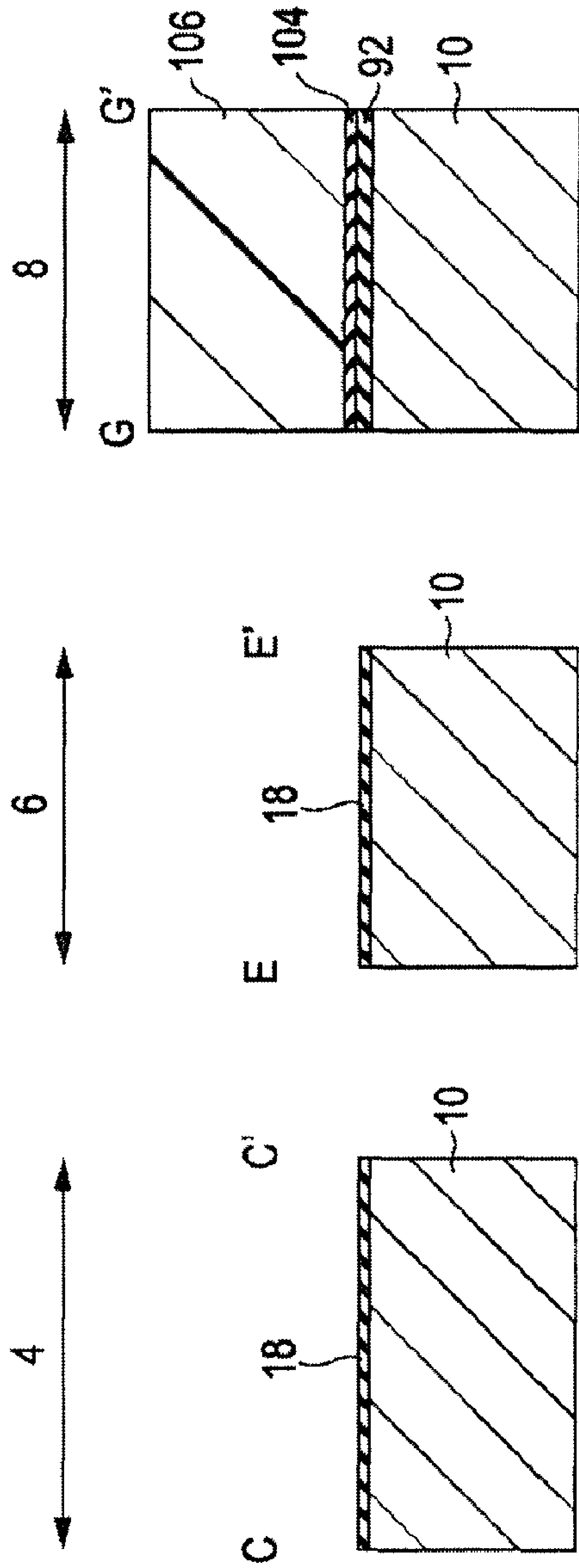


FIG. 42A

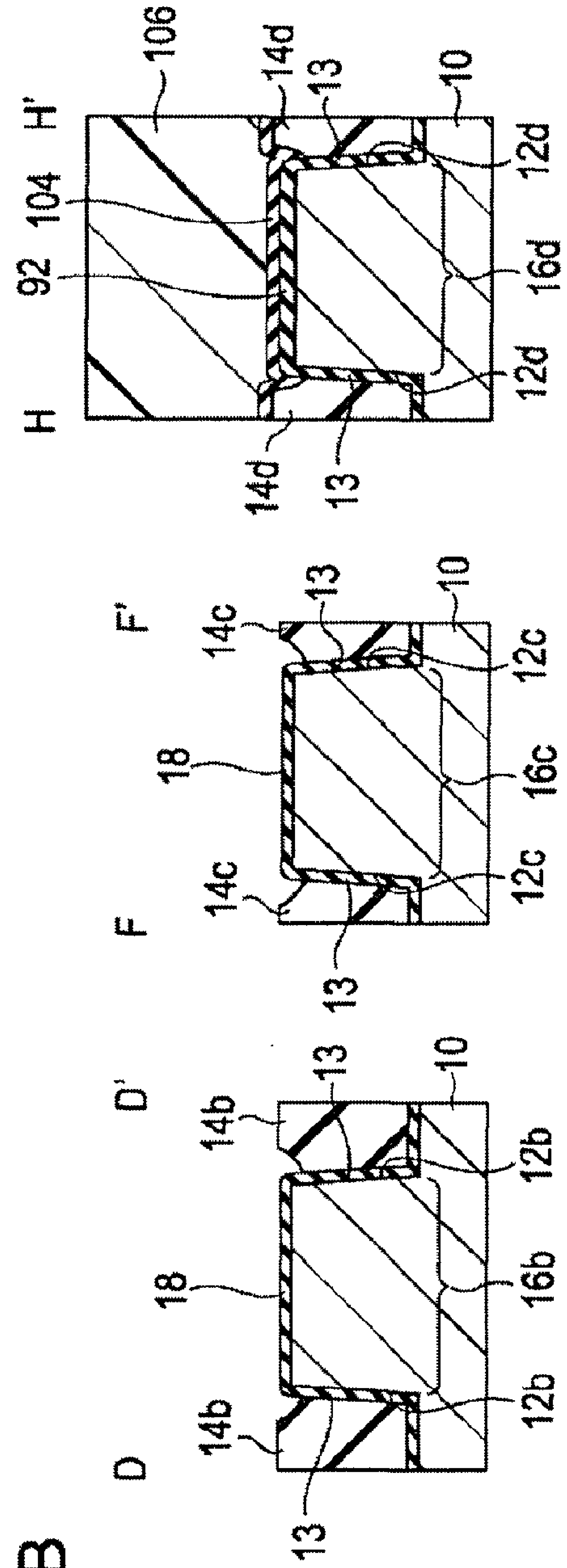


FIG. 42B

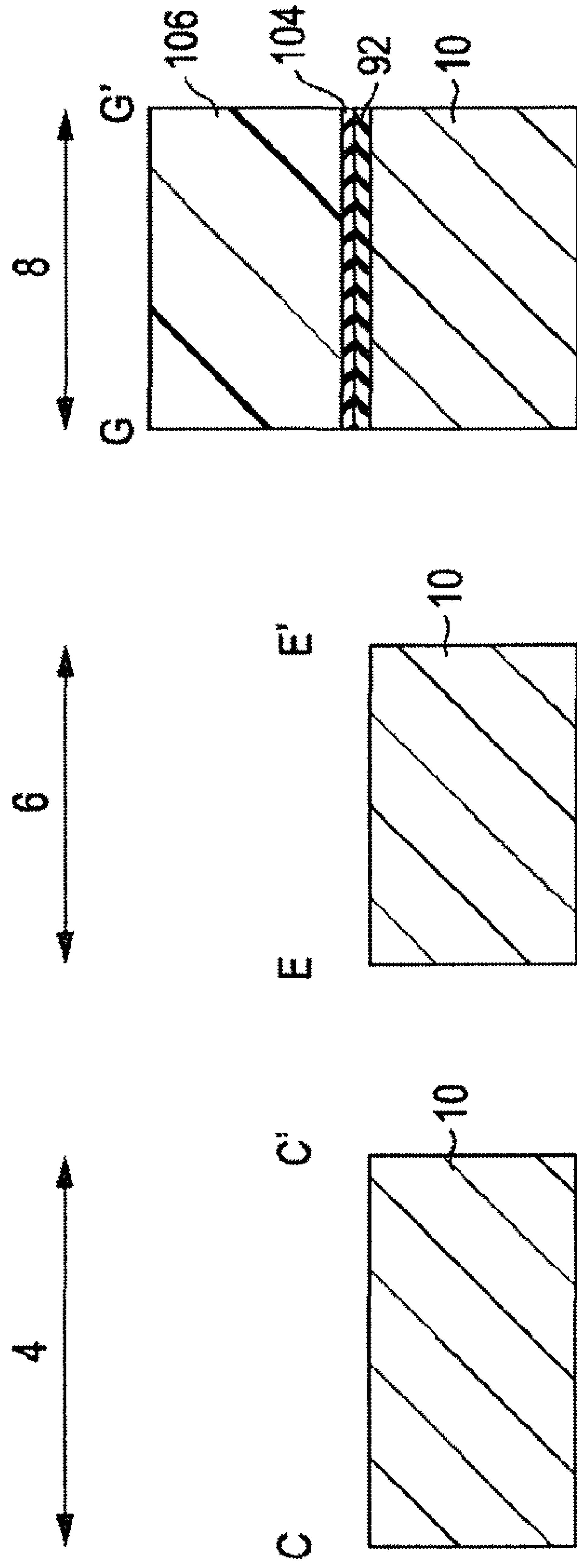


FIG. 43A

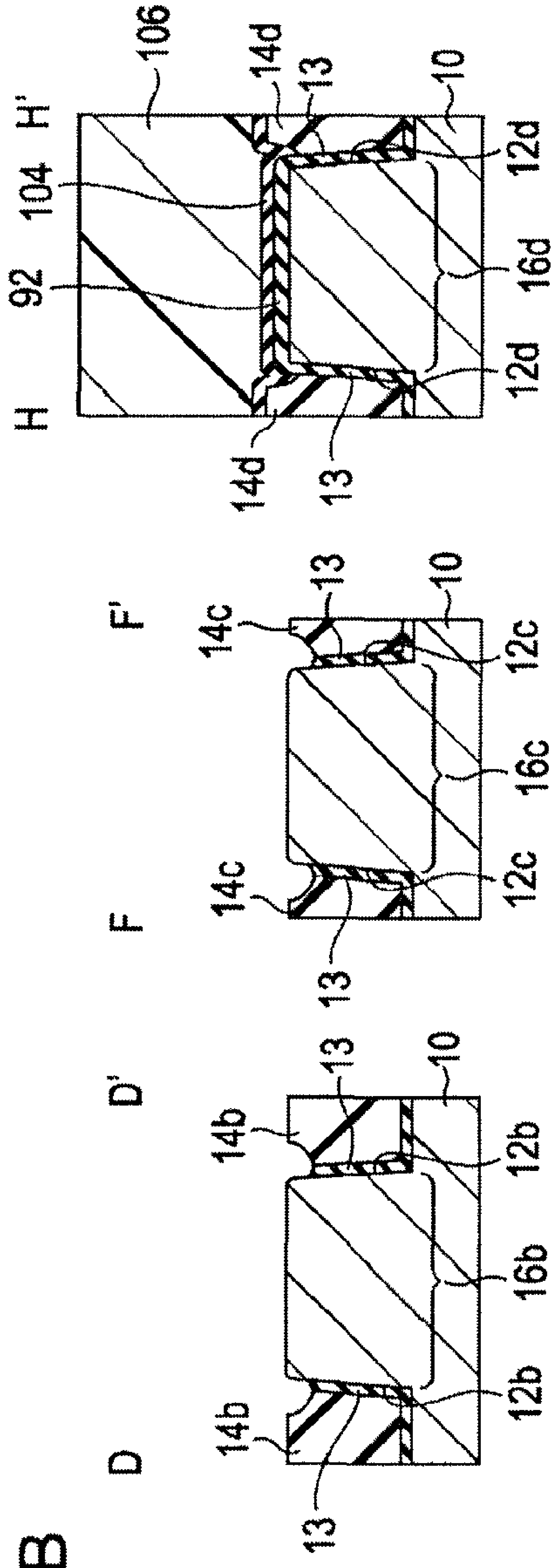


FIG. 43B

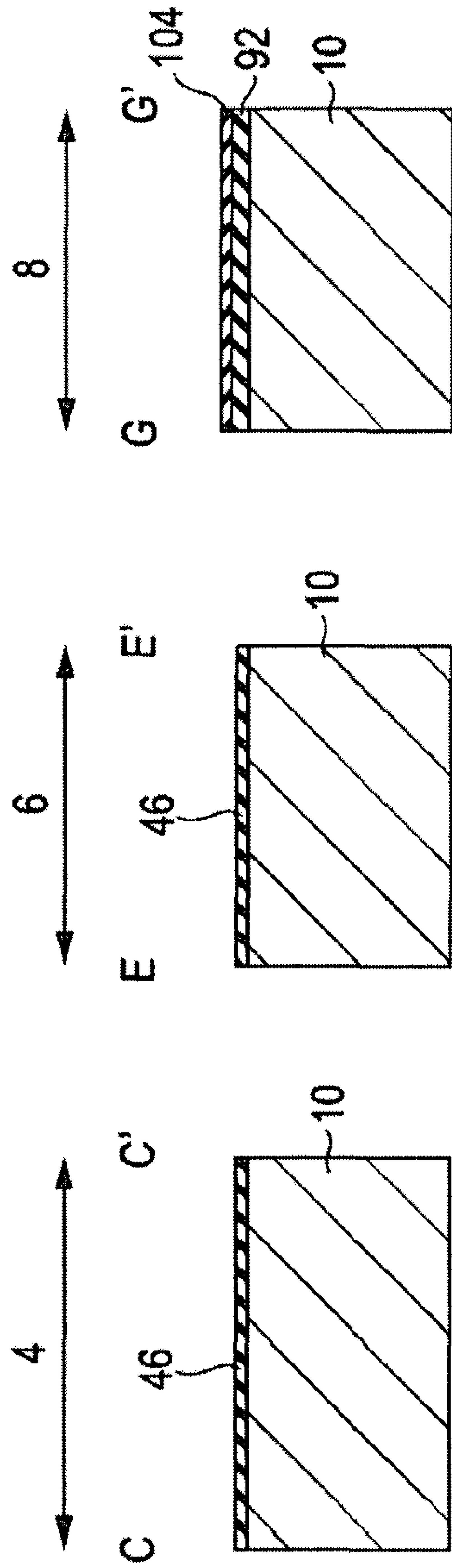


FIG. 44A

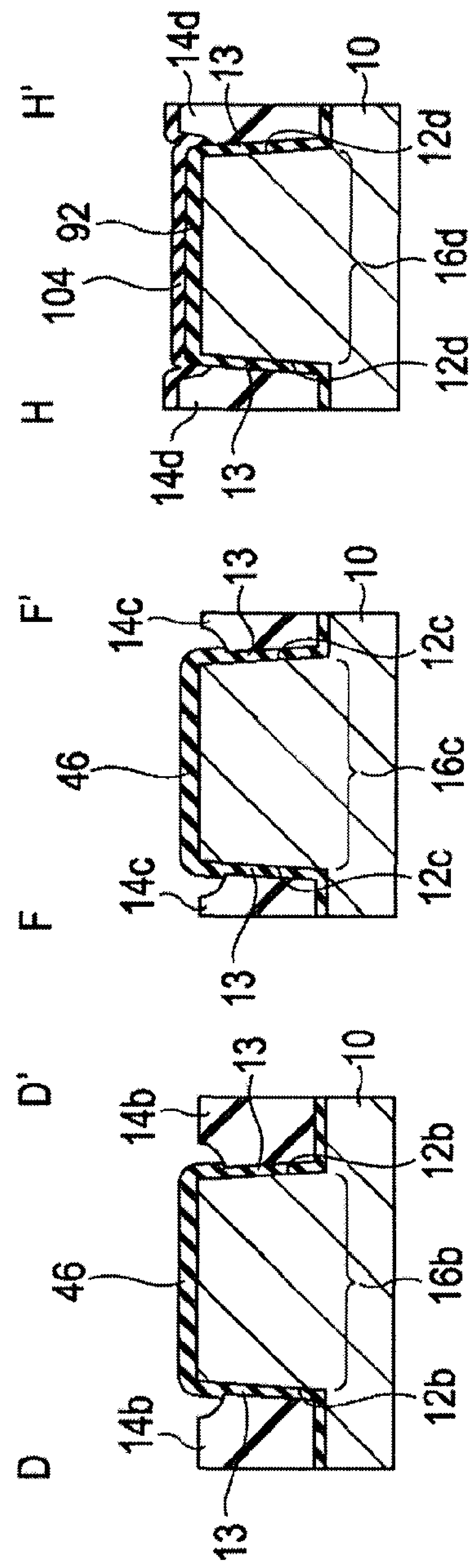


FIG. 44B

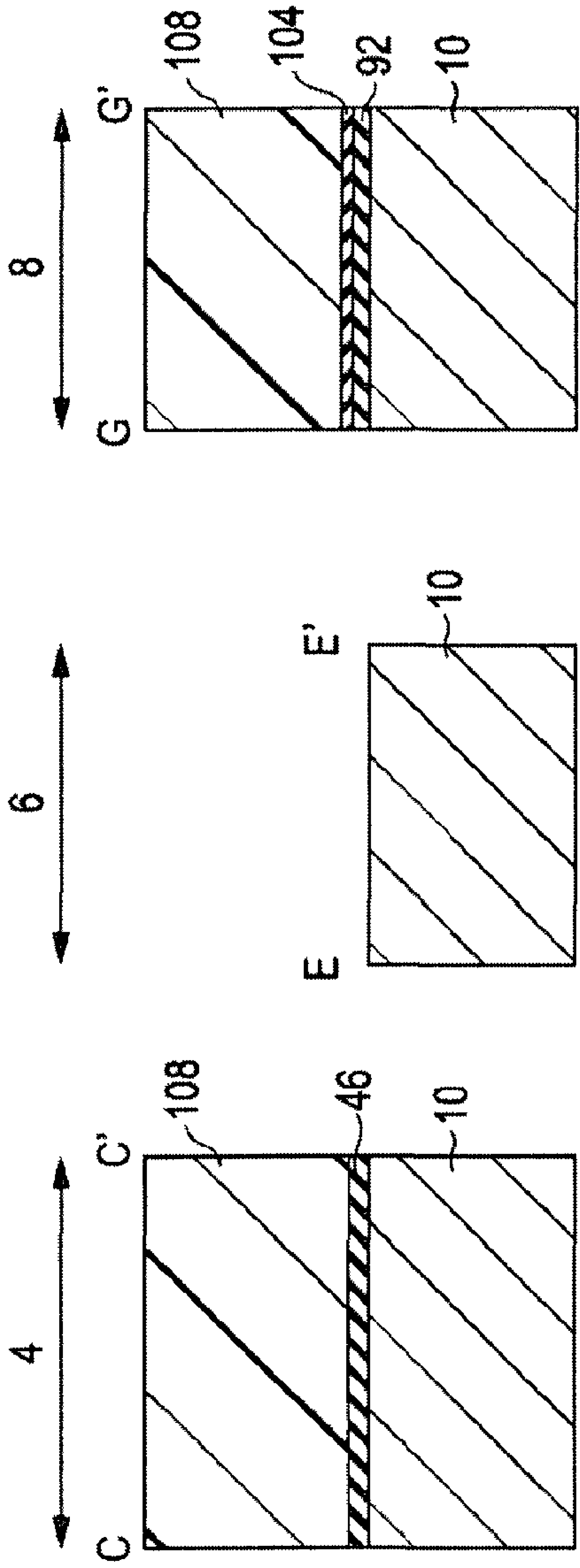


FIG. 45A

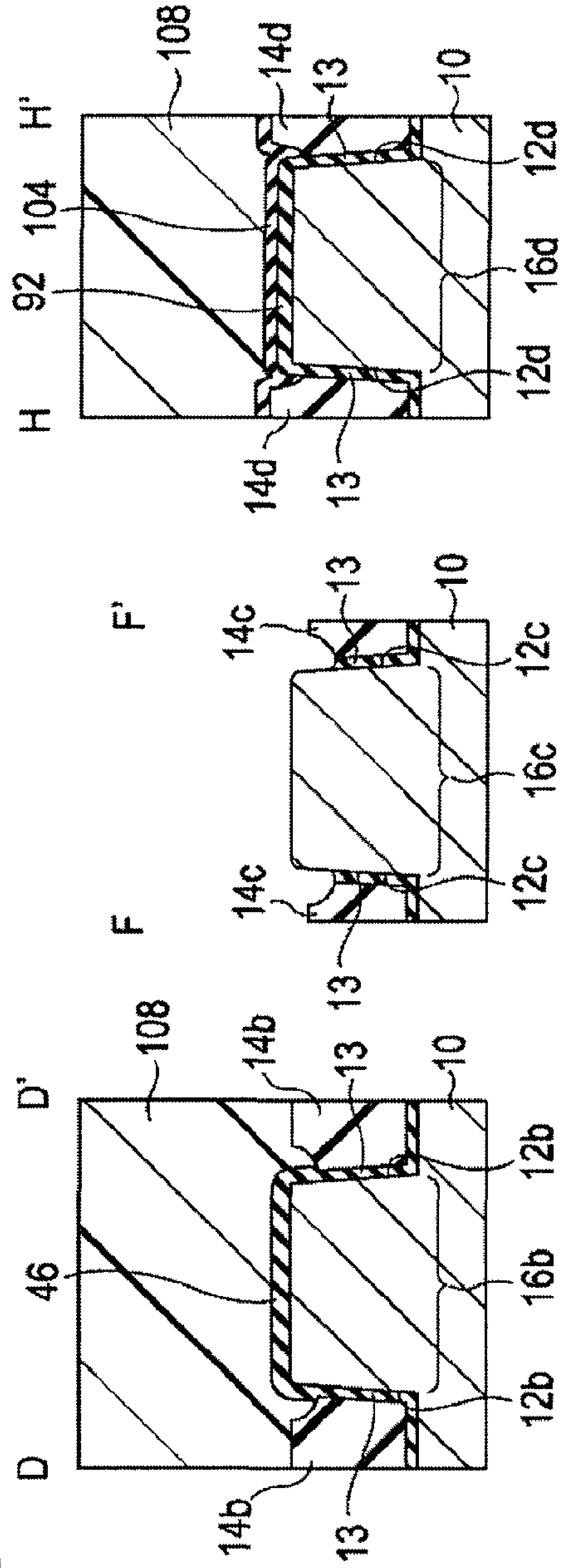


FIG. 45B

FIG. 46A

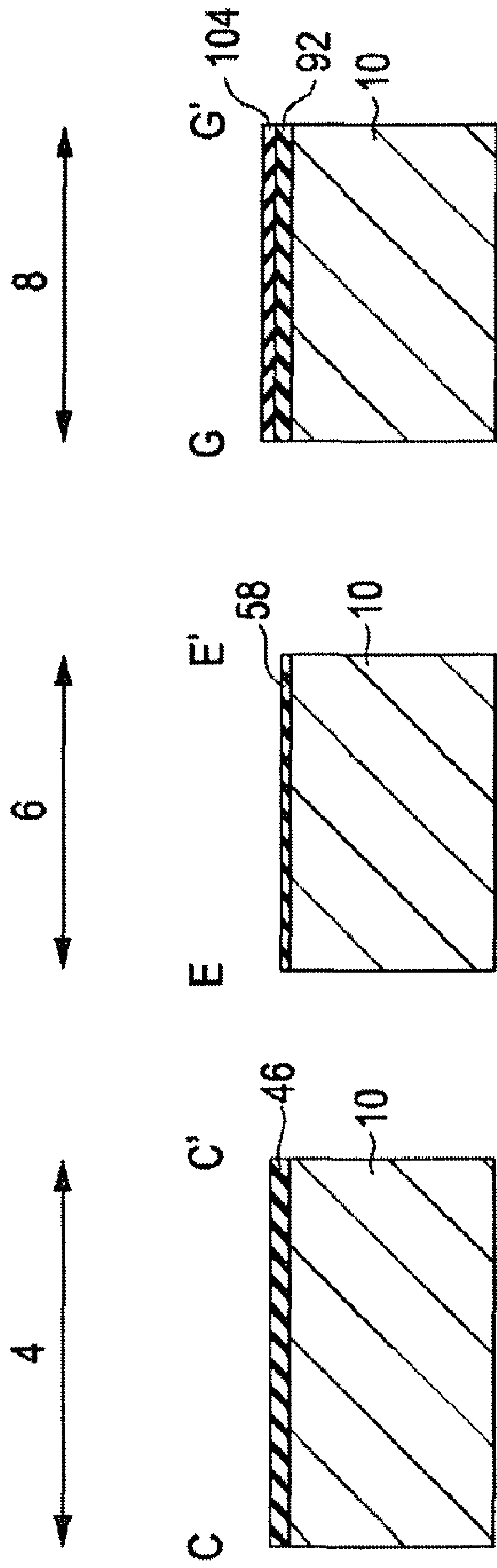
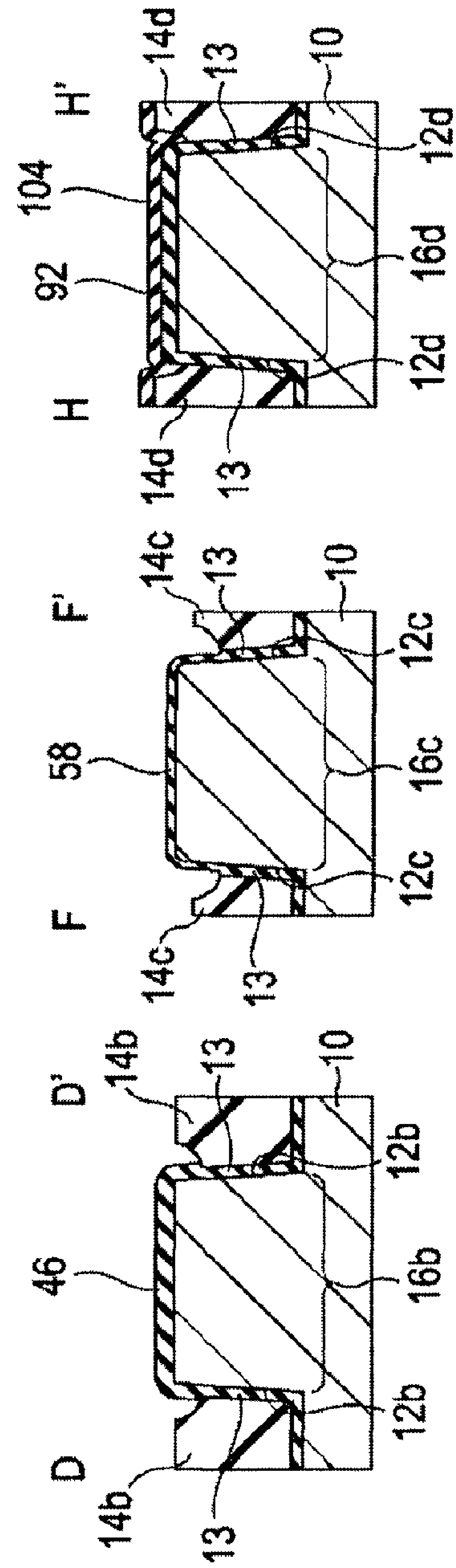


FIG. 46B



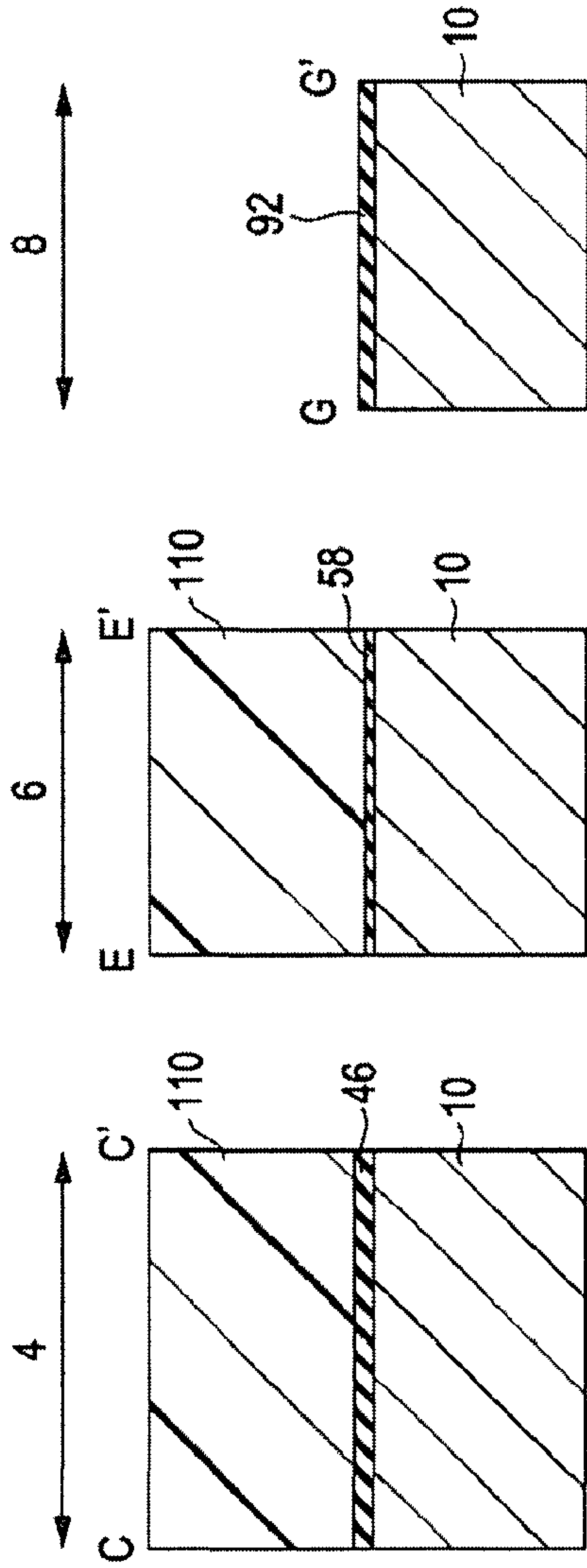


FIG. 47A

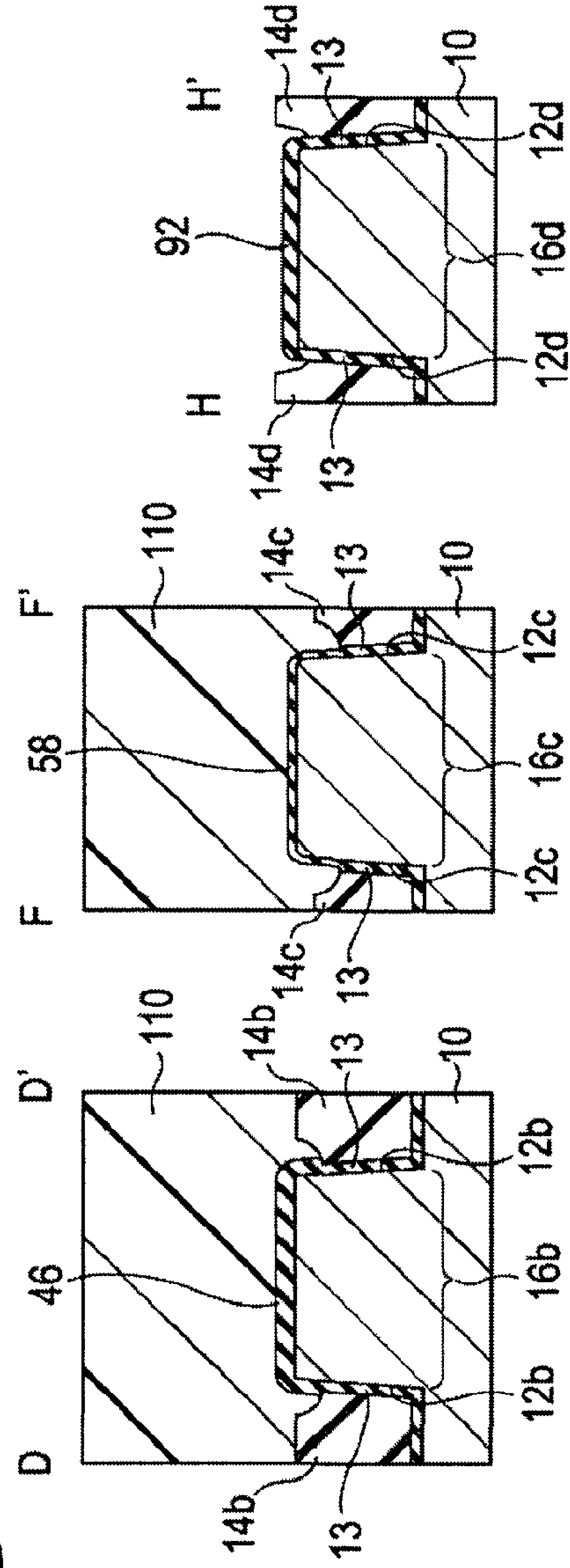


FIG. 47B

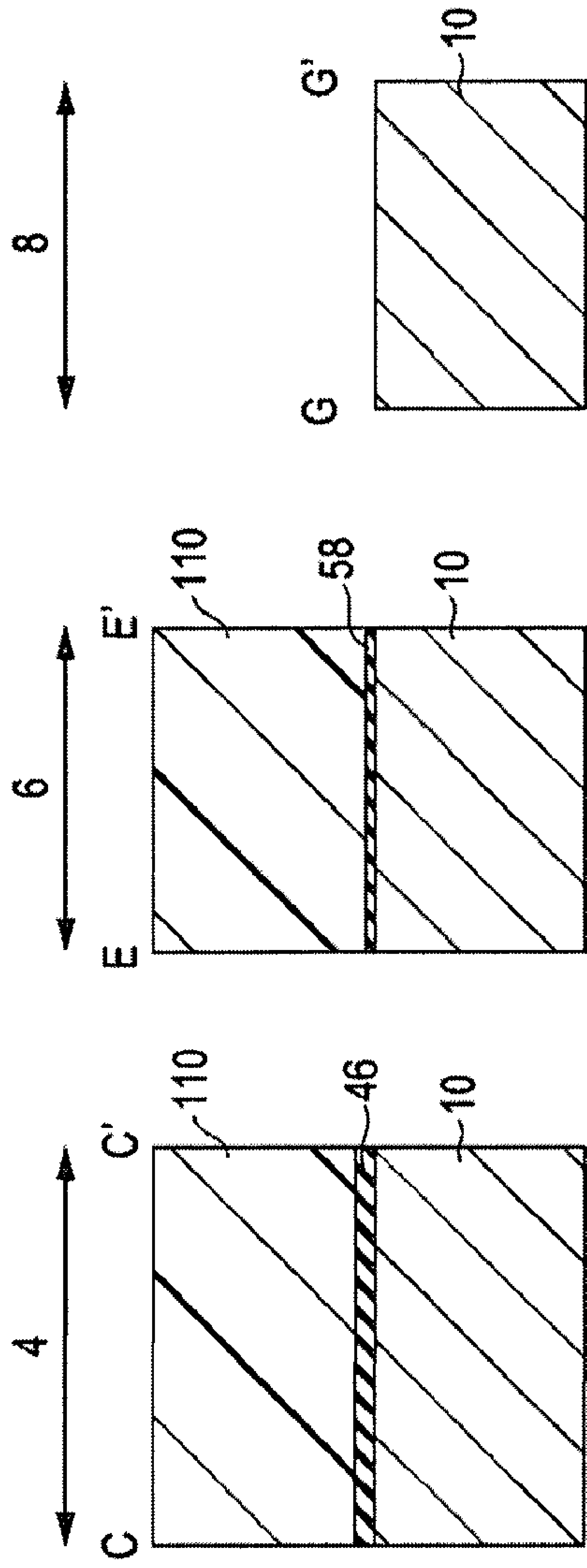


FIG. 48A
4
C
C'
110
46
10
6
E
E'
110
58
10
8
G
G'
10

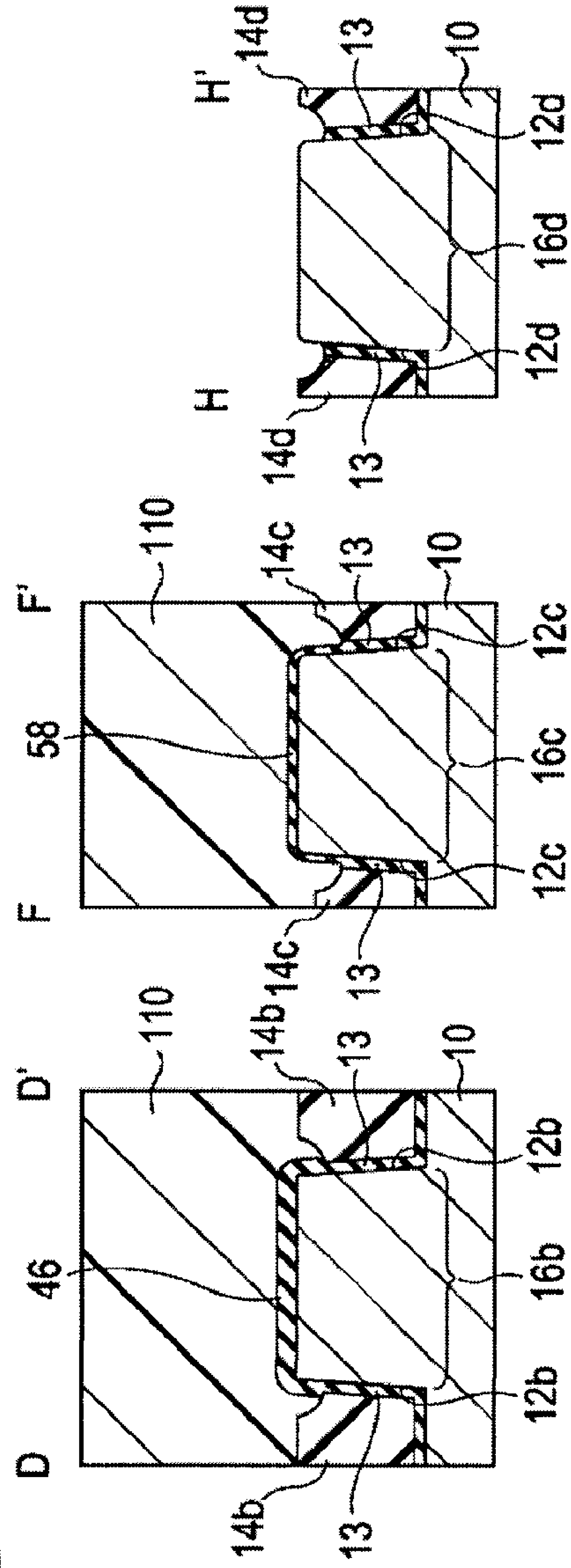


FIG. 48B
D
D'
110
46
14b
13
12b
16b
10
F
F'
110
58
14c
13
12c
16c
10
H
H'
14d
13
12d
16d
10

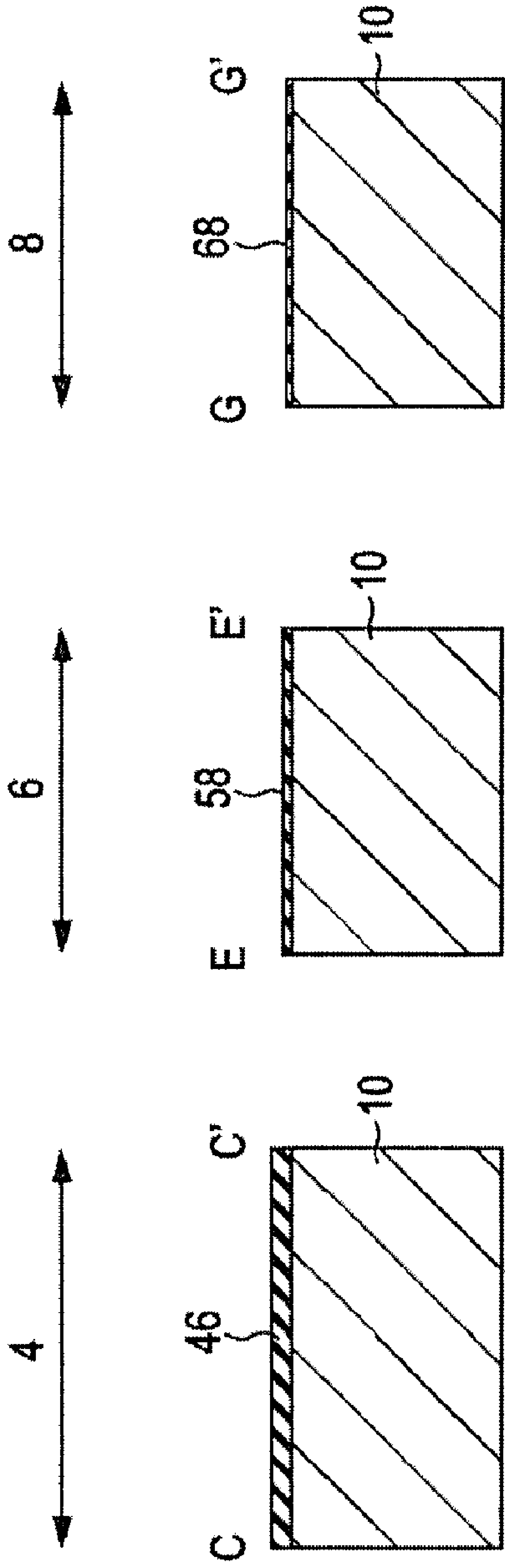


FIG. 49A

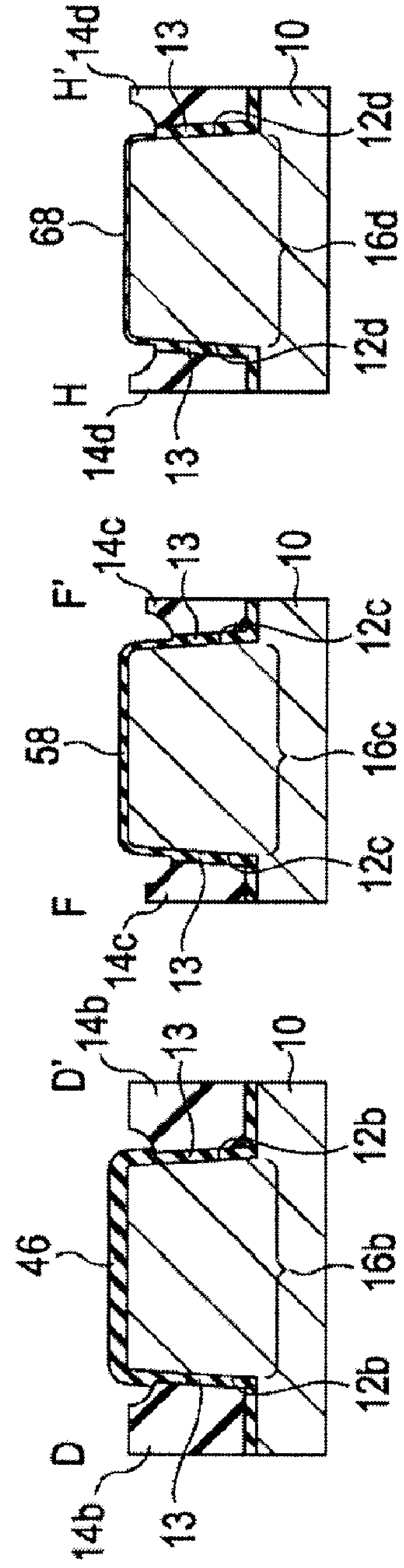


FIG. 49B

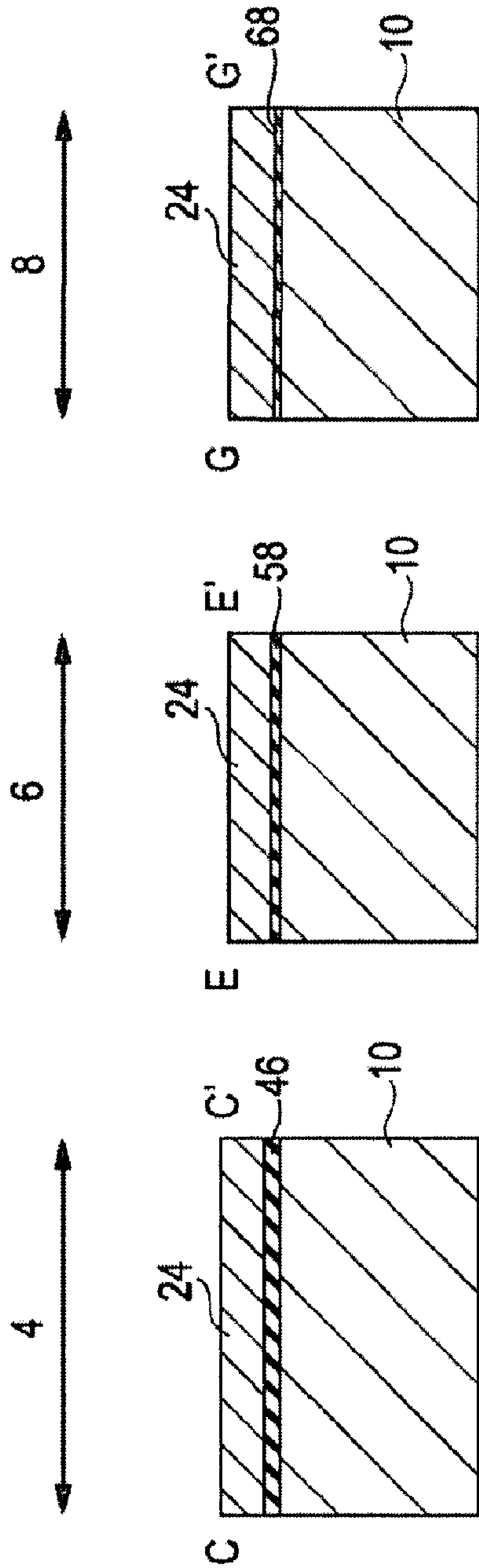


FIG. 50A

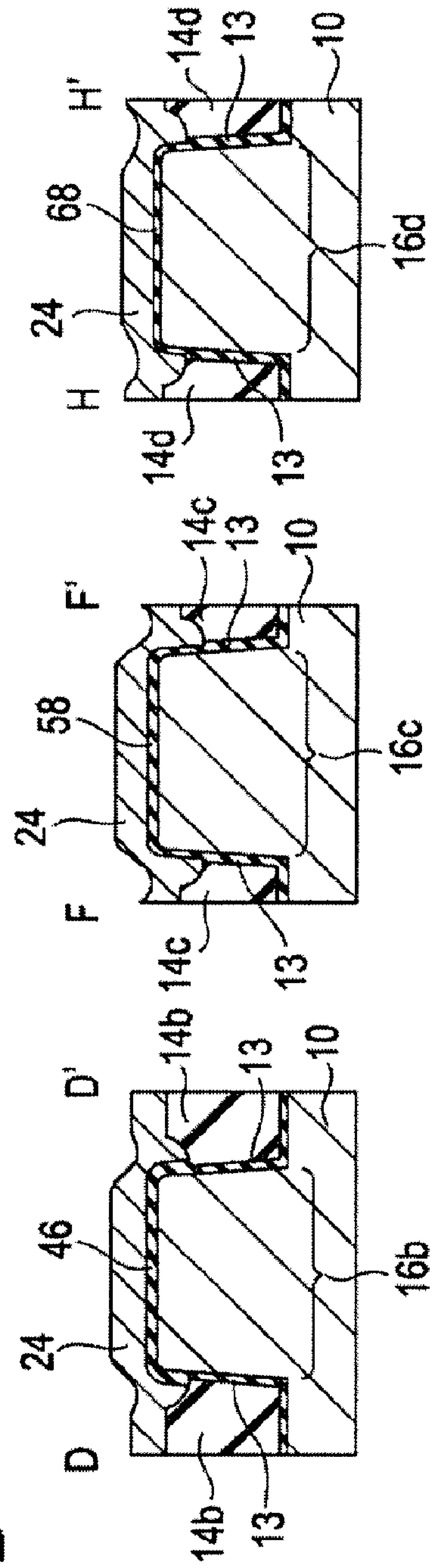


FIG. 50B

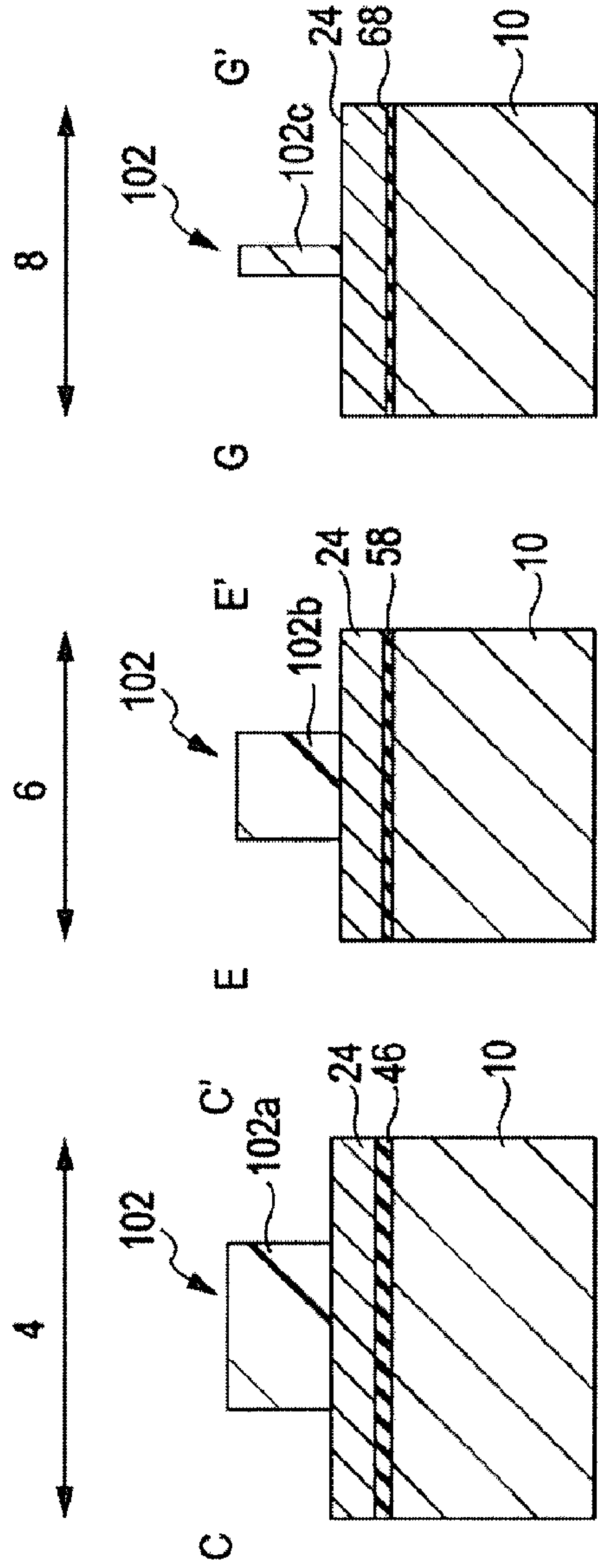


FIG. 51A

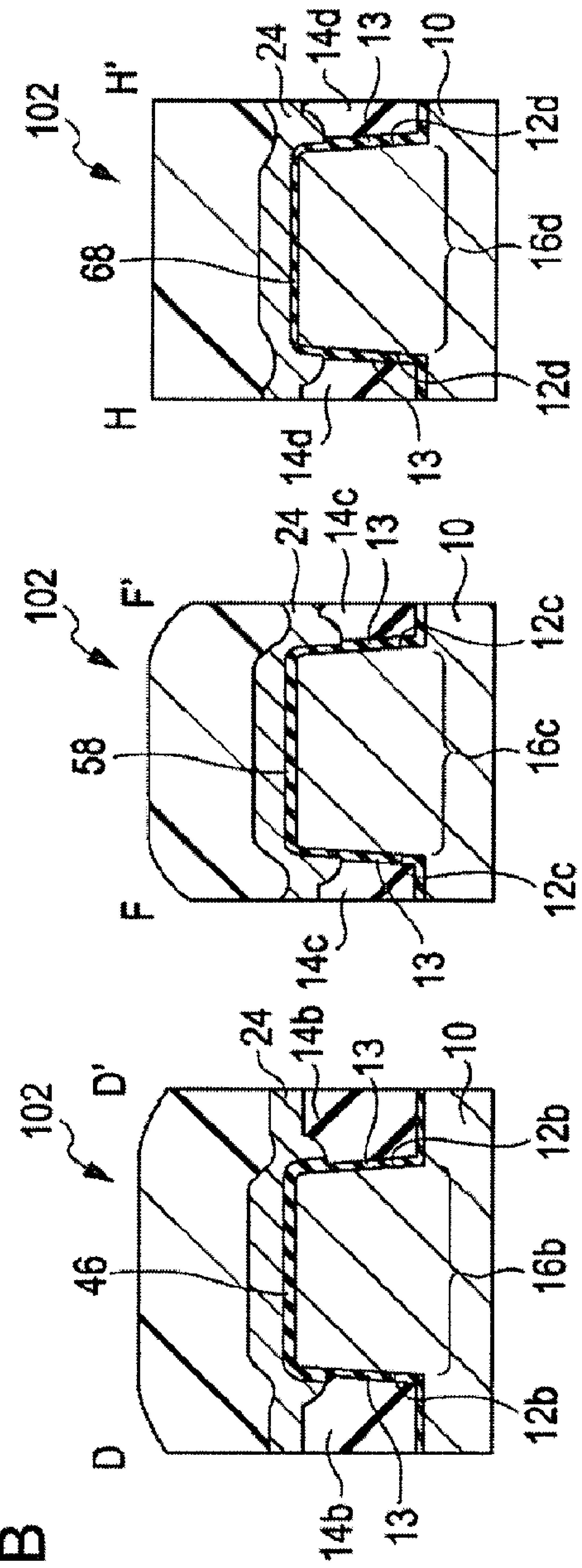


FIG. 51B

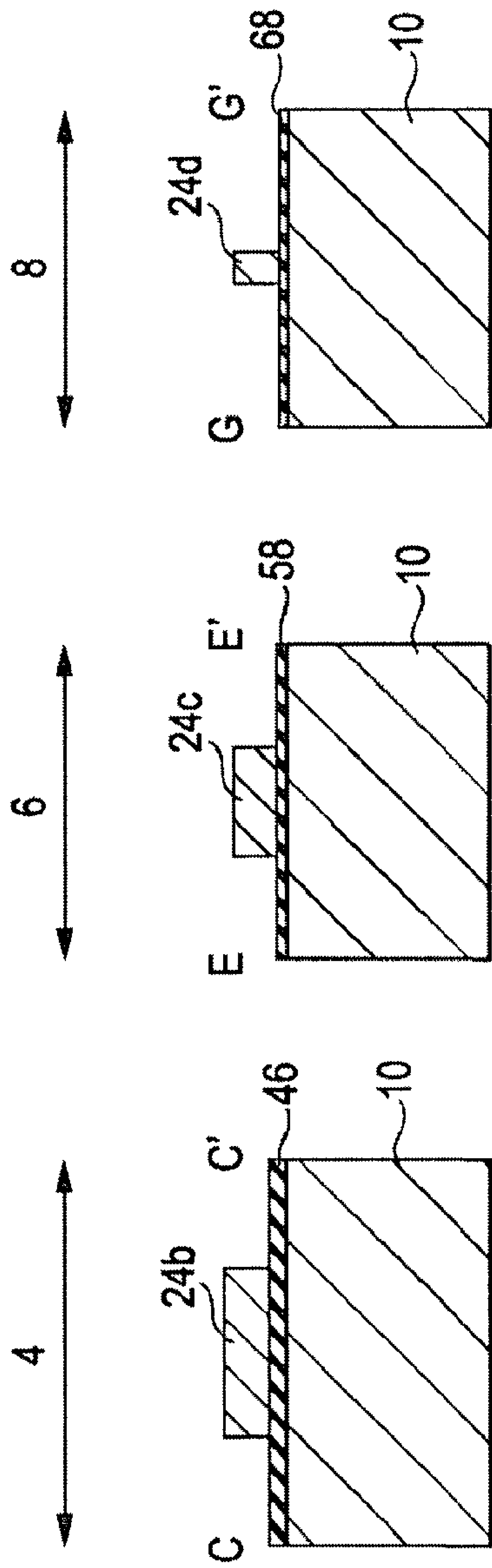


FIG. 52A

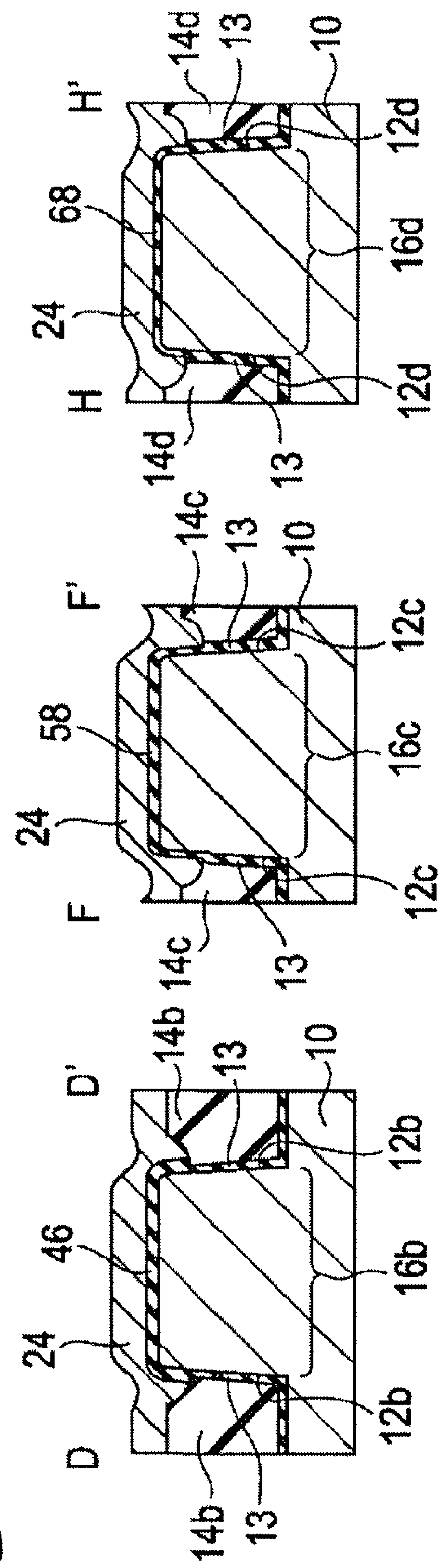


FIG. 52B

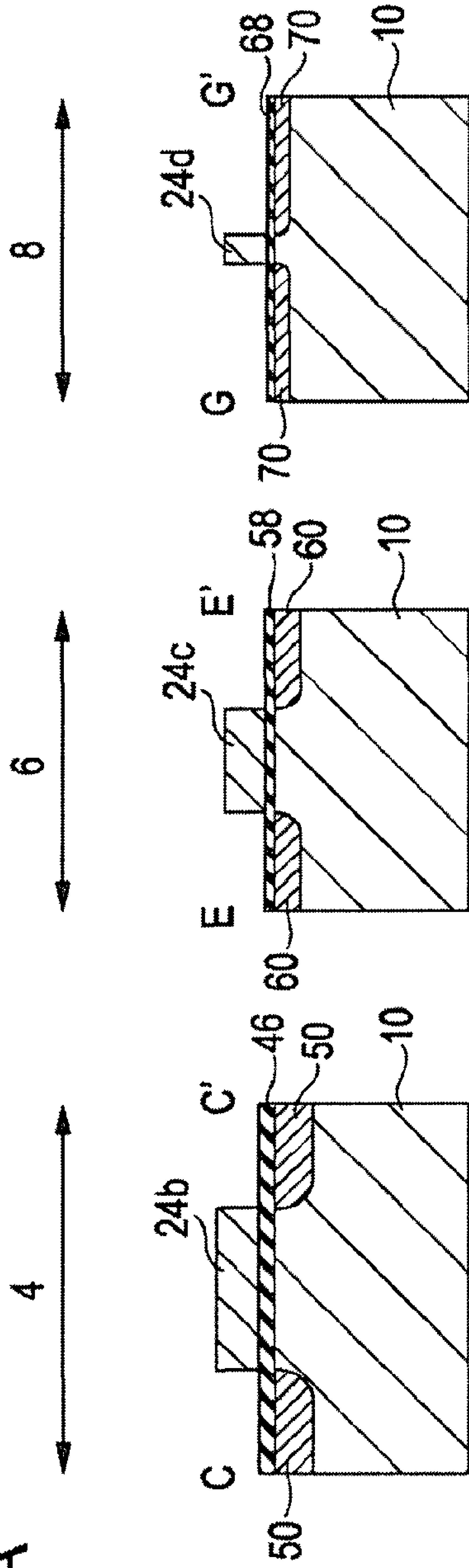


FIG. 53A

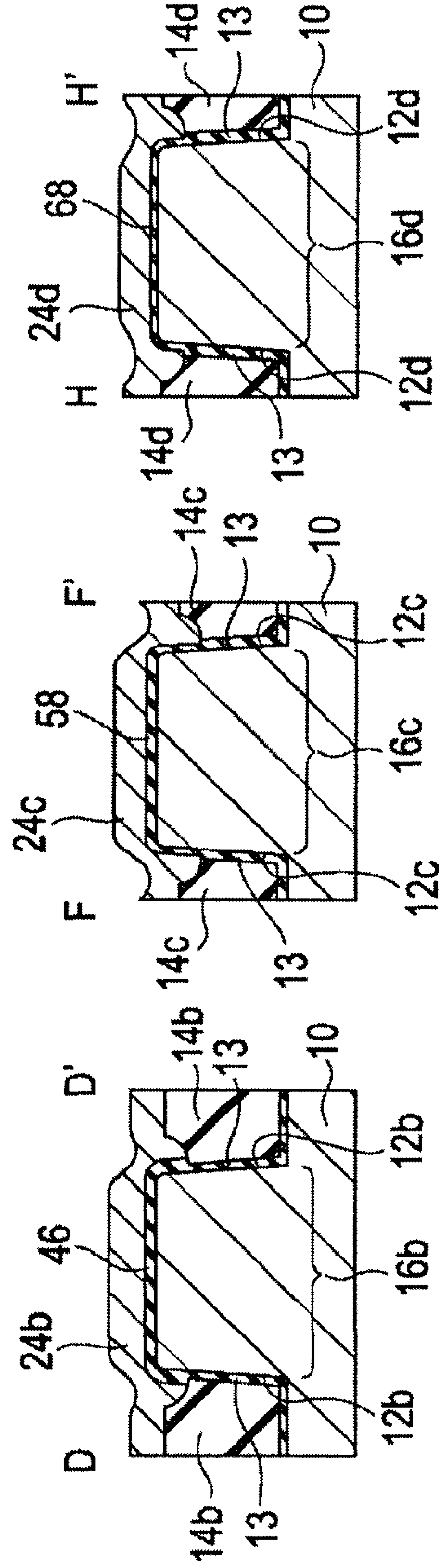


FIG. 53B

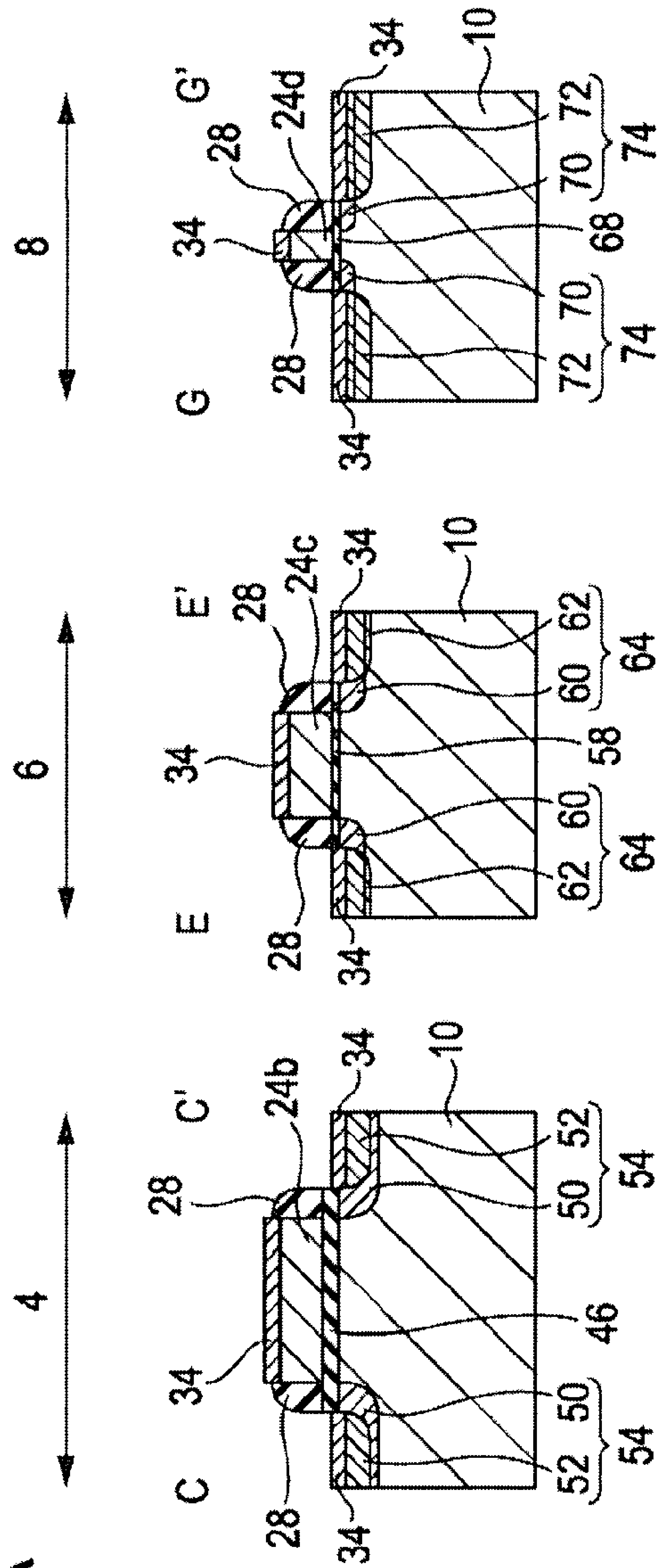


FIG. 54A

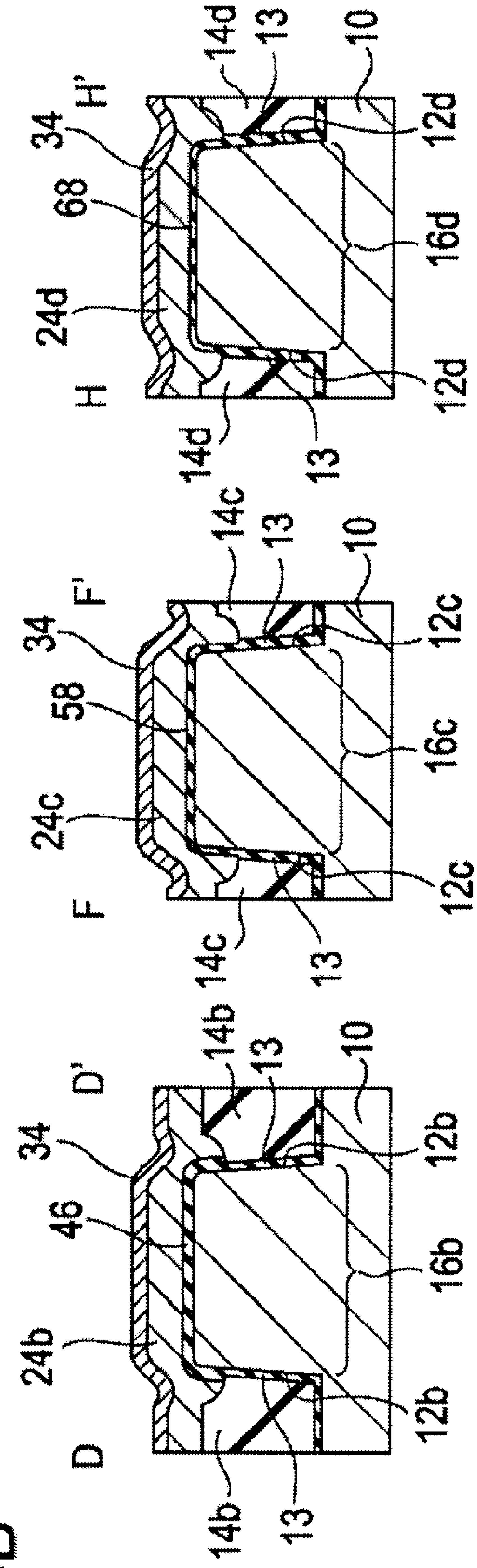


FIG. 54B

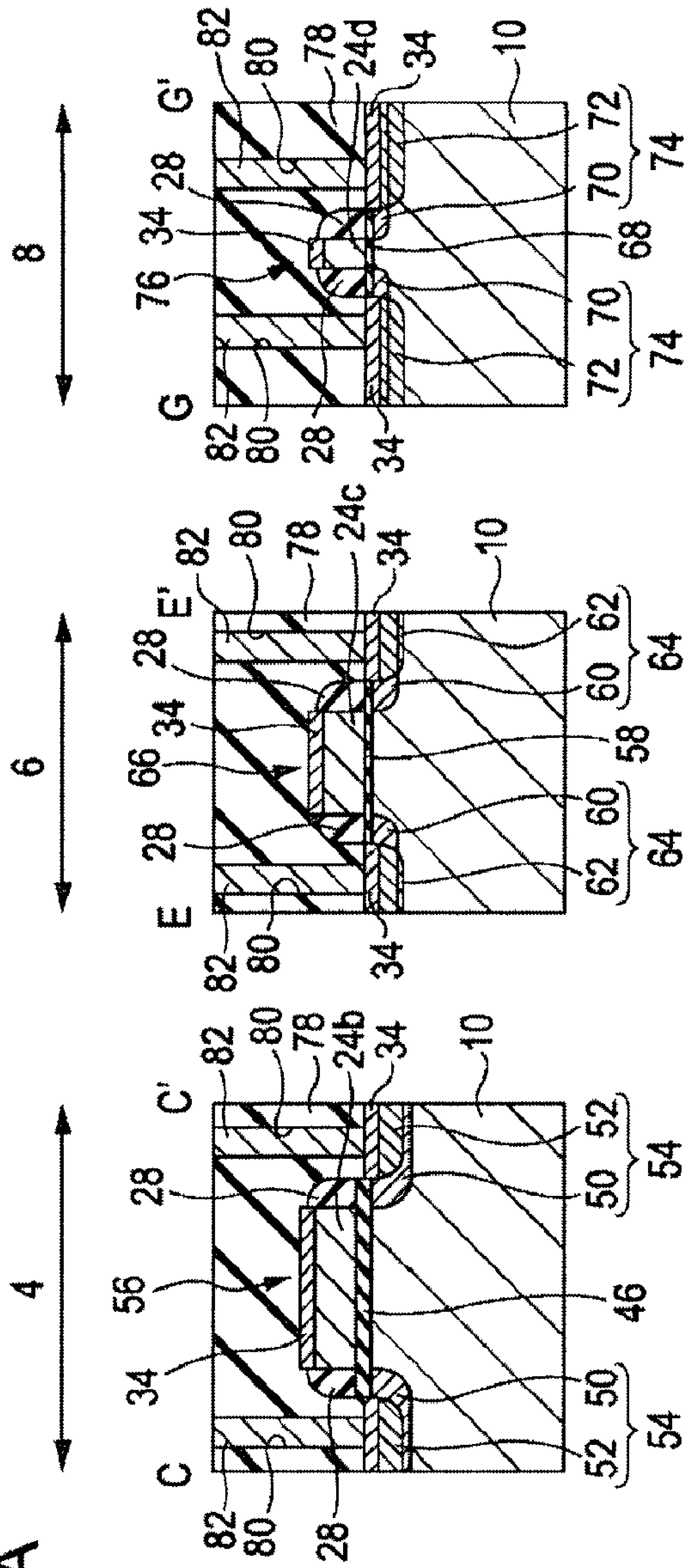


FIG. 55A

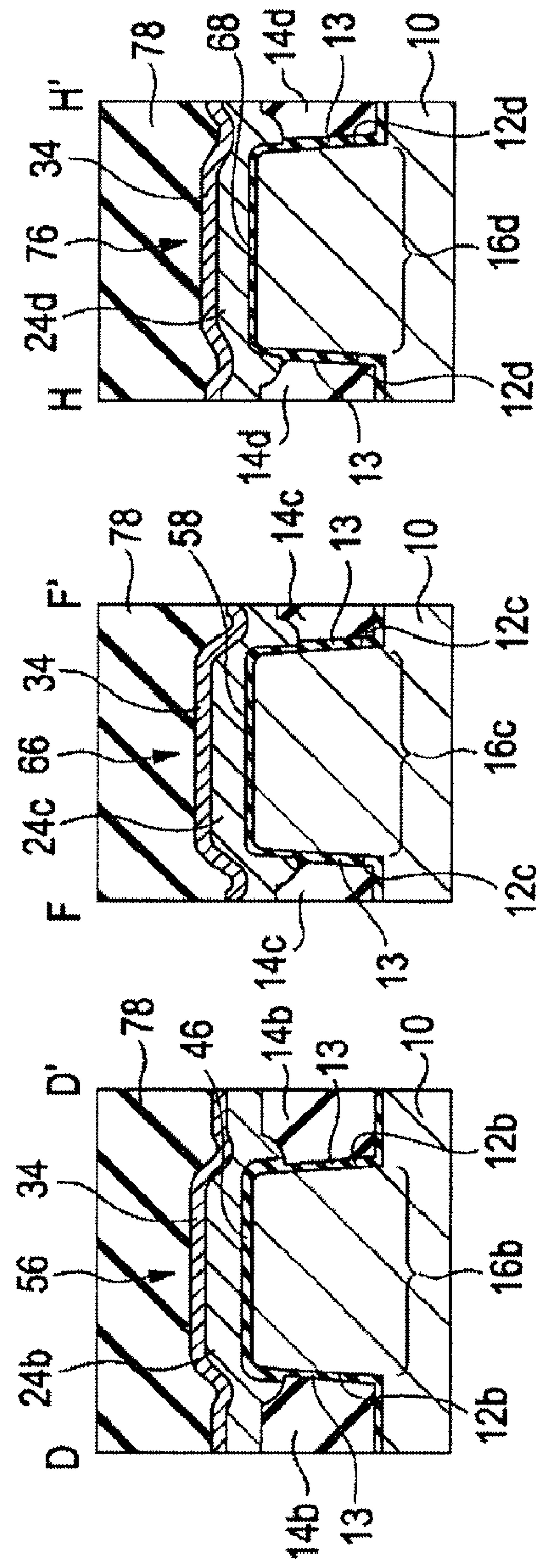


FIG. 55B

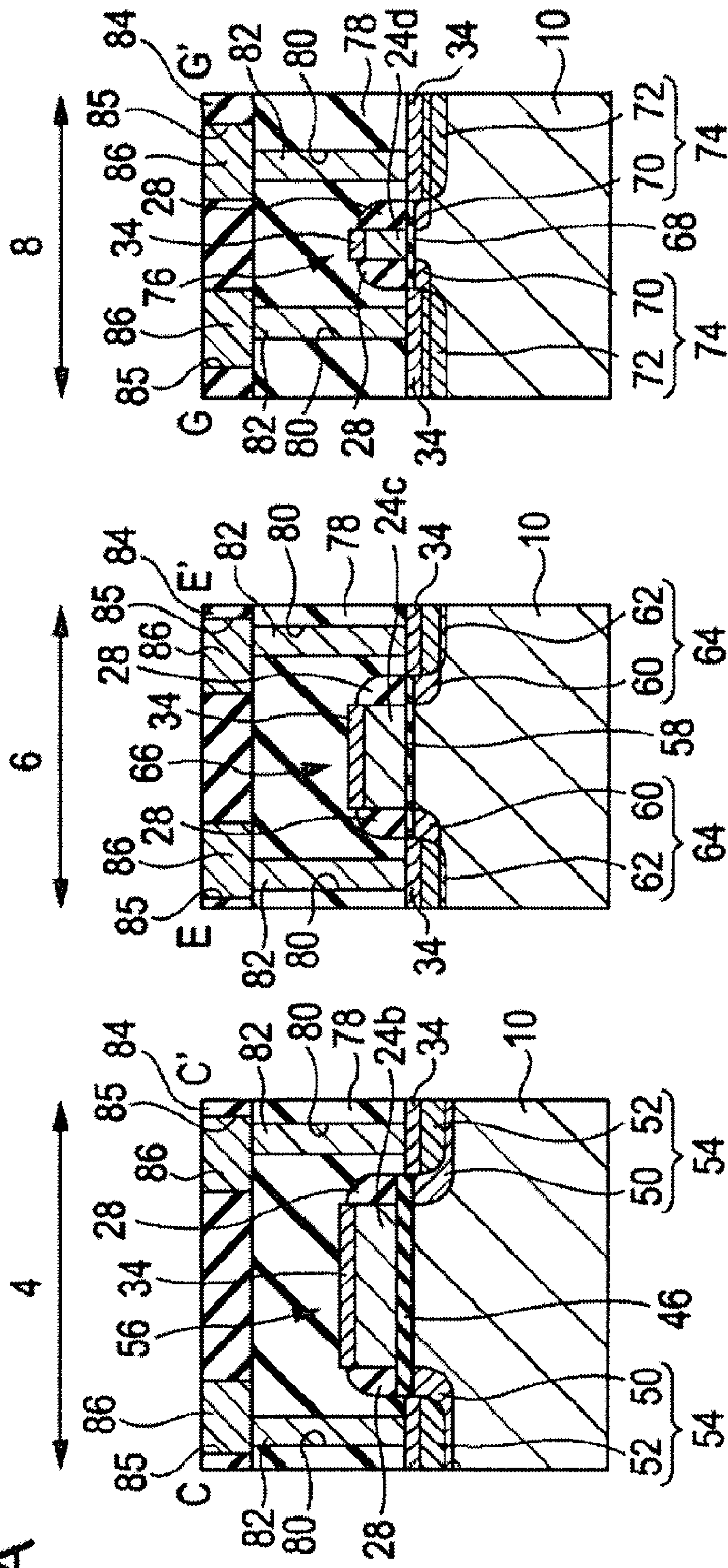


FIG. 56A

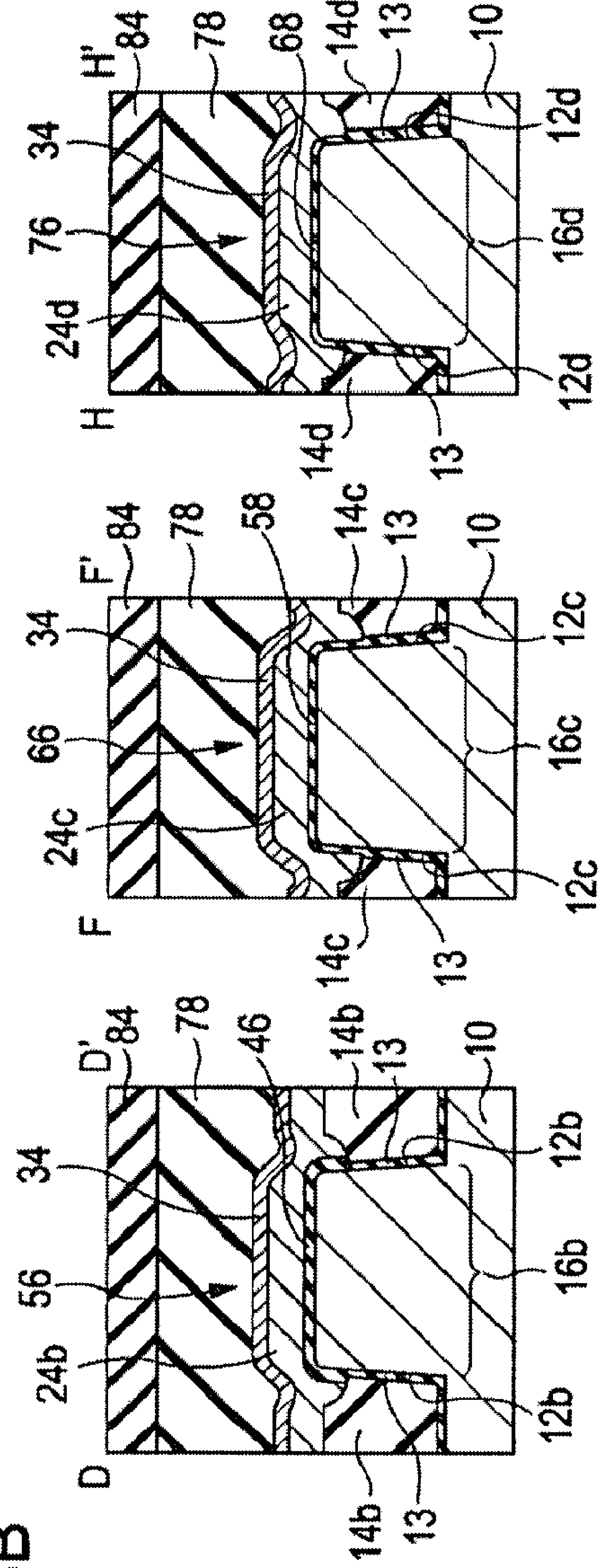


FIG. 56B

FIG.57

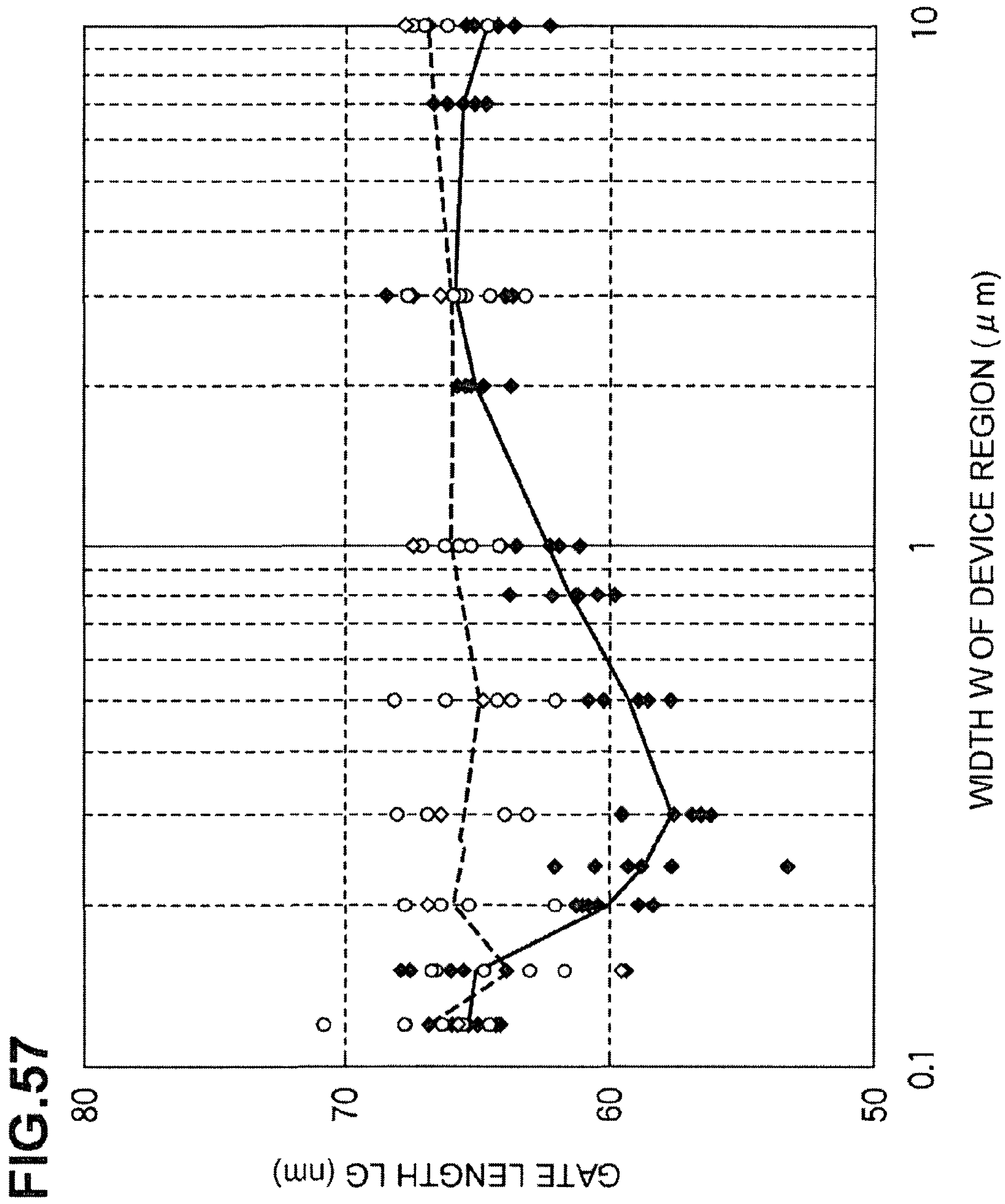


FIG.58

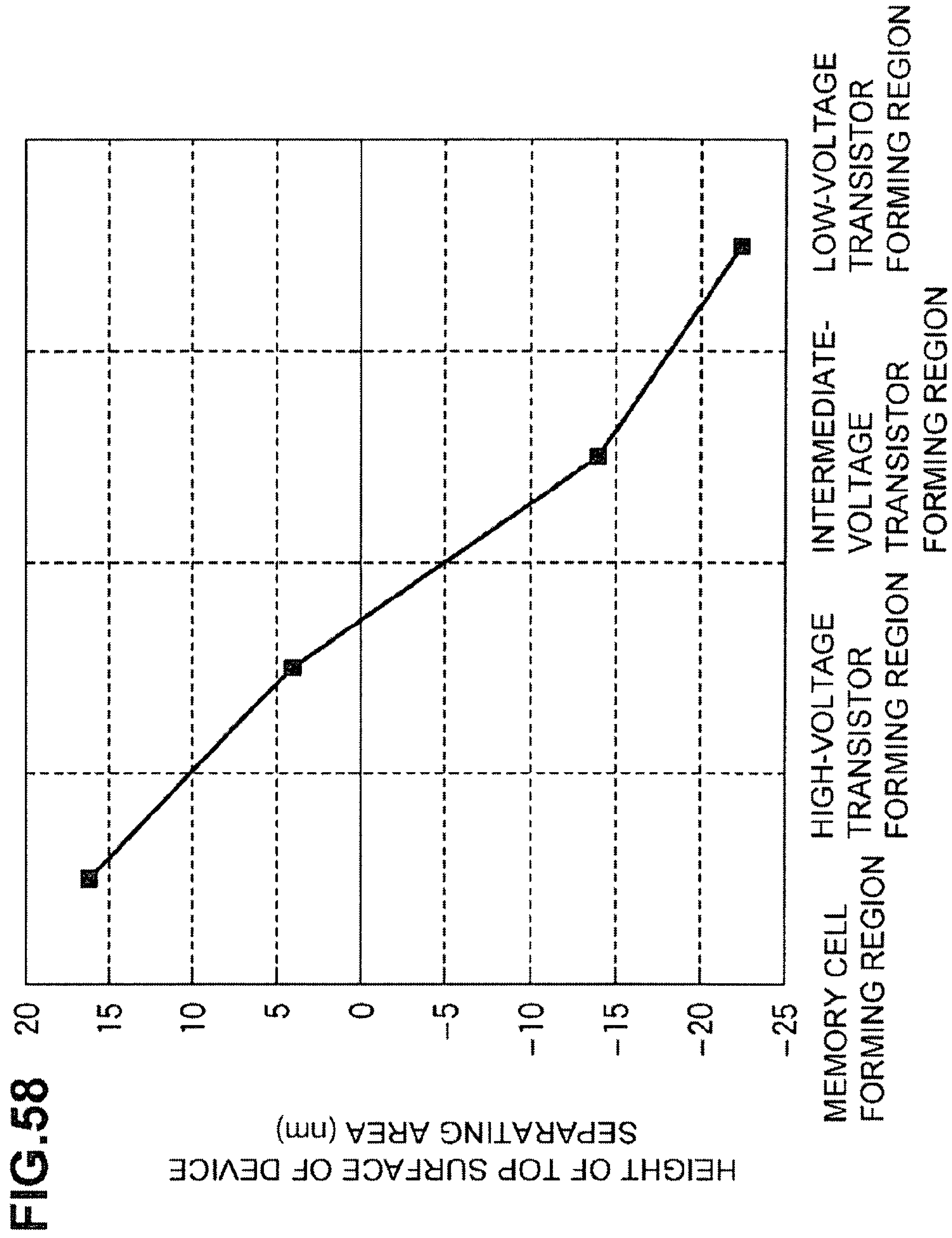


FIG. 59A

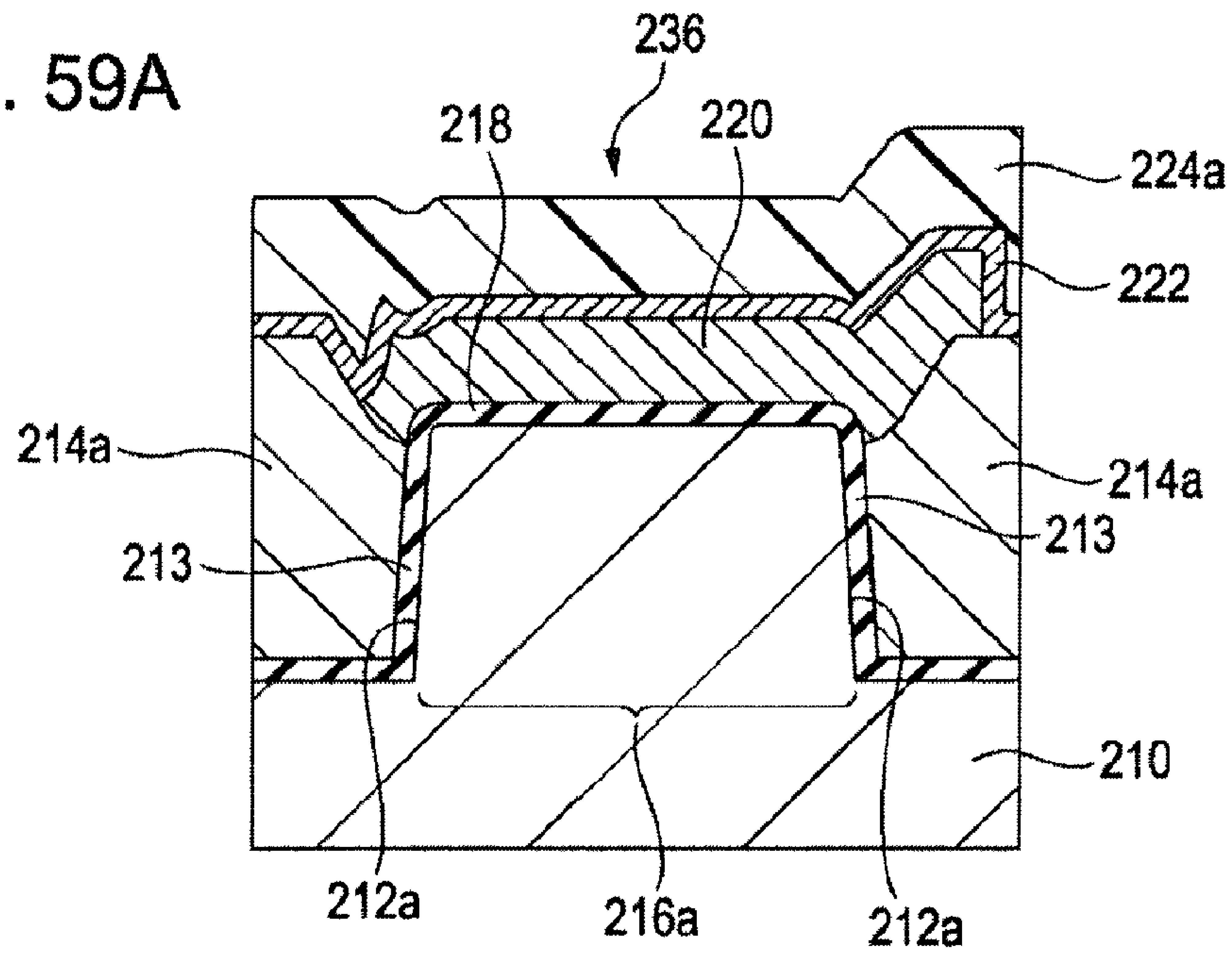


FIG. 59B

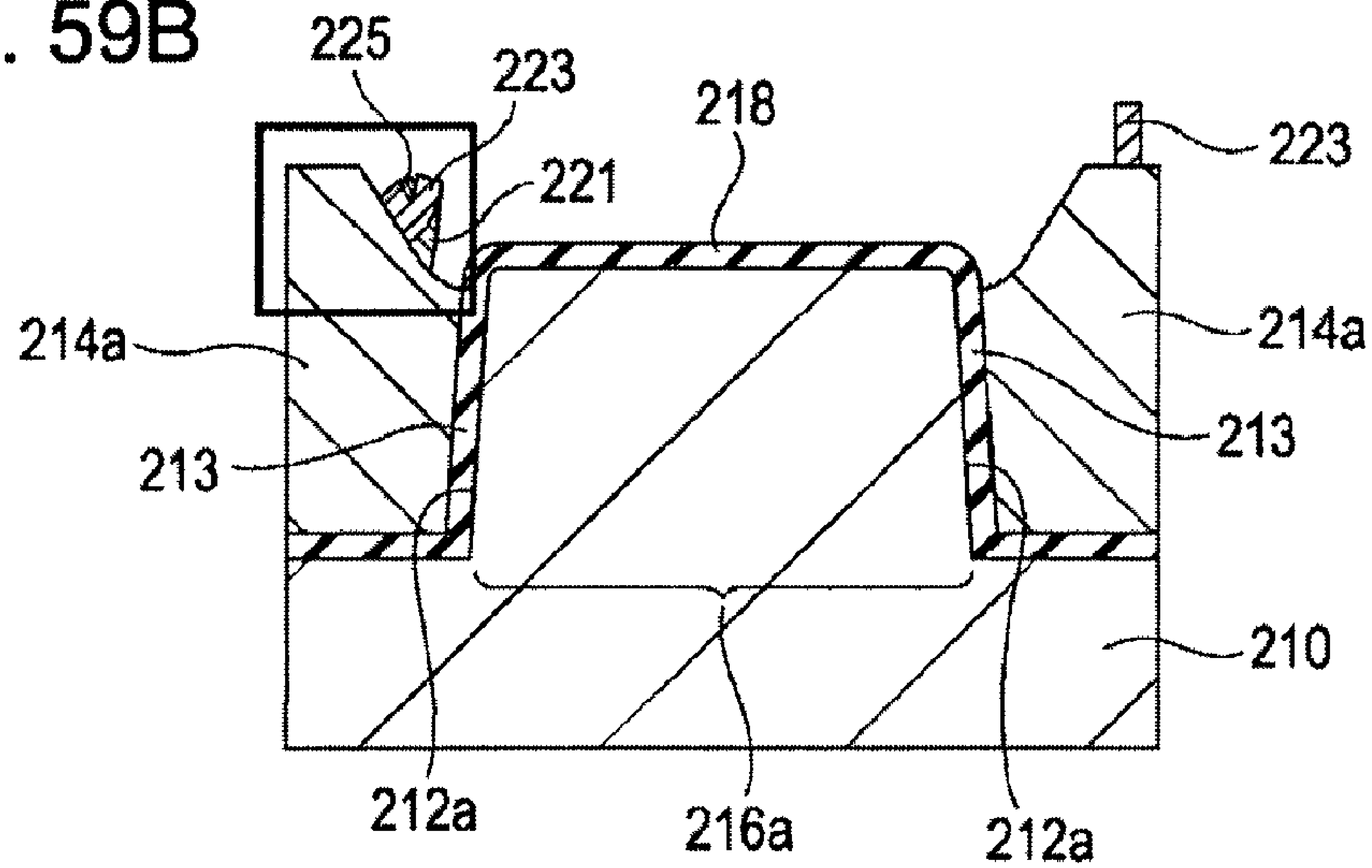
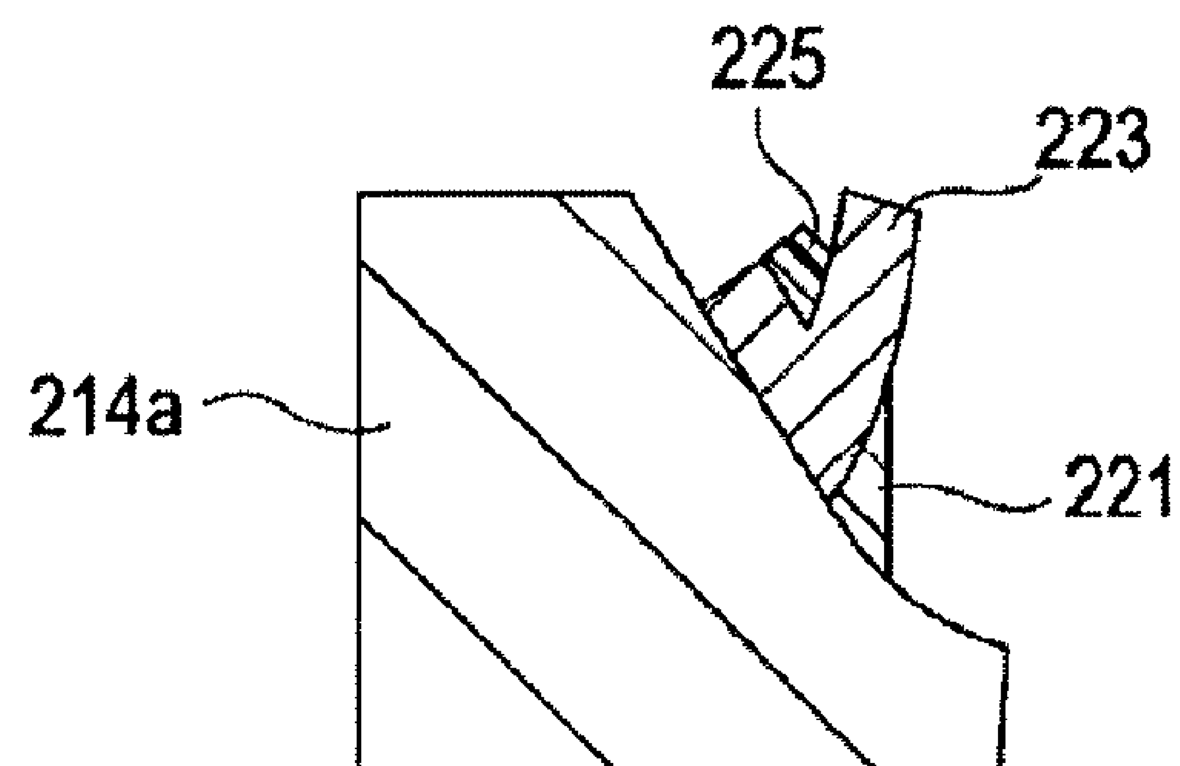


FIG. 59C



SEMICONDUCTOR DEVICE

INCORPORATED-BY-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. Ser. No. 12/187,851 filed Aug. 7, 2008, which is based on and claims priority from Japanese Patent Application No. 2007-209410 filed on Aug. 10, 2007, the entire contents of which are incorporated by reference.

BACKGROUND

This technique relates to a semiconductor device and a method of manufacturing the same and, more particularly, to a semiconductor device having a plurality of types of transistors having different thicknesses of a gate insulating film, and a method of manufacturing the same.

Recently, a semiconductor device is proposed that a memory cell, a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor are mixedly provided on the same substrate.

In the proposed semiconductor device, the memory cell having a floating gate and a control gate with a stack gate structure is formed within a memory cell forming-region. Within a high-voltage transistor forming-region, the high-voltage transistor with a relatively high thickness of a gate insulating film is formed. Within an intermediate-voltage transistor forming-region, the intermediate-voltage transistor having a gate insulating film with a thickness lower than that of the gate insulating film of the high-voltage transistor is formed. Within a low-voltage transistor forming-region, the low-voltage transistor having a gate insulating film lower than that of the gate insulating film of the intermediate-voltage transistor is formed.

However, in the case of simply forming the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor, the height of a top surface of a device separating area in the high-voltage transistor forming region is lower than the height of a top surface of a device separating area in the memory cell forming region, the height of a top surface of a device separating area in the intermediate-voltage transistor forming region is lower than the height of the top surface of the device separating area in the high-voltage transistor forming region, and the height of a top surface of the device separating area in the low-voltage transistor forming region is lower than the height of the top surface of the device separating area of the intermediate-voltage transistor forming region. Therefore, the height of the top surface of the device separating area in the low-voltage transistor forming region is extremely lower than the height of the top surface of the device area in the low-voltage transistor forming region. When the height of the top surface of the device separating area in the low-voltage transistor forming region is extremely lower than the height of the top surface of the device area in the low-voltage transistor forming region, a low-voltage transistor having a gate electrode with a desired gate length cannot be formed, and a semiconductor device having preferable electrical characteristics cannot be provided.

SUMMARY

According to an aspect of an embodiment, a semiconductor device has a substrate a first insulator formed in a first area of the substrate, and a second insulator formed in the second area of the substrate, a first transistor formed over a first device region surrounded by the first area, the first transistor comprising a first gate insulating film having a first thickness, the first gate insulating film being formed over the first device region, a first gate electrode formed over the first gate insulating film, and first source and drain regions formed in the first device region at both sides of the first gate electrode and a second transistor formed over a second device region surrounded by the second area, the second transistor comprising a second gate insulating film formed over the second device region, a second gate insulating film having a second thickness less than the first thickness of the first gate insulating film, a second gate electrode, the second gate electrode formed over the second gate insulating film, and second source and drain regions formed in the second device region at both sides of the second gate electrode, wherein a first height of a top surface of the first insulator is less than a second height of a top surface of the second insulator.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and **1**B are cross-sectional views showing a semiconductor device according to the first embodiment of the present technique;

FIG. **2** is a plan view showing a memory cell in the semiconductor device according to the first embodiment of the present technique;

FIGS. **3**A to **3**C are plan views showing a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor in the semiconductor device according to the first embodiment of the present technique;

FIG. **4** is a graph showing a relationship between the height of a top surface of a device separating area and the heights of top surfaces of active regions in the semiconductor device according to the first embodiment of the present technique;

FIGS. **5**A and **5**B are cross-sectional views showing a step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **6**A and **6**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **7**A and **7**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **8**A and **8**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **9**A and **9**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **10**A and **10**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **11**A and **11**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **12**A and **12**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **13**A and **13**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **14**A and **14**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **15**A and **15**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **16**A and **16**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **17**A and **17**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **18**A and **18**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **19**A and **19**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **20**A and **20**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **21**A and **21**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **22**A and **22**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **23**A and **23**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **24**A and **24**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **25**A and **25**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **26**A and **26**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **27**A and **27**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **28**A and **28**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **29**A and **29**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **30**A and **30**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **31**A and **31**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the first embodiment of the present technique;

FIGS. **32**A and **32**B are cross-sectional views showing a semiconductor device according to the second embodiment of the present technique;

FIGS. **33**A to **33**C are plan views showing a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor in the semiconductor device according to the second embodiment of the present technique;

FIG. **34** is a graph showing a relationship between the height of a top surface of a device separating area and the heights of top surfaces of active regions in the semiconductor device according to the second embodiment of the present technique;

FIGS. **35**A and **35**B are cross-sectional views showing a step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **36**A and **36**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **37**A and **37**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **38**A and **38**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **39**A and **39**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **40**A and **40**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **41**A and **41**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **42**A and **42**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **43**A and **43**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **44**A and **44**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **45**A and **45**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **46**A and **46**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **47**A and **47**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **48**A and **48**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **49**A and **49**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **50**A and **50**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **51**A and **51**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **52**A and **52**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **53**A and **53**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **54**A and **54**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **55**A and **55**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIGS. **56**A and **56**B are cross-sectional views showing the step of manufacturing the semiconductor device according to the second embodiment of the present technique;

FIG. **57** is a graph showing a measurement result of a gate length of the low-voltage transistor upon forming the low-voltage transistor with a gate length of 65 nm;

FIG. **58** is a graph showing the height of a top surface of a device separating area upon forming a memory cell, a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor with a general method; and

FIGS. **59**A to **59**C are cross-sectional views showing the case of setting the top surface of the device separating area to be extremely high in a step of forming the device separating area.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **57** is a graph showing a measurement result of a gate length of a low-voltage transistor upon forming a low-voltage transistor having a gate length of 65 nm. Referring to FIG. **57**, the abscissa denotes a width W of an active region, and the ordinate denotes a gate length Lg.

Further, referring to FIG. **57**, a plot shown by an O mark denotes a measurement result of the gate length of the low-voltage transistor, when the height of a top surface of a device separating area is equal to the height of a top surface of the active region or when the height of the top surface of the device separating area is slightly higher than the height of the top surface of the active region. A dotted line in FIG. **57** denotes an average of the plots shown by the O mark.

Furthermore, referring to FIG. **57**, a plot shown by a ♦ mark denotes a measurement result of the gate length of the low-voltage transistor when the height of the top surface of the device separating area is lower than the height of the top surface of the active region by 10 nm. A solid line in FIG. **57** denotes an average of the plots shown by the ♦ mark.

As will be obvious with reference to FIG. **57**, when the height of the top surface of the device separating area is lower than the height of the top surface of the active region by 10 nm, the gate length is reduced by 7 nm as the maximum length.

The gate length is reduced when the height of the top surface of the device separating area is lower than the height of the top surface of the active region because it is considered that a pattern having a photoresist film for patterning the gate electrode is extended in the longitudinal direction and the pattern having the photoresist film becomes thin.

Since the low-voltage transistor has a relatively short gate-length, the change in gate length greatly influences on electrical characteristics of the low-voltage transistor. When the gate length of the low-voltage transistor actually-formed is smaller, by 7 nm, than a gate length of 65 nm as a design value of the low-voltage transistor, it is not possible to obtain the low-voltage transistor having desired electrical characteristics. Therefore, significantly, the change in gate length with respect to the design value is suppressed in the low-voltage transistor.

Incidentally, in a memory cell, a high-voltage transistor, and an intermediate-voltage transistor with a stack gate structure, the gate length is relatively long. Accordingly, even if the gate length changes to some degree, this influences on the electrical characteristics with a relatively low level thereof and there are no problems.

FIG. **58** is a graph showing the height of the top surface of the device separating area upon forming the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with a general method.

Referring to FIG. **58**, upon forming the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with the general method, the height of the top surface of the device separating area in the high-voltage transistor forming region is lower than the height of the top surface of the device separating area in the memory cell forming region, the height of the top surface of the device separating area in the intermediate-voltage transistor forming region is lower than the height of the top surface of the device separating area in the high-voltage transistor forming region, and the height of the top surface of the device separating area in the low-voltage transistor forming region is lower than the height of the top surface of the device separating area in the intermediate-voltage transistor forming region. Therefore, the height of the top surface of the device separating area in the low-voltage transistor forming region is extremely lower than the height of the top surface of the active region in the low-voltage transistor forming region. Thus, the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor is strongly extended in the longitudinal direction and the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor becomes extremely thin. Accordingly, upon forming the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with the general method, the low-voltage transistor having the gate electrode with a desired gate length cannot be formed, and the semiconductor device having preferable electrical characteristics cannot be provided.

Upon patterning the gate electrode, in a step of forming the device separating area so as to prevent the height of the top surface of the device separating area in the low-voltage transistor forming region from being extremely low, the height of the top surface of the device separating area can be set to be exceedingly high.

FIGS. **59**A to **59**C are cross-sectional views showing the case of setting the top surface of the device separating area to be extremely height in the step of forming the device separating area. FIG. **59**A is a cross-sectional view showing a region for forming a floating gate **220** and a control gate **224***a* of the memory cell forming region, and FIG. **59**B is a cross-sectional view showing a region for removing the floating gate **220** and the control gate **224***a* from the memory cell forming region by etching. FIG. **59**C is a cross-sectional view showing an enlarged portion surrounded by a thick line in FIG. **59**B.

Referring to FIG. **59**A, a semiconductor substrate **210** in the memory cell forming region has a trench **212***a* for forming a device separating area **214***a*. The bottom surface and the side wall of the trench **212***a* include a silicon oxidation film **213**. The trench **212***a* to which the silicon oxidation film **213** is formed has the device separating area **214***a*. The device separating area **214***a* determines an active region **216***a*. The height of the top surface of the device separating area **214***a* is set to be extremely higher than the height of the top surface of the active region **216***a*. On the active region **216***a*, a floating gate **220** containing amorphous silicon is formed via a tunnel insulating film **218**. On the floating gate **220**, a control gate **224***a* containing polysilicon is formed via an ONO film **222**. As mentioned above, a memory cell **236** with a stack gate structure having the floating gate **220** and the control gate **224***a* is formed to the memory cell forming region.

However, when the height of the top surface of the device separating area **214***a* is set to be extremely high upon forming the device separating area **214***a*, a steep inclination is caused on the side of the active region **216***a* of the device separating area **214***a*. In this case, when causing a positional deviation in the patterning, in the region for removing the floating gate **220**, there is a danger that residue **221** of amorphous silicon can remain below residue **223** containing an ONO film (refer to FIGS. **59**B and **59**C). Further, there is a danger that residue **225** containing polysilicon can remain above the residue of the ONO film **222**. When causing the residue **221** or **225** containing amorphous silicon or polysilicon under or above the residue **223** containing the ONO film **222**, the memory cells **236** adjacent to each other are short-circuited, or charges

of the floating gate **220** are leaked, and normal operation is not performed. Consequently, in the step of forming the device separating area, it is not preferable to set the height of the top surface of the device separating area in advance to be extremely high.

Hereinbelow, a description will be given of a semiconductor device and a method of manufacturing the semiconductor device according to the first embodiment of the present technique with reference to FIGS. **1**A to **31**B.

First, a description will be given of a semiconductor device and a method of manufacturing the semiconductor device according to the first embodiment of the present technique with reference to FIGS. **1**A to **4**. FIGS. **1**A and **1**B are cross-sectional views showing the semiconductor device according to the first embodiment. FIG. **2** is a plan view showing a memory cell of the semiconductor device according to the first embodiment. FIGS. **3**A to **3**C are plan views showing a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor in the semiconductor device according to the first embodiment. FIG. **3**A shows the high-voltage transistor, FIG. **3**B shows the intermediate-voltage transistor, and FIG. **3**C shows the low-voltage transistor. FIG. **4** is a graph showing a relationship between the height of a top surface of a device separating area and the height of top surfaces of active regions.

The semiconductor device according to the first embodiment includes: a memory cell forming region **2** having a flash memory cell; a high-voltage transistor forming region **4** having a high-voltage transistor; an intermediate-voltage transistor forming region **6** having an intermediate-voltage transistor having a withstand voltage higher than of the high-voltage transistor; and a low-voltage transistor forming region **8** having a low-voltage transistor having a withstand voltage lower than that of the intermediate-voltage transistor.

On the semiconductor substrate **10** in the memory cell forming region **2**, a trench **12***a* for forming a device separating area **14***a* is formed. On the side wall and the bottom surface of the trench **12***a*, a silicon oxidation film **13** is formed. In the trench **12***a* to which the silicon oxidation film **13** is formed, the device separating area **14***a* for determining an active region **16***a* is embedded. The device separating area **14***a* is formed with a Shallow Trench Isolation (STI) method. The cross section of the memory cell forming region **2** shown in FIG. **1**A corresponds to a cross section of an A-A' line in FIG. **2**, the cross section of the memory cell forming region **2** shown in FIG. **1**B corresponds to a cross section of a B-B' line in FIG. **2**.

On the active region **16***a* in the memory cell forming region **2**, a tunnel insulating film (gate insulating film) **18** containing a silicon oxidation film is formed. A floating gate **20** is formed on the tunnel insulating film **18**.

On the floating gate **20**, a laminated film **22** containing a silicon nitride film is formed. Specifically, on the floating gate **20**, the laminated film **22** is formed with a first silicon-oxidation film, a silicon nitride film formed on the first silicon-oxidation film, and a second silicon-oxidation film formed on the silicon nitride film. The above-mentioned laminated film **22** with the silicon oxidation film, silicon nitride film, and silicon oxidation film is also referred to as an ONO film.

On the floating gate **20**, a control gate **24***a* is formed via the ONO film **22**.

Within the active region **16***a* on both sides of the floating gate **20** and the control gate **24***a*, extension areas **26** and pocket areas (not shown) are formed.

On the side walls of the floating gate **20** and the control gate **24***a*, side-wall insulating films **28** are formed.

Within the active region **16***a* on both sides of the floating gate **20** and the control gate **24***a* to which the side-wall insulating film **28***s* are formed, high-concentration impurity areas **30** are formed. Source and drain diffusion layer **32** includes the extension area **26**, the high-concentration impurity area **30**, and the like.

On the control gate **24** and the source and the drain region **32**, silicide films **34** are formed. The silicide film **34** on the source and the drain region **32** functions as a source and drain electrode.

As mentioned above, a memory cell **36** is formed with a stack gate structure having the floating gate **20**, the control gate **24**, and the source and the drain region **32**.

To the high-voltage transistor forming region **4**, a trench **12***b* for forming a device separating area **14***b* is formed. On the side wall and the bottom surface of the trench **12***b*, the silicon oxidation film **13** is formed. Within the trench **12***b* to which the silicon oxidation film **13** is formed, the device separating area **14***b* for forming an active region **16***b* is embedded. The cross section of the high-voltage transistor forming region **4** shown in FIG. **1**A corresponds to a C-C' cross-section in FIG. **3**A, and the cross section of the high-voltage transistor forming region **4** shown in FIG. **1**B corresponds to a D-D' cross-section shown in FIG. **3**A.

On the active region **16***b* in the high-voltage transistor forming region **4**, a gate insulating film **46** with a relatively-high thickness is formed. The thickness of the gate insulating film **46** is, e.g., 15 nm.

A gate electrode **24***b* having a relatively-long gate length is formed on the gate insulating film **46**. The gate length of the gate electrode **24***b* is, e.g., 700 nm.

Within the active region **16***b* on both sides of the gate electrode **24***b*, extension areas **50** and pocket areas (not shown) are formed.

On the side walls of the gate electrode **24***b*, the side-wall insulating films **28** are formed.

Within the active region **16***b* on both sides of the gate electrode **24***b* to which the side-wall insulating films **28** are formed, high-concentration impurity areas **52** are formed. A source and drain region **54** includes the extension area **50**, the high-concentration impurity area **52**, and the like.

On the gate electrode **24***b* and the source and the drain region **54**, the silicide films **34** are formed. The silicide film **34** on the source and the drain region **54** functions as a source and drain electrode.

As mentioned above, a high-voltage transistor **56** having the gate electrode **24***b* and the source and the drain region **54** is formed.

To the intermediate-voltage transistor forming region **6**, a trench **12***c* for forming a device separating area **14***c* is formed. On the side wall and the bottom surface of the trench **12***c*, the silicon oxidation films **13** are formed. Within the trench **12***c* to which the silicon oxidation film **13** is formed, the device separating area **14***c* for determining a active region **16***c* is embedded. A cross section of the intermediate-voltage transistor forming region **6** shown in FIG. **1**A corresponds to an E-E' cross-section shown in FIG. **3**B, and a cross section of the intermediate-voltage transistor forming region **6** shown in FIG. **1**B corresponds to an F-F' cross-section shown in FIG. **3**B.

On the active region **16***c* in the intermediate-voltage transistor forming region **6**, a gate insulating film **58** is formed with a thickness smaller than that of the gate insulating film **46** of the high-voltage transistor **56**. The thickness of the gate insulating film **58** is, e.g., 7 nm.

On the gate insulating film **58**, a gate electrode **24***c* is formed with a gate length shorter than that of the gate elec-

trode **24**_b_ of the high-voltage transistor **56**. The gate length of the gate electrode **24**_c_ is 350 nm.

Within the active region **16**_c_ on both sides of the gate electrode **24**_c_, extension areas **60** and pocket areas (not shown) are formed.

On the side wall of the gate electrode **24**_c_, the side-wall insulating film **28** is formed.

Within the active region **16**_c_ on both sides of the gate electrode **24**_c_ to which the side-wall insulating film **28** is formed, a high-concentration impurity area **62** is formed. A source and drain region **64** includes the extension area **60**, the high-concentration impurity area **62**, and the like.

On the gate electrode **24**_c_ and the source and the drain region **64**, the silicide films **34** are individually formed. The silicide film **34** on the source and the drain region **64** functions as a source and drain electrode.

As mentioned above, an intermediate-voltage transistor **66** is structured with the gate electrode **24**_c_ and the source and the drain region **64**.

To the low-voltage transistor forming region **8**, a trench **12**_d_ for forming a device separating area **14**_d_ is formed. On the side wall and the bottom surface of the trench **12**_d_, the silicon oxidation film **13** is formed. Within the trench **12**_d_ to which the silicon oxidation film **13** is formed, the device separating area **14**_d_ for determining a active region **16**_d_ is embedded. A cross section of the low-voltage transistor forming region **8** shown in FIG. **1**A corresponds to a G-G' cross-section shown in FIG. **3**C, and a cross section of the low-voltage transistor forming region **8** shown in FIG. **1**B corresponds to an H-H' cross-section shown in FIG. **3**C.

On the active region **16**_d_ in the low-voltage transistor forming region **8**, a gate insulating film **68** is formed with a thickness smaller than that of the gate insulating film **58** of the intermediate-voltage transistor **66**. The thickness of the gate insulating film **68** is, e.g., 1.5 nm.

On the gate insulating film **68**, a gate electrode **24**_d_ is formed with a gate length shorter than that of the gate electrode **24**_c_ of the intermediate-voltage transistor **66**. The gate length of the gate electrode **24**_d_ is 60 nm.

Within the active region **16**_d_ on both sides of the gate electrode **24**_d_, extension areas **70** and pocket areas (not shown) are formed.

On the side wall of the gate electrode **24**_d_, the side-wall insulating film **28** is formed.

Within the active region **16**_d_ on both sides of the gate electrode **24**_d_ to which the side-wall insulating film **28** is formed, a high-concentration impurity area **72** is formed. A source and drain region **74** includes the extension area **70**, the high-concentration impurity area **72**, and the like.

On the gate electrode **24**_d_ and the source and the drain region **74**, the silicide films **34** are individually formed. The silicide film **34** on the source and the drain region **74** functions as a source and drain electrode.

As mentioned above, a low-voltage transistor **76** includes the gate electrode **24**_d_ and the source and the drain region **74**.

FIG. **4** is a graph showing the height of the top surface of the device separating area with respect to the top surface of the active region.

Plots shown by ● marks show a case of the semiconductor device according to the first embodiment. Plots shown by ■ marks show a comparison, i.e., a case of forming the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with a general method.

Referring to FIG. **4**, according to the first embodiment, the height of the top surface of the device separating area **14**_a_ in the memory cell forming region **2** is higher, by 8 nm, than the height of the top surface of the active region **16**_a_ in the memory cell forming region **2**.

Further, according to the first embodiment, the height of the top surface of the device separating area **14**_b_ in the high-voltage transistor forming region **4** is lower, by 3 nm, than the height of the top surface of the active region **16**_b_ in the high-voltage transistor forming region **4**.

Furthermore, according to the first embodiment, the height of the top surface of the device separating area **14**_c_ in the intermediate-voltage transistor forming region **6** is lower than, by 21 nm, than the height of the top surface of the active region **16**_c_ in the intermediate-voltage transistor forming region **6**.

In addition, according to the first embodiment, the height of the top surface of the device separating area **14**_d_ in the low-voltage transistor forming region **8** is approximately equal to the height of the top surface of the active region **16**_d_ in the low-voltage transistor forming region **8**. That is, according to the first embodiment, the height of the top surface of the device separating area **14**_d_ in the low-voltage transistor forming region **8** is higher than the height of the top surface of the device separating area **14**_c_ in the intermediate-voltage transistor forming region **6**.

Upon forming, with the general method, the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor, as shown in the comparison in FIG. **4**, the height of the top surface of the device separating area in the high-voltage transistor forming region is lower than the height of the top surface of the device separating area in the memory cell forming region, the height of the top surface of the device separating area in the intermediate-voltage transistor forming region is lower than the height of the top surface of the device separating area in the high-voltage transistor forming region, and the height of the top surface of the device separating area in the low-voltage transistor forming region is lower than the height of the top surface of the device separating area in the intermediate-voltage transistor forming region. Therefore, the height of the top surface of the device separating area in the low-voltage transistor forming region is extremely lower than the height of the top surface of the active region. Hence, upon forming, with the general method, the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor, the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor is strongly pulled in the longitudinal direction and the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor is extremely thin. Accordingly, upon forming, with the general method, the memory cell, the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor, a low-voltage transistor having a gate electrode with a desired gate length cannot be formed and the semiconductor device having preferable electrical characteristics cannot be also provided.

On the other hand, according to the first embodiment, the height of the top surface of the device separating area **14**_d_ in the low-voltage transistor forming region **8** is not extremely lower than the height of the top surface of the active region **16**_d_ in the low-voltage transistor forming region **8**. Thus, a pattern **102**_c_ (refer to FIGS. **26**A and **26**B) of a photoresist film for patterning the gate electrode **24**_d_ of the low-voltage transistor **76** is not strongly pulled in the longitudinal direction, and it is possible to prevent, from being extremely thin, the pattern **102**_c_ of the photoresist film for patterning the gate electrode **24**_d_ of the low-voltage transistor **76**. Therefore, according to the first embodiment, the low-voltage transistor **76** having the gate electrode **24**_d_ with a desired gate length

can be formed and the semiconductor device having preferable electrical characteristics can be also provided.

On the semiconductor substrate **10** having the memory cell **36**, the high-voltage transistor **56**, the intermediate-voltage transistor **66**, and the low-voltage transistor **76**, an inter-layer insulating film **78** is formed.

A contact hole **80** that reaches the silicide film **34** is formed to the inter-layer insulating film **78**. In the contact hole **80**, a contact plug **82** is embedded.

On the inter-layer insulating film **78** in which the contact plug **82** is embedded, an inter-layer insulating film **84** is formed.

A trench **85** for embedding a wiring **86** is formed to the inter-layer insulating film **84**.

In the trench **85** that is formed to the inter-layer insulating film **84**, the wiring **86** is embedded. The wirings **86** are electrically connected to the source and the drain electrode **34** via the contact plug **82**.

As mentioned above, according to the first embodiment, the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** is substantially equal to the height of the top surface of the active region **16***d* in the low-voltage transistor forming region **8**. That is, according to the first embodiment, since the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** is not extremely lower than the height of the top surface of the active region **16***d* in the low-voltage transistor forming region **8**, it is possible to prevent, from being strongly pulled in the longitudinal direction, the pattern **102***c* (refer to FIGS. **26**A and **26**B) of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Further, it is possible to prevent, from being excessively thin, a photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Therefore, according to the first embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can be formed and the semiconductor device having preferable electrical characteristics can be also provided.

As mentioned above, the semiconductor device according to the first embodiment can be structured.

Next, a description will be given of a method of manufacturing the semiconductor device according to the first embodiment with reference to FIGS. **5**A to **31**B. FIGS. **5**A to **31**B are cross-sectional views of steps of manufacturing the semiconductor device according to the first embodiment.

First, with a thermal oxidation method, a silicon oxidation film **88** with a thickness of 10 nm is formed on the semiconductor substrate **10**. As the semiconductor substrate **10**, e.g., a silicon substrate is used.

Subsequently, with a CVD method to the whole substrate, a silicon nitride film **90** with a thickness of 80 nm is formed.

Subsequently, with a spin coat method to the whole substrate, a photoresist film (not shown) is coated. When the minimal width of the active regions **16***a* to **16***d* is 100 nm, the thickness of photoresist film is 200 nm.

Subsequently, with a photolithography technology, the photoresist film is patterned.

Subsequently, by using the photoresist film as a mask, the silicon nitride film **90** is subjected to anisotropic etching. In this case, the photoresist film on the silicon nitride film **90** is also almost removed with etching. Thereafter, the photoresist film remaining on the silicon nitride film **90** is removed.

Subsequently, by using the silicon nitride film **90** as the mask, the semiconductor substrate **10** is etched. Thus, the trenches **12***a* to **12***d* with a depth of 300 nm are individually formed in the memory cell forming region **2**, the high-voltage transistor forming region **4**, the intermediate-voltage transistor forming region **6**, and the low-voltage transistor forming region **8** (refer to FIGS. **5**A and **5**B). Upon etching the semiconductor substrate **10** by using the silicon nitride film **90** as the mask, the top of the silicon nitride film **90** is slightly etched and the thickness of the silicon nitride film **90** is 60 nm.

Subsequently, with a thermal oxidation method, side walls and side surfaces of the trenches **12***a* to **12***d* are oxidized. Accordingly, the silicon oxidation film **13** with a thickness of 5 nm is formed to bottom surfaces and side walls of the trenches **12***a* to **12***d*.

Subsequently, with a dense-plasma CVD method to the whole substrate, a silicon oxidation film **14** with a thickness of 400 nm is formed (refer to FIGS. **6**A and **6**B).

Subsequently, referring to FIGS. **7**A and **7**B, with a Chemical Mechanical Polishing (CMP) method, the silicon oxidation film **14** is polished until exposing the surface of the silicon nitride film **90**. In this case, even the surface of the silicon nitride film **90** is slightly polished, and the thickness of the silicon nitride film **90** is therefore 30 nm. Since the silicon nitride film **90** is formed on the silicon oxidation film with a thickness of 10 nm, formed on the semiconductor substrate **10**, the height of the top surface of the silicon nitride film **90** is 40 nm from the surface of the semiconductor substrate **10**. The height of the top surface of the device separating areas **14***a* to **14***d* having the silicon oxidation film embedded to trenches **14***a* to **14***d* is equal to the height of the top surface of the silicon nitride film **90**. Top surfaces of the device separating areas **14***a* to **14***d* are higher, by 40 nm, than the surface of the semiconductor substrate **10**.

Subsequently, with hydrofluoric acid, the device separating areas **14***a* to **14***d* are etched with a thickness of 7 nm. After etching the thickness of 7 nm of the device separating areas **14***a* to **14***d*, the top surfaces of the device separating areas **14***a* to **14***d* are higher, by 33 nm, than the surface of the semiconductor substrate **10**. Incidentally, the thickness of 7 nm of the device separating areas **14***a* to **14***d* is etched from the device separating areas **14***a* to **14***d* so as to finally set the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** to be substantially equal to the height of the top surface of the active region **16***d*.

Subsequently, with heated phosphoric acid, the silicon nitride film **90** is removed by etching (refer to FIGS. **8**A and **8**B). If etching the silicon nitride film **90** with the phosphoric acid, an etching selecting ratio of the silicon nitride film **90** with respect to the silicon oxidation film **88** can be sufficiently ensured. Thus, the silicon oxidation film **88** on the active regions **16***a* to **16***d* remains without etching. Therefore, the silicon oxidation film **88** with a thickness of 10 nm remains on the active regions **16***a* to **16***d*.

Subsequently, referring to FIGS. **9**A and **9**B, with hydrofluoric acid, the silicon oxidation film **88** on the active regions **16***a* to **16***d* is removed by etching. Upon etching the silicon oxidation film **88** with a thickness of 10 nm, the etching is performed for a time period corresponding to the etching of a silicon oxidation film with a thickness of 12 nm, as that of 1.2 multiples of the silicon oxidation film **88**. Therefore, a silicon oxidation film forming the device separating areas **14***a* to **14***d* is etched by 12 nm. Therefore, after etching the silicon oxidation film **88**, top surfaces of the device separating areas **14***a* to **14***d* are higher, by 21 nm, than the top surfaces of the active regions **16***a* to **16***d*.

Accordingly, with the STI method, the device separating areas **14***a* to **14***d* are formed.

Subsequently, referring to FIGS. **10**A and **10**B, with a thermal oxidation method to the whole substrate, a sacrificial oxidation film **92** having a silicon oxidation film with a thick-

ness of 8 to 12 nm is formed. Herein, the thickness of the sacrificial oxidation film **92** is, e.g., 10 nm.

Dopant impurities are implanted to the memory cell forming region **2** and the high-voltage transistor forming region **4**, thereby properly forming a predetermined conductive well (not shown).

Further, with the ion-implantation method, dopant impurities are implanted to the memory cell forming region **2** and the high-voltage transistor forming region **4**, thereby properly forming a threshold-voltage control layer (not shown).

Subsequently, with the spin coat method to the whole substrate, a photoresist film **94** is formed.

Subsequently, with the photolithography technology, the photoresist film **94** is patterned. Thus, the photoresist film **94** covering the low-voltage transistor forming region **8** is formed.

Subsequently, by using the photoresist film **94** as the mask, the sacrificial oxidation films **92** in the memory cell forming region **2**, the high-voltage transistor forming region **4**, and the intermediate-voltage transistor forming region **6** is removed with etching (refer to FIGS. **11**A and **11**B). As etching solution, e.g., hydrofluoric acid is used. The sacrificial oxidation film **92** with a thickness of 10 nm is etched for a time period necessary for etching the silicon oxidation film with a thickness of 12 nm as that of 1.2 multiples of the sacrificial oxidation film **92**. Therefore, after etching the sacrificial oxidation film **92**, the top surface of the device separating area **14***a* in the memory cell forming region **2**, the top surface of the device separating area **14***b* in the high-voltage transistor forming region **4**, the top surface of the device separating area **14***c* in the intermediate-voltage transistor forming region **6** are higher, by 9 nm, than the top surface of the active regions **16***a* to **16***c*. Since the device separating area **16***d* in the low-voltage transistor forming region **8** is covered with the photoresist film **94**, the etching is not performed. The top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** maintains to be higher, by 21 nm, than the top surface of the active region **16***d*. Thereafter, the photoresist film **94** is peeled.

Herein, the description is given of the example of removing by etching the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6**. However, the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6** may not be removed by etching. By etching with the photoresist film that covers the intermediate-voltage transistor forming region **6** and the low-voltage transistor forming region **8**, the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6** can not be etched.

Subsequently, referring to FIGS. **12**A and **12**B, with the thermal oxidation method, the tunnel insulating film **18** containing a silicon oxidation film with a thickness of 10 nm is formed. Thus, on the active region **16***a* in the memory cell forming region **2**, the active region **16***b* on the high-voltage transistor forming region **4**, and the active region **16***c* on the intermediate-voltage transistor forming region **6**, the tunnel insulating film **18** is formed with a thickness of 10 nm. In the low-voltage transistor forming region **8**, since there is the sacrificial oxidation film **92** on the active region **16***d*, a silicon oxidation film is grown with a thickness of 7 nm in the low-voltage transistor forming region **8** upon forming the tunnel insulating film **18**. Therefore, the silicon oxidation film **92** on the active region **16***d* in the low-voltage transistor forming region **8** has the total thickness of 17 nm.

Subsequently, referring to FIGS. **13**A and **13**B, with the CVD method, an amorphous silicon film **20** to which dopant impurities are guided is formed. As the dopant impurities, e.g., phosphorus (P) is used. The thickness of the amorphous silicon film **20** is, e.g., 70 nm. The amorphous silicon film **20** becomes a floating gate.

Subsequently, referring to FIGS. **14**A and **14**B, with the photolithography technology, the amorphous silicon film **20** is patterned. Thus, the amorphous silicon film **20** in the memory cell forming region **2** is patterned with a predetermined shape. Further, the amorphous silicon film **20** in a region except for the memory cell forming region **2** is removed by etching.

Subsequently, referring to FIGS. **15**A and **15**B, with the CVD method to the whole substrate, an ONO film (laminated film) **22** is formed by sequentially laminating a silicon oxidation film with a thickness of 6 to 10 nm, a silicon nitride film with a thickness of 4 to 8 nm, and a silicon oxidation film with a thickness of 3 to 7 nm.

Subsequently, with the ion-implantation method, dopant impurities are guided to the intermediate-voltage transistor forming region **6** and the low-voltage transistor forming region **8**, thereby properly forming a predetermined conductive well (not shown).

Further, with the ion-implantation method, dopant impurities are guided to the intermediate-voltage transistor forming region **6** and the low-voltage transistor forming region **8**, thereby properly forming a threshold-voltage control layer (not shown).

Subsequently, with the spin coat method to the whole substrate, a photoresist film **96** is formed.

Subsequently, with the photolithography technology, the photoresist film **96** is patterned. Thus, the photoresist film **96** for exposing the high-voltage transistor forming region **4** and the intermediate-voltage transistor forming region **6** is formed.

Subsequently, by using the photoresist film **96** as the mask, the ONO film **22** in the high-voltage transistor forming region **4** and the intermediate-voltage transistor forming region **6** is removed by etching (refer to FIGS. **16**A and **16**B). Upon etching a silicon oxidation film partly forming the ONO film **22**, e.g., wet etching is used. Upon etching a silicon nitride film partly forming the ONO film **22**, e.g., dry etching is used. That is, the wet etching and the dry etching are used together, thereby etching the ONO film **22**.

Herein, the description is given of the example of removing by etching the ONO film **22** in the high-voltage transistor forming region **4** and the intermediate-voltage transistor forming region **6**. However, the ONO film **22** in the intermediate-voltage transistor forming region **6** may not be etched. By the etching using, as the mask, the photoresist film that covers the memory cell forming region **2**, the intermediate-voltage transistor forming region **6**, and the low-voltage transistor forming region **8**, the ONO film **22** in the intermediate-voltage transistor forming region **6** cannot be removed by etching.

However, in order to reduce the number of steps of manufacturing the semiconductor device, at this stage, preferably, the ONO film **22** in the intermediate-voltage transistor forming region **6** may be removed by etching.

Subsequently, referring to FIGS. **17**A and **17**B, by using the photoresist film **96** as the mask, the tunnel insulating film **18** is removed by etching. Thus, the active region **16***b* of the high-voltage transistor forming region **4** is exposed. Incidentally, the active region **16***c* of the intermediate-voltage transistor forming region **6** is also exposed. As etching solution, e.g., hydrofluoric acid is used. The tunnel insulating film **18** containing a silicon oxidation film with a thickness of 10 nm is etched for a time period necessary for etching a silicon oxidation film with a thickness of 12 nm as that of 1.2 mul-

tiples of the tunnel insulating film **18**. Therefore, the device separating area **14***b* of the high-voltage transistor forming region **4** and the device separating area **14***c* of the intermediate-voltage transistor forming region **6** are etched with a thickness of 12 nm. Therefore, after etching the tunnel insulating film **18**, the top surface of the device separating area **14***b* of the high-voltage transistor forming region **4** and the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** are lower, by a thickness of 3 nm, than the top surfaces of the active regions **16***b* and **16***d*. On the other hand, the top surface of the device separating area **14***a* of the memory cell forming region **2** maintains to be higher, by a thickness of 9 nm, than the top surface of the active region **16***a*. Further, the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** maintains to be higher, by 21 nm, than the top surface of the active region **16***d*.

Subsequently, referring to FIGS. **18**A and **18**B, on the active region **16***b* of the high-voltage transistor forming region **4**, the gate insulating film **46** is formed with a thickness of 15 nm. In this case, on the active region **16***c* of the intermediate-voltage transistor forming region **6**, the gate insulating film **46** is also formed with a thickness of 15 nm. A silicon nitride film partly forming the ONO film **22** has the oxidation resistance. Therefore, in a region covered with the ONO film **22**, i.e., the memory cell forming region **22** and the low-voltage transistor forming region **8**, the silicon oxidation film cannot be grown.

Subsequently, with the spin coat method to the entire substrate, a photoresist film **98** is formed.

Subsequently, with the photolithography technology, the photoresist film **98** is patterned. Thus, the photoresist film **98** for exposing the intermediate-voltage transistor forming region **6** is formed.

Subsequently, by using the photoresist film **98** as the mask, the gate insulating film **46** on the active region **16***c* of the intermediate-voltage transistor forming region **6** is removed by etching (refer to FIGS. **19**A and **19**B). As etching solution, e.g., hydrofluoric acid is used. The gate insulating film **46** with a thickness of 15 nm is etched for a time period necessary for etching a silicon oxidation film with a thickness of 18 nm as that of 1.2 multiples of the gate insulating film **46**. Therefore, after etching the gate insulating film **46**, the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** is lower, with thickness of 21 nm, than the active region **16***c*. On the other hand, the top surface of the device separating area **14***a* of the memory cell forming region **2** maintains to be higher, with a thickness of 9 nm, than the top surface of the active region **16***a*. Further, the top surface of the device separating area **14***b* of the high-voltage transistor forming region **4** maintains to be lower, with a thickness of 3 nm, than the top surface of the active region **16***b*. Furthermore, the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** maintains to be higher, with a thickness of 21 nm, than the top surface of the active region **16***d*. Thereafter, the photoresist film **98** is peeled.

Subsequently, referring to FIGS. **20**A and **20**B, with the thermal oxidation method, on the active region **16***c* of the intermediate-voltage transistor forming region **6**, the gate insulating film **58** with a thickness of 7 nm is formed. As mentioned above, a silicon nitride film partly forming the ONO film **22** has the oxidation resistance. Therefore, in a region covered with the ONO film **22**, i.e., in the memory cell forming region **2** and the low-voltage transistor forming region **8**, the silicon oxidation film cannot be grown.

Subsequently, with the spin coat method to the whole substrate, a photoresist film **100** is formed.

Subsequently, with the photolithography technology, the photoresist film **100** is patterned. Thus, the photoresist film **100** for exposing the low-voltage transistor forming region **8** is formed (refer to FIGS. **21**A and **21**B).

Subsequently, referring to FIGS. **22**A and **22**B, by using the photoresist film **100** as the mask, the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8** is removed by etching. As etching solution, e.g., hydrofluoric acid is used. The silicon oxidation film **92** with a thickness of 17 nm is etched for a time period necessary for etching a silicon oxidation film with a thickness of 21 nm as that of 1.2 multiples of the silicon oxidation film **92**. Therefore, after etching the gate insulating film **92**, the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** is substantially equal to the height of the top surface of the active region **16***d*. On the other hand, the top surface of the device separating area **14***a* of the memory cell forming region **2** maintains to be higher, by 9 nm, than the top surface of the active region **16***a*. Further, the top surface of the device separating area **14***b* of the high-voltage transistor forming region **4** maintains to be lower, with a thickness of 3 nm, than the top surface of the active region **16***b*. Furthermore, the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** maintains to be lower, with a thickness of 21 nm, than the top surface of the active region **16***c*. Thereafter, the photoresist film **100** is peeled.

Subsequently, referring to FIGS. **23**A and **23**B, with the thermal oxidation method, the gate insulating film **68** with a thickness of 1.5 nm is formed on the active region **16***d* of the low-voltage transistor forming region **8**.

Subsequently, referring to FIGS. **24**A and **24**B, with the CVD method, a polysilicon film **24** with a thickness of 100 nm is formed.

Subsequently, with the photolithography technology, the polysilicon film **24** in the memory cell forming region **2** is patterned. Thus, the control gate **24***a* is formed on the floating gate **20** (refer to FIG. **25**A).

Subsequently, with the spin coat method to the whole substrate, a photoresist film **102** is formed.

Subsequently, with the photolithography technology, the photoresist film **102** is patterned. Thus, a pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* of the high-voltage transistor **56**, a pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* of the intermediate-voltage transistor **66**, and the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** are formed (refer to FIGS. **26**A and **26**B).

Referring to FIG. **4**, in the memory cell forming region **2**, the top surface of the device separating area **14***a* is higher than the top surface of the active region **16***a* with a thickness of 9 nm. Further, in the high-voltage transistor forming region **4**, the top surface of the device separating area **14***b* is lower than the top surface of the active region **16***b* with a thickness of 3 nm. Furthermore, in the intermediate-voltage transistor forming region **6**, the top surface of the device separating area **14***c* is lower than the top surface of the active region **16***c* with a thickness of 21 nm. In addition, in the low-voltage transistor forming region **8**, the height of the top surface of the device separating area **14***d* is substantially equal to the height of the top surface of the active region **16***d*.

In the low-voltage transistor forming region **8**, the height of the top surface of the device separating area **14***d* is substantially equal to the height of the top surface of the active region **16***d*, the pattern **102***c* of the photoresist film for patterning the

gate electrode **24***d* of the low-voltage transistor **76** is not thus strongly pulled in the longitudinal direction. Therefore, according to the first embodiment, the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** can be prevented from being excessively thin. As a consequence, according to the first embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can be formed and the semiconductor device having preferable electrical characteristics can be also provided.

Incidentally, in the intermediate-voltage transistor forming region **6**, the top surface of the device separating area **14***c* is lower than the top surface of the active region **16***c* to some degree, the pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* of the intermediate-voltage transistor **66** is pulled in the longitudinal direction. However, the gate length of the gate electrode **24***c* of the intermediate-voltage transistor **66** is relatively long, i.e., 350 nm and, even if the pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* is thin by several nanometers, this cannot influence on electrical characteristics of the intermediate-voltage transistor **66**.

Further, in the high-voltage transistor forming region **4**, the top surface of the device separating area **14***b* is also lower than the top surface of the active region **16***b* to some degree, the pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* of the high-voltage transistor **56** is pulled in the longitudinal direction. However, the gate length of the gate electrode **24***b* of the high-voltage transistor **56** is relatively long, i.e., 700 nm and, even if the pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* is thin by several nanometers, this cannot influence on electrical characteristics of the high-voltage transistor **56**.

Subsequently, by using the photoresist film **102** as the mask, the polysilicon film **24** is etched. Thus, the gate electrode **24***b* of the high-voltage transistor **56**, the gate electrode **24***c* of the intermediate-voltage transistor **66**, and the gate electrode **24***d* of the low-voltage transistor **76** are formed (refer to FIGS. **27**A and **27**B).

Dopant impurities are guided to the active region **16***a* on both sides of the control gate **24***a*, thereby forming an extension area **26** and a pocket area (not shown).

Further, dopant impurities are guided to the active region **16***b* on both sides of the gate electrode **24***b*, thereby forming a extension area (extension area) **50** and a pocket area (not shown).

Furthermore, dopant impurities are guided to the active region **16***c* on both sides of the gate electrode **24***c*, thereby forming an extension area **60** and a pocket area (not shown).

In addition, dopant impurities are guided to the active region **16***d* on both sides of the gate electrode **24***d*, thereby forming an extension area **70** and a pocket area (not shown) (refer to FIGS. **28**A and **28**B).

Subsequently, side-wall insulating films (side-wall spacers) are individually formed to side wall portions of the floating gate and the control gate, a side wall portion of the gate electrode of the high-voltage transistor, a side wall portion of the gate electrode of the intermediate-voltage transistor, and a side wall portion of the gate electrode of the low-voltage transistor.

Subsequently, with the ion-implantation method, within the active region **16***a* on both sides of the floating gate **20** and the control gate **24***a* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **30** is formed. Accordingly, the source and the drain region **32** having the extension area **26** and the high-concentration impurity area **30** are formed.

Further, with the ion-implantation method, within the active region **16***b* on both sides of the gate electrode **24***b* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **52** is formed. Accordingly, the source and the drain region **54** having the extension area **50** and the high-concentration impurity area **52** are formed.

Furthermore, with the ion-implantation method, within the active region **16***c* on both sides of the gate electrode **24***c* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **62** is formed. Accordingly, the source and the drain region **64** having the extension area **60** and the high-concentration impurity area **62** are formed.

In addition, with the ion-implantation method, within the active region **16***d* on both sides of the gate electrode **24***d* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **72** is formed. Accordingly, the source and the drain region **74** having the extension area **70** and the high-concentration impurity area **72** are formed.

Subsequently, the silicide films **34** are formed on the control gate **24***a*, the gate electrodes **24***b* to **24***d*, and the source and the drain regions **32**, **54**, **64**, and **74** (refer to FIGS. **29**A and **29**B). The silicide films **34** on the source and the drain regions **32**, **54**, **64**, and **74** function as source and drain electrodes.

Subsequently, with the CVD method to the whole substrate, the inter-layer insulating film **78** having a silicon oxidation film is formed.

Subsequently, with the photolithography technology, the contact hole **80** reaching the source and the drain electrode **34** is formed.

Subsequently, with the CVD method to the whole substrate, a conductive film is formed.

Subsequently, with the CMP method, the conductive film is polished until exposing the surface of the inter-layer insulating film **78**. Thus, the conductive plug **82** containing the conductive film is embedded into the contact hole **80** (Refer to FIGS. **30**A and **30**B).

Subsequently, with the CVD method to the whole substrate, the inter-layer insulating film **84** containing, e.g., a silicon oxidation film is formed.

Subsequently, the trench **85** for embedding the wiring **86** is formed to the inter-layer insulating film **84**.

Subsequently, with the sputtering method to the whole substrate, the conductive film is formed.

Subsequently, with the photolithography technology, the conductive film is patterned. Thus, the wiring **86** having conductive film is embedded into the trench **85**.

As mentioned above, the semiconductor device according to the first embodiment is manufactured (refer to FIGS. **31**A and **31**B).

As mentioned above, according to the first embodiment, in a state in which there is the sacrificial oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8** without removing the sacrificial oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8**, the tunnel insulating film **18** is formed. Hence, it is possible to prevent the silicon oxidation film from being grown to be thick on the active region **16***d* of the low-voltage transistor forming region **8**. Therefore, upon removing the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8**, it is possible to prevent the excessive etching of the device separating area **14***d* of the low-voltage transistor forming region **8**, and also possible to possible to prevent the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** from being extremely lower than the active region **16***d*.

Further, according to the first embodiment, in a state in which there is the ONO film **22** on the active region **16***d* of the low-voltage transistor forming region **8** without removing the ONO film **22** on the active region **16***d* of the low-voltage transistor forming region **8**, the gate insulating film **46** of the high-voltage transistor **56** and the gate insulating film **58** of the intermediate-voltage transistor **66** are formed. As a consequence, it is possible to prevent the silicon oxidation film **92** from being grown to be thick on the active region **16***d* of the low-voltage transistor **76**. Therefore, it is possible to prevent the excessive etching of the device separating area **14***d* of the low-voltage transistor forming region **8** upon removing the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8**, and is also possible to prevent the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** from being excessively lower than the active region **16***d*.

Consequently, according to the first embodiment, it is possible to prevent the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** from being strongly pulled in the longitudinal direction, and is also possible to prevent an excessive thin state of a pattern **102***d* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Therefore, according to the first embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can be formed, and the semiconductor device having preferable electrical characteristics can be also provided.

Hereinbelow, a description will be given of a semiconductor device and a method of manufacturing the same according to the second embodiment of the present technique with reference to FIGS. **32**A to **56**B. The same reference numerals as those in the semiconductor device and the method of manufacturing the same according to the first embodiment shown in FIGS. **1**A to **31**B denote the same components, and a description thereof will be omitted or brief.

First of all, a description will be given of the semiconductor device and the method of manufacturing the same according to the second embodiment with reference to FIGS. **32**A to **34**. FIGS. **32**A and **32**B are cross-sectional views showing the semiconductor device according to the second embodiment. FIGS. **33**A to **33**C are plan views showing the semiconductor device having a high-voltage transistor, an intermediate-voltage transistor, and a low-voltage transistor. FIG. **33**A shows the high-voltage transistor, FIG. **33**B shows the intermediate-voltage transistor, and FIG. **33**C shows the low-voltage transistor. FIG. **34** is a graph showing the height of a top surface of the device separating area and the height of the top surface of the active region.

The semiconductor device according to the second embodiment includes: a high-voltage transistor **56**; and an intermediate-voltage transistor **66** having a withstand voltage lower than that of the high-voltage transistor; and a low-voltage transistor **76** having a withstand voltage lower than that of the intermediate-voltage transistor. However, there is a main feature that the semiconductor device does not have the memory cell **36** with the stack gate structure.

The high-voltage transistor forming region **4** includes the trench **12***b* for forming the device separating area **14***b*. On the side wall and the bottom surface of the trench **12***b*, the silicon oxidation film **13** is formed. In the trench **12***b* to which the silicon oxidation film **13** is formed, the device separating area **14***b* for determining the active region **16***b* is embedded. The cross section of the high-voltage transistor forming region **4** shown in FIG. **32**A corresponds to a C-C' cross-section shown in FIG. **33**A, and the cross section of the high-voltage transistor forming region **4** shown in FIG. **32**B corresponds to a D-D' cross-section shown in FIG. **33**A.

On the active region **16***b* in the high-voltage transistor forming region **4**, the gate insulating film **46** with a relatively high thickness is formed. The thickness of the gate insulating film **46** is, e.g., 15 nm.

On the gate insulating film **46**, the gate electrode **24***b* with a relatively long gate length is formed. The gate length of the gate electrode **24***b* is, e.g., 700 nm.

Within the active region **16***b* on both sides of the gate electrode **24***b*, the extension area **50** and a pocket area (not shown) are formed.

On the side wall of the gate electrode **24***b*, the side-wall insulating film **28** is formed.

Within the active region **16***b* on both sides of the gate electrode **24***b* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **52** is formed. The source and the drain region **54** have the extension area **50** and the high-concentration impurity area **52**.

On the gate electrode **24***b* and the source and the drain region **54**, the silicide films **34** are formed. The silicide film **34** on the source and the drain region **54** functions as a the source and the drain electrode.

Accordingly, the high-voltage transistor **56** includes the gate electrode **24***b* and the source and the drain region **54**.

The intermediate-voltage transistor forming region **6** includes the trench **12***c* for forming the device separating area **14***c*. On the side wall and the bottom surface of the trench **12***c*, the silicon oxidation film **13** is formed. The device separating area **14***c* for determining the active region **16***c* is embedded into the trench **12***c* to which the silicon oxidation film **13** is formed. The cross section of the intermediate-voltage transistor forming region **6** shown in FIG. **32**A corresponds to an E-E' cross-section shown in FIG. **33**B, and the cross section of the intermediate-voltage transistor forming region **6** shown in FIG. **32**B corresponds to an F-F' cross-section shown in FIG. **33**B.

On the active region **16***c* within the intermediate-voltage transistor forming region **6**, the gate insulating film **58** is formed with a thickness lower than that of the gate insulating film **46** of the high-voltage transistor **56**. The thickness of the gate insulating film **58** is, e.g., 7 nm.

On the gate insulating film **58**, the gate electrode **24***c* is formed with a gate length shorter than that of the gate electrode **24***b* of the high-voltage transistor **56**. The gate length of the gate electrode **24***c* is 350 nm.

Within the active region **16***c* on both sides of the gate electrode **24***c*, the extension area **60** and a pocket area (not shown) are formed.

On the side wall of the gate electrode **24***c*, the side-wall insulating film **28** is formed.

Within the active region **16***c* on both sides of the gate electrode **24***c* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **62** is formed. The source and the drain region **64** have the extension area **60** and the high-concentration impurity area **62**.

On the gate electrode **24***c* and the source and the drain region **64**, the silicide films **34** are formed. The silicide film **34** on the source and the drain region **64** functions a source and a drain electrode.

Accordingly, the intermediate-voltage transistor **66** includes the gate electrode **24***c* and the source and the drain region **64**.

To the low-voltage transistor forming region **8**, the trench **12***d* for forming the device separating area **14***d* is formed. On the side wall and the bottom surface of the trench **12***d*, the silicon oxidation film **13** is formed. In the trench **12***d* to which

the silicon oxidation film **13** is formed, the device separating area **14***d* for determining the active region **16***d* is embedded. The cross section of the low-voltage transistor forming region **8** shown in FIG. **32**A corresponds to a G-G' cross-section shown in FIG. **33**C, and the cross section of the low-voltage transistor forming region **8** shown in FIG. **32**B corresponds to an H-H' cross-section shown in FIG. **33**C.

On the active region **16***d* in the low-voltage transistor forming region **8**, the gate insulating film **68** is formed with a thickness thinner than that of the gate insulating film **58** of the intermediate-voltage transistor **66**. The thickness of the gate insulating film **68** is, e.g. 1.5 nm.

On the gate insulating film **68**, the gate electrode **24***d* is formed with a gate length shorter than that of the gate electrode **24***c* of the intermediate-voltage transistor **66**. The gate length of the gate electrode **24***d* is 60 nm.

Within the active region **16***d* on both sides of the gate electrode **24***d*, the extension area **70** and a pocket area (not shown) are formed.

On the side wall of the gate electrode **24***d*, the side-wall insulating film **28** is formed.

Within the active region **16***d* on both sides of the gate electrode **24***d* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **72** is formed. The source and the drain region **74** include the extension area **70** and the high-concentration impurity area **72**.

On the gate electrode **24***d* and the source and the drain region **74**, the silicide films **34** are individually formed. The silicide film **34** on the source and the drain region **74** functions as a source and drain electrode.

Accordingly, the low-voltage transistor **76** includes the gate electrode **24***d* and the source and the drain region **74**.

FIG. **34** is a graph showing the height of the top surface of the device separating area relative to the top surface of the active region.

Referring to FIG. **34**, according to the second embodiment, the height of the top surface of the device separating area **14***b* in the high-voltage transistor forming region **4** is substantially equal to the height of the top surface of the active region **16***b* of the high-voltage transistor forming region **4**.

Further, according to the second embodiment, the height of the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** is lower, by 6 nm, than the height of the top surface of the active region **16***c* of the intermediate-voltage transistor forming region **6**.

Furthermore, according to the second embodiment, the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** is substantially equal to the height of the top surface of the active region **16***d* of the low-voltage transistor forming region **8**. That is, according to the second embodiment, the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** is higher than the height of the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6**.

Upon forming the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with a general method, the height of the top surface of the device separating area in the intermediate-voltage transistor forming region is lower than the height of the top surface of the device separating area in the high-voltage transistor forming region, and the height of the top surface of the device separating area in the low-voltage transistor forming region is lower than the height of the top surface of the device separating area in the intermediate-voltage transistor forming region. Therefore, the height of the top surface of the device separating area in the low-voltage transistor forming region is extremely lower than the height of the top surface of the active region. Thus, upon forming the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with the general method, the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor is strongly pulled in the longitudinal direction, and the pattern of the photoresist film for patterning the gate electrode of the low-voltage transistor is extremely thin. Accordingly, upon forming the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor with the general method, it is not possible to form the low-voltage transistor having the gate electrode with a desired gate length, and the semiconductor device having preferable electrical characteristics cannot be provided.

On the other hand, according to the second embodiment, the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** is not extremely lower than the height of the top surface of the active region **16***d* of the low-voltage transistor forming region **8**. As a consequence, the pattern **102***c* (refer to FIGS. **51**A and **51**B) of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** is not strongly pulled in the longitudinal direction, and it is thus possible to prevent, from becoming extremely thin, the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Therefore, according to the second embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can be formed and the semiconductor device having preferable electrical characteristics can be provided.

On the semiconductor substrate **10** having the high-voltage transistor **56**, the intermediate-voltage transistor **66**, and the low-voltage transistor **76**, the inter-layer insulating film **78** are formed.

The inter-layer insulating film **78** has the contact hole **80** reaching the source and the drain electrode **34**. The contact plug **82** is embedded in the contact hole **80**.

On the inter-layer insulating film **78** in which the contact plug **82** is embedded, the inter-layer insulating film **84** is formed.

To the inter-layer insulating film **84**, the trench **85** for embedding the wiring **86** is formed.

The wiring **86** is embedded in the trench **85** formed to the inter-layer insulating film **84**. The wiring **86** is electrically connected to the source and the drain electrode **34** via the contact plug **82**.

As mentioned above, according to the second embodiment, the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** is substantially equal to the height of the top surface of the active region **16***d* of the low-voltage transistor forming region **8**. That is, according to the second embodiment, since the height of the top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** is not extremely lower than the height of the top surface of the active region **16***d* in the low-voltage transistor forming region **8**, it is possible to prevent, from being strongly pulled in the longitudinal direction, the pattern **102***c* (refer to FIGS. **51**A and **51**B) of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Further, it is possible to prevent, from being excessively thin, the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Therefore, according to the second embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can be formed and the semiconductor device having preferable electrical characteristics can be also provided.

As mentioned above, the semiconductor device according to the second embodiment can be structured.

Next, a description will be given of a method of manufacturing the semiconductor device according to the second embodiment with reference to FIGS. **35**A to **56**B. FIGS. **35**A to **56**B are cross-sectional views of the step of manufacturing the semiconductor device according to the second embodiment.

First of all, with the thermal oxidation method, the silicon oxidation film **88** with a thickness of 10 nm is formed on the semiconductor substrate **10**. As the semiconductor substrate **10**, e.g., a silicon substrate is used.

Subsequently, with the CVD method to the whole substrate, the silicon nitride film **90** with a thickness of 50 nm is formed.

Subsequently, with the spin coat method to the whole substrate, a photoresist film (not shown) is coated. When the minimal width of the active regions **16***a* to **16***d* is 50 nm, the thickness of photoresist film is 100 nm.

Subsequently, with the photolithography technology, the photoresist film is patterned.

Subsequently, by using the photoresist film as the mask, the silicon nitride film **90** is subjected to anisotropic etching. In this case, the photoresist film on the silicon nitride film **90** is substantially removed by etching. Thereafter, the photoresist film remaining on the silicon nitride film **90** is removed.

Subsequently, by using the silicon nitride film **90** as the mask, the semiconductor substrate **10** is etched. Thus, the trenches **12***b* to **12***d* with a depth of 150 nm are respectively formed in the memory cell forming region **2**, the high-voltage transistor forming region **4**, the intermediate-voltage transistor forming region **6**, and the low-voltage transistor forming region **8** (refer to FIGS. **35**A and **35**B). Upon etching the semiconductor substrate **10** by using the silicon nitride film **90** as the mask, the top of the silicon nitride film **90** is slightly etched and the thickness of the silicon nitride film **90** is thus 40 nm.

Subsequently, with the thermal oxidation method, the side wall and the bottom surface of the trenches **12***a* to **12***d* are oxidized. Thus, the silicon oxidation film **13** with a thickness of 2 nm is formed to the bottom surfaces and the side walls of the trenches **12***b* to **12***d*.

Subsequently, with a high-density plasma CVD method to the whole substrate, the silicon oxidation film **14** is with a thickness of 200 nm (refer to FIGS. **36**A and **36**B).

Subsequently, referring to FIGS. **37**A and **37**B, with the CMP method, the silicon oxidation film **14** is polished until exposing the surface of the silicon nitride film **90**. In this case, since the surface of the silicon nitride film **90** is slightly polished, the thickness of the silicon nitride film **90** is 20 nm. The silicon nitride film **90** is formed on the silicon oxidation film **88** with a thickness of 10 nm formed on the semiconductor substrate **10**, and the height of the top surface of the silicon nitride film **90** is therefore 30 nm from the surface of the semiconductor substrate **10**. The heights of the top surfaces of the device separating areas **14***b* to **14***d* containing the silicon oxidation films embedded to trenches **14***b* to **14***d* are equal to the height of the top surface of the silicon nitride film **90**. The top surfaces of the device separating areas **14***b* to **14***d* are higher, by 30 nm, than the surface of the semiconductor substrate **10**.

Subsequently, with hydrofluoric acid, the device separating areas **14***b* to **14***d* are etched with a thickness of 6 nm. After etching the device separating areas **14***b* to **14***d* with the thickness of 6 nm, the top surfaces of the device separating areas **14***b* to **14***d* are higher, by 24 nm, than the surface of the semiconductor substrate **10**. The device separating areas **14***b* to **14***d* are etched with the thick of 6 nm because the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** is finally set to be substantially equal to the height of the top surface of the active region **16***d*.

Subsequently, with heated phosphoric acid, the silicon nitride film **90** is removed by etching (refer to FIGS. **38**A and **38**B). The etching the silicon nitride film **90** with the phosphoric acid sufficiently ensures an etching selection ratio of the silicon nitride film **90** to the silicon oxidation film **88**, and almost the silicon oxidation film **88** on the active regions **16***b* to **16***d* thus remains without etching. Therefore, the silicon oxidation films **88** remains with a thickness of 10 nm on the active regions **16***b* to **16***d*.

Subsequently, referring to FIGS. **39**A and **39**B, with hydrofluoric acid, the silicon oxidation films **88** on the active regions **16***b* to **16***d* are removed by etching. The silicon oxidation film **88** with the thickness of 10 nm is etched for a time period necessary for etching the silicon oxidation film with a thickness of 12 nm as that of 1.2 multiples of the silicon oxidation film **88**. Therefore, the silicon oxidation film forming the device separating areas **14***b* to **14***d* is etched with the thickness of 12 nm. Therefore, after etching the silicon oxidation film **88**, the top surfaces of the device separating areas **14***b* to **14***d* are higher, by 12 nm, than the top surfaces of the active regions **16***b* to **16***d*.

Subsequently, referring to FIGS. **40**A and **40**B, with the thermal oxidation method to the whole substrate, the sacrificial oxidation film **92** containing a silicon oxidation film with a thickness of 10 nm is formed.

Subsequently, referring to FIGS. **41**A and **41**B, with the CVD method to the whole substrate, a silicon nitride film **104** with a thickness of 3 to 7 nm is formed. Herein, the thickness of the silicon nitride film **104** is, e.g., 5 nm.

Subsequently, with the ion-implantation method, dopant impurities are guided to the high-voltage transistor forming region **4**, the intermediate-voltage transistor forming region **6**, and the low-voltage transistor forming region **8**, thereby properly forming a predetermined conductive well (not shown).

Further, with the ion-implantation method, dopant impurities are guided to the high-voltage transistor forming region **4**, the intermediate-voltage transistor forming region **6**, and the low-voltage transistor forming region **8**, thereby properly forming a threshold-voltage control layer (not shown).

Herein, although the well and the threshold-voltage control layer are formed after forming the silicon nitride film **104**, the well and the threshold-voltage control layer may be formed after forming the sacrificial oxidation film **92**, before forming the silicon nitride film **104**.

Subsequently, with the spin coat method to the whole substrate, a photoresist film **106** is formed.

Subsequently, with the photolithography technology, the photoresist film **106** is patterned. Thus, the photoresist film **106** for covering the low-voltage transistor forming region **8** is formed.

Subsequently, by using the photoresist film **106** as the mask, the silicon nitride films **104** in the high-voltage transistor forming region **4** and the intermediate-voltage transistor forming region **6** are removed by etching (refer to FIGS. **42**A and **42**B).

Subsequently, by using the photoresist film **106** as the mask, the sacrificial oxidation films **92** in the high-voltage transistor forming region **4** and the intermediate-voltage transistor forming region **6** are removed by etching (refer to FIGS. **43**A and **43**B). As etching solution, e.g., hydrofluoric acid is used. The sacrificial oxidation film **92** with a thickness of 10

nm is etched for a time period necessary for etching the silicon oxidation film with a thickness of 12 nm as that of 1.2 multiples of the sacrificial oxidation film **92**. Therefore, after etching the sacrificial oxidation film **92**, the height of the top surface of the device separating area **14***b* in the high-voltage transistor forming region **4** and the height of the top surface of the device separating area **14***c* in the intermediate-voltage transistor forming region **6** are substantially equal to the height of the top surface of the active regions **16***b* and **16***c*. Since the device separating area **16***d* in the low-voltage transistor forming region **8** is covered with the photoresist film **106**, it is not etched. The top surface of the device separating area **14***d* in the low-voltage transistor forming region **8** maintains to be higher, by 12 nm, than the top surface of the active region **16***d*. Thereafter, the photoresist film **106** is peeled.

Herein, the description is given of the case of removing, by etching, the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6**. However, the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6** may not be removed by the etching. The etching using the photoresist film for covering the intermediate-voltage transistor forming region **6** and the low-voltage transistor forming region **8** enables the etching of the sacrificial oxidation film **92** in the intermediate-voltage transistor forming region **6** to be prevented.

Subsequently, referring to FIGS. **44**A and **44**B, the gate insulating film **46** is formed with a thickness of 15 nm on the active region **16***b* of the high-voltage transistor forming region **4**. In this case, the gate insulating film **46** is also formed with a thickness of 15 nm on the active region **16***c* of the intermediate-voltage transistor forming region **6**. The silicon nitride film **104** has the oxidation resistance. Therefore, in a region covered by the silicon nitride film **104**, i.e., the low-voltage transistor forming region **8**, the silicon oxidation film is not grown.

Subsequently, with the spin coat method to the whole substrate, a photoresist film **108** is formed.

Subsequently, with the photolithography technology, the photoresist film **108** is patterned. Thus, the photoresist film **108** for exposing the intermediate-voltage transistor forming region **6** is formed.

Subsequently, by using the photoresist film **108** as the mask, the gate insulating film **46** on the active region **16***c* of the intermediate-voltage transistor forming region **6** is removed by etching (refer to FIGS. **45**A and **45**B). As etching solution, e.g., hydrofluoric acid is used. The gate insulating film **46** with a thickness of 15 nm is etched for a time period necessary for etching the silicon oxidation film with a thickness of 18 nm, as that of 1.2 multiples of the gate insulating film **46**. Therefore, after etching the gate insulating film **46**, the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** is lower, by 6 nm, than the top surface of the active region **16***c*. On the other hand, the height of the top surface of the device separating area **14***b* of the high-voltage transistor forming region **4** maintains to be substantially equal to the height of the top surface of the active region **16***b*. Further, the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** also maintains to be substantially equal to the height of the top surface of the active region **16***d*. Thereafter, the photoresist film **108** is peeled.

Subsequently, referring to FIGS. **46**A and **46**B, with the thermal oxidation method, the gate insulating film **58** is formed with a thickness of 7 nm on the active region **16***c* of the intermediate-voltage transistor forming region **6**. As mentioned above, the silicon nitride film **104** has the oxidation resistance. Therefore, in a region covered by the silicon nitride film **104**, i.e., the low-voltage transistor forming region **8**, the silicon oxidation film is not grown.

Subsequently, with the spin coat method to the whole substrate, a photoresist film **110** is formed.

Subsequently, with the photolithography technology, the photoresist film **110** is patterned. Thus, the photoresist film **110** for exposing the low-voltage transistor forming region **8** is formed.

Subsequently, by using the photoresist film **110** as the mask, the silicon nitride film **104** on the active region **16***d* of the low-voltage transistor forming region **8** is removed by etching (refer to FIGS. **47**A and **47**B). The etching of the silicon nitride film **104** is used, e.g., dry etching.

Subsequently, referring to FIGS. **48**A and **48**B, by using the photoresist film **110** as the mask, the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8** is removed by etching. As etching solution, e.g., hydrofluoric acid is used. The silicon oxidation film **92** is etched for a time period necessary for etching a silicon oxidation film with a thickness of 12 nm as that of 1.2 multiples of the silicon oxidation film **92**. Therefore, after etching the gate insulating film **92**, the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** is substantially equal to the height of the top surface of the active region **16***d*. On the other hand, the height of the top surface of the device separating area **14***b* in the high-voltage transistor forming region **4** maintains to be substantially equal to the height of the top surface of the active region **16***b*. Further, the top surface of the device separating area **14***c* of the intermediate-voltage transistor forming region **6** maintains to be lower, by 6 nm, than the top surface of the active region **16***c*. Thereafter, the photoresist film **110** is peeled.

Subsequently, referring to FIGS. **49**A and **49**B, with the thermal oxidation method, the gate insulating film **68** is formed with a thickness of 1.5 nm on the active region **16***d* of the low-voltage transistor forming region **8**.

Subsequently, referring to FIGS. **50**A and **50**B, with the CVD method, the polysilicon film **24** is formed with a thickness of 100 nm.

Subsequently, with the spin coat method to the whole substrate, a photoresist film **102** is formed.

Subsequently, with the photolithography technology, the photoresist film **102** is patterned. Thus, the pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* of the high-voltage transistor **56**, the pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* of the intermediate-voltage transistor **66**, and the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** are formed (refer to FIGS. **51**A and **51**B).

Referring to FIGS. **34**A and **34**B, in the high-voltage transistor forming region **4**, the height of the top surface of the device separating area **14***b* is substantially equal to the height of the top surface of the active region **16***b*. Further, in the intermediate-voltage transistor forming region **6**, the height of the top surface of the device separating area **14***c* is lower, by 6 nm, than the top surface of the active region **16***c*. Furthermore, in the low-voltage transistor forming region **8**, the height of the top surface of the device separating area **14***d* is substantially equal to the height of the top surface of the active region **16***d*.

In the low-voltage transistor forming region **8**, since the height of the top surface of the device separating area **14***d* is substantially equal to the height of the top surface of the active region **16***d*, it is possible to prevent, from being strongly pulled in the longitudinal direction, the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the

low-voltage transistor **76**. Therefore, according to the second embodiment, it is possible to prevent, from being excessively thin, the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76**. Accordingly, according to the second embodiment, the low-voltage transistor **76** having the gate electrode **24***d* with a desired gate length can formed, and the semiconductor device having preferable electrical characteristics can be also provided.

Also in the intermediate-voltage transistor forming region **6**, since the top surface of the device separating area **14***c* is lower than the top surface of the active region **16***c* to some degree, the pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* of the intermediate-voltage transistor **66** is pulled in the longitudinal direction. However, since the gate length of the gate electrode **24***c* of the intermediate-voltage transistor **66** is relatively long, i.e., 350 nm, even if the pattern **102***b* of the photoresist film for patterning the gate electrode **24***c* is thinner by several nanometers, this does not influence on electrical characteristics of the intermediate-voltage transistor **66**.

Further, also in the high-voltage transistor forming region **4**, since the top surface of the device separating area **14***b* is lower than the top surface of the active region **16***b* to some degree, the pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* of the high-voltage transistor **56** is pulled in the longitudinal direction. However, the gate length of the gate electrode **24***b* of the high-voltage transistor **56** is relatively long, i.e., 700 nm, even if the pattern **102***a* of the photoresist film for patterning the gate electrode **24***b* is thinner by several nanometers, this does not influence on electrical characteristics of the high-voltage transistor **56**.

Subsequently, by using the photoresist film **102** as the mask, the polysilicon film **24** is etched. Thus, the gate electrode **24***b* of the high-voltage transistor **56**, the gate electrode **24***c* of the intermediate-voltage transistor **66**, and the gate electrode **24***d* of the low-voltage transistor **76** are individually formed (refer to FIGS. **52**A and **52**B).

Subsequently, with the ion-implantation method, dopant impurities are guided to the active region **16***a* on both sides of the control gate **24***a*, and the extension area **26** and a pocket area (not shown) are formed.

Further, dopant impurities are guided to the active region **16***b* on both sides of the gate electrode **24***b*, and the extension area **50** and a pocket area (not shown) are formed.

Furthermore, dopant impurities are guided to the active region **16***c* on both sides of the gate electrode **24***c*, thereby forming the extension area **60** and a pocket area (not shown).

In addition, dopant impurities are guided to the active region **16***d* on both sides of the gate electrode **24***d*, and the extension area **70** and a pocket area (not shown) are formed (refer to FIGS. **53**A and **53**B).

Subsequently, the side-wall insulating films (side-wall spacer) **28** is formed to a side wall portion of the gate electrode **24***b* of the high-voltage transistor **56**, a side wall portion of the gate electrode **24***c* of the intermediate-voltage transistor **66**, and a side wall portion of the gate electrode **24***d* of the low-voltage transistor **76**.

Subsequently, with the ion-implantation method, within the active region **16***b* on both sides of the gate electrode **24***b* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **52** is formed. As mentioned above, the source and the drain region **54** has the extension area **50** and the high-concentration impurity area **52**.

Further, with the ion-implantation method, within the active region **16***c* on both sides of the gate electrode **24***c* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **62** is formed. As mentioned above, the source and the drain region **64** has the extension area **60** and the high-concentration impurity area **62**.

Furthermore, with the ion-implantation method, within the active region **16***d* on both sides of the gate electrode **24***d* to which the side-wall insulating film **28** is formed, the high-concentration impurity area **72** is formed. As mentioned above, the source and the drain region **74** has the extension area **70** and the high-concentration impurity area **72**.

Subsequently, on the gate electrodes **24***b* to **24***d* and the source and the drain regions **54**, **64**, and **74**, the silicide films **34** are formed (refer to FIGS. **54**A and **54**B). The silicide films **34** on the source and the drain regions **54**, **64**, and **74** function as the source and the drain electrodes.

Subsequently, with the CVD method to the whole substrate, the inter-layer insulating film **78** containing a silicon oxidation film is formed.

Subsequently, with the photolithography technology, the contact hole **80** reaching the source and the drain electrode **34** is formed.

Subsequently, with the CVD method to the whole substrate, a conductive film is formed.

Subsequently, with the CMP method, a conductive film is polished until exposing the surface of the inter-layer insulating film **78**. Thus, the conductive plug **82** containing the conductive film is embedded into the contact hole **80** (refer to FIGS. **55**A and **55**B).

Subsequently, with the CVD method to the whole substrate, the inter-layer insulating film **84** containing a silicon oxidation film is formed.

Subsequently, the trench **85** for embedding the wiring **86** is formed to the inter-layer insulating film **84**.

Subsequently, with the sputtering method to the whole substrate, a conductive film is formed.

Subsequently, the conductive film is patterned. Thus, the wiring **84** having the conductive film is embedded into the trench **85**.

Accordingly, the semiconductor device according to the first embodiment is manufactured (refer to FIGS. **56**A and **56**B).

As mentioned above, according to the second embodiment, while there is the silicon nitride film **104** on the active region **16***d* of the low-voltage transistor forming region **8** without removing the silicon nitride film **104** on the active region **16***d* of the low-voltage transistor forming region **8**, the gate insulating film **46** of the high-voltage transistor **56** and the gate insulating film **58** of the intermediate-voltage transistor **66** are formed. Therefore, it is possible to prevent, from being grown to be thin, the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor **76**. Further, it is possible to prevent the excessive etching of the device separating area **14***d* of the low-voltage transistor forming region **8** upon removing the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8**. Furthermore, it is possible to prevent the height of the top surface of the device separating area **14***d* of the low-voltage transistor forming region **8** from being excessively lower than the active region **16***d*. Consequently, according to the second embodiment, it is possible to prevent the pattern **102***c* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** from being strongly pulled in the longitudinal direction. In addition, it is possible to prevent the pattern **102***d* of the photoresist film for patterning the gate electrode **24***d* of the low-voltage transistor **76** from being excessively thin. Therefore, according to the second embodiment, it is possible to form the low-voltage transistor **76**

having the gate electrode **24***d* with a desired gate length, and the semiconductor device having preferable electrical characteristics can also be provided.

The present technique is not limited to the embodiments and can be variously modified.

According to the second embodiment, while there is the silicon nitride film **102** on the active region **16***d* of the low-voltage transistor forming region **8**, the gate insulating film **46** is formed on the active region **16***b* of the high-voltage transistor forming region **4** and the gate insulating film **58** is also formed on the active region **16***c* of the intermediate-voltage transistor forming region **4**. However, the silicon nitride film **102** may not be formed. If forming the gate insulating film **46** on the active region **16***b* of the high-voltage transistor forming region **4** and further forming the gate insulating film **58** on the active region **16***c* of the intermediate-voltage transistor forming region **4** while there is the silicon oxidation film **92** on the active region **16***d* of the low-voltage transistor forming region **8**, it is possible to prevent the silicon oxidation film from being grown to be thin on the active region **16***d* of the low-voltage transistor forming region **8**. However, if forming the gate insulating film **46** on the active region **16***b* of the high-voltage transistor forming region **4** and further forming the gate insulating film **58** on the active region **16***c* of the intermediate-voltage transistor forming region **4** while forming the silicon nitride film **104** on the active region **16***d* of the low-voltage transistor forming region **8**, it is possible to prevent the silicon oxidation film from being grown on the active region **16***d* of the low-voltage transistor forming region **8** without fail. Consequently, preferably, while forming the silicon nitride film **104** on the active region **16***d* of the low-voltage transistor forming region **8**, the gate insulating film **46** is formed on the active region **16***b* of the high-voltage transistor forming region **4** and the gate insulating film **58** is also formed on the active region **16***c* of intermediate-voltage transistor forming region **4**.

Further, according to the embodiments, the description is given of the example of forming the high-voltage transistor **56**, the intermediate-voltage transistor **66**, and the low-voltage transistor **76**. However, the three types of transistors including the high-voltage transistor, the intermediate-voltage transistor, and the low-voltage transistor may not be provided. The present technique can be widely applied to the semiconductor device having two or more types of transistors having different withstand-voltages, i.e., the semiconductor device including two or more types of transistors with different thicknesses of the gate insulating film.

Furthermore, according to the embodiments, as the film having the oxidation resistance, the silicon nitride film **104** is formed as the example. However, the film having the oxidation resistance is not limited to the silicon nitride film **104**. For example, as the film having the oxidation resistance, a carbonized silicon film may be formed.

As mentioned above in details, the features of the present technique are summarized as follows.

What is claimed is:

1. A semiconductor device comprising:

a substrate;

a first insulator formed in a first area of the substrate, and a second insulator formed in a second area of the substrate;

a first transistor formed over a first device region surrounded by the first area, the first transistor comprising

a first gate insulating film having a first thickness, the first gate insulating film being formed over the first device region,

a first gate electrode formed over the first gate insulating film, and

first source and drain regions formed in the first device region at both sides of the first gate electrode;

a second transistor formed over a second device region surrounded by the second area, the second transistor comprising

a second gate insulating film formed over the second device region, the second gate insulating film having a second thickness less than the first thickness of the first gate insulating film,

a second gate electrode formed over the second gate insulating film, and

second source and drain regions formed in the second device region at both sides of the second gate electrode;

a third insulator formed in a third area of the substrate; and

a memory cell formed over a third device region surrounded by the third area, the memory cell further comprising

a tunnel insulating film formed over the third device region,

a floating gate formed over the tunnel insulating film,

an insulating film formed over the floating gate,

a control gate formed over the tunnel insulating film, and

third source and drain regions formed in third device region at both sides of the floating gate and the control gate;

wherein a first height of a top surface of the first insulator is less than a second height of a top surface of the second insulator, and

wherein the first height of the top surface of the first insulator is less than a third height of a top surface of the third insulator.

2. The semiconductor device according to claim **1**, further comprising:

a fourth insulator formed in a fourth area of the substrate; and

a third transistor formed over a fourth device region surrounded by the fourth area, the third transistor further comprising

a fourth gate insulating film formed over the fourth device region, the fourth gate insulating film having a third thickness greater than the first thickness of the first gate insulating film,

a third gate electrode formed over the fourth gate insulating film, and fourth source and

drain regions formed in the fourth device region at both sides of the electrode.

3. The semiconductor device according to claim **1**, wherein the second height of the top surface of the second insulator is less than the height of the top surface of the third insulator.

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