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**Barriac**

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(54) **METHOD AND APPARATUS FOR PROCESSING SUPPLEMENTAL AND NON SUPPLEMENTAL ASSIGNMENTS**

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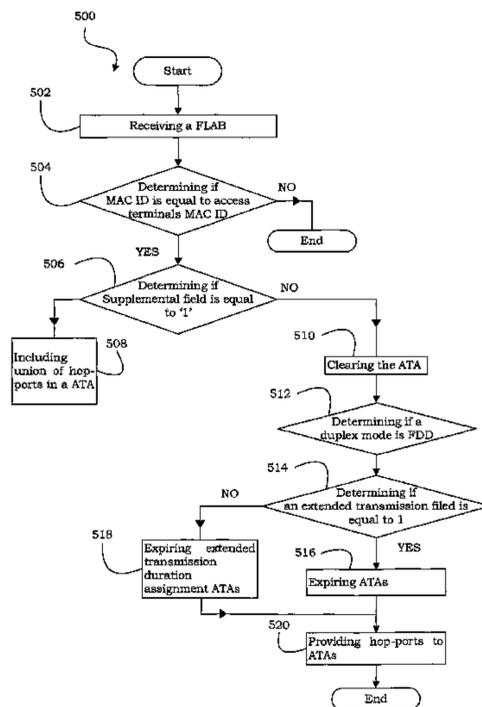
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(57) **ABSTRACT**

A method and apparatus for processing supplemental and non supplement assignments in a wireless communication system are described. A forward link assignment block (FLAB) is received from a shared signaling medium access control (SS MAC) protocol. It is determined if a medium access control identity (MAC ID) of the FLAB is equal to the MAC ID of an access terminal and it is determined if a supplemental field of a FLAB is equal to '1'.

**22 Claims, 6 Drawing Sheets**



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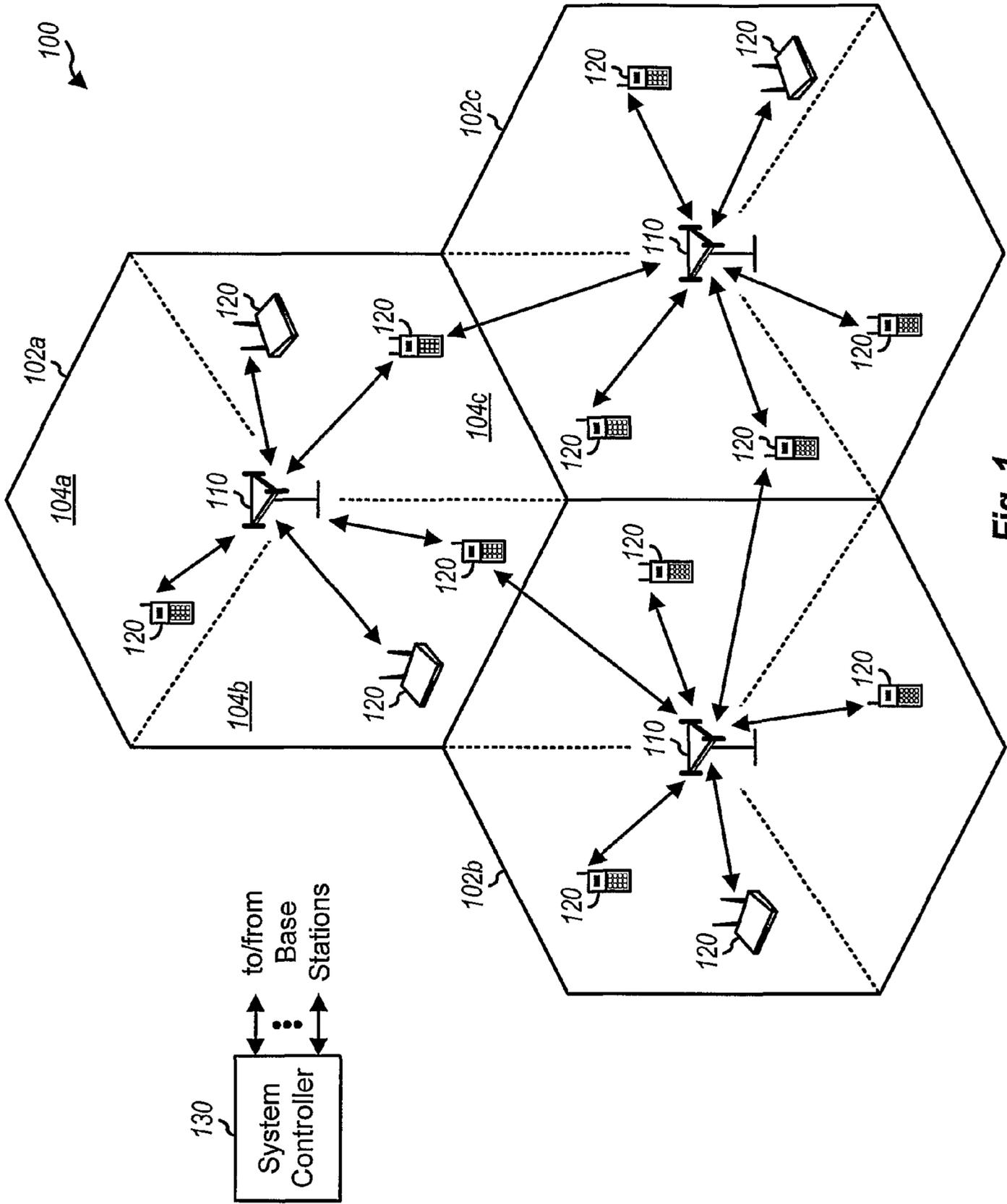


Fig. 1



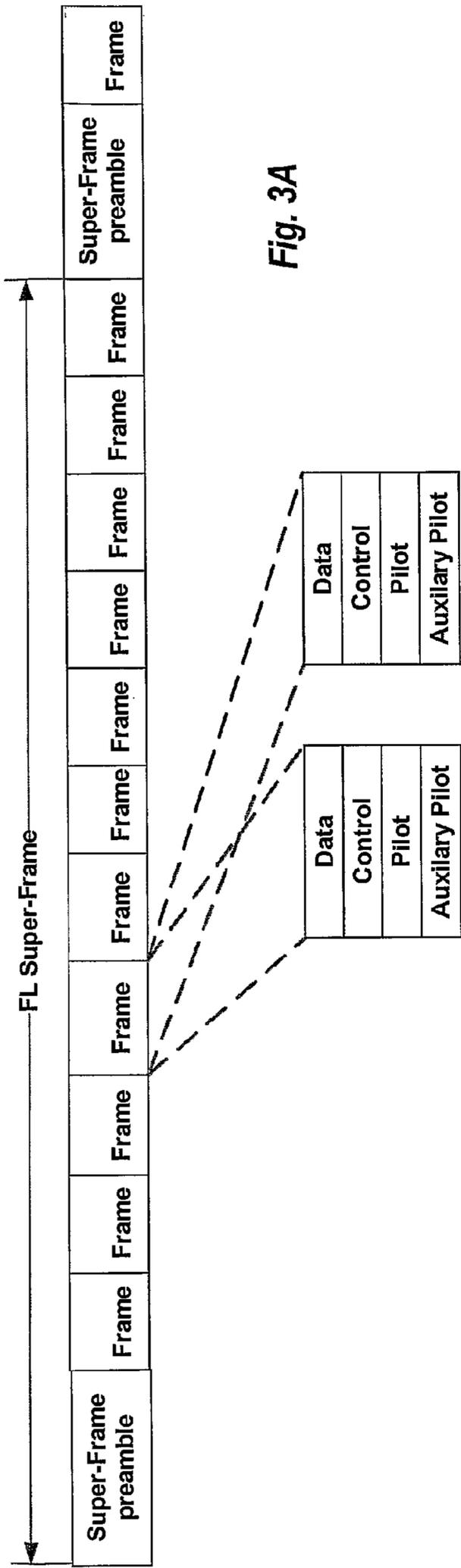


Fig. 3A

Block Hopping mode      Symbol Rate Hopping mode

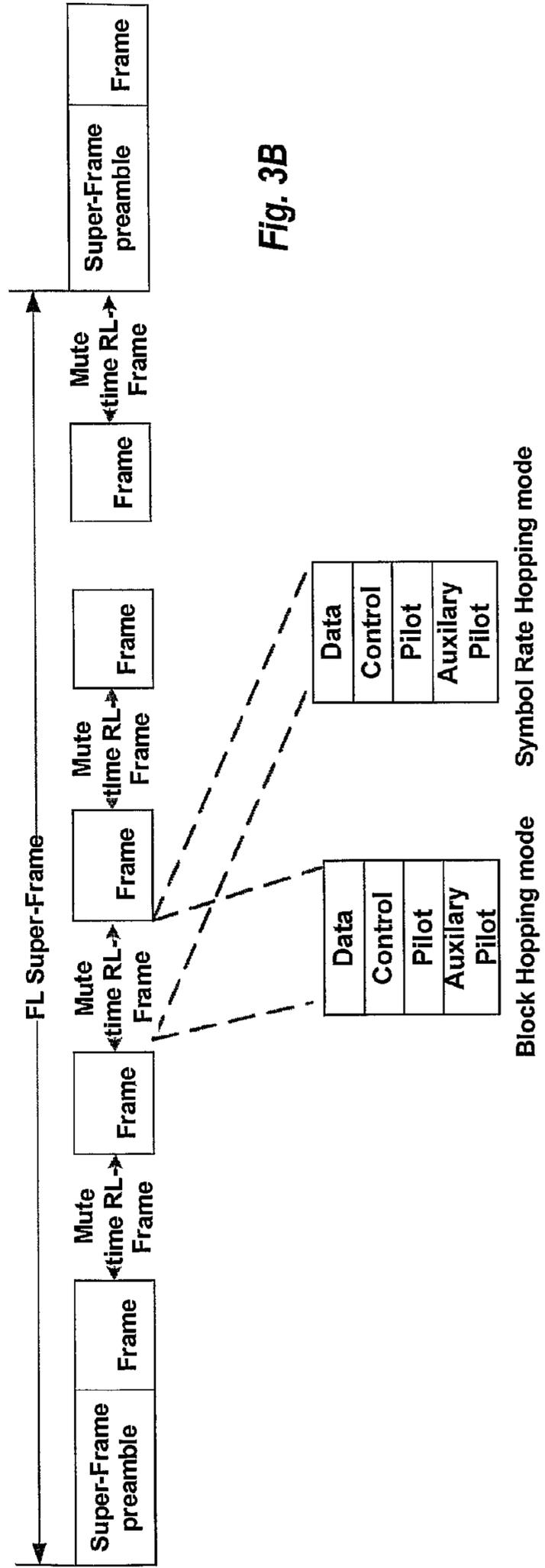


Fig. 3B

Block Hopping mode      Symbol Rate Hopping mode

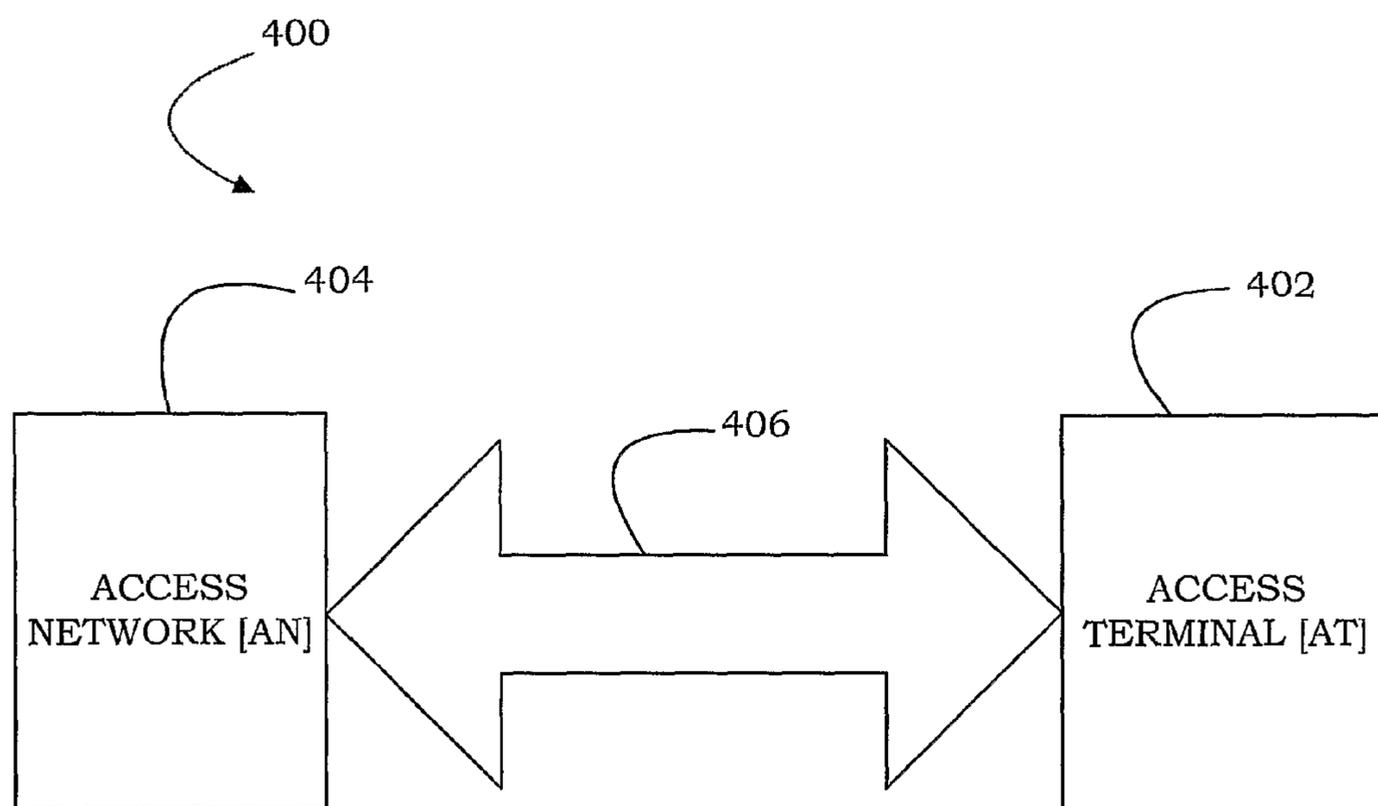


Fig. 4

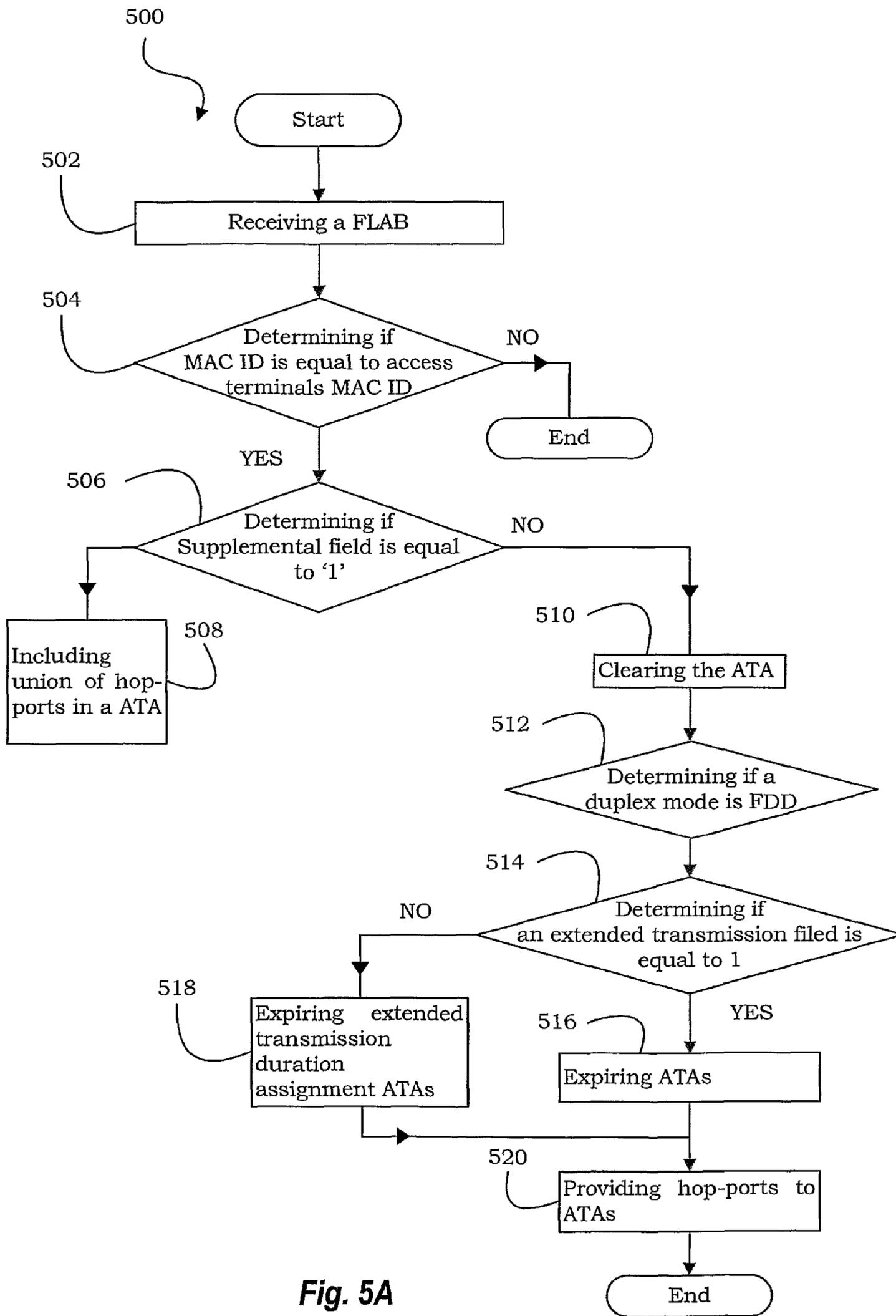


Fig. 5A

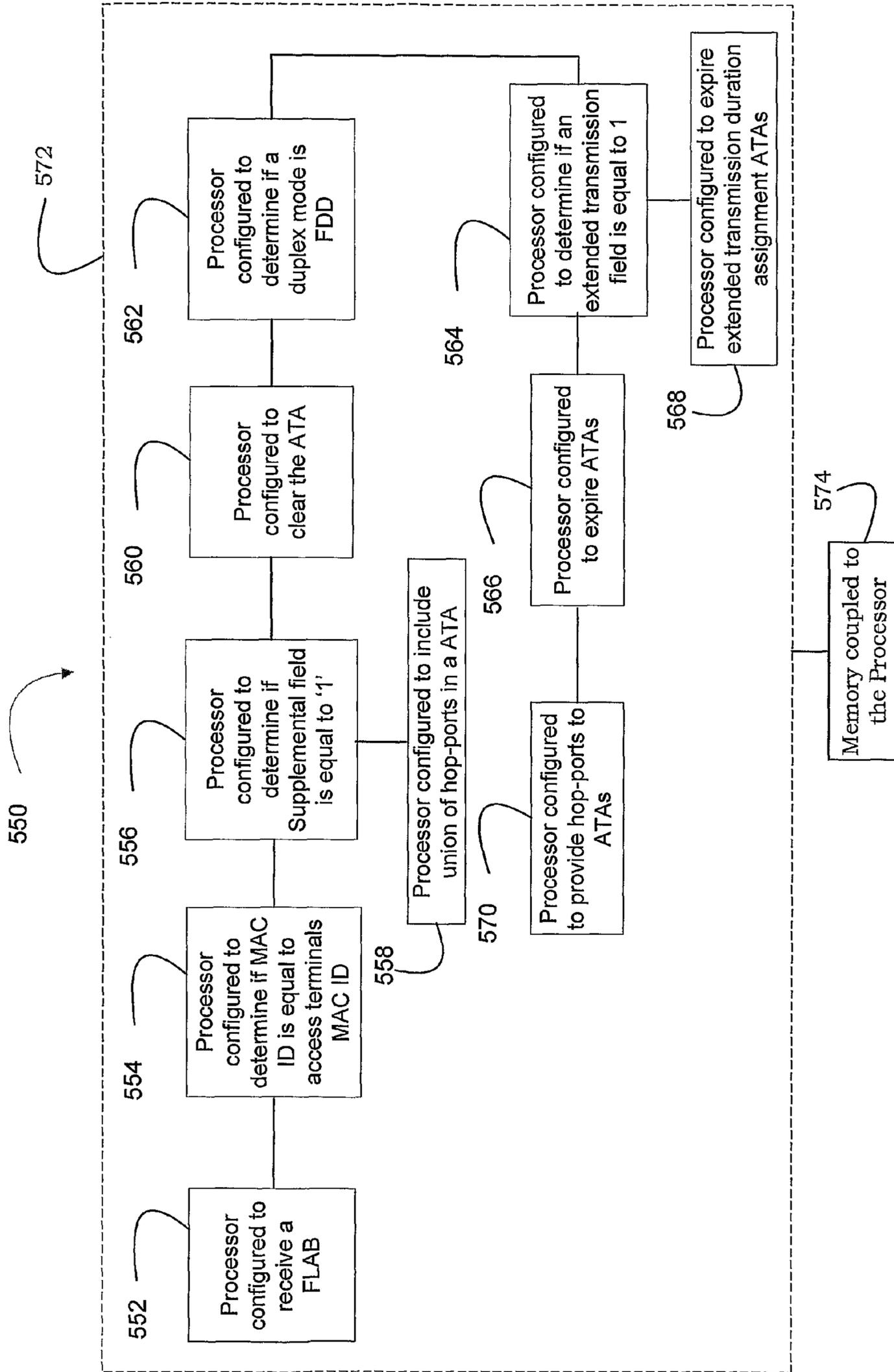


Fig. 5B

**METHOD AND APPARATUS FOR  
PROCESSING SUPPLEMENTAL AND NON  
SUPPLEMENTAL ASSIGNMENTS**

CLAIM OF PRIORITY UNDER 35 U.S.C. §119

The present Application for Patent claims priority to Provisional Application Ser. No. 60/731,037, entitled "METHODS AND APPARATUS FOR PROVIDING MOBILE BROADBAND WIRELESS HIGHER MAC", filed Oct. 27, 2005, assigned to the assignee hereof, and expressly incorporated herein by reference.

BACKGROUND

1. Field

The present disclosure relates generally to wireless communications, and more particularly to methods and apparatus for processing supplemental and non supplemental assignments.

2. Background

Wireless communication systems have become a prevalent means by which a majority of people worldwide have come to communicate. Wireless communication devices have become smaller and more powerful in order to meet consumer needs and to improve portability and convenience. The increase in processing power in mobile devices such as cellular telephones has lead to an increase in demands on wireless network transmission systems. Such systems typically are not as easily updated as the cellular devices that communicate there over. As mobile device capabilities expand, it can be difficult to maintain an older wireless network system in a manner that facilitates fully exploiting new and improved wireless device capabilities.

Wireless communication systems generally utilize different approaches to generate transmission resources in the form of channels. These systems may be code division multiplexing (CDM) systems, frequency division multiplexing (FDM) systems, and time division multiplexing (TDM) systems. One commonly utilized variant of FDM is orthogonal frequency division multiplexing (OFDM) that effectively partitions the overall system bandwidth into multiple orthogonal subcarriers. These subcarriers may also be referred to as tones, bins, and frequency channels. Each subcarrier can be modulated with data. With time division based techniques, each subcarrier can comprise a portion of sequential time slices or time slots. Each user may be provided with a one or more time slot and sub carrier combinations for transmitting and receiving information in a defined burst period or frame. The hopping schemes may generally be a symbol rate hopping scheme or a block hopping scheme.

Code division based techniques typically transmit data over a number of frequencies available at any time in a range. In general, data is digitized and spread over available bandwidth, wherein multiple users can be overlaid on the channel and respective users can be assigned a unique sequence code. Users can transmit in the same wide-band chunk of spectrum, wherein each user's signal is spread over the entire bandwidth by its respective unique spreading code. This technique can provide for sharing, wherein one or more users can concurrently transmit and receive. Such sharing can be achieved through spread spectrum digital modulation, wherein a user's stream of bits is encoded and spread across a very wide channel in a pseudo-random fashion. The receiver is designed to recognize the associated unique sequence code and undo the randomization in order to collect the bits for a particular user in a coherent manner.

A typical wireless communication network (e.g., employing frequency, time, and/or code division techniques) includes one or more base stations that provide a coverage area and one or more mobile (e.g., wireless) terminals that can transmit and receive data within the coverage area. A typical base station can simultaneously transmit multiple data streams for broadcast, multicast, and/or unicast services, wherein a data stream is a stream of data that can be of independent reception interest to a mobile terminal. A mobile terminal within the coverage area of that base station can be interested in receiving one, more than one or all the data streams transmitted from the base station. Likewise, a mobile terminal can transmit data to the base station or another mobile terminal. In these systems the bandwidth and other system resources are assigned utilizing a scheduler.

The signals, signal formats, signal exchanges, methods, processes, and techniques disclosed herein provide several advantages over known approaches. These include, for example, reduced signaling overhead, improved system throughput, increased signaling flexibility, reduced information processing, reduced transmission bandwidth, reduced bit processing, increased robustness, improved efficiency, and reduced transmission power.

SUMMARY

The following presents a simplified summary of one or more aspects in order to provide a basic understanding of such aspects. This summary is not an extensive overview of all contemplated aspects, and is intended to neither identify key or critical elements of all aspects nor delineate the scope of any or all aspects. Its sole purpose is to present some concepts of one or more aspects in a simplified form as a prelude to the more detailed description that is presented later.

According to one embodiment, a method is provided for processing supplemental and non supplemental assignments in a wireless communication system, the method comprising receiving a forward link assignment block (FLAB) from a shared signaling medium access control (SS MAC) protocol, determining if MAC ID of the FLAB is equal to the MAC ID of an access terminal and determining if a supplemental field of a FLAB is equal to '1'.

According to another embodiment, a non-transitory computer readable medium is described having a first set of instructions for receiving a forward link assignment block (FLAB) from a shared signaling medium access control (SS MAC) protocol a second set of instructions for determining if MAC ID of the FLAB is equal to the MAC ID of an access terminal and a third set of instructions for determining if a supplemental field of a FLAB is equal to '1'.

According to yet another embodiment, an apparatus operable in a wireless communication system, is described which includes means for receiving a forward link assignment block (FLAB) from a shared signaling medium access control (SS MAC) protocol, means for determining if MAC ID of the FLAB is equal to the MAC ID of an access terminal and means for determining if a supplemental field of a FLAB is equal to '1'.

To the accomplishment of the foregoing and related ends, the one or more aspects comprise the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative aspects of the one or more aspects. These aspects are indicative, however, of but a few of the various ways in which the principles of various aspects may

be employed and the described aspects are intended to include all such aspects and their equivalents.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates embodiments of a multiple access wireless communication system;

FIG. 2 illustrates embodiments of a transmitter and receiver in a multiple access wireless communication system;

FIGS. 3A and 3B illustrate embodiments of superframe structures for a multiple access wireless communication system;

FIG. 4 illustrate embodiment of a communication between an access terminal and an access network;

FIG. 5A illustrates a flow diagram of a process used by access terminal; and

FIG. 5B illustrates one or more processors configured for processing supplemental and non supplement assignments.

#### DETAILED DESCRIPTION

Various embodiments are now described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more embodiments. It may be evident, however, that such embodiment(s) may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to facilitate describing one or more embodiments.

Referring to FIG. 1, a multiple access wireless communication system according to one embodiment is illustrated. A multiple access wireless communication system 100 includes multiple cells, e.g. cells 102, 104, and 106. In the embodiment of FIG. 1, each cell 102, 104, and 106 may include an access point 150 that includes multiple sectors. The multiple sectors are formed by groups of antennas each responsible for communication with access terminals in a portion of the cell. In cell 102, antenna groups 112, 114, and 116 each correspond to a different sector. In cell 104, antenna groups 118, 120, and 122 each correspond to a different sector. In cell 106, antenna groups 124, 126, and 128 each correspond to a different sector.

Each cell includes several access terminals which are in communication with one or more sectors of each access point. For example, access terminals 130 and 132 are in communication base 142, access terminals 134 and 136 are in communication with access point 144, and access terminals 138 and 140 are in communication with access point 146.

Controller 130 is coupled to each of the cells 102, 104, and 106. Controller 130 may contain one or more connections to multiple networks, e.g. the Internet, other packet based networks, or circuit switched voice networks that provide information to, and from, the access terminals in communication with the cells of the multiple access wireless communication system 100. The controller 130 includes, or is coupled with, a scheduler that schedules transmission from and to access terminals. In other embodiments, the scheduler may reside in each individual cell, each sector of a cell, or a combination thereof.

As used herein, an access point may be a fixed station used for communicating with the terminals and may also be referred to as, and include some or all the functionality of, a base station, a Node B, or some other terminology. An access terminal may also be referred to as, and include some or all the

functionality of a user equipment (UE), a wireless communication device, terminal, a mobile station or some other terminology.

It should be noted that while FIG. 1, depicts physical sectors, i.e. having different antenna groups for different sectors, other approaches may be utilized. For example) utilizing multiple fixed “beams” that each cover different areas of the cell in frequency space may be utilized in lieu of, or in combination with physical sectors. Such an approach is depicted and disclosed in copending U.S. patent application Ser. No. 11/260,895, entitled “Adaptive Sectorization In Cellular System.”

Referring to FIG. 2, a block diagram of an embodiment of a transmitter system 210 and a receiver system 250 in a MIMO system 200 is illustrated. At transmitter system 210, traffic data for a number of data streams is provided from a data source 212 to transmit (TX) data processor 214. In an embodiment, each data stream is transmitted over a respective transmit antenna. TX data processor 214 formats, codes, and interleaves the traffic data for each data stream based on a particular coding scheme selected for that data stream to provide coded data.

The coded data for each data stream may be multiplexed with pilot data using OFDM, or other orthogonalization or non-orthogonalization techniques. The pilot data is typically a known data pattern that is processed in a known manner and may be used at the receiver system to estimate the channel response. The multiplexed pilot and coded data for each data stream is then modulated (i.e., symbol mapped) based on one or more particular modulation schemes (e.g., BPSK, QSPK, M-PSK, or M-QAM) selected for that data stream to provide modulation symbols. The data rate, coding, and modulation for each data stream may be determined by instructions performed on provided by processor 230.

The modulation symbols for all data streams are then provided to a TX processor 220, which may further process the modulation symbols (e.g., for OFDM). TX processor 220 then provides  $N_T$  modulation symbol streams to  $N_T$  transmitters (TMTR) 222a through 222t. Each transmitter 222 receives and processes a respective symbol stream to provide one or more analog signals, and further conditions (e.g., amplifies, filters, and upconverts) the analog signals to provide a modulated signal suitable for transmission over the MIMO channel.  $N_T$  modulated signals from transmitters 222a through 222t are then transmitted from  $N_T$  antennas 224a through 224t, respectively.

At receiver system 250, the transmitted modulated signals are received by  $N_R$  antennas 252a through 252r and the received signal from each antenna 252 is provided to a respective receiver (RCVR) 254. Each receiver 254 conditions (e.g., filters, amplifies, and downconverts) a respective received signal, digitizes the conditioned signal to provide samples, and further processes the samples to provide a corresponding “received” symbol stream.

An RX data processor 260 then receives and processes the  $N_R$  received symbol streams from  $N_R$  receivers 254 based on a particular receiver processing technique to provide  $N_T$  “detected” symbol streams. The processing by RX data processor 260 is described in finer detail below. Each detected symbol stream includes symbols that are estimates of the modulation symbols transmitted for the corresponding data stream. RX data processor 260 then demodulates, deinterleaves, and decodes each detected symbol stream to recover the traffic data for the data stream. The processing by RX data processor 218 is complementary to that performed by TX processor 220 and TX data processor 214 at transmitter system 210.

RX data processor **260** may be limited in the number of subcarriers that it may simultaneously demodulate, e.g. **512** subcarriers or 5 MHz, and such a receiver should be scheduled on a single carrier. This limitation may be a function of its FFT range, e.g. sample rates at which the processor **260** may operate, the memory available for FFT, or other functions available for demodulation. Further, the greater the number of subcarriers utilized the greater the expense of the access terminal.

The channel response estimate generated by RX processor **260** may be used to perform space, space/time processing at the receiver, adjust power levels, change modulation rates or schemes, or other actions. RX processor **260** may further estimate the signal-to-noise-and-interference ratios (SNRs) of the detected symbol streams, and possibly other channel characteristics, and provides these quantities to a processor **270**. RX data processor **260** or processor **270** may further derive an estimate of the “operating” SNR for the system. Processor **270** then provides channel state information (CSI), which may comprise various types of information regarding the communication link and/or the received data stream. For example, the CSI may comprise only the operating SNR. In other embodiments, the CSI may comprise a channel quality indicator (CQI), which may be a numerical value indicative of one or more channel conditions. The CSI is then processed by a TX data processor **278**, modulated by a modulator **280**, conditioned by transmitters **254a** through **254r**, and transmitted back to transmitter system **210**.

At transmitter system **210**, the modulated signals from receiver system **250** are received by antennas **224**, conditioned by receivers **222**, demodulated by a demodulator **240**, and processed by a RX data processor **242** to recover the CSI reported by the receiver system. The reported CSI is then provided to processor **230** and used to (1) determine the data rates and coding and modulation schemes to be used for the data streams and (2) generate various controls for TX data processor **214** and TX processor **220**. Alternatively, the CSI may be utilized by processor **270** to determine modulation schemes and/or coding rates for transmission, along with other information. This may then be provided to the transmitter which uses this information, which may be quantized, to provide later transmissions to the receiver.

Processors **230** and **270** direct the operation at the transmitter and receiver systems, respectively. Memories **232** and **272** provide storage for program codes and data used by processors **230** and **270**, respectively.

At the receiver, various processing techniques may be used to process the NR received signals to detect the  $N_T$  transmitted symbol streams. These receiver processing techniques may be grouped into two primary categories (i) spatial and space-time receiver processing techniques (which are also referred to as equalization techniques); and (ii) “successive nulling/equalization and interference cancellation” receiver processing technique (which is also referred to as “successive interference cancellation” or “successive cancellation” receiver processing technique).

While FIG. 2 discusses a MEMO system, the same system may be applied to a multi-input single-output system where multiple transmit antennas, e.g. those on a base station, transmit one or more symbol streams to a single antenna device, e.g. a mobile station. Also, a single output to single input antenna system may be utilized in the same manner as described with respect to FIG. 2.

The transmission techniques described herein may be implemented by various means. For example, these techniques may be implemented in hardware, firmware, software, or a combination thereof. For a hardware implementation, the

processing units at a transmitter may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, electronic devices, other electronic units designed to perform the functions described herein, or a combination thereof. The processing units at a receiver may also be implemented within one or more ASICs, DSPs, processors, and so on.

For a software implementation, the transmission techniques may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. The software codes may be stored in a memory (e.g., memory **230**, **272x** or **272y** in FIG. 2) and executed by a processor (e.g., processor **232**, **270x** or **270y**). The memory may be implemented within the processor or external to the processor.

It should be noted that the concept of channels herein refers to information or transmission types that may be transmitted by the access point or access terminal. It does not require or utilize fixed or predetermined blocks of subcarriers, time periods, or other resources dedicated to such transmissions.

Referring to FIGS. 3A and 3B, embodiments of superframe structures for a multiple access wireless communication system are illustrated. FIG. 3A illustrates embodiments of superframe structures for a frequency division duplexed (FDD) multiple access wireless communication system, while FIG. 3B illustrates embodiments of superframe structures for a time division duplexed (TDD) multiple access wireless communication system. The superframe preamble may be transmitted separately for each carrier or may span all of the carriers of the sector.

In both FIGS. 3A and 3B, the forward link transmission is divided into units of superframes. A superframe may consist of a superframe preamble followed by a series of frames. In an FDD system, the reverse link and the forward link transmission may occupy different frequency bandwidths so that transmissions on the links do not, or for the most part do not, overlap on any frequency subcarriers. In a TDD system, N forward link frames and M reverse link frames define the number of sequential forward link and reverse link frames that may be continuously transmitted prior to allowing transmission of the opposite type of frame. It should be noted that the number of N and M may vary within a given superframe or between superframes.

In both FDD and TDD systems each superframe may comprise a superframe preamble. In certain embodiments, the superframe preamble includes a pilot channel that includes pilots that may be used for channel estimation by access terminals, a broadcast channel that includes configuration information that the access terminal may utilize to demodulate the information contained in the forward link frame. Further acquisition information such as timing and other information sufficient for an access terminal to communicate on one of the carriers and basic power control or offset information may also be included in the superframe preamble. In other cases, only some of the above and/or other information may be included in this superframe preamble.

As shown in FIGS. 3A and 3B, the superframe preamble is followed by a sequence of frames. Each frame may consist of a same or a different number of OFDM symbols, which may constitute a number of subcarriers that may simultaneously be utilized for transmission over some defined period. Further, each frame may operate according to a symbol rate hopping mode, where one or more non-contiguous OFDM symbols are assigned to a user on a forward link or reverse link, or a

block hopping mode, where users hop within a block of OFDM symbols. The actual blocks or OFDM symbols may or may not hop between frames.

FIG. 4 illustrates communication between an access terminal 402 and an access network 404 using a communication link 406. The communication link may be implemented using communication protocols/standards such as World Interoperability for Microwave Access (WiMAX), infrared protocols such as Infrared Data Association (IrDA), short-range wireless protocols/technologies, Bluetooth® technology, Zig-Bee® protocol, ultra wide band (UWB) protocol, home radio frequency (HomeRF), shared wireless access protocol (SWAP), wideband technology such as a wireless Ethernet compatibility alliance (WECA), wireless fidelity alliance (Wi-Fi Alliance), 802.11 network technology, public switched telephone network technology, public heterogeneous communications network technology such as the Internet, private wireless communications network, land mobile radio network, code division multiple access (CDMA), wideband code division multiple access (WCDMA), universal mobile telecommunications system (UMTS), advanced mobile phone service (AMPS), time division multiple access (TDMA), frequency division multiple access (FDMA), orthogonal frequency division multiple (OFDM), orthogonal frequency division multiple access (OFDMA), orthogonal frequency division multiple FLASH (OFDM-FLASH), global system for mobile communications (GSM), single carrier (1X) radio transmission technology (RTT), evolution data only (EV-DO) technology, general packet radio service (GPRS), enhanced data GSM environment (EDGE), high speed downlink data packet access (HSPDA), analog and digital satellite systems, and any other technologies/protocols that may be used in at least one of a wireless communications network and a data communications network.

FIG. 5A illustrates a flow diagram of process 500, according to an embodiment. At 502, a forward link assignment block (FLAB) is received from a shared signaling medium access control (SS MAC) protocol. In an embodiment, at 504, determining if MAC ID of the FLAB is equal to the MAC ID of an access terminal. If so, in an embodiment, at 506, determining if a supplemental field of a FLAB is equal to '1'. In an embodiment at 508, a new access terminal assignment (ATA) is provided on an interlace by including union of hop-ports in the old ATA.

In another embodiment, at 510, the ATA is cleared and the hop-ports specified by a channel identity (ChID) in the FLAB are added to the ATA for the interlace. At 512, determining if a duplex mode is frequency division duplex (FDD). If so, at 514, determining if an extended transmission field of the FLAB is equal to '1'. In one embodiment, at 516, ATAs are expired except for an external transmission duration assignment ATA which does not overlap in the with a new assignment. In another embodiment, at 518, the extended transmission duration assignment ATAs are expired. At 520, hop-ports specified by the ChID in the FLAB are provided to the ATA in the corresponding interlace. Determining if a supplemental field of a FLAB is equal to '1' increases access terminal efficiency such that one or more of the aforementioned embodiments need not occur.

FIG. 5B illustrates a processor 550 for processing supplemental and non supplemental assignments. The processor referred to may be electronic devices and may comprise one or more processors configured for processing supplemental and non supplemental assignments. Processor 552 is configured to receive a forward link assignment block (LAB) from a shared signaling medium access control (SS MAC) protocol. In an embodiment, processor 554 is configured to deter-

mine if MAC ID of the FLAB is equal to the MAC ID of an access terminal. If so, in an embodiment, processor 556 is configured to determine if a supplemental field of a FLAB is equal to '1'. In an embodiment, processor 558 is configured to provide a new access terminal assignment (ATA) on an interlace by including union of hop-ports in the old ATA. In another embodiment processor 560 is configured to clear the ATA and add the hop-ports specified by a channel identity (ChID) in the FLAB to the ATA for the interlace, processor 562 is configured to determine if a duplex mode is frequency division duplex (FDD). If so, processor 564 is configured to determine if an extended transmission field of the FLAB is equal to '1'. In an embodiment, processor 566 is configured to expire the ATAs except for an external transmission duration assignment ATA which does not overlap in time with a new assignment. In another embodiment, processor 568 is configured to expire the extended transmission duration assignment ATAs. Processor 520 is configured to provide hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace. Determining if a supplemental field of a FLAB is equal to '1' increases processing efficiency such that one or more of the aforementioned embodiments need not occur. The functionality of the discrete processors 552 to 570 depicted in the figure may be combined into a single processor 572. A memory 574 is also coupled to the processor 572.

In an embodiment, an apparatus is described which comprises means for receiving a forward link assignment block (FLAB) from a shared signaling medium access control (SS MAC) protocol, means for determining if MAC ID of the FLAB is equal to the MAC ID of an access terminal and means for determining if a supplemental field of a FLAB is equal to '1'. The apparatus further comprises means for providing a new access terminal assignment (ATA) on an interlace by including union of hop-ports in the old ATA, means for clearing the ATA and adding the hop-ports specified by a channel identity (ChID) in the FLAB to the ATA for the interlace, means for determining if a duplex mode is frequency division duplex (FDD), means for determining if an extended transmission field of the FLAB is equal to '1' means for expiring the ATAs except for an external transmission duration assignment ATA which does not overlap in time with a new assignment, means for expiring the extended transmission duration assignment ATAs and means for providing hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace. The means described herein may comprise one or more processors.

Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, or any combination thereof. When implemented in software, firmware, middleware or microcode, the program code or code segments to perform the necessary tasks may be stored in a machine readable medium such as a separate storage(s) not shown. A processor may perform the necessary tasks. A code segment may represent a procedure, a function, a subprogram, a program, a routine, a subroutine, a module, a software package, a class, or any combination of instructions, data structures, or program statements. A code segment may be coupled to another code segment or a hardware circuit by passing and/or receiving information, data, arguments, parameters, or memory contents. Information, arguments, parameters, data, etc. may be passed forwarded, or transmitted via any suitable means including memory sharing, message passing, token passing, network transmission, etc.

Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments. Thus, the description is not intended to be limited to

the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

I claim:

1. A method of processing supplemental and non supplemental assignments of hop-ports for an access terminal in a wireless communication system, comprising:

receiving a forward link assignment block (FLAB) according to a shared signaling medium access control (SS MAC) protocol;

determining if a medium access control identity (MAC ID) of the FLAB is equal to a MAC ID of an access terminal;

clearing an access terminal assignment (ATA) on an interlace and adding hop-ports specified by a channel identity (ChID) in the FLAB to the ATA for the interlace;

determining if a duplex mode is a frequency division duplex (FDD);

determining if an extended transmission field of the FLAB is equal to 1;

expiring, based upon determining that the extended transmission field of the FLAB is equal to 1, the ATA except for an extended transmission duration assignment ATA which does not overlap in time with a new assignment.

2. The method of claim 1 further comprising:

expiring, based upon determining that the extended transmission field of the FLAB is not equal to 1, the extended transmission duration assignment ATA.

3. The method of claim 1 further comprising:

providing hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace, after expiring the ATA.

4. The method of claim 1 further comprising:

providing hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace, after expiring the extended transmission duration assignment ATA.

5. The method of claim 1, further comprising:

determining if a supplemental field of the FLAB is equal to 1; and

providing a new ATA on an interlace by including a union of hop-ports in an old ATA in response to determining the supplemental field of the FLAB is equal to 1.

6. The method of claim 5, further comprising:

replacing, in response to determining that the supplemental field of the FLAB is not equal to 1, the ATA with hop-ports specified by the ChID in the FLAB to the ATA for the interlace.

7. A non-transitory computer readable medium communicatively coupled to a processor, the medium including instructions stored thereon, wherein the instructions are executed by the processor, comprising:

a first set of instructions for receiving a forward link assignment block (FLAB) according to a shared signaling medium access control (SS MAC) protocol;

a second set of instructions for determining if a medium access control identity (MAC ID) of the FLAB is equal to a MAC ID of an access terminal;

a third set of instructions for clearing an access terminal assignment (ATA) on an interlace and adding hop-ports specified by a channel identity (ChID) in the FLAB to the ATA for the interlace;

a fourth set of instructions for determining if a duplex mode is a frequency division duplex (FDD);

a fifth set of instructions for determining if an extended transmission field of the FLAB is equal to 1;

a sixth set of instructions for expiring, based upon determining that the extended transmission field of the FLAB is equal to 1, the ATA except for an extended transmis-

sion duration assignment ATA which does not overlap in time with a new assignment.

8. The non-transitory computer readable medium of claim 7, further comprising:

a seventh set of instructions for determining if a supplemental field of the FLAB is equal to 1; and

an eighth set of instructions for replacing an ATA for the interlace with the hop-ports specified by the ChID in the FLAB to the ATA for the interlace, in response to determining that the supplemental field of the FLAB is not equal to 1.

9. The non-transitory computer-readable medium of claim 8, further comprising:

a ninth set of instructions providing a new ATA for the interlace by including a union of hop-ports in an old ATA in response to determining the supplemental field of the FLAB is equal to 1.

10. An apparatus operable in a wireless communication system, comprising:

at least one processor executing instructions comprising: receiving a forward link assignment block (FLAB) according to a shared signaling medium access control (SS MAC) protocol;

determining if a medium access control identity (MAC ID) of the FLAB is equal to a MAC ID of an access terminal; clearing an access terminal assignment (ATA) on an interlace and add hop-ports specified by a channel identity (ChID) in the FLAB to the ATA for the interlace;

determining if a duplex mode is frequency division duplex (FDD) after clearing the ATA and adding the hop ports; and

determining, based upon determining the duplex mode is a FDD, if an extended transmission field of the FLAB is equal to 1;

expiring, based upon determining that the extended transmission field of the FLAB is equal to 1, the ATA except for an extended transmission duration assignment ATA which does not overlap in time with a new assignment.

11. The apparatus of claim 10 the instructions further comprising:

expiring the extended transmission duration assignment ATA.

12. The apparatus of claim 11, the instructions further comprising:

providing hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace, after expiring the extended transmission duration assignment ATA.

13. The apparatus of claim 10 the instructions further comprising:

providing hop-ports specified by the ChID in the FLAB to the ATA in the corresponding interlace, after expiring the ATA.

14. The apparatus of claim 10; the instructions further comprising:

replacing the ATA with the hop-ports specified by the ChID in the FLAB to the ATA for the interlace.

15. The apparatus of claim 10, the instructions further comprising:

determining if a supplemental field of the FLAB is equal to 1; and

providing a new ATA on the interlace by including a union of hop-ports in an old ATA in response to determining the supplemental field of the FLAB is equal to 1.

16. A system for processing supplemental and non supplemental assignments of hop-ports in a wireless communication system, comprising:

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an access terminal further comprising:  
 a processor;  
 a non-transitory computer-readable storage medium  
 communicatively coupled to the processor and storing  
 computer executable components executed by the processor,  
 wherein the processor is configured to:  
 receive a forward link assignment block (FLAB) according  
 to a shared signaling medium access control (SS MAC)  
 protocol;  
 determine if a medium access control identity (MAC ID) of  
 the FLAB is equal to a MAC ID of an access terminal;  
 clear an access terminal assignment (ATA) on an interlace  
 and add hop-ports specified by a channel identity (ChID)  
 in the FLAB to the ATA for the interlace;  
 determine whether a duplex mode is a frequency division  
 duplex (FDD) after the ATA is cleared and the hop ports  
 added;  
 determine, based upon determining the duplex mode is a  
 FDD, if an extended transmission field of the FLAB is  
 equal to 1; and  
 expire, based upon the determination that the extended  
 transmission field of the FLAB is equal to 1, the ATA  
 except for an extended transmission duration assign-  
 ment ATA which does not overlap in time with a new  
 assignment.  
 17. The system of claim 16, the processor is further con-  
 figured to:

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expire, based upon the determination that the extended  
 transmission field of the FLAB is not equal to 1, the  
 extended transmission duration assignment ATA.  
 18. The system of claim 16, the processor is further con-  
 figured to:  
 provide hop-ports specified by the ChID in the FLAB to the  
 ATA in the corresponding interlace, after expiration of  
 the ATA.  
 19. The system of claim 16, the processor is further con-  
 figured to:  
 provide hop-ports specified by the ChID in the FLAB to the  
 ATA in the corresponding interlace, after expiration of  
 the extended transmission duration assignment ATA.  
 20. The system of claim 16, the processor is further con-  
 figured to determine if a supplemental field of the FLAB is  
 equal to 1.  
 21. The system of claim 20, the processor is further con-  
 figured to provide a new ATA on the interlace by including a  
 union of hop-ports in an old ATA in response to the determi-  
 nation that the supplemental field of the FLAB is equal to 1.  
 22. The system of claim 21, the processor is further con-  
 figured to replace, in response to the determination that the  
 supplemental field of the FLAB is not equal to 1, the ATA with  
 the hop-ports specified by the ChID in the FLAB to the ATA  
 for the interlace.

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