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(54) **SEMICONDUCTOR MEMORY DEVICE**

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This patent is subject to a terminal disclaimer.

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G11C 7/10 (2006.01)

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See application file for complete search history.

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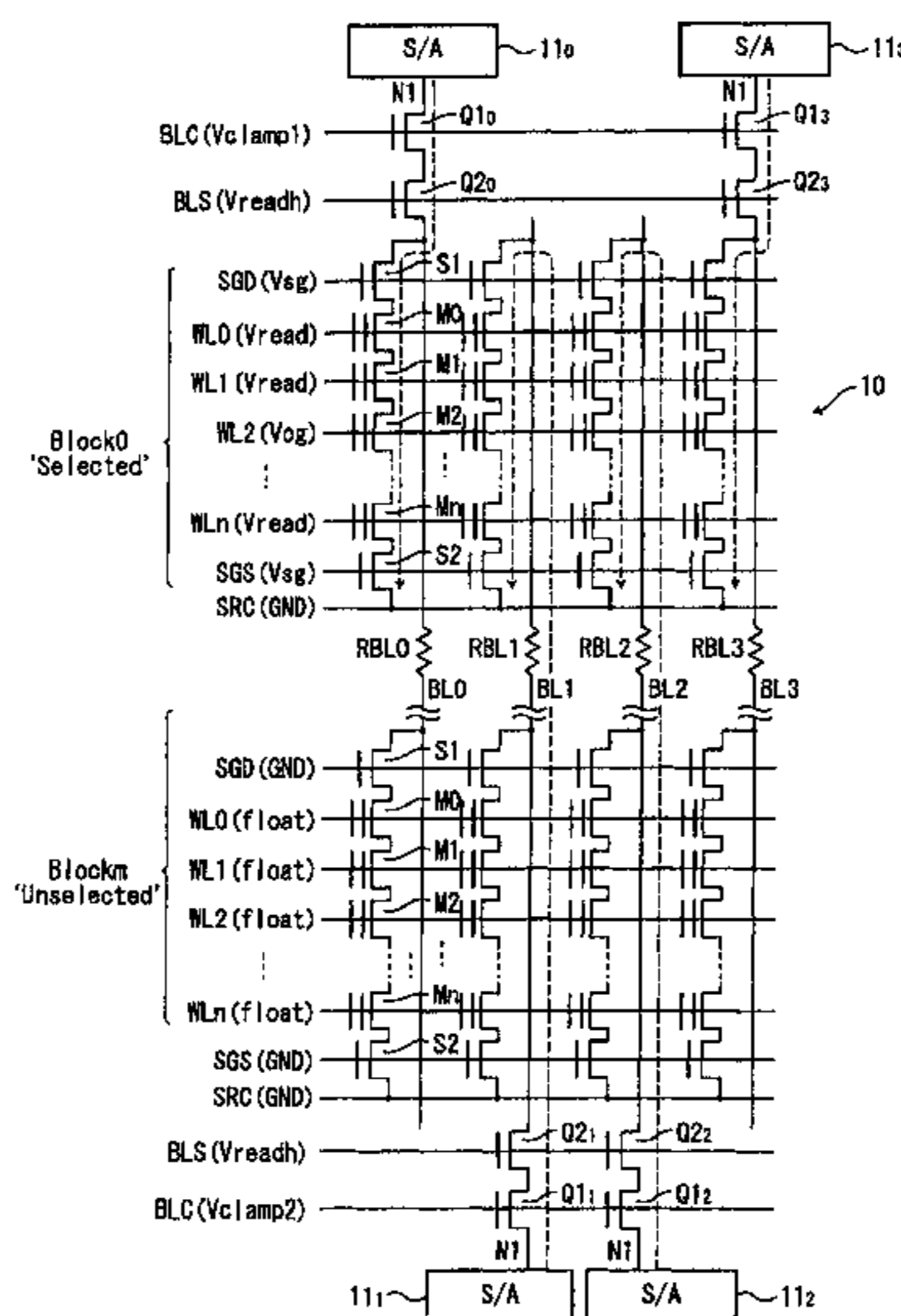
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(57) **ABSTRACT**

A semiconductor memory device comprising: a memory cell array having a plurality of memory cells that are arranged in a shape of a matrix along a plurality of bit lines arranged in parallel and a plurality of word lines intersecting orthogonally to the bit lines, and that have their data read out to the bit lines; a sense amplifier which detects a voltage or a current of the bit line, and which decides the read data from each of the memory cells; a clamping transistor which is connected between the sense amplifier and the bit lines, and which determines a voltage in a charging mode of the bit lines by a clamp voltage applied to a gate thereof; and a clamp voltage generation circuit which generates the clamp voltage so as to become larger as a distance from the sense amplifier to a selected one of the memory cells is longer.

11 Claims, 8 Drawing Sheets



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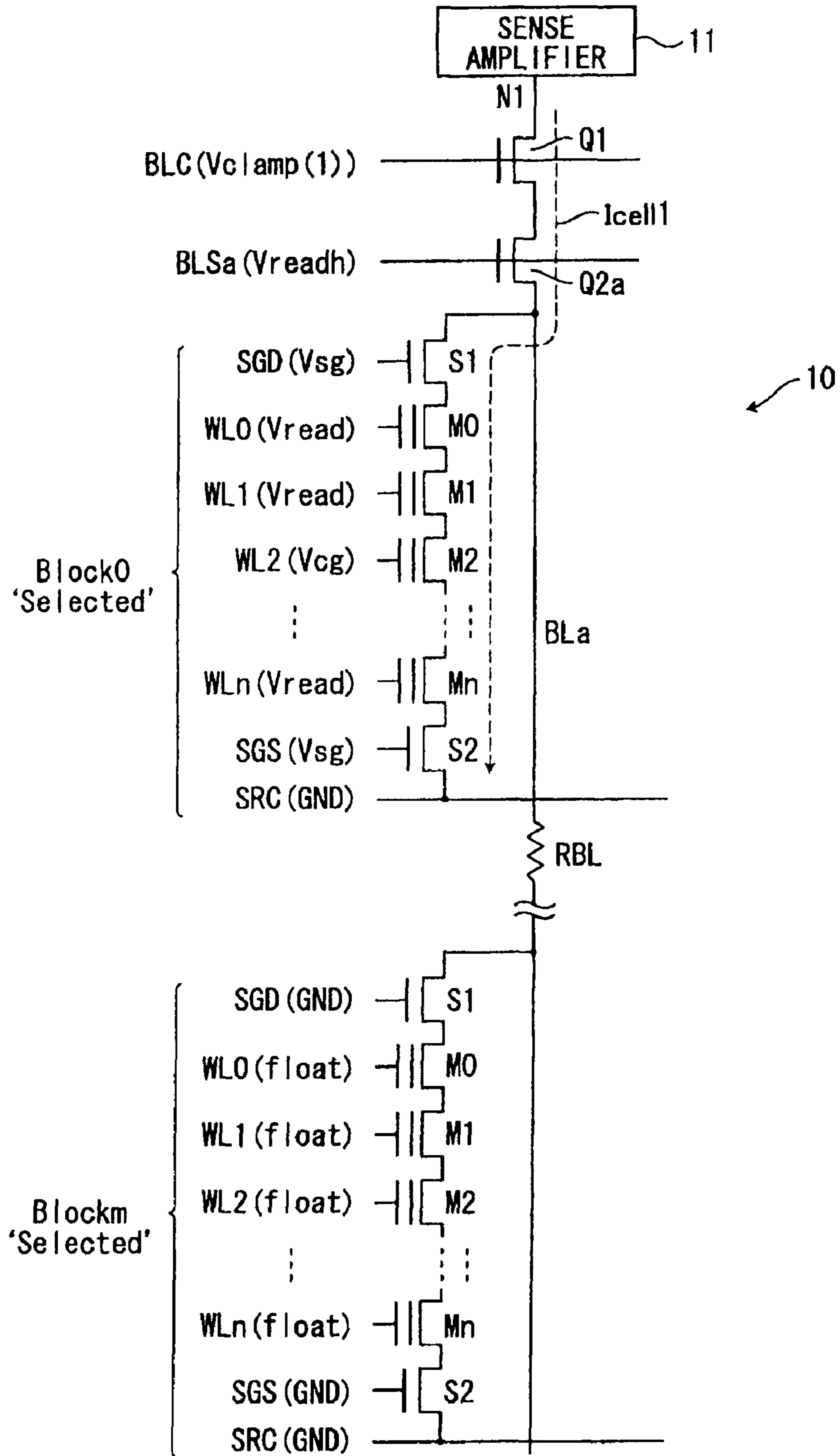


Fig.2

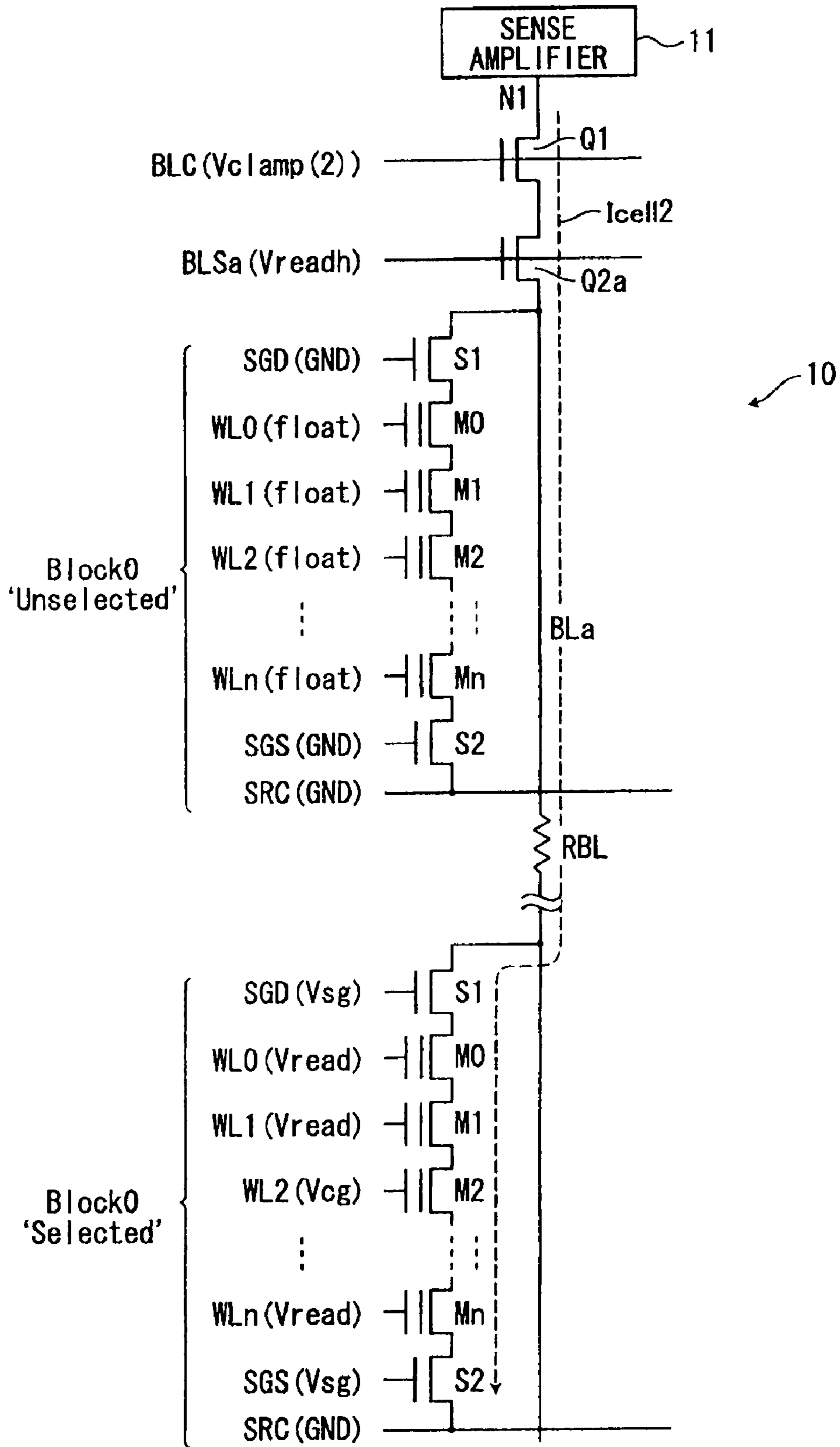


Fig.3

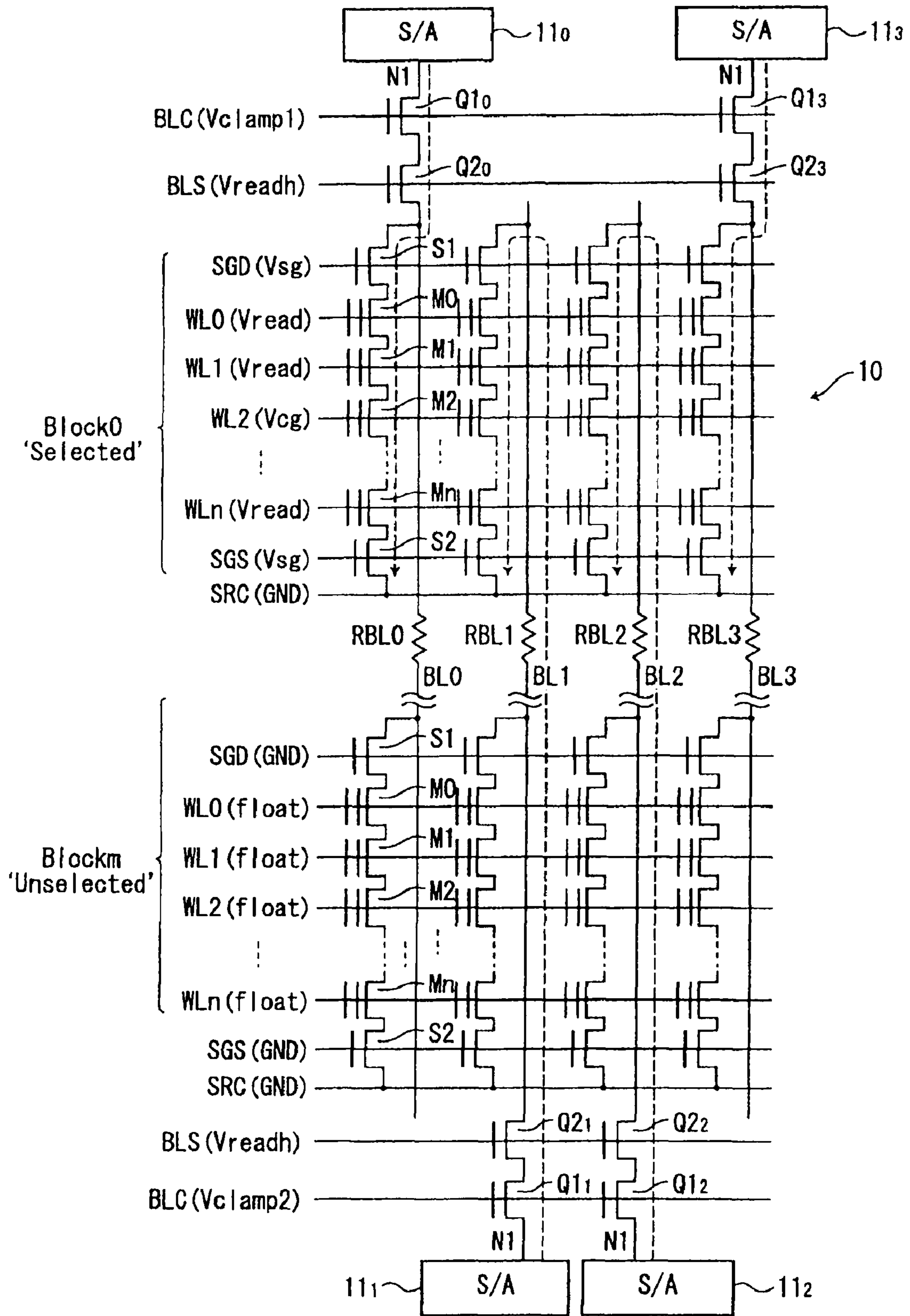


Fig.4

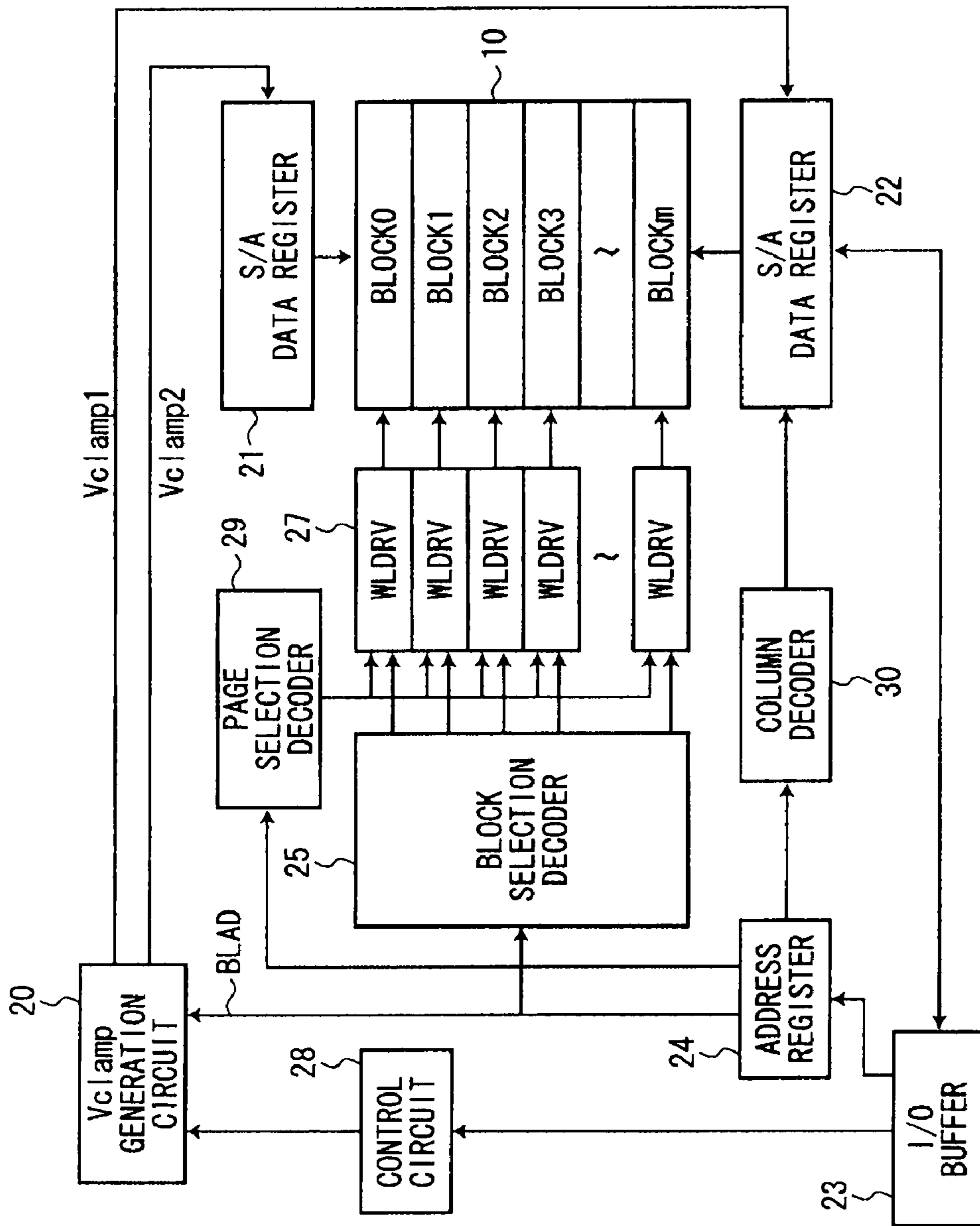


Fig.5

SELECTED BLOCK	AROW3	AROW2	AROW1	AROW0
Block0	1	1	1	1
Block1	1	1	1	0
Block2	1	1	0	1
Block3	1	1	0	0
Block4	1	0	1	1
Block5	1	0	1	0
Block6	1	0	0	1
Block7	1	0	0	0
Block8	0	1	1	1
Block9	0	1	1	0
Block10	0	1	0	1
Block11	0	1	0	0
Block12	0	0	1	1
Block13	0	0	1	0
Block14	0	0	0	1
Block15	0	0	0	0

Fig.7

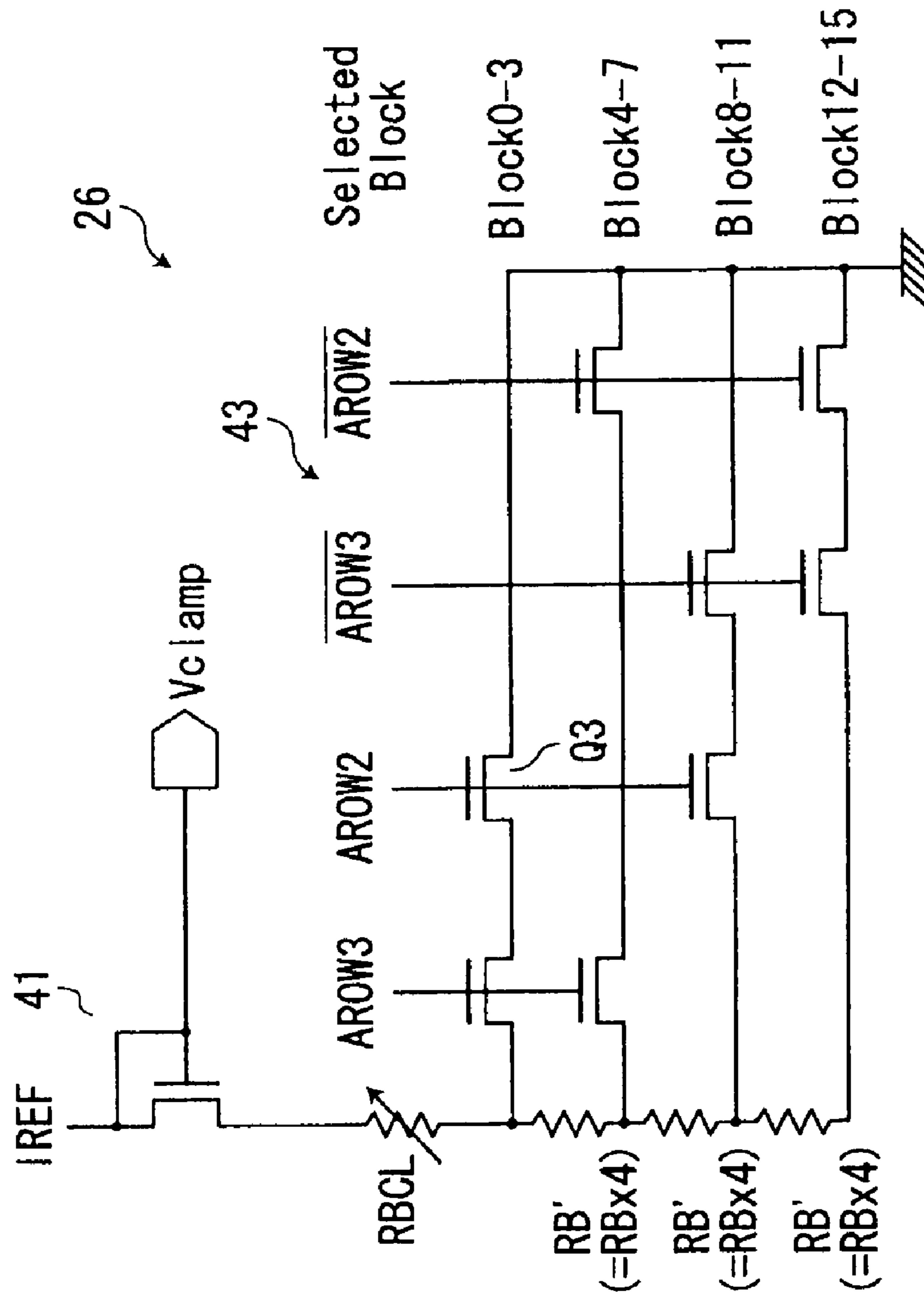


Fig.8

SEMICONDUCTOR MEMORY DEVICE**CROSS-REFERENCE TO RELATED APPLICATIONS**

This application is a continuation of and claims the benefit of priority under 35 U.S.C. §120 from U.S. Ser. No. 12/128,324 filed May 28, 2008, now U.S. Pat. No. 7,924,632 and claims the benefit of priority under 35 U.S.C. §119 from Japanese Patent Application No. P2007-141538 filed May 29, 2007, the entire contents of each of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor memory devices such as NAND cell, NOR cell, DINOR (Divided bit line NOR) cell and AND cell type EEPROMs, and more particularly to a semiconductor memory device in which a detection precision in a sense amplifier can be enhanced.

2. Description of the Related Art

The sense amplifier of a flash memory or the like semiconductor memory device decides the value of data basically by detecting the existence or nonexistence or the magnitude of a cell current which flows in accordance with the data of a memory cell. This sense amplifier is usually connected to bit lines (data lines) to which a large number of memory cells are connected, and the sensing schemes thereof are broadly classified into a voltage detection type and a current detection type.

With the voltage detection type sense amplifier, by way of example, the bit lines in states where they are separated from the memory cells are precharged to a predetermined voltage, the bit line is thereafter discharged by the selected memory cell, and the discharge state of the bit line is detected at a sense node joined to the bit line. In sensing the data, the bit line is separated from a current source load, and a bit-line voltage determined by the cell data is detected. This sense amplifier scheme is usually employed in a NAND type flash memory.

On the other hand, the current detection type sense amplifier senses the data by causing a read current to flow to the memory cell through the bit line. Also in this case, however, the bit-line voltage is determined by the cell data, and the data decision at the sense node joined to the bit line, finally detects the difference of the voltage based on the difference of the cell current.

In general, the voltage detection type sense amplifier and the current detection type sense amplifier have merits and demerits as stated below. The voltage detection type utilizes the charging and discharging of the bit lines, and hence, power consumption may be low. In a large-capacity memory of large bit-line capacitances, however, a long time is expended on the charging and discharging, and hence, high-speed sensing becomes difficult. Besides, the bit-line voltage is oscillated comparatively largely in accordance with the cell data, so that the noise between the adjacent bit lines becomes a problem.

On the other hand, the current detection type sense amplifier is capable of the high-speed sensing in such a way that the data is sensed while causing the read current to flow to the memory cell through the bit line. Besides, the amplitude of the bit-line voltage corresponding to the cell data can be suppressed to a small one by a clamping transistor (pre-sense amplifier) arranged between the bit line and the sense node, so that the noise between the bit lines is difficult to become problematic. In the current detection type sense amplifier,

however, the power consumption enlarges more than in the voltage detection type sense amplifier to the extent that the data is sensed while the current is kept flowing.

In the NAND type flash memory of the enlarged capacity, the voltage detection type sense amplifier has heretofore been extensively employed. However, in a case where the capacity of the memory is enlarged more, how the high-speed sensing is performed with the power consumption suppressed becomes an important problem to-be-solved. Further, when the microfabrication and capacity enlargement of the memory are advanced, the dispersion of currents attributed to the resistance values of the bit lines becomes a problem.

More specifically, in the NAND type flash memory, a read voltage V_{cg} which turns ON or OFF the selected cell in accordance with the content of the data is applied to the control gate of the selected cell from which the data is read out, among the plurality of NAND-connected memory cells. Also, a path voltage V_{read} which turns ON the other unselected cells irrespective of the contents of the data is applied to the control gates of the unselected cells. Thus, the content of the data of the selected cell is decided, depending upon if the current flows to the bit line through the memory cells. The voltage of the bit line is determined by a voltage V_{clamp} which is fed to the gate of the bit-line clamping transistor interposed between the sense amplifier and the bit line, and a voltage ($V_{clamp} - V_{thn}$) (where " V_{thn} " indicates the threshold voltage of the clamping transistor) is charged to the bit line. Since each cell operates in a linear region, the cell current tends to depend upon the drain-source voltage V_{ds} of the selected cell. The voltage of the drain side of the selected cell is determined by the voltage of the bit line, the resistance value of the bit line, and the resistance values of the unselected cells nearer to the bit line than the selected cell, within a memory cell array, while the voltage of the source side of the selected cell is determined by the float of a source line (SRC), and the resistance values of the unselected cells nearer to the source line SRC than the selected cell, within the memory cell array. In this regard, there has also been proposed a technique for decreasing the cell current in such a way that the path voltage V_{read} which is fed to the unselected cells between the selected cell and the source line is controlled in accordance with the number of the unselected cells.

When the microfabrication and capacity enlargement of the memory are further advanced in the future, it is expected that the resistance value of the bit line will increase more and more. When the resistance value of the bit line increases, a dispersion occurs in the voltage of the drain side of the selected cell between in a case where the memory cell nearer to the sense amplifier has been selected and in a case where the memory cell remoter from the sense amplifier has been selected, and the dispersion of the voltage incurs the dispersion of the cell current. That is, in the case where the selected cell is remoter from the sense amplifier, a voltage drop IR-DROP ascribable to the bit-line resistance appears, and the voltage V_{ds} of the selected cell decreases. As a result, the cell current becomes small. In the worst case, there is the problem that the read data will be erroneously decided.

BRIEF SUMMARY OF THE INVENTION

A semiconductor memory device comprising: a memory cell array which includes a plurality of memory cells that are arranged in a shape of a matrix along a plurality of bit lines arranged in parallel and a plurality of word lines intersecting orthogonally to the bit lines, and that have their data read out to the bit lines; a sense amplifier which detects a voltage or a current of the bit line, and which decides the read data from

each of the memory cells; a clamping transistor which is connected between the sense amplifier and the bit lines, and which determines a voltage in a charging mode of the bit lines by a clamp voltage applied to a gate thereof; and a clamp voltage generation circuit which generates the clamp voltage so as to become larger as a distance from the sense amplifier to a selected one of the memory cells is longer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a circuit diagram of the essential portions of a NAND type flash memory according to the first embodiment of the present invention;

FIG. 2 is a circuit diagram for explaining the operation of the memory;

FIG. 3 is a circuit diagram for explaining the operation of the memory;

FIG. 4 is a circuit diagram of the essential portions of a NAND type flash memory according to the second embodiment of the invention;

FIG. 5 is a block diagram showing the whole configuration of the memory of the second embodiment;

FIG. 6 is a circuit diagram of an example of a Vclamp generation circuit in the memory of the second embodiment;

FIG. 7 is a diagram showing the relations between addresses inputted to the Vclamp generation circuit and selected blocks; and

FIG. 8 is a circuit diagram of another example of the Vclamp generation circuit in the memory of the second embodiment.

DETAILED DESCRIPTION OF THE INVENTION

First Embodiment

FIG. 1 is a circuit diagram of the essential portions of a NAND type flash memory according to the first embodiment of the present invention. A memory cell array **10** is configured in such a way that bit lines BL are formed in a vertical line in the figure, while word lines WL are formed in a lateral direction, and that a plurality of NAND strings NS are arranged in the shape of a matrix along the bit lines BL and the word lines WL. Each of the NAND strings NS is configured including a memory cell array in which a plurality of memory cells M0-Mn are connected in series in such a shape that impurity regions (sources/drains) are shared by the adjacent ones of the memory cells, and a first selection gate transistor S1 and a second selection gate transistor S2 which are respectively connected at both the ends of the memory cell array. Each of the memory cells M0-Mn is made of a MOSFET in which a floating gate (charge accumulation layer) and a control gate (CG) are stacked through an insulating film on a semiconductor substrate serving as a channel region. The drain of the first selection gate transistor S1 is connected to the bit line BL extending in parallel with the arrayal direction of the memory cells M0-Mn, and the source of the second selection gate transistor S2 is connected to a source line SRC. The control gate of each of the memory cells M0-Mn constitutes the word line WL intersecting orthogonally to the bit line BL, and the gates of the selection gate transistors S1 and S2 constitute selection gates SGD and SGS intersecting orthogonally to the bit line BL. The plurality of NAND strings NS which are arranged in the shape of arrays in this manner, are grouped in such a manner that one block is formed by the NAND strings juxtaposed in the direction of the word lines WL. That is, the

memory cell array **10** is divided into m blocks (Block0-Blockm) in the direction of the bit lines BL.

A sense amplifier **11** detects the magnitude of a current flowing through the bit line BL to the selected memory cell Mi, from the voltage of a sense node N1, so as to decide the read data of the selected memory cell Mi. Either a current detection type or a voltage detection type may be employed as the sense amplifier **11**. In order to reduce bit-line capacitance coupling noise, the sense amplifier **11** is shared by the adjacent two bit lines BLa and BLb. The sense node N1 of the sense amplifier **11** is connected to the bit line BLa through a clamping transistor Q1 and a bit selection transistor Q2a which are connected in series, and it is connected to the bit line BLb through the clamping transistor Q1 and a bit selection transistor Q2b which are connected in series. The clamping transistor Q1 is a transistor which determines a potential in the charging mode of the bit lines BLa and BLb, and it affords a voltage which is obtained by subtracting the threshold voltage Vthn of the transistor Q1 from a clamp voltage Vclamp applied to its gate as a control signal BLC, to the end parts of the bit lines BLa and BLb on the sides of the sense amplifier **11**. A Vclamp generation circuit **12** generates the clamp voltage Vclamp on the basis of the address signal BLAD of the block in which the selected cell is included, and it feeds the generated voltage to the gate of the clamping transistor Q1 as the gate control signal BLC. The bit-line selection transistors Q2a and Q2b are respectively fed with voltages Vreadh and /Vreadh to their gates as bit-line selection signals BLSa and BLSb, so as to connect either of the bit lines BLa and BLb to the sense amplifier **11**.

Next, the operation of the data read mode of the NAND type flash memory thus configured will be explained with reference to FIGS. 2 and 3. Incidentally, FIGS. 2 and 3 show a state where the bit line BLa is selected by the bit-line selection transistor Q2a, and the bit line BLb and the NAND strings NS connected thereto are omitted from illustration.

FIG. 2 shows a case where the block Block0 nearest to the sense amplifier **11** is selected, and where data is read out from the memory cell M2 corresponding to the word line WL2 in the block Block0. In this case, a clamp voltage Vclamp(1) is applied as the gate control signal BLC of the clamping transistor Q1, and hence, the bit line BLa is charged up to a voltage (Vclamp(1)-Vthn).

In the case of reading out the data from the memory cell M2 within the selected block Block0, a read voltage Vcg (for example, 0 V) which becomes ON or OFF in accordance with the stored data is applied to the control gate of the selected memory cell M2, a read voltage Vread (for example, about 4 V) which becomes ON irrespective of stored data is applied to the control gates of the other memory cells M0, M1, M3, . . . , and Mn, and a voltage Vsg (for example, about 4 V) which becomes ON is applied to the gates of the selection transistors S1 and S2. The source line SRC is set at 0 V. Besides, the control gates of the memory cells M0-Mn of the unselected blocks (Block1-Blockm) are all brought into floating states, and the selection transistors S1 and S2 are brought into OFF states.

In a case where data "0" is written in the selected memory cell M2 of the selected block Block0, the memory cell M2 exhibits a threshold voltage higher than the voltage Vcg, and hence, this memory cell M2 keeps an OFF state, so that any current does not flow through the bit line BLa, or only a slight current flows therethrough. On the other hand, in a case where data "1" is written in the selected memory cell M2, the memory cell M2 exhibits a threshold voltage lower than the voltage Vcg, and hence, this memory cell M2 turns ON, so that a large current flows through the bit line BLa. Thus, the

potential of the sense node N1 lowers. Accordingly, the read data is discriminated to be "1" when the potential of the sense node N1 has lowered, and it is discriminated to be "0" when the potential of the sense node N1 has not lowered considerably.

Here, since the selected memory cell M2 operates in a linear region, a current I_{cell1} to flow through the selected memory cell M2 is determined by the drain-source voltage V_{ds} of the selected memory cell M2. The voltage of the drain side of the selected memory cell M2 is determined by the voltage of the bit line BL_a, the resistance value of the bit line BL_a, and the resistance values of the unselected cells M0 and M1 nearer to the bit line BL_a than the selected memory cell M2, within the NAND string NS, while the voltage of the source side of the selected memory cell M2 is determined by the float of the source line (SRC), and the resistance values of the unselected memory cells M3-M_n nearer to the source line SRC than the selected memory cell M2, within the NAND string NS. In the case of the example in FIG. 2, the block Block0 nearest from the sense amplifier 11 is selected, and hence, a voltage drop IR-DROP hardly appears due to the resistance value in the bit line BL_a. Accordingly, the drain-source voltage V_{ds} of the selected memory cell M2 becomes a sufficiently large value. In this case, the clamp voltage $V_{clamp}(1)$ may be determined so as to limit the current value I_{cell1} in consideration of power consumption.

On the other hand, FIG. 3 shows a case where the block Block_m remotest from the sense amplifier 11 is selected, and where data is read out from the memory cell M2 corresponding to the word line WL2 within the block Block_m. In this case, a clamp voltage $V_{clamp}(2)$ is applied as the gate control signal BLC of the clamping transistor Q1, and hence, the bit line BL_a is charged up to a voltage ($V_{clamp}(2) - V_{thn}$). Incidentally, $V_{clamp}(2) > V_{clamp}(1)$ holds here.

The operation of reading out the data of the selected memory cell M2 is the same as in the above. In the case of the example in FIG. 3, the block Block_m remotest from the sense amplifier 11 is selected, and hence, the resistance value RBL of the bit line BL_a becomes the maximum. In this case, the clamp voltage $V_{clamp}(2)$ is determined so that a sufficient bit-line current I_{cell2} which does not develop erroneous read may be caused to flow. As a result, the relation of $V_{clamp}(2) > V_{clamp}(1)$ holds.

According to this embodiment, the dispersion of that current value of the bit line which depends upon the position of the selected block can be suppressed, and the reduction of the power consumption and the prevention of the erroneous read can be attained.

Second Embodiment

FIG. 4 is a circuit diagram of the essential portions of a NAND type flash memory according to the second embodiment of the invention. In this embodiment, sense amplifiers 11₀ and 11₃ and sense amplifiers 11₁ and 11₂ are respectively arranged on both sides in the direction of the bit lines BL of a memory cell array 10. More specifically, the sense amplifiers 11₀, 11₁, . . . are alternately arranged on the upper end sides and lower end sides of the bit lines BL₀, BL₁, . . . as seen in the figure, every second bit line. By the way, in actuality, one sense amplifier 11 is shared by the two bit lines BL, but one of the two paired bit lines and a NAND string NU joined thereto are omitted from illustration for the brevity of explanation.

In this embodiment, clamping transistors Q1₀, Q1₃, . . . which are respectively connected between the sense amplifiers 11₀, 11₃, . . . on the upper end sides of the bit lines BL and the bit lines BL₀, BL₃, . . . are fed with a clamp voltage

V_{clamp1} as a gate control signal BLC, while clamping transistors Q1₁, Q1₂, . . . which are respectively connected between the sense amplifiers 11₁, 11₂, . . . on the lower end sides of the bit lines BL and the bit lines BL₁, BL₂, . . . are fed with a clamp voltage V_{clamp2} as a gate control signal BLC.

According to this embodiment, in a case, for example, where data is readout from the memory cell M2 of a block Block0, the block Block0 is at the shortest distance from the sense amplifiers 11₀, 11₃, . . . and at the longest distance from the sense amplifiers 11₁, 11₂, . . . , and hence, the clamp voltages are set at $V_{clamp1} < V_{clamp2}$. Besides, in a case where a block (m/2) located at the middle position between the upper and lower ends of the bit lines BL has been selected, the clamp voltages are set at $V_{clamp1} = V_{clamp2}$, and in a case where a block Block_m located in the vicinity of the lower ends of the bit lines BL has been selected, the clamp voltages are set at $V_{clamp1} > V_{clamp2}$.

Thus, the dispersion of a bit-line current value which depends upon the position of the selected block can be suppressed, and the reduction of power consumption and the prevention of erroneous read can be attained. FIG. 5 is a block diagram showing the whole configuration of the NAND type flash memory according to this embodiment. Sense amplifier/data register circuits 21 and 22 are respectively arranged on both sides in the direction of the bit lines of the memory cell array 10 consisting of the blocks Block0-Block_m. The sense amplifier/data register circuits 21 and 22 include the sense amplifiers 11, the clamping transistors Q1, bit-line selection transistors Q2, and data registers. These sense amplifier/data register circuits 21 and 22 exchange data with the exterior of the flash memory through an I/O buffer 23. That address signal of the memory which is fed from the exterior is stored in an address register 24 through the I/O buffer 23. In the address signal stored in the address register 24, a block address signal BLAD consisting of high-order bits is fed to a block selection decoder 25 and also to a V_{clamp} generation circuit 26. The block selection decoder 25 decodes the fed block address signal BLAD, so as to activate one of m word line drivers 27. The V_{clamp} generation circuit 26 generates the clamp voltages V_{clamp1} and V_{clamp2} corresponding to the block address signal BLAD, on the basis of a control signal fed from a control circuit 28, and it feeds the generated clamp voltages to the clamping transistors to the sense amplifier/data register circuits 21 and 22. In the address signal stored in the address register 24, a further high-order address signal in a low-order address signal is fed to a page selection decoder 29, and the lower-order address signal is fed to a column decoder 30. The page selection decoder 29 activates one of the word lines WL of n memory cells M0-M_n within one block. Besides, the column decoder 30 selects the bit line BL to-be-accessed in accordance with the low-order address signal.

FIG. 6 shows a configurational example of the V_{clamp} generation circuit. This example is an example in which sixteen blocks Block0-Block15 are connected to one bit line BL. Besides, FIG. 6 shows only a portion for generating the clamp voltage V_{clamp1} in FIG. 5, and the clamp voltage V_{clamp1} is expressed as " V_{clamp} ".

A constant-voltage circuit 41 formed of a transistor which has its gate and its drain connected and which causes a constant current IREF to flow, outputs the gate voltage thereof as the clamp voltage V_{clamp} . The constant-voltage circuit 41, a variable resistor RBCL, and fifteen resistors RB are connected in series. The fifteen resistors RB have the same resistances, respectively. A switch circuit 42 in which a plurality of transistors Q3 are connected in the shape of a matrix, is connected to the connection ends of the respective resistors

RB and both the ends of a resistor array. The switch circuit **42** is fed with 4-bit high-order row address signals AROW0-AROW3 and /AROW0-/AROW3 as the block address signal BLAD, and it grounds any of the connection ends of the resistors RB in accordance with the high-order row address signals AROW0-AROW3 and /AROW0-/AROW3.

As shown in FIG. 7 by way of example, in a case where the block Block0 nearest to the sense amplifier/data register circuit **21** has been selected, "1111" is inputted as the high-order row addresses AROW0-AROW3, so that the four transistors Q3 at the uppermost stage of the switch circuit **42** are simultaneously brought into ON states, and a voltage corresponding to $(IREF \times RBCL)$ is outputted as the clamp voltage Vclamp. This is an example in which the lowest voltage is generated as the clamp voltage Vclamp. On the other hand, in a case where the block Block15 remotest from the sense amplifier/data register circuit **21** has been selected, "0000" is inputted as the high-order row addresses AROW0-AROW3, so that the four transistors Q3 at the lowermost stage of the switch circuit **42** are simultaneously brought into ON states, and a voltage corresponding to $(IREF \times RBCL + 15 \times RB)$ is outputted as the clamp voltage Vclamp. This is an example in which the highest voltage is generated as the clamp voltage Vclamp. Incidentally, a circuit for generating the clamp voltage Vclamp2 is quite opposite in logic, and it is so configured that the clamp voltage which is generated when the block Block0 has been selected becomes the highest value, whereas the clamp voltage which is generated when the block Block15 has been selected becomes the lowest value.

According to this embodiment, the different values of the clamp voltage Vclamp are respectively allotted to the sixteen blocks, and hence, the current values of the bit lines BL can be finely controlled.

However, in a case where such a fine current control is unnecessary, a simple Vclamp generation circuit **26** can be configured as shown in FIG. 8 by way of example. In this example, a switch **43** is fed with 2-bit high-order row addresses AROW2 and AROW3, and the clamp voltage Vclamp is switched in four stages in the cases where the blocks Block0-Block3, Block4-Block7, Block8-Block 11, and Block12-Block15 have been selected. Each resistor RB' for use has a resistance value which is four times as large as the resistance value of each resistor RB in the circuit shown in FIG. 6.

This embodiment has the advantage that it can be configured of the simple circuit, though it is inferior to the preceding embodiment in a controllability for canceling the resistance components of the bit lines BL.

Incidentally, in the foregoing embodiments, the clamp voltage Vclamp is linearly changed on the basis of the block addresses, but it can also be nonlinearly changed. In this case, the respective resistance values of resistors for use may be made different, or how to select the resistors by a switch circuit may be made nonlinear.

The sense amplifier for use in each of the embodiments may be either a current detection type or a voltage detection type, but the use of the sense amplifier of the current control type is more advantageous for the reason that a current control is possible.

Besides, although the NAND type flash memory has been exemplified in each of the embodiments, the invention is not restricted to the NAND type flash memory, but it is also

applicable to semiconductor memory devices such as NOR type, DINOR (Divided bit line NOR) type and AND type EEPROMs.

What is claimed is:

1. A semiconductor memory device comprising:
a memory cell array having a plurality of memory cells that are arranged in a shape of a matrix along a plurality of bit lines arranged in parallel and a plurality of word lines intersecting orthogonally to the bit lines;

a sense amplifier;

a clamping transistor connected between the sense amplifier and the bit lines and a clamp voltage applied to a gate thereof;

a clamp voltage generation circuit generating the clamp voltage; and

wherein the memory cell array is divided into a plurality of blocks in a direction in which the bit lines extend, and the clamp voltage generation circuit determines the clamp voltage on the basis of an address of the block to which the selected memory cell belongs.

2. The semiconductor memory device according to claim 1, wherein the clamp voltage generation circuit generating the clamp voltage so as to become larger as a distance from the sense amplifier to a selected one of the memory cells is longer.

3. The semiconductor memory device according to claim 2, wherein such sense amplifiers and such clamping transistors are distributively arranged in halves, on both sides of the memory cell array in the extending direction of the bit lines.

4. The semiconductor memory device according to claim 3, wherein the clamp voltage generation circuit feeds a first clamp voltage to the clamping transistor on one side of the memory cell array, and it feeds a second clamp voltage to the clamping transistor on another side of the memory cell array.

5. The semiconductor memory device according to claim 1, wherein the clamp voltage generation circuit has a constant-voltage circuit and a plurality of resistors connected in series and a switch circuit.

6. The semiconductor memory device according to claim 5, wherein the switch circuit has a plurality of transistors, and a gate of the plurality of transistors is input a part of the address of the block.

7. The semiconductor memory device according to claim 5, wherein the clamp voltage generation circuit decides an end of a resistor in the plurality of resistors applied to grand voltage according to the address of the block.

8. The semiconductor memory device according to claim 6, wherein the clamp voltage generation circuit decides an end of a resistor in the plurality of resistors applied to grand voltage according to the address of the block.

9. The semiconductor memory device according to claim 6, wherein the part of the address of the block is high-order row address.

10. The semiconductor memory device according to claim 5, wherein the switch circuit has a plurality of transistors connecting to an one end of the plurality of resistors, and a number of the plurality of transistors is equal to a number of a bit of the address of the block.

11. The semiconductor memory device according to claim 5, wherein the switch circuit has a plurality of transistors connecting to an one end of the plurality of resistors, and a number of the plurality of transistors is less than a number of a bit of the address of the block.