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Kim

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(54) **METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE WITH A SUBSTRATE PROTRUSION**

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H01L 21/8238 (2006.01)

(52) **U.S. Cl.** **438/221**; 257/E21.54; 438/301

(58) **Field of Classification Search** 257/401, 257/E21.54, E21.663; 438/221, 214
See application file for complete search history.

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(57) **ABSTRACT**

A semiconductor device includes a substrate having an active region and an isolation region, a gate pattern crossing both the active region and the isolation region of the substrate, and a protrusion having a surface higher than that of the substrate over at least an edge of the active region contacting a portion of the isolation region under the gate pattern.

16 Claims, 5 Drawing Sheets

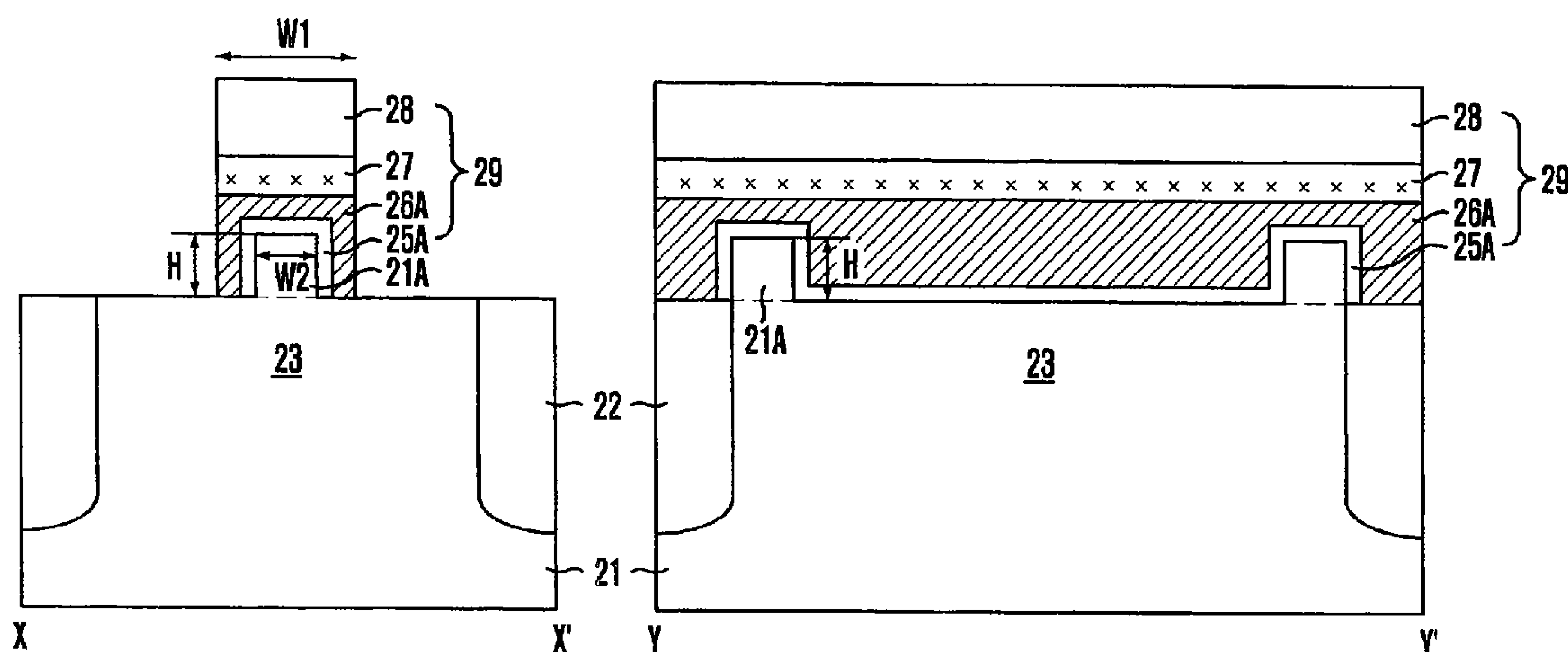


FIG. 1
(RELATED ART)

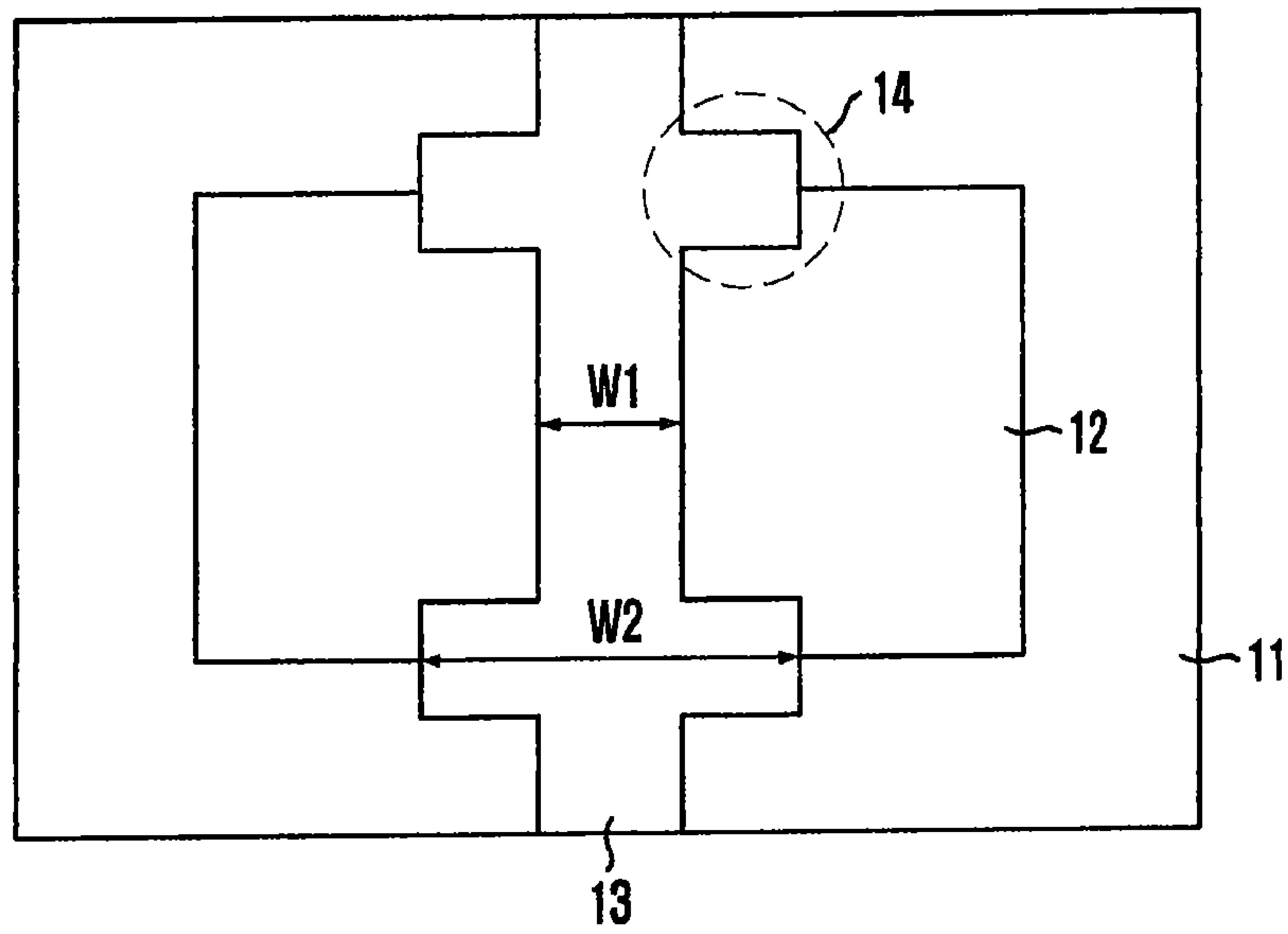
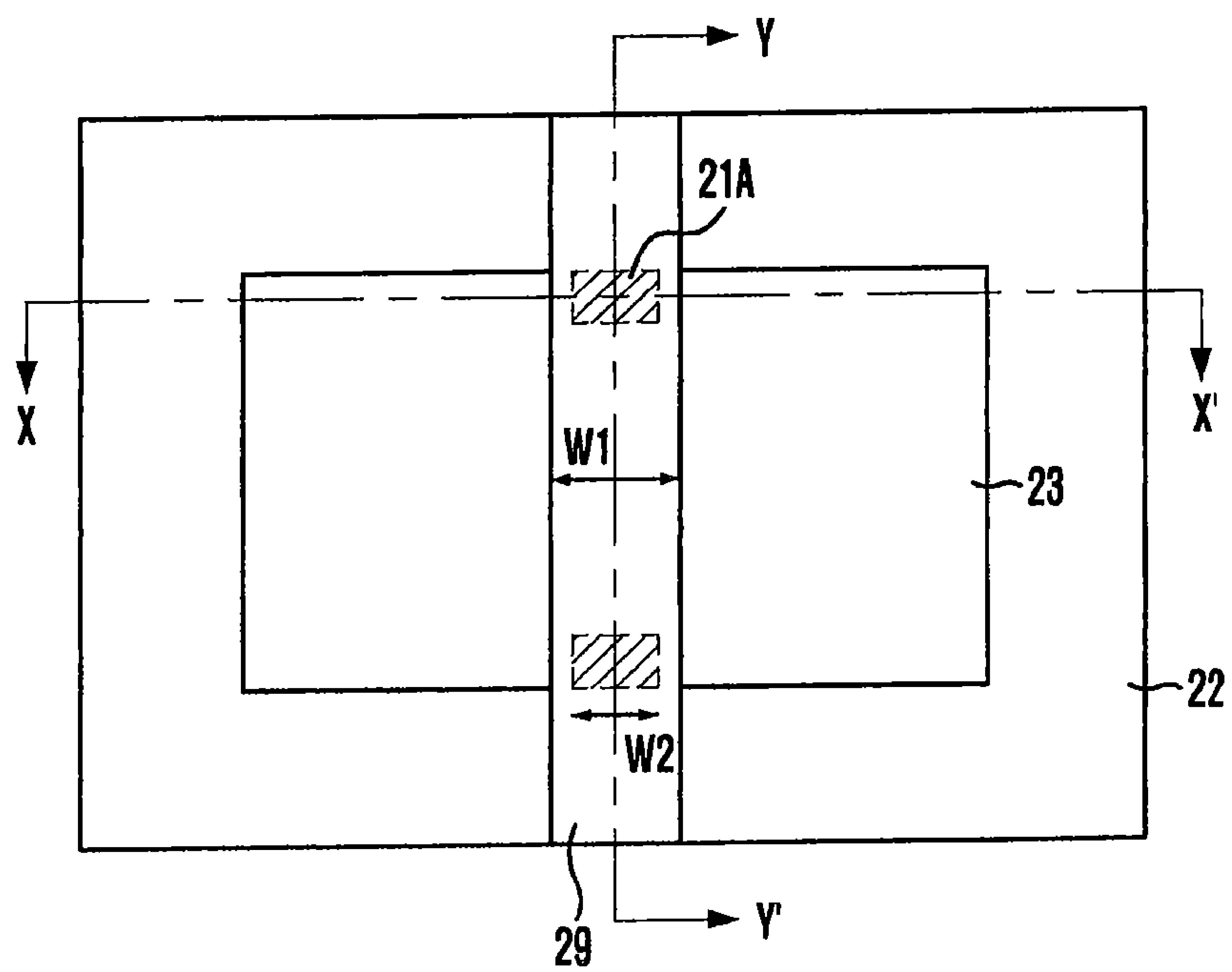


FIG. 2A



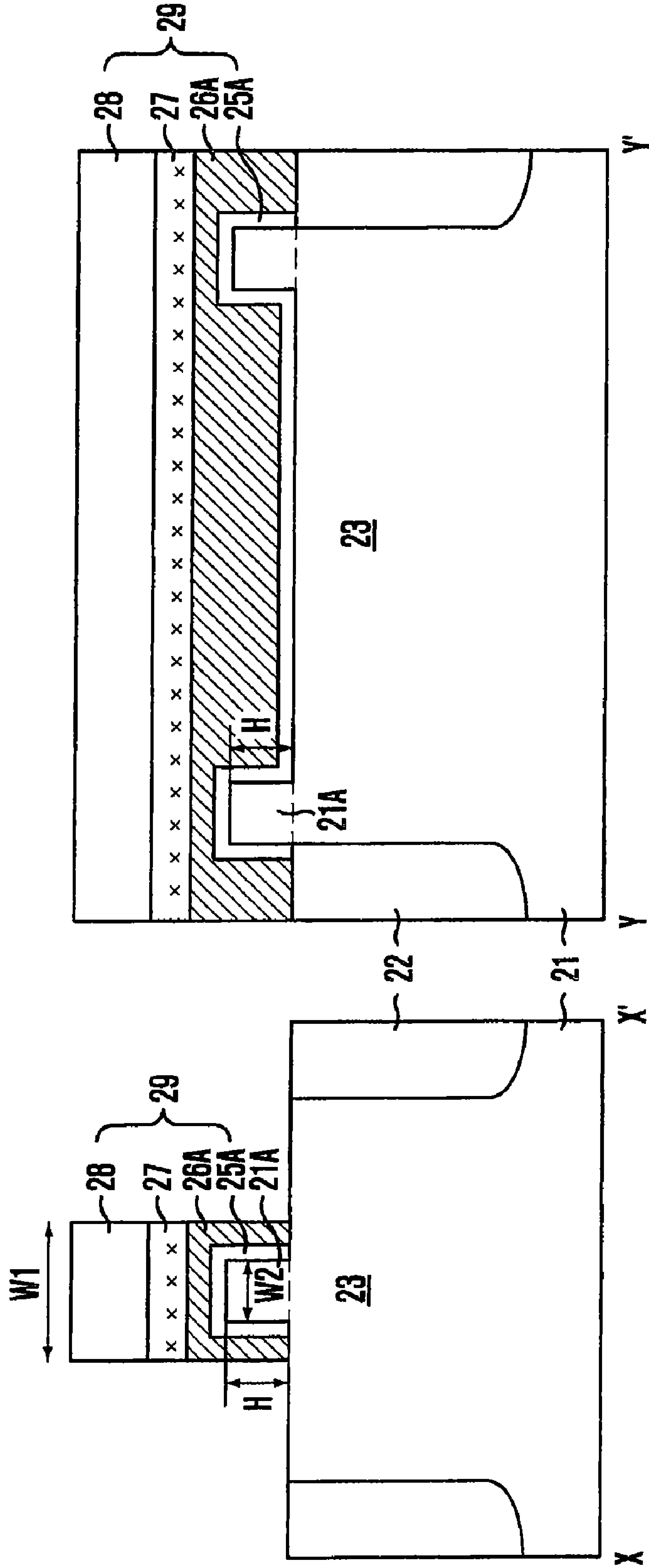


FIG. 2B

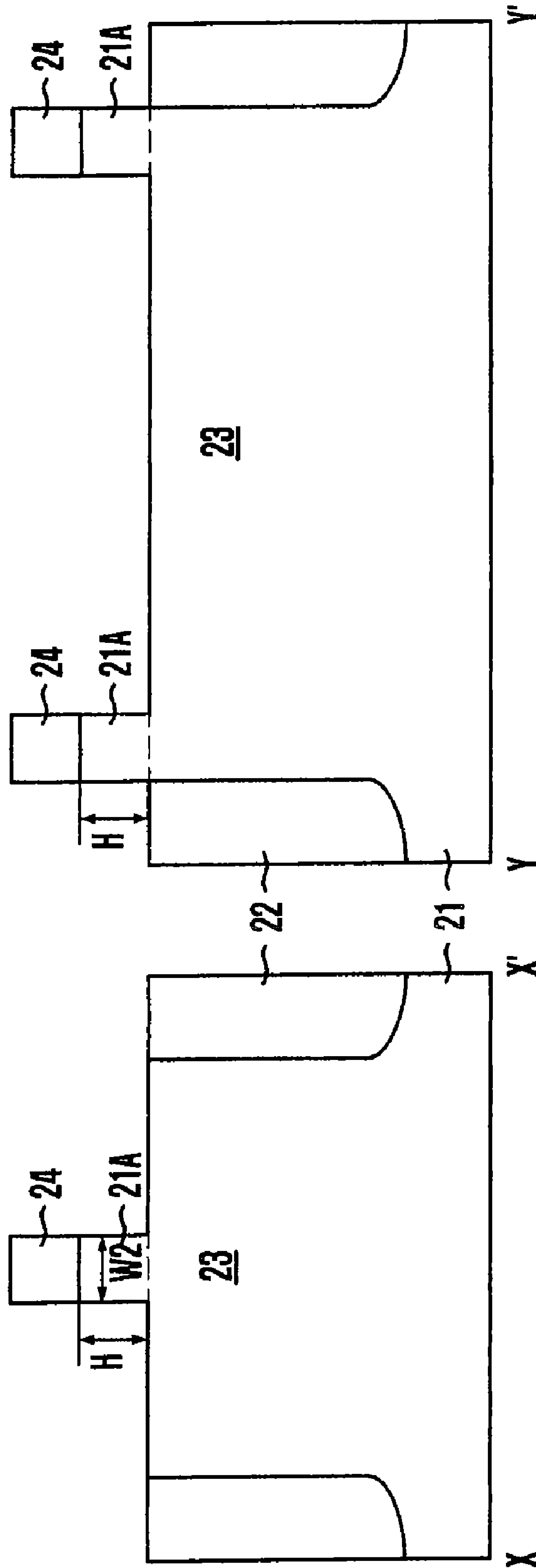


FIG. 3A

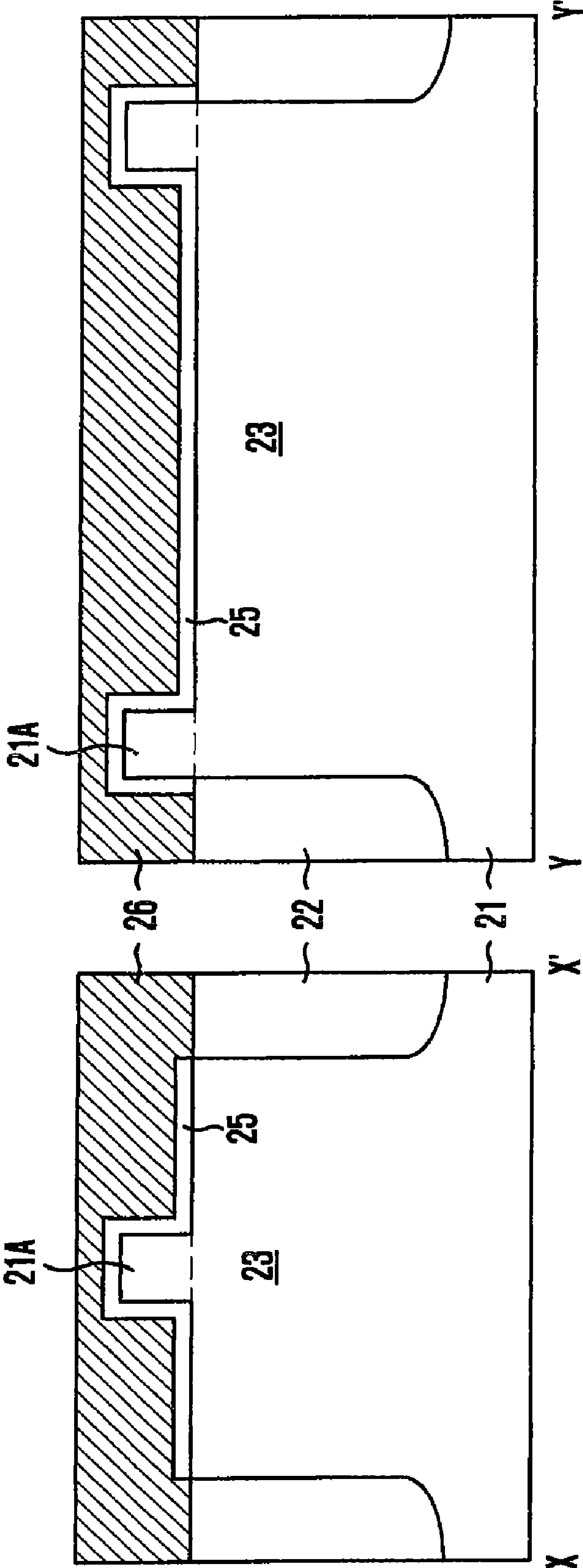
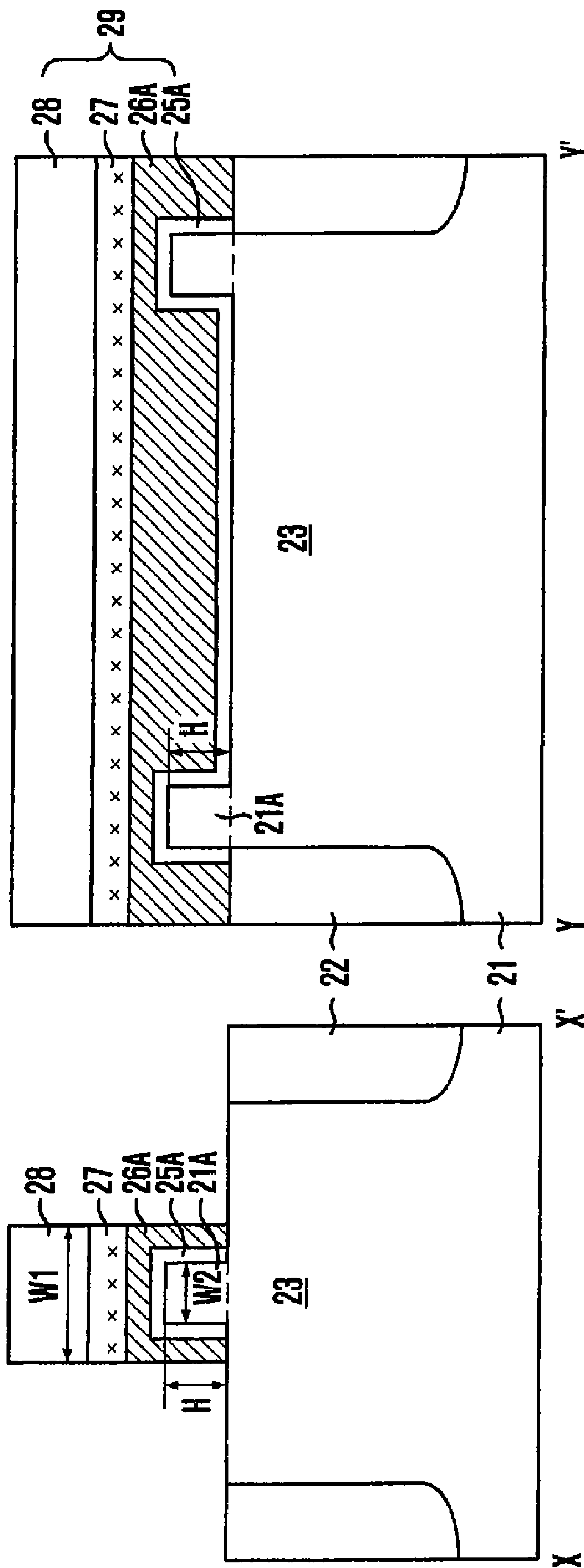


FIG. 3B

FIG.3C



METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE WITH A SUBSTRATE PROTRUSION

CROSS-REFERENCE TO RELATED APPLICATIONS

The present invention claims priority of Korean patent application number 10-2007-0100723, filed on Oct. 8, 2007, which is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a fabricating method thereof, and more particularly, to a semiconductor device that may relieve hot electron induced punchthrough phenomenon even without using a gate tab, and a fabricating method thereof.

Recently, as a design rule of a semiconductor device shrinks to 100 nm or less, an interval between the source and the drain of a transistor narrows and the doping concentrations of the channel, source, and drain increase. Therefore, a phenomena such as a short channel effect (SCE), a hot carrier effect (HCE), and a gate induced drain leakage (GIDL) occur to reduce the electrical characteristics of a transistor.

Particularly, in the case of a positive metal oxide semiconductor (PMOS) transistor formed in a peripheral region, electrons are additionally generated by holes, which are majority carriers. These electrons are trapped into an isolation layer adjacent to an inversion channel of the PMOS transistor, leading to reduction of an effective channel length. The channel inversion caused by trapping of electrons is generated at the edge of an active region contacting a portion of the isolation layer under a gate pattern.

As described above, the undesired channel inversion in the PMOS transistor increases a leakage current during a turn-off operation to increase power consumption, reducing an operating speed, and reducing a breakdown voltage (BV). A phenomenon generating these limitations is generally called a hot electron induced punchthrough (HEIP) phenomenon.

To solve the limitations caused by the HEIP, a technology has been proposed which installs a gate tap at a point where HEIP phenomenon is induced, that is, a boundary region between an active region and an isolation region that overlaps a gate pattern in an aspect of the structure of a semiconductor device.

FIG. **1** illustrates a plan view of a typical semiconductor device having a gate tap.

Referring to FIG. **1**, a gate tap **14** is formed at a gate electrode **13** located at the edge of an active region **12** to increase the length of this portion of the gate electrode **13**. Therefore, the length W**2** of a channel formed at the edge of the active region **12** contacting an isolation region **11** becomes longer than the length W**1** of the channel formed at the active region **12**, so that the HEIP phenomenon may be relieved.

However, as a channel length reduces as a semiconductor device becomes highly integrated, the length of the gate tap **14** needs to be increased to compensate for the reduced channel length. In this case, the active region **12** needs to be increased to maintain a constant interval between gate electrodes **13** in a region where transistors requiring the gate tap **14** are densely aggregated. This increases a net die size of a semiconductor device. Accordingly, it is difficult to improve the degree of integration of a semiconductor device. Also, when the degree of integration increases, the characteristic of a transistor is difficult to secure.

SUMMARY OF THE INVENTION

Embodiments of the present invention relate to a semiconductor device that may prevent an HEIP phenomenon without using a gate tap, and a fabricating method thereof.

In accordance with an aspect of the present invention, there is provided a semiconductor device. The semiconductor device includes a substrate having an active region and an isolation region, a gate pattern crossing both the active region and the isolation region of the substrate, and a protrusion having a surface higher than that of the substrate over at least an edge of the active region contacting a portion of the isolation region under the gate pattern.

In accordance with another aspect of the present invention, there is provided a method for fabricating a semiconductor device. The method includes forming hard mask patterns over a substrate including an active region and an isolation region, etching the substrate using the hard mask patterns as an etch barrier (or etch mask) to form a protrusion having a higher surface than that of the substrate, forming a gate insulation layer over the substrate including the protrusion, forming a gate conductive layer and a gate hard mask layer over the gate insulation layer, and forming a gate pattern overlapping the protrusion by selectively etching the gate hard mask layer, the gate conductive layer, and the gate insulation layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a plan view of a typical semiconductor device having a gate tap.

FIG. **2**A illustrates a plan view of a semiconductor device in accordance with an embodiment of the present invention.

FIG. **2**B illustrates a cross-sectional view of a semiconductor device in accordance with an embodiment of the present invention, taken along the line X-X' and the line Y-Y' of FIG. **2**A.

FIGS. **3**A to **3**C illustrate a method for fabricating a semiconductor device in accordance with an embodiment of the present invention, taken along the lines X-X' and Y-Y' of FIG. **2**A.

DESCRIPTION OF SPECIFIC EMBODIMENTS

Hereinafter, a semiconductor device and a method for fabricating the same in accordance with the present invention will be described in detail with reference to the accompanying drawings.

FIG. **2**A illustrates a plan view of a semiconductor device in accordance with an embodiment of the present invention, and FIG. **2**B illustrates a cross-sectional view of a semiconductor device in accordance with an embodiment of the present invention, taken along the line X-X' and the line Y-Y' of FIG. **2**A.

Referring to FIGS. **2**A and **2**B, the semiconductor device includes a gate pattern **29** crossing an active region **23** and an isolation region **22** with both over a substrate **21**. It also includes a protrusion **21**A having a surface higher than that of the substrate **21** in at least an edge of the active region **23** and contacting a portion of the isolation region **22** under the gate pattern **29**.

The protrusion **21**A may be a portion of the substrate **21** corresponding to the edge of the active region **23** contacting the isolation region **22**, or a portion of the substrate **21** corresponding to a boundary between the isolation region **22** and

the active region **23**. The protrusion **21**A may have a three-dimensional structure, that is, a cube shape or a rectangular parallelepiped shape.

The width W**2** of the protrusion **21**A may be formed smaller than the width W**1** of the gate pattern **29** so that the gate pattern **29** may include the protrusion **21**A. The height H of the protrusion **21**A may be formed greater than the width W**1** of the gate pattern **29** to increase a channel length at the edge of the active region **23** contacting the isolation region **22** under the gate pattern **29**.

The channel length at the edge of the active region **23** contacting a portion of the isolation region **22** under the gate pattern **29** is described in more detail below.

The channel length of the gate pattern **29** formed in the central portion of the active region **23** is the same as the width W**1** of the gate pattern **29**. A channel length at the boundary between the active region **23** and the isolation region **22** where a hot electron induced punch through (HEIP) phenomenon occurs is formed along the surface of the protrusion **21**A, so that the channel length is a value obtained by adding the height H of the protrusion **21**A two times to the width W**2** of the protrusion **21**A. Therefore, since the channel length at the edge of the active region **23** is longer than the channel length at the central portion of the active region **23**, a reduced effective channel length due to an HEIP phenomenon at the edge of the active region **23** contacting a portion of the isolation region **22** under the gate pattern **29** is compensated for.

The gate pattern **29** may include a gate insulation layer pattern **25**A covering the surface of the protrusion **21**A, a gate electrode formed over the gate insulation layer pattern **25**A, and a gate hard mask layer **28** formed over the gate electrode. At this point, the gate insulation layer pattern **25**A may be a silicon oxide layer.

The gate electrode may be formed in a structure in which a first gate conductive layer **26**A and a second gate conductive layer **27** are stacked. Each of the first gate conductive layer **26**A and the second gate conductive layer **27** may be one of a polysilicon layer, a metal layer (e.g., a Ti layer and a W layer), a conductive metal nitride layer (e.g., a TiN layer), a metal silicide layer (e.g., a titanium silicide layer and a tungsten silicide layer), and a stacked layer including a combination of these layers. The first gate conductive layer **26**A may be formed using the gate insulation layer pattern **25**A, for example, a silicon oxide layer and a polysilicon layer having an excellent interface characteristic. The second gate conductive layer **27** may be formed using one of a metal layer having an excellent electrical conductivity, a conductive metal nitride layer, or a metal silicide layer.

The gate hard mask layer **28** may be one of an oxide layer, a nitride layer, an oxynitride layer, a carbon containing layer, and a stacked layer including a combination of these layers. For example, the oxide layer may be one of a silicon oxide (SiO_2) layer, boron phosphorus silicate glass (BPSG), phosphorus silicate glass (PSG), tetra ethyle ortho silicate (TEOS), un-doped silicate glass (USG), spin on glass (SOG), high density plasma (HDP), and spin on dielectric (SOD). The nitride layer may be a silicon nitride layer (Si_3N_4). The carbon containing layer may be one of an amorphous carbon layer (ACL) and a carbon rich polymer layer.

As descried above, the present invention may relieve the HEIP phenomenon even without using a gate tap by forming the protrusion **21**A of the three-dimensional structure over the edge of the active region **23** contacting the portion of the isolation region **22** under the gate pattern **29**, or the boundary region between the isolation region **22** and the active region **23** under the gate pattern **29** where the HEIP phenomenon occurs to increase the channel length.

Also, the present invention may relieve the HEIP phenomenon even without using a gate tap, thereby reducing a net die size. Accordingly, the productivity of a semiconductor device may be improved.

Also, since a gate insulation layer pattern **25**A is formed over a protrusion surface in accordance with the present invention, deterioration of the characteristic of the gate insulation layer pattern **25**A due to a moat formed over the edge of the isolation region **22** contacting the active region **23** is prevented. That is, limitations (e.g., a hump) and a leakage current generated by a thinly formed gate insulation layer pattern **25**A in a region where a moat is formed in a typical semiconductor device may be prevented.

FIGS. **3**A to **3**C illustrate a method for fabricating a semiconductor device in accordance with an embodiment of the present invention, taken along the lines X-X' and Y-Y' of FIG. **2**A.

Referring to FIG. **3**A, hard mask patterns (not shown) including a pad oxide layer (not shown) and a pad nitride layer (not shown) are formed over the substrate **21**, and the substrate **21** is etched using the hard mask patterns as an etch barrier (or etch mask) to form a trench.

A sidewall oxide layer (not shown), a liner nitride layer (not shown), and a liner oxide layer (not shown) are sequentially formed over the surface of the trench, and a dielectric for an isolation layer is formed to fill the trench.

The dielectric for the isolation layer is planarized using chemical mechanical polishing (CMP) to expose the pad nitride layer, and the hard mask patterns are removed to form the isolation region **22**. At this point, though not shown in the drawing, a moat is formed at the edge of the isolation region **22** contacting the active region **23** while portions of the sidewall oxide layer and the liner nitride layer are lost during a process of removing the hard mask patterns.

A portion of the substrate **21** excluding a region where the isolation region **22** has been formed is defined as the active region **23**.

Hard mask patterns **24** are formed over the substrate **21** including the isolation region **22** and the active region **23**, and the substrate **21** is etched using the hard mask patterns **24** as an etch barrier to form the protrusion **21**A having a higher surface than that of the substrate **21** at the edge of the active region **23** contacting the isolation region **22**. Also, the protrusion **21**A may be formed in the boundary region between the isolation region **22** and the active region **23**.

The protrusion **21**A plays the same role as that of the typical gate tap, and may be formed such that its height H is greater than its width W**2** to secure a required channel length through a subsequent process.

Referring to FIG. **3**B, a gate insulation layer **25** is formed over the entire surface of the substrate **21** including the protrusion **21**A. At this point, the gate insulation layer **25** may be formed using a silicon oxide layer through thermal oxidation. Since the gate insulation layer **25** is formed over the surface of the protrusion **21**A, it is not influenced by the moat formed in a portion of the isolation region **22** contacting the active region **23**. Generally, the gate insulation layer **25** formed in a region where a moat is generated is formed thin due to a sharp shape of the moat, and accordingly, has been considered as a reason for generating limitations such as a hump and a leakage current.

A first gate conductive layer **26** is formed over the gate insulation layer **25** to cover the protrusion **21**A. At this point, the first gate conductive layer **26** may be formed using the gate insulation layer **25**, for example, a silicon oxide layer and a polysilicon layer having an excellent interface characteristic.

A planarization process is performed to remove a height difference of the first gate conductive layer **26** caused by the protrusion **21**A. At this point, the planarization process may be performed using CMP.

Referring to FIG. **3**C, a second gate conductive layer **27** is formed over the first gate conductive layer **26**. At this point, the second conductive layer **27** may be one of a metal layer (e.g., a W layer and a Ni layer having excellent conductivity compared to the first gate conductive layer **26**), a conductive metal nitride layer (e.g., a TiN layer), a metal silicide layer (e.g., a tungsten silicide layer and a nickel silicide layer), and a stacked layer including a combination of these layers.

The gate hard mask layer **28** is formed over the second gate conductive layer **27**. At this point, the gate hard mask layer **28** may be one of an oxide layer, a nitride layer, an oxynitride layer, a carbon containing layer, and a stacked layer including a combination thereof.

Hard mask patterns (not shown) are formed over the gate hard mask layer **28**, and the gate hard mask layer **28**, the second gate conductive layer **27**, the first gate conductive layer **26**, and the gate insulation layer **25** are sequentially etched using the hard mask patterns as an etch barrier. Through this process, the gate insulation layer pattern **25**A covering the surface of the protrusion **21**A, a gate electrode in which the first gate conductive layer **26**A and the second gate conductive layer **27** are stacked, and a gate pattern **29** in which the gate hard mask layer **28** formed over the gate electrode is stacked, may be formed.

As descried above, the present invention may relieve the HEIP phenomenon even without using a gate tap by forming the protrusion **21**A of the three-dimensional structure over the edge of the active region **23** contacting the portion of the isolation region **22** under the gate pattern **29**, or the boundary region between the isolation region **22** and the active region **23** under the gate pattern **29** where the HEIP phenomenon occurs to increase the channel length.

Also, the present invention may relieve the HEIP phenomenon even without using a gate tap, thereby improving degree of integration of a semiconductor device. Accordingly, the productivity of a semiconductor device may be improved.

Also, since the gate insulation layer pattern **25**A is formed over the surface of the protrusion **21**A in accordance with the present invention, deterioration of the electrical characteristic of a semiconductor device due to a moat formed over the edge of an isolation region contacting an active region is prevented.

In accordance with the present invention, the protrusion of a three-dimensional structure is formed in the edge of an active region contacting a portion of an isolation region under a gate pattern, or a boundary region between a portion of the isolation region and a portion of the active region under the gate pattern where an HEIP phenomenon occurs to increase a channel length, so that the HEIP phenomenon may be relieved even without using a gate tap.

Also, since the HEIP phenomenon may be relieved even without a gate tap in accordance with the present invention, the degree of integration of a semiconductor device may be improved and thus productivity of a semiconductor device is improved.

Also, since a gate insulation layer is formed over a protrusion surface in accordance with the present invention, deterioration of the electrical characteristic of a semiconductor device due to moat formed over the edge of an isolation region contacting an active region is prevented.

While the present invention has been described with respect to the specific embodiments, the above embodiments of the present invention are illustrative and not limitative. It will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

1. A method for fabricating a semiconductor device, the method comprising:
- forming an isolation region in a substrate by filling a trench formed in the substrate with a dielectric layer;
- forming hard mask patterns over the substrate including an active region and the isolation region;
- etching the substrate using the hard mask patterns as an etch mask to form a protrusion having a higher surface than that of the substrate;
- forming a gate insulation layer over the substrate including the protrusion;
- forming a gate conductive layer and a gate hard mask layer over the gate insulation layer; and
- forming a gate pattern overlapping the protrusion by selectively etching the gate hard mask layer, the gate conductive layer, and the gate insulation layer, wherein the protrusion is formed on an upper surface of the active region corresponding to a boundary region between the active region and the isolation region, and five surfaces of the protrusion protruded from the surface of the substrate are surrounded by the gate conductive layer.

2. The method of claim **1**, wherein the protrusion is formed over an edge of the active region that contacts a portion of the isolation region under the gate pattern.

3. The method of claim **1**, wherein the protrusion is formed over a boundary region between the isolation region and the active region under the gate pattern.

4. The method of claim **1**, wherein a width of the protrusion is smaller than that of the gate pattern.

5. The method of claim **1**, wherein a height of the protrusion is greater than a width of the gate pattern.

6. The method of claim **1**, wherein the protrusion has a shape of cube or rectangular parallelepiped.

7. The method of claim **1**, wherein the gate insulation layer is formed to be contacted with an upper surface of the active region.

8. The method of claim **1**, further comprising forming source and drain regions in the active region on opposing sides of the gate pattern, wherein upper surfaces of the source and drain regions are at a lower elevation than the higher surface of the protrusion.

9. A method for fabricating a semiconductor device, the method comprising:
- forming an isolation region in a substrate by filling a trench formed in the substrate with a dielectric layer;
- forming hard mask patterns over the substrate including an active region and the isolation region;
- etching the substrate using the hard mask patterns as an etch mask to form a protrusion having a higher surface than that of the substrate;
- forming a gate insulation layer over the substrate including the protrusion;
- forming a gate conductive layer and a gate hard mask layer over the gate insulation layer;
- forming a gate pattern overlapping the protrusion by selectively etching the gate hard mask layer, the gate conductive layer, and the gate insulation layer, wherein the protrusion is formed on an upper surface of the active region corresponding to a boundary region between the active region and the isolation region, and is surrounded by the gate conductive layer; and
- forming source and drain regions in the active region on opposing sides of the gate pattern, wherein upper sur-

faces of the source and drain regions are at a lower elevation than the higher surface of the protrusion.

10. The method of claim **9**, wherein the protrusion is formed over an edge of the active region that contacts a portion of the isolation region under the gate pattern.

11. The method of claim **9**, wherein the protrusion is formed over a boundary region between the isolation region and the active region under the gate pattern.

12. The method of claim **9**, wherein a width of the protrusion is smaller than that of the gate pattern.

13. The method of claim **9**, wherein a height of the protrusion is greater than a width of the gate pattern.

14. The method of claim **9**, wherein the protrusion has a shape of cube or rectangular parallelepiped.

15. The method of claim **9**, wherein the gate insulation layer is formed to be contacted with an upper surface of the active region.

16. The method of claim **9**, wherein five surfaces of the protrusion protruded from the surface of the substrate are surrounded by the gate conductive layer.

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