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(54) **SYSTEM AND METHOD FOR COMMUNICATING BETWEEN MULTIPLE VOLTAGE TIERS**

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(52) **U.S. Cl.** **327/540; 327/536; 327/544**

(58) **Field of Classification Search** None
See application file for complete search history.

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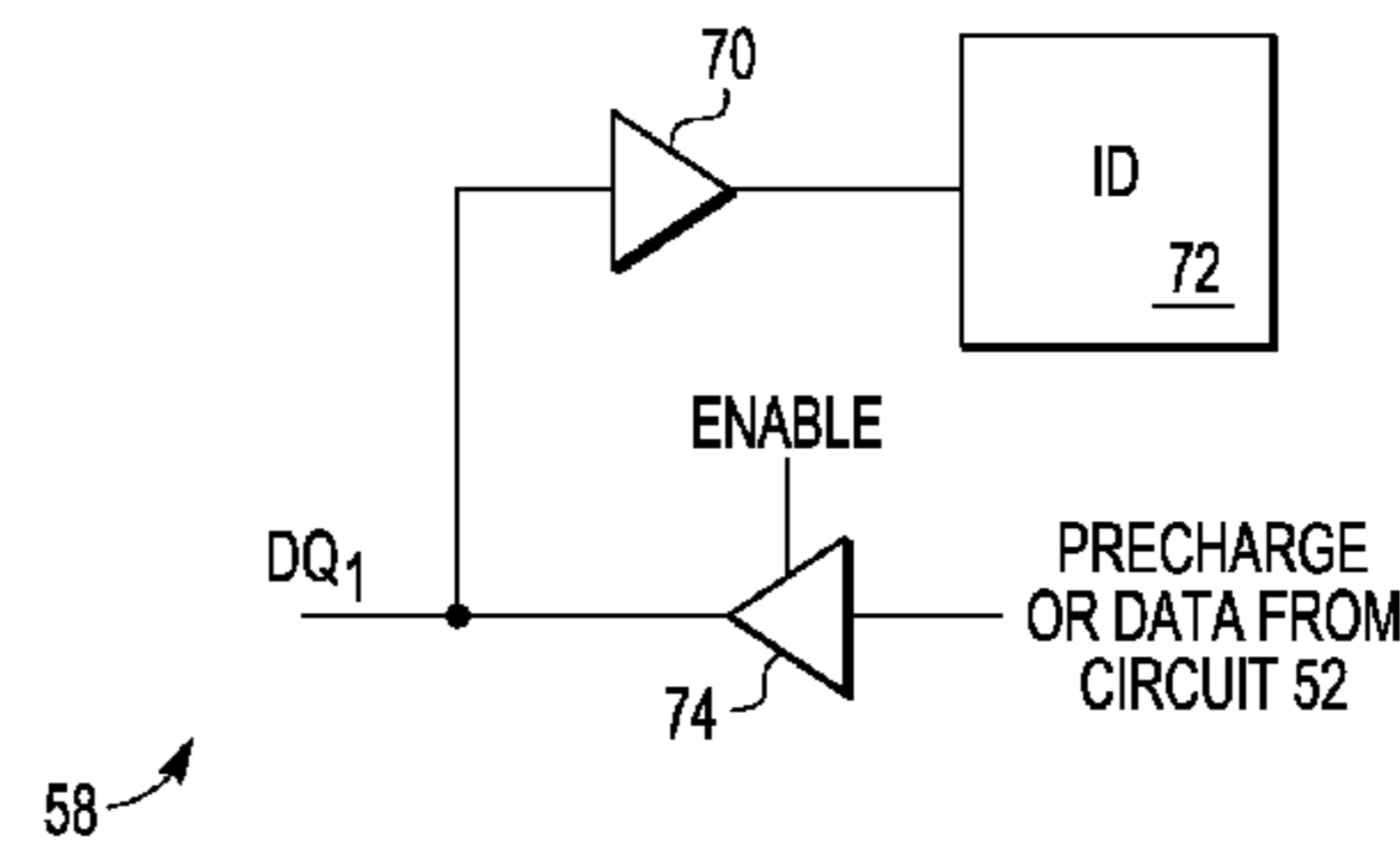
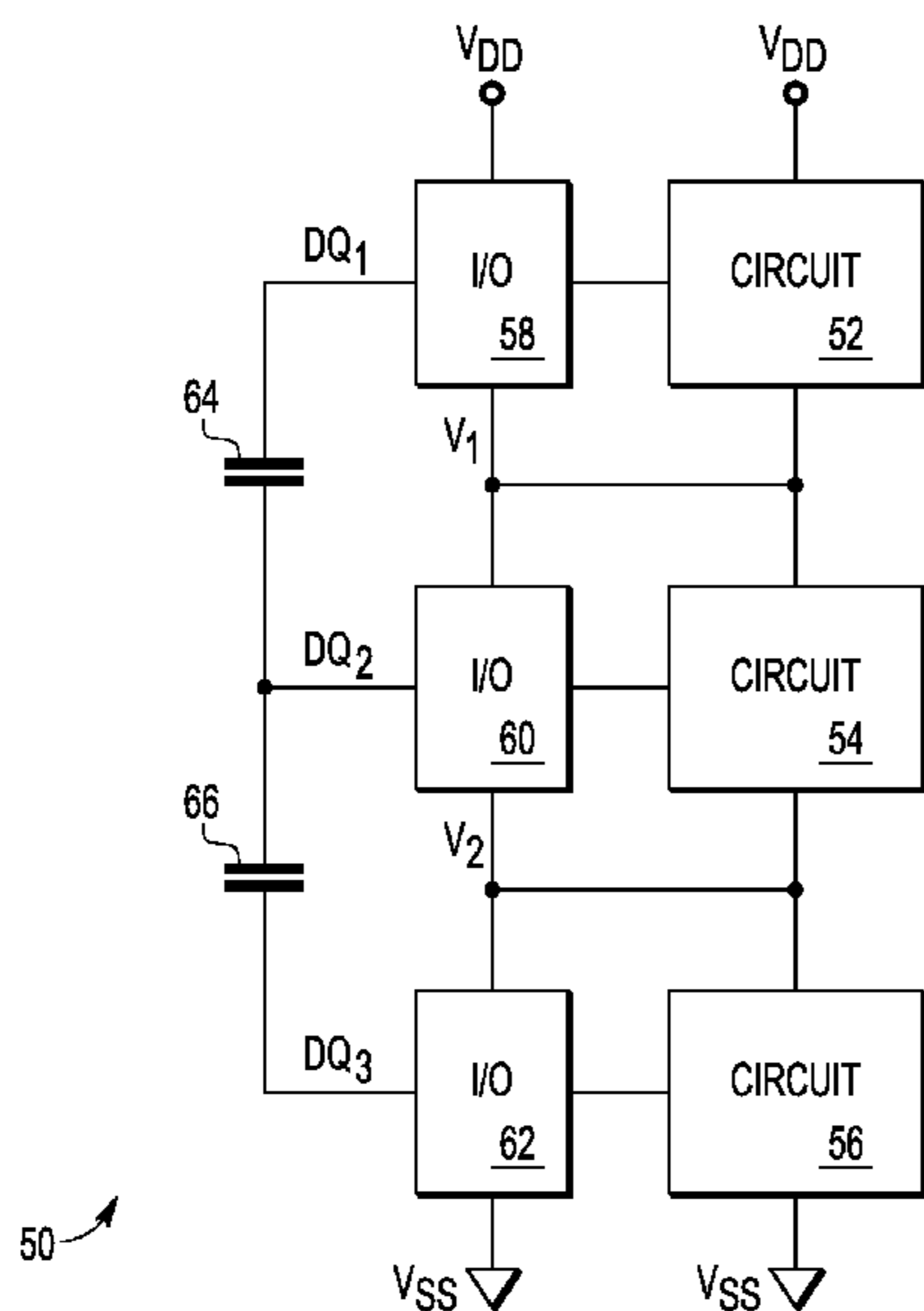
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(57) **ABSTRACT**

A system includes first, second, and third circuits and first and second capacitors. The first capacitor has a first power supply terminal coupled to positive power supply terminal, a second power supply terminal, and an input/output. The second capacitor has a first power supply terminal coupled the second power supply terminal of the first circuit, a second power supply terminal, and an input/output. The third circuit has a first power supply terminal coupled the second power supply terminal of the second circuit, a second power supply terminal, and an input/output. The first capacitor has a first terminal coupled to the input/output of the first circuit and a second terminal coupled to the input/output of the second circuit. The second capacitor has a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the input/output of the third circuit.

19 Claims, 3 Drawing Sheets



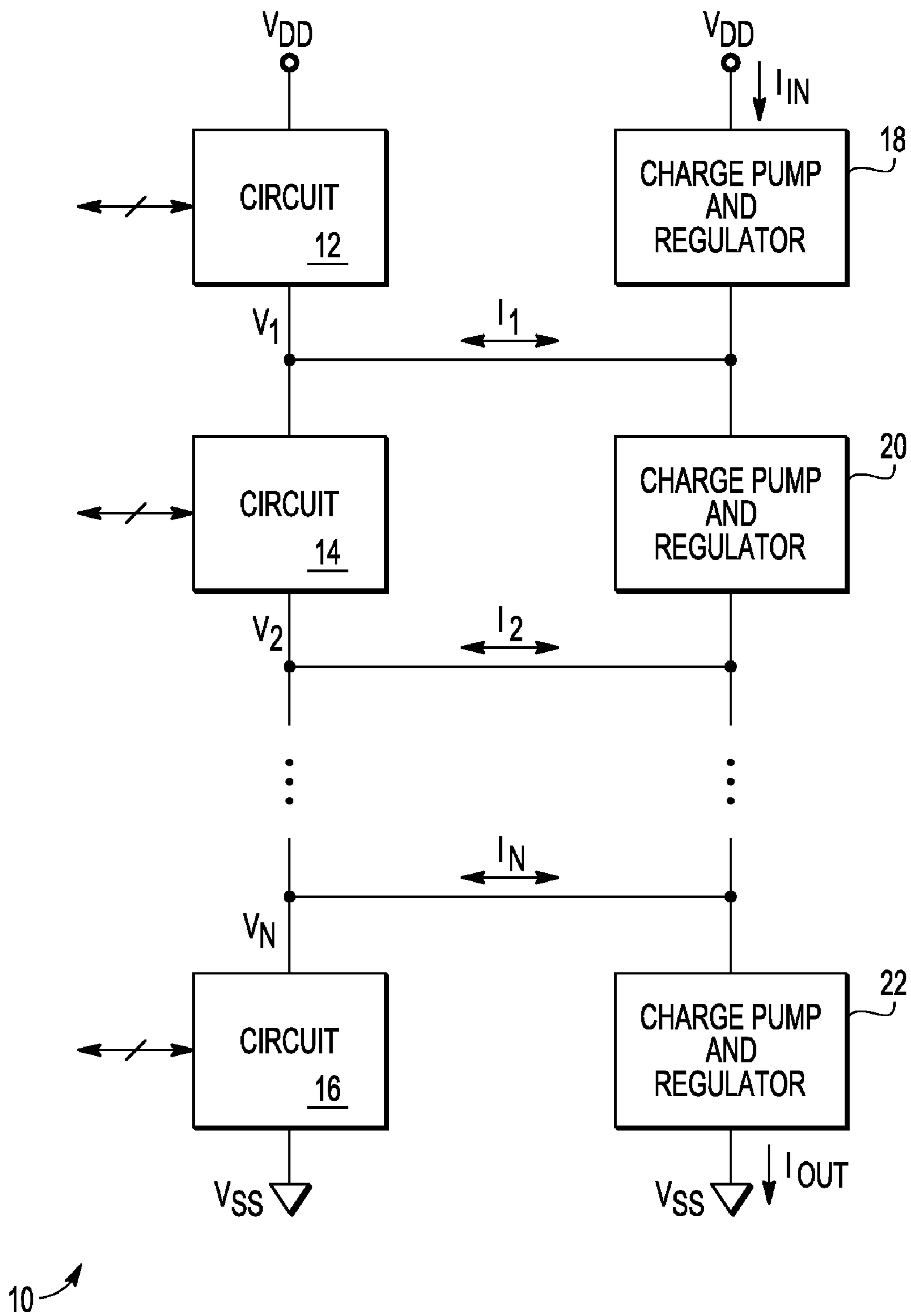


FIG. 1

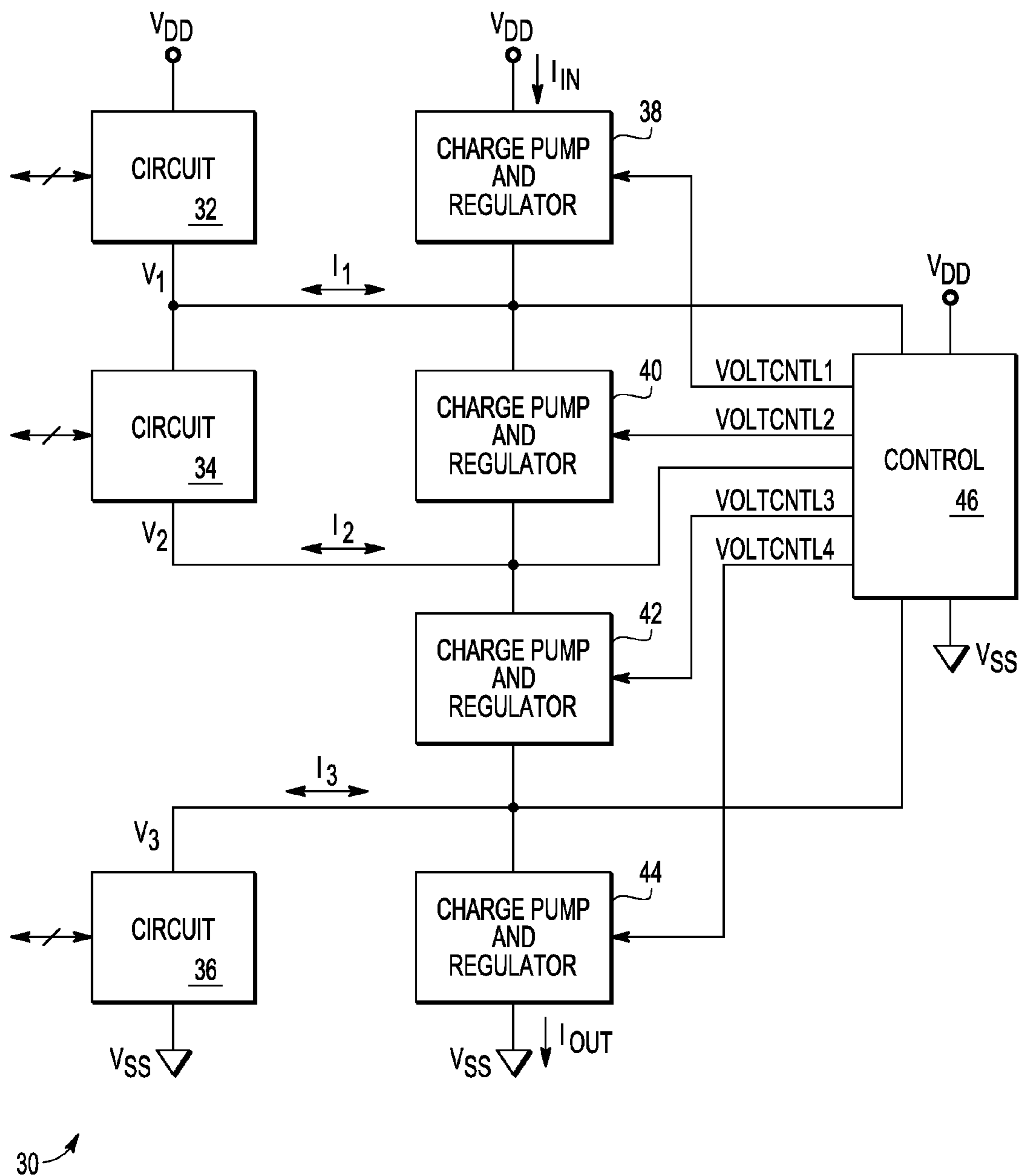


FIG. 2

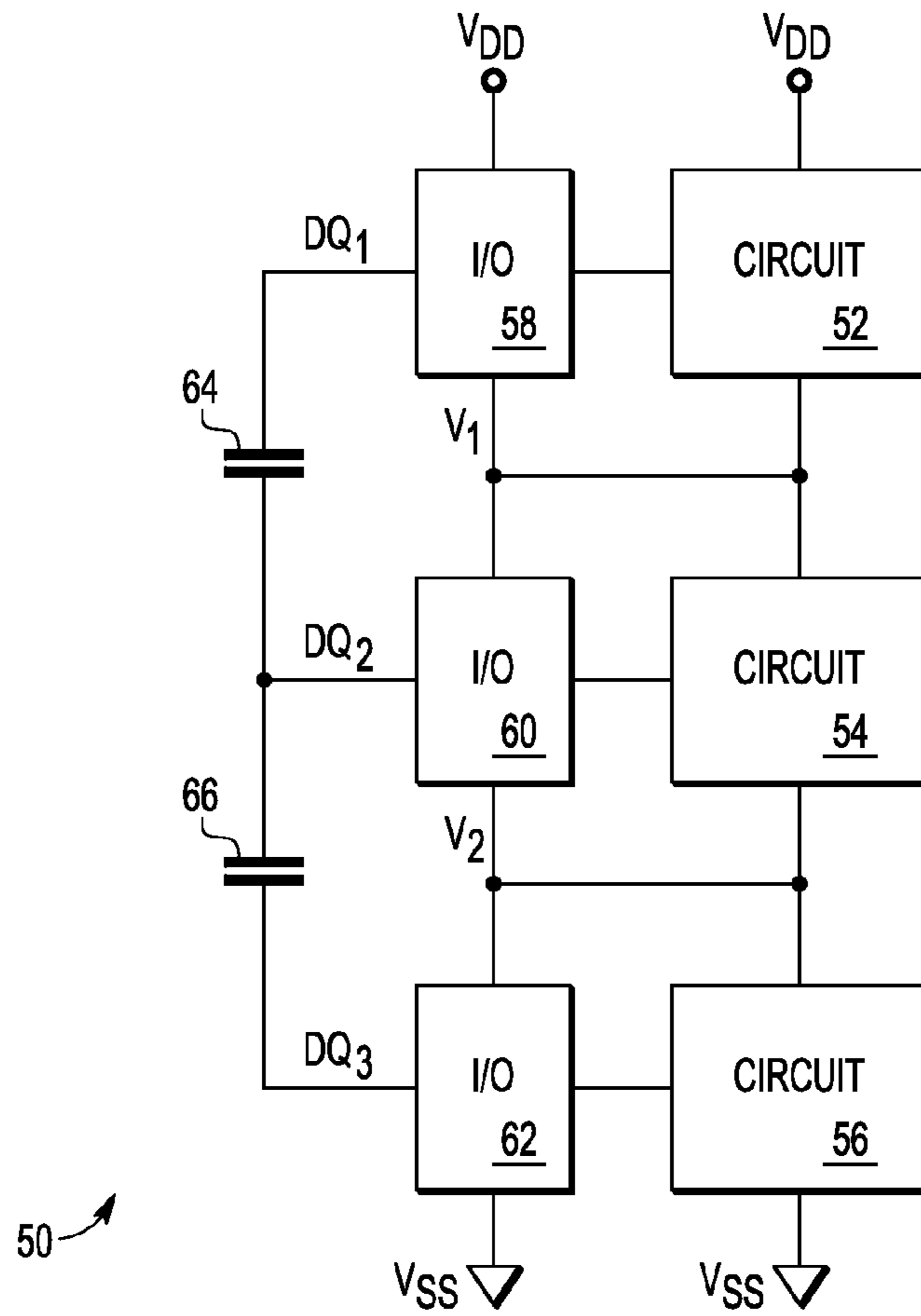


FIG. 3

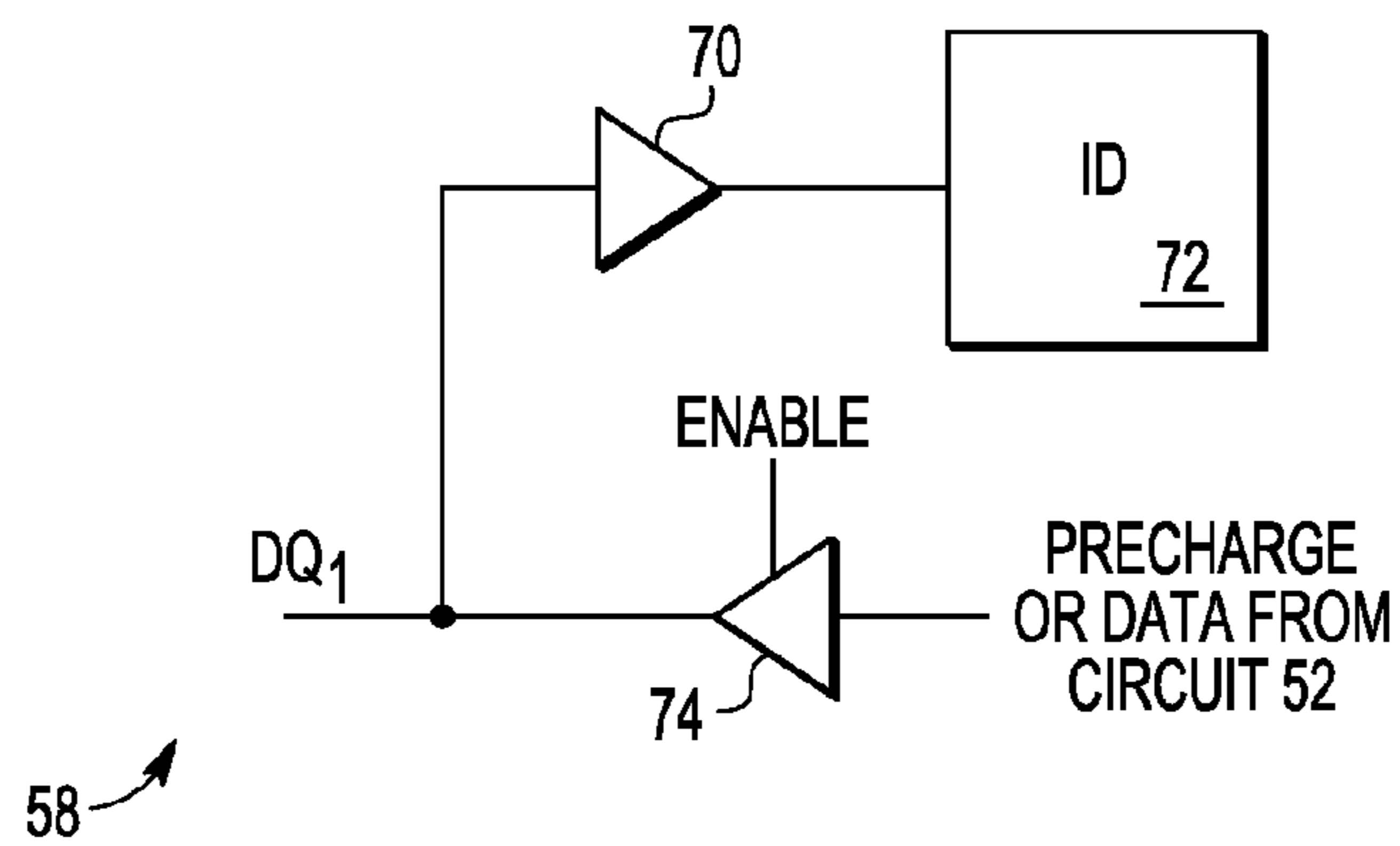


FIG. 4

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SYSTEM AND METHOD FOR COMMUNICATING BETWEEN MULTIPLE VOLTAGE TIERS

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to a co-pending application Ser. No. 12/621,005, By Perry Pelley, entitled "System Having Multiple Voltage Tiers and Method Therefor", and filed concurrently herewith.

BACKGROUND

1. Field

This disclosure relates generally to electronic circuits, and more specifically, to a system and method for communicating between multiple voltage tiers.

2. Related Art

Reducing power consumption in integrated circuits has become a high priority. One way power is saved in logic circuits is to use multiple voltage tiers to "stack" logic elements between power supply voltage rails. This allows a current used to perform one logic operation to be reused, or recycled, to perform additional logic operations. However, as transistor sizes are reduced, requiring lower power supply voltages, system noise becomes a larger percentage of the power supply voltage. In this case, the use of multiple voltage tiers becomes even more difficult. Also, it may be necessary for circuits of the multiple voltage tiers to be able to communicate with each other. One or more level shifters can be used to level shift a signal from one voltage tier to another, however, a level shifter can generally only translate between adjacent voltage tiers, requiring the use of multiple level shifters when there are more than two voltage tiers.

Therefore, what is needed is a system that solves the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

FIG. 1 illustrates, in block diagram form, a system in accordance with an embodiment.

FIG. 2 illustrates, in block diagram form, a system in accordance with another embodiment.

FIG. 3 illustrates, in block diagram form, a system in accordance with another embodiment.

FIG. 4 illustrates, in block diagram form, an input/output (I/O) circuit if the circuit of FIG. 3.

DETAILED DESCRIPTION

Generally, there is provided, a plurality of circuits, where each of the plurality of circuits receives a power supply voltage that is a predetermined fraction of a rail-to-rail power supply voltage. A charge pump and regulator circuit is coupled to each of the power supply terminals of each of the plurality of circuits. The charge pump and regulator circuit sinks or sources current at the power supply terminals of one of the plurality of circuits to balance the amount of current provided through the circuit. Balancing the current provides for less power consumption while also providing for more reliable operation. Also, the use of multiple voltage tiers

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provides the benefits of a very low power supply voltage while allowing the integrated circuit to be powered using a more easily usable, customer friendly, power supply voltage.

Also, there is provided, a circuit for allowing communication between circuits of multiple voltage tiers. The circuit includes a plurality of capacitors coupled together in series, where a capacitor of the series is coupled between the outputs of input/output circuits corresponding to each of the plurality of circuits. The series of capacitors are first precharged to a predetermined voltage. Then, when one of the I/O circuits provides a data bit to the series of capacitors, the data bit causes the voltage stored on each capacitor to increase or decrease by the same amount, thereby translating the data bit to each of the different voltage tiers simultaneously. By translating the data bit using the series of capacitors, level shifters are not required. Also, translating using the series of capacitors is much faster than traditional level shifters because a traditional level shifter generally can only level shift between adjacent voltage tiers. To level shift a signal between multiple voltage tiers requires a level shifter between each tier and the level shifting between tiers must be done serially.

The integrated circuit may comprise a semiconductor substrate formed from any semiconductor material or combinations of materials, such as gallium arsenide, silicon germanium, silicon-on-insulator (SOI), silicon, monocrystalline silicon, the like, and combinations of the above.

In one aspect, there is provided, a system, comprising: a first circuit having a first power supply terminal coupled to positive power supply terminal, a second power supply terminal, and an input/output; a second circuit having a first power supply terminal coupled the second power supply terminal of the first circuit, a second power supply terminal, and an input/output; a third circuit having a first power supply terminal coupled the second power supply terminal of the second circuit, a second power supply terminal, and an input/output; a first capacitor having a first terminal coupled to the input/output of the first circuit and a second terminal coupled to the input/output of the second circuit; and a second capacitor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the input/output of the third circuit. The first circuit may be for precharging the first terminal of the first capacitor to a first voltage during a precharge phase, wherein the first voltage may be between a voltage present on the first power supply terminal and the second power supply terminal of the first circuit. The second circuit may be for precharging the second terminal of the first capacitor and the first terminal of the second capacitor to a second voltage during the precharge phase, wherein the second voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the second circuit. The third circuit may be for precharging the second terminal of the second capacitor to a third voltage during the precharge phase, wherein the third voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the third circuit. The first circuit, when selected to provide an output, may be for providing an output signal on its input/output during a data phase following the precharge phase. The second circuit, when the first circuit is selected to provide an output and the second circuit is selected to receive an input, may be for interpreting a voltage present on the second terminal of the first capacitor in response to the first circuit providing the output signal to determine a logic state of the output signal. Each of the first, second, and third circuits may further comprise an identity recognition circuit for comparing an identification portion of a received signal with a stored circuit identification value to determine which of the

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first, second, and third circuits is the intended recipient of the received signal. The system may further comprise: a fourth circuit having a first power supply terminal coupled the second power supply terminal of the third circuit, a second power supply terminal, and an input/output; and a third capacitor having a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to the input/output of the fourth circuit. The fourth circuit may be for precharging the second terminal of the third capacitor to a fourth voltage during the precharge phase, wherein the fourth voltage may be between a voltage present on the first power supply terminal and the second power supply terminal of the fourth circuit. The fourth circuit, when the first circuit is selected to provide an output and the fourth circuit is selected to receive an input, may be for interpreting a voltage present on the second terminal of the third capacitor in response to the first circuit providing the output signal to determine the logic state of the output signal. The system may further comprise: a first charge pump having an input coupled to the first power supply terminal of the first circuit and an output coupled to the second power supply terminal of the first circuit; a second charge pump having an input coupled to the first power supply terminal of the second circuit and an output coupled to the second power supply terminal of the second circuit; and a third charge pump having an input coupled to the first power supply terminal of the third circuit and an output coupled to the second power supply terminal of the third circuit. The third charge pump may pass current from the first power supply terminal of the third circuit to the second supply terminal of the third circuit if a current supplied by the second circuit to the second power supply terminal of the second circuit exceeds a maximum current requirement of the third circuit. The first charge pump may provide current to the second circuit if a current passing through the first circuit is less than a minimum current required for the second circuit.

In another aspect, there is provided, a method, comprising: providing a first circuit having a first power supply terminal coupled to positive power supply terminal, a second power supply terminal, and an input/output; providing a second circuit having a first power supply terminal coupled the second power supply terminal of the first circuit, a second power supply terminal, and an input/output; providing a third circuit having a first power supply terminal coupled the second power supply terminal of the second circuit, a second power supply terminal, and an input/output; providing a first capacitor having a first terminal coupled to the input/output of the first circuit and a second terminal coupled to the input/output of the second circuit; providing a second capacitor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the input/output of the third circuit; precharging the first terminal of the first capacitor to a first voltage during a precharge phase, wherein the first voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the first circuit; precharging the second terminal of the first capacitor and the first terminal of the second capacitor to a second voltage during the precharge phase, wherein the second voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the second circuit; and precharging the second terminal of the second capacitor to a third voltage during the precharge phase, wherein the third voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the third circuit. The method may further comprise: providing an output signal on the input/output of the first circuit; and interpreting a voltage present on the second terminal of the first capacitor in response to the output

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signal being provided. The step of interpreting may be for determining a logic state of the output signal. The method may further comprise interpreting a voltage present on the second terminal of the second capacitor in response to the output signal being provided. The method may further comprise: passing a current through the first circuit; determining if the current exceeds a maximum current requirement of the second circuit; if the current exceeds the maximum current requirement, diverting a sufficient portion of the current away from the second circuit so that a remaining portion of the current does not exceed the maximum current requirement of the second circuit. The step of diverting is performed by passing the sufficient portion of the current through a charge pump coupled in parallel with the second circuit. The method may further comprise: passing a current through the first circuit; determining if the current is less than a minimum current requirement of the second circuit; and if the current is less than the minimum current requirement, adding an additional current to the first current so that a sum of the additional current and the first current is not less than the minimum current requirement of the second circuit. The step of adding may be performed by providing the additional current from a charge pump coupled in parallel with the first circuit.

In yet another aspect, there is provided, a system, comprising: a plurality of circuits having serially connected power supply terminals coupled between a positive power supply terminal and a negative power supply terminal; and a plurality of capacitors coupled in series; wherein: at a first end of the plurality of capacitors, a first capacitor has a terminal; at a second end of the plurality of capacitors, a last capacitor has a terminal; each circuit of the plurality of circuits has a first power supply terminal, a second power supply terminal, and an input/output; a first circuit of the plurality of circuits has its input/output coupled to the terminal of the first capacitor and is for precharging the terminal of the first capacitor during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the terminal of the first capacitor during a data phase following the precharge phase; a last circuit of the plurality of circuits has its input/output coupled to the terminal of the last capacitor and is for precharging the terminal of the last capacitor during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the terminal of the last capacitor during a data phase following the precharge phase; and each circuit of the plurality of circuits between the first and last circuits has its input/output coupled to a connection between two capacitors of the plurality of capacitors and is for precharging the connection at its input/output during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the connection at its input/output during a data phase following the precharge phase. The system may further comprise a plurality of charge pumps, wherein each charge pump may be coupled in parallel with one of the circuits of the plurality of circuits.

As used herein, the term "bus" is used to refer to a plurality of signals or conductors which may be used to transfer one or more various types of information, such as data, addresses, control, or status. The conductors as discussed herein may be illustrated or described in reference to being a single conductor, a plurality of conductors, unidirectional conductors, or bidirectional conductors. However, different embodiments may vary the implementation of the conductors. For example, separate unidirectional conductors may be used rather than bidirectional conductors and vice versa. Also, plurality of conductors may be replaced with a single conductor that transfers multiple signals serially or in a time multiplexed

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manner. Likewise, single conductors carrying multiple signals may be separated out into various different conductors carrying subsets of these signals. Therefore, many options exist for transferring signals.

The terms “assert” or “set” and “negate” (or “deassert” or “clear”) are used herein when referring to the rendering of a signal, status bit, or similar apparatus into its logically true or logically false state, respectively. If the logically true state is a logic level one, the logically false state is a logic level zero. And if the logically true state is a logic level zero, the logically false state is a logic level one.

Each signal described herein may be designed as positive or negative logic, where negative logic can be indicated by a bar over the signal name or an asterix (*) following the name. In the case of a negative logic signal, the signal is active low where the logically true state corresponds to a logic level zero. In the case of a positive logic signal, the signal is active high where the logically true state corresponds to a logic level one. Note that any of the signals described herein can be designed as either negative or positive logic signals. Therefore, in alternate embodiments, those signals described as positive logic signals may be implemented as negative logic signals, and those signals described as negative logic signals may be implemented as positive logic signals.

FIG. 1 illustrates, in block diagram form, a system 10 in accordance with an embodiment. System 10 includes a plurality of circuits such as circuits 12, 14, and 16. Circuits 12, 14, and 16 can include any type of circuit, such as data processing, digital signal processing (DSP), memory, or the like. For example, circuits 12, 14, and 16 can be digital logic circuits, analog circuits, or a combination of digital and analog circuits. System 10 also includes a plurality of charge pump and regulator circuits, such as charge pump and regulator circuits 18, 20, and 22. The charge pump can be any kind of charge pump and the regulator can be any kind of voltage regulator. Circuit 12 has a first power supply voltage terminal for receiving a power supply voltage labeled “VDD”, a second power supply voltage terminal for receiving a power supply voltage labeled “V1”, and a plurality of bidirectional terminals for coupling circuit 12 to another circuit (not shown), if necessary. Circuit 14 has a first power supply voltage terminal for receiving a power supply voltage labeled “V1”, a second power supply voltage terminal for receiving a power supply voltage labeled “V2”, and a plurality of bidirectional terminals for coupling circuit 14 to another circuit (not shown). Circuit 16 has a first power supply voltage terminal for receiving a power supply voltage labeled “VN”, a second power supply voltage terminal for receiving a power supply voltage labeled “VSS”, and a plurality of bidirectional terminals for coupling circuit 16 to another circuit (not shown).

Each of the circuits 12, 14, through 16 belong to a “voltage tier”, where a voltage tier is determined by where it is positioned relative to other voltage tiers in the power supply voltage VDD. For example, the voltage tier of circuit 12 is a difference between VDD and voltage V1. The voltage tier of circuit 14 is a difference between V1 and V2 and the voltage tier of circuit 16 is voltage VN minus VSS.

Charge pump and regulator 18 has a first power supply voltage terminal for receiving power supply voltage VDD, and a second power supply voltage terminal for receiving power supply voltage V1. Charge pump and regulator 20 has a first power supply voltage terminal for receiving power supply voltage V1, and a second power supply voltage terminal for receiving power supply voltage V2. Charge pump and regulator 22 has a first power supply voltage terminal for receiving power supply voltage VN, and a second power

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supply voltage terminal for receiving VSS. A current labeled “I1” can be either sourced by charge pump and regulator 18, or sinked by charge pump and regulator 20. A current labeled “I2” can be either sourced by charge pump and regulator 20, or sinked by a charge pump and regulator circuit coupled to power supply voltage terminal V2 but not shown. A current labeled “I_N” can be either sourced by a charge pump and regulator that is not shown, or sinked by charge pump and regulator 22.

In one embodiment, circuits 12, 14, and 16 are implemented as CMOS (complementary metal-oxide semiconductor) logic circuits. In another embodiment, the circuit portions may be a different kind of logic circuit, or an analog circuit. Also, in one embodiment, power supply voltage VDD is a positive power supply voltage, such as for example, 2.7 volts, and VSS is at ground potential. In another embodiment, VDD may be at ground potential while VSS is a negative power supply voltage. Generally, circuit 12 has as its power supply voltage, a voltage difference between VDD and V1 (first voltage tier). Likewise, circuit 14 has a power supply voltage that is the voltage difference between V1 and V2 (second voltage tier). Also, circuit 16 has a power supply voltage that is the voltage difference between VN and VSS (nth voltage tier).

Ideally, the power supply voltages used by each of circuits 12, 14, and 16 are substantially equal. Also, a current into the VDD power supply voltage terminal labeled “I_{VN}” is equal to a current at the VSS power supply voltage terminal. However, circuit differences, or imbalances, may cause one of the circuit portions to use more current than another one of the circuit portions. Charge pump and regulator circuits 18, 20, and 22 are used to pump a current that corrects, or compensates, for the imbalance in currents. Because the charge pump only has to provide a difference current, a relatively poor charge pump efficiency only applies to the difference current and therefore minimally impacts the power consumption. In one example, charge pump and regulator 18 supplies current to circuit 14 if current supplied by circuit 12 at the power supply node V1 is less than a minimum current requirement of circuit 14. Also, charge pump and regulator 20 passes current from voltage node V1 through circuit 14 to the voltage node V2 if the current supplied by circuit 12 to voltage node V1 exceeds a maximum current requirement of circuit 14. Charge pump and regulator 18 determines if the minimum current requirement is met by detecting a voltage on voltage node V1. Also, charge pump and regulator 20 may determine if the maximum current requirement is met by detecting the voltage on the node V1. Likewise, charge pump and regulator 20 supplies current to circuit 16 (if there were only three circuits 12, 14, and 16 in an embodiment) if the current supplied by circuit 14 at node V2 is less than a minimum current requirement of circuit 16. Charge pump and regulator 22 passes current from node VN through charge pump and regulator 22 to VSS if the current supplied by circuit 14 to node VN (or V2) exceeds a maximum current requirement of circuit 16.

FIG. 2 illustrates, in block diagram form, a system 30 in accordance with another embodiment. System 30 includes circuits 32, 34, and 36, charge pump and regulator circuit 38, 40, 42, and 44, and control circuit 46. Circuits 32, 34, and 36 can include any type of circuit, such as data processing, digital signal processing (DSP), memory, or the like. For example, circuits 12, 14, and 16 can be digital logic circuits, analog circuits, or a combination of digital and analog circuits. Circuit 32 has a first power supply voltage terminal for receiving a power supply voltage labeled “VDD”, and a second power supply voltage terminal for receiving a power

supply voltage labeled “V1”. Circuit 34 has a first power supply voltage terminal for receiving power supply voltage V1, and a second power supply voltage terminal for receiving a power supply voltage labeled “V2”. Circuit 36 has a first power supply voltage terminal coupled to receive a power supply voltage labeled “V3”, and a second power supply voltage terminal for receiving power supply voltage VSS. Each of circuits 32, 34, and 36 have a plurality of bi-directional terminals for communicating with other circuits (not shown).

Charge pump and regulator 38 has a first power supply terminal coupled to VDD, a second power supply voltage terminal coupled to V1 for sinking and/or sourcing a current labeled “I2”, and an input terminal for receiving a control signal labeled “VOLTCNTL 1”. Charge pump and regulator 40 has a first power supply voltage terminal coupled to V1, a second power supply voltage terminal coupled to V2 for sinking and/or sourcing a current labeled “I2”, and an input terminal for receiving a control signal labeled “VOLTCNTL 2”. Charge pump and regulator 42 has a first power supply voltage terminal coupled to V2, a second power supply voltage terminal coupled to V3, and an input terminal for receiving control signal VOLTCNTL 3. Charge pump and regulator 44 has a first power supply voltage terminal coupled to V3 for sinking and/or sourcing a current labeled “I3”, a second power supply voltage terminal coupled to VSS, and an input terminal couple to receive control signal VOLTCNTL 4. Control circuit 46 has a first power supply voltage terminal coupled to receive power supply voltage VDD, a second power supply voltage terminal coupled to VSS, and output terminals for providing voltage control signals VOLTCNTL 1-VOLTCNTL 4. Note that the embodiment of FIG. 2 includes three circuits and four charge pump and regulator circuits for illustration purposes only. In other embodiments there can be any number of circuits, and corresponding charge pump and regulator circuits.

The full rail power supply voltage of system 30 is VDD, where VSS is coupled to ground. Circuit 32 receives a power supply voltage equal to VDD minus V1, where VDD minus V1 establishes a first voltage tier. Likewise, circuit 34 receives a power supply voltage equal to V1 minus V2 (second voltage tier), and circuit 36 receives a power supply voltage equal to V3 minus VSS (third voltage tier). In one embodiment, the voltage tiers by each of circuits 32, 34, and 36 may be intended to be substantially equal. However, circuit imbalances may cause one of the circuits to use more current than the other circuits. In the embodiment of FIG. 2 each of the voltage tiers can be set independently of the other tiers. Charge pump and regulator circuits 38, 40, 42, and 44 can be used to source or sink a difference current as described above in the discussion of FIG. 1. In addition, control circuit 46 is used to control the voltage drop across each of circuits 32, 34, and 36. In the event the supply voltage dropped by all of the circuits 32, 34, and 36 is not equal to VDD, then charge pump and regulator 42 is used to make up the difference.

FIG. 3 illustrates, in block diagram form, a system 50 in accordance with another embodiment. System 50 includes circuits 52, 54, and 56, input/output (I/O) circuits 58, 60, and 62, and capacitors 64 and 66. Circuit 52 has a first power supply voltage terminal coupled to receive power supply voltage VDD, an I/O terminal, and a second power supply voltage terminal coupled to receive voltage V1. Circuit 54 has a first power supply terminal coupled to V1, an I/O terminal, and a second power supply terminal coupled to voltage V2. Circuit 56 has a first power supply terminal coupled to voltage V2, an I/O terminal, and a second power supply terminal coupled to VSS. I/O circuit 58 has a first power supply voltage terminal

coupled to VDD, a first I/O terminal for providing or receiving data signal DQ1, a second I/O terminal coupled to the I/O terminal of circuit 52, and a second power supply terminal coupled to V1. I/O circuit 60 has a first power supply voltage terminal coupled to V1, a first I/O terminal for providing or receiving data signal DQ2, a second I/O terminal coupled to the I/O terminal of circuit 54, and a second power supply terminal coupled to V2. I/O circuit 62 has a first power supply voltage terminal coupled to V2, a first I/O terminal for providing or receiving data signal DQ3, a second I/O terminal coupled to the I/O terminal of circuit 56, and a second power supply terminal coupled to VSS. Capacitor 64 has a first plate electrode coupled to the first I/O terminal of I/O circuit 58, and a second plate electrode coupled to the first I/O terminal of I/O circuit 54. Capacitor 66 has a first plate electrode coupled to the first I/O terminal of I/O circuit 60, and a second plate electrode coupled to the first I/O terminal of I/O circuit 62. Note that system 50 includes two series-connected capacitors for illustration purposes only. Other embodiments may include more than two series-connected capacitors. Also, note that the described embodiment includes bi-directional I/O terminals. In other embodiments, the I/O terminals may be implemented as separate input and output terminals.

Circuit 52 includes circuitry for precharging the first plate electrode of capacitor 64 to a first voltage during a precharge phase. The first voltage is between a voltage present on power supply terminal VDD and power supply terminal V1 of circuit 52. Circuit 54 includes circuitry for precharging the second plate electrode of capacitor 64 and the first plate electrode of capacitor 66 to a second voltage during the precharge phase. The second voltage is between a voltage present on the power supply terminal V1 and power supply terminal V2 of circuit 54. Circuit 56 includes circuitry for precharging the second plate electrode of capacitor 66 to a third voltage during the precharge phase. The third voltage is between a voltage present on power supply terminal V2 and the power supply terminal VSS of circuit 56. Circuit 52, when selected to provide an output signal, will provide an output signal DQ1 on its I/O terminal during a data phase following the precharge phase. Circuit 54, when circuit 52 selected to provide an output and circuit 54 is selected to receive an input signal DQ2, will interpret a voltage present on the second plate electrode of capacitor 64 in response to circuit 52 providing the output signal DQ1 to determine a logic state of the output signal DQ1. Circuit 56, when circuit 52 is selected to provide output DQ1 and circuit 56 is selected to receive an input DQ3, will interpret a voltage present on the second plate electrode of capacitor 66 in response to circuit 52 providing output signal DQ1 to determine the logic state of output signal DQ1. Further, there can be any number of circuits and capacitors. For example, there may be a fourth circuit (not shown in FIG. 3) having a first power supply terminal coupled to the second power supply terminal of circuit 56, a second power supply terminal coupled to VSS, and an input/output terminal coupled to an additional capacitor. The additional capacitor having a first plate electrode coupled to the second plate electrode of capacitor 66 and a second plate electrode coupled to the input/output of the fourth circuit. The fourth circuit may also include circuitry for precharging the second plate electrode of the third capacitor to a fourth voltage during a precharge phase. The fourth voltage would be a fraction of the power supply voltage between rails VDD and VSS, the magnitude of the power supply voltage would depend on the number of voltage tiers in the system. The fourth circuit would communicate with circuits of the other voltage tiers as described above.

System 50 of FIG. 3 may also include charge pump and regulator circuits as described above for FIG. 1 and FIG. 2. For example, there may be a first charge pump having an input coupled to the V1 terminal of circuit 52, a second charge pump having an input coupled to the V1 terminal and the V2 terminal, and a third charge pump having an input coupled to the V2 terminal. The third charge pump can pass current from the first power supply terminal of circuit 56 to the second supply terminal of circuit 56 if a current supplied by circuit 54 to the second power supply terminal of circuit 54 exceeds a maximum current requirement of circuit 56.

Series-connected capacitors 64 and 66 and I/O circuits 58, 60, and 62 provide for communication between circuits of multiple voltage tiers, such as circuits 52, 54, and 56. The series-connected capacitors are first precharged to a predetermined voltage. The precharge voltage can be provided by circuit 52 as illustrated in FIG. 4, or may be generated within any of I/O circuits such as I/O circuit 58. The precharge voltage causes charge to accumulate on the capacitors. Each of the series-connected capacitors will be charged to substantially the same voltage. Then, one of the I/O circuits provides a data bit in the form of a voltage level to the series of capacitors. The data bit can be provided by buffer 74 as illustrated, or by another buffer (not shown). The data bit causes the voltage stored on each of capacitors 64 and 66 to increase or decrease by the same amount, thereby translating the data bit to each of the different voltage tiers simultaneously. For example, if the data bit is higher than the precharge voltage, the voltage level of the capacitors is increased and a logical one may be transmitted. If the data is lower than the precharge voltage, the voltage level on the capacitors is lowered and a logic zero may be transmitted.

FIG. 4 illustrates, in block diagram form, input/output (I/O) circuit 58 if system 50 of FIG. 3. I/O circuit 58 includes buffers 70 and 74, and identity recognition circuit 72. Buffer 70 has an input terminal for receiving signal DQ1, and an output terminal. Buffer 74 has an input terminal coupled to receive either a precharge signal or a data signal from circuit 52, an output terminal for providing signal DQ1, and a control terminal for receiving enable signal ENABLE. Identity recognition circuit 72 has an input terminal coupled to the output terminal of buffer 70. Identity recognition circuit 72 is used to determine the intended recipient of a signal transmitted to capacitors 64 and 66. In one embodiment, identity recognition circuit 72 includes a comparator for comparing an identification portion of a received signal to a stored circuit identification value to determine if it is the intended recipient of the received signal. For example, an output signal DQ1 might include an identification recognition portion directing the DQ1 signal to only I/O circuit 62. I/O circuit 60 would then ignore the DQ1 signal after processing a recognition portion of the DQ1 signal.

Note that the charge pump and regulator circuits of FIGS. 1 and 2 can also be used with the system 50 of FIG. 3.

By translating the data bit using the series of capacitors, level shifters are not required. Also, translating using the series of capacitors is much faster than traditional level shifters because a traditional level shifter generally can only level shift between adjacent voltage tiers. To level shift a signal between multiple voltage tiers requires a level shifter between each tier and the level shifting between tiers must be done serially.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and

appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

Some of the above embodiments, as applicable, may be implemented using a variety of different information processing systems. For example, although FIG. 1 and the discussion thereof describe an exemplary information processing system, this exemplary system is presented merely to provide a useful reference in discussing various aspects of the embodiment. Of course, the description of the system has been simplified for purposes of discussion, and it is just one of many different types of appropriate systems that may be used. Those skilled in the art will recognize that the boundaries between logic blocks are merely illustrative and that alternative embodiments may merge logic blocks or circuit elements or impose an alternate decomposition of functionality upon various logic blocks or circuit elements.

Thus, it is to be understood that the systems depicted herein are merely exemplary, and that in fact many other systems can be implemented which achieve the same functionality. In an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operation may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

Although the invention is described herein with reference to specific embodiments, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all the claims.

The term "coupled," as used herein, is not intended to be limited to a direct coupling or a mechanical coupling.

Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles.

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Unless stated otherwise, terms such as “first” and “second” are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements.

What is claimed is:

1. A system, comprising:
 - a first circuit having a first power supply terminal coupled to positive power supply terminal, a second power supply terminal, and an input/output;
 - a second circuit having a first power supply terminal coupled the second power supply terminal of the first circuit, a second power supply terminal, and an input/output;
 - a third circuit having a first power supply terminal coupled the second power supply terminal of the second circuit, a second power supply terminal, and an input/output;
 - a first capacitor having a first terminal coupled to the input/output of the first circuit and a second terminal coupled to the input/output of the second circuit; and
 - a second capacitor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the input/output of the third circuit, wherein the first circuit is for precharging the first terminal of the first capacitor to a first voltage during a precharge phase, wherein the first voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the first circuit;
 - wherein the second circuit is for precharging the second terminal of the first capacitor and the first terminal of the second capacitor to a second voltage during the precharge phase, wherein the second voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the second circuit; and
 - wherein the third circuit is for precharging the second terminal of the second capacitor to a third voltage during the precharge phase, wherein the third voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the third circuit.
2. The system of claim 1, wherein:
 - the first circuit, when selected to provide an output, is for providing an output signal on its input/output during a data phase following the precharge phase;
 - the second circuit, when the first circuit is selected to provide an output and the second circuit is selected to receive an input, is for interpreting a voltage present on the second terminal of the first capacitor in response to the first circuit providing the output signal to determine a logic state of the output signal.
3. The system of claim 1, wherein each of the first, second, and third circuits further comprises:
 - an identity recognition circuit for comparing an identification portion of a received signal with a stored circuit identification value to determine which of the first, second, and third circuits is the intended recipient of the received signal.
4. The system of claim 1, further comprising:
 - a fourth circuit having a first power supply terminal coupled to the second power supply terminal of the third circuit, a second power supply terminal, and an input/output; and
 - a third capacitor having a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to the input/output of the fourth circuit.

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5. The system of claim 4, wherein:
 - the fourth circuit is for precharging the second terminal of the third capacitor to a fourth voltage during the precharge phase, wherein the fourth voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the fourth circuit.
6. The system of claim 5, wherein:
 - the fourth circuit, when the first circuit is selected to provide an output and the fourth circuit is selected to receive an input, is for interpreting a voltage present on the second terminal of the third capacitor in response to the first circuit providing the output signal to determine the logic state of the output signal.
7. The system of claim 1, further comprising:
 - a first charge pump having an input coupled to the first power supply terminal of the first circuit and an output coupled to the second power supply terminal of the first circuit;
 - a second charge pump having an input coupled to the first power supply terminal of the second circuit and an output coupled to the second power supply terminal of the second circuit; and
 - a third charge pump having an input coupled to the first power supply terminal of the third circuit and an output coupled to the second power supply terminal of the third circuit.
8. The system of claim 7, wherein:
 - the third charge pump passes a current from the first power supply terminal of the third circuit to the second supply terminal of the third circuit if a current supplied by the second circuit to the second power supply terminal of the second circuit exceeds a maximum current requirement of the third circuit.
9. The system of claim 7, wherein:
 - the first charge pump provides a current to the second circuit if a current passing through the first circuit is less than a minimum current required for the second circuit.
10. A method, comprising:
 - providing a first circuit having a first power supply terminal coupled to positive power supply terminal, a second power supply terminal, and an input/output;
 - providing a second circuit having a first power supply terminal coupled the second power supply terminal of the first circuit, a second power supply terminal, and an input/output;
 - providing a third circuit having a first power supply terminal coupled the second power supply terminal of the second circuit, a second power supply terminal, and an input/output;
 - providing a first capacitor having a first terminal coupled to the input/output of the first circuit and a second terminal coupled to the input/output of the second circuit;
 - providing a second capacitor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the input/output of the third circuit;
 - precharging the first terminal of the first capacitor to a first voltage during a precharge phase, wherein the first voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the first circuit;
 - precharging the second terminal of the first capacitor and the first terminal of the second capacitor to a second voltage during the precharge phase, wherein the second voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the second circuit; and

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precharging the second terminal of the second capacitor to a third voltage during the precharge phase, wherein the third voltage is between a voltage present on the first power supply terminal and the second power supply terminal of the third circuit.

11. The method of claim **10**, further comprising: providing an output signal on the input/output of the first circuit; and

interpreting a voltage present on the second terminal of the first capacitor in response to the output signal being provided.

12. The method of claim **11**, wherein the step of interpreting is for determining a logic state of the output signal.

13. The method of claim **12**, further comprising interpreting a voltage present on the second terminal of the second capacitor in response to the output signal being provided.

14. The method of claim **11** further comprising: passing a current through the first circuit; determining if the current exceeds a maximum current requirement of the second circuit;

if the current exceeds the maximum current requirement, diverting a sufficient portion of the current away from the second circuit so that a remaining portion of the current does not exceed the maximum current requirement of the second circuit.

15. The method of claim **11**, wherein the step of diverting is performed by passing the sufficient portion of the current through a charge pump coupled in parallel with the second circuit.

16. The method of claim **11** further comprising: passing a current through the first circuit; determining if the current is less than a minimum current requirement of the second circuit; and

if the current is less than the minimum current requirement, adding an additional current to the first current so that a sum of the additional current and the first current is not less than the minimum current requirement of the second circuit.

17. The method of claim **16**, wherein the step of adding is performed by providing the additional current from a charge pump coupled in parallel with the first circuit.

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18. A system, comprising:

a plurality of circuits having serially connected power supply terminals coupled between a positive power supply terminal and a negative power supply terminal; and a plurality of capacitors coupled in series; wherein:

at a first end of the plurality of capacitors, a first capacitor has a terminal;

at a second end of the plurality of capacitors, a last capacitor has a terminal;

each circuit of the plurality of circuits has a first power supply terminal, a second power supply terminal, and an input/output;

a first circuit of the plurality of circuits has its input/output coupled to the terminal of the first capacitor and is for precharging the terminal of the first capacitor during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the terminal of the first capacitor during a data phase following the precharge phase;

a last circuit of the plurality of circuits has its input/output coupled to the terminal of the last capacitor and is for precharging the terminal of the last capacitor during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the terminal of the last capacitor during a data phase following the precharge phase; and

each circuit of the plurality of circuits between the first and last circuits has its input/output coupled to a connection between two capacitors of the plurality of capacitors and is for precharging the connection at its input/output during a precharge phase to a voltage between its first and second power supply terminals and receiving or providing data on the connection at its input/output during a data phase following the precharge phase.

19. The system of claim **18**, further comprising:

a plurality of charge pumps, wherein each charge pump is coupled in parallel with one of the circuits of the plurality of circuits.

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