US008169017B2

(12) **United States Patent**
Ema et al.

(10) **Patent No.: US 8,169,017 B2**
(45) **Date of Patent: May 1, 2012**

(54) SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

(75) Inventors: **Taija Ema**, Kawasaki (JP); **Toru Anezaki**, Kawasaki (JP)

(73) Assignee: **Fujitsu Semiconductor Limited**, Yokohama (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 111 days.

(21) Appl. No.: **12/285,275**

(22) Filed: **Oct. 1, 2008**

(65) **Prior Publication Data**

US 2009/0045451 A1 Feb. 19, 2009

Related U.S. Application Data

(62) Division of application No. 11/044,458, filed on Jan. 28, 2005, now Pat. No. 7,445,989.

(30) **Foreign Application Priority Data**

Oct. 29, 2004 (JP) 2004-316974

(51) **Int. Cl.**
H01L 29/788 (2006.01)

(52) **U.S. Cl.** **257/315**; 257/E29.129

(58) **Field of Classification Search** 257/315, 257/316, E29.129
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,852,311	A	12/1998	Kwon et al.	
5,879,983	A	3/1999	Segawa et al.	
6,124,160	A	9/2000	Segawa et al.	
6,335,244	B1 *	1/2002	Ikeda	438/257
6,373,093	B2 *	4/2002	Fujii et al.	257/314
6,489,650	B2 *	12/2002	Kumazaki	257/318
6,492,672	B1	12/2002	Segawa et al.	
6,680,510	B2	1/2004	Ikeda	
6,933,569	B2	8/2005	Koh et al.	
6,964,896	B2 *	11/2005	Gonzalez	438/241
7,235,476	B2 *	6/2007	Nakagawa	438/622
7,259,419	B2 *	8/2007	Koo et al.	257/314
2001/0004120	A1 *	6/2001	Colclaser et al.	257/326
2002/0011616	A1	1/2002	Inoue et al.	
2003/0022445	A1	1/2003	Taniguchi et al.	
2003/0030096	A1 *	2/2003	Hsu	257/314
2003/0127681	A1 *	7/2003	Nishioka et al.	257/315

(Continued)

FOREIGN PATENT DOCUMENTS

JP	6-97457 A	4/1994

(Continued)

OTHER PUBLICATIONS

Japanese Office Action mailed Mar. 16, 2010, issued in corresponding Japanese Patent Application No. 2004-316974.

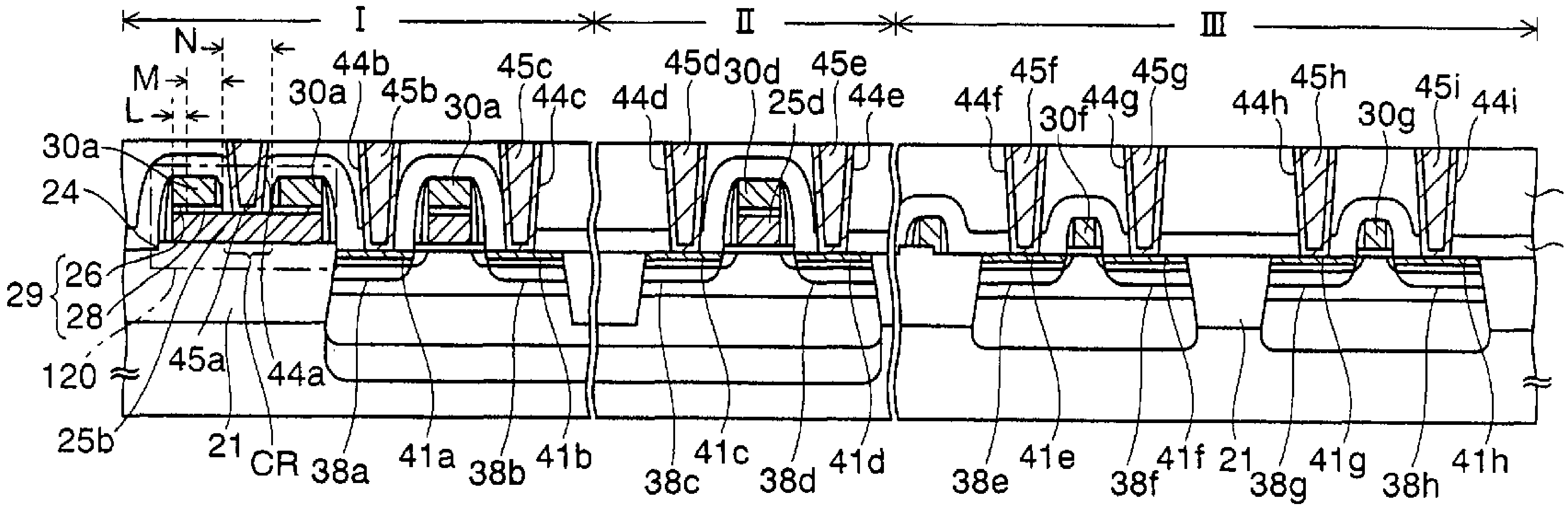
Primary Examiner — Allan R Wilson

(74) *Attorney, Agent, or Firm* — Westerman, Hattori, Daniels & Adrian, LLP

(57) ABSTRACT

A method of manufacturing a semiconductor device that comprises the steps of: removing a second insulating film on a contact region of a first conductor; forming a second conductive film on the second insulating film; removing the second conductive film on the contact region of the first conductor to make the second conductive film into a second conductor; forming an interlayer insulating film (a third insulating film) covering the second conductor; forming a first hole in the interlayer insulating film on the contact region; and forming a conductive plug, which is electrically connected with the contact region, in the first hole.

11 Claims, 69 Drawing Sheets



U.S. PATENT DOCUMENTS

2004/0033664	A1 *	2/2004	Park	438/264
2004/0124477	A1	7/2004	Mimami et al.	
2004/0219755	A1 *	11/2004	Rabkin et al.	438/299
2005/0269663	A1	12/2005	Minami et al.	
2009/0122609	A1 *	5/2009	Okazaki et al.	365/185.05

FOREIGN PATENT DOCUMENTS

JP	09-082896	A	3/1997
JP	10-56161	A	2/1998
JP	10-189954	A	7/1998
JP	11-31799	A	2/1999
JP	11-219595	A	8/1999
JP	2000-269465	A	9/2000
JP	2003-37169	A	2/2003
JP	2003-100887	A	4/2003
JP	2003-124356	A	4/2003
JP	2003-158242	A	5/2003
JP	2004-55763	A	2/2004

* cited by examiner

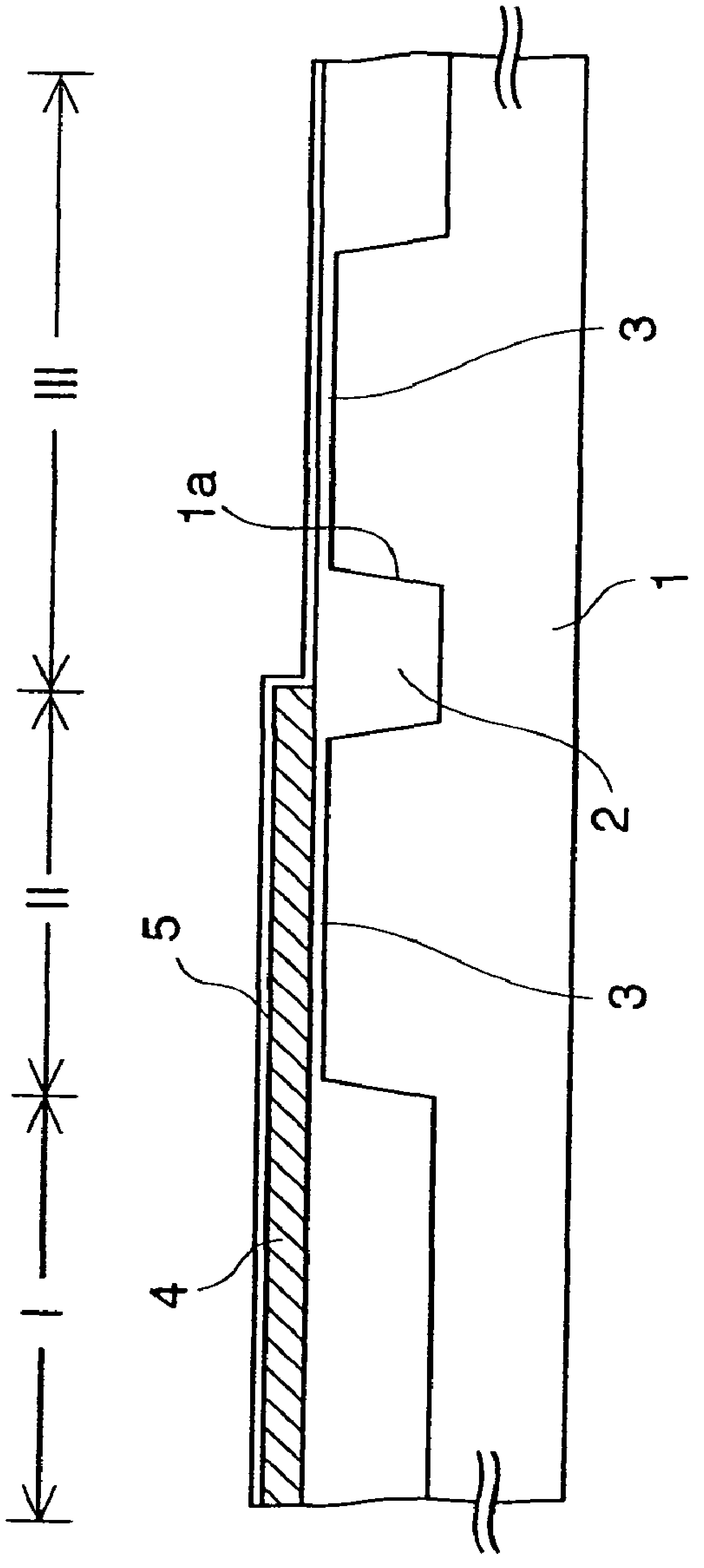


FIG. 1A

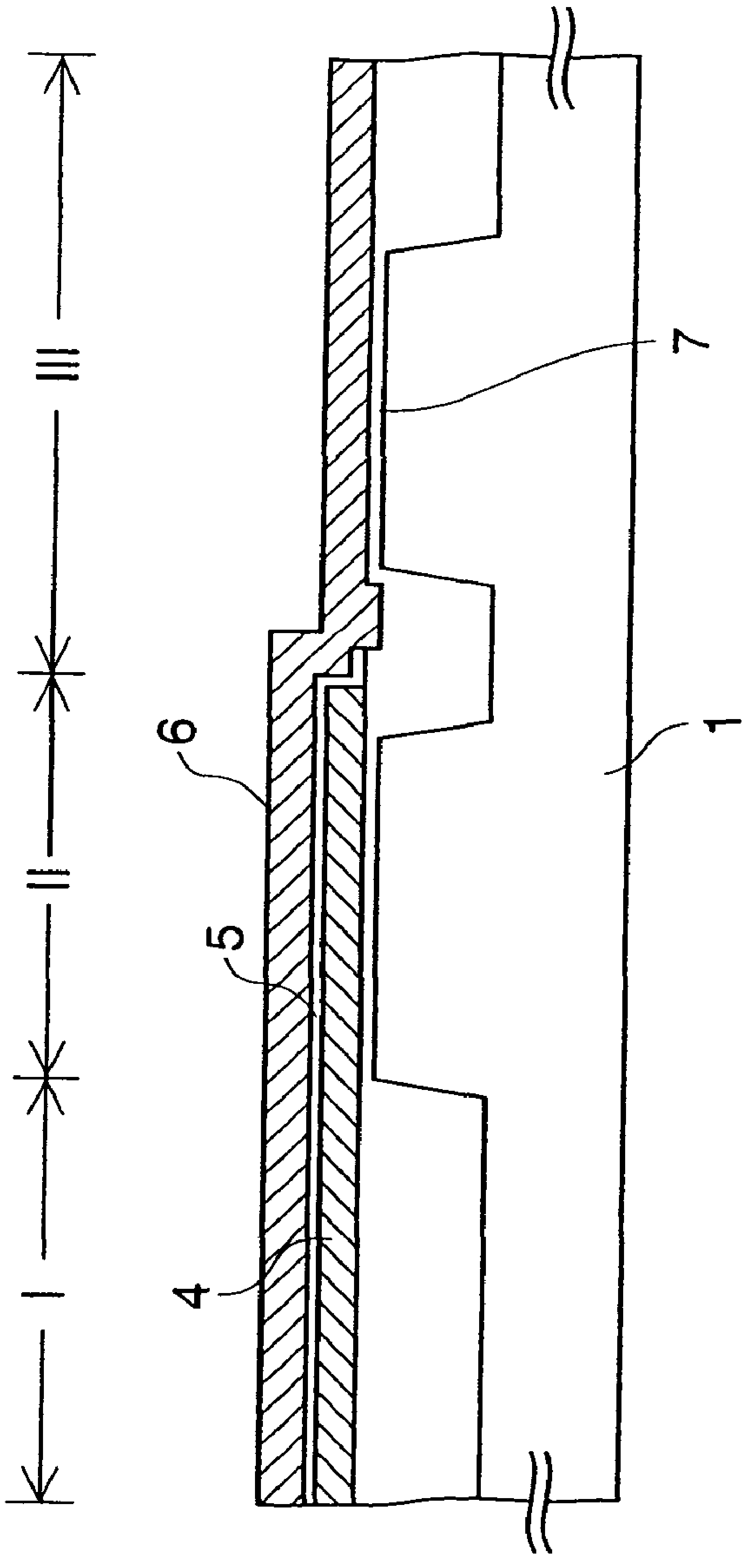


FIG. 1B

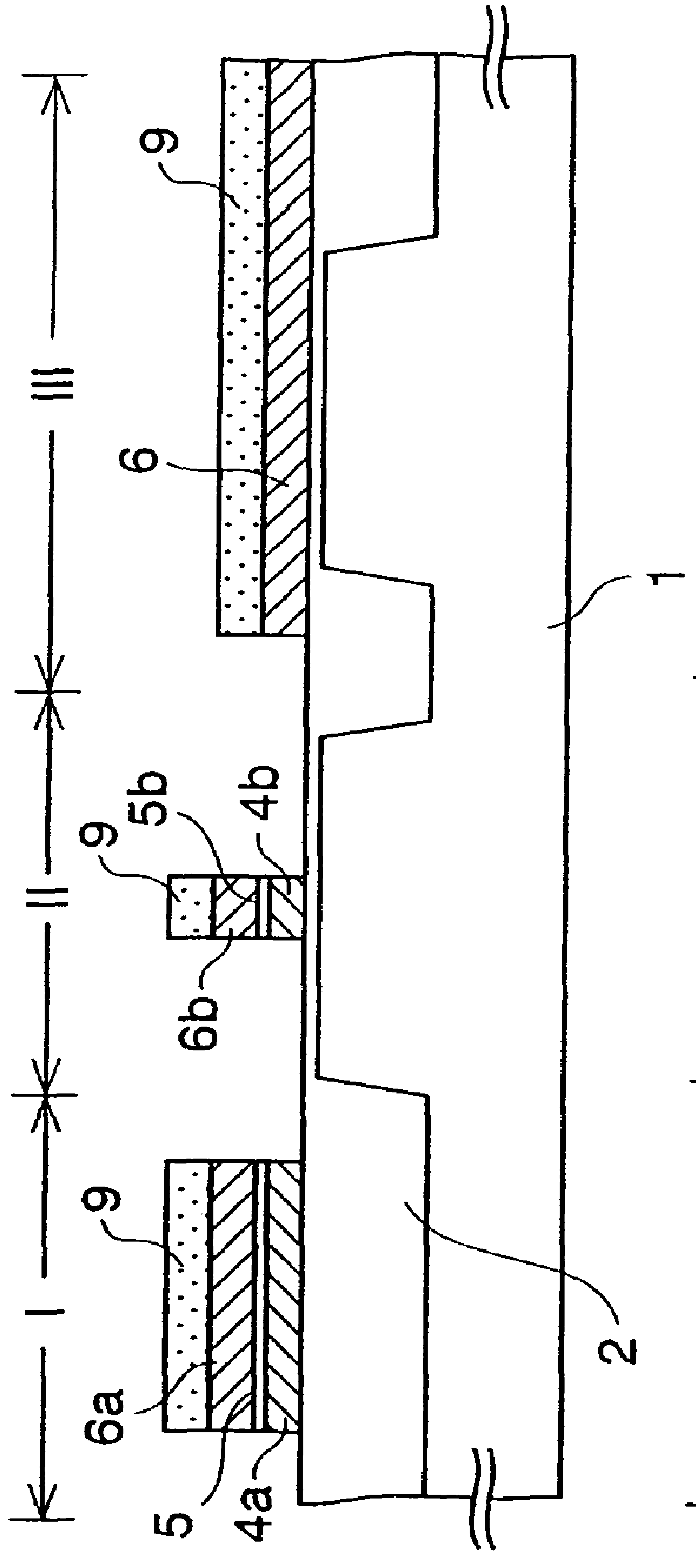


FIG. 1C

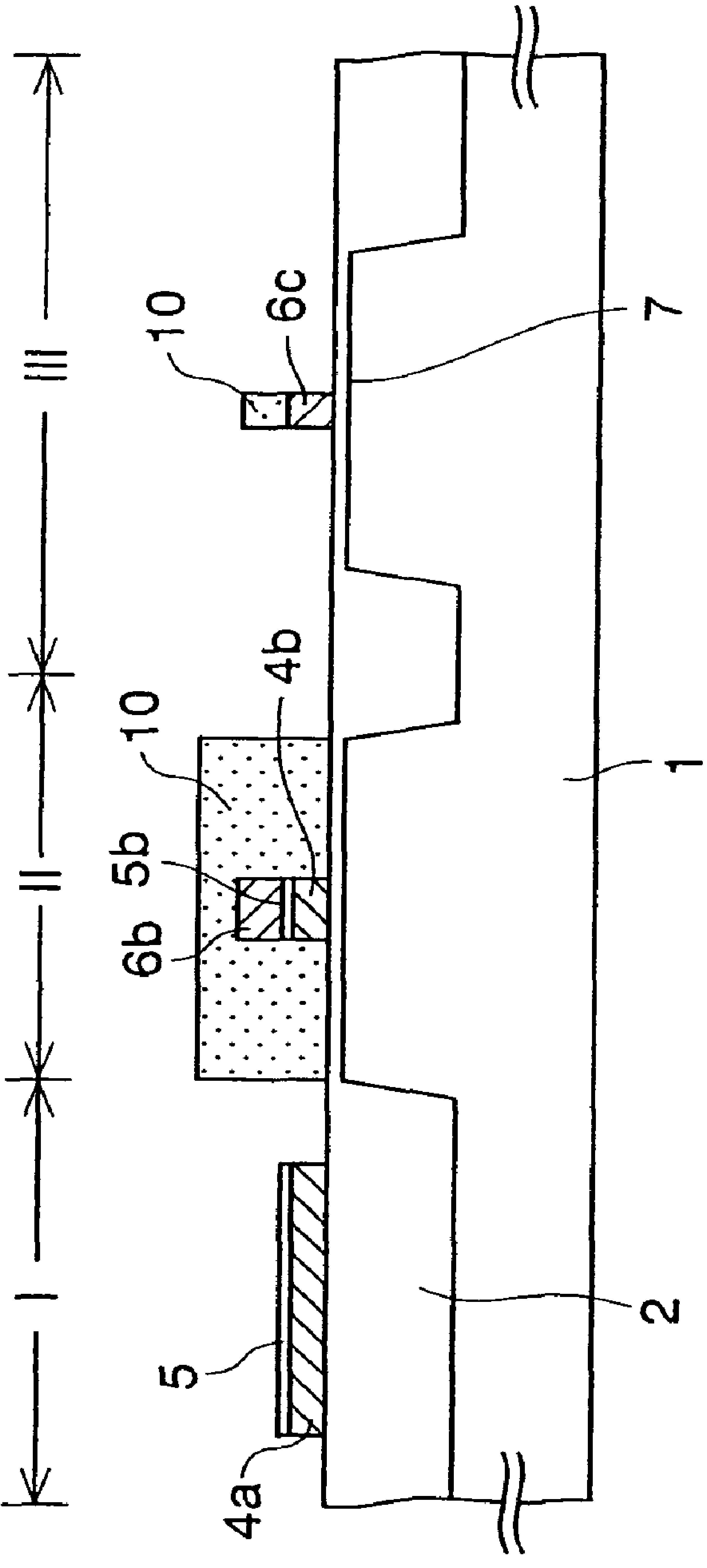


FIG. 1D

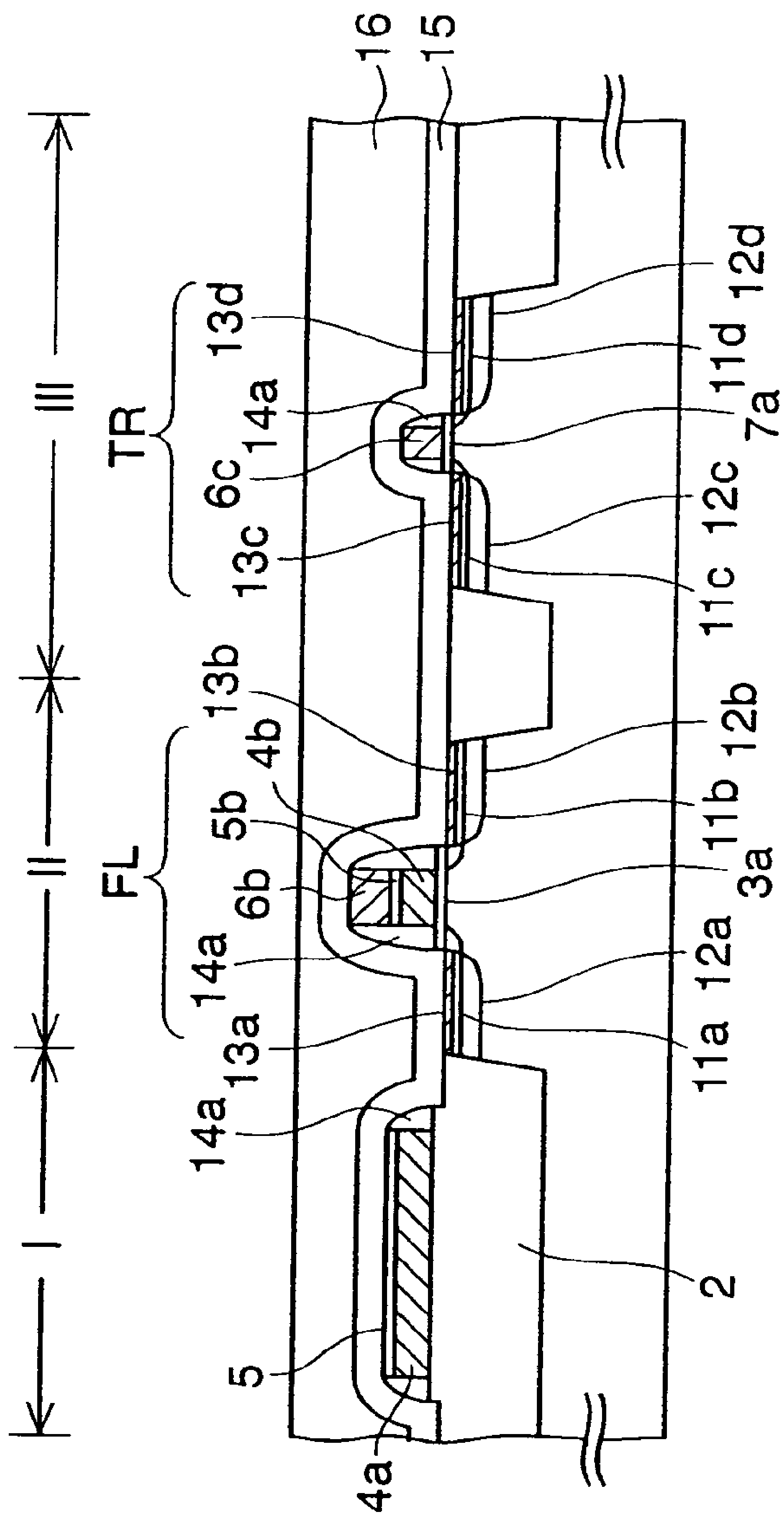

16
15
13d
12d
11d
14a
7a
TR
6c
13c
12c
11c
III
II
I
13b
4b
12b
5b
11b
FL
6b
3a
14a
12a
13a
11a
14a
5
2
4a

FIG. 1E

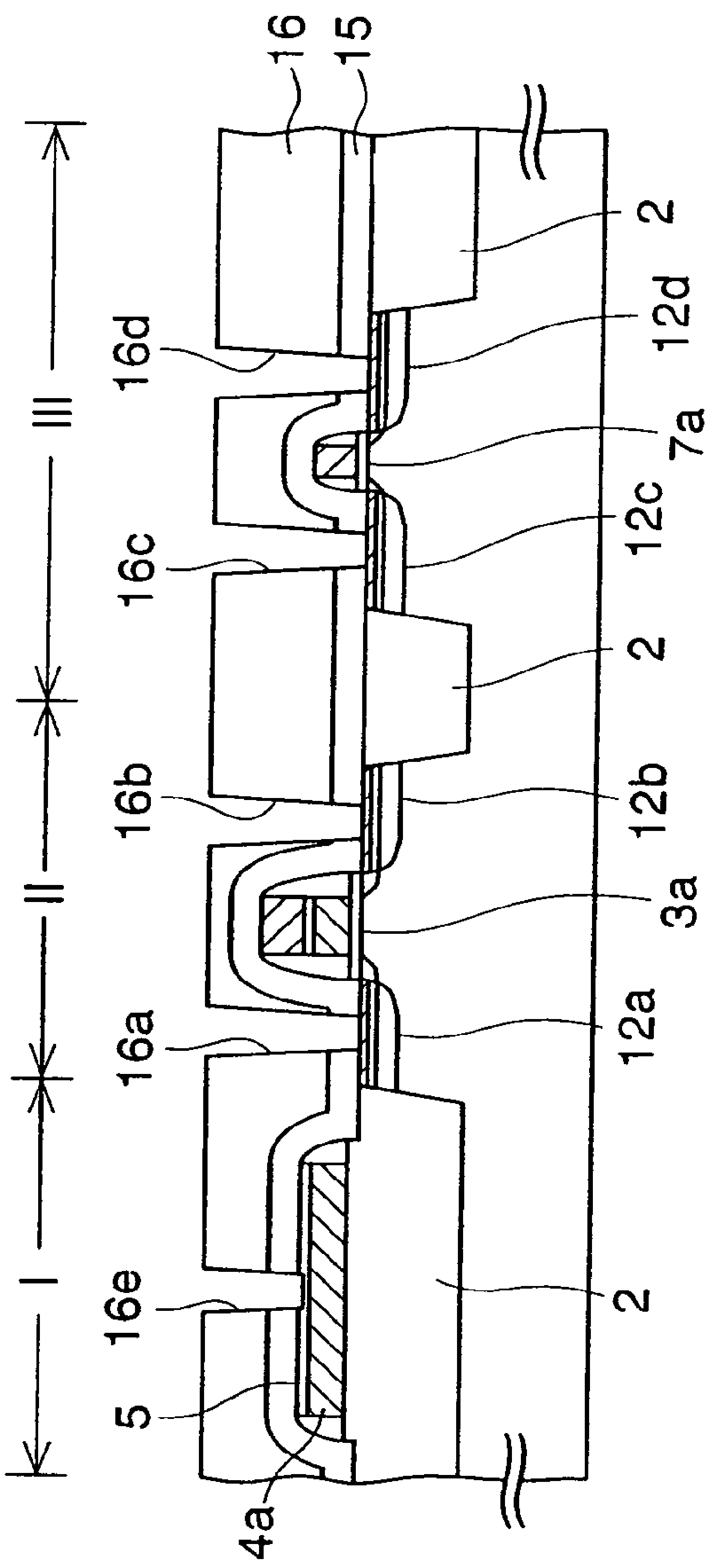

16
15
2
16d
12d
7a
III
16c
12c
2
16b
12b
3a
II
16a
12a
I
16e
2
5
4a

FIG. 1F

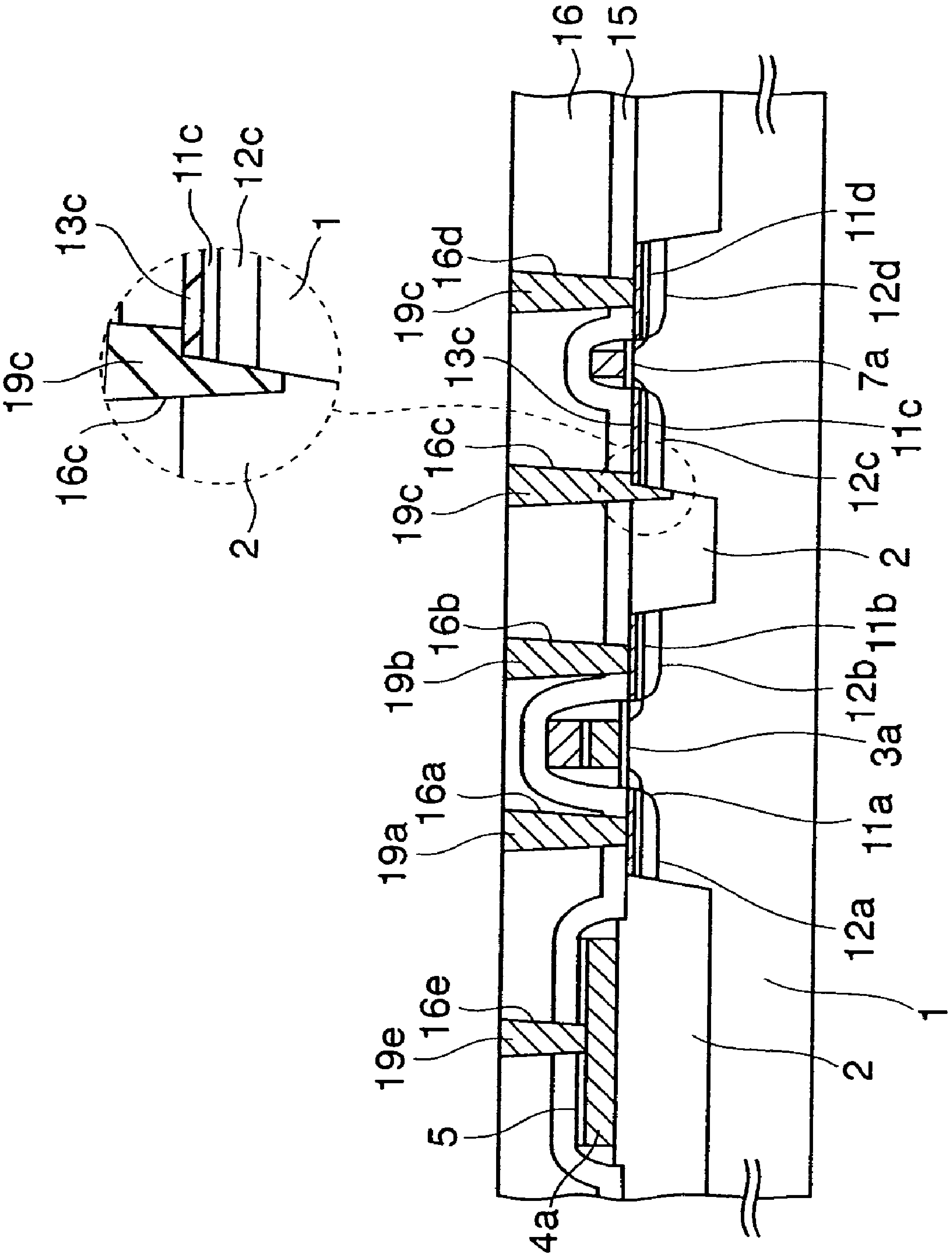

16
15
13c
11c
12c
1
19c
16c
2
16d
19c
12d
11d
13c
7a
16c
11c
12c
19c
2
16b
19b
11b
12b
3a
16a
19a
11a
12a
16e
19e
5
4a
2
1

FIG. 1G

FIG. 2A

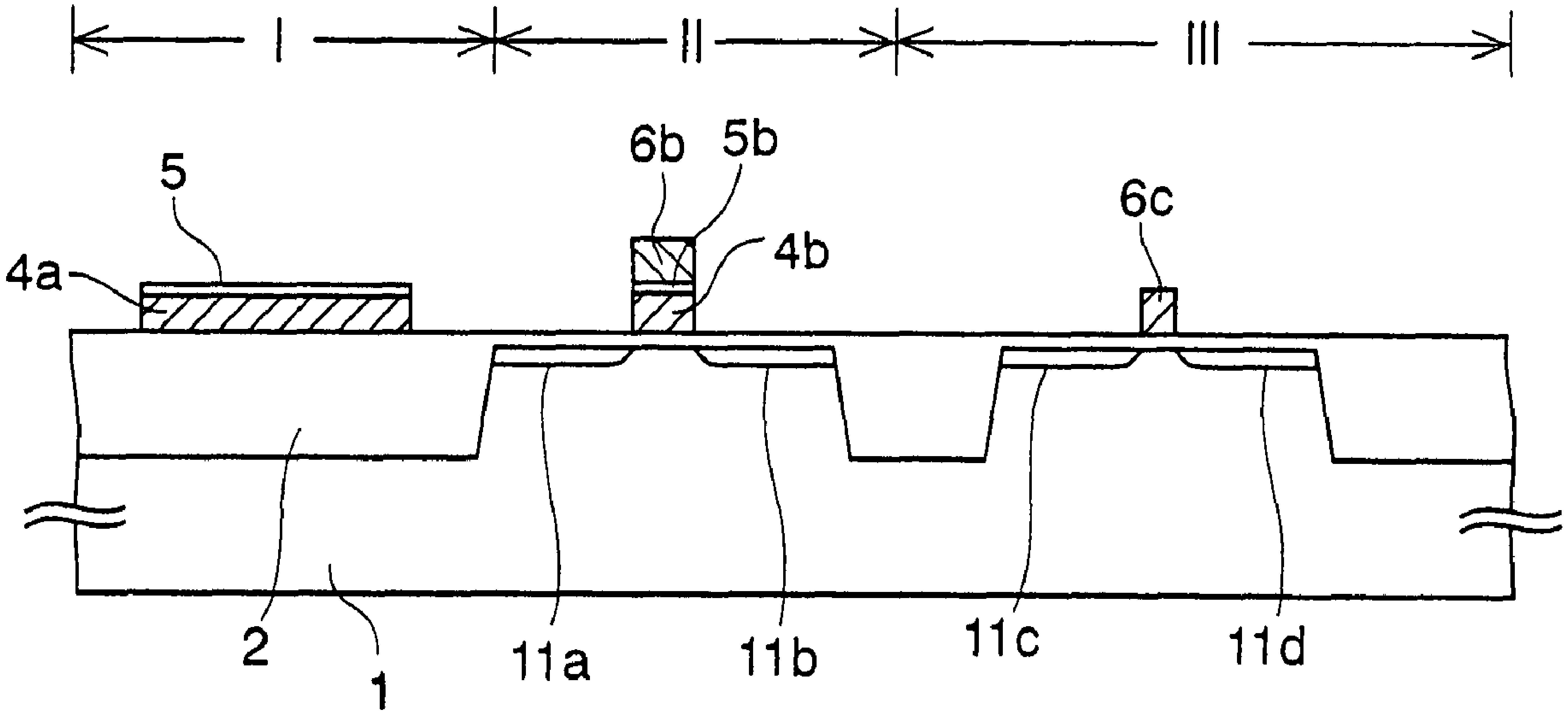
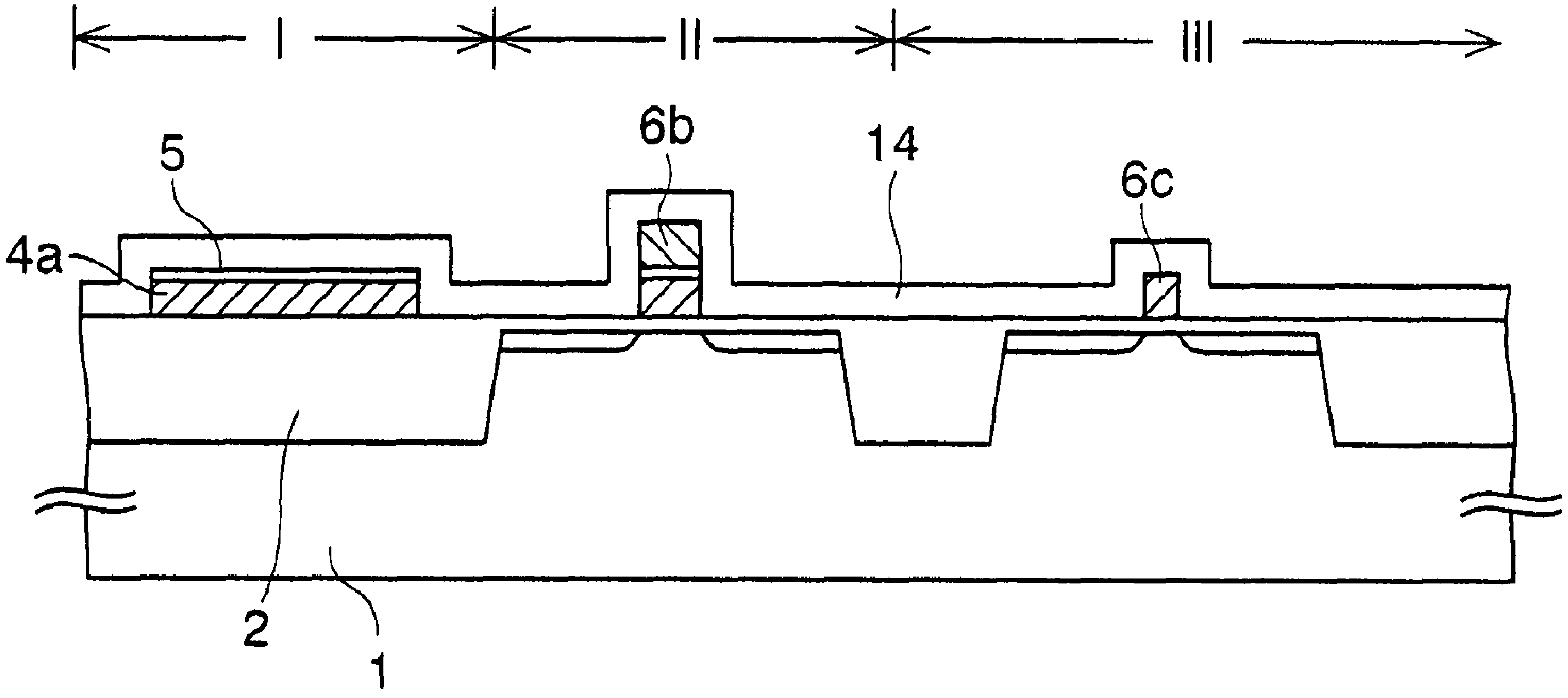


FIG. 2B



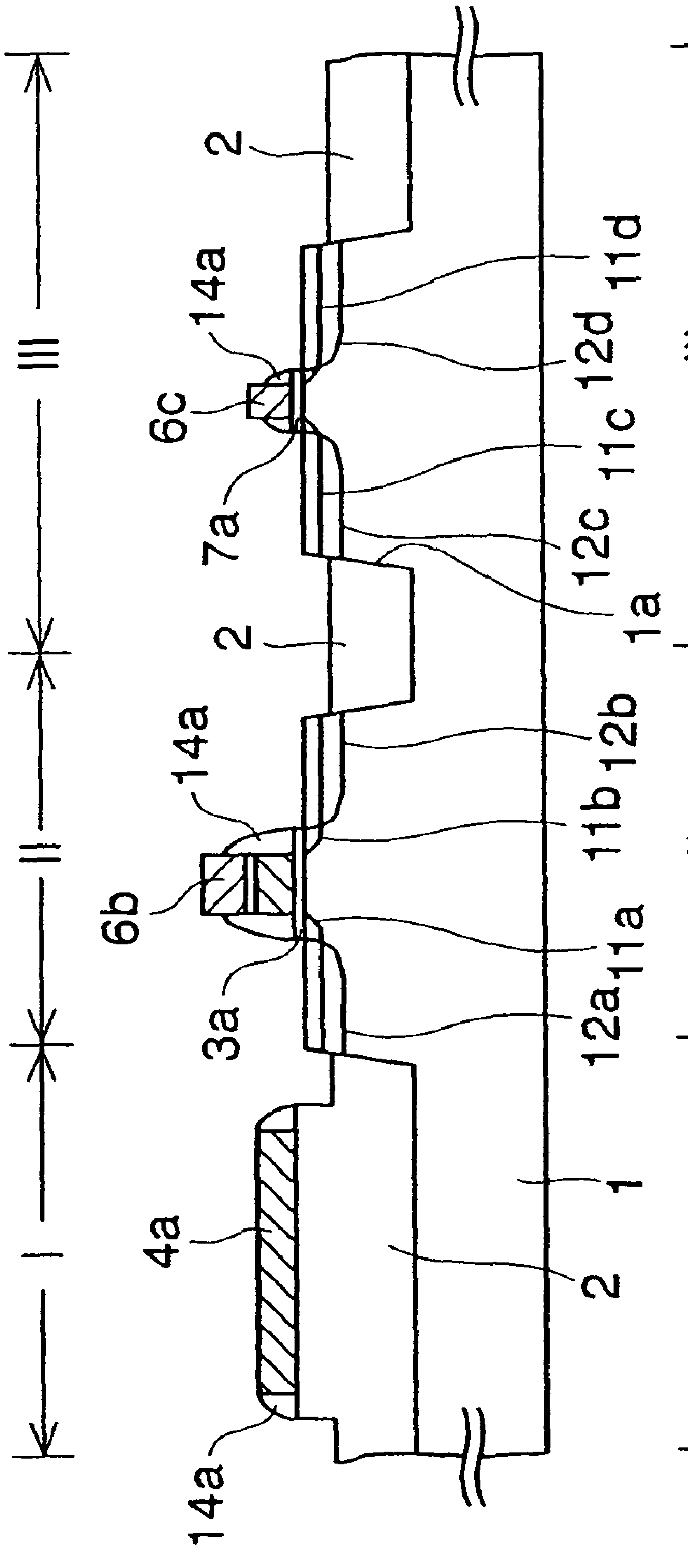

I
II
III
14a
4a
2
1
3a
6b
14a
12a
11a
11b
12b
2
1a
7a
6c
14a
12c
11c
12d
11d
2

FIG. 2C

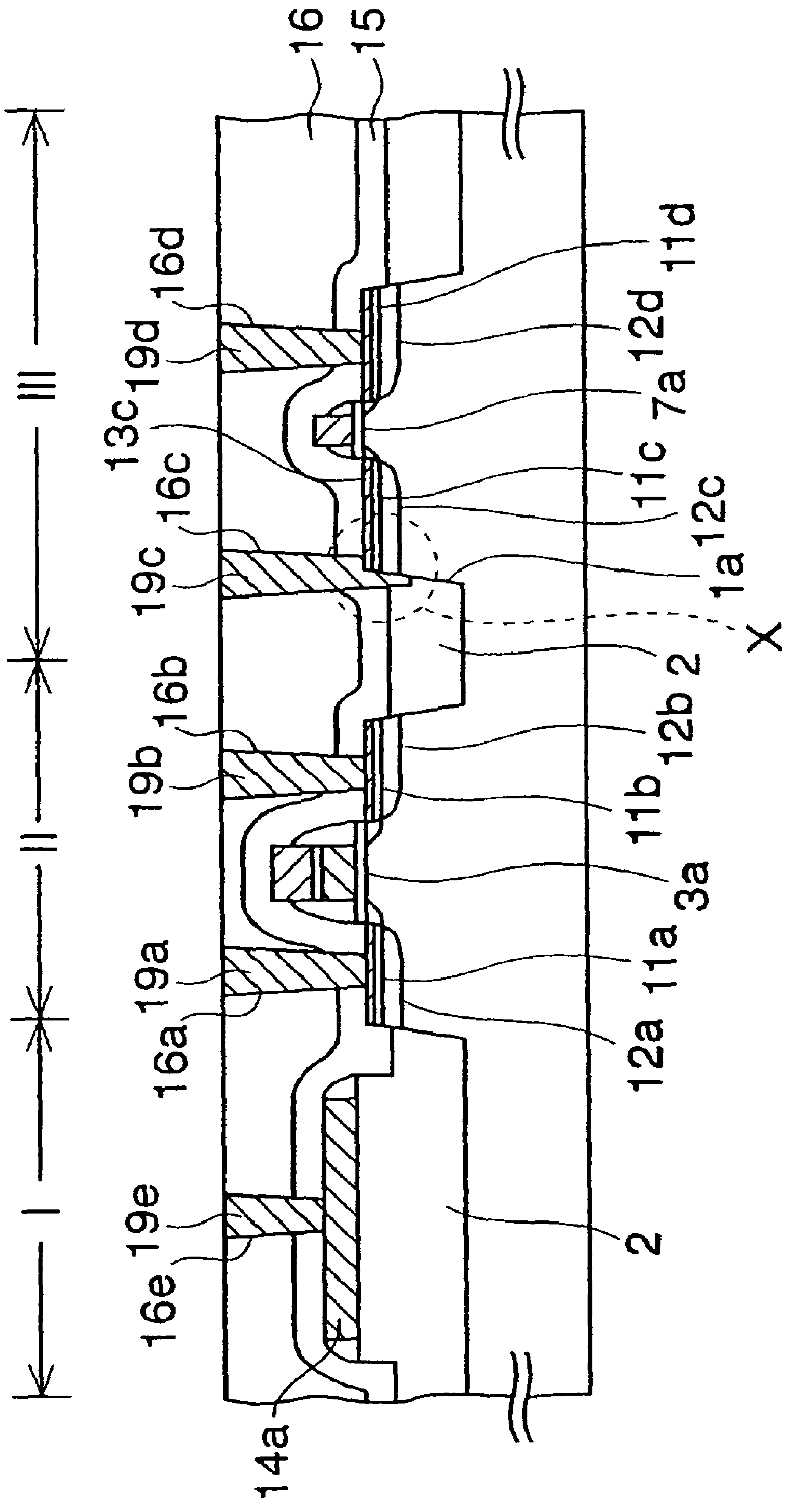

I
II
III
14a
16e
19e
2
16a
19a
12a
11a
3a
19b
16b
11b
12b
2
19c
16c
X
1a
12c
11c
13c
19d
16d
7a
12d
11d
16
15

FIG. 2D

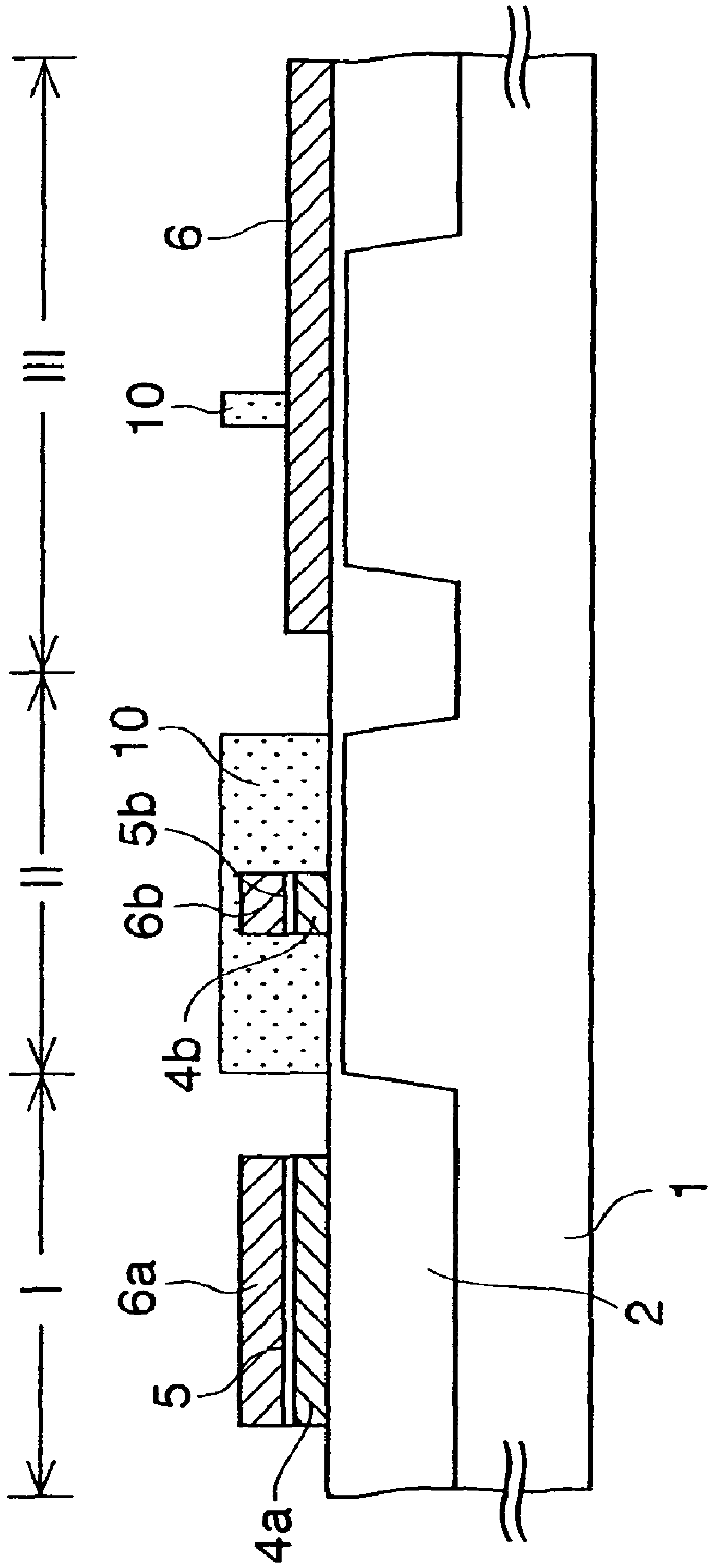


FIG. 3A

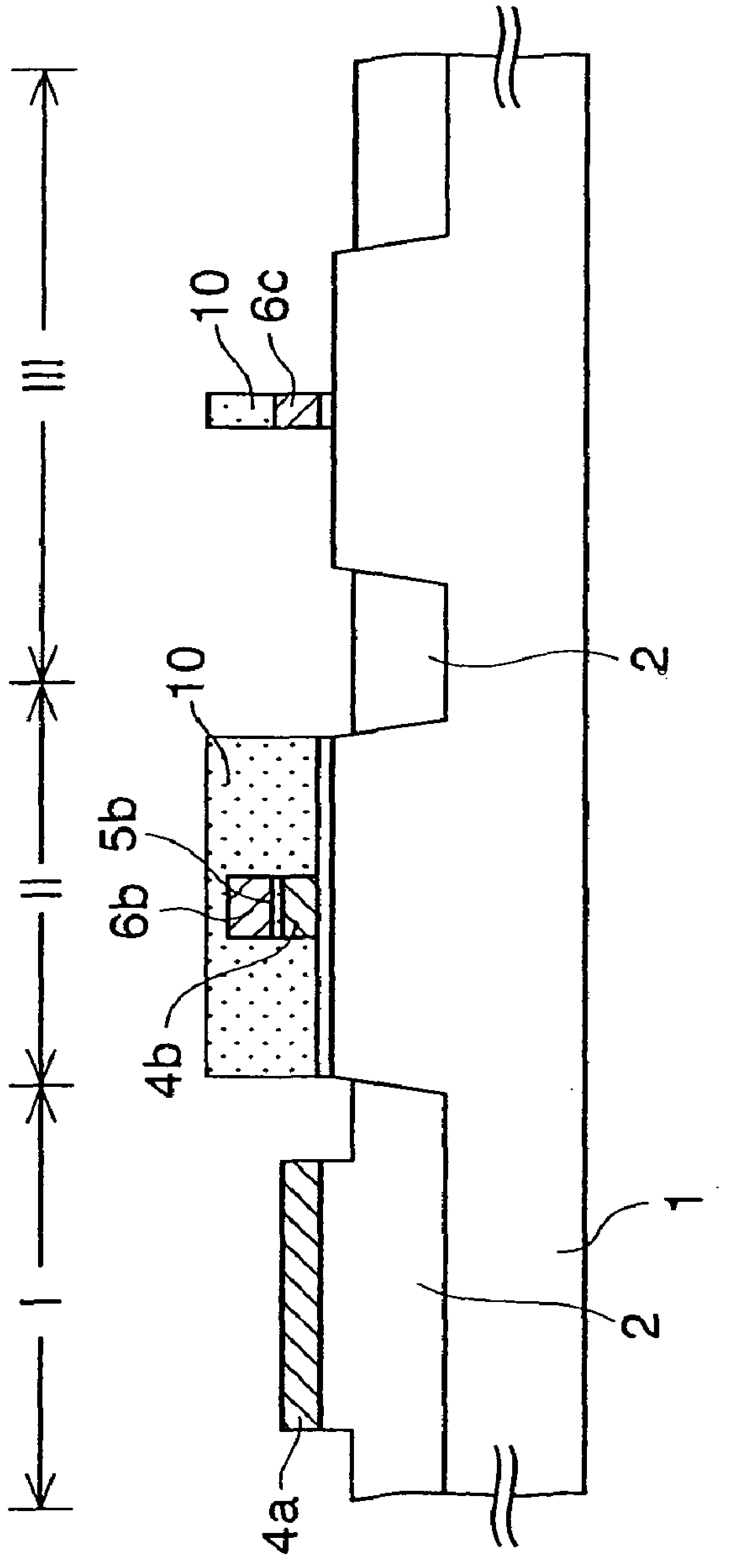


FIG. 3B

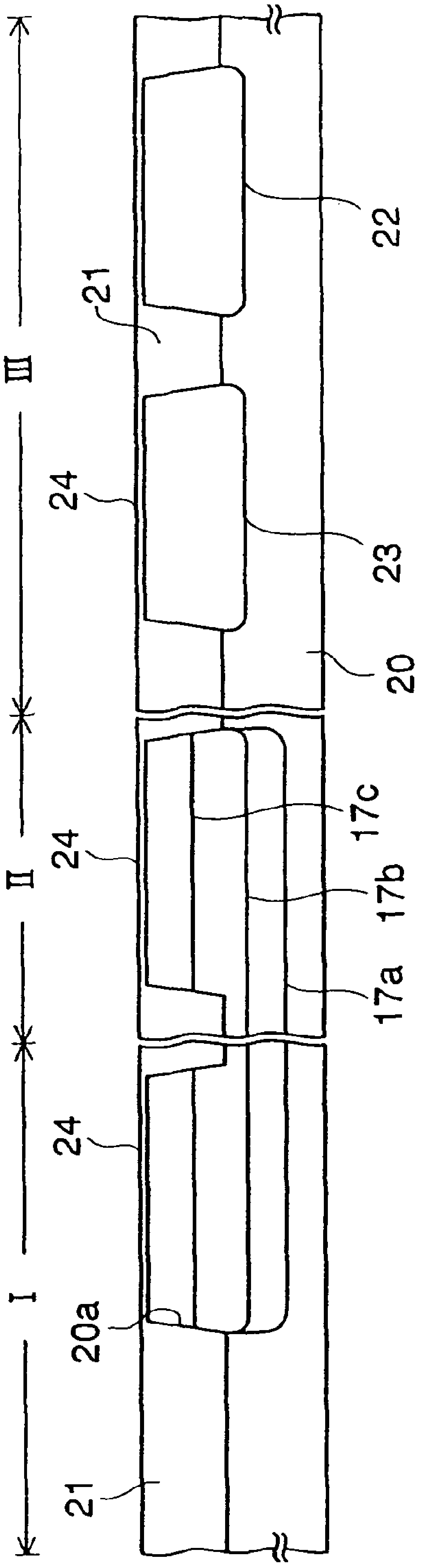

III
21
22
24
23
20
II
24
17c
17b
17a
I
24
20a
21

FIG. 4A

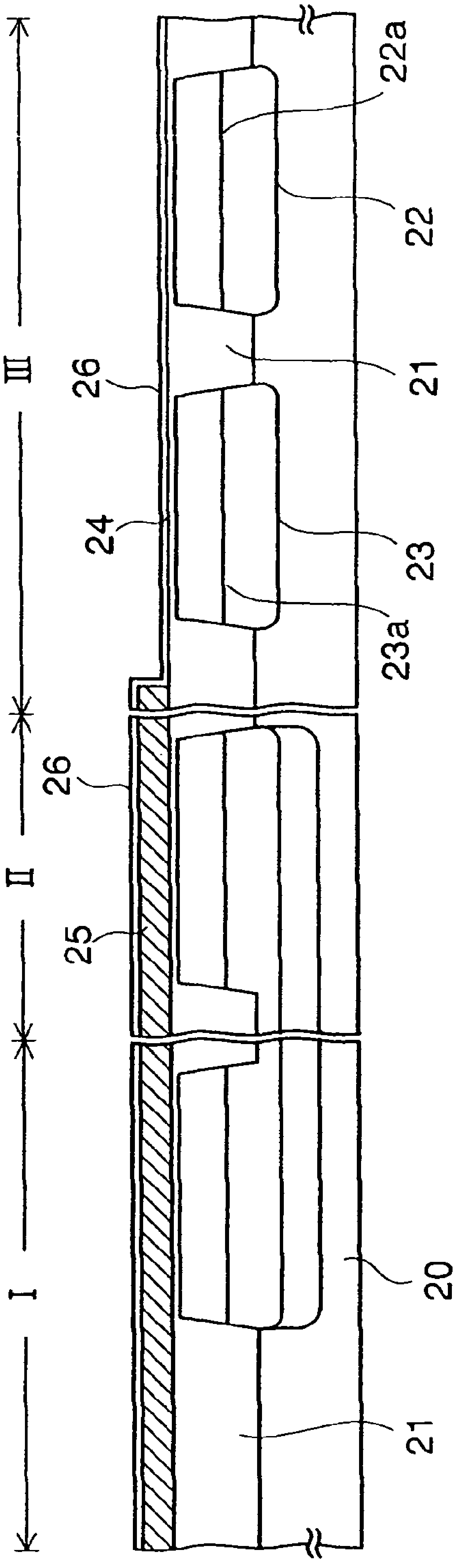

III
22a
22
26
21
24
23
23a
II
26
25
I
20
21

FIG. 4B

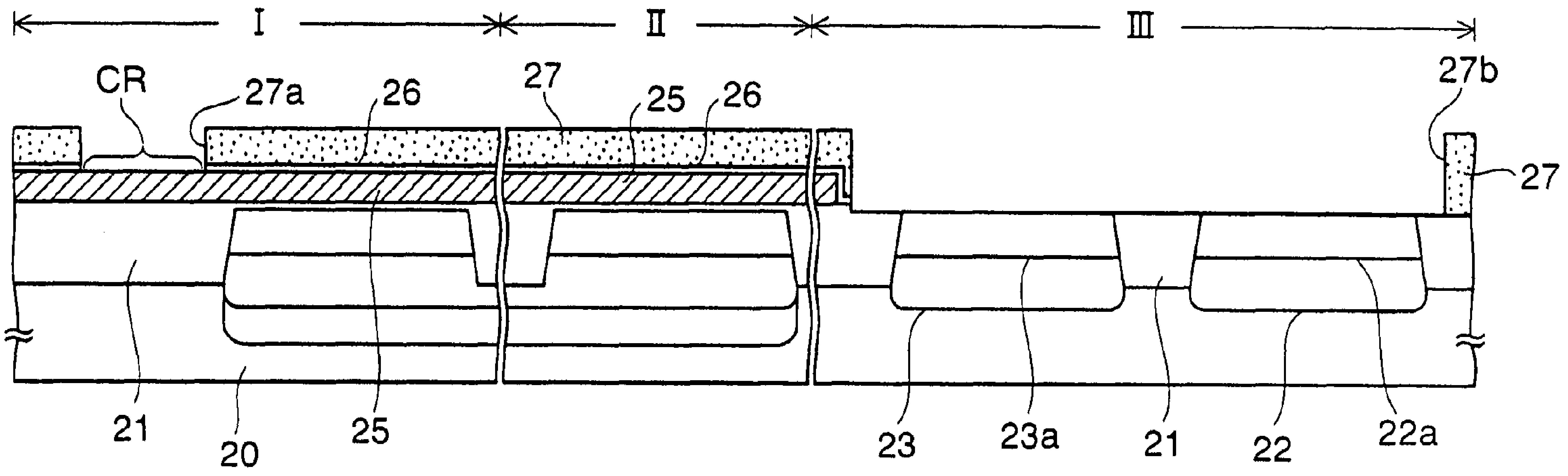

I
II
III
CR
27a
26
27
25
26
27b
27
21
20
25
23
23a
21
22
22a

FIG. 4C

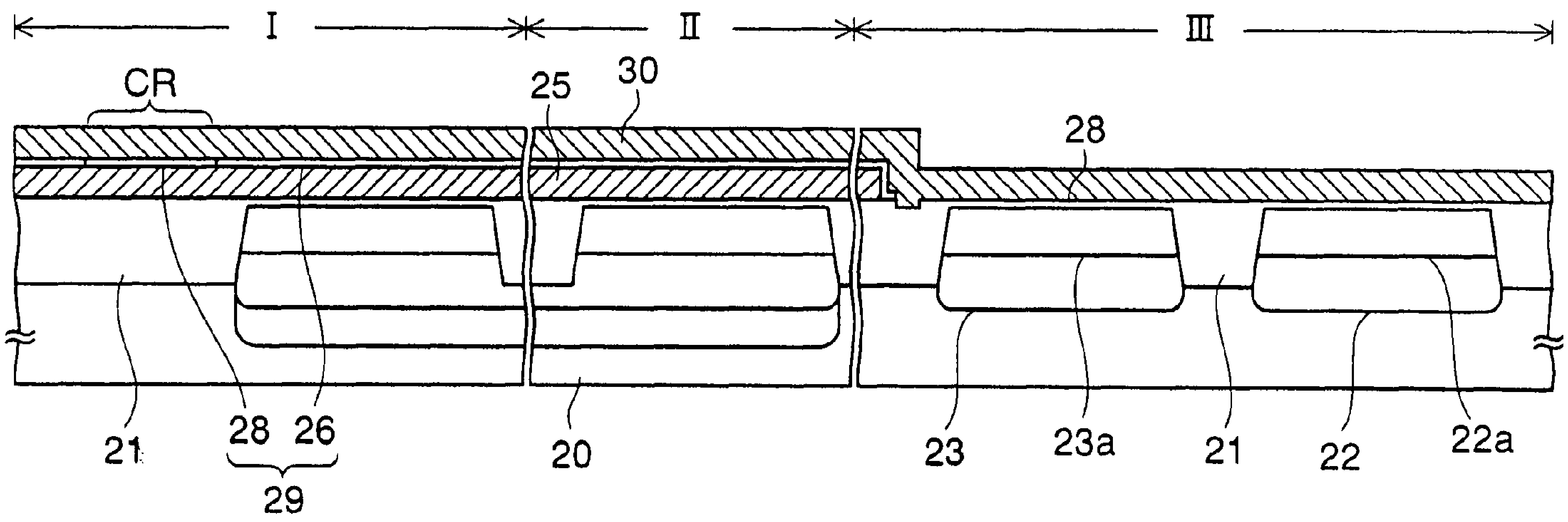

I
II
III
CR
25
30
28
21
28
26
29
20
23
23a
21
22
22a

FIG. 4D

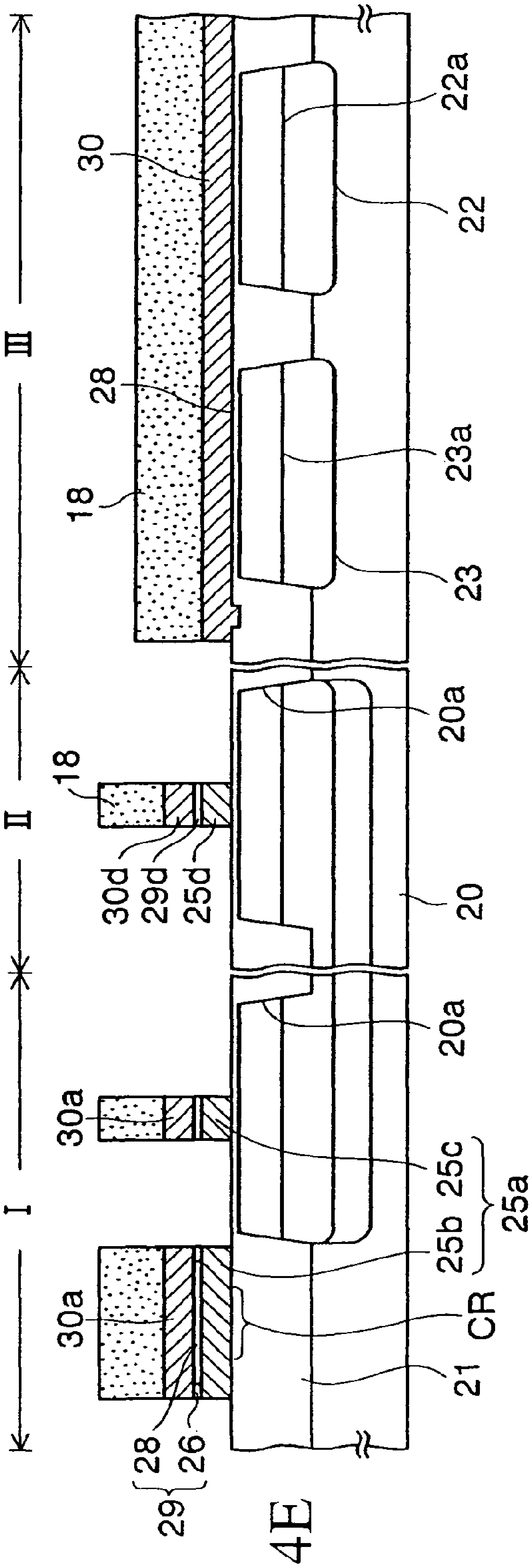

I
II
III
30
28
18
22a
22
23a
23
20a
20
18
30d
29d
25d
20a
30a
25c
25b
25a
30a
CR
21
28
26
29

FIG. 4E

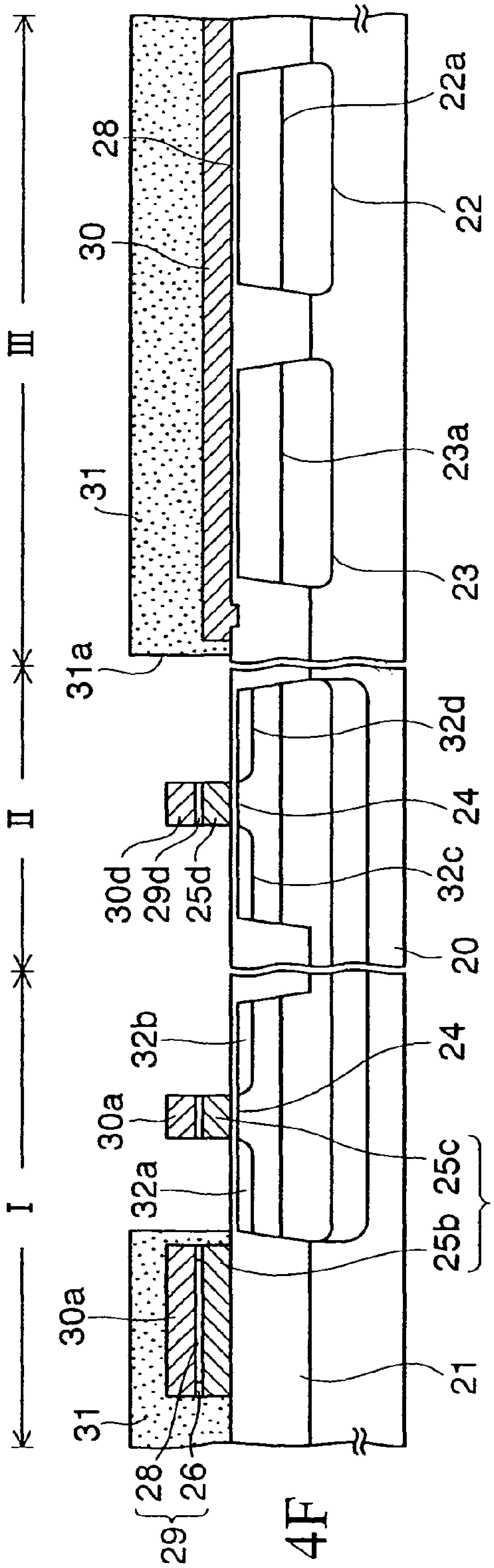

I
II
III
28
30
31
31a
22a
22
23a
23
32d
24
32c
30d
29d
25d
20
32b
24
30a
32a
25c
25b
25a
30a
21
31
28
26
29

FIG. 4F

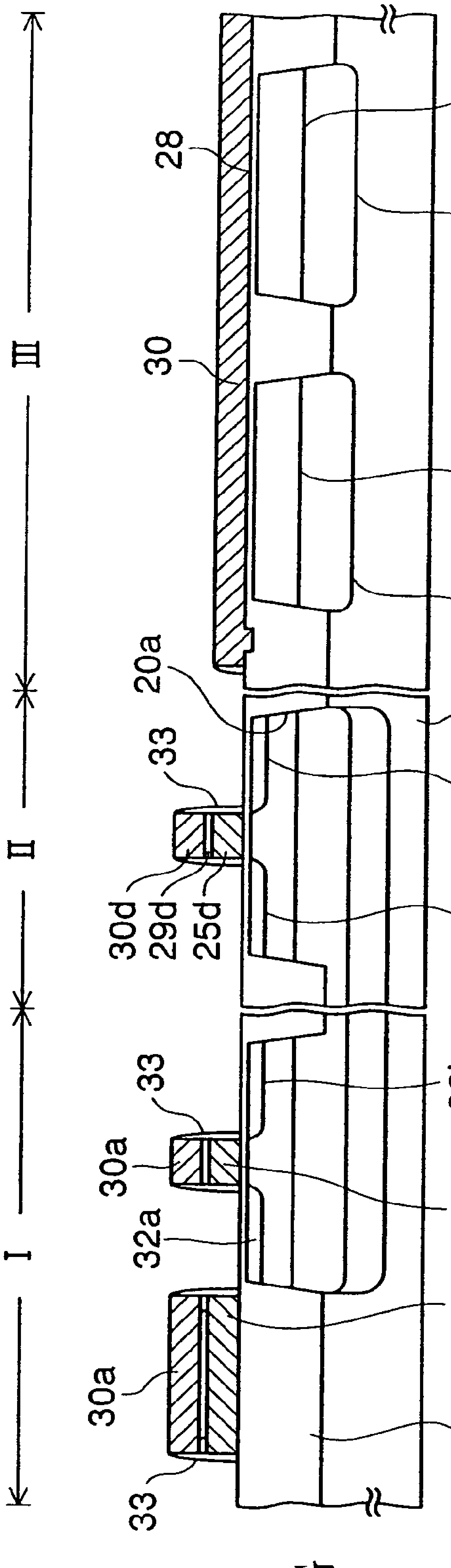

I
II
III
28
30
22a
22
23a
23
20a
20
33
32d
30d
29d
25d
32c
32b
33
30a
25c
32a
25b
25c
25a
30a
21
33

FIG. 4G

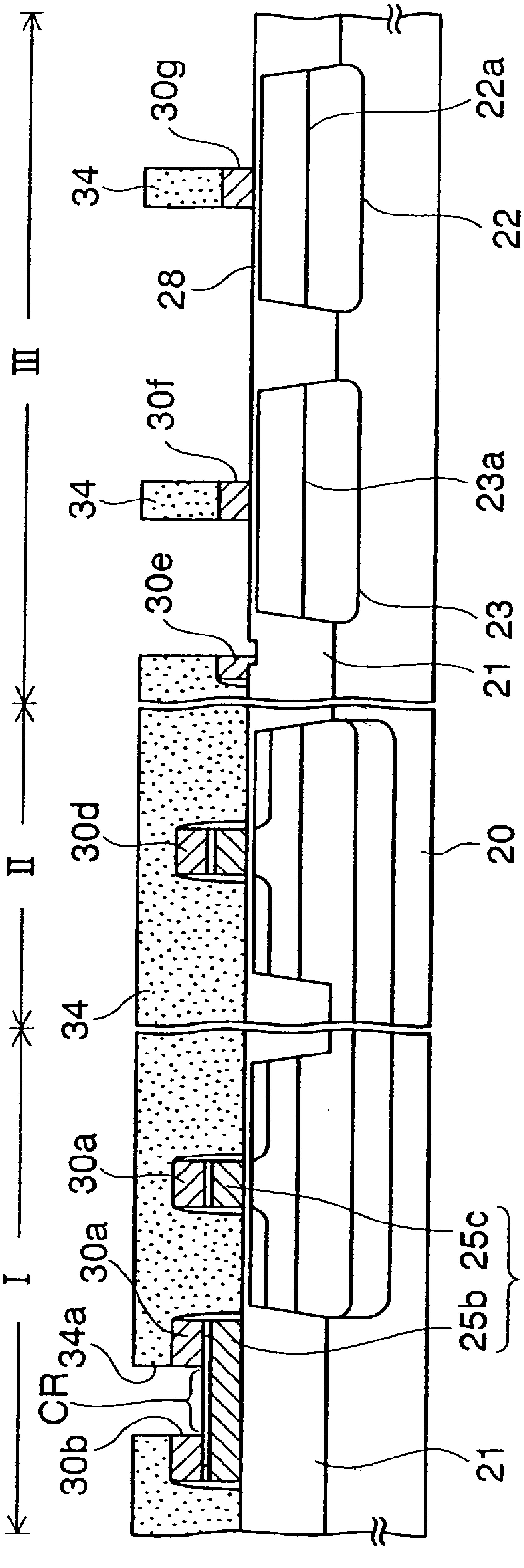

I
II
III
30g
34
22a
22
28
30f
34
23a
30e
23
21
20
30d
34
30a
25c
30a
34a
25b
25c
25a
CR
30b
21

FIG. 4H

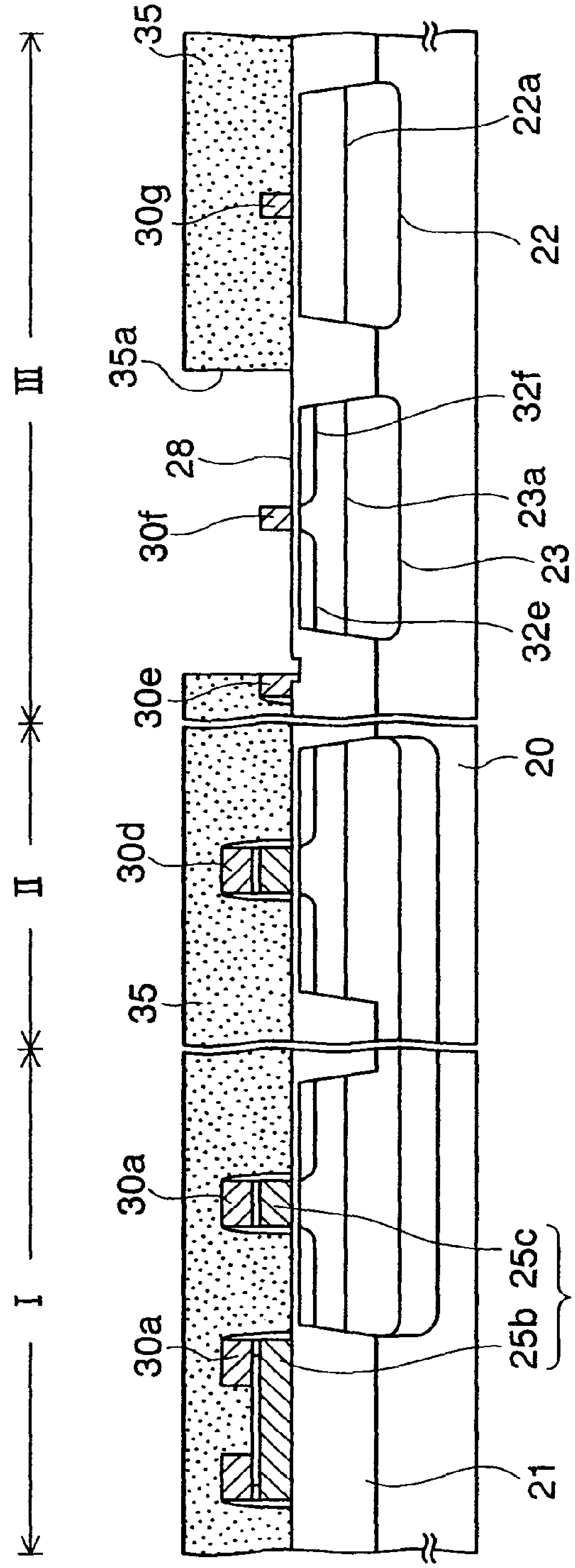

35
30g
35a
III
28
30f
30e
30d
II
35
30a
I
30a
22a
22
32f
23a
23
32e
20
25c
25b
25a
21

FIG. 4I

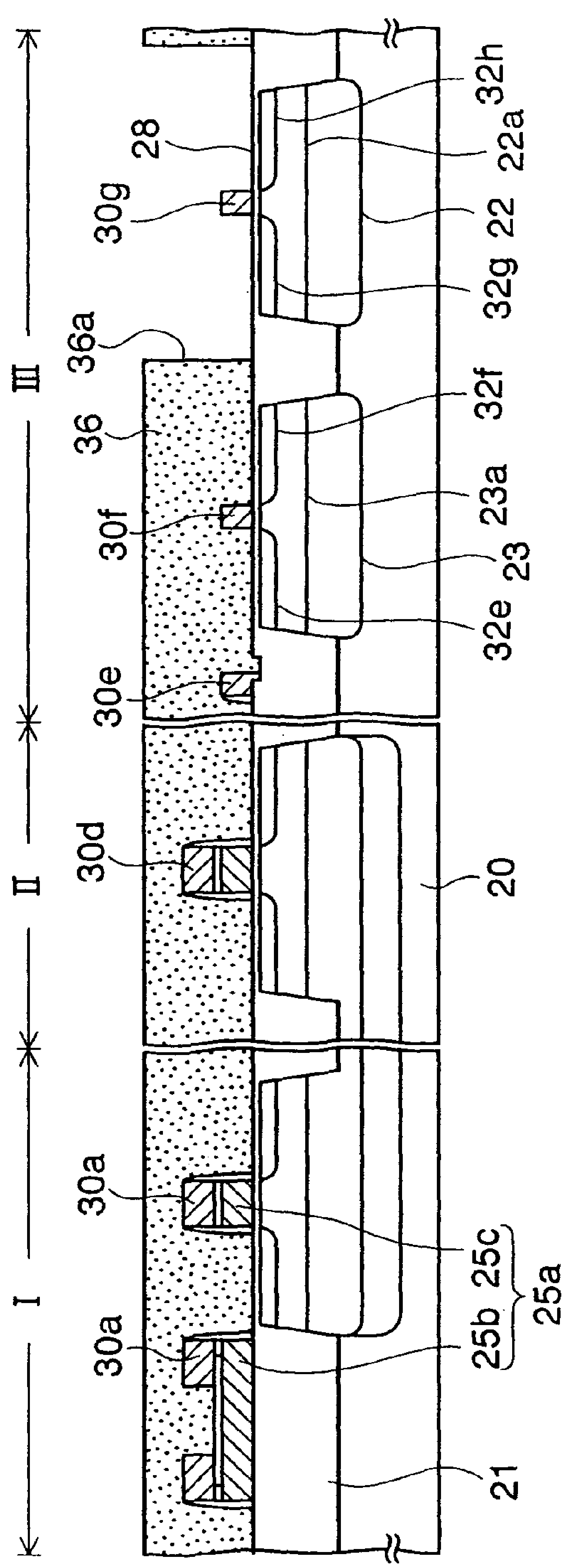

28
30g
36a
III
36
30f
30e
30d
II
30a
I
30a
32h
22a
22
32g
32f
23a
23
32e
20
25c
25b
25a
21

FIG. 4J

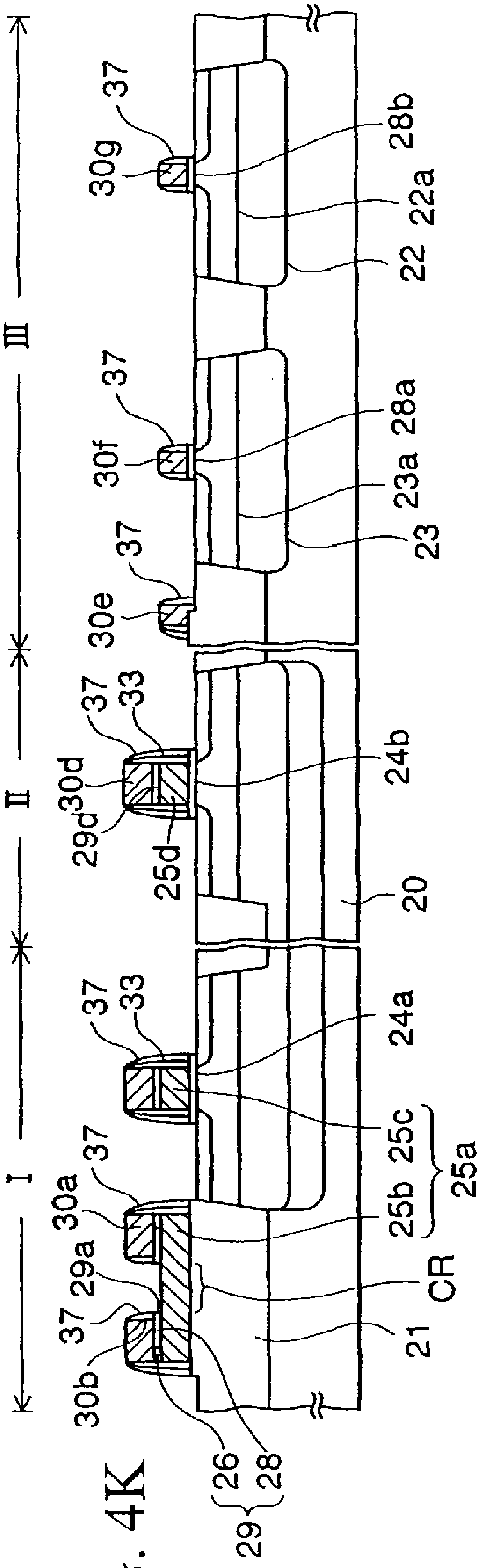

I
II
III
30b
37
29a
30a
37
37
33
25d
29d
30d
37
33
30e
37
30f
37
30g
37
26
28
29
21
CR
25b
25c
25a
24a
20
24b
23
23a
28a
22
22a
28b

FIG. 4K

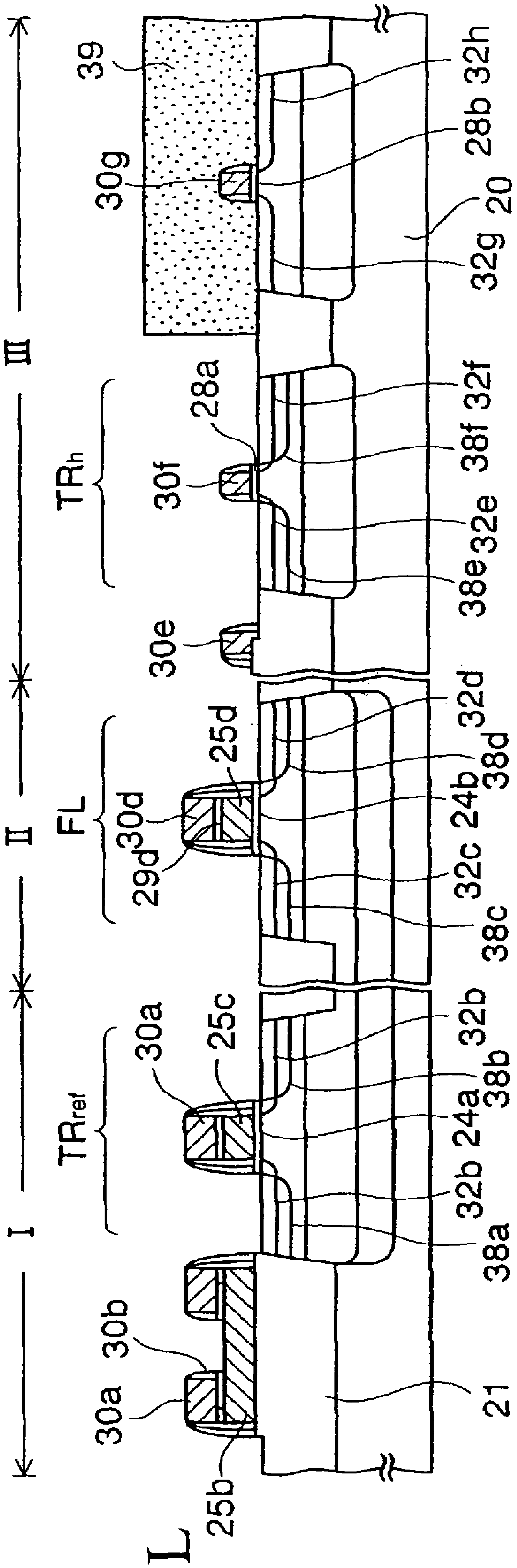

I
II
III
TRref
FL
TRh
30a
30b
30a
25c
29d
30d
25d
30e
30f
28a
30g
39
25b
21
38a
32b
24a
38b
32b
38c
32c
24b
38d
32d
38e
32e
38f
32f
32g
20
28b
32h

FIG. 4L

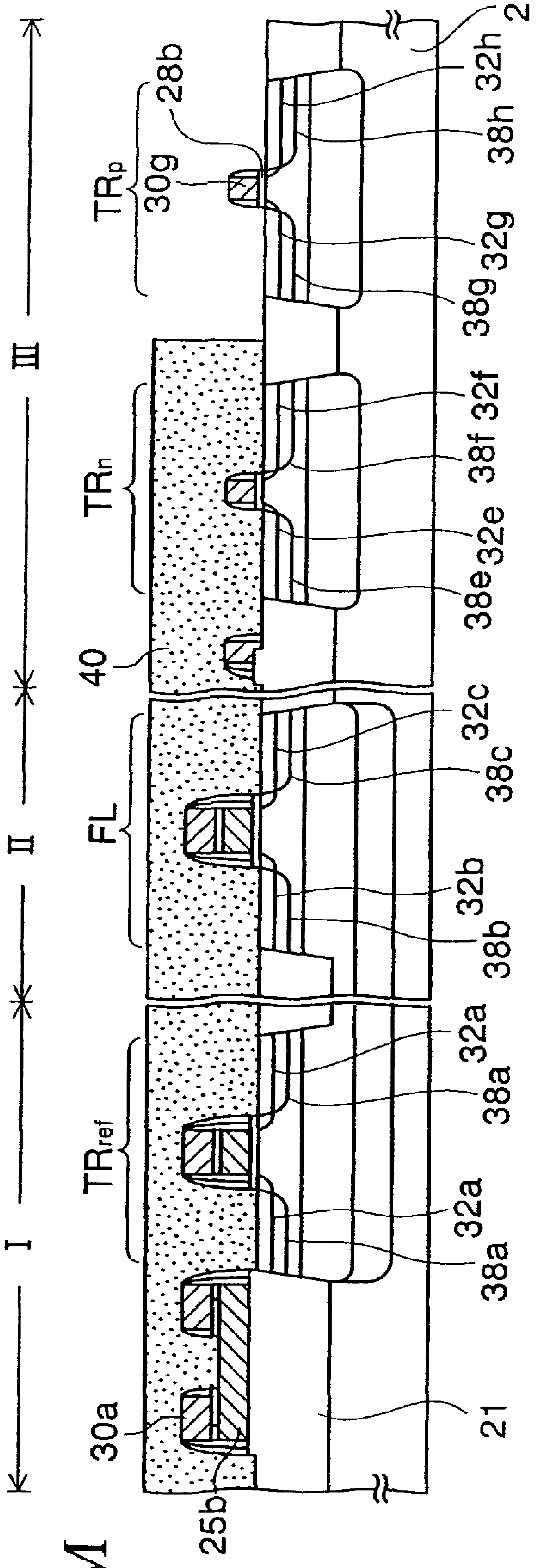

I
II
III
TR_ref
FL
TR_n
TR_p
28b
30g
32h
38h
32g
38g
32f
38f
32e
38e
40
32c
38c
32b
38b
32a
38a
32a
38a
30a
21
25b
20

FIG. 4M

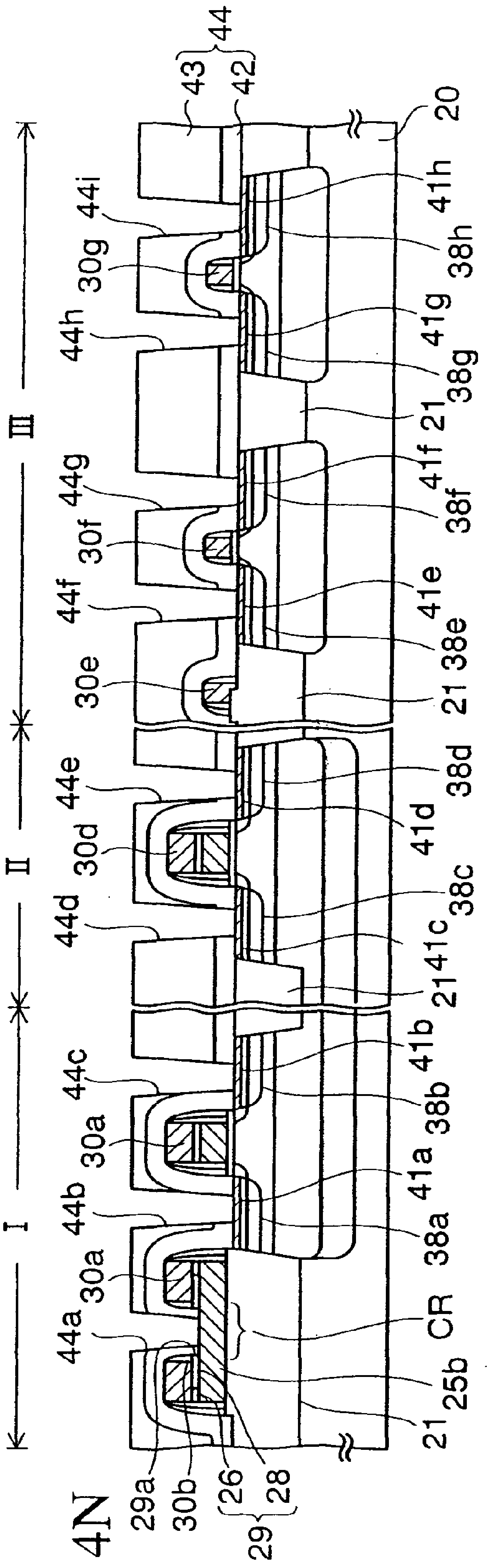

44
43
42
20
44i
41h
38h
30g
44h
41g
38g
21
44g
41f
38f
30f
44f
41e
38e
30e
21
44e
38d
30d
41d
44d
38c
41c
21
44c
41b
38b
30a
41a
44b
38a
30a
44a
CR
25b
21
29a
30b
26
28
29
I
II
III

FIG. 4N

FIG. 4O

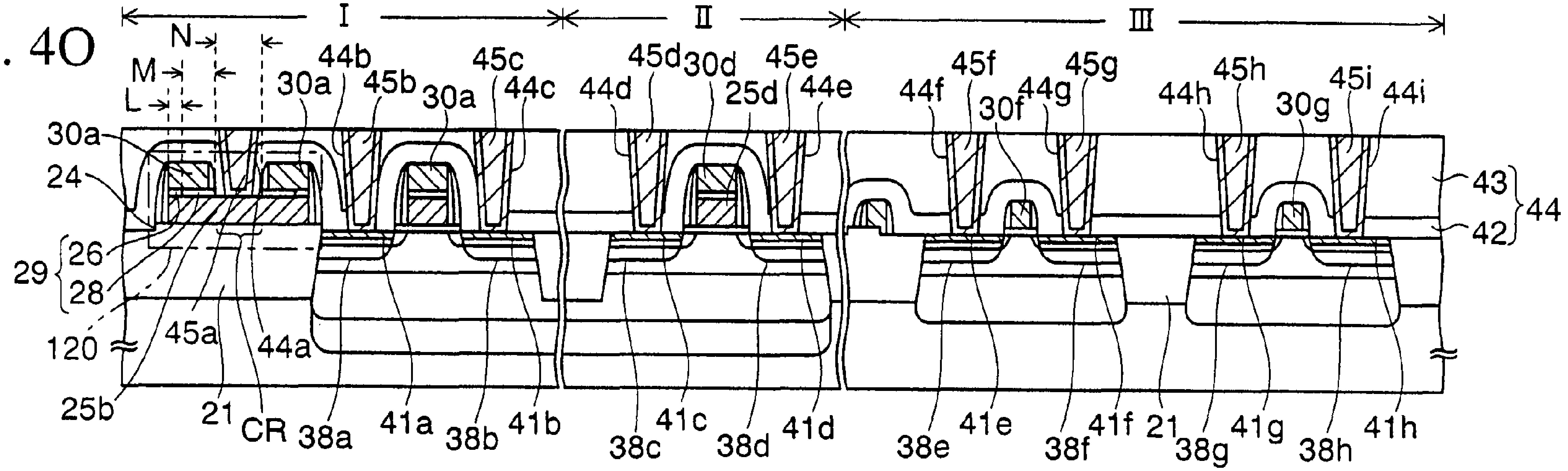
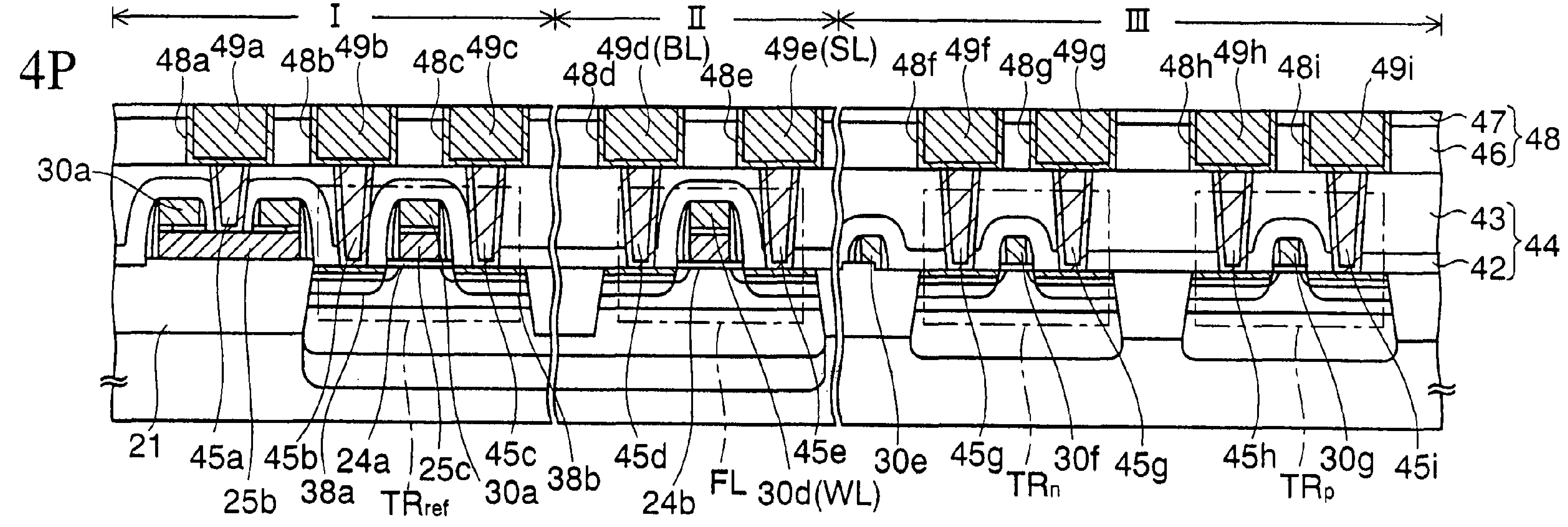

I
II
III
N
M
L
30a
44b
45b
30a
45c
44c
44d
45d
30d
25d
45e
44e
44f
45f
30f
44g
45g
44h
45h
30g
45i
44i
30a
24
26
28
29
120
25b
45a
21
44a
CR
38a
41a
38b
41b
38c
41c
38d
41d
38e
41e
38f
41f
21
38g
41g
38h
41h
43
42
44

FIG. 4P


I
II
III
48a
49a
48b
49b
48c
49c
48d
49d(BL)
48e
49e(SL)
48f
49f
48g
49g
48h
49h
48i
49i
30a
47
46
48
43
42
44
21
45a
25b
45b
38a
24a
TR$_{ref}$
25c
30a
45c
38b
45d
24b
FL
30d(WL)
45e
30e
45g
TR$_n$
30f
45g
45h
TR$_p$
30g
45i

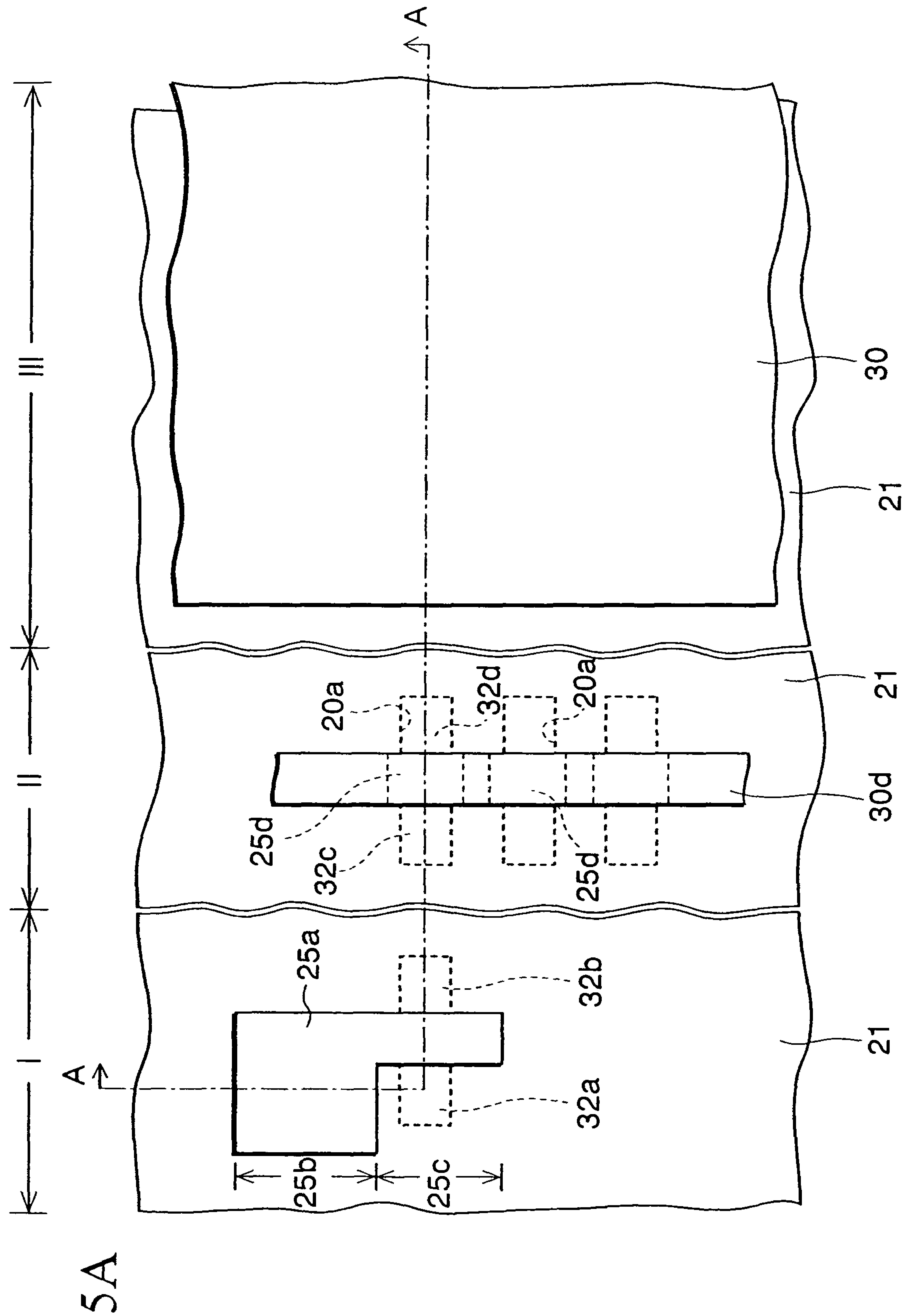

A
A
I
II
III
30
21
21
21
20a
32d
20a
30d
25d
32c
25d
25a
32b
32a
25b
25c

FIG. 5A

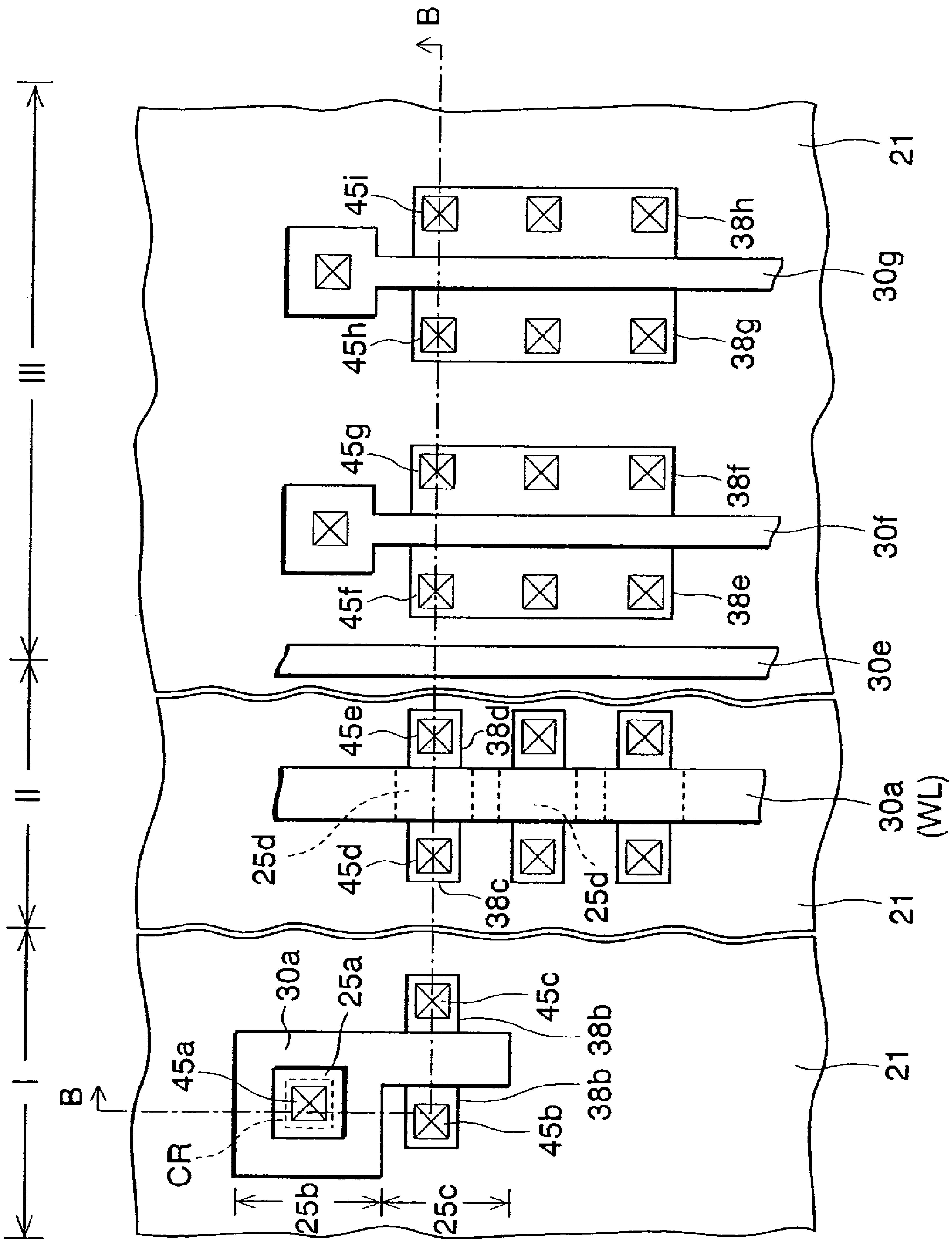

B
B
I
II
III
CR
45a
25a
30a
45b
45c
38b
38b 38b
25b
25c
25d
25d
45d
45e
38c
38d
30a
(WL)
30e
45f
45g
38e
38f
30f
45h
45i
38g
38h
30g
21
21
21

FIG. 5B

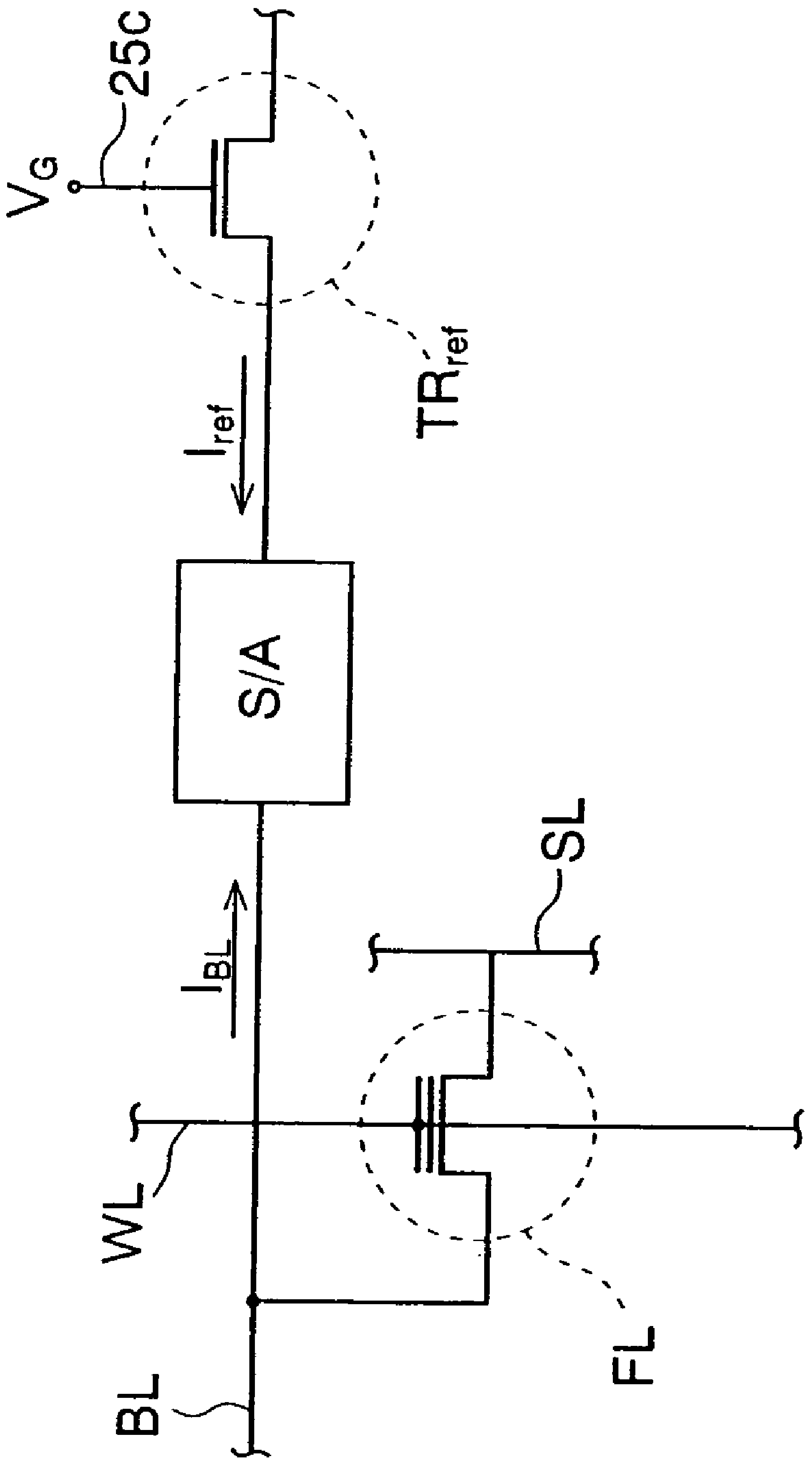


FIG. 6

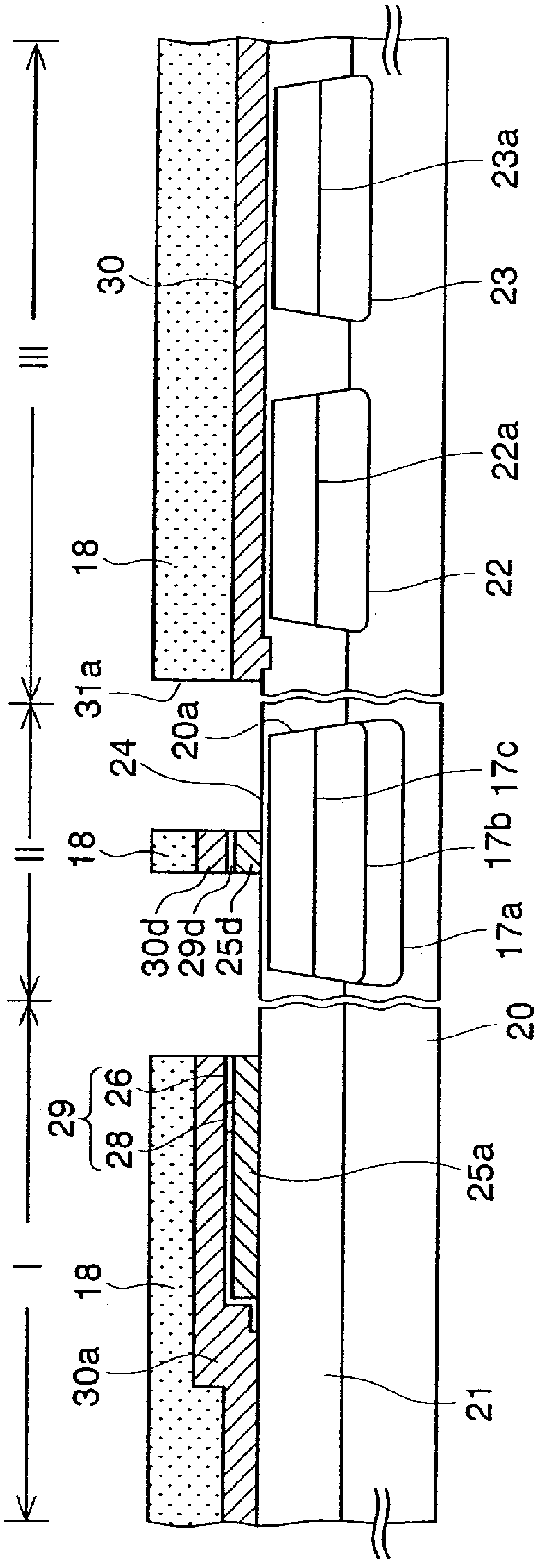

III
II
I
30
18
31a
20a
24
18
30d
29d
25d
29
26
28
18
30a
23a
23
22a
22
17c
17b
17a
20
25a
21

FIG. 7A

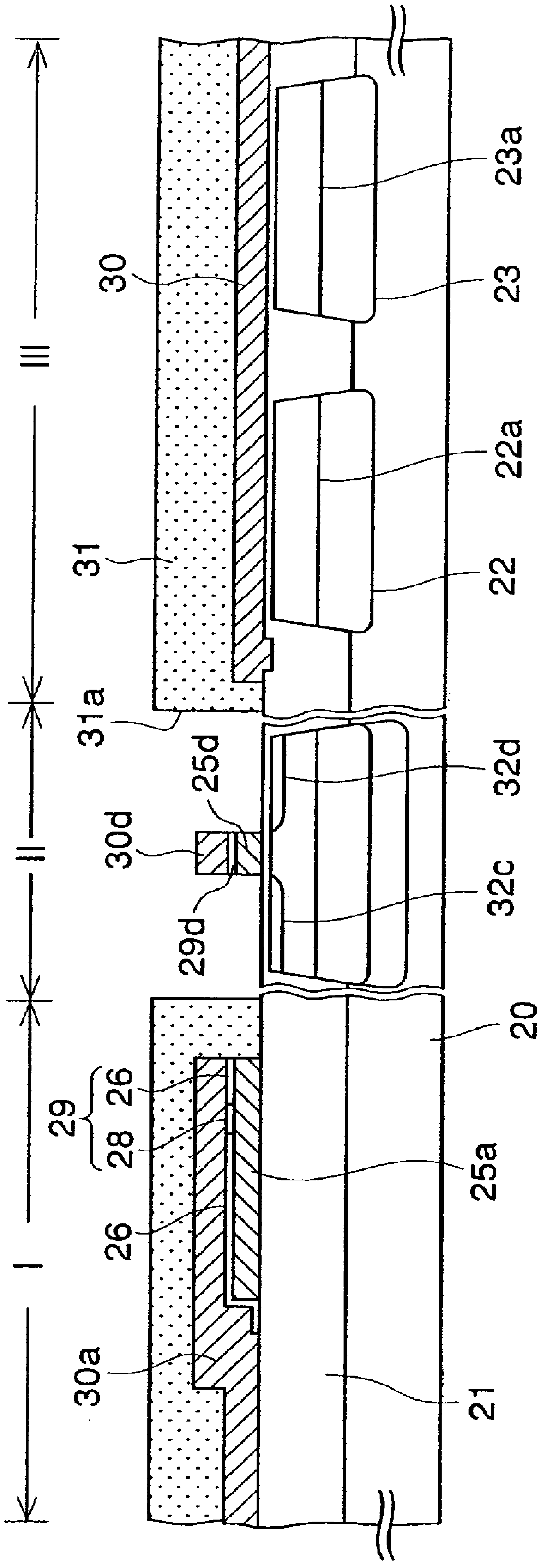

III
II
I
30
31
31a
25d
30d
29d
29
26
28
26
30a
23a
23
22a
22
32d
32c
20
25a
21

FIG. 7B

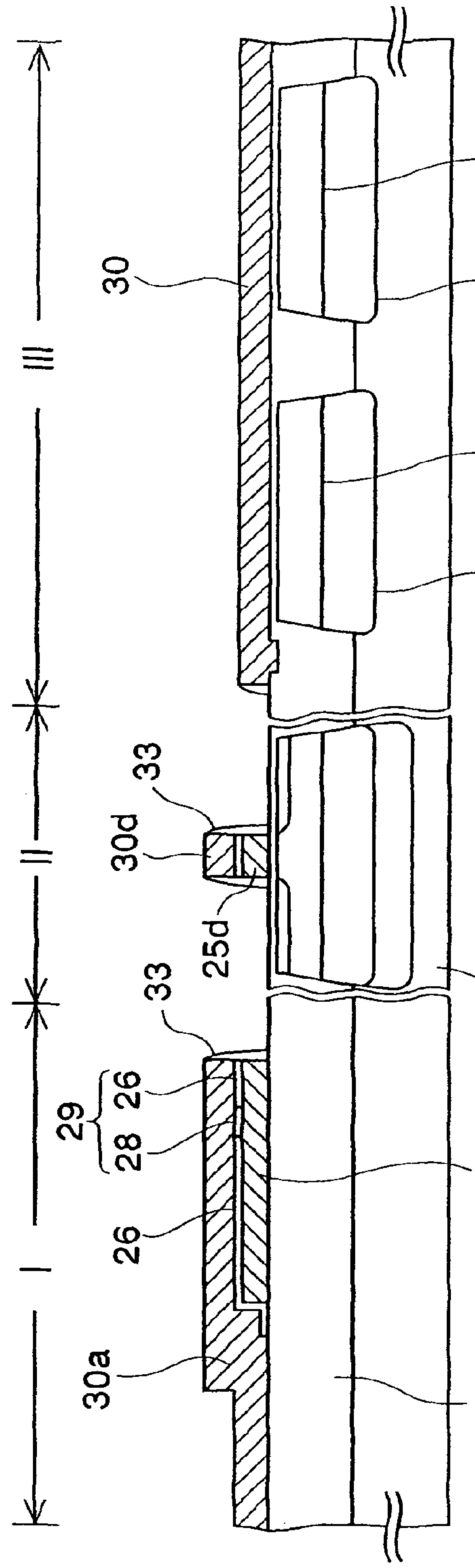

I
II
III
30a
26
28
26
29
33
25d
30d
33
30
21
25a
20
22
22a
23
23a

FIG. 7C

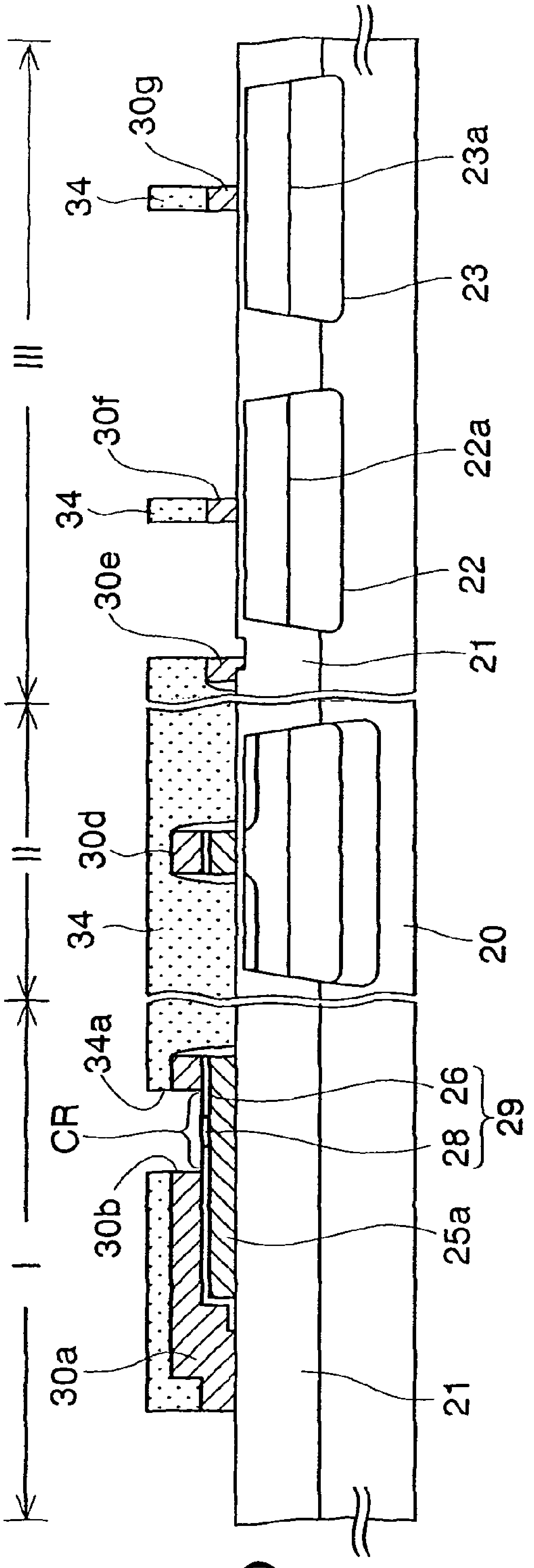

I
II
III
30a
30b
CR
34a
34
30d
30e
34
30f
34
30g
21
25a
28
26
29
20
21
22
22a
23
23a

FIG. 7D

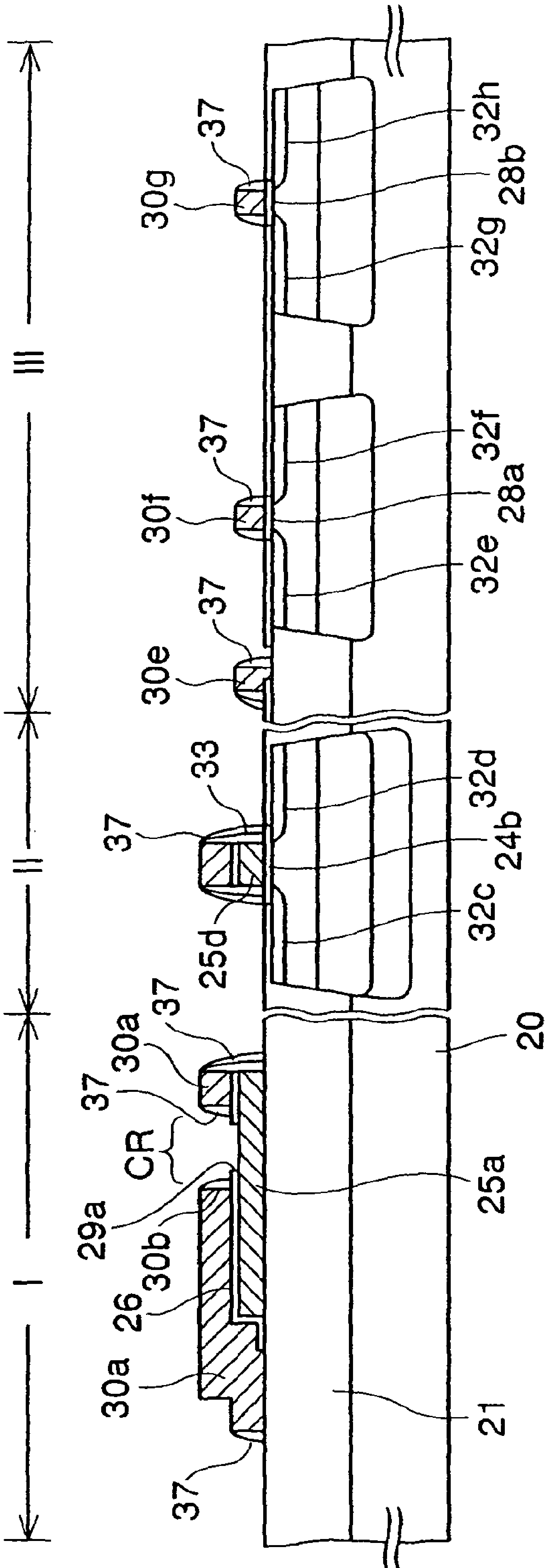

I
II
III
37
30a
26
30b
29a
CR
37
30a
37
25a
21
20
25d
37
24b
33
32c
32d
30e
37
30f
37
28a
32e
32f
30g
37
28b
32g
32h

FIG. 7E

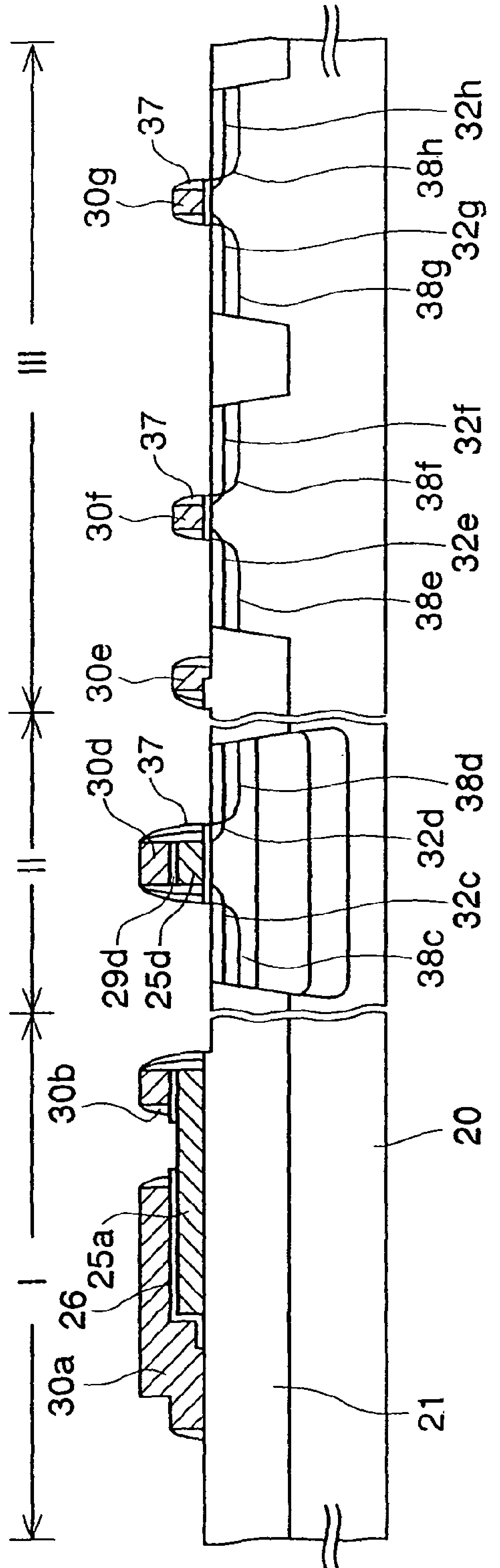
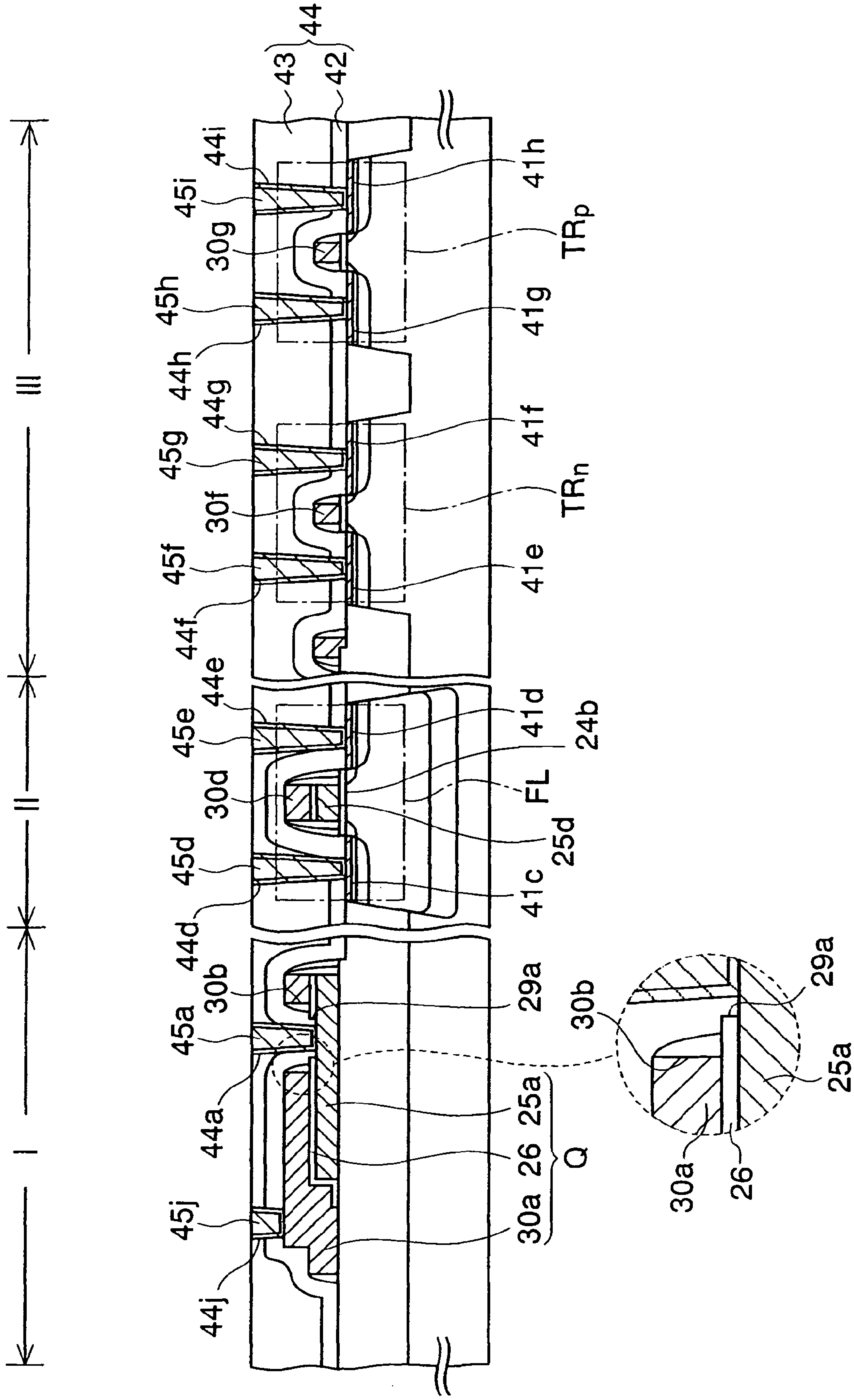

I
II
III
30a
26
25a
30b
21
20
29d
25d
30d
37
38c
32c
32d
38d
30e
30f
37
38e
32e
38f
32f
30g
37
38g
32g
38h
32h

FIG. 7F

FIG. 7G


I
II
III
44
43
42
44i
45i
30g
45h
44h
44g
45g
30f
45f
44f
44e
45e
30d
45d
44d
30b
45a
44a
45j
44j
41h
TRp
41g
41f
TRn
41e
41d
24b
FL
25d
41c
29a
25a
26
30a
Q
30b
29a
25a
30a
26

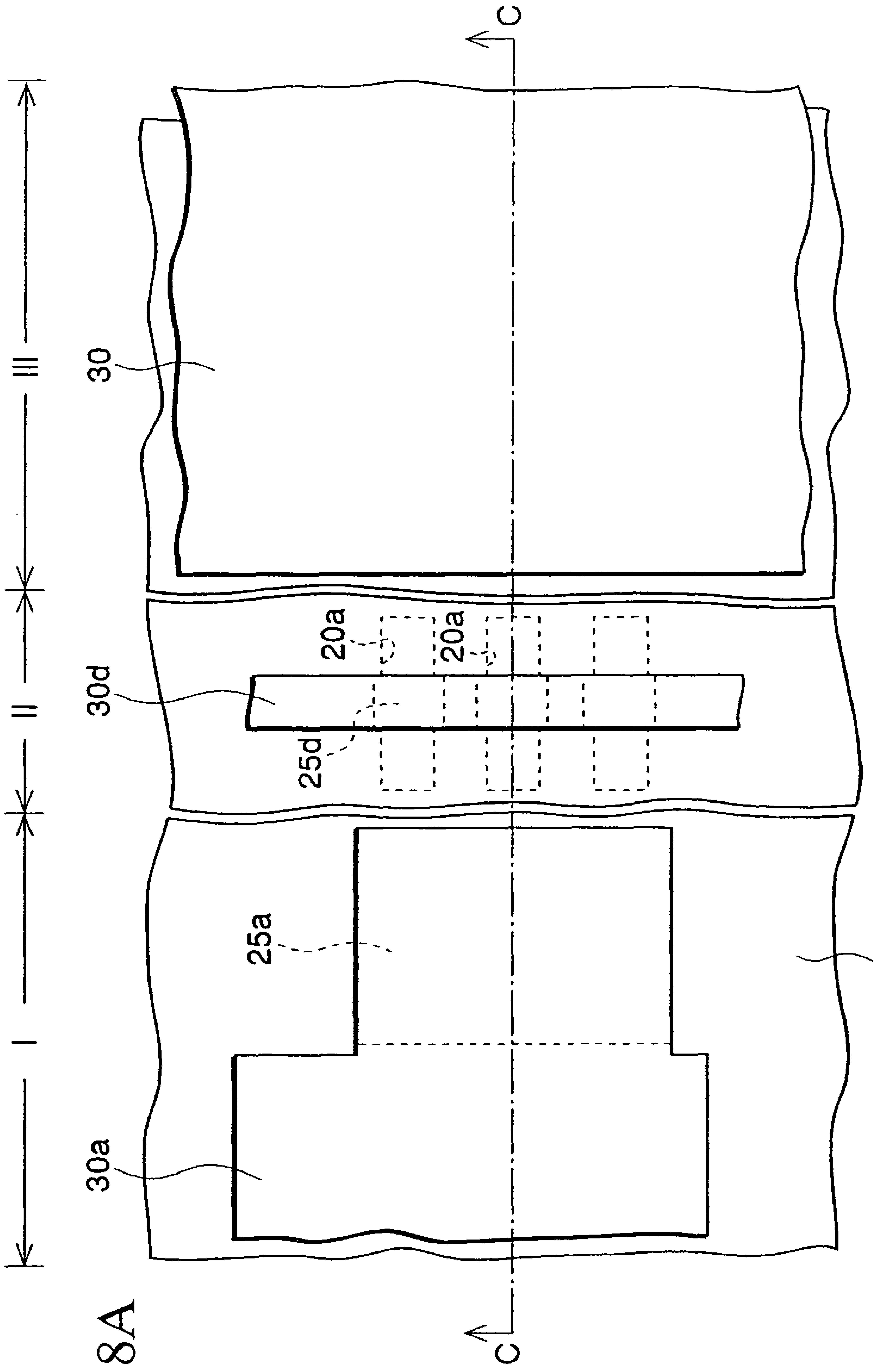


FIG. 8A

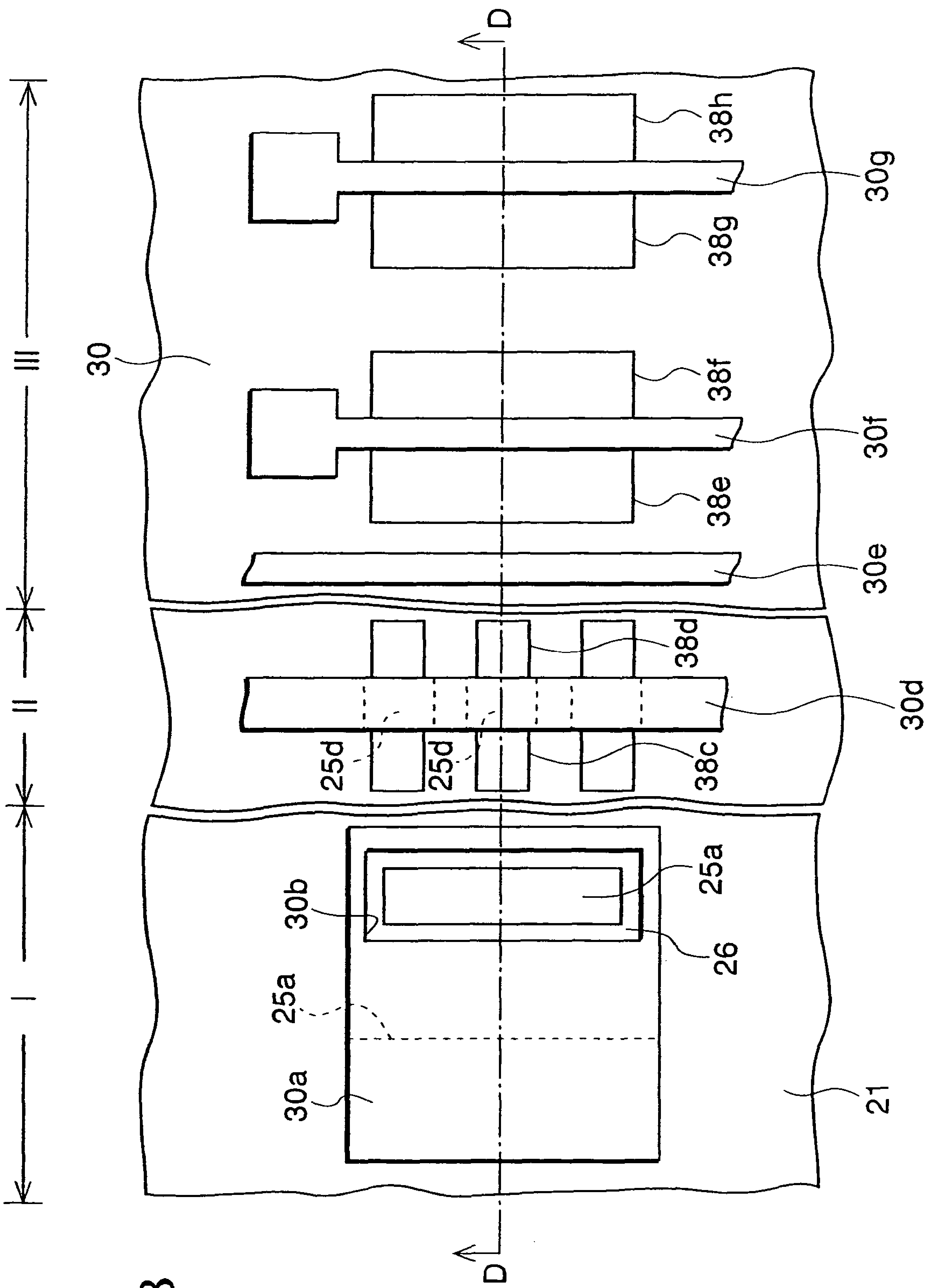

D
D
I
II
III
30
38h
30g
38g
38f
30f
38e
30e
38d
30d
38c
25d
25d
30b
25a
26
25a
30a
21

FIG. 8B

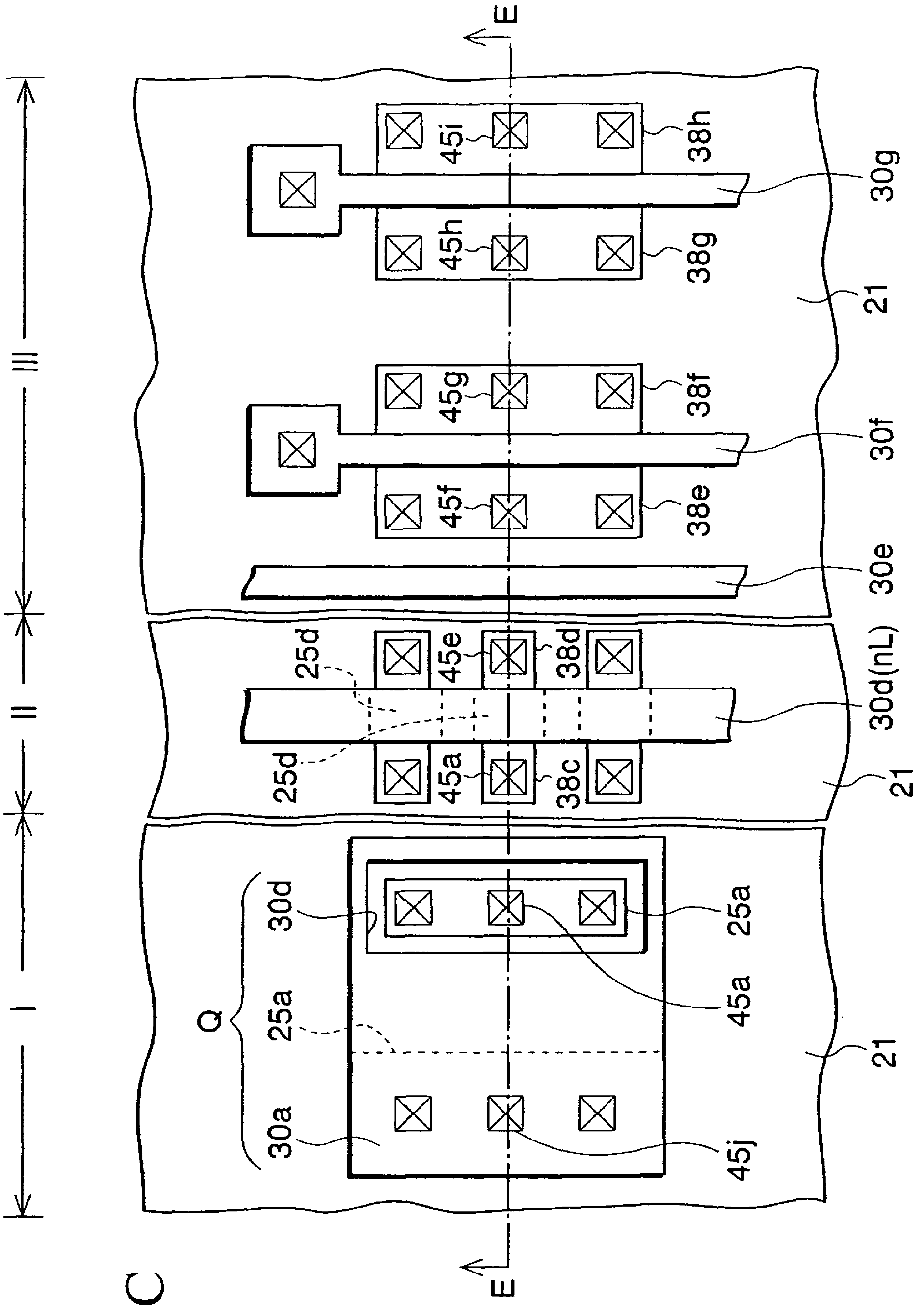

E
E
I
II
III
Q
30a
25a
25a
30d
25a
45a
45j
21
21
21
25d
25d
45a
38c
45e
38d
30d(nL)
30e
45f
38e
30f
45g
38f
45h
38g
30g
45i
38h

FIG. 8C

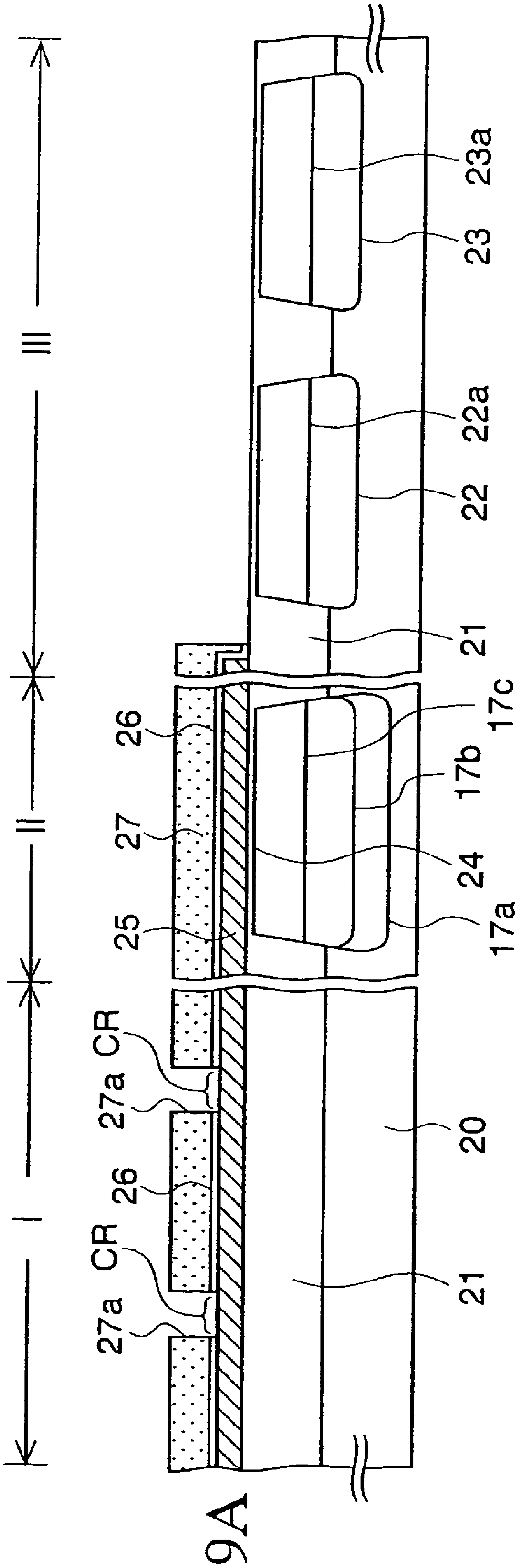

I
II
III
27a
CR
26
27a
CR
25
27
26
21
20
17a
24
17b
17c
21
22
22a
23
23a

FIG. 9A

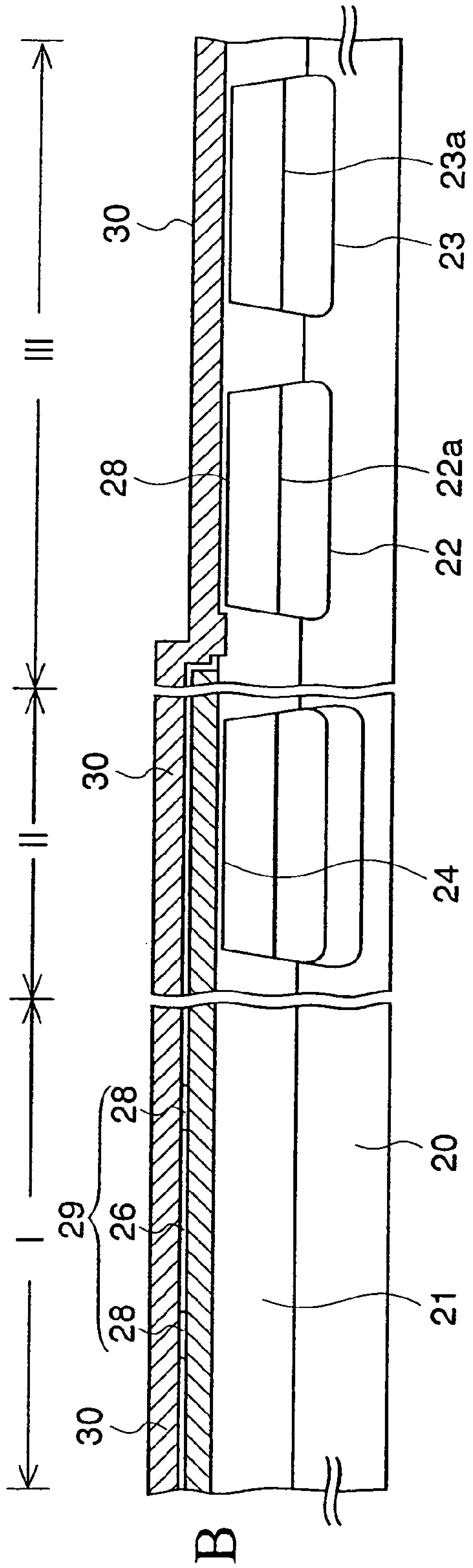

I
II
III
30
28
26
28
29
30
28
30
21
20
24
22
22a
23
23a

FIG. 9B

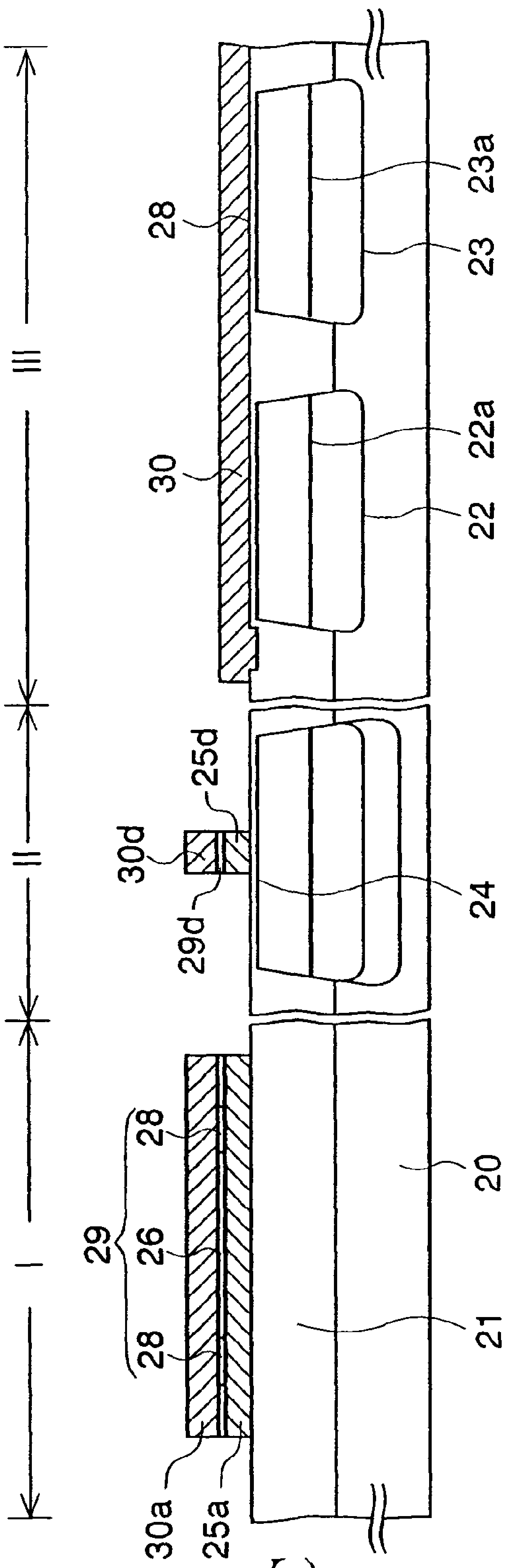

I
II
III
28
30
23a
23
22a
22
30d
25d
29d
24
29
28
26
28
20
21
30a
25a

FIG. 9C

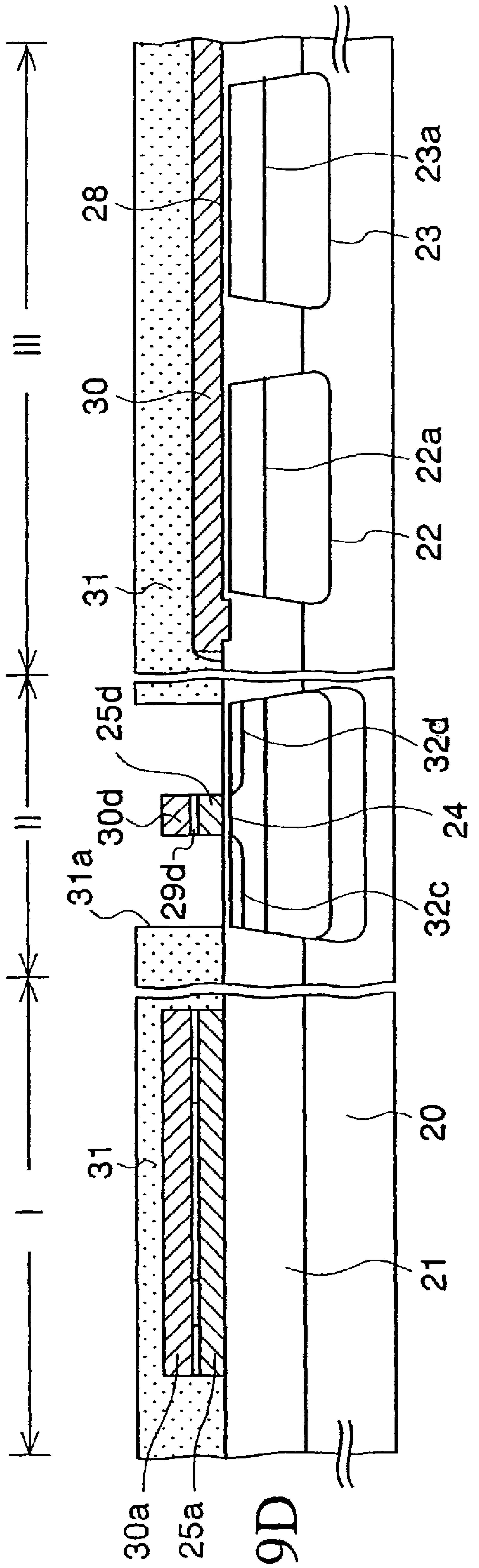

I
II
III
28
30
31
23a
23
22a
22
25d
30d
32d
24
31a
29d
32c
31
20
21
30a
25a

FIG. 9D

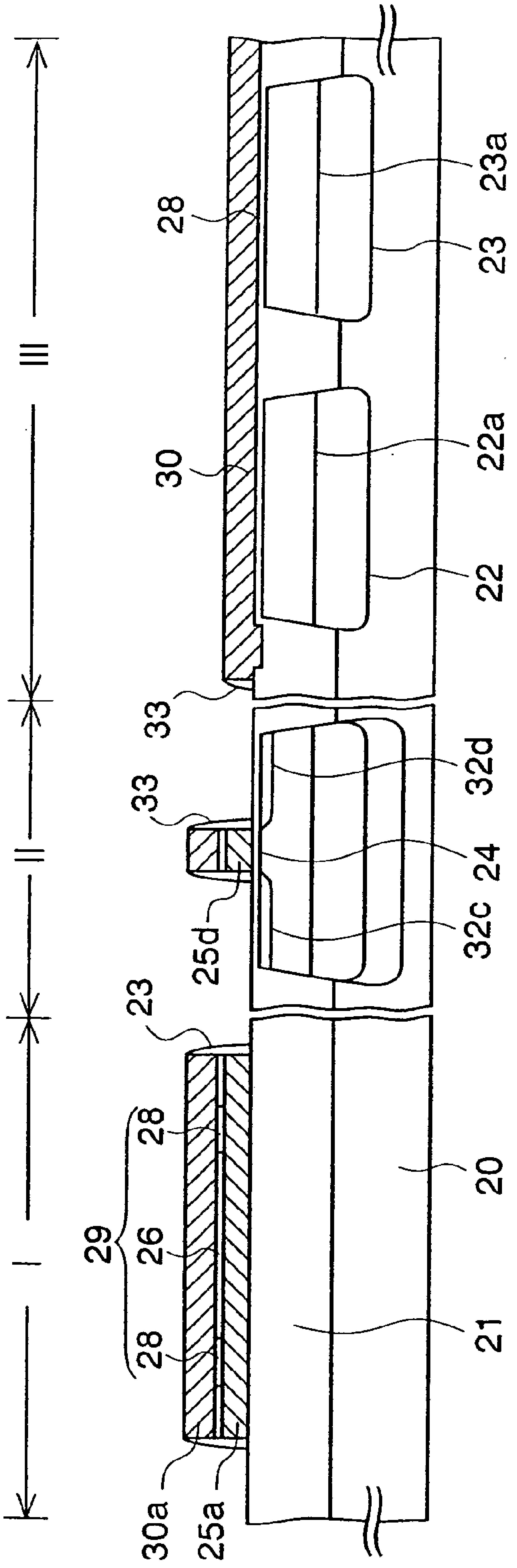

I
II
III
28
30
33
33
25d
23
29
28
26
28
30a
25a
23a
23
22a
22
32d
24
32c
20
21

FIG. 9E

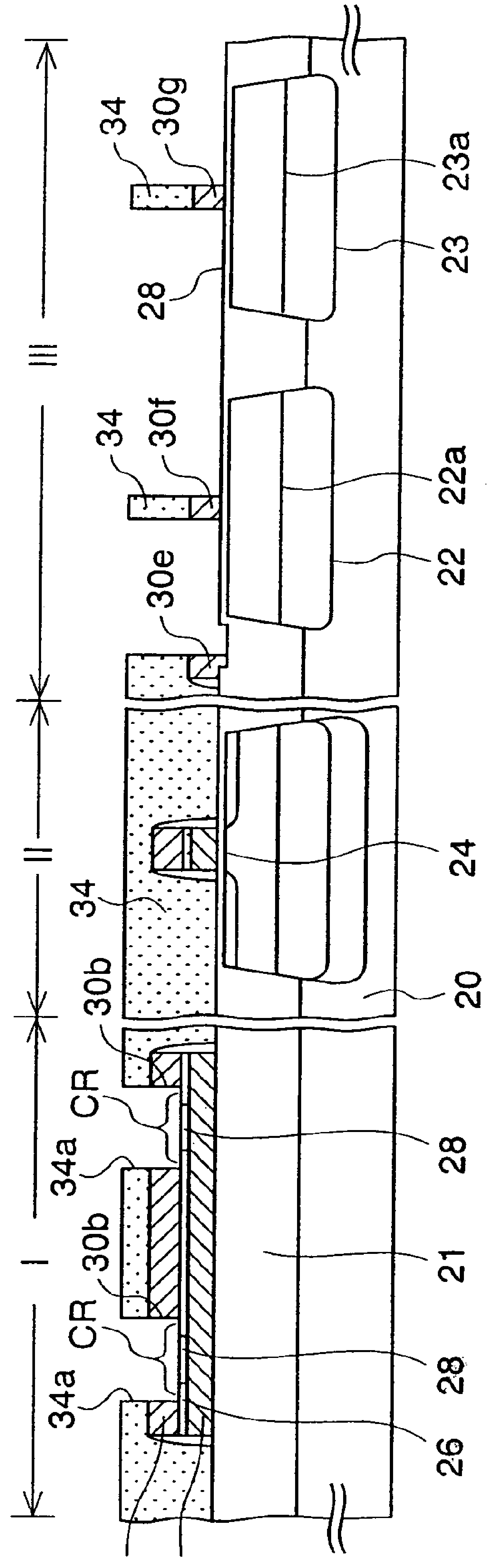

I
II
III
34
30g
34
30f
30e
34
30b
CR
34a
30b
CR
34a
30a
25a
23a
23
28
22a
22
24
20
28
21
28
26

FIG. 9F

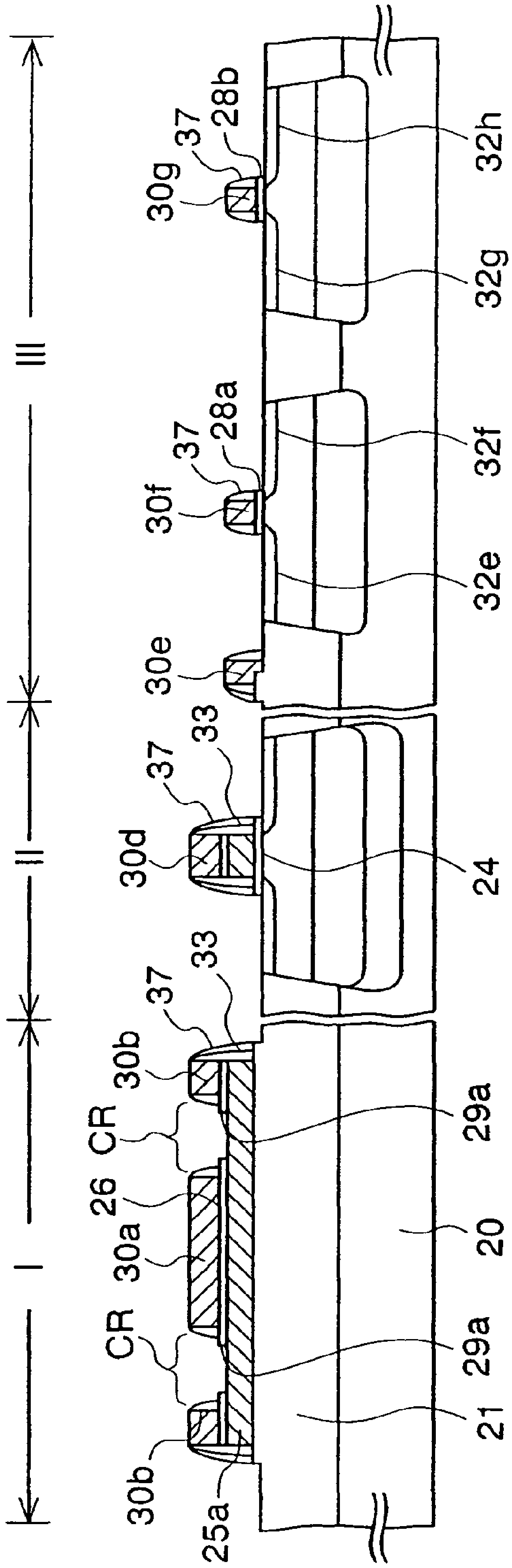

I
II
III
30b
25a
CR
30a
26
CR
30b
37
33
29a
21
29a
20
30d
37
33
24
30e
30f
37
28a
32e
32f
30g
37
28b
32g
32h

FIG. 9G

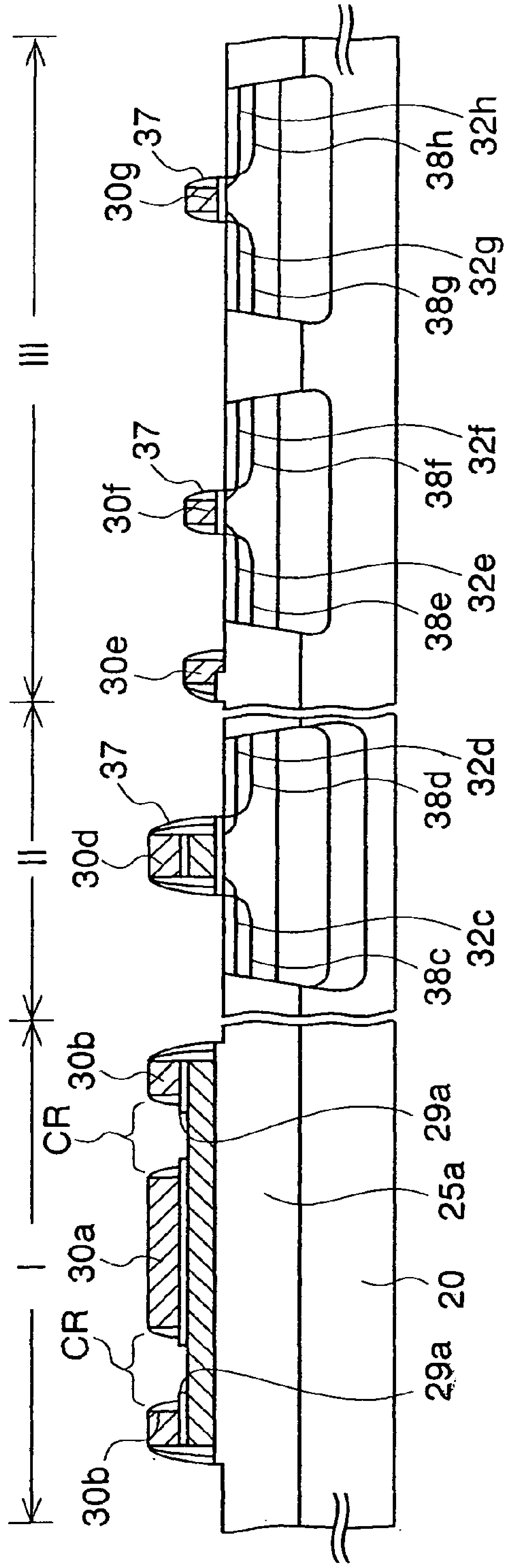

I
II
III
30b
CR
30a
CR
30b
29a
29a
25a
20
30d
37
38c
32c
38d
32d
30e
30f
37
38e
32e
38f
32f
30g
37
38g
32g
38h
32h

FIG. 9H

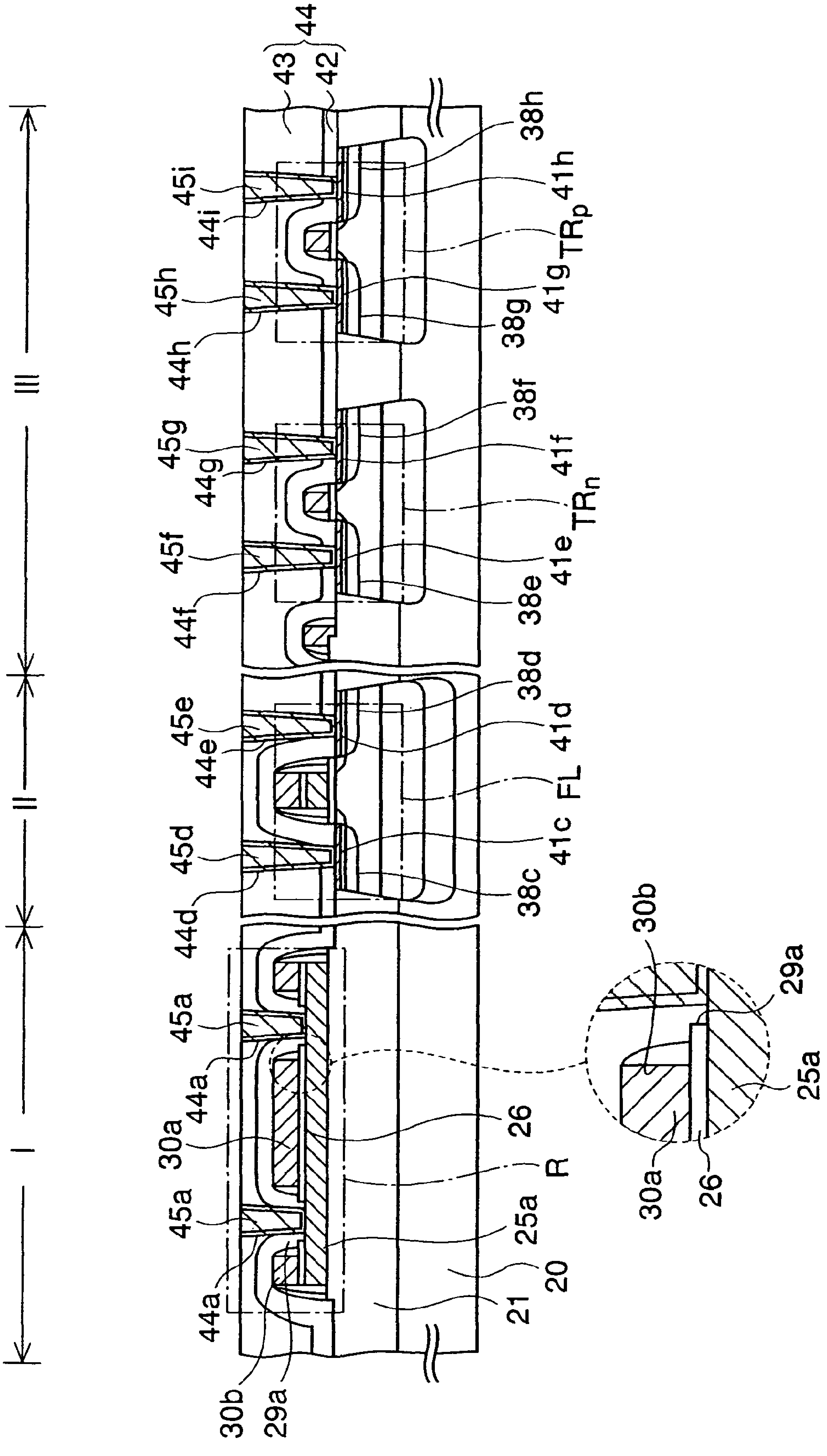

I
II
III
44
43
42
45i
44i
38h
41h
41g
TR$_p$
45h
44h
38g
45g
44g
38f
41f
TR$_n$
45f
44f
41e
38e
45e
44e
38d
41d
FL
45d
44d
41c
38c
45a
44a
30a
45a
44a
26
R
25a
20
21
30b
29a
30b
29a
25a
30a
26

FIG. 9I

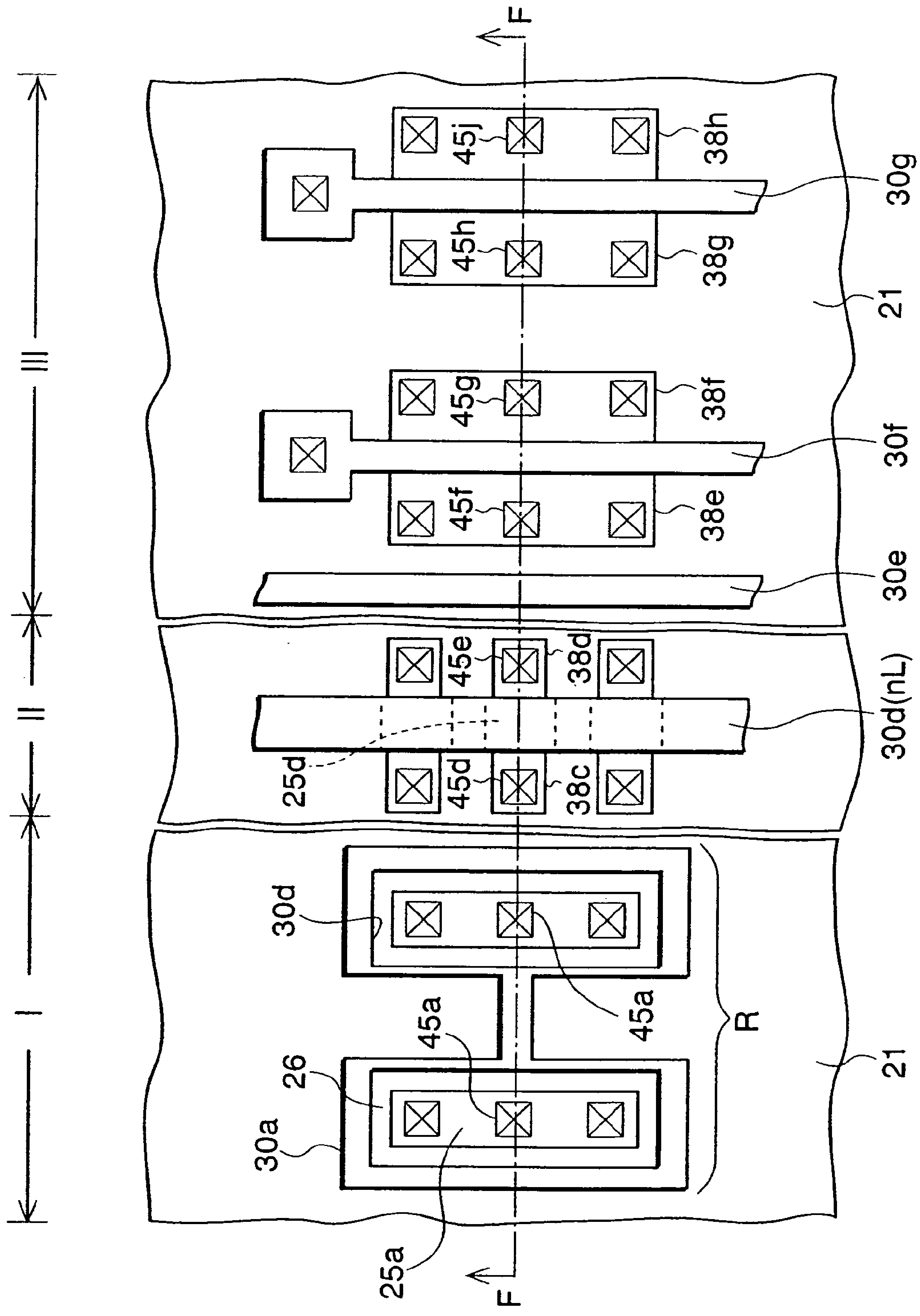

F
45j
38h
30g
45h
38g
21
45g
38f
30f
45f
38e
30e
45e
38d
30d(nL)
25d
45d
38c
30d
45a
45a
R
26
30a
25a
21
F
III
II
I

FIG. 10

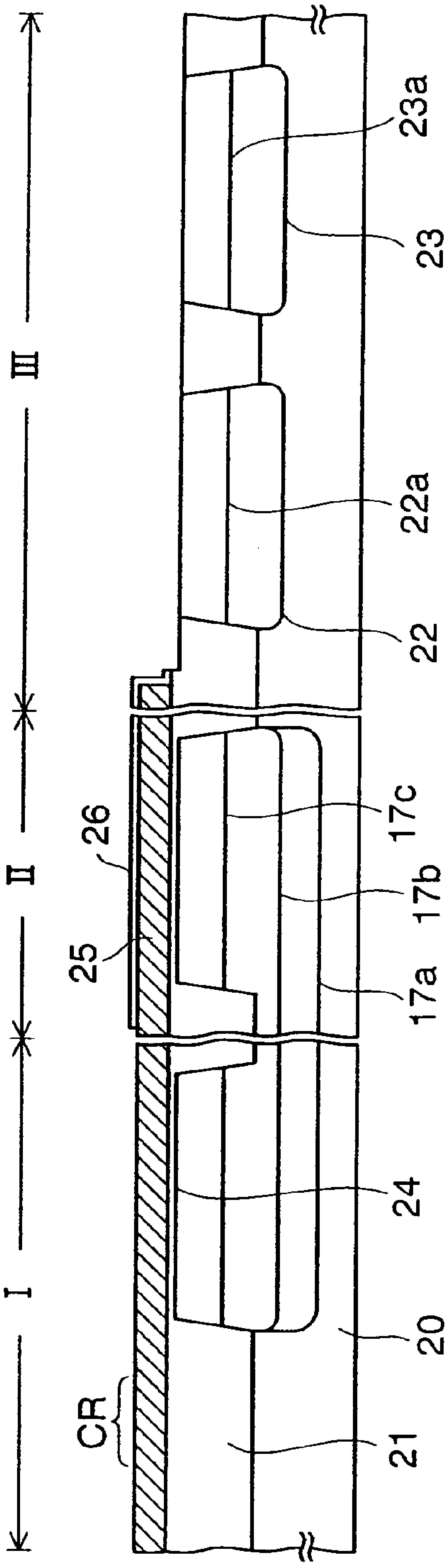


FIG. 11A

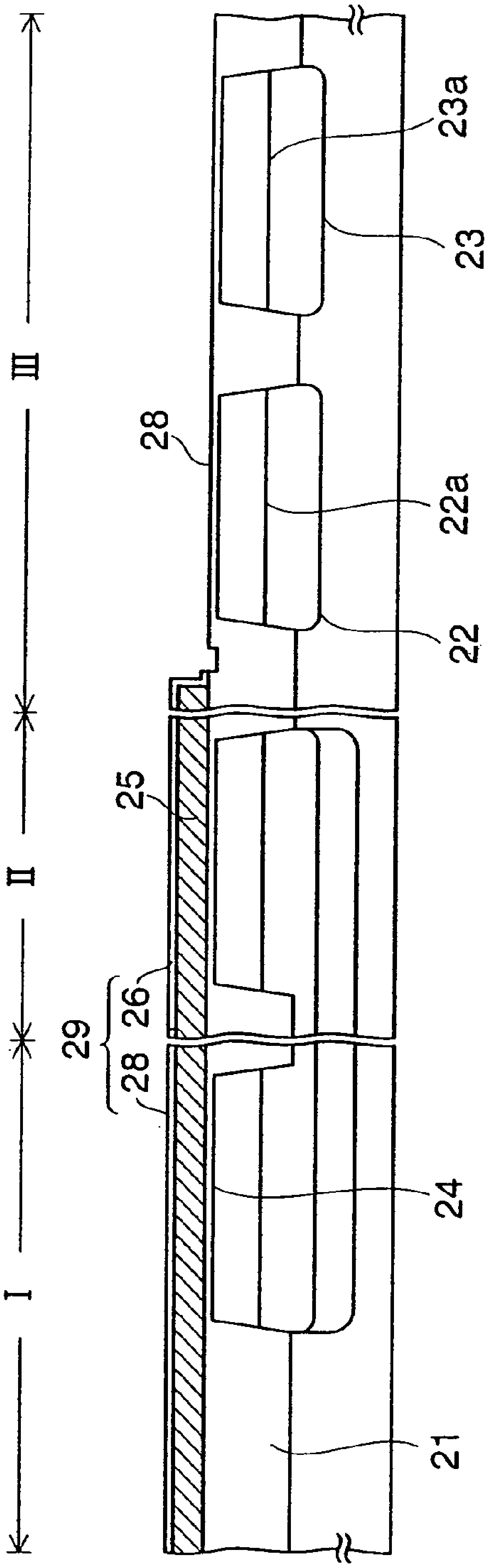


FIG. 11B

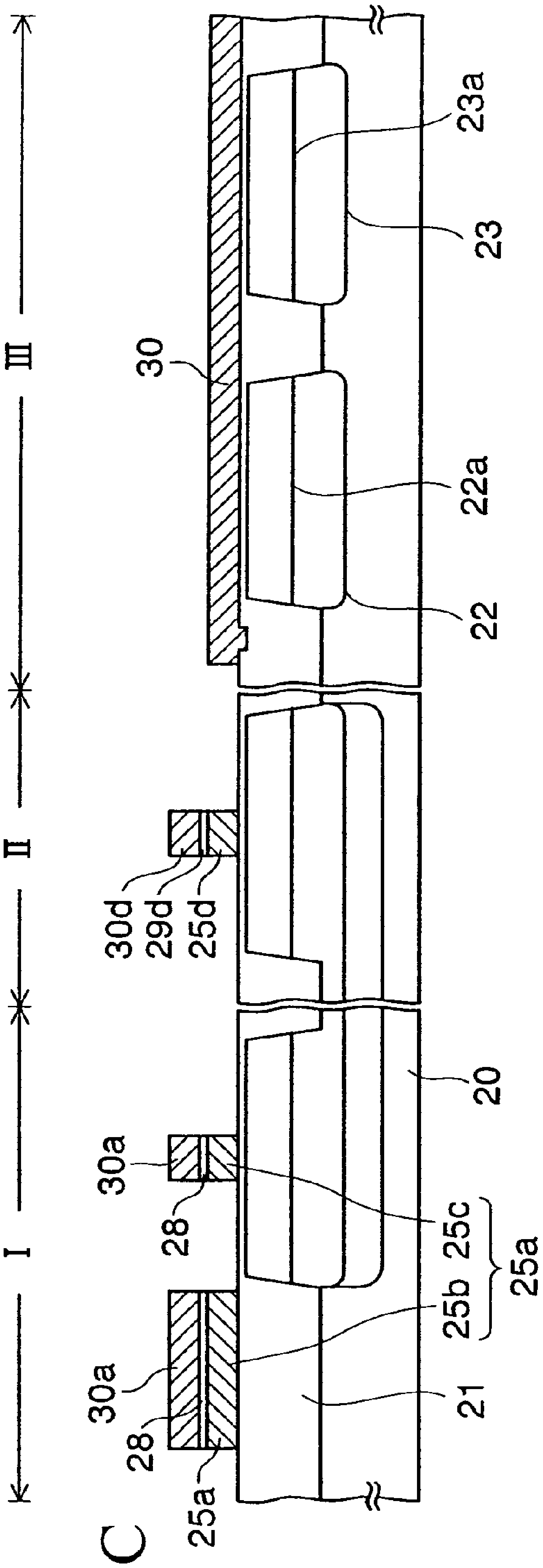


FIG. 11C

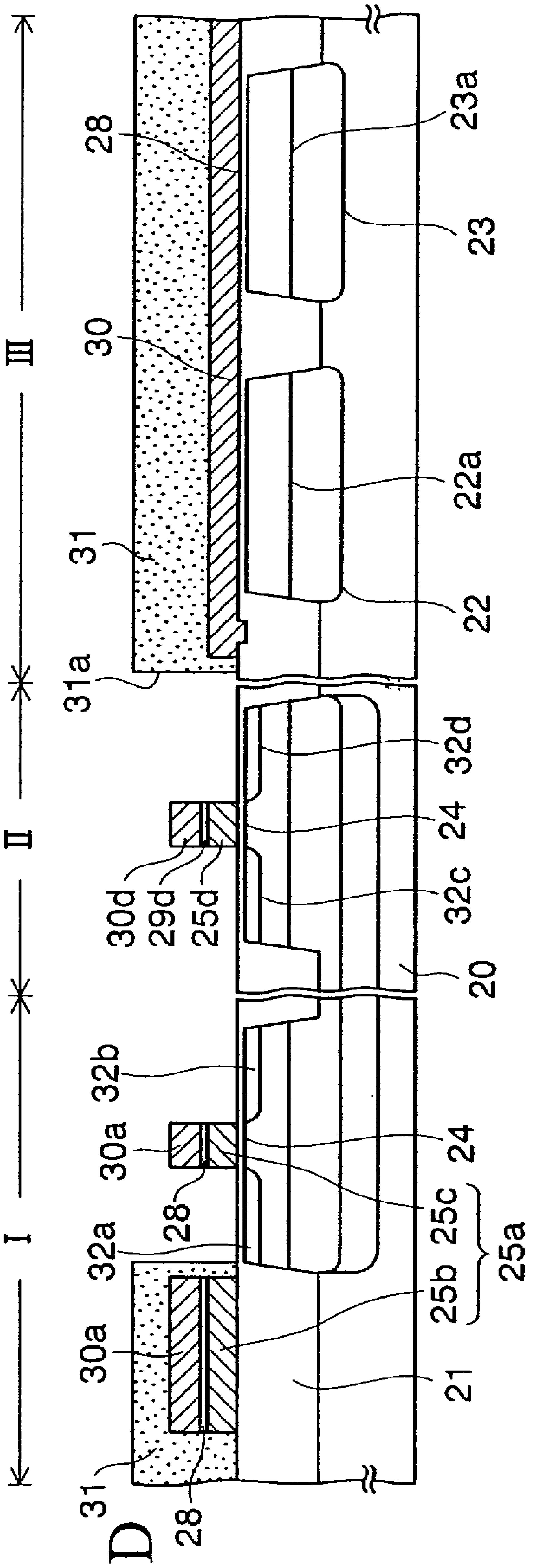


FIG. 11D

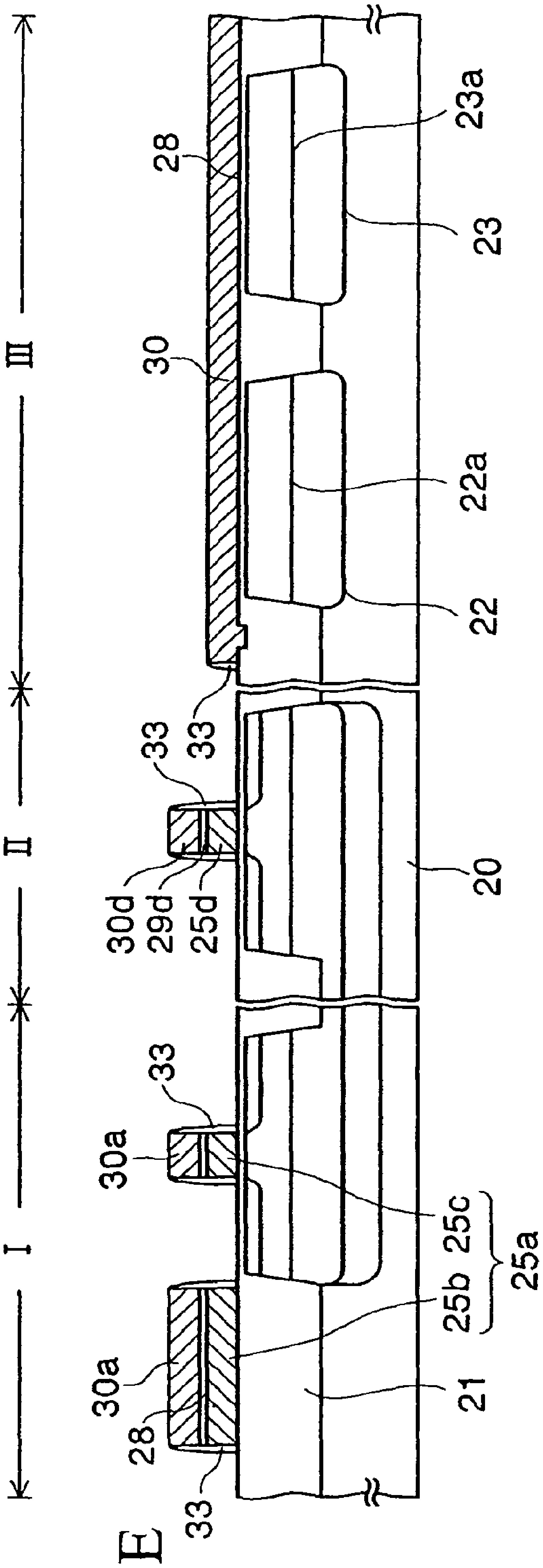


FIG. 11E

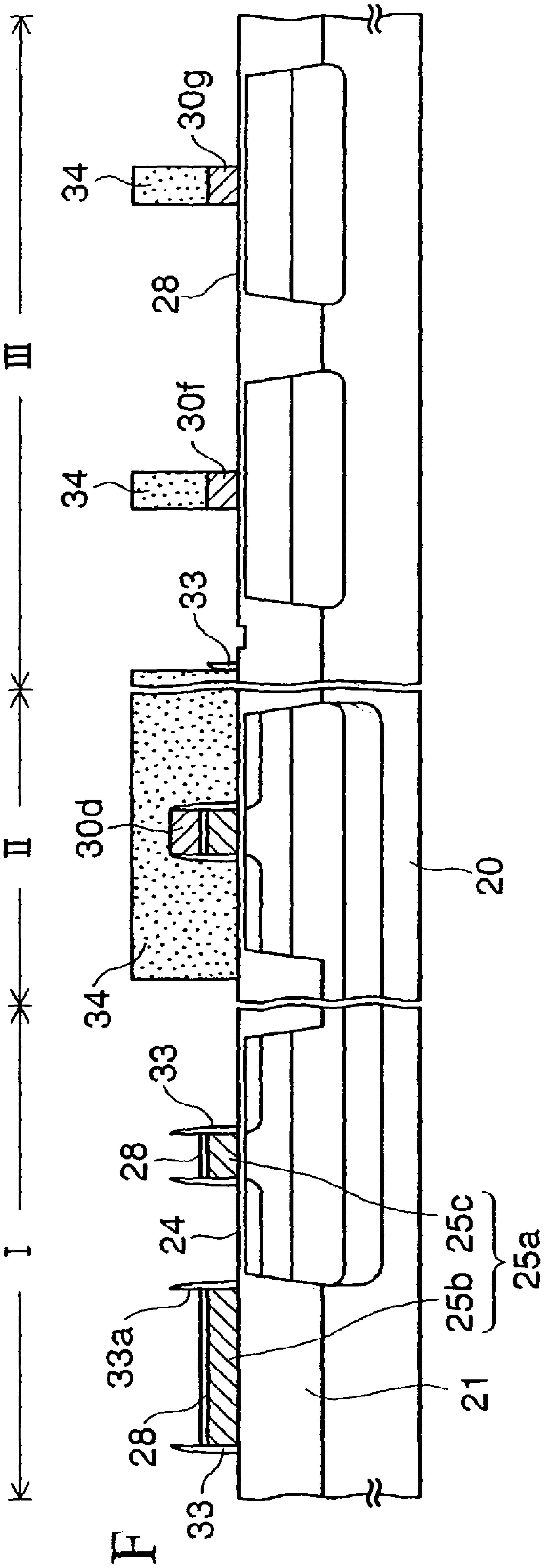


FIG. 11F

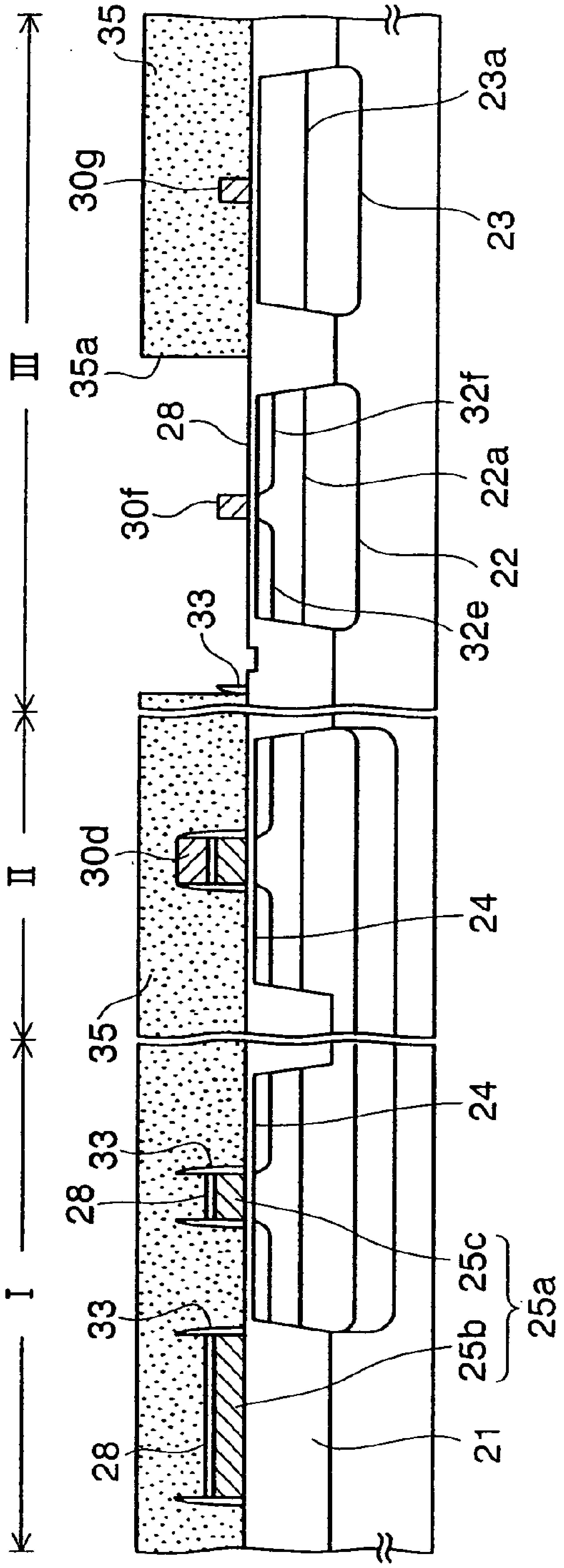


FIG. 11G

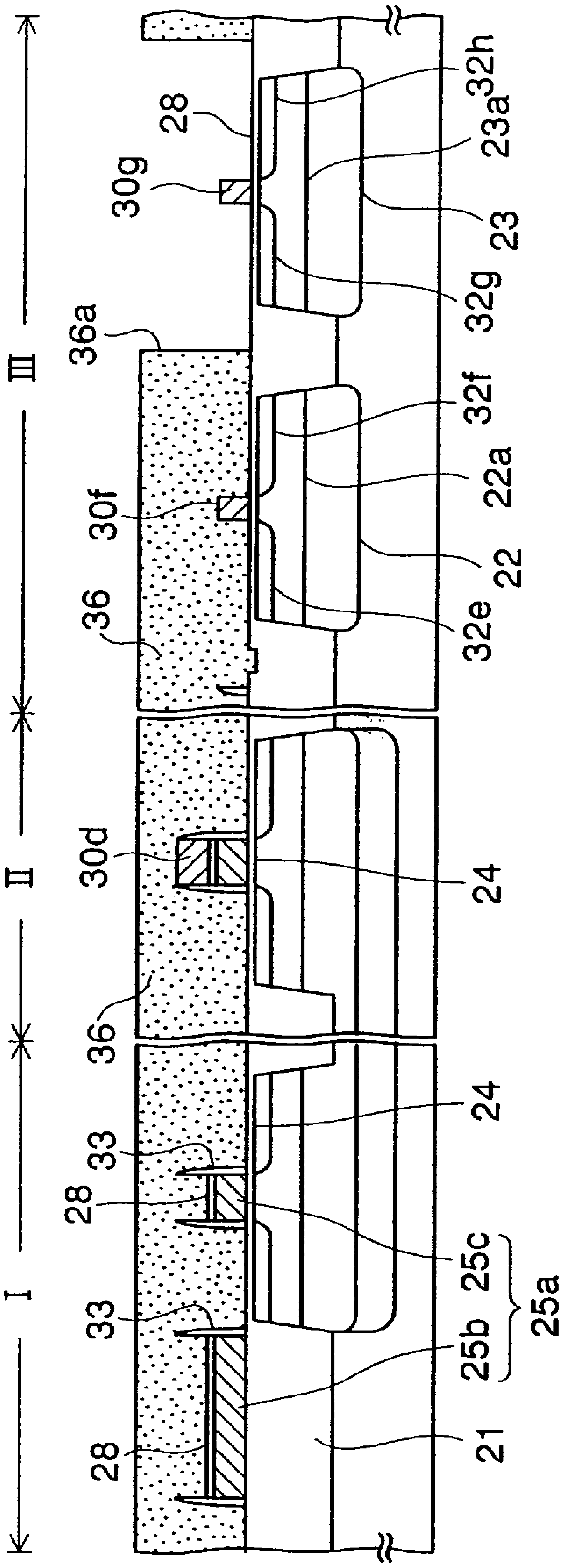


FIG. 11H

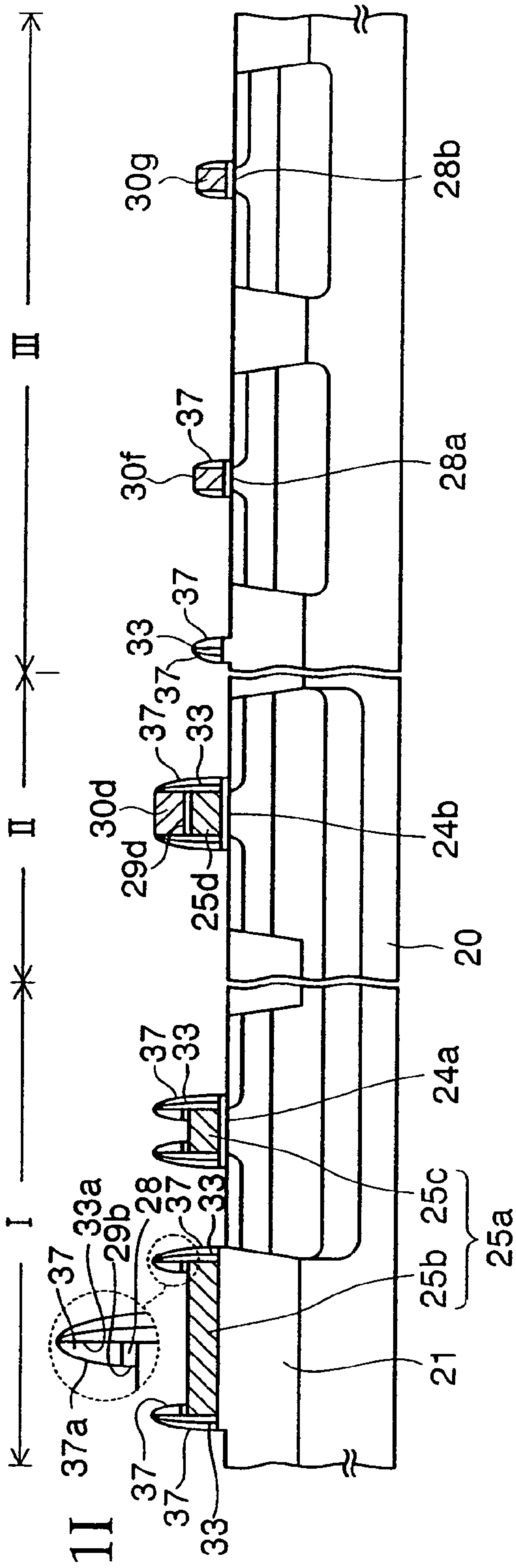


FIG. 11I

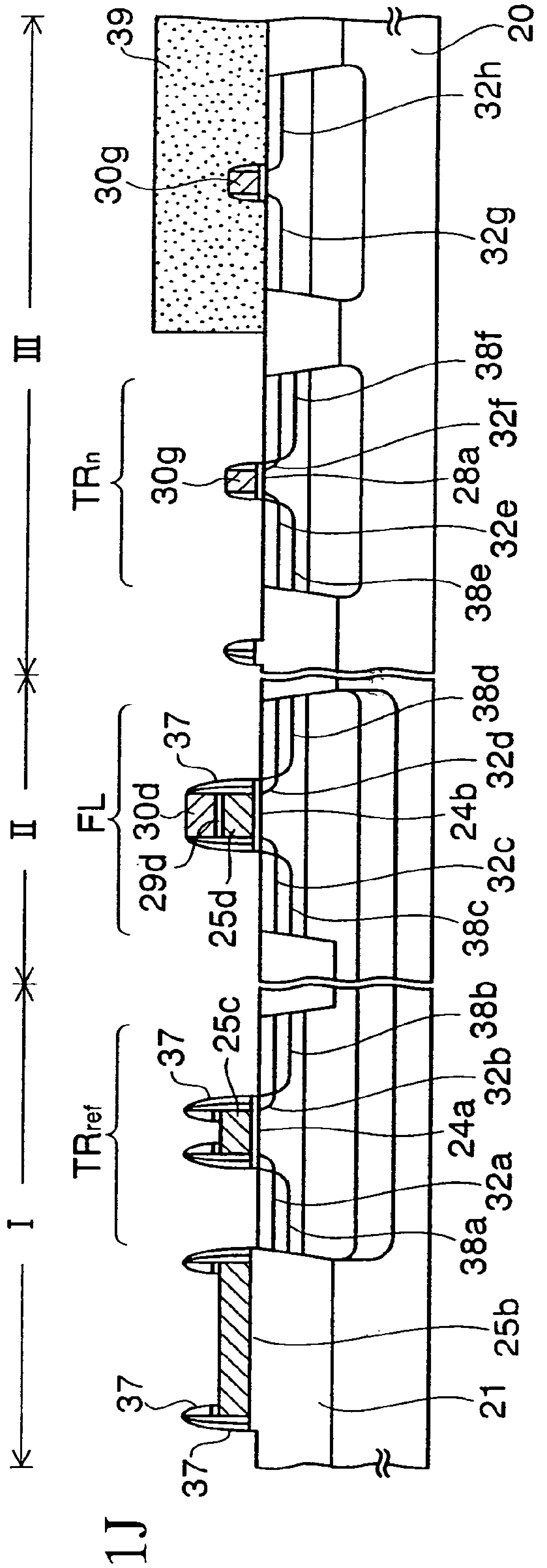


FIG. 11J

FIG. 11K

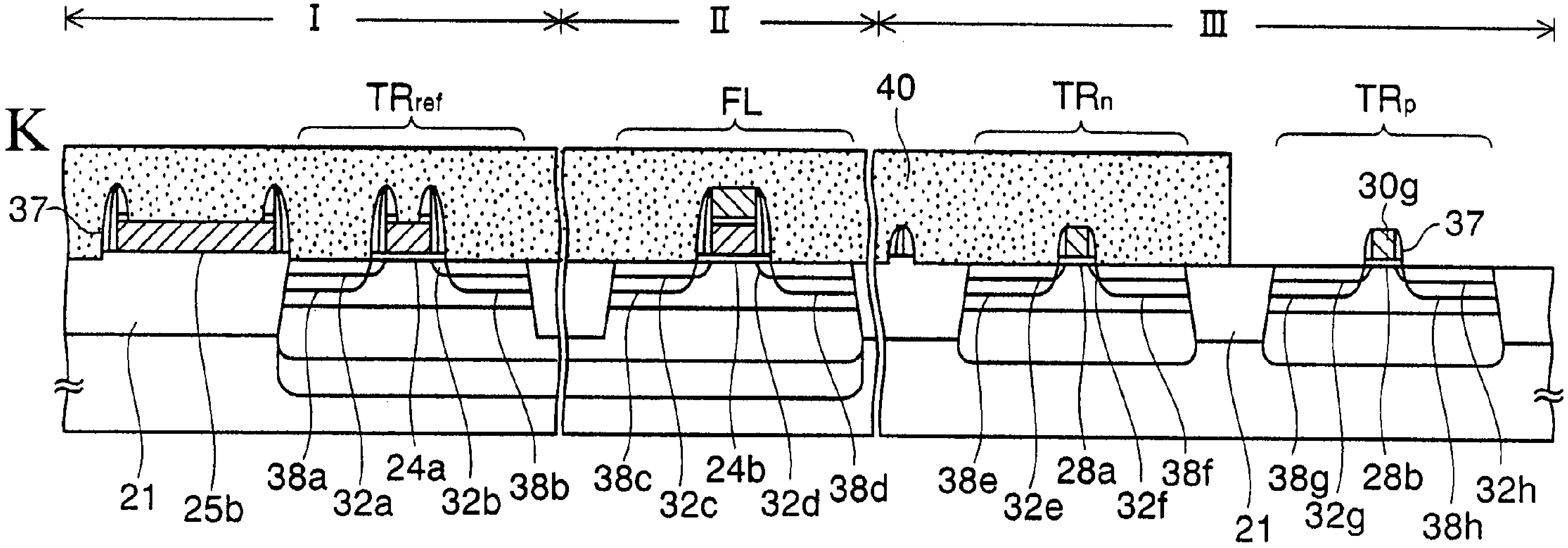


FIG. 11L

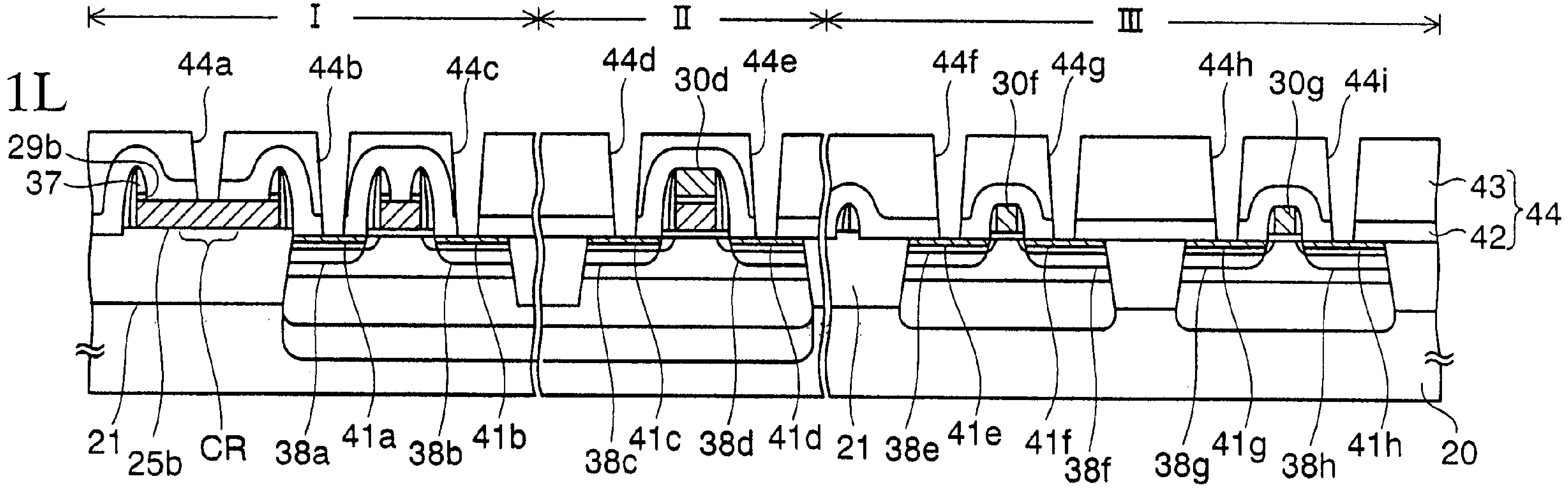
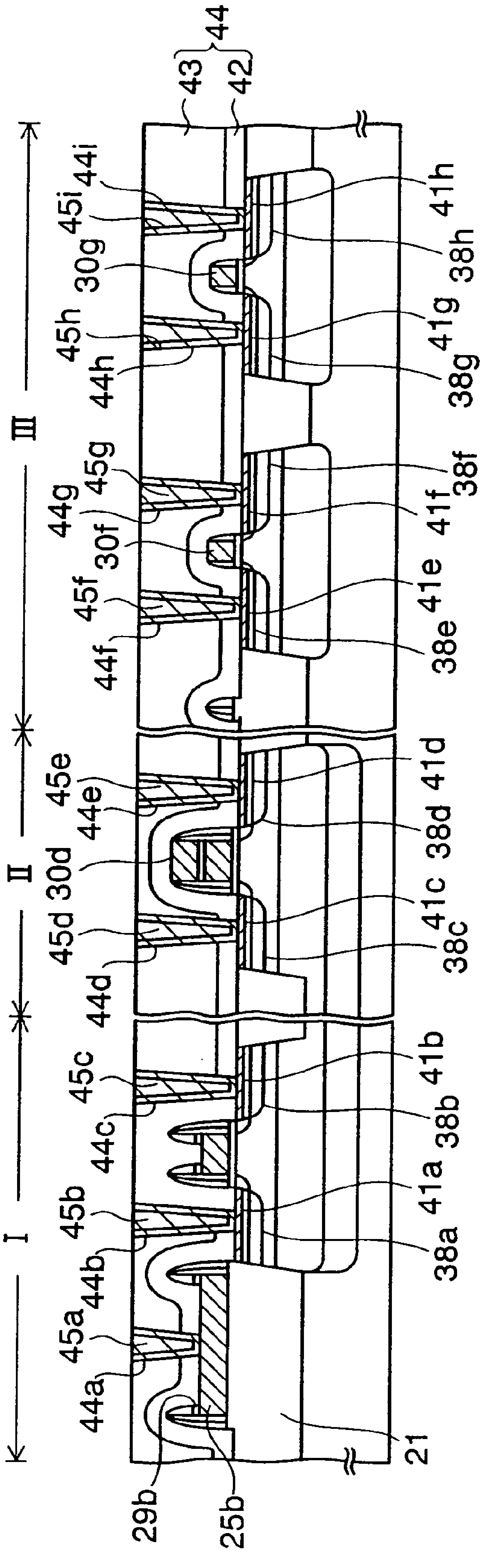


FIG. 11M


43
42
44
44i
45i
30g
45h
44h
41h
38h
41g
38g
III
45g
44g
30f
45f
44f
41f
38f
41e
38e
45e
44e
II
30d
45d
44d
41d
38d
41c
38c
45c
44c
45b
44b
I
45a
44a
41b
38b
41a
38a
21
29b
25b

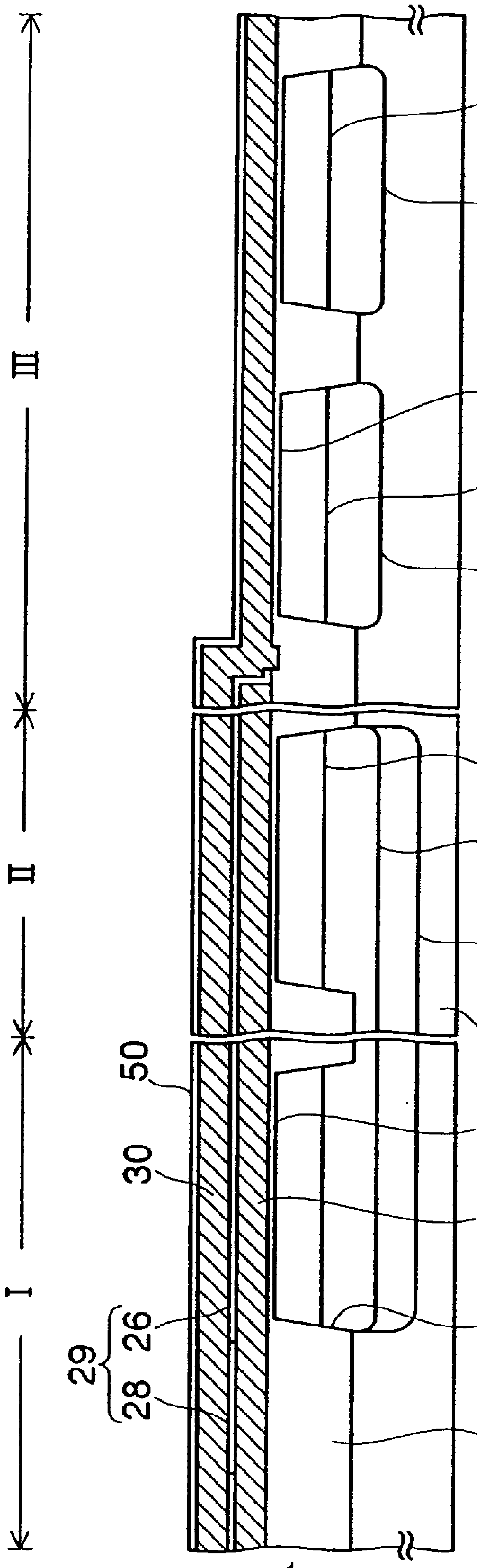


FIG. 12A

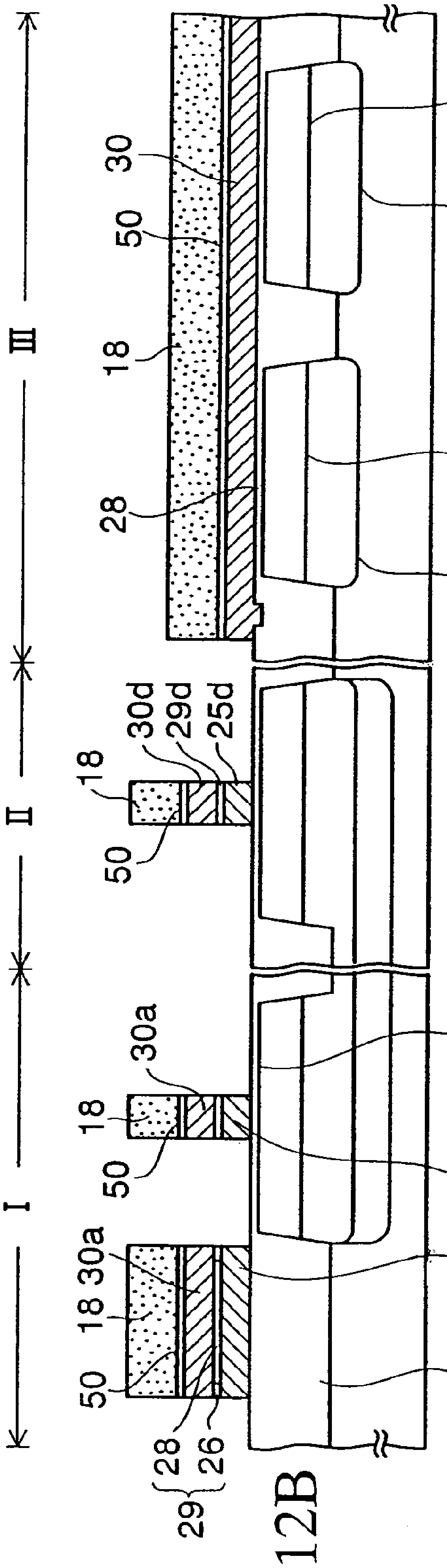


FIG. 12B

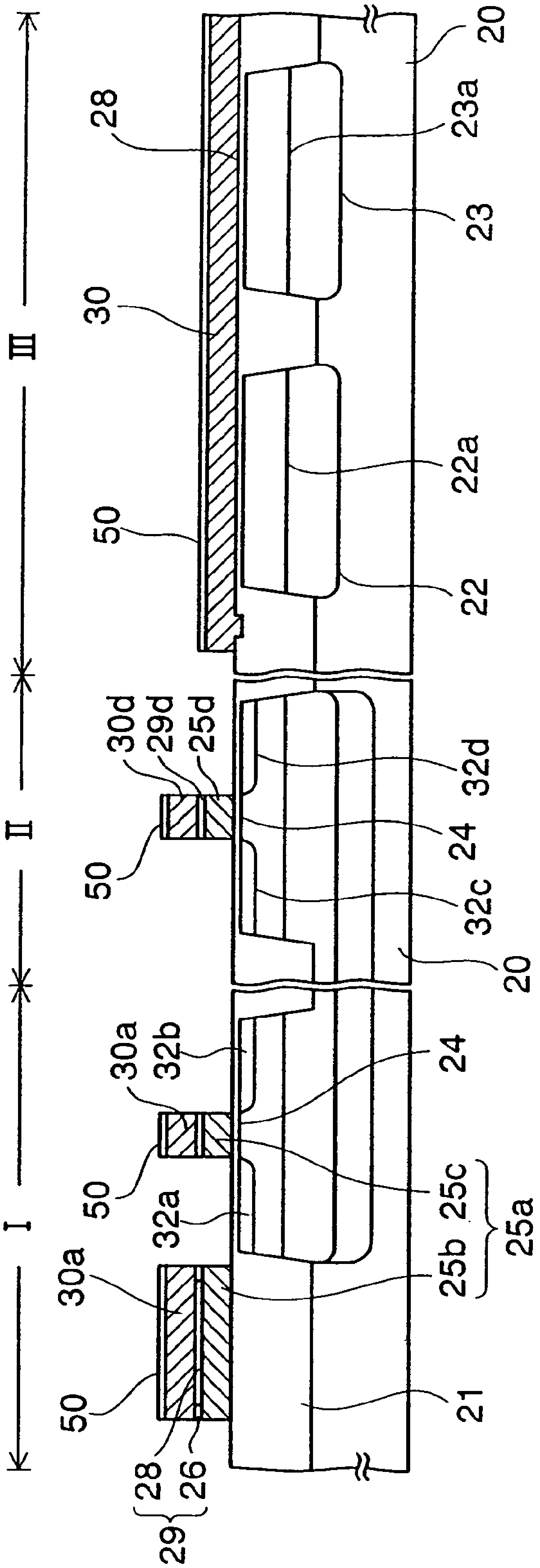

I
II
III
29
28
26
50
30a
21
25b
25a
32a
50
25c
30a
32b
24
20
32c
50
30d
29d
25d
24
32d
50
22
22a
30
23
23a
28
20

FIG. 12C

FIG. 13

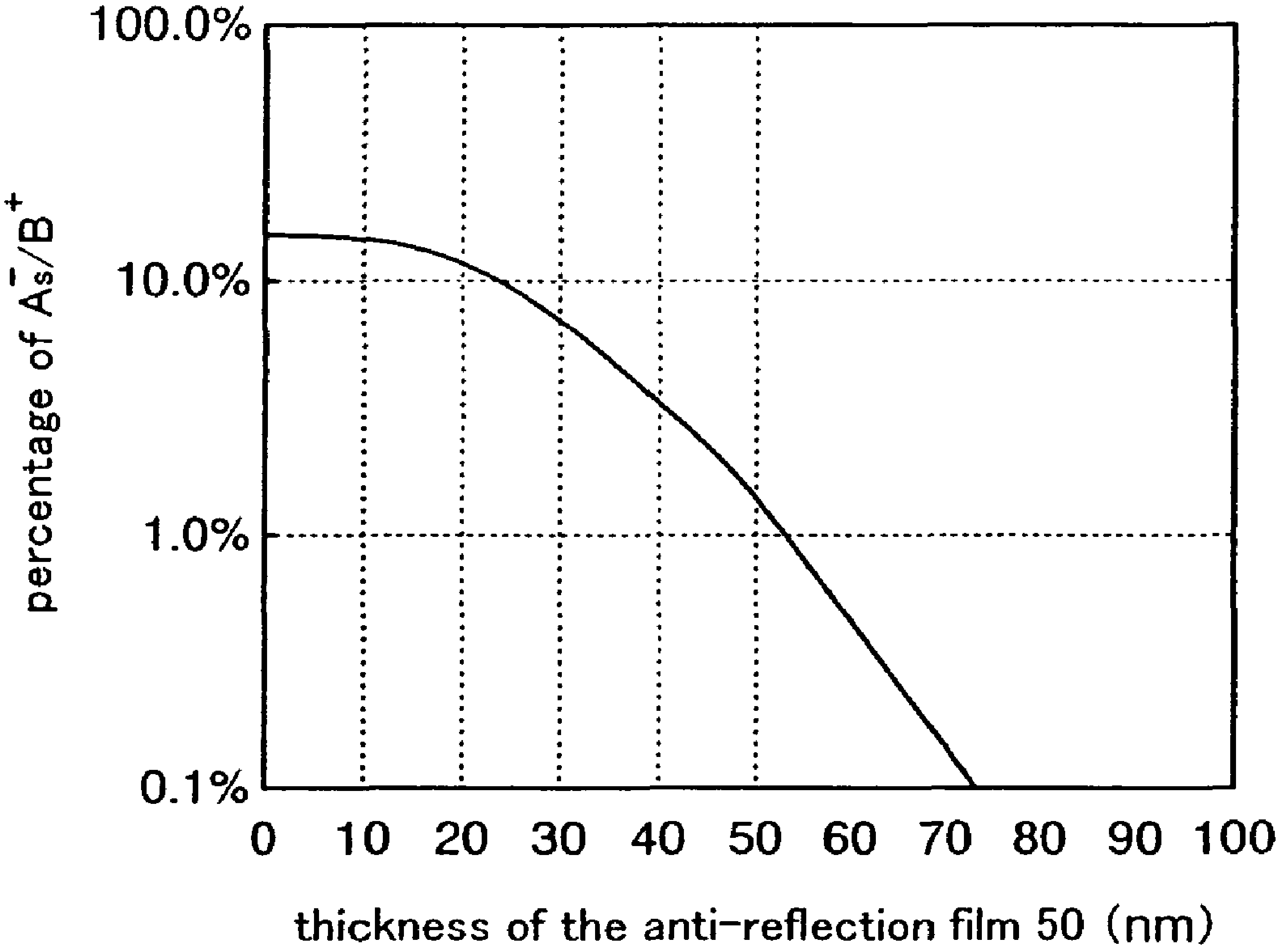

100.0%
10.0%
1.0%
0.1%
percentage of A_s^-/B^+
0
10
20
30
40
50
60
70
80
90
100
thickness of the anti-reflection film 50 (nm)

FIG. 14A

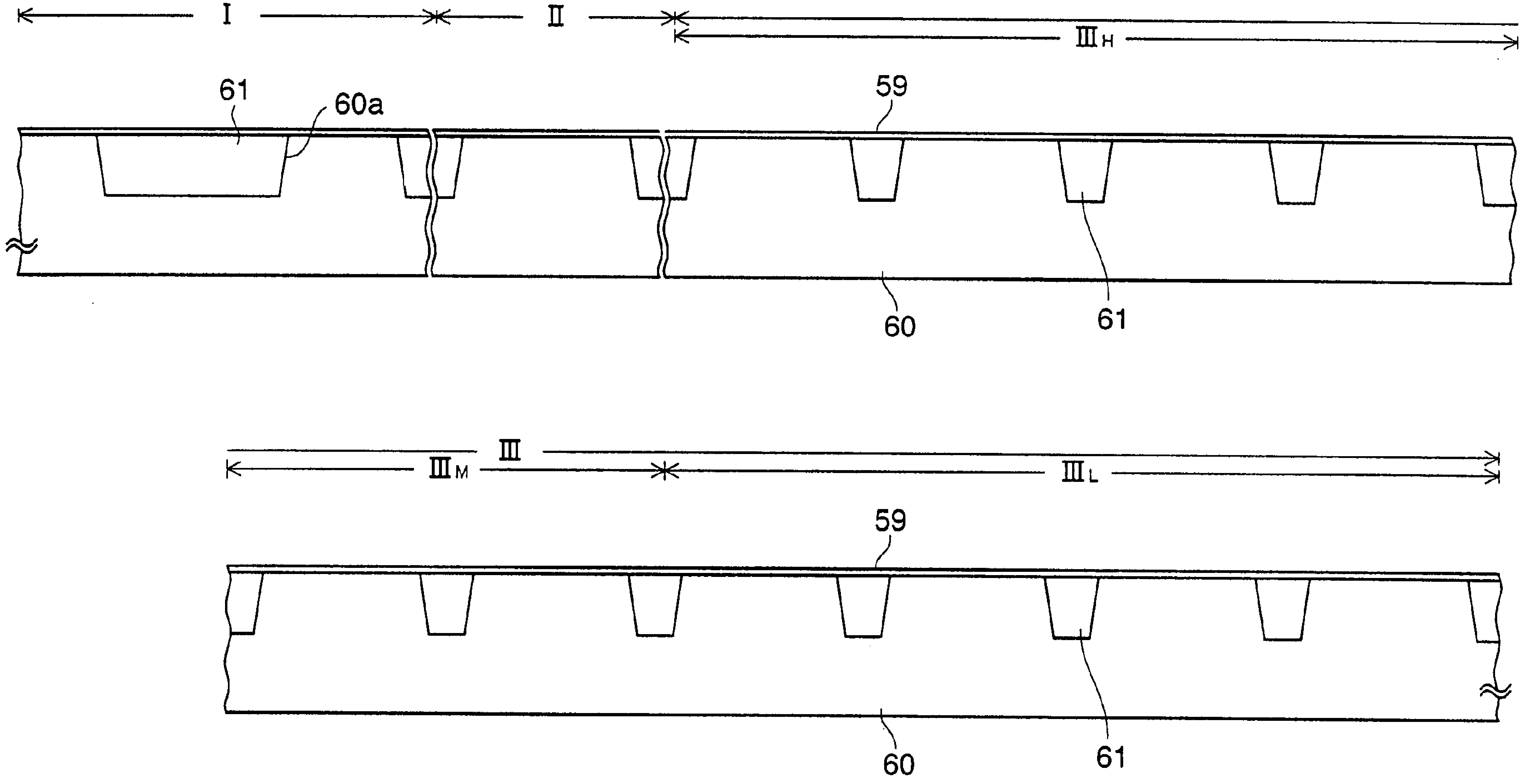

I
II
III_H
61
60a
59
60
61
III
III_M
III_L
59
60
61

FIG. 14B

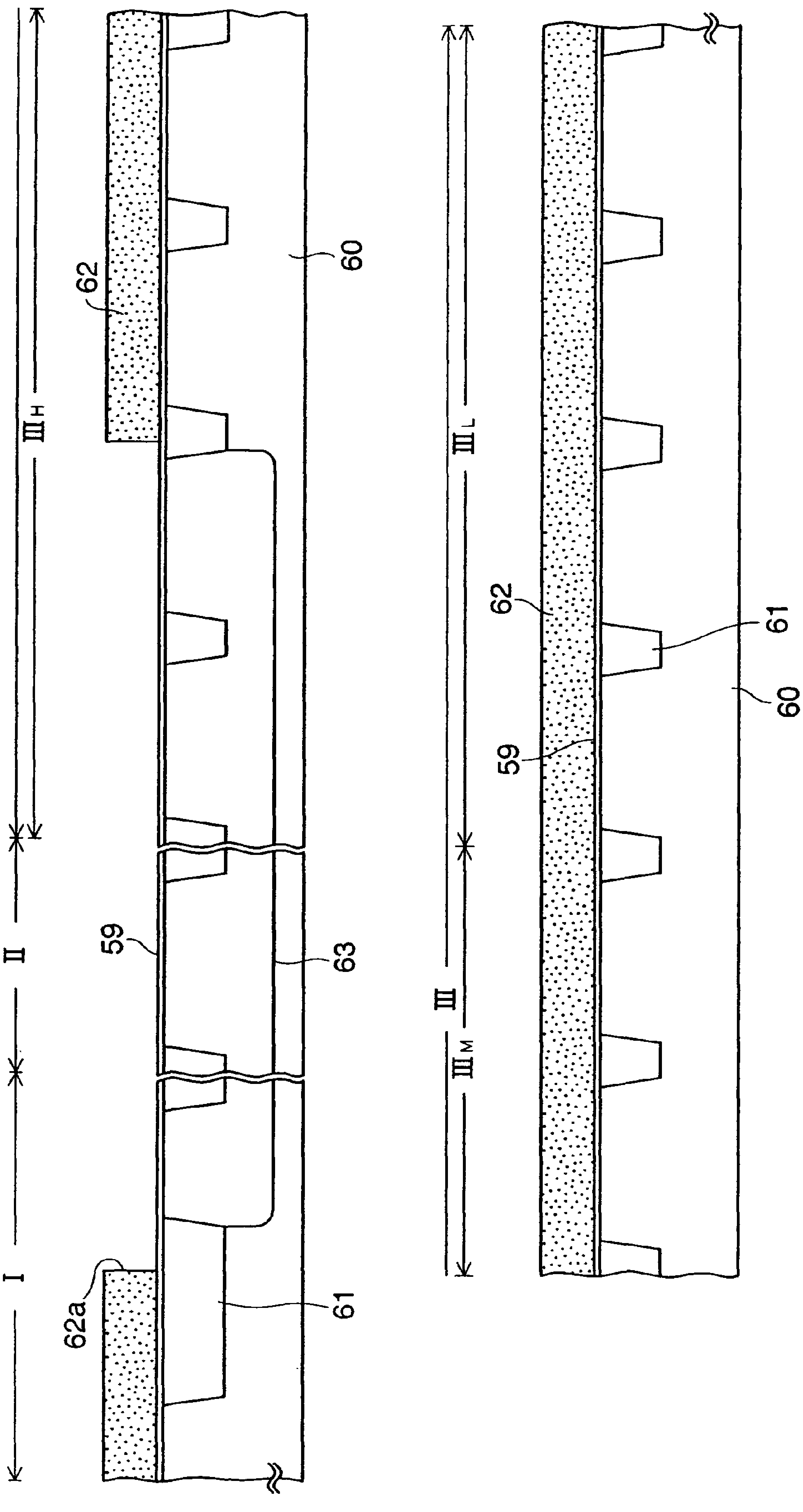
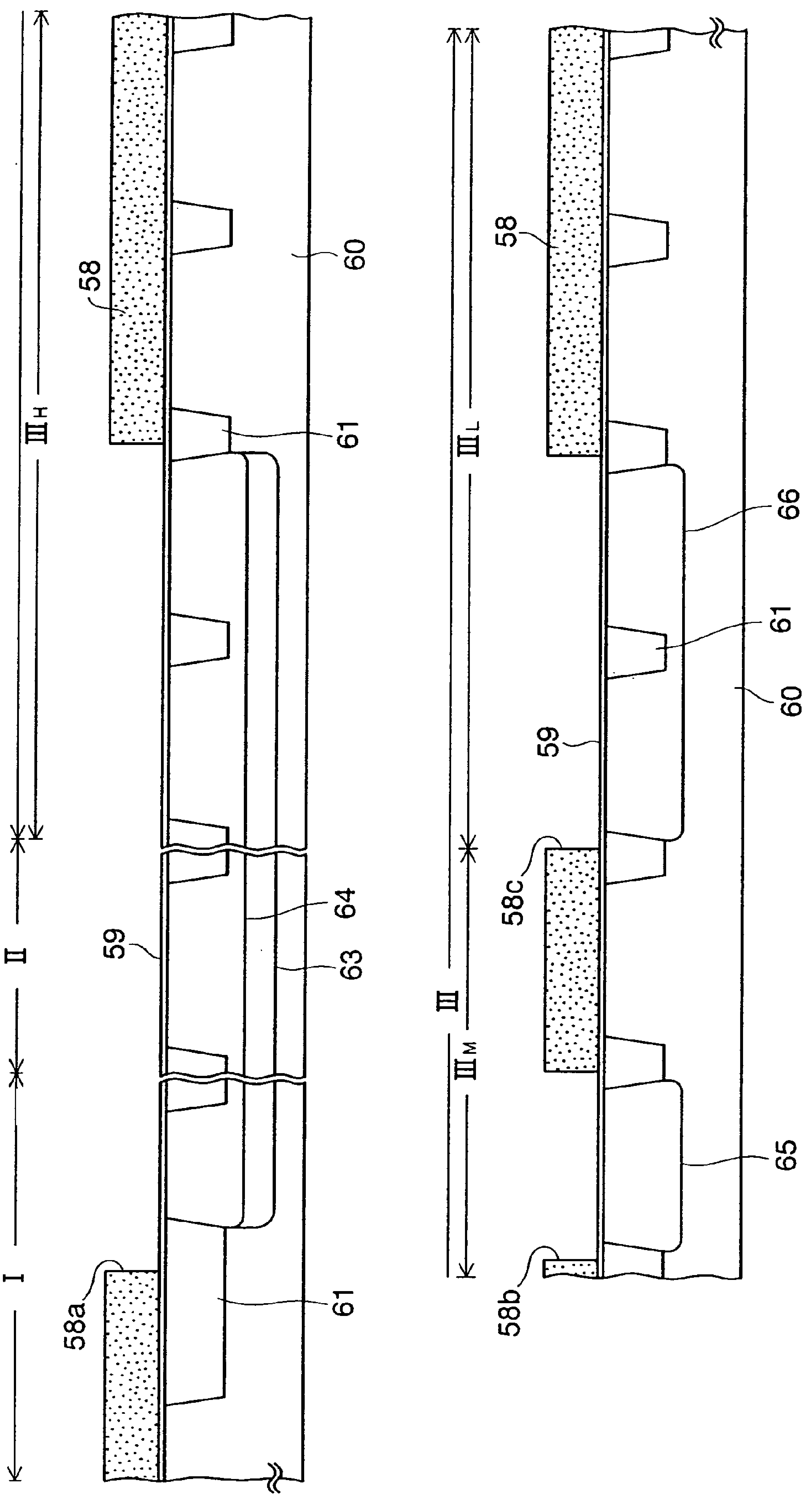

62
60
III_H
II
59
63
I
62a
61
III_L
III
III_M
62
61
59
60

FIG. 14C


III_H
58
60
61
59
64
63
II
I
58a
61
III_L
58
66
61
60
59
58c
III
III_M
65
58b

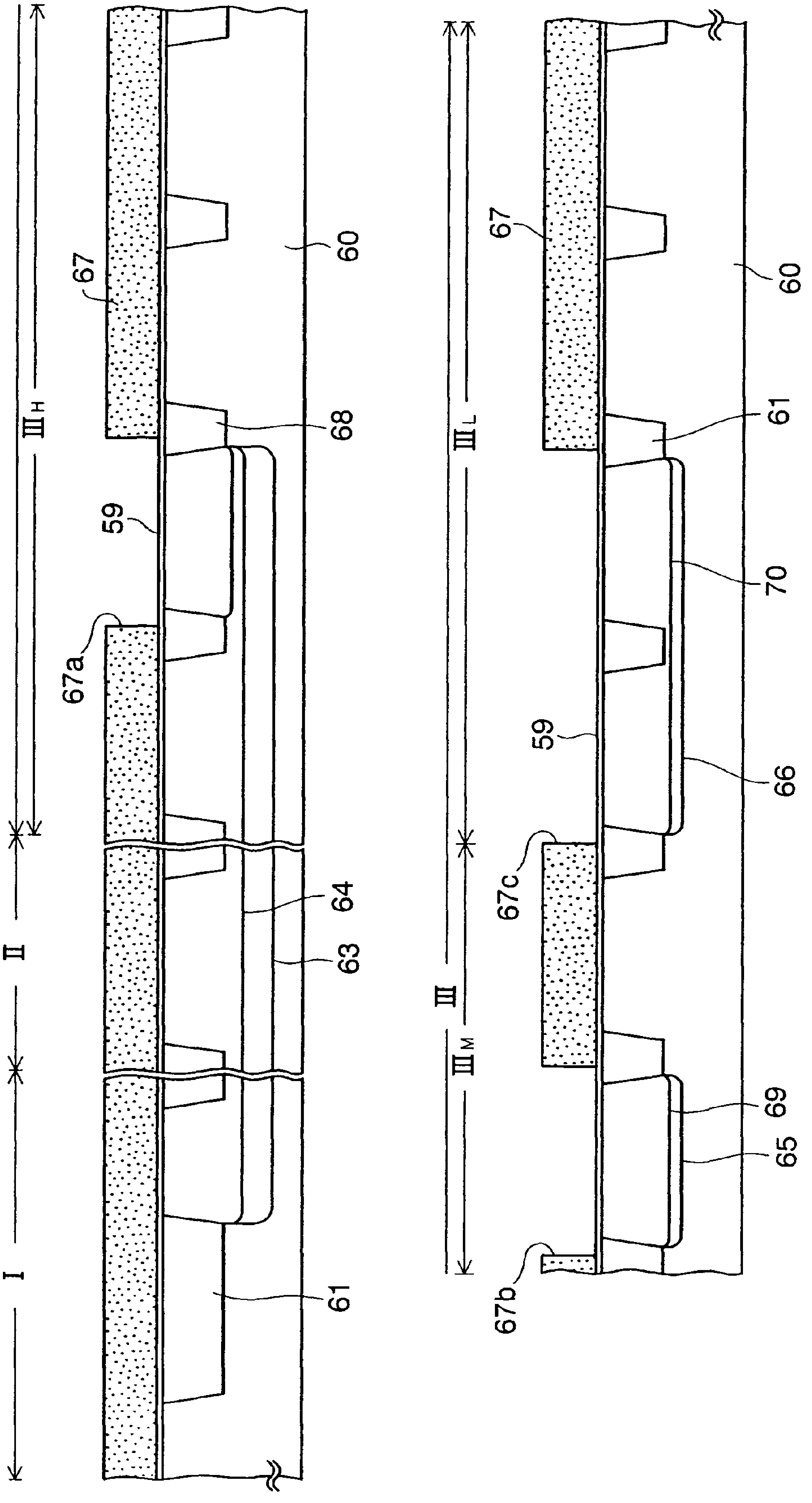

I
II
III_H
61
63
64
67a
59
68
60
67
III
III_M
III_L
67b
65
69
67c
66
59
70
61
60
67

FIG. 14D

FIG. 14E

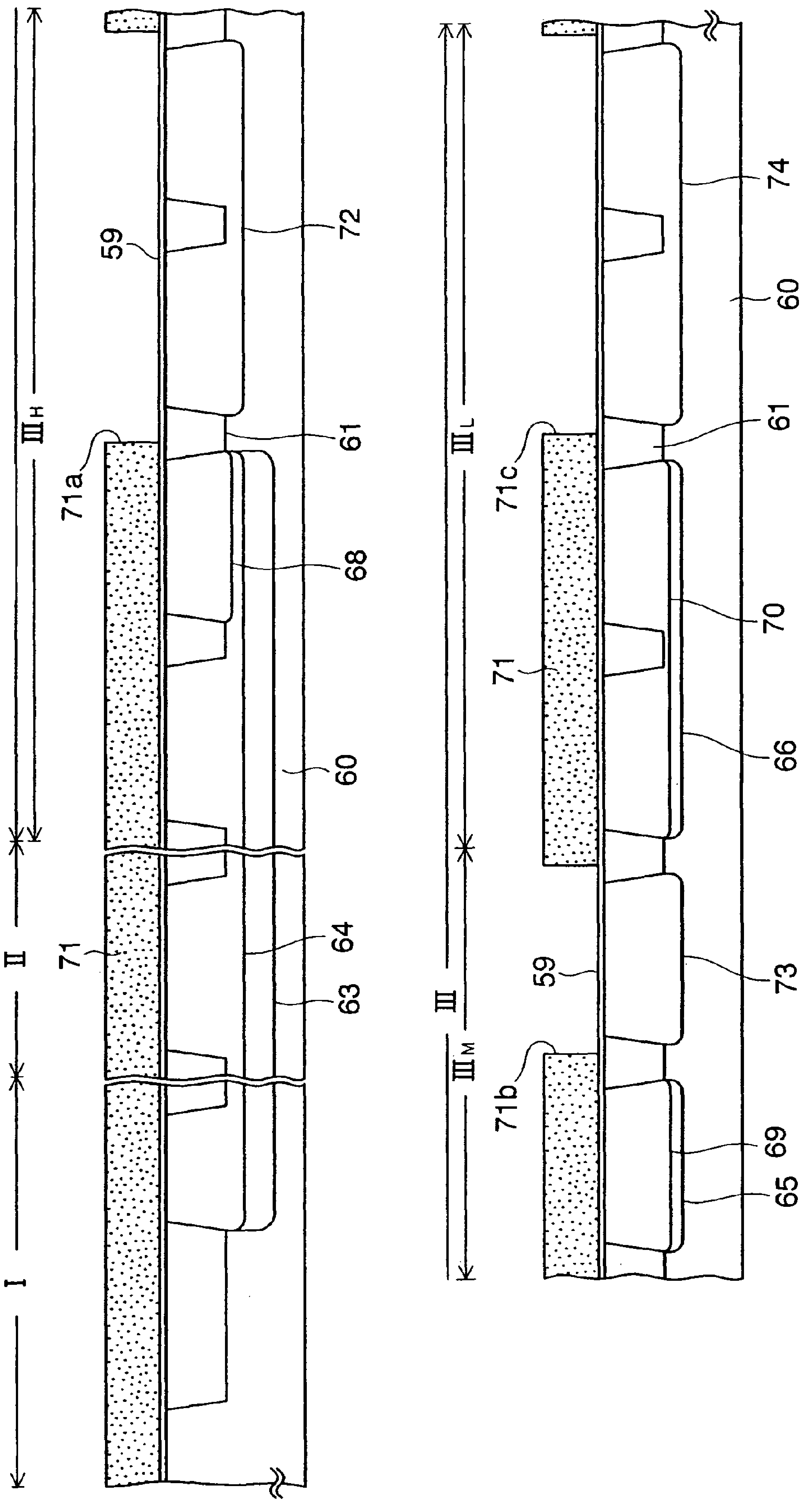

I
II
III_H
71
71a
59
72
61
68
60
64
63
III
III_M
III_L
71b
71c
71
59
74
60
61
70
66
73
69
65

FIG. 14F

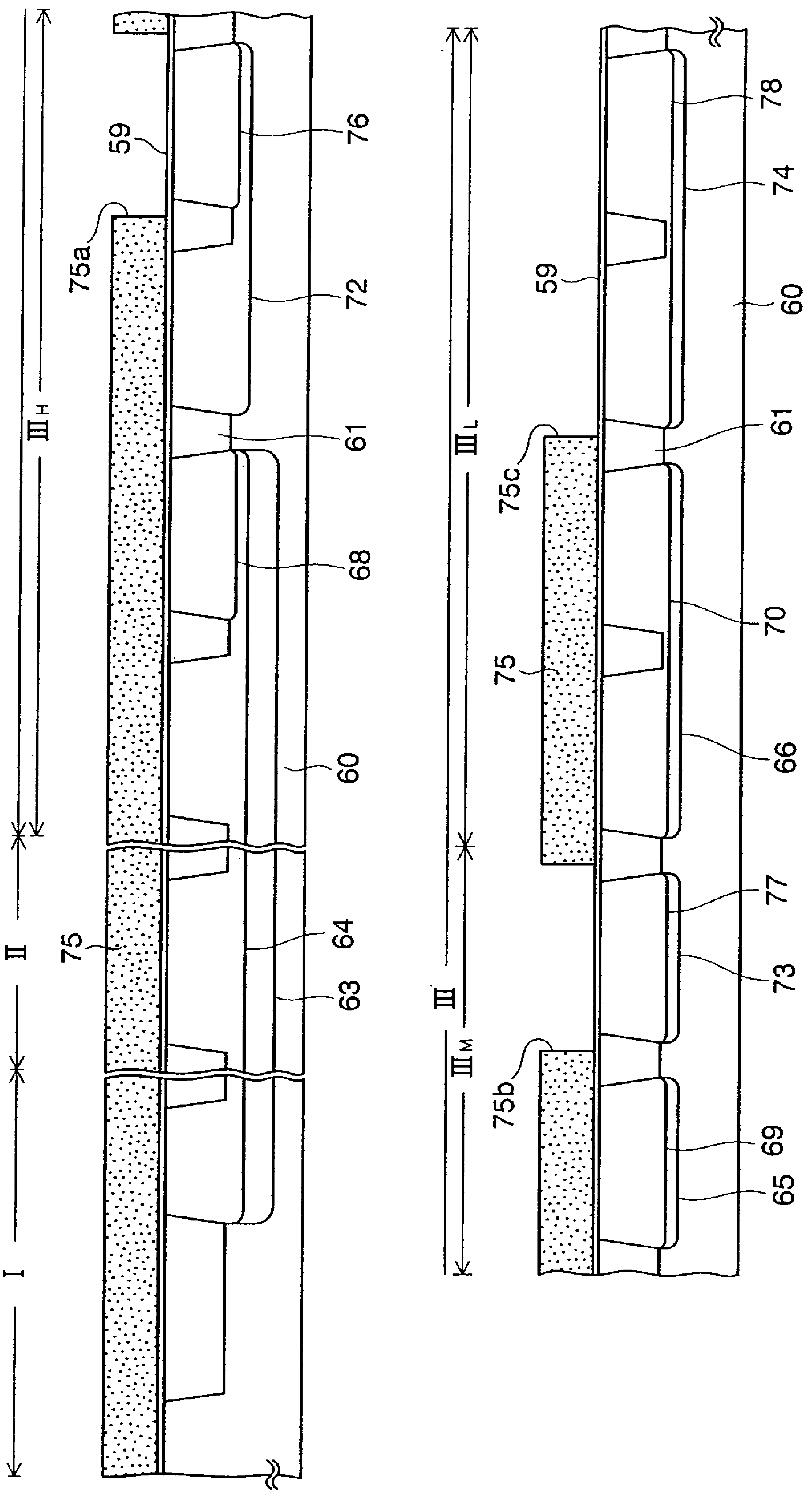

I
II
III_H
III
III_M
III_L
59
75a
75
76
72
61
68
60
64
63
78
74
59
60
61
75c
70
75
66
77
73
75b
69
65

FIG. 14G

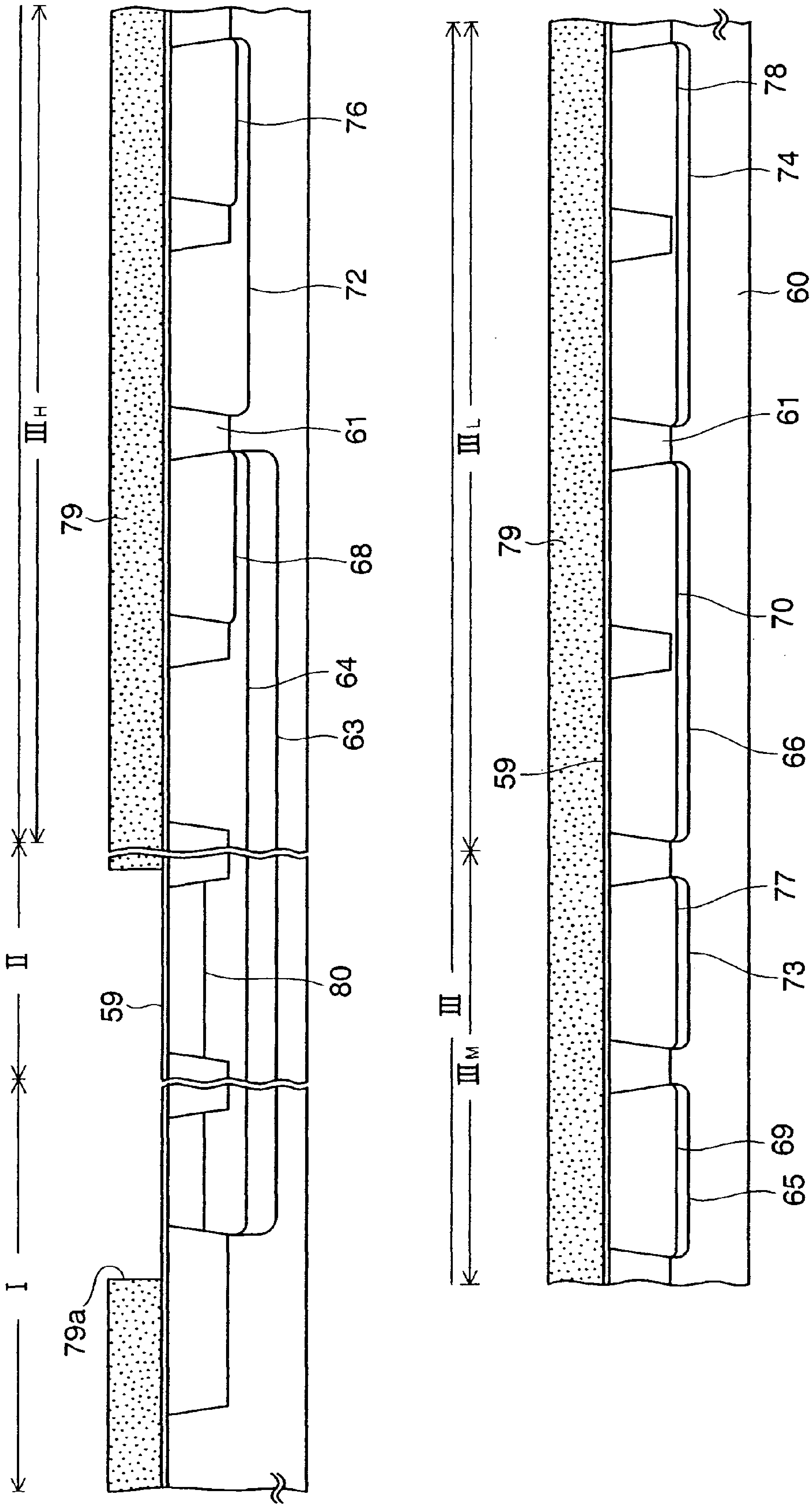

I
II
III_H
79a
59
80
63
64
68
79
61
72
76
III
III_M
III_L
79
59
65
69
73
77
66
70
61
60
74
78

FIG. 14H

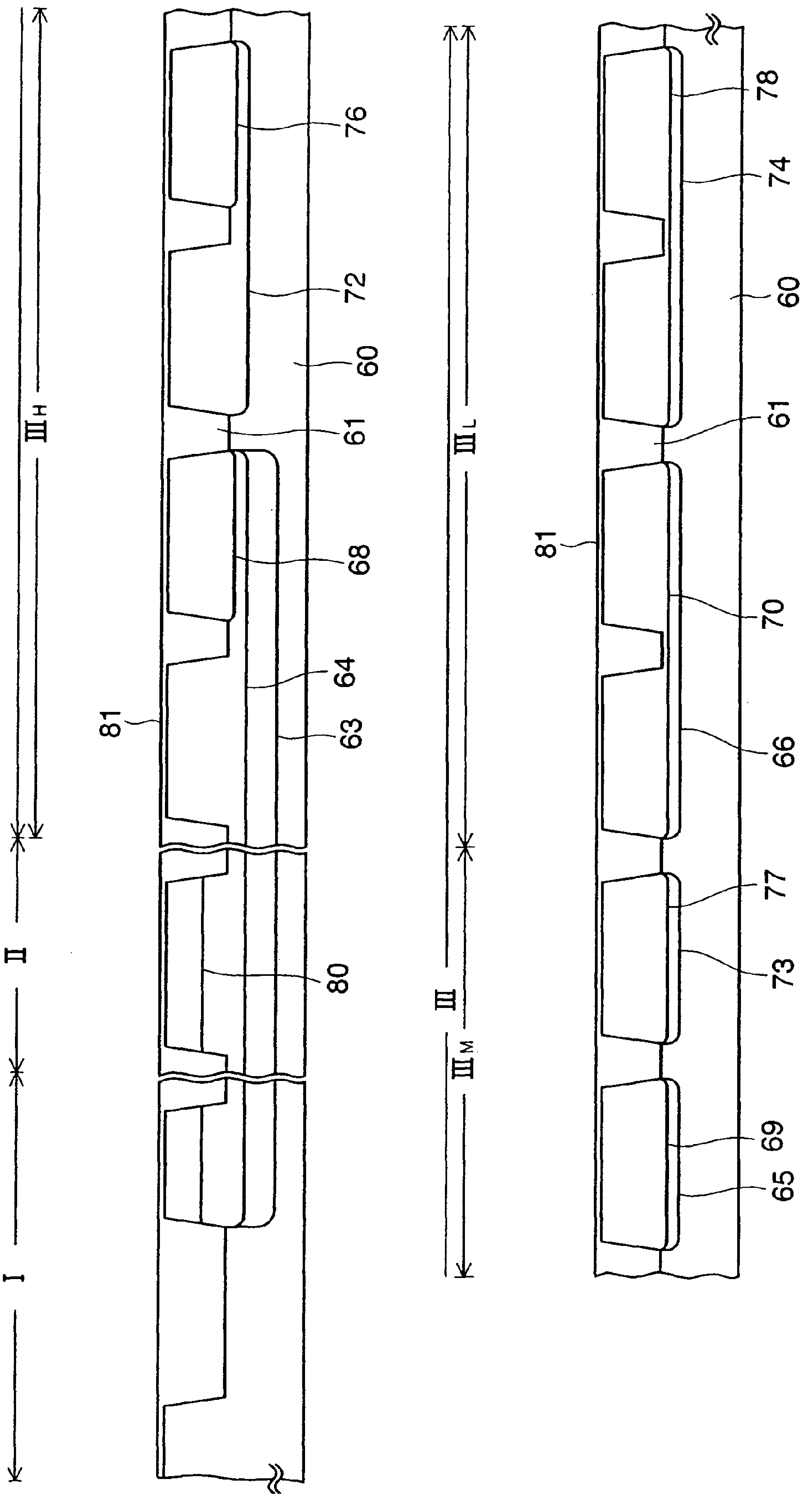
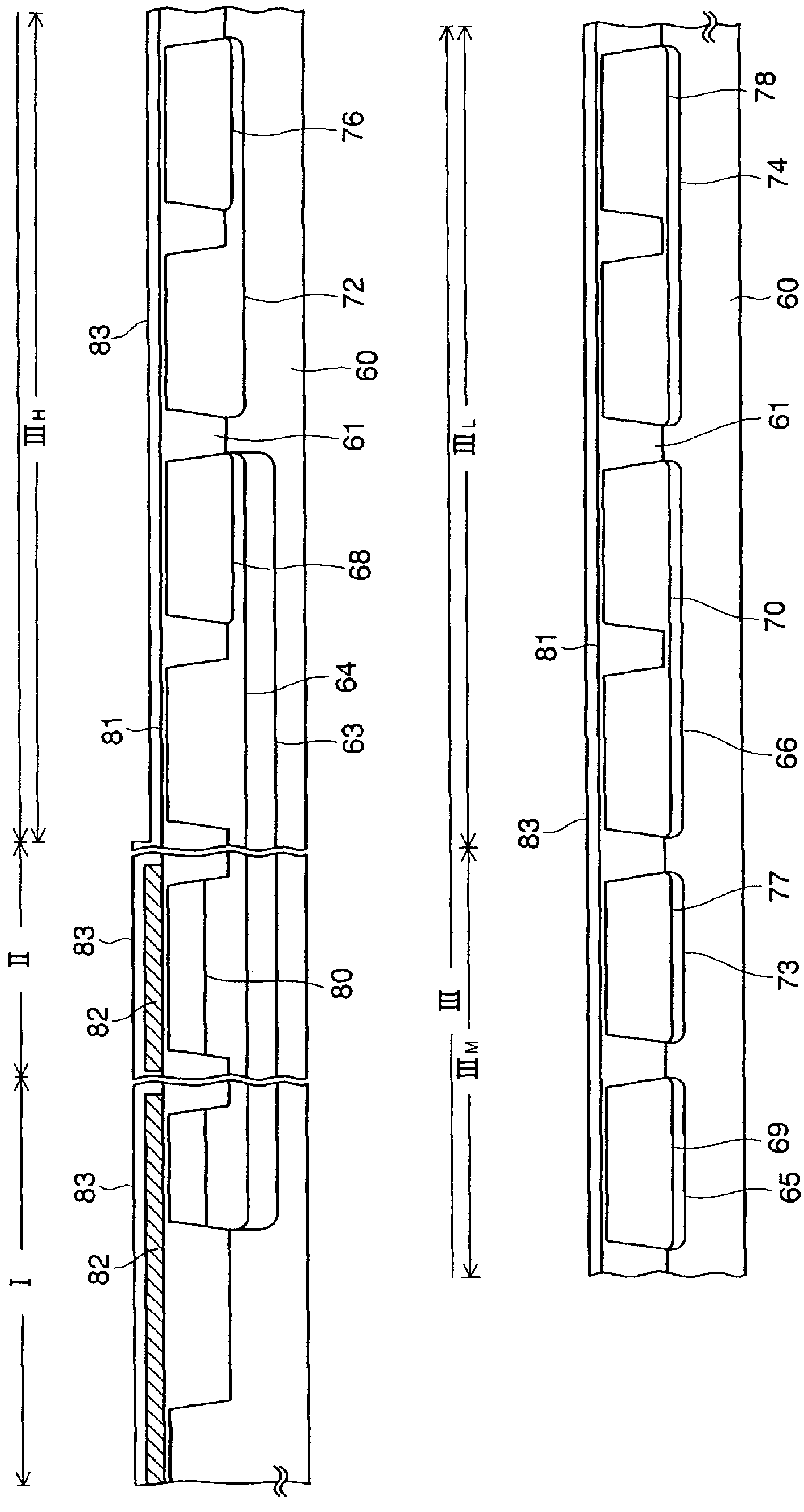

I
II
III_H
76
72
60
61
68
64
63
81
80
III_M
III
III_L
78
74
60
61
81
70
66
77
73
69
65

FIG. 14I



I
II
III_H
III
III_M
III_L
83
82
83
82
80
81
63
64
68
61
60
72
83
76
65
69
73
77
83
66
81
70
61
60
74
78

FIG. 14J

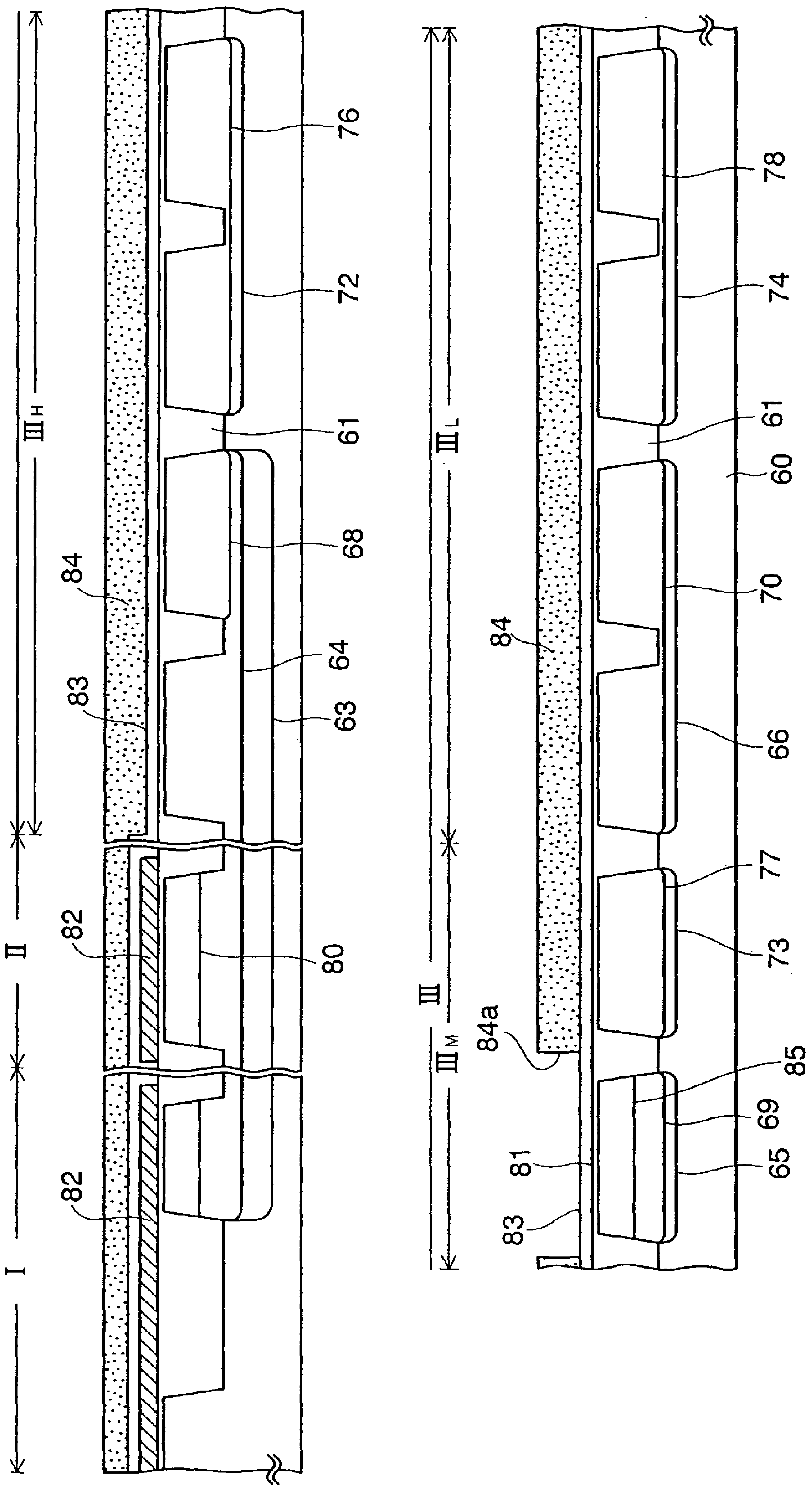

I
II
III_H
84
83
82
82
80
76
72
61
68
64
63
III_L
III
III_M
84
84a
78
74
61
60
70
66
77
73
85
69
65
81
83

FIG. 14K

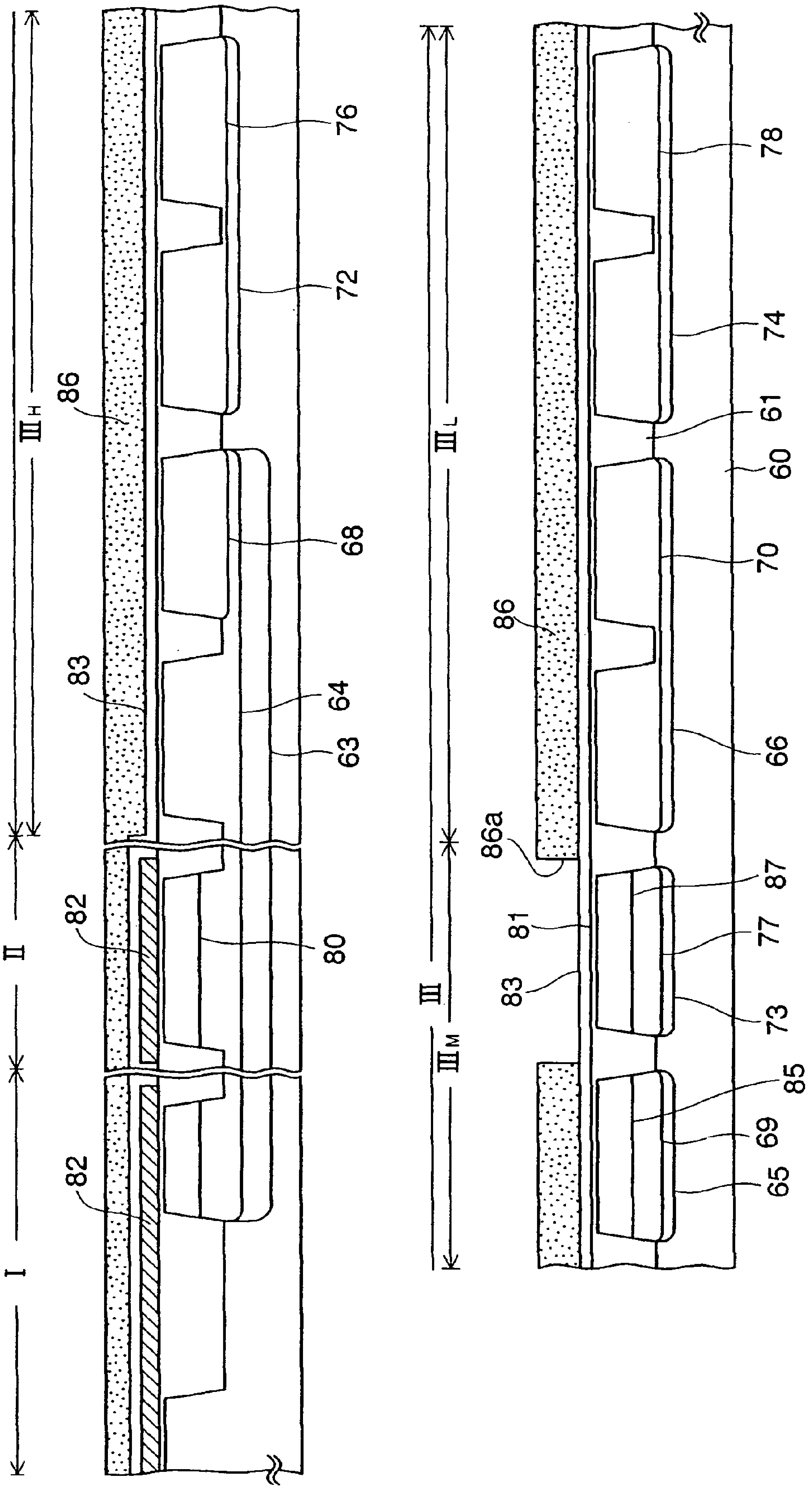

I
II
III_H
86
83
82
82
80
76
72
68
64
63
III
III_M
III_L
86
86a
81
83
78
74
61
60
70
66
87
77
73
85
69
65

FIG. 14L

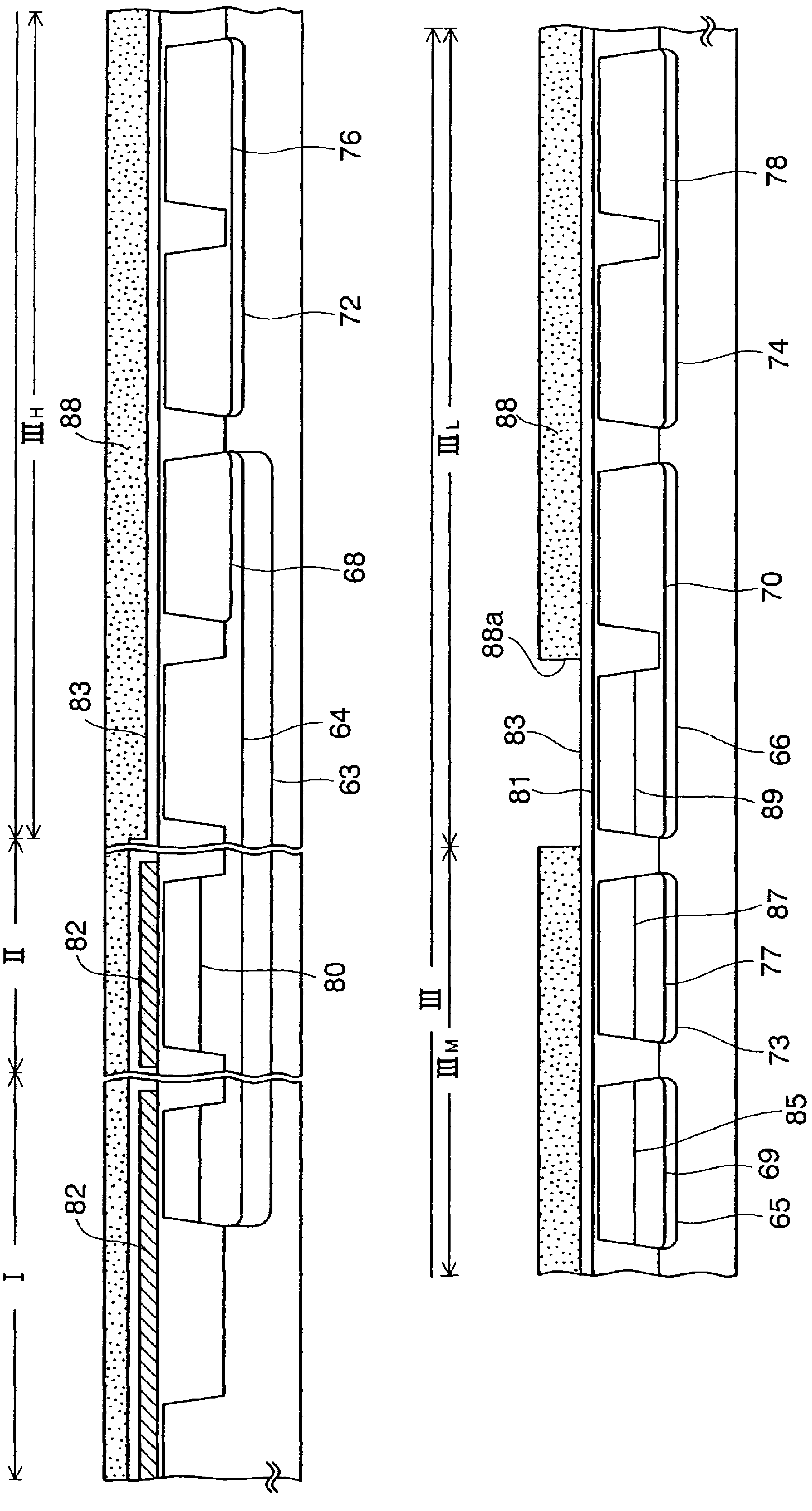

I
II
III_H
88
83
82
82
80
76
72
68
64
63
III
III_M
III_L
88
88a
83
81
78
74
70
66
89
87
77
73
85
69
65

FIG. 14M

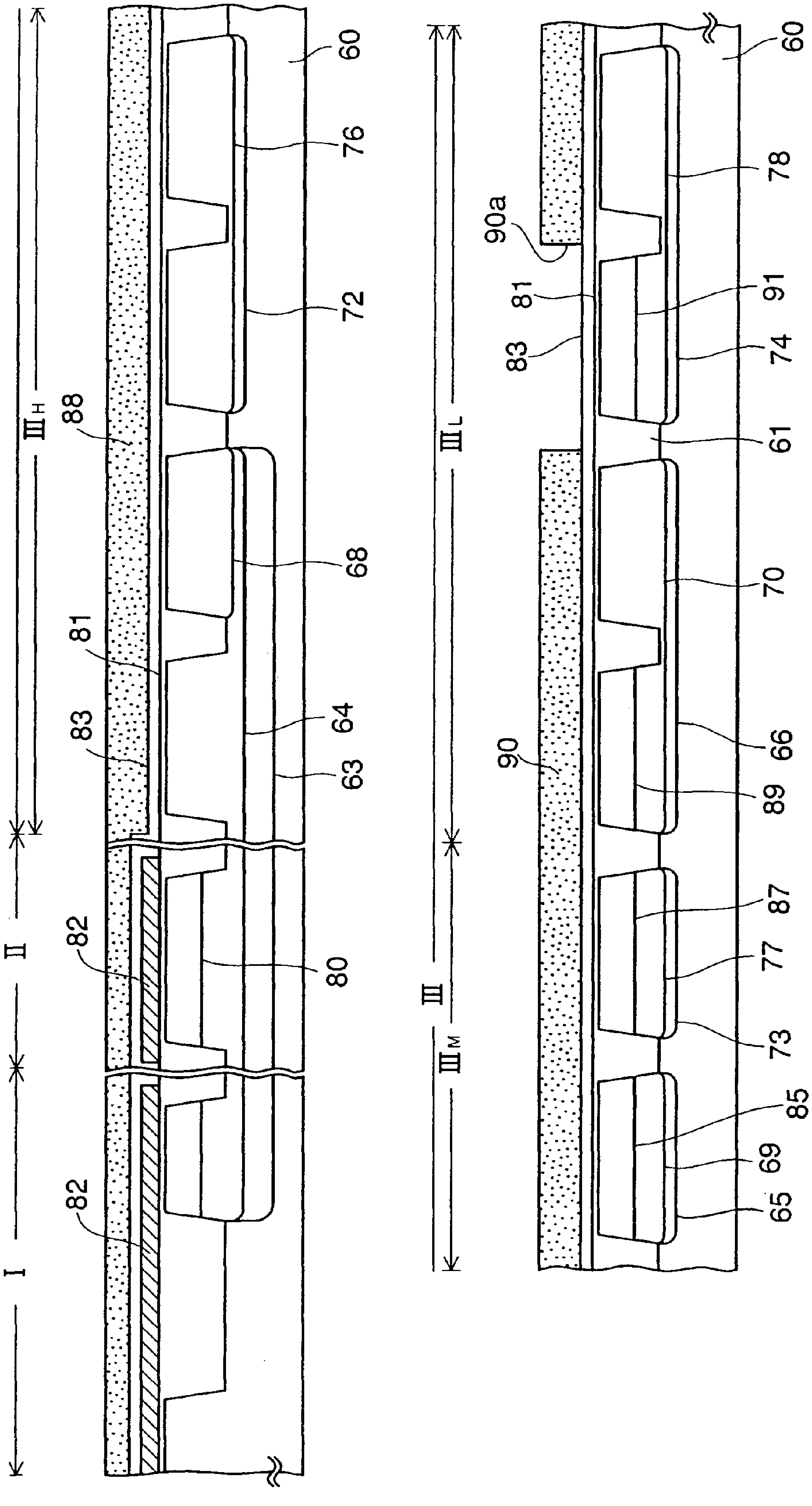

I
II
IIIH
82
82
80
83
81
88
64
63
68
72
76
60
IIIM
III
IIIL
90
90a
83
81
65
69
85
73
77
87
89
66
70
61
74
91
78
60

FIG. 14N

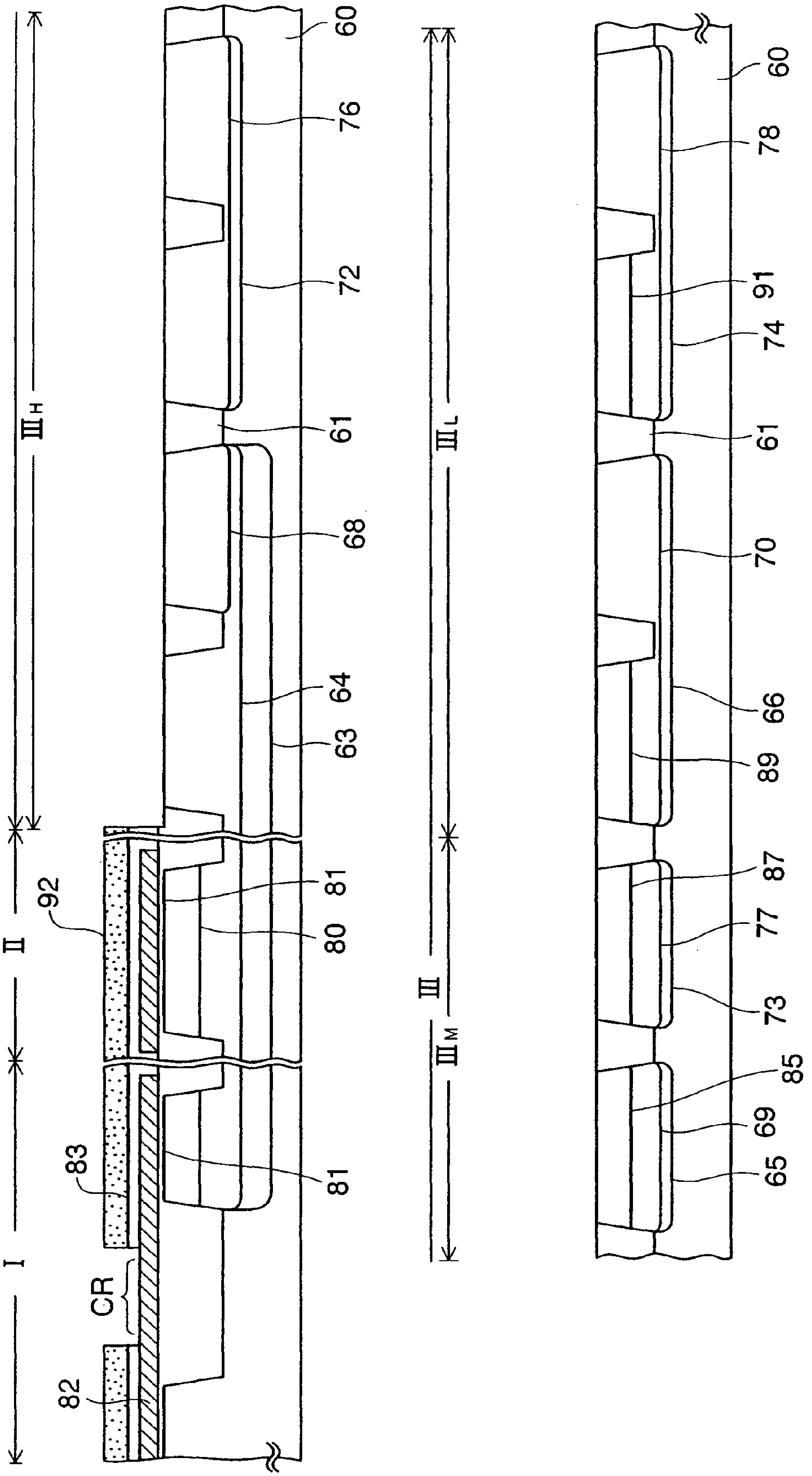

I
II
III_H
III_L
III
III_M
CR
60
76
72
61
68
64
63
81
80
92
83
82
81
60
78
91
74
61
70
66
89
87
77
73
85
69
65

FIG. 14O

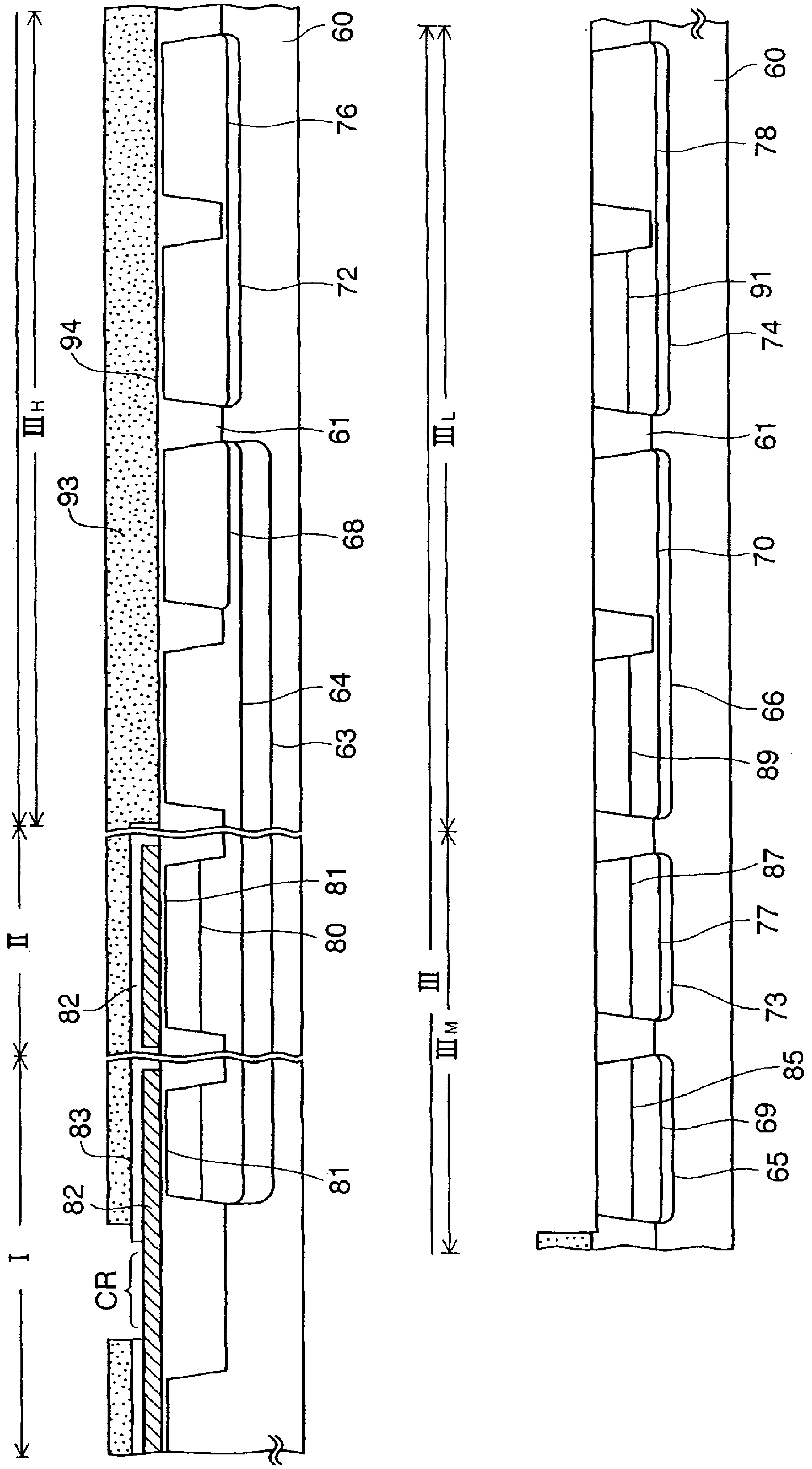
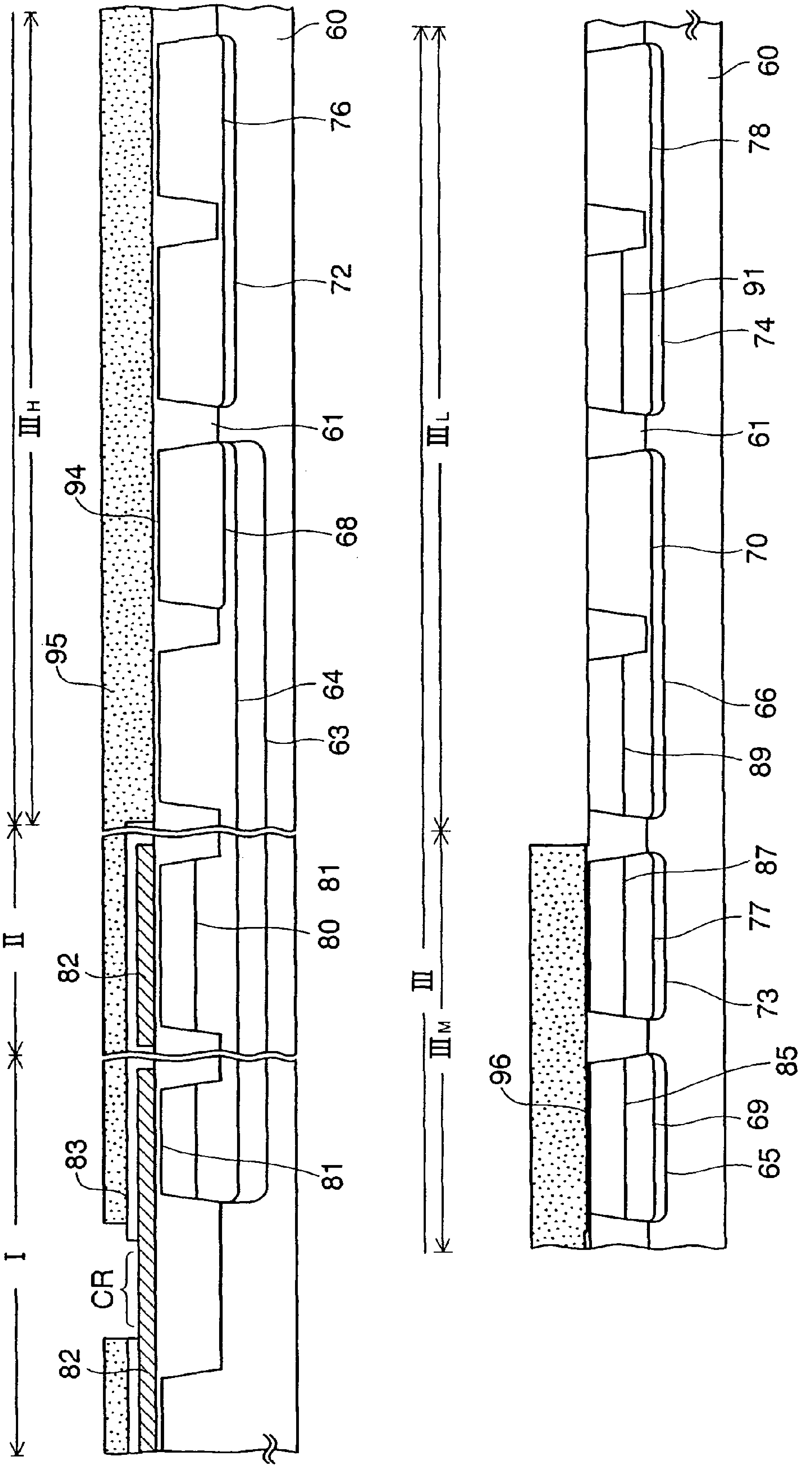

I
CR
82
83
81
II
82
80
81
IIIH
93
94
61
68
64
63
72
76
60
III
IIIM
IIIL
65
69
85
73
77
87
89
66
70
61
74
91
78
60

FIG. 14P



I
82
CR
83
81
II
82
80
81
III_H
95
94
63
64
68
61
72
76
60
III_M
III
III_L
96
65
69
85
73
77
87
89
66
70
61
74
91
78
60

FIG. 14Q

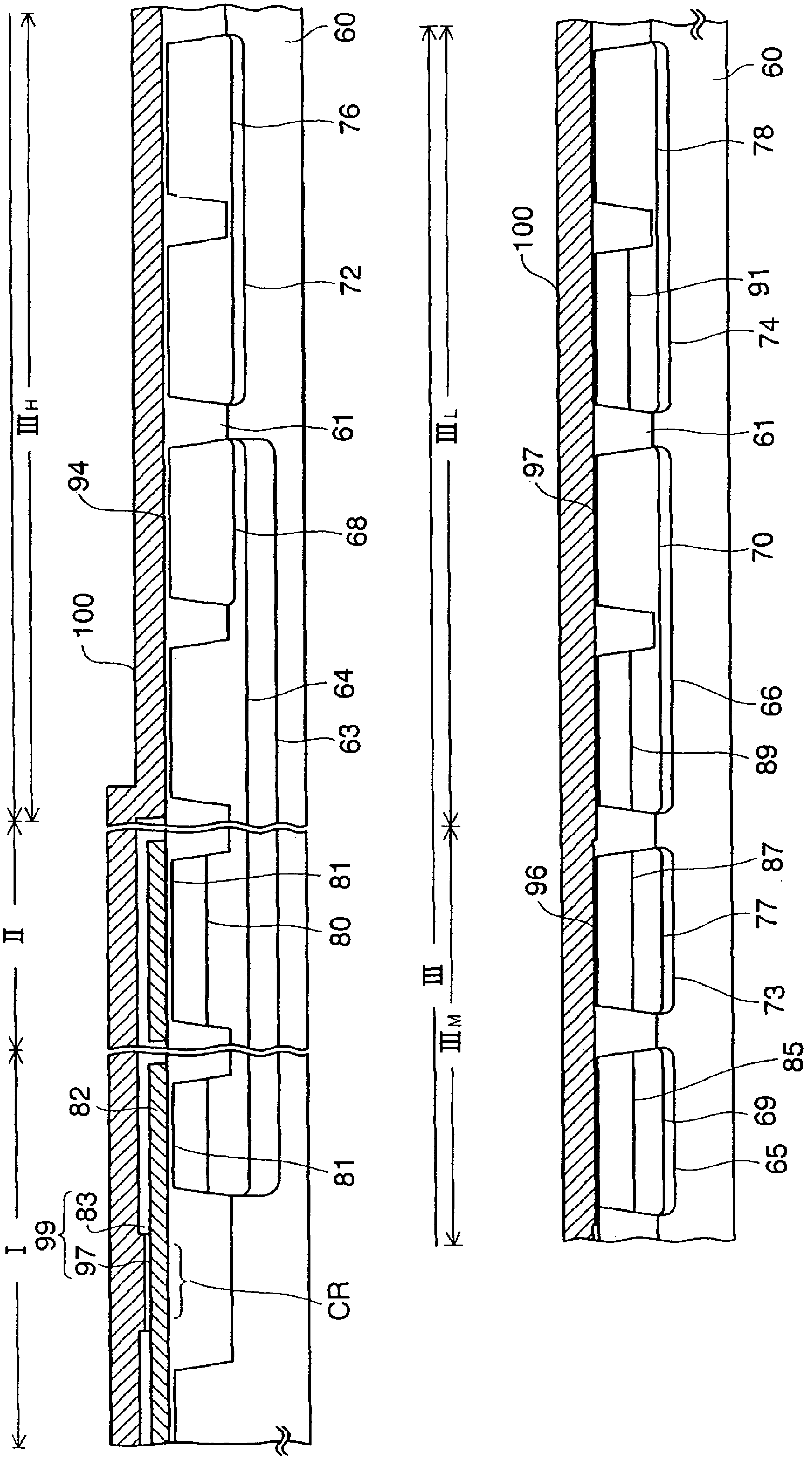

60
76
72
61
94
68
100
64
63
81
80
82
83
99
97
CR
III_H
II
I
III_L
III
III_M
60
78
100
91
74
61
97
70
66
89
87
77
73
96
85
69
65

FIG. 14R

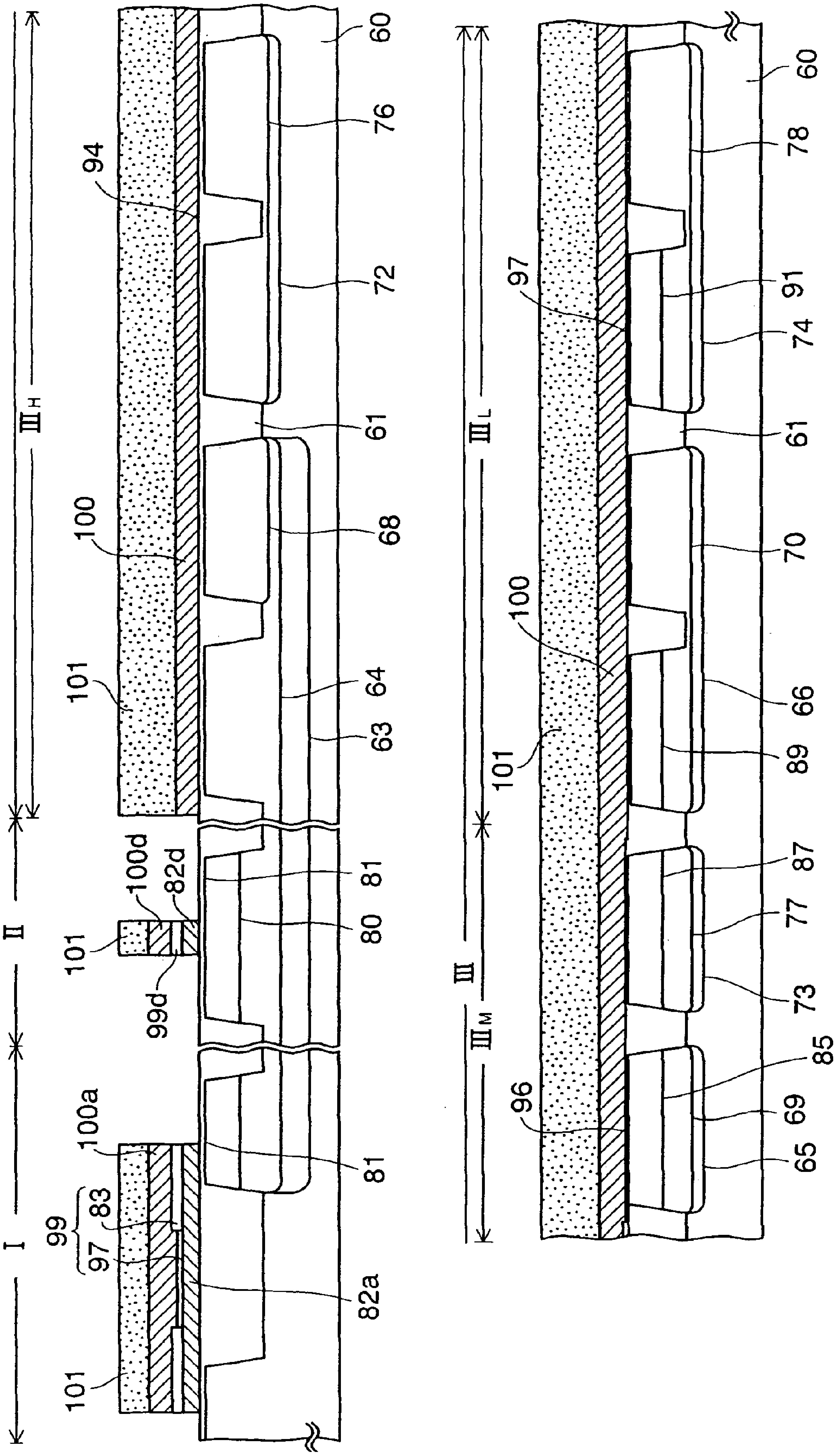

I
II
III_H
III
III_M
III_L
60
76
94
72
61
100
68
101
64
63
100d
82d
81
80
99d
101
100a
99
83
97
82a
101
81
60
78
97
91
74
61
100
70
101
66
89
87
77
73
85
69
65
96

FIG. 14S

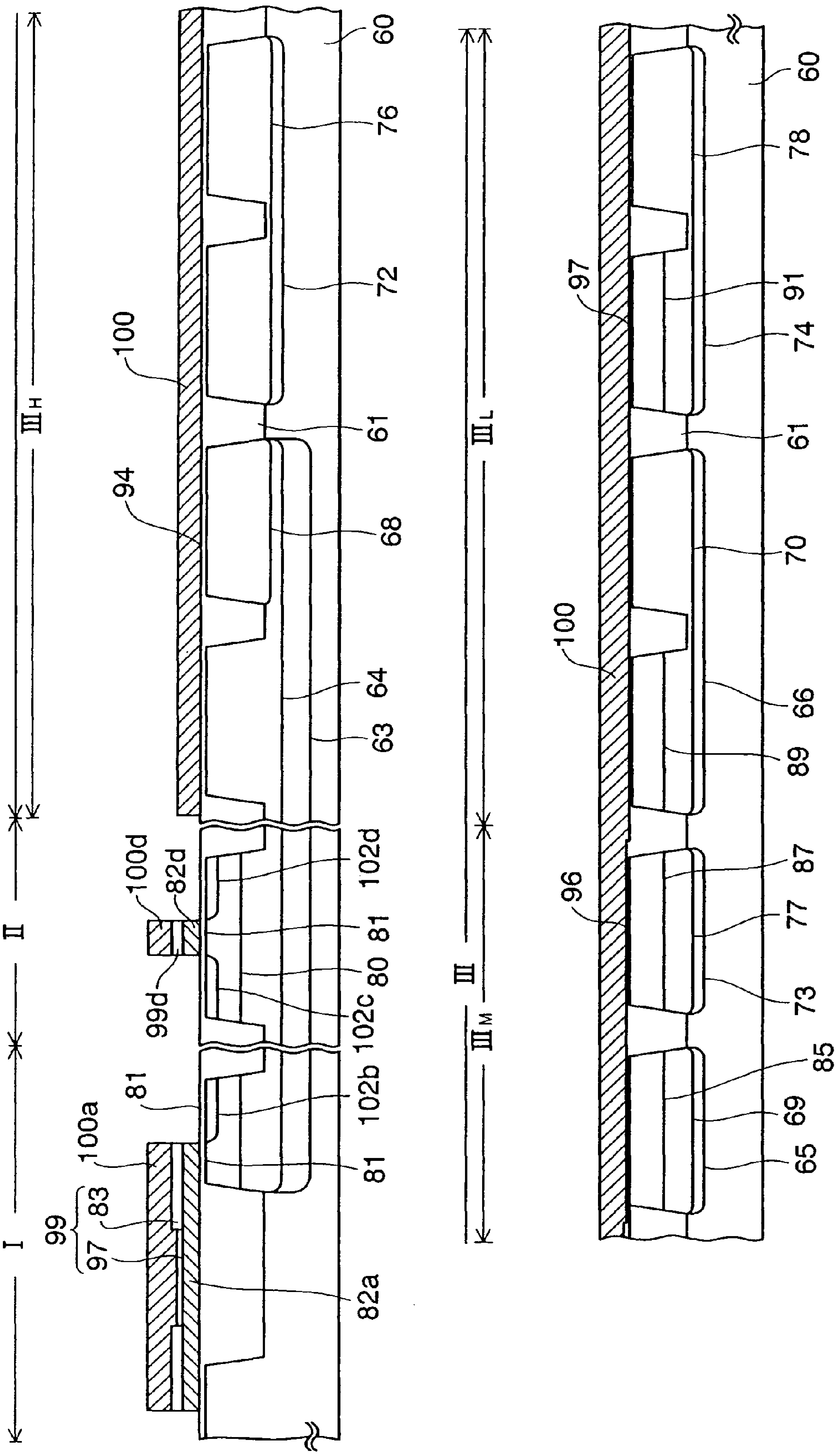

I
II
III
III_H
III_M
III_L
99
97
83
100a
81
82a
102b
100d
82d
99d
80
102c
102d
100
94
60
76
72
61
68
64
63
96
97
85
69
65
73
77
87
89
66
70
74
91
78

FIG. 14T

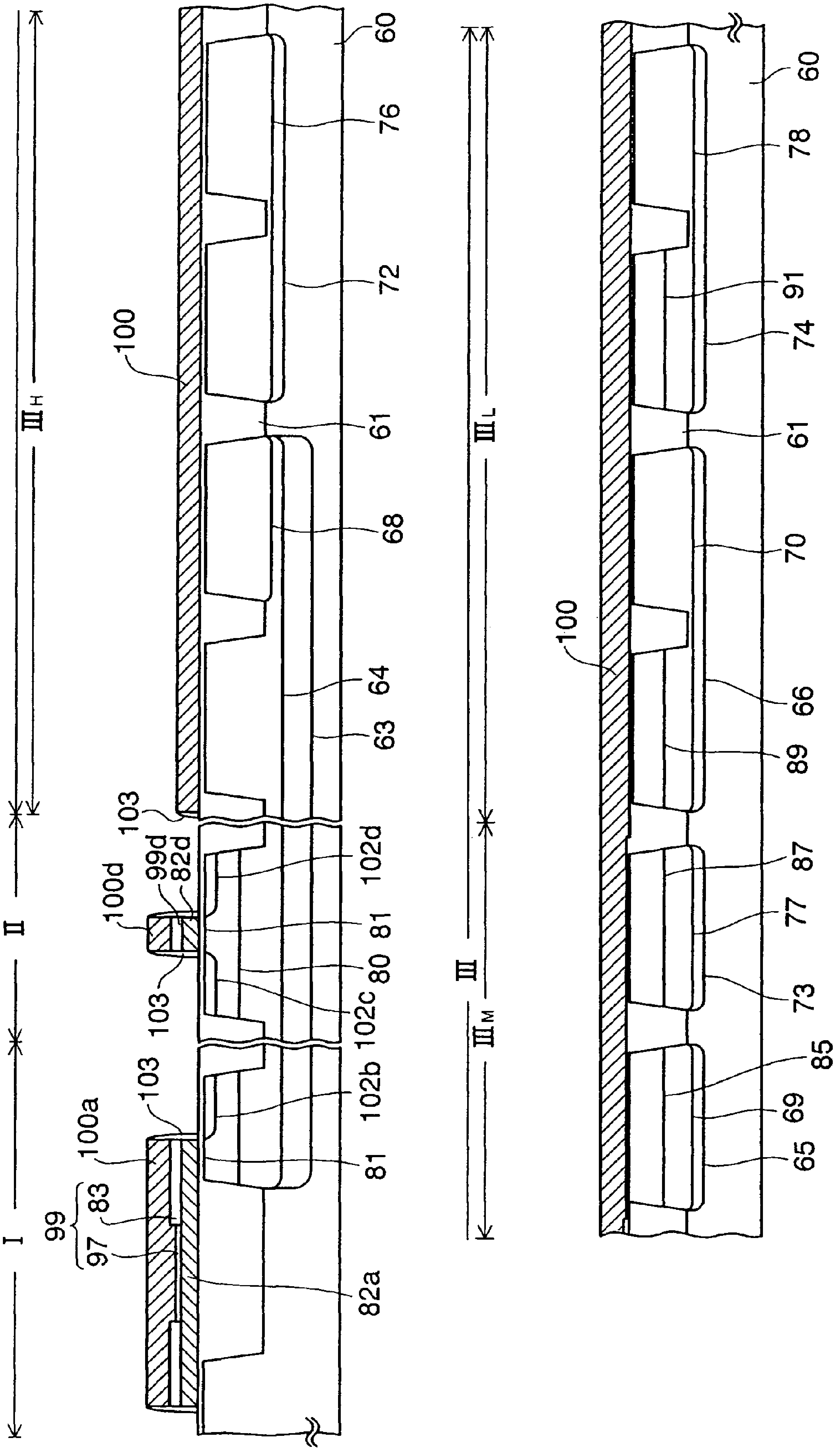

I
II
III
ⅢH
ⅢM
ⅢL
60
76
72
100
61
68
64
63
103
102d
99d
82d
100d
81
80
102c
103
102b
103
100a
81
99
83
97
82a
60
78
91
74
61
70
100
66
89
87
77
73
85
69
65

FIG. 14U

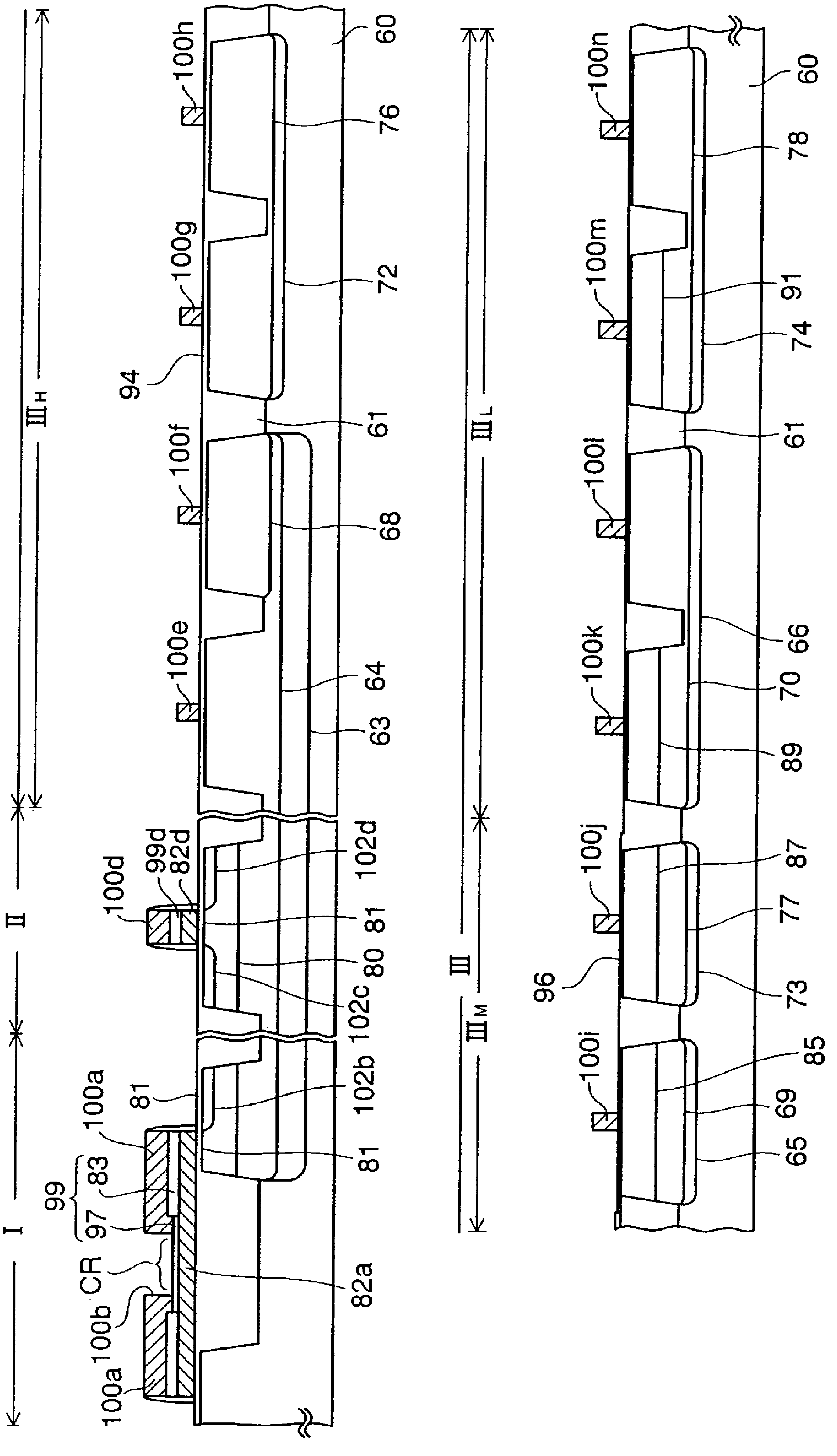

I
II
III_H
III
III_M
III_L
100a
100b
CR
99
97
83
100a
82a
81
81
102b
100d
99d
82d
102d
81
80
102c
100e
100f
100g
100h
94
63
64
68
61
72
76
60
100i
100j
100k
100l
100m
100n
96
65
69
85
73
77
87
89
70
66
61
74
91
78
60

FIG. 14V

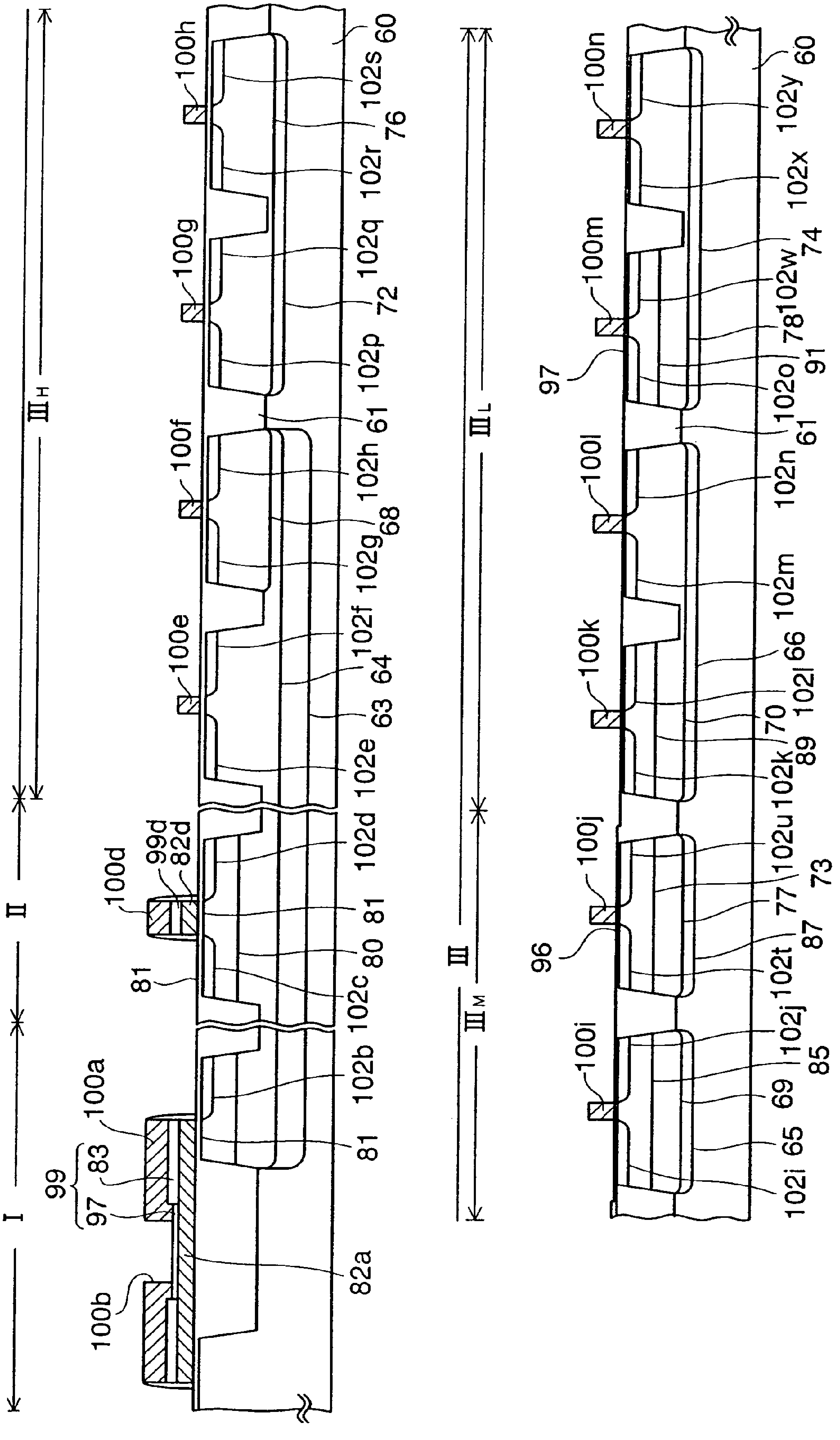

I
II
III
III_H
III_M
III_L
99
97
83
100a
100b
82a
81
102b
100d
99d
82d
81
80
81
102c
102d
100e
102e
63
64
102f
100f
102g
68
102h
61
100g
102p
72
102q
100h
102r
76
102s
60
100i
102i
65
69
85
102j
96
100j
102t
87
77
73
102u
100k
102k
89
70
102l
66
102m
100l
102n
61
97
100m
102o
91
78
102w
74
102x
100n
102y
60

FIG. 14W

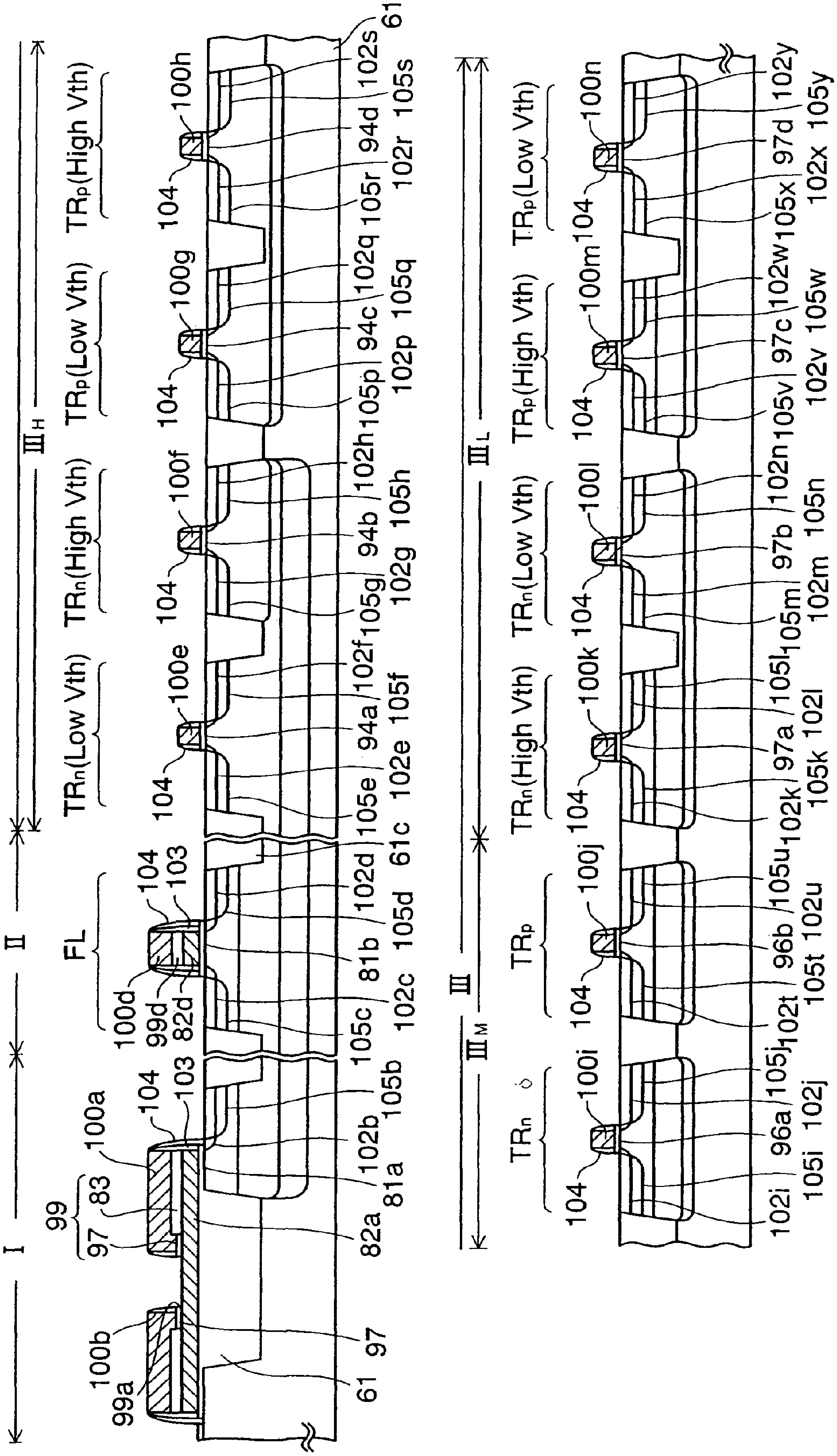

I
II
III
IIIH
IIIM
IIIL
99
97
83
99a
100b
100a
104
103
97
61
82a
81a
102b
105b
FL
100d
99d
82d
104
103
105c
102c
81b
105d
102d
61c
TRn(Low Vth)
104
100e
105e
102e
94a
105f
102f
TRn(High Vth)
104
100f
105g
102g
94b
105h
102h
TRp(Low Vth)
104
100g
105p
102p
94c
105q
102q
TRp(High Vth)
104
100h
105r
102r
94d
105s
102s
61
TRn
104
100i
102i
105i
96a
102j
105j
TRp
104
100j
102t
105t
96b
102u
105u
TRn(High Vth)
104
100k
102k
105k
97a
102l
105l
TRn(Low Vth)
104
100l
105m
102m
97b
105n
102n
TRp(High Vth)
104
100m
105v
102v
97c
105w
102w
TRp(Low Vth)
104
100n
105x
102x
97d
105y
102y

FIG. 14X

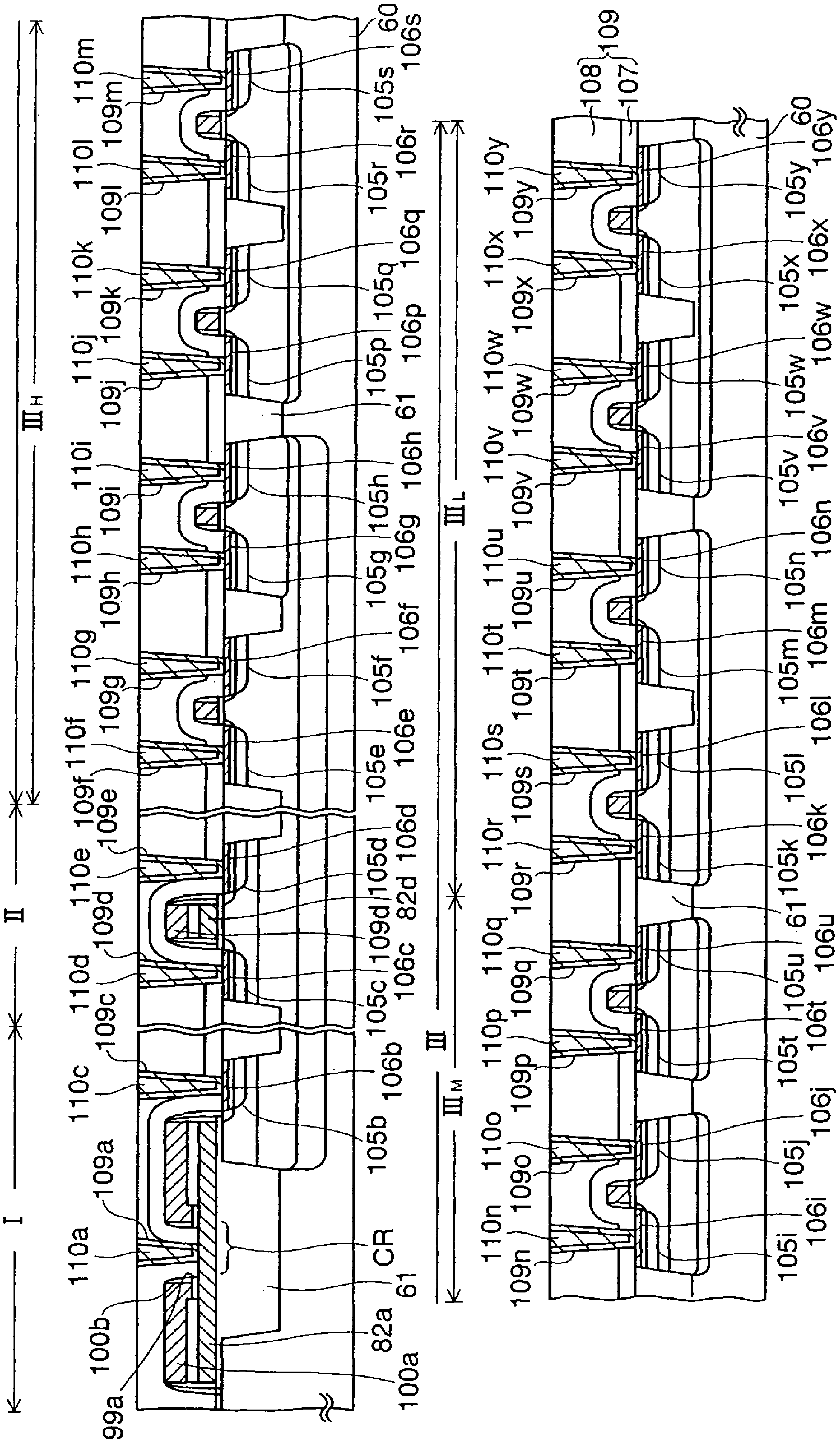
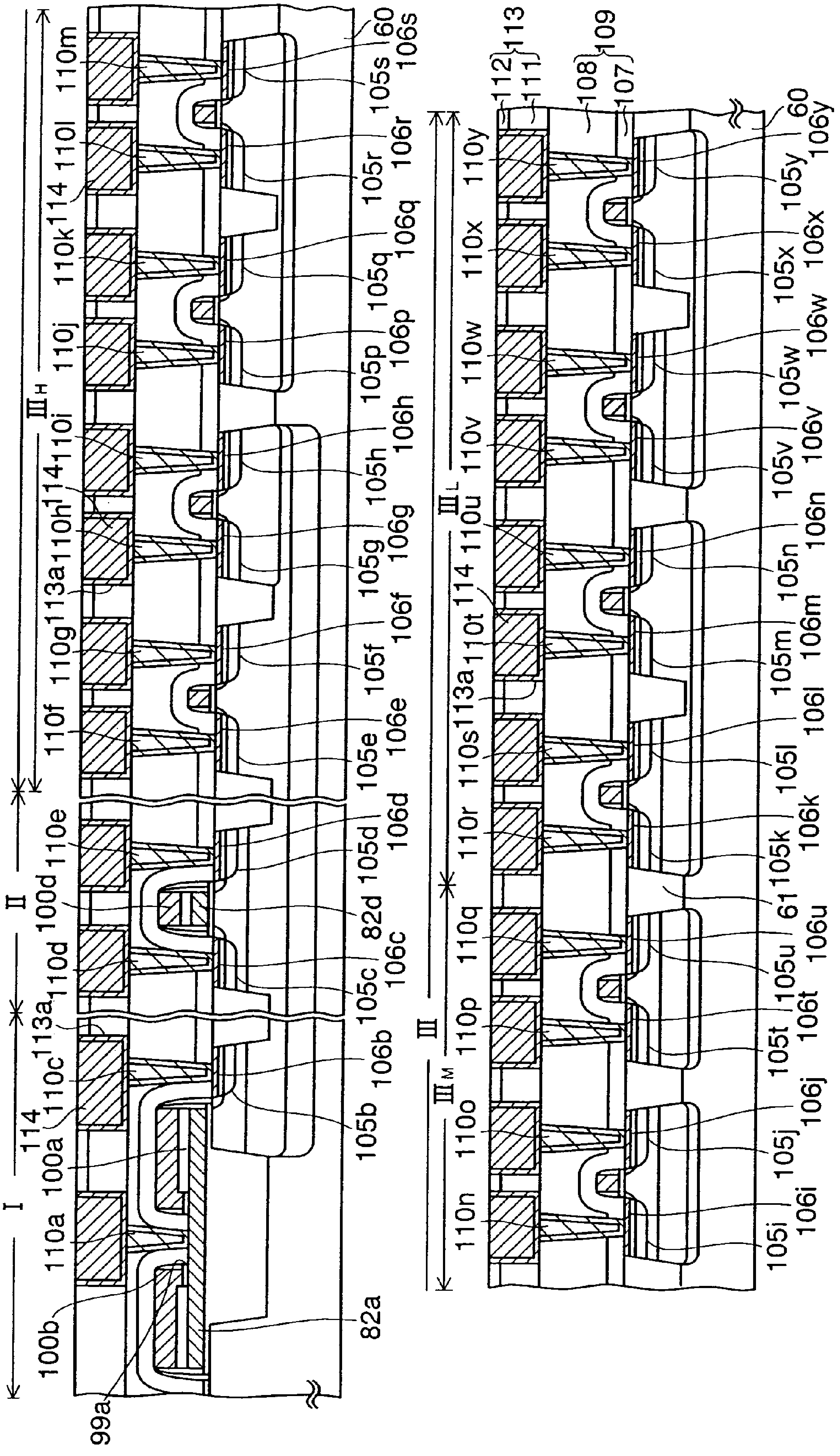

I
II
III
IIIH
IIIM
IIIL
99a
100a
100b
82a
61
CR
109a
110a
110c
105b
106b
109c
110d
109d
105c
106c
109d
82d
110e
105d
106d
109e
109f
110f
105e
106e
109g
110g
105f
106f
109h
110h
105g
106g
109i
110i
105h
106h
61
109j
110j
105p
106p
109k
110k
105q
106q
109l
110l
105r
106r
109m
110m
105s
106s
60
109n
110n
105i
106i
109o
110o
105j
106j
109p
110p
105t
106t
109q
110q
105u
106u
61
109r
110r
105k
106k
109s
110s
105l
106l
109t
110t
105m
106m
109u
110u
105n
106n
109v
110v
105v
106v
109w
110w
105w
106w
109x
110x
105x
106x
109y
110y
105y
106y
60
107
108
109

FIG. 14Y


I
II
III
IIIH
IIIM
IIIL
99a
100b
110a
100a
114
110c
113a
110d
100d
110e
82d
82a
105b
106b
105c
106c
105d
106d
110f
110g
113a
110h
114
110i
110j
110k
114
110l
110m
105e
106e
105f
106f
105g
106g
105h
106h
105p
106p
105q
106q
105r
106r
105s
106s
60
110n
110o
110p
110q
110r
110s
113a
110t
114
110u
110v
110w
110x
110y
112
111
113
108
107
109
60
105i
106i
105j
106j
105t
106t
105u
106u
61
105k
106k
105l
106l
105m
106m
105n
106n
105v
106v
105w
106w
105x
106x
105y
106y

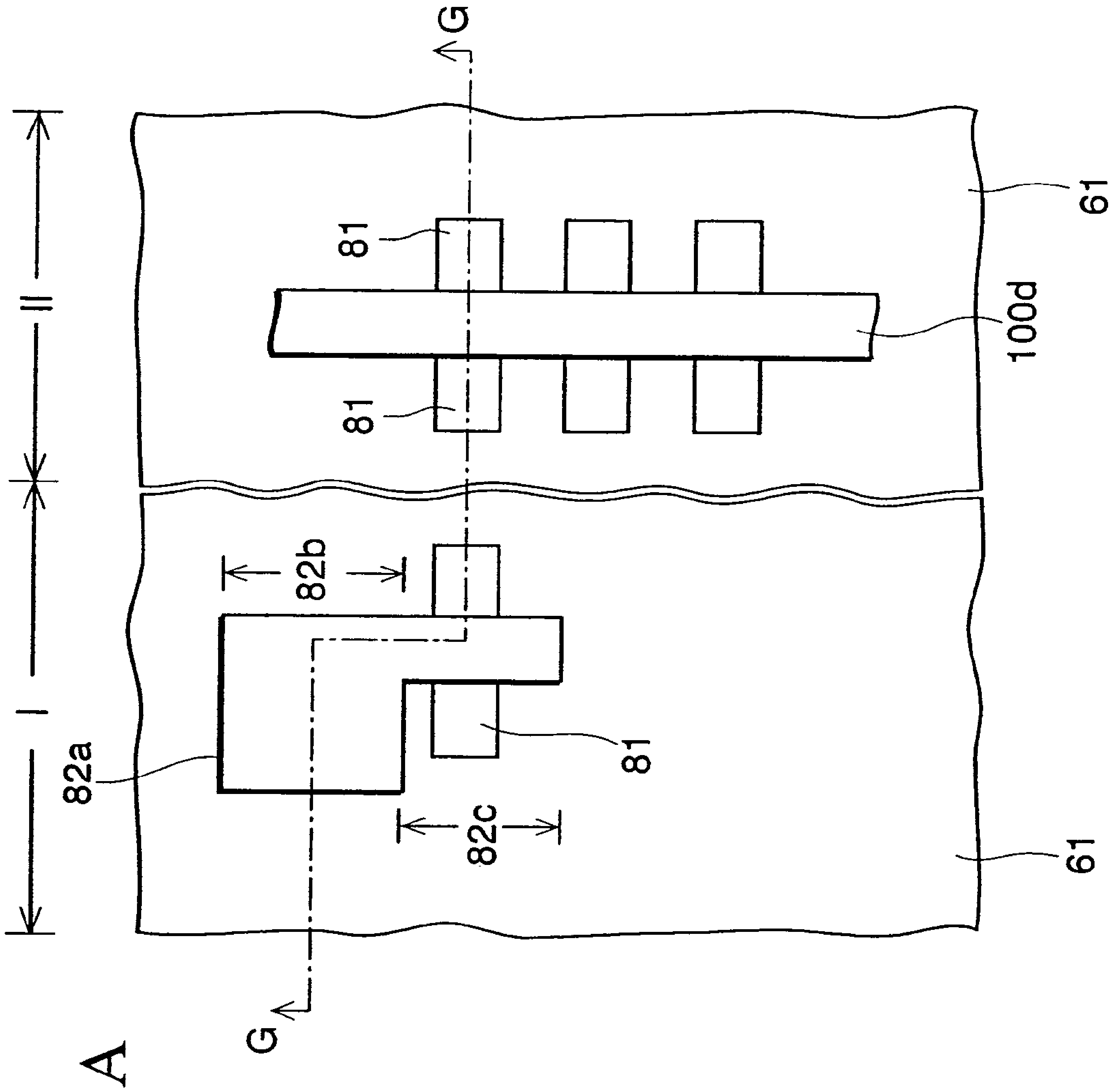


FIG. 15A

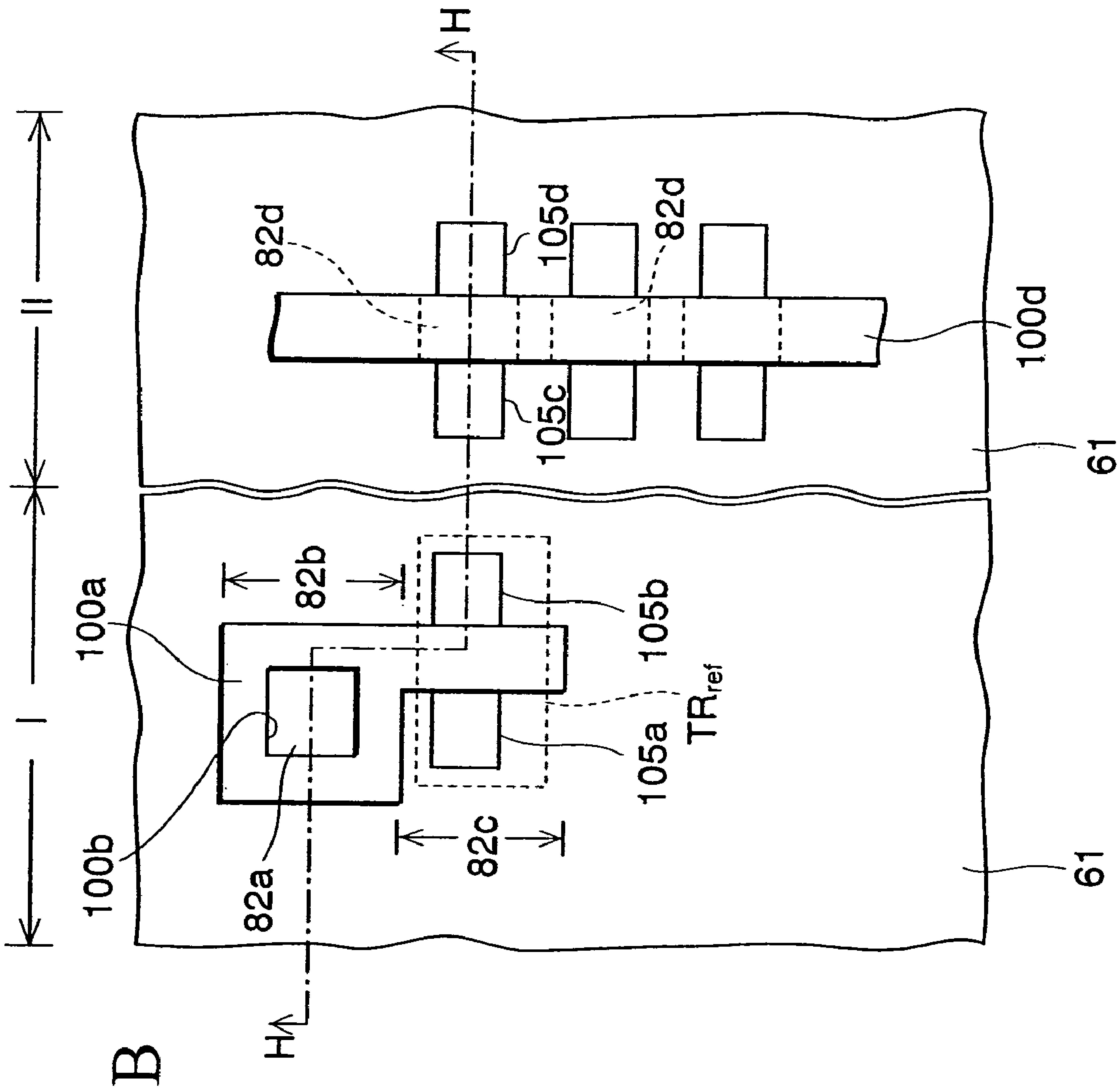

H
H
I
II
100a
100b
82a
82b
82c
105a
105b
TR$_{ref}$
82d
82d
105c
105d
100d
61
61

FIG. 15B

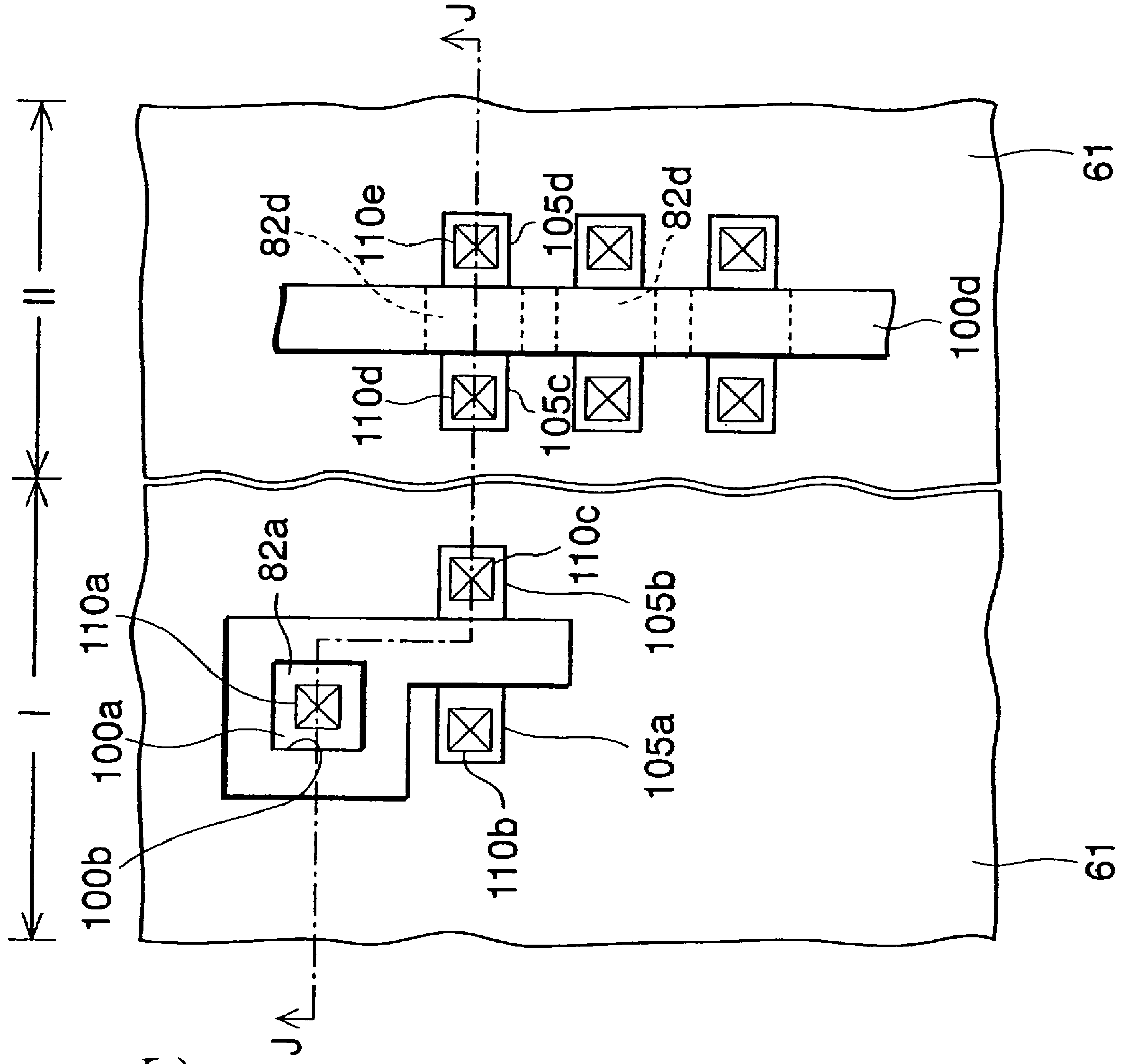

J
J
I
II
61
61
82d
110e
105d
82d
100d
110d
105c
82a
110a
110c
105b
100a
105a
100b
110b

FIG. 15C

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 11/044,458, filed on Jan. 28, 2005 which is based on and claims priority of Japanese Patent Application No. 2004-316974 filed on Oct. 29, 2004, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and a method of manufacturing the device.

2. Description of the Related Art

A flash memory, which can hold memory even after power is turned off, is used in mobile devices such as a cell phone and also used in an FPGA (Field Programmable Gate Array) embedded with a logic circuit. Particularly, when the flash memory is embedded with the logic circuit as in the latter case, it is necessary to utilize each manufacturing process of the memory cell and the logic circuit well to prevent a problem from occurring in a logic-embedded memory to be shipped as a product.

In the logic-embedded memory, breakdown voltage of a tunnel insulating film that constituting the flash memory is monitored before shipping the product in some cases. However, because the tunnel insulating film is formed under a floating gate, in order to monitor the breakdown voltage by applying voltage from above and below the film, it is necessary that a conductive plug be directly contact the floating gate without contacting a control gate and test voltage be applied between the conductive plug and a semiconductor substrate.

For this reason, it is important how the process of the conductive plug contacting the floating gate is incorporated into the manufacturing process of a peripheral logic circuit.

The following Patent Documents 1 to 10 disclose various kinds of logic-embedded memory related to the present invention.

[Patent Document 1] Japanese Patent Laid-open No. 6-97457 publication

[Patent Document 2] Japanese Patent Laid-open No. 2003-158242 publication

[Patent Document 3] Japanese Patent Laid-open No. 11-219595 publication

[Patent Document 4] Japanese Patent Laid-open No. 2004-55763 publication

[Patent Document 5] Japanese Patent Laid-open No. 10-56161 publication

[Patent Document 6] Japanese Patent Laid-open No. 11-31799 publication

[Patent Document 7] Japanese Patent Laid-open No. 10-189954 publication

[Patent Document 8] Japanese Patent Laid-open No. 2003-37169 publication

[Patent Document 9] Japanese Patent Laid-open No. 2003-100887 publication

[Patent Document 10] Japanese Patent Laid-open No. 2003-124356 publication

SUMMARY OF THE INVENTION

According to one aspect of the present invention, there is provided a semiconductor device comprising: a laminated

structure body, which integrally has: a first portion where a first insulating film, a first conductor, a second insulating film, and a second conductor are sequentially formed on a first region of a semiconductor substrate; a second portion where any one of said first conductor and said second conductor, or said first conductor and said second insulating film are laminated on said semiconductor substrate; and a third portion where neither said second insulating film nor said second conductor is formed on said semiconductor substrate; and a third insulating film, which covers said laminated structure body and includes a hole where a contact region of said first conductor of said laminated structure body is exposed at a part of said third portion.

Further, according to another aspect of the present invention, there is provided a semiconductor device comprising: a semiconductor substrate; a first insulating film and a first conductor sequentially formed on a first region of the semiconductor substrate; an insulator formed on a region of the first conductor other than the contact region; an interlayer insulating film that covers said first conductor and the insulator and includes hole on said contact region; and conductive plug that is formed in said hole and electrically connected with the contact region of the first conductor.

Furthermore, according to another aspect of the present invention, there is provided a method of manufacturing a semiconductor device comprising the steps of: forming a first insulating film on a first region of a semiconductor substrate; forming a first conductor on said first insulating film; forming a second insulating film on said first conductor; removing said second insulating film on the contact region of said first conductor; forming a second conductive film on said second insulating film; removing said second conductive film on the contact region of said first conductor to make the second conductive film into a second conductor; forming a third insulating film covering said second conductor; forming a first hole on said third insulating film on the contact region; and forming a first conductive plug, which is electrically connected with said contact region, in said first hole.

In the method of manufacturing a semiconductor substrate, it is preferable to form the first insulating film also on the second region of the semiconductor substrate in the step of forming the first insulating film, to form the second conductive film also on the first insulating film of the second region in the step of forming the second conductive film, to pattern the second conductive film in the second region to make it into a control gate in the step of making the second conductive film into the second conductor, to leave the second insulating film under the control gate as an intermediate insulating film in the step of removing the second insulating film on the contact region, to form a floating gate made up of the same material as the first conductor under the intermediate insulating film in the step of forming the first conductor, and to further comprise the step of forming a first and a second source/drain regions in the semiconductor substrate beside the floating gate to constitute a flash memory cell by the first and second source/drain regions, the first insulating film, the floating gate, the intermediate insulating film, and the control gate.

Furthermore, where the flash memory cell is formed in this manner, it is preferable to form the first insulating film also on the third region of the semiconductor substrate in the step of forming the first insulating film. Then, it is preferable to form the second insulating film also on the first insulating film of the third region, and to comprise the step of implanting an impurity into the semiconductor substrate of the third region while using the first and second insulating films as a through-film.

The first and second insulating films used as the through-film in this manner may be removed in the step of removing the second insulating film on the contact region after the above-described impurity is implanted.

According to this, the step of removing the second insulating film of the third region, which is not needed after it is used as the through-film for impurity implantation, serves also as a step of removing the second insulating film on the contact region. Therefore, the second insulating film above the contact region can be selectively removed without adding an additional mask step.

Moreover, in the step of removing the second insulating film in this manner, only the second insulating film is removed in the first region whereas the two layers of the first insulating film and the second insulating film are removed in the third region, so that etching amount in the third region is larger than that in the first region. Therefore, by setting the etching amount in this step to that in the third region, it is possible to prevent excessive etching of the first and second insulating films in the third region while the second insulating film in the first region is completely removed and to prevent a device isolation or the like from being etched.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A to **1**G are in-process sectional views of a virtual semiconductor device (first example) on which a flash memory and a logic circuit are embedded.

FIGS. **2**A to **2**D are in-process sectional views of a virtual semiconductor device (second example) on which the flash memory and the logic circuit are embedded.

FIGS. **3**A and **3**B are in-process sectional views of a virtual semiconductor device (third example).

FIGS. **4**A and **4**B are in-process sectional views of a semiconductor device according to a first embodiment of the present invention (1).

FIGS. **4**C to **4**P are in-process sectional views of the semiconductor device according to the first embodiment of the present invention.

FIGS. **5**A and **5**B are in-process plan views of the semiconductor device according to the first embodiment of the present invention.

FIG. **6** is a view showing an example of an equivalent circuit of the semiconductor device according to the first embodiment of the present invention.

FIGS. **7**A to **7**G are in-process sectional views of a semiconductor device according to a second embodiment of the present invention.

FIGS. **8**A to **8**C are in-process plan views of the semiconductor device according to the second embodiment of the present invention.

FIGS. **9**A to **9**I are in-process sectional views of a semiconductor device according to a third embodiment of the present invention.

FIG. **10** is an in-process plan view of the semiconductor device according to the third embodiment of the present invention.

FIGS. **11**A to **11**M are in-process sectional views of a semiconductor device according to a fourth embodiment of the present invention.

FIGS. **12**A to **12**C are in-process sectional views of a semiconductor device according to a fifth embodiment of the present invention.

FIG. **13** is a graph obtained after checking how much As^- ion is blocked depending on the thickness of an anti-reflection film in the fifth embodiment of the present invention.

FIGS. **14**A to **14**Y are in-process sectional views of a semiconductor device according to a sixth embodiment of the present invention.

FIGS. **15**A to **15**C are in-process plan views of the semiconductor device according to the sixth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(1) Preliminary Explanation

Prior to explaining the embodiments of the present invention, preliminary explanation will be made for the present invention.

(i) First Example

FIGS. **1**A to **1**G are the in-process sectional views of a virtual semiconductor device on which the flash memory and the logic circuit are embedded (first example).

First of all, description will be made for the process until the sectional structure shown in FIG. **1**A will be obtained.

Firstly, a device isolation trench **1***a* for STI (Shallow Trench Isolation) is formed in a silicon substrate **1**, and then a silicon dioxide film is buried as a device isolation insulating film **2** in the trench **1***a*. Subsequently, after thermal oxidation is performed to the surface of the silicon substrate **1** to form a first thermal oxide film **3**, a first polysilicon film **4** is formed on the entire surface and it is patterned to leave the polysilicon film **4** only in a first peripheral circuit region I and a cell region II. Then, an ONO film **5** is formed on the entire surface.

Subsequently, as shown in FIG. **1**B, the first thermal oxide film **3** and the ONO film **5** on a second peripheral circuit region III are etched and removed. Then, after thermal oxidation is performed to the surface of the silicon substrate **1** in the second peripheral circuit region III to form a second thermal oxide film **7**, a second polysilicon film **6** is formed on the entire surface.

Next, as shown in FIG. **1**C, a resist pattern **9** is formed on the second polysilicon film **6**. Then, the films (**4** to **6**) in the first peripheral circuit region I and the cell region II are etched by using the first resist pattern **9** as a mask. Thus, a floating gate **4***b* and a control gate **6***b*, which are made of polysilicon, are left in the cell region II. Further, first and second conductors (**4***a*, **6***a*), which are made of polysilicon, are left in the first peripheral circuit region I.

Thereafter, the first resist pattern **9** is removed.

Next, as shown in FIG. **1**D, a second resist pattern **10** where the second conductor **6***a* is exposed is formed in the cell region II and the second peripheral circuit region III. Then, by etching the second polysilicon film **6** by using the second resist pattern **10** as a mask, a gate electrode **6***c* is formed in the second peripheral circuit region III and the second conductor **6***a* in the first peripheral circuit region I is removed to expose the ONO film **5**.

Subsequently, description will be made for the process until the sectional structure shown in FIG. **1**E will be obtained.

Firstly, n-type impurity is ion-implanted into the silicon substrate **1** by using the floating gate **4***b* and the gate electrode **6***c* as a mask to form first to fourth source/drain extensions (**11***a* to **11***d*) in the silicon substrate **1** beside each gate (**4***b*, **6***c*). Next, after an insulating film such as a silicon oxide film is formed on the entire surface, the film is etched back and left as insulative sidewalls **14***a* beside each gate (**4***b*, **6***c*) and the first conductor **4***a*. When etching back the film, the first and second thermal oxide films (**3**, **7**) are patterned to be made into a tunnel insulating film **3***a* and a gate insulating film **7***a*, respectively.

Then, the n-type impurity is ion-implanted into the silicon substrate **1** again by using the insulative sidewalls **14***a* as a mask to form first to fourth n-type source/drain regions (**12***a* to **12***d*) in the silicon substrate **1**.

Next, after first to fourth silicide layers (**13***a* to **13***d*) are formed on the first to fourth impurity diffusion regions (**12***a* to **12***d*), a cover insulating film **15** and an interlayer insulating film **16** are sequentially formed on the entire surface. Although not shown in the figure, the silicide layers are also formed on the top surface of the gate electrodes **6***b* and **6***c*.

According to the above-described process, a peripheral transistor TR, which is made up of the first and second n-type impurity diffusion region (**12***a*, **12***b*) and the gate electrode **6***c*, is formed in the second peripheral circuit region III, and a flash memory cell FL, which is made up of the first and second n-type impurity diffusion regions (**12***a*, **12***b*), the tunnel insulating film **3***a*, the floating gate **4***b*, the intermediate insulating film **5***b*, and the control gate **6***b*, is formed in the cell region II.

On the other hand, the first conductor **4***a* in the first peripheral circuit region I serves also as the gate electrode of a reference transistor (not shown). Since the reference transistor has a gate insulating film formed in the same process as the tunnel insulating film **3***a* of the flash memory cell FL, it is possible to check the breakdown voltage of the tunnel insulating film **3***a* of the flash memory cell FL by checking the breakdown voltage of the reference transistor.

Next, as shown in FIG. **1**F, the cover insulating film **15** and the interlayer insulating film **16** are patterned to form first to fourth holes (**16***a* to **16***d*) having a depth reaching the first to fourth silicide layers (**13***a* to **13***d*) and to form a fifth hole **16***e* above the first conductor **4***a*.

The holes (**16***a* to **16***d*) are formed by etching the interlayer insulating film **16** while the cover insulating film **15** is firstly used as an etching stopper film, and then by etching the cover insulating film **15** after changing etching gas.

Among these holes, the contact structure of the first to fourth holes (**16***a* to **16***d*) is called as a borderless contact. In the borderless contact, even if the holes (**16***a* to **16***d*) suffer from slight positional shift and a part of them overlaps the device isolation insulating film **2**, the etching amount of the device isolation insulating film **2** during the formation of the holes is suppressed by the difference of etching rate between the device isolation insulating film **2** and the cover insulating film **15**.

On the other hand, since the fifth hole **16***e* is formed to contact the first conductor **4***a* and to apply gate voltage to the reference transistor, the first conductor **4***a* must be exposed under the bottom of the fifth hole **16***e*. However, it is necessary to etch the ONO film **5** under the cover insulating film **15** in order to form the fifth hole **16***e* whereas the formation of the first to fourth holes (**16***a* to **16***d*) is completed simultaneously with the end of etching to the cover insulating film **15**.

Therefore, when the etching time of the holes is set to the etching time of the first to fourth holes (**16***a* to **16***d*), the etching amount of the fifth hole **16***e* becomes insufficient and the hole **16***e* does not open completely, and thus the first conductor **4***a* is not exposed.

Therefore, to open the fifth hole **16***e*, etching must be additionally performed by a quantity for the etching time of the ONO film **5** in which the fifth hole **16***e* is formed completely, in addition to the etching time necessary for forming the first to fourth holes (**16***a* to **16***d*).

Despite such long etching time, problem does not arise if a positional shift does not occur between the first to fourth holes (**16***a* to **16***d*) and the first to fourth silicide layers (**13***a* to **13***d*).

However, if there is a positional shift between them, the device isolation insulating film **2** under the third hole **16***c* is etched, for example, and the silicon substrate **1** is exposed on the third hole **16***c* as shown in the dotted circle of FIG. **1**G. Consequently, short circuit occurs between a third conductive plug **19***c* buried in the third hole **16***c* and the silicon substrate **1**, and it becomes impossible for the conductive plug **19***c* to control the electric potential of the third n-type source/drain region **12***c*. Such a problem could occur, not only in the third conductive plug **19***c*, but also in first, second and fourth conductive plugs (**19***a*, **19***b*, **19***d*) formed in the first, second, and fourth holes (**16***a*, **16***b*, **16***d*).

(ii) Second Example

To solve the problem in the first example, the following method is also considered.

FIGS. **2**A to **2**D are the in-process sectional views of the virtual semiconductor device (second example).

Firstly, after completing the process of FIG. **1**D shown in the first example, the n-type impurity is ion-implanted into the silicon substrate **1** by using the floating gate **4***b* and the gate electrode **6***c* as a mask to form the first to fourth source/drain extensions (**11***a* to **11***d*) in the silicon substrate **1** beside each gate (**4***b*, **6***c*) as shown in FIG. **2**A.

Next, as shown in FIG. **2**B, the insulating film **14** such as silicon oxide is formed on the entire surface.

Subsequently, as shown in FIG. **2**C, the insulating film **14** is etched back and left as the insulative sidewalls **14***a* beside each gate (**4***b*, **6***c*) and the first conductor **4***a*. Etching is further performed in this example to remove the ONO film **5** on the first conductor **1**.

Then, the n-type impurity is ion-implanted into the silicon substrate **1** again using the insulative sidewalls **14***a* as a mask to form the first to fourth n-type source/drain regions (**12***a* to **12***d*) in the silicon substrate **1**.

Next, the first to fourth silicide layers (**13***a* to **13***d*) are formed on the first to fourth n-type source/drain regions (**12***a* to **12***d*).

Thereafter, the first to fifth holes (**16***a* to **16***e*) are formed in the interlayer insulating film **16** by performing the process of FIGS. **1**E to **1**G explained in the first example, and the sectional structure shown in FIG. **2**D is obtained.

In the above-described second example, the ONO film **5** is removed simultaneously when the insulative sidewalls **14***a* are formed by etchback as shown in FIG. **2**C, and the surface of the first conductor **4***a* is exposed. Accordingly, the surface of the first conductor **4***a* is exposed under the fifth hole **16***e* without conducting excessive etching to the first to fourth holes (**16***a* to **16***d*).

However, since etching is performed longer than etching time originally required in the etchback process shown in FIG. **2**C, the device isolation insulating film **2** is etched and its top surface becomes lower than that of the silicon substrate **1**. As a result, side surfaces of the third n-type source/drain region **12***c* and the silicon substrate **1** appear on the sidewalls of the device isolation trench **1***a* as shown in the dotted line X of FIG. **2**D. Therefore, when positional shift occurs in the third hole **16***c*, short circuit is caused between the third conductive plug **19***c* formed in the third hole **16***c* and the silicon substrate **1** similar to the first example.

(iii) Third Example

The following method is considered in addition to the above-described first and second examples.

FIGS. **3**A and **3**B are the in-process sectional views of the virtual semiconductor device (third example).

Firstly, after the process of FIG. **1**C shown in the first example, a second resist pattern **10** is formed on the control gate **6***b* and the second polysilicon film **6**, where the second conductor **6***a* is exposed, as shown in FIG. **3**A.

Next, as shown in FIG. **3**B, the second polysilicon film **6** is etched by using the second resist pattern **10** as a mask to form the gate electrode **6***c*, and the second conductor **6***a* and the ONO film **5** are etched and removed to expose the first conductor **4***a*. Then, the second resist pattern **10** is removed.

Thereafter, the process of FIGS. **1**E to **1**G explained in the first example will be performed.

In the third example, the ONO film **5** is etched and removed during the patterning of the gate electrode **6***c*. Since the top surface of the device isolation insulating film **2** becomes lower than the top surface of the silicon substrate **1** due to the etching, a problem similar to the second example occurs. Further, if the gate insulating film in the second peripheral circuit region III is thin, such a problem occurs that the surface of the silicon substrate **1** in a region, where source/drain is to be formed, is exposed to etching atmosphere of RIE or the like for a long period of time and is contaminated, and the silicon substrate **1** is etched, when the ONO film is etched.

Although the above-described first to third examples have different methods of removing the ONO film **5** on the first conductor **4***a*, short circuit occurs in all examples between the conductive plug and the silicon substrate **1** in the first to fourth holes (**16***a* to **16***d*) when removing the ONO film. To prevent this, addition of photolithographic process exclusively for removing the ONO film **5** could be considered, but this increases the number of processes to deteriorate the productivity of semiconductor devices.

The inventors thought out the following embodiments of the present invention in order to solve the problems in the first to third examples.

(2) First Embodiment

FIGS. **4**A to **4**P are in-process sectional views of a semiconductor device according to a first embodiment of the present invention, and FIGS. **5**A and **5**B are the plan views thereof.

In this embodiment, a logic-embedded memory such as an FPGA is fabricated.

First of all, description will be made for the process until the sectional structure shown in FIG. **4**A will be obtained.

Firstly, after a device isolation trench **20***a* for STI is formed on a p-type silicon substrate (semiconductor substrate) **20**, on which the first peripheral circuit region (first region) I, the cell region (second region) II, and the second peripheral circuit region (third region) III are defined, silicon oxide is buried in the device isolation trench **20***a* as a device isolation insulating film **21**.

Next, thermal oxidation is performed to the surface of the silicon substrate **20** to form a sacrifice oxide film (not shown), and P^+ ion as n-type impurity is ion-implanted into the silicon substrate **20** while the sacrifice oxide film is used as a through-film to form a first n-well **17***a* in a deep portion of the silicon substrate **20**. Accelerating energy of 2 MeV and dose of 2×10^{13} cm^{-3}, for example, are employed as the conditions of ion implantation.

Subsequently, B^+ ion of the p-type impurity is implanted into the silicon substrate **20** to form a first p-well **17***b* in the silicon substrate **20** at a shallower portion than the first n-well **17***a*. This ion-implantation is performed by first and second steps, and the condition of the first step includes accelerating energy of 400 KeV and dose of 1.5×10^{13} cm^{-3}, whereas the second step includes accelerating energy of 100 KeV and the dose of 2×10^{12} cm^{-3}.

Furthermore, B^+ ion is ion-implanted into the silicon substrate **20** under the conditions of the accelerating energy of 40 KeV and the dose of 6×10^{13} cm^{-3}, and an impurity diffusion region **17***c* for cell for controlling threshold voltage is formed.

Thereafter, ion implantation is also performed in the second peripheral circuit region III to form a second n-well **22** and a second p-well **23** as shown in the drawing. Of these wells, ion implantation to the second n-well **22** is conducted in the two steps, where the accelerating energy of 600 KeV and the dose of 1.5×10^{13} cm^{-3} of P^+ ion is employed as the first conditions, and the accelerating energy of 240 KeV and the dose of 6.0×10^{12} cm^{-3} is employed as the second conditions. Further, the second p-well **23** is formed by two step ion implantation, where the accelerating energy of 400 KeV and the dose of 1.5×10^{3} cm^{-3} of B^+ ion is employed as the first conditions, and the accelerating energy of 100 KeV and the dose of 8×10^{12} cm^{-3} are employed as the second conditions.

Note that the implantation of the above-described n-type impurity and p-type impurity are respectively performed using resist patterns (not shown), and the resist patterns are removed after the ion implantations are completed.

Then, after the sacrifice oxide film used as the through-film of ion implantation is removed by hydrofluoric acid solution to expose a clean surface of the silicon substrate **20**, thermal oxidation is performed to the clean surface in the mixed atmosphere of Ar and O_2 under the condition of temperature at 900° C. to 1050° C. Thus, a thermal oxide film having the thickness of about 10 nm is formed as a first insulating film **24** on each region (I to III) of the silicon substrate **20**.

Subsequently, description will be made for the process until the sectional structure shown in FIG. **4**B will be obtained.

Firstly, a polysilicon film as a first conductive film **25** is formed on the first insulating film **24** with the thickness of about 90 nm by a low pressure CVD (Chemical Vapor Deposition) using SiH_4 (silane) and PH_3 (phosphine) as reactive gas. In-situ phosphorous is doped into the polysilicon film due to PH_3 in the reactive gas.

Then, the first conductive film **25** is patterned by photolithography to remove it from the second peripheral circuit region III. The first conductive film **25** in the cell region II becomes a stripe shape in word line directions.

Next, a silicon oxide film and a silicon nitride film are formed in this order on the first conductive film **25** and the first insulating film **24** on the second peripheral circuit region III with the thickness of 5 nm and 10 nm, respectively, by using the low pressure CVD method. Further, the surface of the silicon nitride film is oxidized in O_2 atmosphere under the condition of substrate temperature at about 950° C. and heating time for about 90 minutes to form a silicon oxide film having the thickness of about 30 nm on the surface of the silicon nitride film. Consequently, the ONO film, where the silicon oxide film, the silicon nitride film, and the silicon oxide film are laminated in this order, is formed as a second insulating film **26** on the entire surface.

The ONO film constituting the second insulating film **26** has smaller leakage current comparing to the silicon oxide film even if it is formed at low temperature. Therefore, by using the second insulating film **26** as an intermediate insulating film between the floating gate and the control gate of the flash memory cell, electric charge stored in the floating gate is difficult to flow toward the control gate, by which information written in the flash memory cell can be held for a long period of time.

After forming the second insulating film **26**, by employing conditions of the accelerating energy of 150 KeV and the dose of 3×10^{12} cm^{-3}, As^{-} ion of the n-type impurity is ion-implanted into the silicon substrate **20** while the first and second insulating films (**24**, **26**) are used as the through-film, thus an n-type impurity diffusion region **22***a* is formed. The n-type impurity diffusion region **22***a* serves to adjust the threshold voltage of a p-type MOS transistor that will be formed later.

Furthermore, B^{+} ion of the p-type impurity is ion-implanted into the silicon substrate **20** while the first and second insulating films (**24**, **26**) are used as the through-film under the conditions of the accelerating energy of 30 KeV and the dose of 5×10^{12} cm^{-3}. Thus, a p-type impurity diffusion region **23***a* for adjusting the threshold voltage of the n-type MOS transistor is formed in the second peripheral circuit region III.

Note that n-type impurity and p-type impurity are independently implanted in the silicon substrate **20** for the impurity diffusion regions (**22***a*, **23***a*) by using resist patterns (not shown).

Subsequently, as shown in FIG. **4**C, a first resist pattern **27** is formed on the second insulating film **26**. The first resist pattern **27** has a first window **27***a* on a contact region CR of the first conductive film **25**, which will be connected with the conductive plug later, and a second window **27***b* in the second peripheral circuit region III. Then, the second insulating film **26** in a region that is not covered by the first resist pattern **27** is etched by plasma etching using the gas mixture of CHF_3 and O_2 while the first resist pattern **27** is used as a mask, and thus the silicon oxide film and the silicon nitride film of the top layer, which constitute the second insulating film **26**, are etched. Next, by using HF solution, wet etching is performed for the silicon oxide film of the bottom layer of the second insulating film **26** to remove it while the first resist pattern is used as a mask.

Consequently, the first conductive film **25** in the contact region CR and the silicon substrate **20** in the second peripheral circuit region III are exposed, and the second insulating film is left only in a region other than the contact region CR.

Then, after removing the first resist pattern **27** by oxygen ashing, the surface of the silicon substrate **20** is cleaned by wet treatment.

Next, description will be made for the process until the sectional structure shown in FIG. **4**D will be obtained.

Firstly, oxidizing condition where substrate temperature is set to about 850° C. in oxygen atmosphere is employed, and thus silicon in an area that is not covered by the second insulating film **26** is thermally oxidized. Consequently, a thermal oxide film having the thickness of about 2.2 nm is formed as a third insulating film **28** on the surface of an area on the first conductive film **25** made of polysilicon, where the second insulating film **26** has been removed, and on the surface of the silicon substrate **20** of the second peripheral circuit region III. The third insulating film **28** is formed adjacent to the second insulating film **26**, and the second and third insulating films (**26**, **28**) constitute an insulator **29**. Although not shown in FIG. **4**D, it should be noted that the thickness of the insulator **29** on the contact region CR is significantly thinner than that of other regions.

Thereafter, a non-doped polysilicon film having the thickness of about 180 nm is formed as a second conductive film **30** on each insulating film (**26**, **28**) by a low-pressure CVD method using SiH_4 as reactive gas.

Next, description will be made for the process until the sectional structure shown in FIG. **4**E will be obtained.

Firstly, photoresist is coated on the second conductive film **30**, and it is exposed and developed to form a second resist pattern **18**. Next, the first and second conductive films (**25**, **30**) and the insulator **29** are patterned by using the second resist pattern **18** as an etching mask. The patterning is conducted in a plasma etching chamber, gas mixture of Cl_2 and O_2 is used as etching gas for the first and second conductive films (**25**, **30**) made of polysilicon, and gas mixture of CHF_3 and O_2 is used as etching gas for the second insulating film **26** made of the ONO film.

As a result of the patterning, the first and second conductive films (**25**, **30**) in the first peripheral circuit region I are made into first and second conductor (**25***a*, **30***a*) respectively in the region including the contact region CR while the second conductive film **30** is left in the second peripheral circuit region III. In the cell region, the first and second conductive films (**25**, **30**) and the insulator **29** are made into a floating gate **25***d*, a control gate **30***d*, and an intermediate insulating film **29***d*, respectively.

After this, the second resist pattern **30** is removed.

FIG. **5**A is the plan view after completing the process, and the previous FIG. **4**E corresponds to the sectional view taken along A-A line of FIG. **5**A. As shown in this drawing, the first conductor **25***a* is made up of a pad portion **25***b* on the device isolation insulating film **21** and a gate portion **25***c* on the first insulating film **24**.

Next, as shown in FIG. **4**F, a third resist pattern **31**, which covers the pad portion **25***b* of the first conductor **25***a* and the second conductive film **30** and includes a third window **31***a* where the gate portion **25***c* and the floating gate **25***d* are exposed, is formed on each region (I to III). Then, As of the n-type impurity is ion-implanted into the silicon substrate **20** through the third window **31***a* under the conditions of the accelerating energy of 50 KeV and the dose of 6×10^{14} cm^{-3}, first to fourth n-type source/drain extensions (**32***a* to **32***d*) are formed in the silicon substrate **20** beside the floating gate **25***d* and the gate portion **25***c*.

The third resist pattern **31** is removed after this.

Next, as shown in FIG. **4**G, after the side surfaces of the floating gate **25***d* and the control gate **30***d* are oxidized to form a thermal oxide film (not shown), a silicon nitride film is formed on the entire surface and it is etched back, and it is left as first insulative sidewalls **33** on the side surfaces of the second conductor **30***a* and the floating gate **25***d*.

Next, as shown in FIG. **4**H, a fourth resist pattern **34** is formed on each region (I to III). The fourth resist pattern **34** has a fourth window **34***a* on the contact region CR of the pad portion **25***b* and has a gate electrode shape on the second peripheral circuit region III. Then, the mixed gas of Cl_2 and O_2 is employed as etching gas and plasma etching is performed to the second conductor **30***a* and the second conductive film **30** while the fourth resist pattern **34** is used as a mask. Thus, the second conductor **30***a* on the contact region CR is removed to form a first opening **30***b* and first and second gate electrodes (**30***f*, **30***g*) are formed on the second peripheral circuit region III. Further, in this etching, the second conductive film **30** extended on the device isolation insulating film **21** is patterned into wiring **30***e*.

The fourth resist pattern **34** is removed after this.

Next, as shown in FIG. **4**I, a fifth resist pattern **35** including a fifth window **35***a* of a size, where the third insulating film **28** beside the first gate electrode **30***f* is exposed, is formed on each region (I to III). Then, B^{+} is ion-implanted into the silicon substrate **20** under the conditions of the tilt angle of 0°, the accelerating energy of 0.5 KeV and the dose of 3.5×10^{14}

cm^{-3} while the fifth resist pattern **35** is used as a mask. Subsequently, As^+ is ion-implanted into the silicon substrate **20** from four directions through the fifth window **35***a* under the conditions of the tilt angle of 28°, the accelerating energy of 80 KeV and the dose of 7.0×10^{12} cm^{-3}, and thus fifth and sixth p-type source/drain extensions (**32***e*, **32***f*) including n-type pocket regions are formed in the silicon substrate **20** beside the first gate electrode **30***f*. After this, the fifth resist pattern **35** is removed.

Then, as shown in FIG. **4**J, sixth resist pattern **36** including a sixth window **36***a* of a size, where the third insulating film **28** beside the second gate electrode **30***g* is exposed, is formed on each region (I to III).

Then, As^+ is ion-implanted into the silicon substrate **20** under the conditions of the tilt angle of 0°, the accelerating energy of 3.0 KeV and the dose of 1.0×10^{15} cm^{-3} while the sixth resist pattern **36** is used as a mask. Subsequently, BF_2 is ion-implanted into the silicon substrate **20** through the sixth window **36***a* under the conditions of the tilt angle of 28°, the accelerating energy of 35 KeV and the dose of 1.0×10^{13} cm^{-3}, and thus first and second n-type source/drain extensions (**32***g*, **32***h*) including p-type pocket regions are formed in the silicon substrate **20** beside the second gate electrode **30***g*. After this, the sixth resist pattern **36** is removed.

Next, description will be made for the process until the sectional structure shown in FIG. **4**K will be obtained.

Firstly, after a silicon oxide film is formed on the entire surface by the CVD method, the silicon oxide film is etched back to form second insulative sidewalls **37** on the side surfaces of the second conductor **30***a*, the control gate **30***d*, the wiring **30***e*, and the first and second gate electrodes (**30***f*, **30***g*). Then, by continuing the etchback, the third insulating film **28** that constitutes the insulator **29** on the pad portion **25***b* is etched by using the second insulative sidewall **37** as a mask, and a second opening having a smaller diameter than the first opening **30***b* is formed.

Further, the first insulating film **24** is patterned by the etchback while the second insulative sidewalls **37** function as a mask, and the first insulating film **24** is left as a gate insulating film **24***a* and a tunnel insulating film **24***b* under the gate portion **25***c* and the floating gate **25***d*, respectively.

Furthermore, the third insulating film **28** is patterned in the second peripheral circuit region III, and it is left as gate insulating films (**28***a*, **28***b*) under the first and second gates (**30***f*, **30***g*).

Subsequently, as shown in FIG. **4**L, a seventh resist pattern **39** where an NMOS forming region is exposed is formed on the silicon substrate **20**, and P^+ is ion-implanted into the silicon substrate **20** under the conditions of the accelerating energy of 10 KeV and the dose of 6×10^{15} cm^{-3} while the resist pattern **39** is used as a mask. Consequently, first and sixth n-type source/drains (**38***a* to **38***f*) are formed in the silicon substrate **20** beside the gate portion **25***c*, the floating gate **25***d*, and the first gate electrode **30***f*. In addition, the n-type impurity is also introduced into the second conductor **30***a*, the control gate **30***d*, and the first gate electrode **30***f*, in this ion implantation, and they are made into n-type.

As a result, a reference transistor TR_{ref}, which is made up of the gate portion **25***c*, gate insulating film **24***a*, and the first and second n-type source/drain regions (**28***a*, **28***b*), is formed in the first peripheral circuit region I. On the other hand, a flash memory cell FL, which is made up of the control gate **30***d*, the intermediate insulating film **29***d*, the floating gate **25***d*, the tunnel insulating film **24***b*, and the third and fourth n-type source/drain regions (**38***c*, **38***d*), is formed in the cell region II. Then, an n-type MOS transistor TR_n, which is made up of the first gate electrode **30***f*, the gate insulating film **28***a*, and the fifth and sixth n-type source/drain regions (**38***e*, **38***f*), are formed in the second peripheral circuit region III.

After this, the seventh resist pattern **39** is removed.

Subsequently, as shown in FIG. **4**M, the first peripheral circuit region I, the cell region II, and the n-type MOS transistor TR_n is covered by an eighth resist pattern **40**. Then, the ion implantation conditions of the accelerating energy of 5 KeV and the dose of 4×10^{15} cm^{-3} are employed, and first and second p-type source/drain regions (**38***g*, **38***h*) are formed by introducing p-type impurity in the silicon substrate **20** beside the second gate electrode **30***g*. Consequently, a p-type MOS transistor TR_p, which is made up of the second gate electrode **30***g*, the gate insulating film **28***b*, and the first and second p-type source/drains (**38***g*, **38***h*), are formed in the second peripheral circuit region III next to the n-type MOS transistor TR_n.

The p-type MOS transistor TR_p constitutes a logic circuit such as a sense amplifier together with the n-type MOS transistor TR_n.

The eighth resist pattern **40** is removed after the ion implantation is completed.

Next, description will be made for the process until the sectional structure shown in FIG. **4**N will be obtained.

Firstly, after a cobalt film is formed on the entire surface at the thickness of about 8 nm by a sputtering method, the cobalt film is annealed to allow it to react with silicon. Then, the cobalt film on the device isolation insulating film **21** or the like, which has not been reacted, is removed by wet etching to form first to eighth cobalt-silicide layers (**41***a* to **41***h*) on the surface layer of the silicon substrate **20**. Although not shown in the figure, cobalt-silicide layers are also formed on the top surface of the gate electrodes

Subsequently, a silicon nitride film is formed in the thickness of about 50 nm by the CVD method, and is used as an etching stopper film **42**. Next, a silicon oxide film as a fourth insulating film **43** is formed on the etching stopper film **42** by the CVD method, and the etching stopper film **42** and the fourth insulating film **43** are made to be a first interlayer insulating film **44**. Note that the thickness of the fourth insulating film **43** is about 1000 nm on the flat surface of the silicon substrate **20**.

Subsequently, the top surface of the first interlayer insulating film **44** is polished to make it flat by a CMP (Chemical Mechanical Polishing) method. Then, the first interlayer insulating film **44** is patterned by photolithography to form first to ninth holes (**44***a* to **44***i*). Of these holes, the first hole **44***a* is positioned on the contact region CR of the pad portion **25***b*, and is formed inside the first and second openings (**30***b*, **29***a*). Further, the remaining second to ninth holes (**44***b* to **44***i*) are respectively formed on the cobalt-silicide layers (**41***a* to **41***h*). Since the second insulating film **26** constituted by the ONO film is not formed under the above-described first hole **44***a*, it is possible to expose the surface of the pad portion **25***b* by forming the first hole **44***a* under the same forming conditions of the fourth to ninth holes (**44***a* to **44***i*) in the second peripheral circuit region III.

Next, description will be made for the process until the sectional structure shown in FIG. **4**O will be obtained.

Firstly, a Ti (titanium) film and a TiN (titanium nitride) film are formed in this order in the first to ninth holes (**44***a* to **44***i*) and on the first interlayer insulating film **44** by the sputtering method, and they are used as a glue-film, and a W (tungsten) film is formed on the glue-film by a CVD method using tungsten hexafluoride as reactive gas to completely fill the inside of the first to ninth holes (**44***a* to **44***i*). Then, excessive W film and glue-film formed on the top surface of the first interlayer insulating film **44** are removed by the CMP method, and they are left as first to ninth conductive plugs (**45**a to **45**i) inside the first to ninth holes (**44**a to **44**i).

Of these conductive plugs, the second to ninth conductive plugs (**45**b to **45**i) are electrically connected with the source/drain regions (**38**a to **38**h) via the cobalt-silicide layers (**41**a to **41**h).

On the other hand, the first conductive plug **45**a is electrically connected with the contact region CR of the first conductor **25**b.

Further, as shown in the drawing, the second insulating film **26** constituting the insulator **29** is structured to be farther from the contact region CR than the third insulating film **28**.

Next, description will be made for the process until the sectional structure shown in FIG. **4**P will be obtained.

Firstly, after a low dielectric constant insulating film **46** of a coating type is formed on the entire surface, a silicon oxide film to prevent the low dielectric constant insulating film **46** from absorbing moisture is formed on it as a cover insulating film **47**, and the low dielectric constant insulating film **46** and the cover insulating film **47** are made to be a second interlayer insulating film **48**.

Subsequently, the second interlayer insulating film **48** is patterned by photolithography to form first to ninth wiring grooves (**48**a to **48**i) on each plug (**45**a **59** **45**i). Note that, in the photolithography, mixed gas of CHF_3 and O_2 is used as the etching gas of plasma etching to the cover insulating film **47** made of silicon oxide, and O_2 is used as the etching gas of plasma etching to the low dielectric constant insulating film **46**.

Then, a Cu (copper) film is formed as a seed layer on the entire surface by the sputtering method after depositing TaN layer, an electrolytic copper plated film is formed on the seed layer by supplying electric power to the seed layer, and each wiring groove (**48**a to **48**i) is completely filled by the copper plated film. After that, excessive seed layer and copper plated film formed on the second interlayer insulating film **48** are removed by the CMP method, and they are left in each wiring groove (**48**a to **48**i) as first to ninth copper wirings (**49**a to **49**i).

Although the function of the first to ninth copper wirings (**49**a to **49**i) is not particularly limited, the fourth and fifth copper wirings (**49**d, **49**e) above the flash memory cell FL function as a bit line (BL) and a source line (SL) of an NOR type flash memory, for example. Furthermore, the control gate **30**d functions as a word line (WL).

FIG. **5**B is the plan view after the process has been finished, and the previous FIG. **4**P corresponds to the sectional view taken along B-B line of FIG. **5**B. It is to be noted that the first to ninth copper wirings (**49**a to **49**i) and the second interlayer insulating film **28** in FIG. **5**B are omitted to make the planar layout of each layer be easily read.

As shown in the drawing, the second conductor **30**a is formed so as to extend from above the gate portion **25**c of the first conductor **25**a to the outside of the contact region CR of the pad portion **25**b. Further, the second conductor **30**a is surrounded by the insulating film and is in an electrically floating state.

The basic structure of the semiconductor device according to the present invention is thus completed.

The semiconductor device has a first portion L where the first insulating film **24**, the first conductor **25**a, the second insulating film **26**, and the second conductor **30**a are sequentially formed on the silicon substrate **20**, as shown in FIG. **4**O. Additionally, the semiconductor device has a second portion M where either the first conductor **25**a and the second conductor **30**a or the first conductor **25**a and the second insulating film **26** are laminated, and a third portion N where neither the second insulating film **26** nor the second conductor **30**a is laminated. Then, a laminated structure body **120** that integrally has the first to third portions (L to N) has been formed in the semiconductor device.

Further, the reference transistor TR_{ref} is formed in this semiconductor device as shown in FIG. **4**P, but the function of the reference transistor TR_{ref} is not particularly limited. For example, the reference transistor TR_{ref} is used to check the breakdown voltage of the tunnel insulating film **24**b of the flash memory cell FL before it is shipped from a factory. To check this, the electric potential of the gate portion **25**c is increased via the first conductive plug **45**a in the state where predetermined voltage is applied to the first and second n-type source/drain regions (**38**a, **38**b) via the second and third conductive plugs (**45**b, **45**c). Then, since electric current is made to flow in the first conductive plug **45**a when breakdown is caused in the gate insulating film **24**a to allow electrons to enter the gate portion **25**c, it is possible to check the breakdown voltage of the tunnel insulating film **24**b, which has been formed in the same process as the gate insulating film **24**a, of the flash memory cell FL by detecting the current.

Alternatively, as shown in FIG. **6**, the above-described reference transistor TR_{ref} may be used in order to generate reference current I_{ref} that is input to a sense amplifier S/A. In this case, voltage of about 2V is applied as gate voltage V_g to the gate portion **25**c of the reference transistor TR_{ref} and voltage of about 0.5V is applied between source-drain. Thus, the reference current I_{ref} is allowed to flow between the source-drain of the reference transistor TR_{ref}, and is input to the sense amplifier S/A. Then, the sense amplifier S/A compares the sizes of the reference current I_{ref} and the readout current I_{BL} of the flash memory cell FL, and it is determined which information of 1 and 0 is written in the flash memory cell FL.

Since the reference transistor TR_{ref} has the same temperature characteristic as the flash memory cell FL, the size of the reference current I_{ref} becomes small when ambient temperature is increased and the size of the readout current I_{BL} becomes small, for example, so that a difference between the currents I_{ref} and I_{BL} is not affected by temperature. Therefore, it is difficult to cause error in the sense amplifier S/A in comparing the currents I_{ref} and I_B even if the ambient temperature is changed, and readout operation of the flash memory cell FL can be performed accurately.

According to this embodiment described above, the n-type impurity diffusion region **22**a and the p-type impurity diffusion region **23**a, which are used for adjusting threshold value, are formed in the second peripheral circuit region III by ion implantation while the first insulating film **24** and the second insulating film **26** made up of the ONO film are used as a through-film, as shown in FIG. **4**B. Then, as shown in FIG. **4**C, the first and second insulating films (**24**, **26**), which completed their function as the through-film after the ion implantation, are removed on the second peripheral circuit region III, and the second insulating film **26** on the contact region CR of the first peripheral circuit region I is also removed simultaneously. Accordingly, this embodiment does not need an additional mask process for removing the second insulating film **26** on the contact region CR, and it is made possible to selectively remove the second insulating film **26** on the contact region CR while suppressing the increase of the number of processes.

In addition, in the etching process of FIG. **4**C, only the second insulating film **26** is removed in the first peripheral circuit region I whereas the two layers of the first and second insulating films (**24**, **26**) are removed in the second peripheral circuit region III, so that the etching amount in the second peripheral circuit region III becomes larger than that in the first peripheral circuit region I. For this reason, by setting the etching amount in this process to that in the second peripheral circuit region III, it is possible to prevent excessive etching of the first and second insulating films (**24**, **26**) in the second peripheral circuit region III while the second insulating film **26** in the first peripheral circuit region I is completely removed. Therefore, since the etching of the device isolation insulating film **21** such as the first to third examples explained in the preliminary explanation of the present invention does not occur in the second peripheral circuit region III, short circuit between the conductive plugs (**45***f* to **45***i*) and the silicon substrate **20** due to the etching of the device isolation insulating film **21** can be prevented, which reduces the number of defective semiconductor devices and improves productivity.

(3) Second Embodiment

Although the transistor having the first conductor **25***a* as a gate was formed in the first embodiment, it is also possible to form a capacitor having the first conductor **25***a* and the second conductor **30** as an electrode. In this embodiment, the above-described first conductor is used in a pumping capacitor to generate high voltage for controlling a flash memory cell.

FIGS. **7**A to **7**G are the in-process sectional view of the semiconductor device according to the second embodiment of the present invention, and FIGS. **8**A to **8**C are the plan views thereof. In these drawings, reference numerals same as those of the first embodiment are attached to elements explained in the first embodiment, and their explanation will be omitted in the following.

First of all, description will be made for the process until the sectional structure shown in FIG. **7**A will be obtained.

Firstly, as described in FIG. **4**E of the first embodiment, the first and second conductive films (**25**, **30**) and the insulator **29** are patterned by using the second resist pattern **18** as an etching mask. However, the gate portion **25***b* as shown in the first embodiment is not formed in the first conductor **25***a*, which was formed by the patterning, on the first peripheral circuit region I, as shown in FIG. **7**A.

FIG. **8**A is the plan view at the point when the patterning completed, and the above FIG. **7**A corresponds to the sectional view taken along C-C line of FIG. **8**A. As shown in the drawing, the first conductor **25***a* is patterned into a rectangular shape of a capacitor lower electrode.

Next, As is ion-implanted into the silicon substrate **20** through the third window **31***a* of the third resist pattern **31** as shown in FIG. **7**B under the conditions of the accelerating energy of 50 KeV and the dose of 6×10^{14} cm^{-3}, second and third n-type source/drain extensions (**32***c*, **32***d*) are formed in the silicon substrate **20** beside the floating gate **25***d*. The third resist pattern **31** is removed after that.

Subsequently, as shown in FIG. **7**C, after forming the silicon nitride film on the entire surface, it is etched back and left as the first insulative sidewalls **33** on the side surfaces of the first insulator **30** and the floating gate **25***d*.

Next, as shown in FIG. **7**D, the fourth resist pattern **34** is formed on each region (I to III) and plasma etching is performed to the second conductor **30***a* and the second conductive film **30** by using the fourth resist pattern **34** as a mask. Thus, the first opening **30***b* is formed in the second conductor **30***a* on the contact region CR, and the second conductor **30***a* is patterned into the rectangular shape of a capacitor upper electrode. The second conductive film **30** is patterned to form the first and second gate electrodes (**30***f*, **30***g*) and the wiring **30***e* in the second peripheral circuit region III.

The fourth resist pattern **34** is removed after this.

FIG. **8**B is the plan view at the point when this process is ended, and the above FIG. **7**D corresponds to the sectional view taken along D-D line of FIG. **8**B.

Next, description will be made for the process until the sectional structure shown in FIG. **7**E will be obtained.

Firstly, by performing the processes described in FIGS. **4**I and **4**J of the first embodiment, the first and second n-type source/drain extensions (**32***e*, **32***f*) and the first and second p-type source/drain extensions (**32***g*, **32***h*) are formed in the silicon substrate **20** beside the first and second gate electrodes (**30***f*, **30***g*). Then, after forming the silicon oxide film on the entire surface by the CVD method, the silicon oxide film is etched back to form the second insulative sidewalls **37** on the side surfaces of the second conductor **30***a*, the control gate **30***d*, the wiring **30***e*, and the first and second gate electrodes (**30***f*, **30***g*).

By conducting small amount of over-etching after the etchback, the third insulating film **28** made of silicon oxide under the first opening is removed to form the second opening **29***a*, and the contact region CR is exposed from the second opening **29***a*. Note that the etchback is performed to the extent where the second insulating film **26** constituted by the ONO film is left, so that a problem of significant reduction of the device isolation insulating film **21** in the peripheral circuit regions does not occur.

Furthermore, as a result of the etchback, the first insulating film **24** under the floating gate **25***d* is patterned into the tunnel insulating film **24***b*, and the third insulating film **28** under the first and second gate electrodes (**30***f*, **30***g*) are patterned into the gate insulating films (**28***a*, **28**).

Thereafter, by performing the ion implantation process of FIGS. **4**L and **4**M described in the first embodiment, the third to sixth n-type source/drain regions (**38***c* to **38***f*) and the first and second p-type source/drain regions (**38***g*, **38***h*) are formed in the silicon substrate **20** beside the floating gate **25***d* and the first and second gate electrodes (**30***f*, **30***g*).

Next, by performing the process of FIGS. **4**N and **4**O described in the first embodiment, the basic structures of the flash memory cell FL, the n-type MOS transistor TR_n, and the p-type MOS transistor TR_p as in the sectional view of FIG. **7**G are completed. Then, as shown in FIG. **7**G, a tenth hole **44***j* having the depth reaching the second conductor **30***a* is formed, and a tenth conductive plug **45***j* electrically connected with the second conductor **30***a* is formed in the hole.

FIG. **8**C is the plan view at the point when this process is ended, and the above FIG. **7**F corresponds to the sectional view taken along E-E line of FIG. **8**C.

After this, by performing the same process described in FIG. **4**P of the first embodiment, the second interlayer insulating layer and the copper wiring are formed to complete the basic structure of the semiconductor device according to this embodiment.

In the semiconductor device, as shown in FIG. **7**G, the insulating film **26** that constitutes the insulator **29** between the first and second conductors (**25***a*, **30***a*) functions as a capacitor dielectric film, and the first and second conductors (**25***a*, **30***a*) and the insulating film **26** constitute a capacitor Q.

Although the function of the capacitor Q is not particularly limited, it is preferable to use the capacitor Q as a pumping capacitor in a voltage boost circuit that boosts the power source voltage of 1.2V to generate high voltage of 10V. The high voltage obtained in this manner is applied to the control gate **30***d* when writing or erasing is performed to the flash memory cell FL, by which electrons are injected or drawn out to/from the floating gate **25***d* via the tunnel insulating film **24***b*.

Further, since the diameter of the second opening **29***a* was set smaller than that of the first opening **30***b* in the capacitor Q, the second insulating film **26** is structured so as to expand between the side surface of the first opening **30***b* and the first conductor **25***a* as shown in the dotted line circle. According to such structure, the second insulating film **26** always exists between the first conductor **25***a* and the second conductor **30***a*, so that the breakdown voltage of the capacitor Q is not deteriorated via the second insulating film **26**.

According to this embodiment described above, as explained referring to FIGS. **4**B and **4**C in the first embodiment, the second insulating film **26** made of the ONO film on the contact region CR of the first peripheral circuit region I is removed simultaneously with the removal of the first and second insulating films (**24**, **26**) that were used as the through-film when forming the impurity regions (**22***a*, **23***b*) for adjusting threshold value of transistor by ion implantation. Consequently, it becomes possible to selectively remove the second insulating film on the contact region CR without adding the mask process, and the etching of the device isolation insulating film **21** such as the first to third examples explained in the preliminary explanation of the present invention does not occur.

(4) Third Embodiment

In this embodiment, the first conductor **25***a* described in the first embodiment is used as a resistor element.

FIGS. **9**A to **9**I are the in-process sectional views of the semiconductor device according to the third embodiment of the present invention, and FIG. **31** is the plan view thereof. In these drawings, reference numerals same as those of the first embodiment are attached to elements explained in the first embodiment, and their explanation will be omitted in the following.

First of all, description will be made for the process until the sectional structure shown in FIG. **9**A will be obtained.

Firstly, after performing the process of FIG. **4**B of the first embodiment, the first resist pattern **27** including the first windows **27***a* on the two contact regions CR of the first conductive film **25** is formed on the second insulating film **26**. Then, the second insulating film **26** on the contact regions CR is removed and the first and second insulating films (**24**, **26**) on the second peripheral circuit region III are removed by photolithography by using the first resist pattern **27** as a mask. After that, the first resist pattern **27** is removed.

Next, as shown in FIG. **9**B, the oxidation conditions same as the first embodiment is employed and silicon that is not covered by the second insulating film **26** is thermally oxidized, and a thermal oxide film formed by the oxidation is used as the third insulating film **28**. Then, a polysilicon film as the second conductive film **30** is formed on the insulator **29** that is made up of the third insulating film **28** and the second insulating film **26**.

Subsequently, as shown in FIG. **9**C, the first and second conductive films (**25**, **30**) and the insulator **29** are patterned by photolithography, and the first and second conductive films (**25**, **30**), which are left without being etched in the first peripheral circuit region I, are made into the first and second conductor (**25***a*, **30***a*), and the first and second conductive films (**25**, **30**) and the insulator in the cell region II are made into the floating gate **25***d*, the control gate **30***d*, and the intermediate insulating film **29***d*, respectively.

Next, as shown in FIG. **9**D, n-type impurity is ion-implanted to the silicon substrate **20** through the third window **31***a* of the third resist pattern **31**, and the second and third n-type source/drain extensions (**32***c*, **32***d*) are formed on the silicon substrate **20** beside the floating gate **25***d*.

The third resist pattern **31** is removed after that.

Next, as shown in FIG. **9**E, after the silicon nitride film is formed on the entire surface, it is etched back to leave it as the first insulative sidewalls **33** on the side surfaces of the second conductor **30***a* and the floating gate **25***d*.

Subsequently, as shown in FIG. **9**F, the second conductor **30***a* and the second conductive film **30** are etched while the fourth resist pattern **34**, which includes two of the fourth windows **34***a* corresponding to the two contact regions CR of the first conductor **25***a*, is used as an etching mask. Consequently, the second conductive film **30** is patterned and the first opening **30***b* is formed on the contact region CR, and the second conductive film **30** on the second peripheral circuit region III is patterned and the first and second gate electrodes (**30***f*, **30***g*) are formed. Further, the second conductive film **30** that has been extended over the device isolation insulating film **21** is also patterned into the wiring **30***e*.

After that, the fourth resist pattern **34** used in patterning is removed.

Next, as shown in FIG. **9**G, the fifth and sixth n-type source/drain extensions (**32***e*, **32***f*) and the first and second p-type source/drain extensions (**32***g*, **32***h*) are formed in the silicon substrate **20** beside the first and gate electrodes (**30***f*, **30***g*).

Then, after the silicon oxide film is formed on the entire surface by the CVD method, the silicon oxide film is etched back to form the second insulative sidewalls **37** on the side surfaces of the second conductor **30***a*, the control gate **30***d*, the wiring **30***e*, and the first and second gate electrodes (**30***f*, **30***g*).

Furthermore, as a result of the etchback, the first insulating film **24** under the floating gate **25***d* is patterned into the tunnel insulating film **24***b*, and the third insulating film **28** under the first and second gate electrodes (**30***f*, **30***g*) is patterned into the gate insulating films (**28***a*, **28***b*). Still further, the third insulating film **28** on the contact region CR of the first conductor **25***a* is removed and the second opening **29***a* smaller than the first opening **30***b* is formed, and the contact region CR is exposed on the second opening **29***a*.

Subsequently, as shown in FIG. **9**H, the third to sixth n-type source/drain extensions (**32***c* to **32***f*) and the first and second p-type source/drain extensions (**32***g*, **32***h*) are formed in the silicon substrate **20** beside the floating gate **25***d*, the first and gate electrodes (**30***f*, **30***g*).

Next, by performing the processes of FIGS. **4**H to **4**O described in the first embodiment, the first, fourth to ninth holes (**44***a*, **44***d* to **44***i*) are formed in the first interlayer insulating film **44** as shown in FIG. **9**I, and then, the first, fourth to ninth conductive plugs (**45***a*, **45***d* to **45***i*) are formed in the holes.

With the foregoing processes, the basic structure of the flash memory cell FL, n-type MOS transistor TR_n, and the p-type MOS transistor TR_p have been completed.

FIG. **10** is the plan view at the point when the processes have completed, and the above FIG. **9**I corresponds to the sectional view taken along F-F line of FIG. **10**.

After this, the second interlayer insulating layer and the copper wiring are formed by performing the process same as the one described in FIG. **4**P of the first embodiment to complete the basic structure of the semiconductor device according to this embodiment.

In the semiconductor device, as shown in FIG. **9**I, two of the first holes **44***a* are formed on the first conductor **25***a* at an interval, and the first conductive plugs **45***a* are formed in each of the first holes **44***a*. Then, a resistor element R having the two of the first conductive plugs **45***a* as a terminal and the first conductor **25***a* as a resistor is formed as shown in the drawing.

The function of the resistor element R is not particularly limited, and may be any resistor required in a logic circuit.

Meanwhile, the second conductor **30***a* on the second insulating film **26** is in an electrically floating state, and is not electrically connected with the above-described resistive element R. However, if the second conductor has short circuit with the first conductor **25***a* near the first opening **30***b*, there is a fear that electric current that should flow in the first conductor **25***a* flows into the second conductor **30***a* to lower the resistance of the resistive element R higher than a designed value.

In view of such point, the diameter of the second opening **29***a* is formed smaller than that of the first opening **30***b*. According to this, the second insulating film **26** is structured so as to expand between the side surface of the first opening **30***b* and the first conductor **25***a* as shown in the dotted line circle, so that the short circuit does not occur between the first conductor **25***a* and the second conductor **30***a* similar to the second embodiment. As the result, variation of the resistance of the resistive element R associated with the short circuit between the first and second conductors (**25***a*, **30***a*) can be controlled, and thus the resistance can be attained as designed.

Furthermore, in this embodiment described above, the second insulating film **26** made of the ONO film on the contact region CR of the first peripheral circuit region I is removed simultaneously with the removal of the first and second insulating films (**24**, **26**) that was used as the through-film when forming the impurity regions (**22***a*, **23***b*) for adjusting threshold value of transistor by ion implantation, as described referring to FIGS. **4**B to **4**C in the first embodiment. For this reason, it is possible to selectively remove the second insulating film on the contact region CR without increasing the number of processes.

Still further, similar to the first embodiment, the etching amount of the second peripheral circuit region III is larger than that in the first peripheral circuit region I in the process of removing the first and second insulating films (**24**, **26**). Therefore, by setting the etching amount in this process to that in the second peripheral circuit region III, it is possible to prevent the etching amount in the second peripheral circuit region III from becoming excessive while the second insulating film **26** on the contact region CR is completely removed, and thus the device isolation insulating film **21** of the second peripheral circuit region III can be prevented from being etched.

(5) Fourth Embodiment

In the first embodiment, the second conductor **30***a* was left in the first peripheral circuit region I, but it is removed halfway during the process in this embodiment.

FIGS. **11**A to **11**M are the in-process sectional view of the semiconductor device according to the fourth embodiment of the present invention. In these drawings, reference numerals same as those of the first embodiment are attached to elements explained in the first embodiment, and their explanation will be omitted in the following.

Firstly, by performing the process of FIG. **4**C described in the first embodiment, the second insulating film **26** is patterned as shown in FIG. **11**A. However, although the second insulating film **26** after patterning was left in the first peripheral circuit region I other than the contact region CR as well in the first embodiment, the second insulating film **26** is left by patterning only in the cell region II in this embodiment.

Subsequently, as shown in FIG. **11**B, the oxidation conditions same as the first embodiment are employed and the first conductive film **25** made of polysilicon on the first peripheral circuit region I and the silicon substrate **20** on the second peripheral circuit region III are thermally oxidized. Then, a thermal oxide film formed by the oxidation is used as the third insulating film **28**, and the third insulating film **28** and the second insulating film **26** are made to be the insulator **29**.

Then, by performing the same process as FIG. **4**E of the first embodiment, the first conductive film **25**, the insulator **29**, and the second conductive film **30** are patterned as shown in FIG. **11**C. As a result, a laminated body of the first conductor **25***a*, the third insulating film **28** constituting the insulator **29**, and the second conductor **30***a* is formed in the first peripheral circuit region I. Then, a laminated body of the floating gate **25***d* that will constitute the flash memory cell later, the intermediate insulating film **29***d*, and the control gate **30***d* is formed in the cell region II.

Next, as shown in FIG. **11**D, n-type impurity is ion-implanted into the silicon substrate **20** through the third window **31***a* of the third resist pattern **31** in the same manner as FIG. **4**F of the first embodiment. With the ion implantation, the first to fourth n-type source/drain extensions (**32***a* to **32***d*) are formed in the silicon substrate **20** beside the floating gate **25***d* and the gate portion **25***c*. After that, the third resist pattern is removed.

Subsequently, as shown in FIG. **1**E, after the silicon nitride film is formed on the entire surface, the silicon nitride film is etched back to leave it as the first insulative sidewalls **33** on the side surfaces of the second conductor **30***a* and the floating gate **25***d*.

Next, description will be made for the process until the sectional structure shown in FIG. **11**F will be obtained.

Firstly, the fourth resist pattern **34** is formed on each region (I to III). The fourth resist pattern **34** covers the cell region II and has a gate electrode shape on the second peripheral circuit region III. The first peripheral circuit region I is not covered by the fourth resist pattern **34** but exposed.

Then, the mixed gas of Cl_2 and O_2 is employed as etching gas and plasma etching is performed to the second conductor **30***a* of the first peripheral circuit region I and the second conductive film **30** of the second peripheral circuit region II while the fourth resist pattern **34** is used as a mask. As a result, all of the second conductor **30***a* is removed to expose the third insulating film **28** and the first insulative sidewalls **33** protrude from the top surface of the third insulating film **28** in the first peripheral circuit region I, and a structure where the side surfaces **33***a* of the sidewalls are exposed is obtained. Then, the second conductive film **30** is patterned into first and second gate electrodes (**30***f*, **30***g*).

The fourth resist pattern **34** is removed after this.

Subsequently, as shown in FIG. **11**G, n-type impurity is ion-implanted into the silicon substrate **20** through the fifth window **35***a* of the fifth resist pattern **35** to form the fifth and sixth n-type source/drain extensions (**32***e*, **32***f*) in the silicon substrate **20** beside the first gate electrode **30***f*. After that, the fifth resist pattern **35** is removed.

Next, as shown in FIG. **11**H, p-type impurity is ion-implanted into the silicon substrate **20** through the sixth window **36***a* of the sixth resist pattern **36** to form the first and second p-type source/drain extensions (**32***g*, **32***h*) in the silicon substrate **20** beside the second gate electrode **30***g*. After that, the sixth resist pattern **36** is removed.

Next, description will be made for the process until the sectional structure shown in FIG. **11**I will be obtained.

Firstly, after the silicon oxide film is formed on the entire surface by the CVD method, the silicon oxide film is etched back to form second insulative sidewalls **37** on the side surfaces **33***a* of the first insulative sidewalls **33**, which have been exposed after the second conductor **30***a* was removed (refer to FIG. **11**E), and on the third insulating film **28**. The second insulative sidewalls **37** are also formed on the control gate **30***d*, and the first and second gate electrodes (**30***f*, **30***g*).

Further, by continuing the etchback, the third insulating film **28** that constitutes the insulator **29** on the pad portion **25***b* is etched by using the second insulative sidewalls **37** as a mask. Thus, the third insulating film **28** of the pad portion **25***b* is patterned to form a third opening **29***b*, and a structure is obtained where a curved surface **37***a* of the second insulative sidewall **37** is in a continuous shape with the side surface of the third opening **29***b*, as shown in the dotted line circle.

Further, the first insulating film **24** is patterned by this etch back while the second insulative sidewalls **37** function as a mask, and the first insulating film **24** is left as the gate insulating film **24***a* and the tunnel insulating film **24***b* under the gate portion **25***c* and the floating gate **25***d*, respectively.

Furthermore, the third insulating film **28** is patterned in the second peripheral circuit region III, and it is left as the gate insulating films (**28***a*, **28***b*) under the first and second gates (**30***f*, **30***g*).

Subsequently, similar to the process of FIG. **4**L described in the first embodiment, the first to sixth n-type source/drain extensions (**38***a* to **38***f*) are formed in the silicon substrate **20** beside the gate portion **25***c*, the floating gate **25***d*, and the first gate electrode **30***f* by the ion implantation using the seventh resist pattern **39** as a mask, as shown in FIG. **11**J. After that, the seventh resist pattern **39** is removed.

With the foregoing processes, the basic structures of the reference transistor TR_{ref}, the flash memory cell FL, and the n-type MOS transistor TR_n have been completed.

Next, similar to the process of FIG. **4**M described in the first embodiment, the first and second p-type source/drain regions (**38***g*, **38***h*) are formed in the silicon substrate **20** beside the second gate electrode **30***g* by the ion implantation using the eighth resist pattern **40** as a mask, as shown in FIG. **11**K. After the ion implantation is ended, the eighth resist pattern **40** is removed. Then, with this process, the p-type MOS transistor TR_p described in the first embodiment is completed in the second peripheral circuit region III.

Subsequently, by performing the process of FIG. **4**N of the first embodiment, the first to eighth-silicide layers (**41***a* to **41***h*) are formed on the surface layer of each of the source/drain regions (**38***a* to **38***h*), and the first interlayer insulating film **44** on them is patterned to form first to ninth holes (**44***a* to **44***i*).

Subsequently, by performing the process of FIG. **4**O of the first embodiment, the first to ninth conductive plugs (**45***a* to **45***i*) that are electrically connected with each of the source/drain regions (**38***a* to **38***h*) are formed in the first to ninth holes (**44***a* to **44***i*).

The forming processes of the second interlayer insulating film and the copper wiring is performed after this, but its explanation will be omitted because the processes are the same as the first embodiment.

According to this embodiment described above, the second insulating film **26** on the contact region CR can be removed without adding an excessive mask process in the process shown in FIG. **11**A due to reasons described in the first to third embodiments, and it is possible to prevent the device isolation insulating film **21** from being etched when removing the second insulating film **26**.

Further, in the process shown in FIG. **11**F, the fourth resist pattern **34** was formed not covering the first peripheral circuit region I, and the second conductor **30***a* on the first peripheral circuit region I was etched and removed. According to this method, the fourth window **34***a* is not formed in the fourth resist pattern **34** as in FIG. **4**H of the first embodiment, so that there is no need to consider alignment between the fourth window **34***a* and the second conductor **30***a* and the alignment accuracy of the fourth resist pattern **34** can be loosened. Moreover, since it is possible to simplify the shape of the fourth resist pattern **34** by an amount of the fourth window **34***a* that is not formed, exposure data required for forming the fourth resist pattern **34** becomes smaller than for the first embodiment, and labor for creating the exposure data can be reduced.

(6) Fifth Embodiment

FIGS. **12**A to **12**C are the in-process sectional views of the semiconductor device according to the fifth embodiment of the present invention. In these drawings, reference numerals same as those of the first embodiment are attached to elements explained in the first embodiment, and their explanation will be omitted in the following.

First of all, description will be made for the process until the sectional structure shown in FIG. **12**A will be obtained.

Firstly, by performing the process of FIG. **4**C of the first embodiment, a polysilicon film having the thickness of about 180 nm is formed as the second conductive film **30** on the second and third insulating films (**26**, **28**) as shown in FIG. **12**A.

After that, a silicon nitride film having the thickness of 70 nm or more is formed as an anti-reflection film **50** that prevents reflection of exposure light during patterning the first and second conductive films (**25**, **30**).

Next, as shown in FIG. **12**B, the second resist pattern **18** is formed on the anti-reflection film **50**, and the anti-reflection film **50**, the first and second conductive films (**25**, **30**) and the insulator **29** are etched by using the second resist pattern **18** as a mask. Mixed gas of Cl_2 and O_2 is used as etching gas for the first and second conductive films (**25**, **30**) made of polysilicon in the etching. Further, mixed gas of CH_3 and O_2 is used as etching gas for the anti-reflection film **50** made of the silicon nitride film and the second insulating film **26** made of the ONO film.

As a result of the etching, the first and second conductive films (**25**, **30**) on the first peripheral circuit region I are made into the first and second conductors (**25***a*, **30***a*), and the first and second conductive films (**25**, **30**) and the insulator **29** on the cell region II are made into the floating gate **25***d*, the control gate **30***d*, and the intermediate insulating film **29***d*, respectively.

The second resist pattern **18** is removed after this.

Subsequently, as shown in FIG. **12**C, As of n-type impurity is ion-implanted into the silicon substrate **20** under the conditions of the accelerating energy of 50 KeV and the dose of 6×10^{15} cm^{-3}, while the thick anti-reflection film **50** having the thickness of 70 nm or more is used as a mask and ion is prevented from being implanted into the control gate **30***d* and the second conductive film **30** of the second peripheral circuit region III by the anti-reflection film **50**. Thus, the first to fourth n-type source/drain extensions (**32***a* to **32***d*) are formed in the silicon substrate **20** beside the floating gate **25***d* and the gate portion **25***c*.

After this, by performing the same processes of FIG. **4**G to **4**P described in the first embodiment, the basic structure of the semiconductor device according to the present invention is completed.

In this embodiment described above, as shown in FIG. **12**A, the anti-reflection film **50** on the control gate **30***d* has the thickness of equal to or more than 70 nm, so that the anti-reflection film **50** can block ion when the first to fourth n-type source/drain extensions (**32***a* to **32***d*) are formed by ion implantation. Therefore, the third resist pattern **31** (see FIG. **4**F), which was formed in the first embodiment in order to prevent n-type impurity from being implanted into the second conductive film **30** during ion implantation, is not necessary, and it is possible to simplify processes by the amount of the forming process of the third resist pattern.

FIG. **13** is the graph obtained by checking how much As^- ion was blocked depending on the thickness of the anti-reflection film **50** made of the silicon nitride film. Particularly, in this survey, percentage of the ratio between the concentration of B^+, which was ion-implanted into the second gate electrode **30***g* to achieve low resistance in the process of FIG. **4**M, and the concentration of As^-, which was implanted into the second gate electrode **30***g* after passing through the anti-reflection film **50** in the ion implantation process of FIG. **40**, has been calculated. The axis of ordinate of FIG. **13** denotes the percentage.

As shown in FIG. **13**, by setting the thickness of the anti-reflection film **50** made of the silicon nitride film to 70 nm or more, it is understood that almost all As^- are blocked by the anti-reflection film **50**.

(7) Sixth Embodiment

FIGS. **14**A to **14**Y are in-process sectional views of the semiconductor device according to the sixth embodiment of the present invention, and FIGS. **15**A to **15**C are its plan views.

In this embodiment, although a logic-embedded memory such as FPGA is fabricated similar to the first embodiment, the function of the logic-embedded memory can be improved significantly because a far larger number of transistors than the first embodiment are formed.

First of all, description will be made for the process until the sectional structure shown in FIG. **14**A will be obtained.

Firstly, a trench **60***a* for STI is formed in a silicon substrate **60** where the first and second peripheral circuit regions (I, III) and the cell region II are defined, and silicon oxide is formed as a device isolation insulating film **61** in the trench **60***a*. Then, the entire surface of the silicon substrate **60** is thermally oxidized to form a thermal oxide film having the thickness of about 10 nm, and it is used as a sacrifice insulating film **59**.

Note that the second peripheral circuit region III of the silicon substrate **60** is further divided into a high voltage transistor forming region III_H, a middle voltage transistor forming region III_M, and a low voltage transistor forming region III_L.

Next, as shown in FIG. **14**B, a first resist pattern **62** including a first window **62***a*, where a region in which an n-type MOS transistor is formed in the high voltage transistor forming region III_H and the cell region II are exposed, is formed on the sacrifice insulating film **59**. A part of the first peripheral circuit region I is also exposed from the first window **62***a*. Then, P^+ ion of n-type impurity is ion-implanted into the silicon substrate **60** through the first window **62***a* to form a first n-well **63** is formed in a deep portion of the silicon substrate **60**. Although the conditions of ion implantation is not particularly limited, the accelerating energy of 2 MeV and dose of 2×10^{13} cm^{-3} are employed in this embodiment.

The first resist pattern **62** is removed after this.

Next, as shown in FIG. **14**C, photoresist is coated on the sacrifice insulating film **59**, and it is exposed and developed to form a second resist pattern **58**. The second resist pattern **58** has a second window **58***a*, where a region in which an n-type MOS transistor is formed in the high voltage transistor forming region III_H and the cell region II are exposed. A part of the first peripheral circuit region I is also exposed from the second window **58***a*.

Further, third and fourth windows (**58***b*, **58***c*) are formed in the second resist pattern **58** on regions where the n-type MOS transistors are formed in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L, respectively.

Then, by implanting B^+ ion of the p-type impurity into the silicon substrate **60** based on ion implantation of the first conditions as the accelerating energy of 400 KeV and the dose of 1.5×10^{13} cm^{-3}, and the second conditions as the accelerating energy of 100 KeV and the dose of 2×10^{12} cm^{-3} by using the second resist pattern **58** as a mask, first to third p-wells (**64** to **66**) are formed.

N-type MOS transistors having high threshold voltage and n-type MOS transistors having low threshold voltage are formed in the high voltage transistor forming region III_H, and the latter threshold voltage is controlled by the first p-well **64**.

The second resist pattern **58** is removed after this.

Next, as shown in FIG. **14**D, a third resist pattern **67** including a fifth window **67** on a region, where the n-type MOS transistor having high threshold voltage is formed in the high voltage transistor forming region III_H, in each of the regions (I to III). In the third resist pattern **67**, sixth and seventh windows (**67***b*, **67***c*) are formed in addition to the fifth window **67***a* on regions where the n-type MOS transistors are formed in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L.

Then, by implanting B^+ ion of the p-type impurity into the silicon substrate **60** based on the conditions as the accelerating energy of 100 KeV and the dose of 6×10^{12} cm^{-1}, fourth to sixth p-wells (**68** to **70**) are formed.

Of these wells, the fourth p-well **68** controls the threshold voltage of the n-type MOS transistors having high threshold voltage, which will be formed later in the high voltage transistor forming region III_H. On the other hand, the fifth and sixth p-wells (**69**, **70**) have a function of a channel stop layer for the n-type MOS transistors that will be formed later in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L.

The third resist pattern **67** is removed after this.

Subsequently, as shown in FIG. **14**E, a fourth resist pattern **71** including eighth to tenth windows (**71***a* to **71***c*) on regions, where p-type MOS transistors are formed in each region (III_H, III_M, III_L), is formed on each region (I to III).

Then, by implanting P^+ ion of the n-type impurity into the silicon substrate **60** based on ion implantation of the first conditions as the accelerating energy of 600 KeV and the dose of 1.5×10^{13} cm^{-3}, and the second conditions as the accelerating energy of 240 KeV and the dose of 3×10^{12} cm^{-3} by using the fourth resist pattern **71** as a mask, second to fourth n-wells (**72** to **74**) are formed.

P-type MOS transistors having high threshold voltage and p-type MOS transistors having low threshold voltage are formed in the high voltage transistor forming region III_H, and the latter threshold voltage is controlled by the second p-well **72**.

The second resist pattern **71** is removed after this.

Next, as shown in FIG. **14**F, a fifth resist pattern **75** including eleventh window **75***a* on a region, where the p-type MOS transistors having high threshold voltage are formed in the high voltage transistor forming region III_H is formed on each region (I to III). On the fifth resist pattern **75**, twelfth and thirteenth windows (**75***b*, **75***c*) are formed on regions where the p-type MOS transistors are formed in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L.

Then, by implanting P^+ ion of the n-type impurity into the silicon substrate **60** based on the conditions as the accelerating energy of 240 KeV and the dose of 6.5×10^{12} cm^{-3} while the fifth resist pattern **75** is used as a mask, fifth to seventh n-wells (**76** to **78**) are formed.

Of these wells, the fifth n-well **76** controls the threshold voltage of the p-type MOS transistors having high threshold voltage, which will be formed later in the high voltage transistor forming region III_H. On the other hand, the sixth and seventh n-wells (**77**, **78**) have a function of a channel stop layer for the p-type MOS transistors that will be formed later in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L.

The fifth resist pattern **75** is removed after this.

Subsequently, as shown in FIG. **14**G, a sixth resist pattern **79** including a fourteenth window **79***a* on the first peripheral circuit region I and the cell region II is formed in each region (I to III). Then, B^+ of the p-type impurity is ion-implanted into the silicon substrate **60** under the conditions of the accelerating energy of 40 KeV and the dose of 6×10^{13} cm^{-3} while the sixth resist pattern **79** is used as a mask, and a first p-type impurity diffusion region **80** is formed. The first p-type impurity diffusion region **80** serves to control the threshold voltage of a flash memory cell that will be formed later in the cell region II.

After this, the sixth resist pattern **79** is removed.

Next, description will be made for the process until the sectional structure shown in FIG. **14**H will be obtained.

Firstly, the sacrifice insulating film **59** is removed by wet etching of hydrofluoric acid solution to expose a clean surface of the silicon substrate **60**. Then, a thermal oxide film having the thickness of about 10 nm is formed on the silicon substrate **60** in the mixed atmosphere of Ar and O_2 under the thermal treatment condition to set the temperature of substrate to 900° C. to 1050° C., and it is used as a first insulating film **81**. The first insulating film **81** will be the tunnel insulating film of the flash memory cell later.

Subsequently, description will be made for the process until the sectional structure shown in FIG. **14**I will be obtained.

Firstly, a polysilicon film into which phosphorous is doped in-situ is formed on the first insulating film **81** at the thickness of about 90 nm by the low pressure CVD method where SiH_4 and PH_3 are used as reactive gas, and it is used as a first conductive film **82**. Subsequently, the first conductive film **82** is patterned by photolithography and removed from the second peripheral circuit region III. The first conductive film **82** in the cell region II becomes a stripe shape in word line directions.

Next, a silicon oxide film and a silicon nitride film are formed in this order on the first conductive film **82** and the first insulating film **81** in the second peripheral circuit region III in the thickness of 5 nm and 10 nm, respectively, by using the low pressure CVD method. Further, the surface of the silicon nitride film is oxidized in O_2 atmosphere under the condition of substrate temperature at about 950° C. to form a silicon oxide film having the thickness of about 3 nm on the surface of the film. Consequently, the ONO film, where the silicon oxide film, the silicon nitride film, and the silicon oxide film are laminated in this order, is formed as a second insulating film **83** on the entire surface.

Note that due to the thermal treatment when oxidizing the silicon nitride film in the ONO film or the thermal treatment when forming the first insulating film **81** described in FIG. **14**H, the impurity in the wells that were formed in the silicon substrate **60** is diffused by about 0.1 to 0.2 μm or more and the impurity distribution in the wells becomes broad.

Subsequently, as shown in FIG. **14**J, a seventh resist pattern **84** including a fifteenth window **84***a* on a region, where n-type transistors are formed in the middle voltage transistor forming region III_M, is formed on each region (I to III). Then, B^+ of the p-type impurity is ion-implanted into the silicon substrate **60** under the conditions of the accelerating energy of 30 KeV and the dose of 5×10^{12} cm^{-1}, while the seventh resist pattern **84** is used as a mask and the first and second insulating films (**81**, **83**) are used as a through-film. Consequently, a second p-type impurity diffusion region **85** for adjusting the threshold voltage of the n-type transistor is formed in the middle voltage transistor forming region III_M.

After this, the seventh resist pattern **84** is removed.

Next, as shown in FIG. **14**K, an eighth resist pattern **86** including a sixteenth window **86***a* on a region, where p-type transistors are formed in the middle voltage transistor forming region III_M, is formed on each region (I to III). Then, As^- ion of the n-type impurity is ion-implanted into the silicon substrate **60** under the conditions of the accelerating energy of 150 KeV and the dose of 3×10^{12} cm^{-3}, while the eighth resist pattern **86** is used as a mask and the first and second insulating films (**81**, **83**) are used as a through-film. Consequently, a first n-type impurity diffusion region **87** for adjusting the threshold voltage of the p-type transistor is formed in the middle voltage transistor forming region III_M.

After this, the eighth resist pattern **86** is removed.

Next, as shown in FIG. **14**L, photoresist is coated on the second insulating film **83**, and it is exposed and developed to form a ninth resist pattern **88** including a seventeenth window **88***a* on the low voltage transistor forming region III_L.

Two n-type MOS transistors having high threshold voltage and low threshold voltage and two p-type MOS transistors having high threshold voltage and low threshold voltage will be formed later in the low voltage transistor forming region III_L, and the above-described seventeenth window **88***a* is formed on a region where the n-type MOS transistor having high threshold voltage will be formed.

Then, B^+ of the p-type impurity is ion-implanted into the silicon substrate **60** through the seventeenth window **88***a* under the conditions of the accelerating energy of 10 KeV and the dose of 5×10^{12} cm^{-3}, while the first and second insulating films (**81**, **83**) are used as a through-film. Consequently, a third p-type impurity diffusion region **89** for adjusting the threshold voltage of the n-type transistor having high threshold voltage is formed in the low voltage transistor forming region III_L.

After this, the ninth resist pattern **88** is removed.

Subsequently, as shown in FIG. **14**M, a tenth resist pattern **90** including a tenth window **90***a* on a region, where an p-type transistor having high threshold voltage is formed in the low voltage transistor forming region III_L, is formed on each region (I to III). Then, As^+ ion of the n-type impurity is ion-implanted into the silicon substrate **60** under the conditions of the accelerating energy of 100 KeV and the dose of 5×10^{12} cm^{-3}, while the first and second insulating films (**81**, **83**) are used as a through-film, and a second n-type impurity diffusion region **91** for adjusting the threshold voltage of the p-type transistor having high threshold voltage is formed.

The tenth resist pattern **90** is removed after the ion implantation is finished.

With the foregoing processes, the formation of the diffusion regions (**85**, **87**, **89**, **91**) for controlling the threshold voltage of the transistors in the second peripheral circuit region III has been completed, so that the first and second insulating films (**81**, **83**) in the second peripheral circuit region III, which were used as the through-film in forming the diffusion regions by ion implantation, are not necessary in the following processes.

Therefore, in the next process shown in FIG. **14**N, the first and second insulating films (**81**, **83**) in the second peripheral circuit region III are removed. To do this, an eleventh resist pattern **92** covering the cell region II is formed on the second insulating film **83** as shown in FIG. **14**N. The contact region CR of the first conductive film **82** in the first peripheral circuit region I and the second peripheral circuit region III are not covered by the eleventh resist pattern **92** but exposed.

Next, the second insulating film **83** on the contact region CR and the first and second insulating films (**81**, **83**) in the second peripheral circuit region III are etched and removed by plasma etching using the mixed gas of CH_3 and O_2 and by subsequent wet etching by HF solution while the eleventh resist pattern **92** is used as a mask. Consequently, the second insulating film **83** is left only in a region other than the contact region CR and the silicon substrate **60** in the second peripheral circuit region III is exposed.

Then, after removing the eleventh resist pattern **92** by oxygen ashing, the surface of the silicon substrate **60** is cleaned by wet treatment.

Next, description will be made for the process until the sectional structure shown in FIG. **14**O will be obtained.

Firstly, the oxidizing condition where substrate temperature is set to 850° C. is employed, and the surface of the silicon substrate **60** exposed in the second peripheral circuit region III is thermally oxidized only by the thickness of 13 nm, and a thermal oxide film formed by the thermal oxidation is used as a third insulating film **94**. In this thermal oxidation, the third insulating film **94** made of thermal oxide film is also formed on the contact region CR of the first conductive film **82** that is not covered by the second insulating film **83** but exposed.

Next, a twelfth resist pattern **93** is formed on the cell region II and the high voltage transistor forming region III_H. Then, the third insulating film **94** on the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L is etched and removed by wet etching using HF solution while the twelfth resist pattern **93** is used as a mask. Further, in this etching, the third insulating film **94** made of thermal oxide film on the contact region CR of the first conductive film **82** is also etched, by which the contact region CR is exposed.

After this, the twelfth resist pattern **93** is removed.

Next, description will be made for the process until the sectional structure shown in FIG. **14**P will be obtained.

Firstly, the oxidizing condition where substrate temperature is set to 850° C. in oxygen atmosphere is employed, and the surface of the silicon substrate **60** exposed in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L is thermally oxidized only by the thickness of about 6 nm, and a thermal oxide film formed by the thermal oxidation is used as a fourth insulating film **96**. The fourth insulating film **96** is also formed on the contact region CR of the first conductive film **82** similar to the previous third insulating film **94**.

Subsequently, a third resist pattern **95** is formed on the cell region II, the high voltage transistor forming region III_H, and the middle voltage transistor forming region III_M. Then, the fourth insulating film **96** on the contact region CR and the low voltage transistor forming region III_L is etched and removed by wet etching using HF solution while the thirteenth resist pattern **95** is used as a mask.

After this, the thirteenth resist pattern **95** is removed.

Next, description will be made for the process until the sectional structure shown in FIG. **14**Q will be obtained.

Firstly, the oxidizing condition where substrate temperature is set to 850° C. in oxygen atmosphere is employed, and silicon of an area that is not covered by the second to fourth insulating films (**83**, **94**, **96**) is thermally oxidized only by the thickness of about 2.2 nm. Thus, a thermal oxide film having the thickness of about 2.2 nm is formed as a fifth insulating film **97** on the surfaces of the contact region CR of the first conductive film **82** made of polysilicon and the silicon substrate **60** in the low voltage transistor forming region III_L. The fifth insulating film **97** is formed adjacent to the second insulating film **83**, and the second and fifth insulating films (**83**, **97**) constitute an insulator **99**. Note that the thickness of the fifth insulating film **97** formed in the contact region CR in this manner is significantly thinner than the second insulating film **83**.

Further, as a result of forming the fifth insulating film **97** by thermal oxidation, the final thickness of the third insulating film **94** and the fourth insulating film **96** becomes 16 nm and 7 nm, respectively.

Thereafter, a non-doped polysilicon film having the thickness of about 180 nm is formed as a second conductive film **100** on the entire surface by the low pressure CVD method using SiH_4 as reactive gas.

Next, description will be made for the process until the sectional structure shown in FIG. **14**R will be obtained.

Firstly, photoresist is coated on the second conductive film **100**, and it is exposed and developed to form a fourteenth resist pattern **101**. Next, the first and second conductive films (**82**, **100**) and the insulator **99** are patterned by using the fourteenth resist pattern **101** as an etching mask. The patterning is conducted in a plasma etching chamber, the mixed gas of Cl_2 and O_2 is used as etching gas for the first and second conductive films (**82**, **100**) made of polysilicon, and the mixed gas of CH_3 and O_2 is used as etching gas for the second insulating film **83** made of the ONO film constituting the insulator **99**.

As a result of the patterning, the first and second conductive films (**82**, **100**) in the first peripheral circuit region I are made into first and second conductor (**85***a*, **100***a*) respectively while the second conductive film **100** is left in the second peripheral circuit region III. In the cell region, the first and second conductive films (**82**, **100**) and the insulator **99** are made into a floating gate **82***d*, a control gate **100***d*, and an intermediate insulating film **99***d*, respectively.

After this, the fourteenth resist pattern **101** is removed.

FIG. **15**A is the plan view after completing the process, and the above FIG. **14**R corresponds to the sectional view taken along G-G line of FIG. **15**A. It is to be noted that the second conductor **100***a* is omitted in the first peripheral circuit region I and the second peripheral circuit region III is omitted to make the layout of be easily read in FIG. **15**A.

As shown in FIG. **15**A, the second conductor **82***a* is made up of a pad portion **82***b* and a gate portion **82***c* on the first insulating film **24**.

Next, description will be made for the process until the sectional structure shown in FIG. **14**S will be obtained.

Firstly, by thermally oxidizing the side surfaces of the floating gate **82***d* and the control gate **100***d*, an extremely thin thermal oxide film (not shown) is formed on the side surfaces. The thermal oxide film serves to improve the retention characteristic of the flash memory cell.

Subsequently, a resist pattern (not shown) covering the second conductor **100***a*, the control gate **100***d*, and the second conductive film **100** is formed, and As^+ is ion-implanted as n-type impurity into the silicon substrate **60** by using the resist pattern as a mask. Although the conditions of the ion implantation is not particularly limited, the accelerating energy of 50 KeV and dose of 6×10^{14} cm^{-3}, for example, are employed in this embodiment. As a result of such ion implantation, second to fourth n-type source/drain extensions (**102**_b_ to **102**_d_) are formed in areas beside the first conductor **82**_a_ and the floating gate **82**_d_.

The above-described resist pattern is removed after this, and the side surfaces of the floating gate **82**_d_ and the control gate **100**_d_ are thermally oxidized again to form a thermal oxide film (not shown).

Next, as shown in FIG. **14**T, after forming a silicon nitride film on the entire surface, it is etched back to leave it as first sidewalls **103** on the side surfaces of the second conductor **100**_a_ and the floating gate **82**_d_.

Next, as shown in FIG. **14**U, the second conductor **100**_a_ on the first peripheral circuit region I and the second conductive film **100** on the second peripheral circuit region III are patterned by photolithography. Consequently, the second conductor **100**_a_ on the contact region CR is removed and a first opening **100**_b_ is formed, and first to tenth gate electrodes (**100**_e_ to **100**_n_) made of the patterned second conductive film **100** are formed in the second peripheral circuit region III.

Subsequently, as shown in FIG. **14**V, the n-type impurity such as As is ion-implanted into the silicon substrate **60** by using the first to tenth gate electrodes (**100**_e_ to **100**_n_) and a resist pattern (not shown) as a mask, and thus fifth to fourteenth n-type source/drain extensions (**102**_e_ to **102**_n_) as described in the drawing are formed. Similarly, by performing ion implantation of the p-type impurity such as B into the silicon substrate **60**, first to tenth p-type source/drain extensions (**102**_p_ to **102**_y_) as shown in the drawing are formed. Note that the implantation of the above-described n-type impurity and p-type impurity are severally performed using resist patterns (not shown) and the resist patterns are removed after the ion implantation is completed.

Next, description will be made for the process until the sectional structure shown in FIG. **14**W will be obtained.

Firstly, after forming a silicon oxide film on the entire surface, the silicon oxide film is etched back to form second insulative sidewalls **104** on the side surfaces of the second conductor **100**_a_, the control gate **100**_d_, and the first to tenth gate electrodes (**100**_e_ to **100**_n_). Then, by performing overetching after the etchback, the fifth insulating film **97** constituting the insulator **99** on the pad portion **25**_b_ is etched while the second insulative sidewalls **104** are used as a mask. Thus, a second opening **99**_a_ having a smaller diameter than the first opening **100**_b_ is formed on the insulator **99**, and the contact region CR is exposed and the silicon substrate **60** of the second peripheral circuit region II is exposed from the second opening **99**_a_.

Further, the first insulating film **81** is patterned by the etchback while the second insulative sidewalls **104** work as a mask, and the first insulating film **81** is left as the gate insulating film **81**_a_ and the tunnel insulating film **81**_b_ under the first conductor **82**_a_ and the floating gate **82**_d_, respectively.

Furthermore, the third to fifth insulating films (**94**, **96**, **97**) are patterned in the second peripheral circuit region III while the first to tenth gate electrodes (**100**_e_ to **100**_n_) work as a mask, and the insulating films are left as gate insulating films (**94**_a_ to **94**_d_, **96**_a_, **96**_b_, **97**_a_ to **97**_d_).

Subsequently, by ion implantation using the second insulative sidewalls **104**, control gate **100**_d_, and the first to tenth gate electrodes (**100**_e_ to **100**_n_) as a mask, first to fourteenth n-type source/drain regions (**105**_a_ to **105**_n_) and first to fourteenth p-type source/drain regions (**105**_p_ to **105**_y_) as shown in the drawing are formed. The implantation of the above-described n-type impurity and p-type impurity are severally performed using resist patterns (not shown) and the resist patterns are removed after the ion implantation is completed.

With the above processes, the n-type MOS transistors (TR_n (Low Vth), TR_n(High Vth) and the p-type MOS transistors (TR_p(Low Vth), TR_p(High Vth), which constitute the logic circuit such as a sense amplifier, are formed in the high voltage transistor forming region III_H and the low voltage transistor forming region III_L. Low Vth and High Vth attached to each transistor denotes high/low of the threshold voltage of the transistor.

When transistors having high threshold voltage and low threshold voltage are mixed, it is possible to operate the circuit in high-speed by using transistors having low threshold voltage. At a stand-by state, the transistors having low threshold voltage are turned off and transistors having high threshold voltage are used instead and they can suppress leakage current that occurs during stand-by.

Further, of the above-described transistors, transistors formed in the high voltage transistor forming region III_H become high voltage transistors having the voltage of 5V applied to the gate electrodes and transistors formed in the low voltage transistor forming region III_L become low voltage transistors having 1.2V.

Then, the n-type MOS transistor TR_n and the p-type MOS transistor TR_p, whose applied voltage is 2.5V, are formed in the middle voltage transistor forming region III_M as shown in the drawing.

On the other hand, a flash memory cell FL, which is made up of the control gate **100**_d_, the intermediate insulating film **99**_d_, the floating gate **82**_d_, the tunnel insulating film **81**_b_, and third and fourth n-type source/drain regions (**105**_c_, **105**_d_), is formed in the cell region II.

FIG. **15**B is the plan view after completing the process, and the previous FIG. **14**W corresponds to the sectional view taken along H-H line of FIG. **15**B. It is to be noted that the second peripheral circuit region III is omitted to make the layout be easily read in FIG. **15**B.

As shown in FIG. **15**B, a first n-type source/drain region **105**_a_ is formed in the silicon substrate **60** beside the gate portion **82**_c_ of the first conductor **82**_a_. Then, the first and second n-type source/drain regions (**105**_a_, **105**_b_), the gate insulating film **81**_a_ (refer to FIG. **14**W), and the gate portion **82**_c_ constitute the reference transistor TR_{ref}.

Next, description will be made for the process until the sectional structure shown in FIG. **14**X will be obtained.

Firstly, after a cobalt film is formed on the entire surface at the thickness of about 8 nm by the sputtering method, the cobalt film is annealed to allow it to react with silicon. Then, the cobalt film on a device isolation insulating film **61** or the like, which has not been reacted, is removed by wet etching to form cobalt-silicide layers (**106**_b_ to **106**_y_) on the surface layer of the silicon substrate **60** and gate electrodes.

Subsequently, a silicon nitride film is formed in the thickness of about 50 nm by the CVD method, and is used as an etching stopper film **107**. Next, a silicon oxide film as a sixth insulating film **108** is formed on the etching stopper film **107** by the CVD method, and the etching stopper film **107** and the sixth insulating film **108** are made to be a first interlayer insulating film **109**. Note that the thickness of the sixth insulating film **108** is about 1 μm on the flat surface of the silicon substrate **60**.

Subsequently, the top surface of the first interlayer insulating film **109** is polished to make it flat by the CMP method. Then, the first interlayer insulating film **109** is patterned by photolithography to form first, third to twenty-fifth holes (**109**_a_, **109**_c_ to **109**_y_). Of these holes, the first hole **109**_a_ is positioned on the contact region CR of the first conductor **82***a* and formed inside the first and second openings (**100***b*, **99***a*). Further, the remaining third to twenty-fifth holes (**109***c* to **109***y*) are respectively formed on the cobalt-silicide layers (**106***b* to **106***y*).

Furthermore, a Ti film and a TiN film are formed in this order the first, third to twenty-fifth holes (**109***a*, **109***c* to **109***y*) and on the first interlayer insulating film **109** by the sputtering method, and they are used as a glue-film. Then, a W film is formed on the glue-film by the CVD method using tungsten hexafluoride as reactive gas to completely fill the inside of the first, third to twenty-fifth holes (**109***a*, **109***c* to **109***y*). Then, excessive W film and glue-film formed on the top surface of the first interlayer insulating film **109** are removed by the CMP method, and they are left as first, third to twenty-fifth conductive plugs (**110***a*, **110***c* to **110***y*) inside the first, third to twenty-fifth holes (**109***a*, **109***c* to **109***y*).

Next, description will be made for the process until the sectional structure shown in FIG. **14**Y will be obtained.

Firstly, after a low dielectric constant insulating film **111** of a coating type is formed on the entire surface, a silicon oxide film is formed on it as a cover insulating film **112**, and the low dielectric constant insulating film **111** and the cover insulating film **112** are made to be a second interlayer insulating film **113**.

Subsequently, the second interlayer insulating film **113** is patterned by photolithography to form wiring grooves **113***a*.

Then, a Cu film is formed as a seed layer on the entire surface by the sputtering method after deposition of TaN, an electrolytic copper plated film is formed on the seed layer by supplying electric power to the seed layer, and each wiring groove **113***a* is completely filled by the copper plated film. After that, excessive seed layer and copper plated film formed on the second interlayer insulating film **113** are removed by the CMP method, and they are left in each wiring groove **113***a* as copper wirings **114**.

FIG. **15**C is the plan view after the process has been finished, and the previous FIG. **14**Y corresponds to the sectional view taken along J-J line of FIG. **15**C. It is to be noted that the second peripheral circuit region III is omitted and copper wirings **114** and the second interlayer insulating film **113** in FIG. **15**C are omitted to make the planar layout of each layer be easily read.

As shown in the drawing, the second n-type source/drain region is formed in the silicon substrate **60** beside the gate portion **82***c* of the first conductor **82***a*, and a second conductive plug is electrically connected thereon. The second conductive plug is formed inside the second hole formed in the second interlayer insulating film, and is formed in the same process as the remaining first, third to twenty-fifth conductive plugs (**110***a*, **110***c* to **110***y*).

With the foregoing processes, the basic structure of the semiconductor device according to this embodiment is completed.

According to the manufacturing method of the semiconductor device, as shown in FIGS. **14**J to **14**M, the wells (**85**, **87**, **89**, **91**) for adjusting threshold voltage are formed in the middle voltage transistor forming region III_M and the low voltage transistor forming region III_L while the second insulating film **83** is used as a through-film. Then, as shown in FIG. **14**N, the second insulating films **83**, whose function as a through-film has ended after the completion of ion implantation, is removed on the second peripheral circuit region III, and the second insulating film **83** on the contact region CR of the first conductor **82***a* is also removed simultaneously. As described, since the removing process of the through-film combines the removing process of the second insulating film **83** on the contact region CR, it becomes possible to remove the second insulating film **83** on the contact region CR without adding an additional mask process.

According to the present invention, the step of removing the second insulating film, which is not needed after it has been used as the through-film for impurity implantation, in the third region combines the step of removing the second insulating film on the contact region, so that the second insulating film above the contact region can be selectively removed without adding an additional mask step.

Further, etching amount in the third region is larger than that in the second region in the step of removing the second insulating film. Therefore, by setting the etching amount on this step to that in the third region, it is possible to prevent excessive etching of the first and second insulating films in the third region while the second insulating film in the second region is completely removed and to prevent an etching from occurring on the device isolation insulating film or the like under the films.

What is claimed is:

1. A semiconductor device comprising:

a laminated structure body, which integrally has on a first region of a semiconductor substrate: a first portion where a first insulating film, a first conductor, a second insulating film, and a second conductor sequentially remain; a second portion where said first conductor and said second conductor are laminated on said semiconductor substrate; and a third portion where neither said second insulating film nor said second conductor remains on said semiconductor substrate; and

a third insulating film, which covers said laminated structure body and includes one or more holes where one or more contact regions of said first conductor of said laminated structure body are exposed at one or more parts of said third portion, wherein said second conductor has a first opening corresponding to said third portion, and

said second insulating film has a second opening that is larger than said first opening.

2. The semiconductor device according to claim **1**, wherein said first insulating film is a silicon oxide film.

3. The semiconductor device according to claim **1**, wherein said second insulating film is an ONO film.

4. The semiconductor device according to claim **1**, comprising:

a flash memory cell made up of a tunnel insulating film, a floating gate constructed from the same material as said first conductor, an intermediate insulating film constructed from the same material as said second insulating film, and a control gate constructed from the same material as said second conductor, which sequentially remain on a second region of said semiconductor substrate, and first and second source/drain regions remaining in said semiconductor substrate beside said floating gate.

5. The semiconductor device according to claim **1**, wherein

said first conductor is made up of a pad portion remaining in said contact region and a gate

portion connected to the pad portion,

third and fourth source/drain regions remain in said semiconductor substrate beside said gate portion, and

said first insulating film, said gate portion, and said third and fourth source/drain regions

constitute a transistor.

6. The semiconductor device according to claim **5**, wherein said first opening remains in said second conductor on said contact region of said pad portion, a silicon oxide film including said second opening on said pad portion inside said first opening remains, and said hole remains inside said first and second openings.

7. The semiconductor device according to claim **1**, wherein said second conductor is in an electrically floating state.

8. The semiconductor device according to claim **1**, wherein further

a fourth insulating film remains between said first conductor and said second conductor in the second portion.

9. A semiconductor device comprising:

a laminated structure body, which integrally has on a first region of a semiconductor substrate: a first portion where a first insulating film, a first conductor, a second insulating film, and a second conductor sequentially remain; a second portion where said first conductor and said second insulating film are laminated on said semiconductor substrate; and a third portion where neither said second insulating film nor said second conductor remains on said semiconductor substrate; and

a third insulating film, which covers said laminated structure body and includes one or more holes where one or more contact regions of said first conductor of said laminated structure body are exposed at one or more parts of said third portion, wherein

said second insulating film has a first opening corresponding to said third portion, and

said second conductor has a second opening that is larger than said first opening.

10. The semiconductor device according to claim **9**, wherein said first conductor, said second insulating film, and said second conductor constitute a capacitor.

11. The semiconductor device according to claim **9**, wherein

two of said holes are formed at an interval, conductive plugs that are electrically connected with said contact regions remain in the each holes, and the two conductive plugs and said first conductor constitute a resistive element.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,169,017 B2
APPLICATION NO. : 12/285275
DATED : May 1, 2012
INVENTOR(S) : Taiji Ema et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

ON THE TITLE PAGE, ITEM 75;
Change

"(75) Inventors: **Taija Ema**, **Kawasaki** (JP); **Toru Anezaki**, **Kawasaki** (JP)"

To be

--(75) Inventors: **Taiji Ema, Kawasaki** (JP); **Toru Anezaki, Kawasaki** (JP)--

Signed and Sealed this
Second Day of October, 2012

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office