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(54) **SINGLE CHIP MICROCONTROLLER INCLUDING BATTERY MANAGEMENT AND PROTECTION**

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See application file for complete search history.

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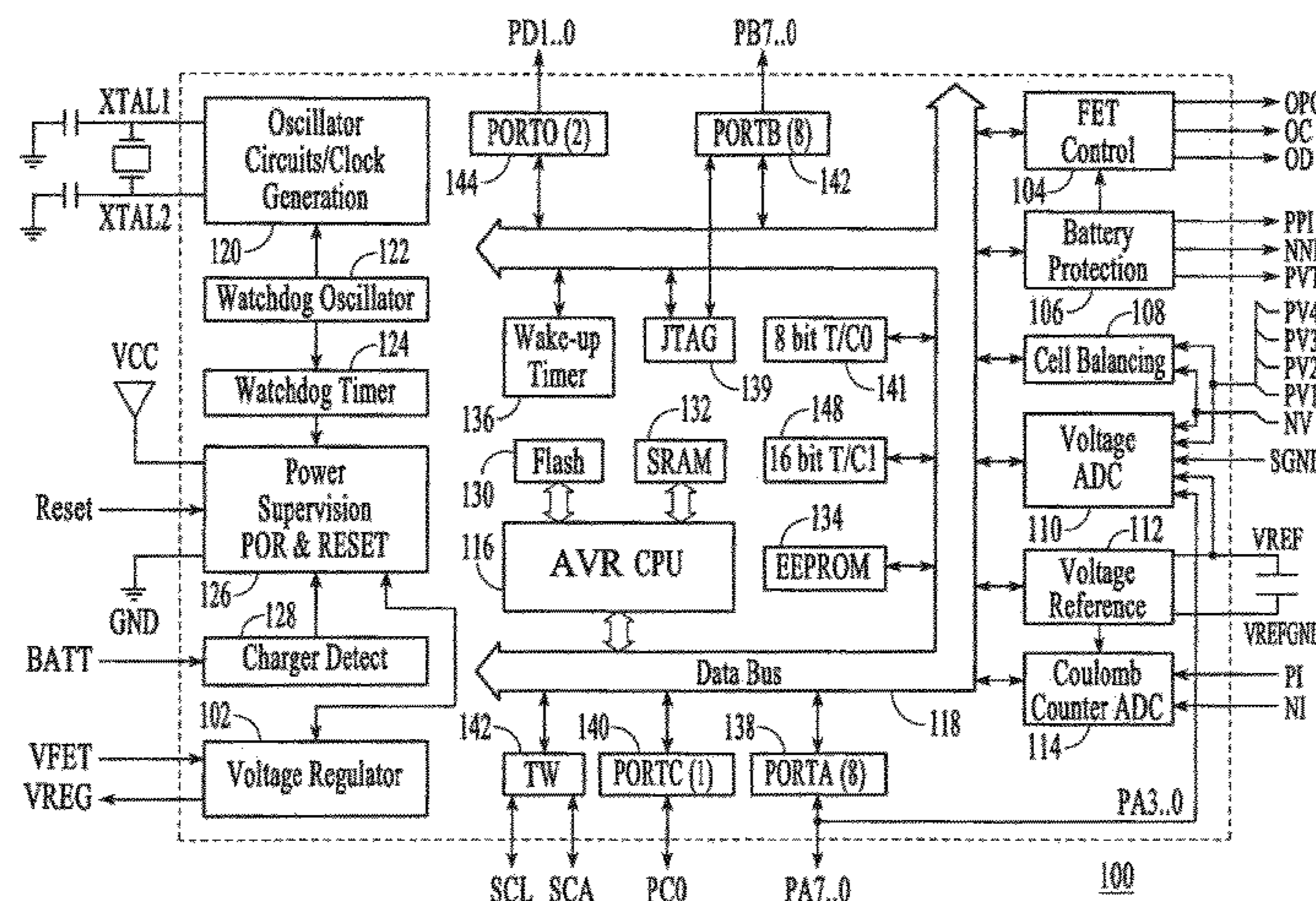
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(57) **ABSTRACT**

A microcontroller is disclosed. The microcontroller comprises a processor system and a high voltage interface coupled to the processor system and adapted to be coupled to a battery. The microcontroller further includes a battery management system for monitoring the battery and managing the battery based upon the monitoring of the battery. The microcontroller is a single chip. This one-chip solution saves design cost and PCB space in addition to broadening the functionality of the smart battery application. With the accuracy of the microcontroller, the charge status of the battery can be predicted more accurately and therefore effectively increases actual battery capacity.

20 Claims, 7 Drawing Sheets



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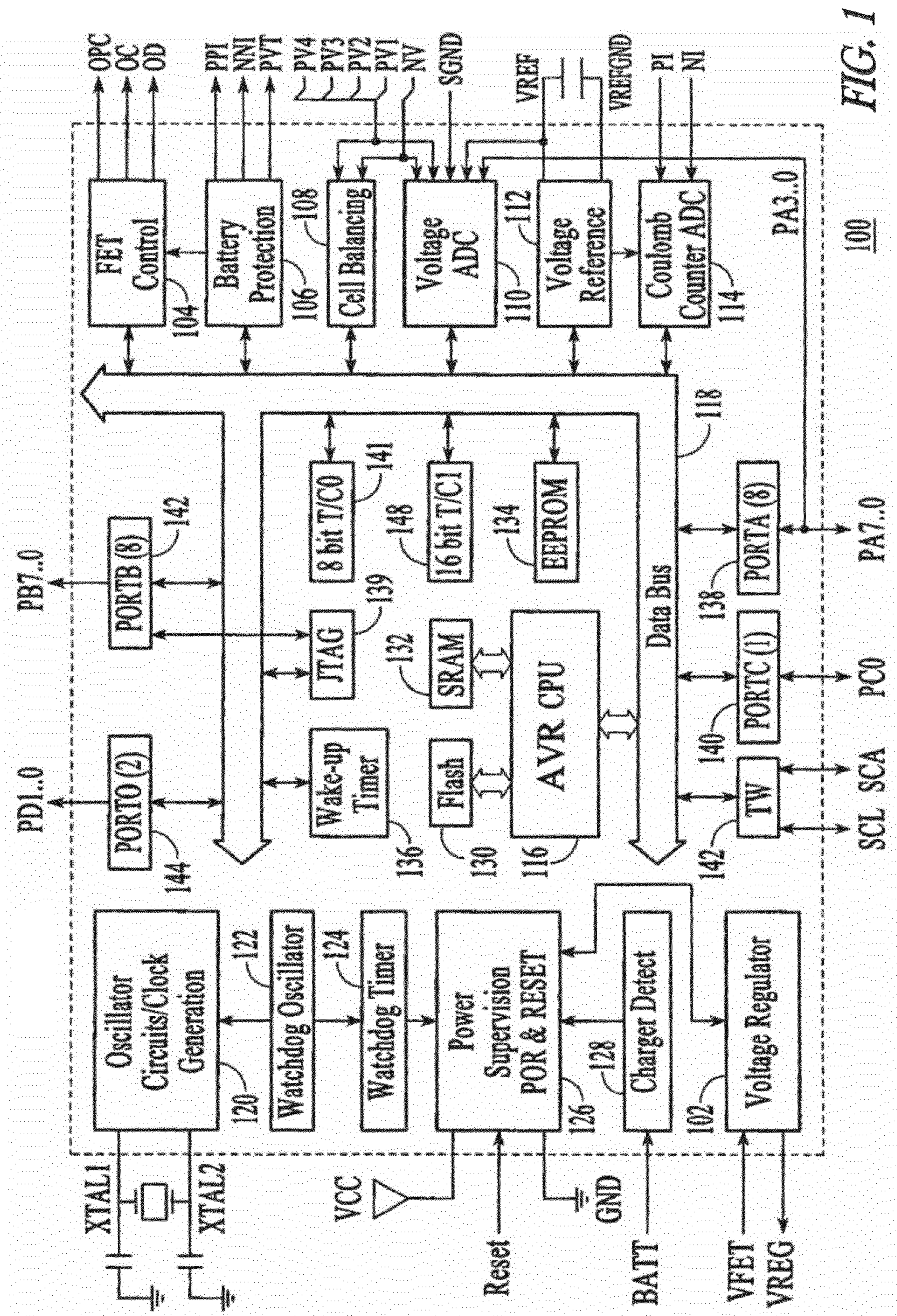


FIG. 1

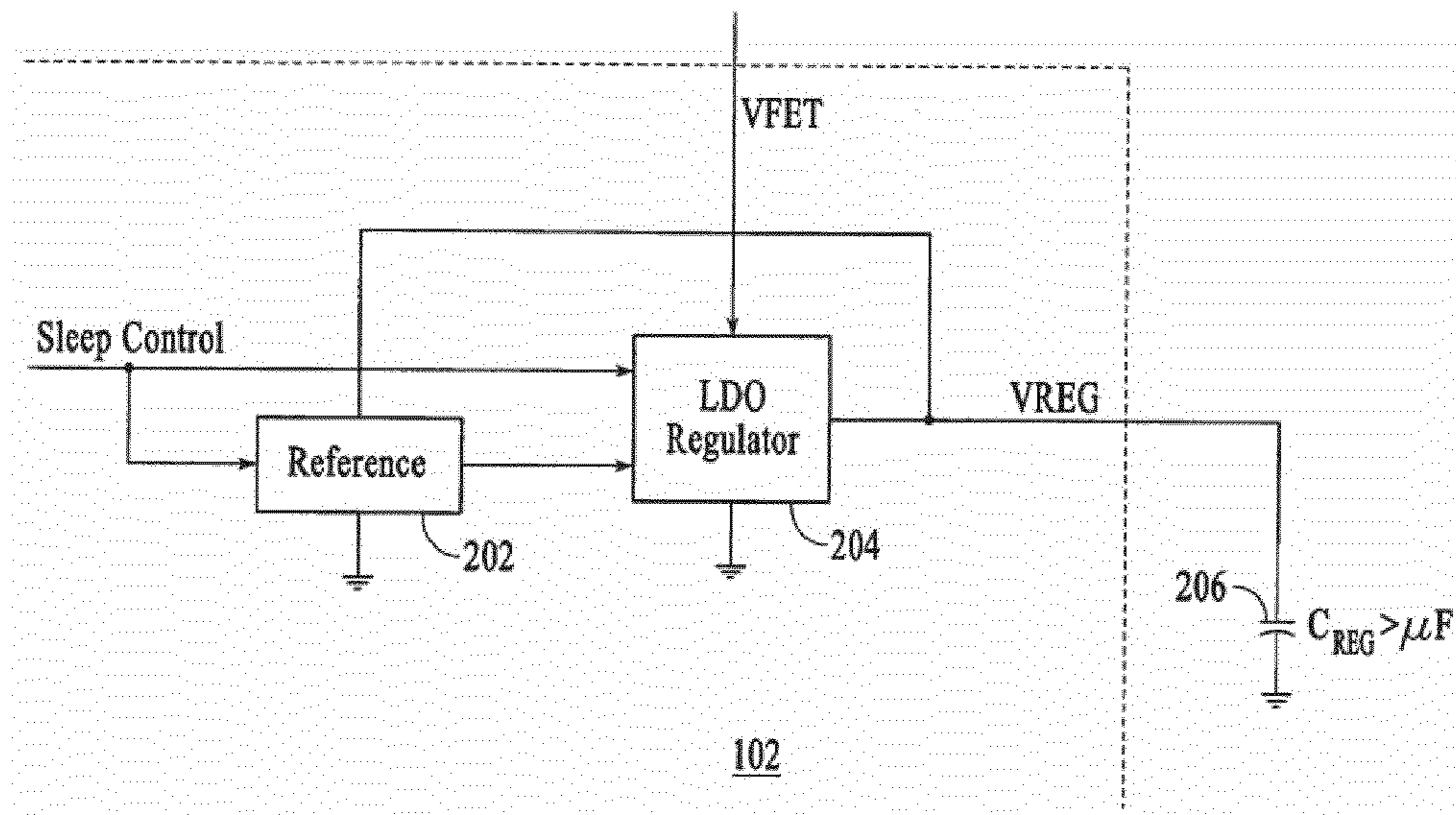


FIG. 2

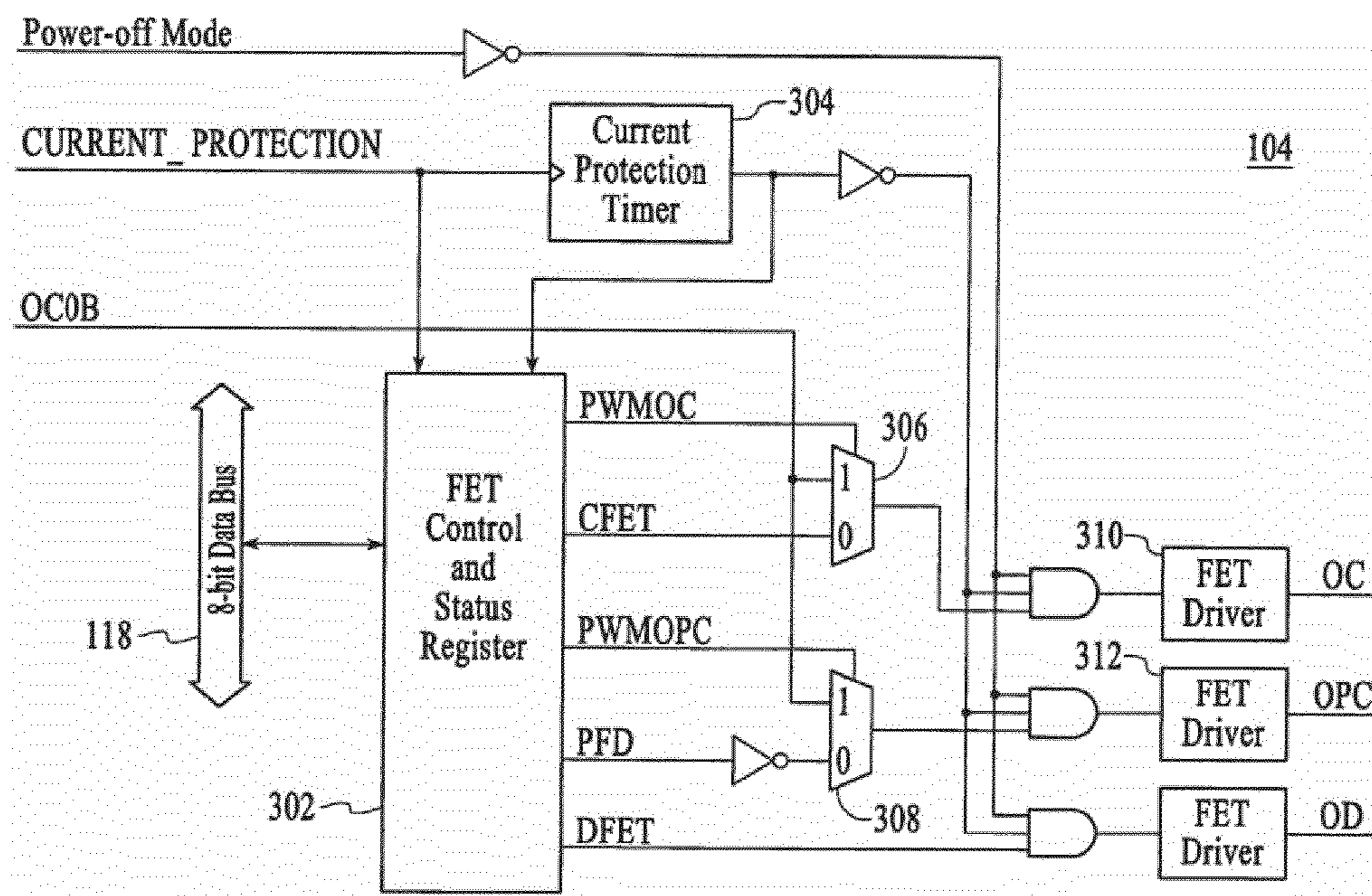


FIG. 3

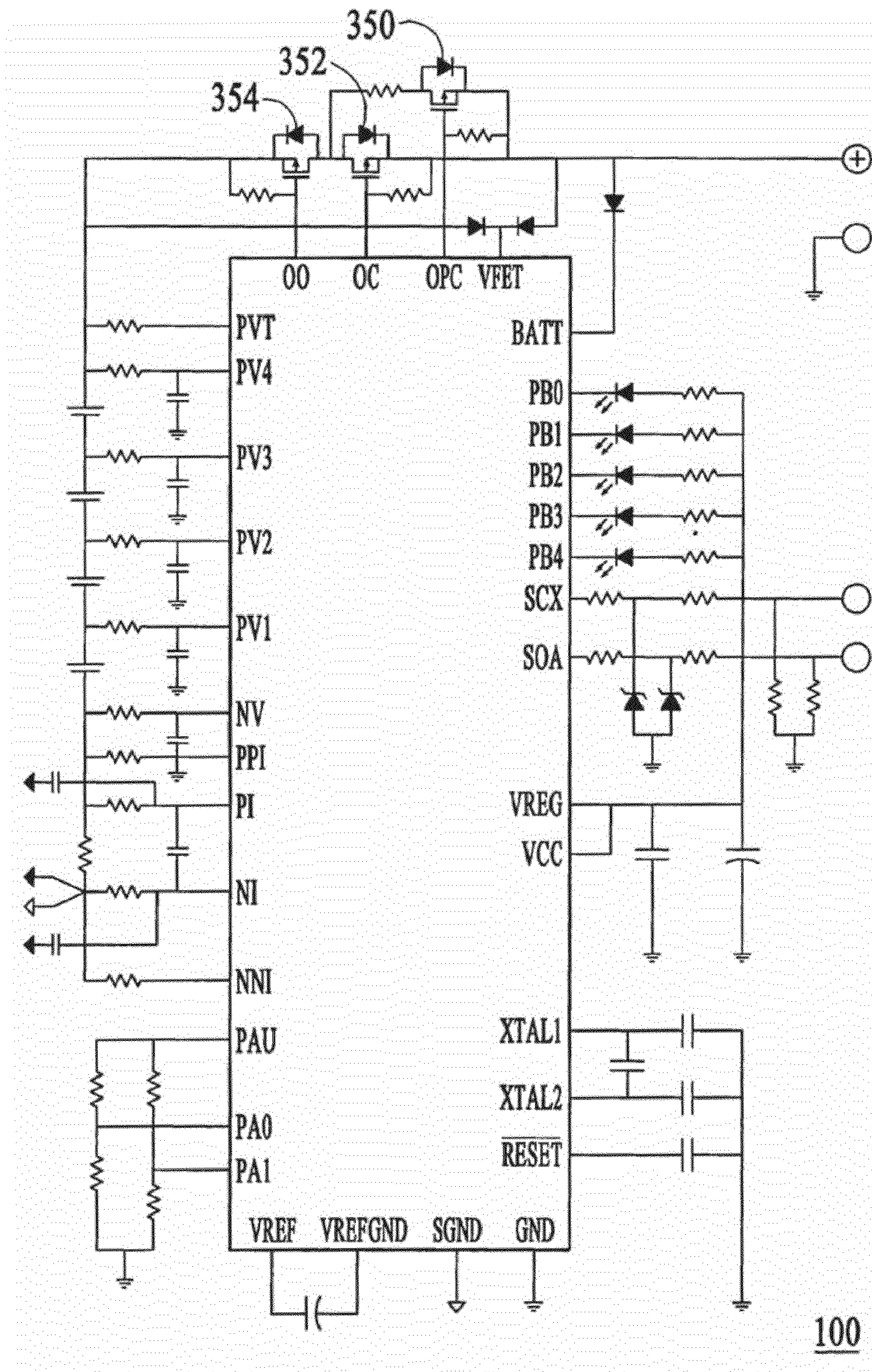


FIG. 3A

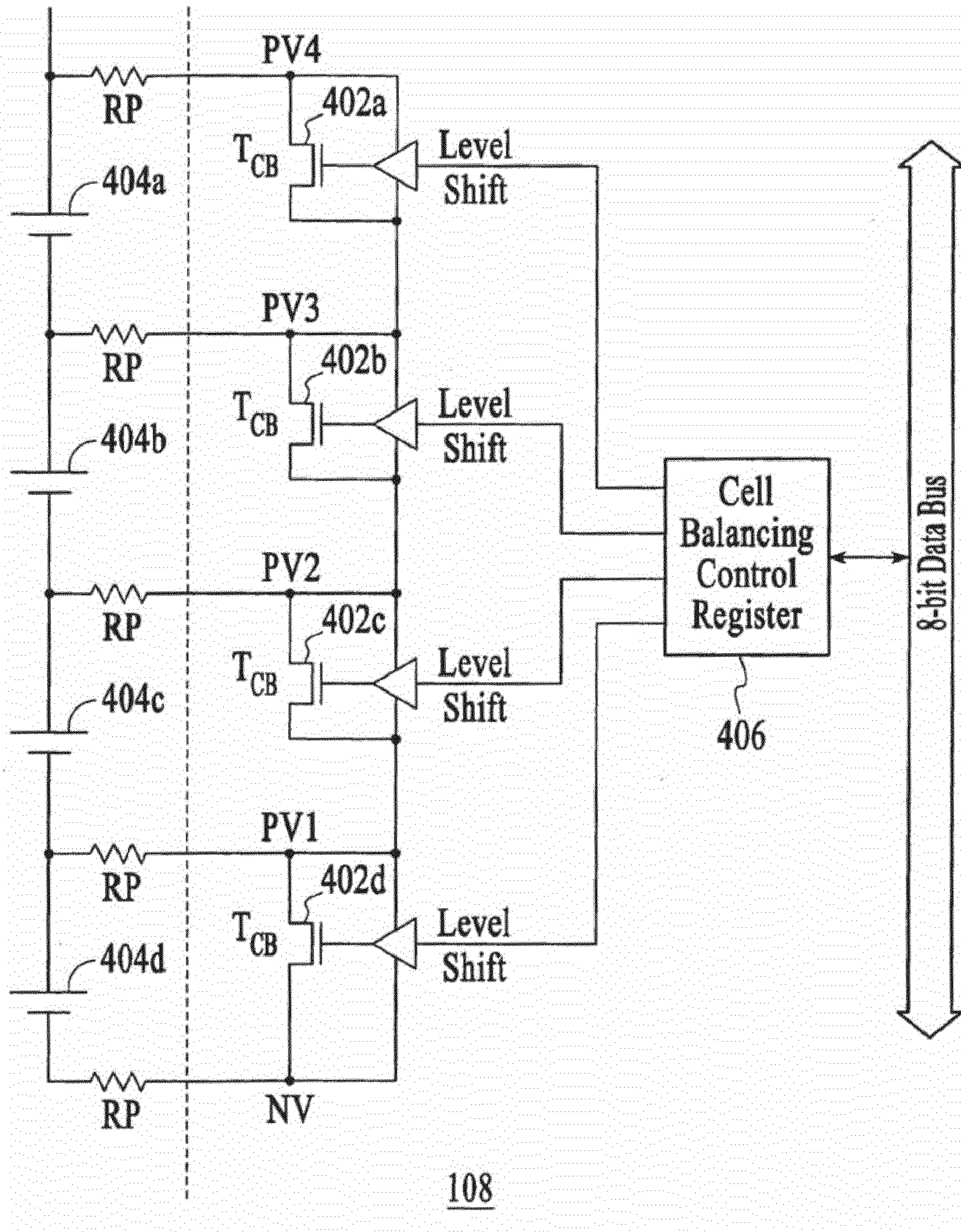


FIG. 4

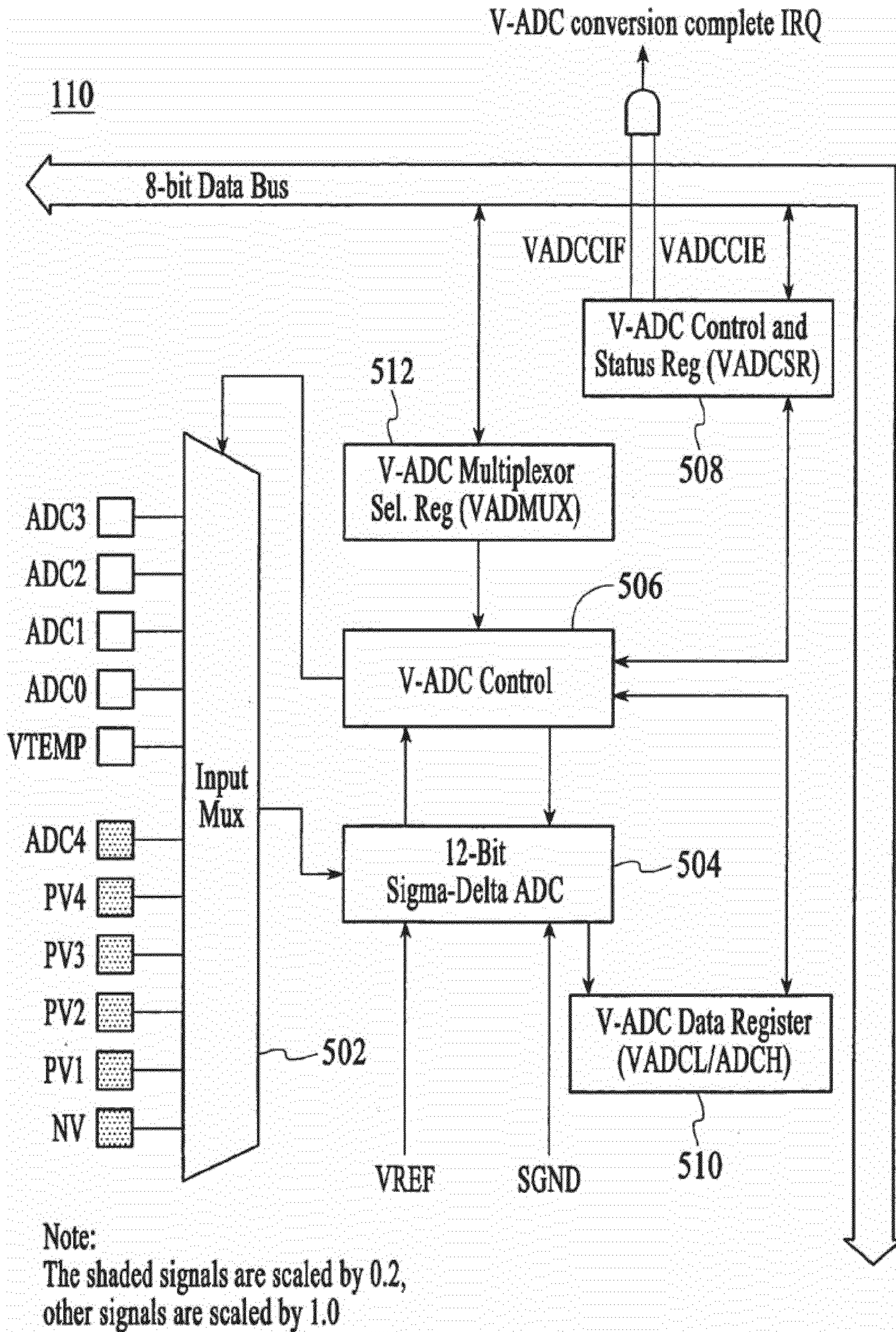


FIG. 5

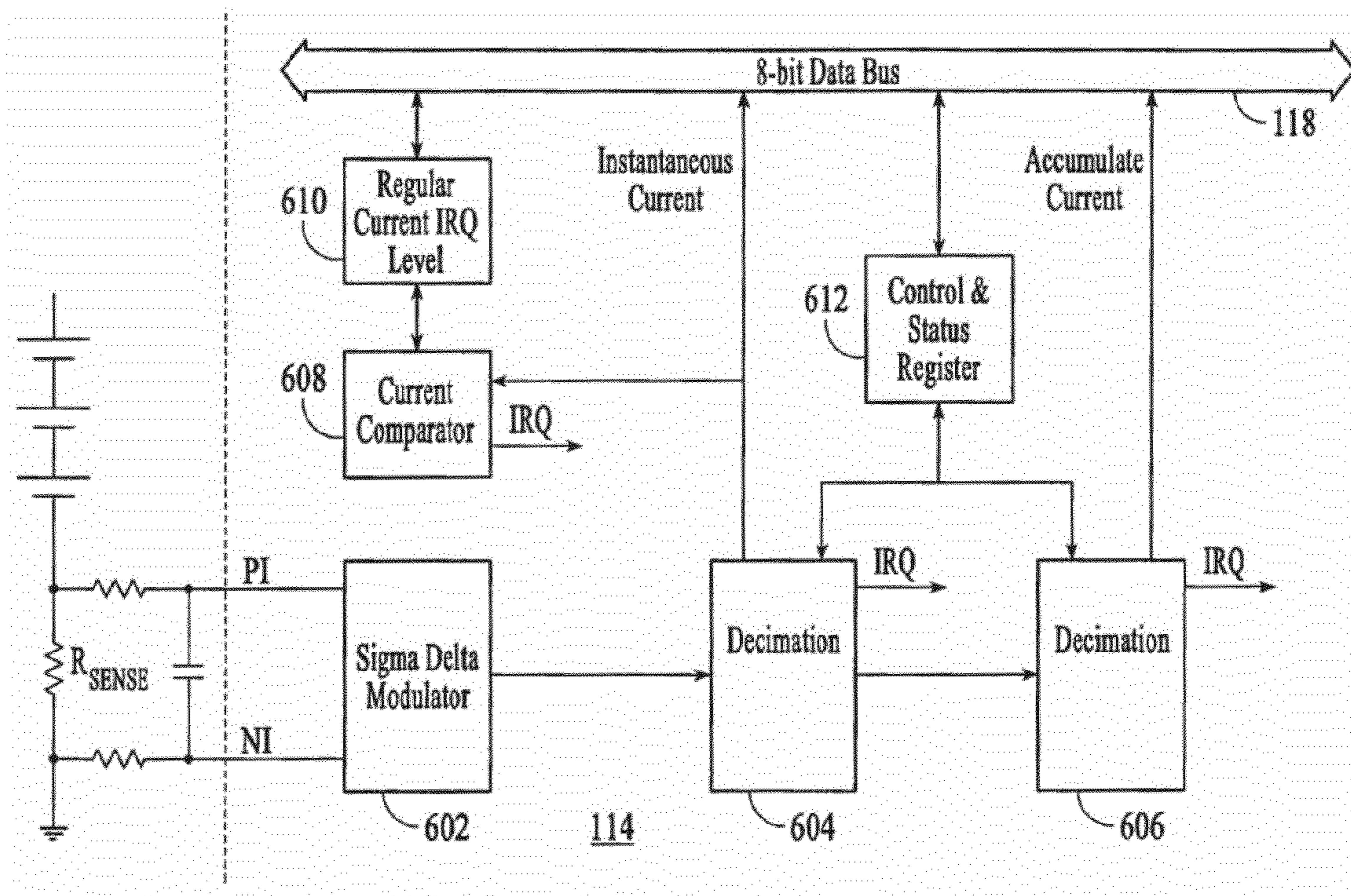


FIG. 6

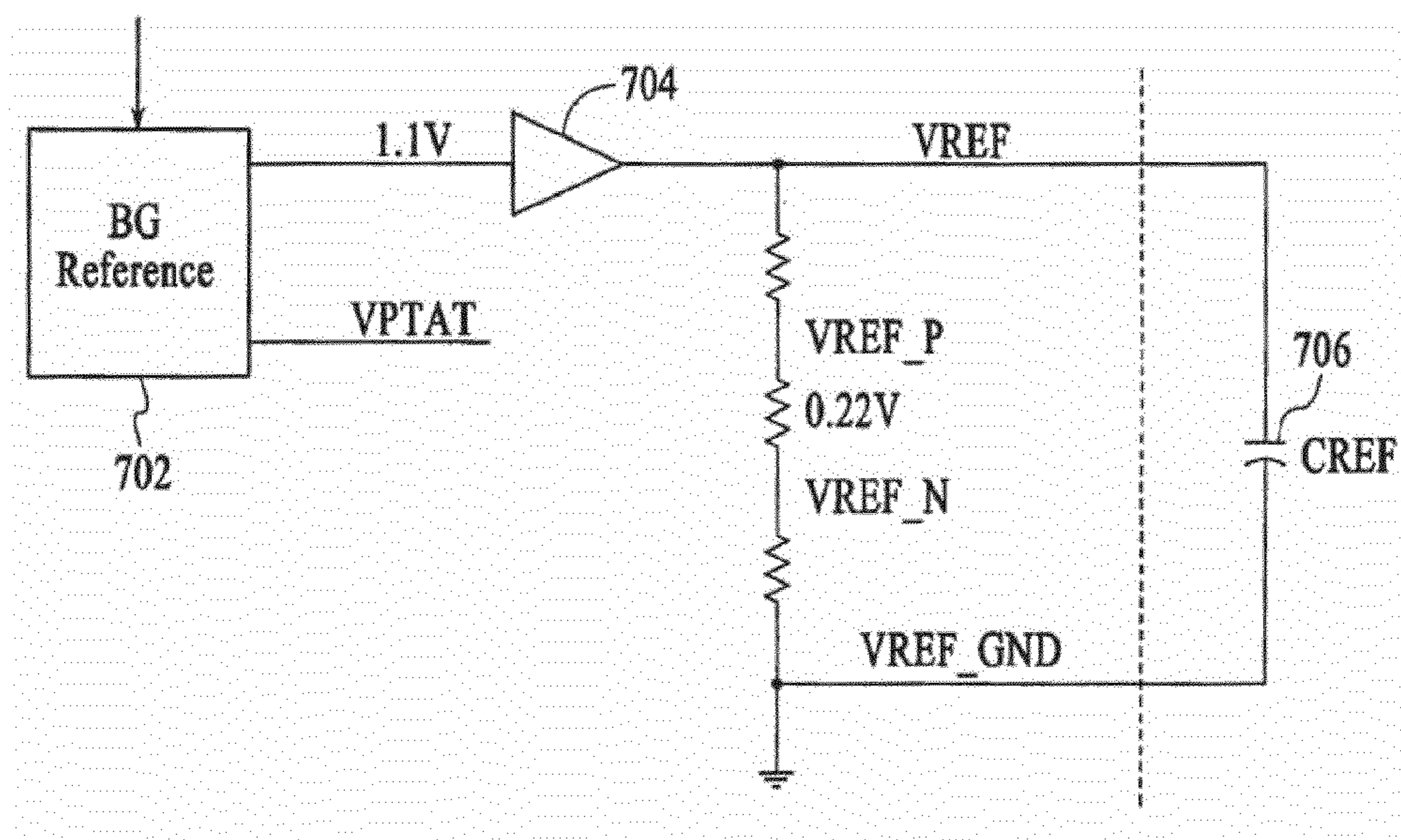


FIG. 7

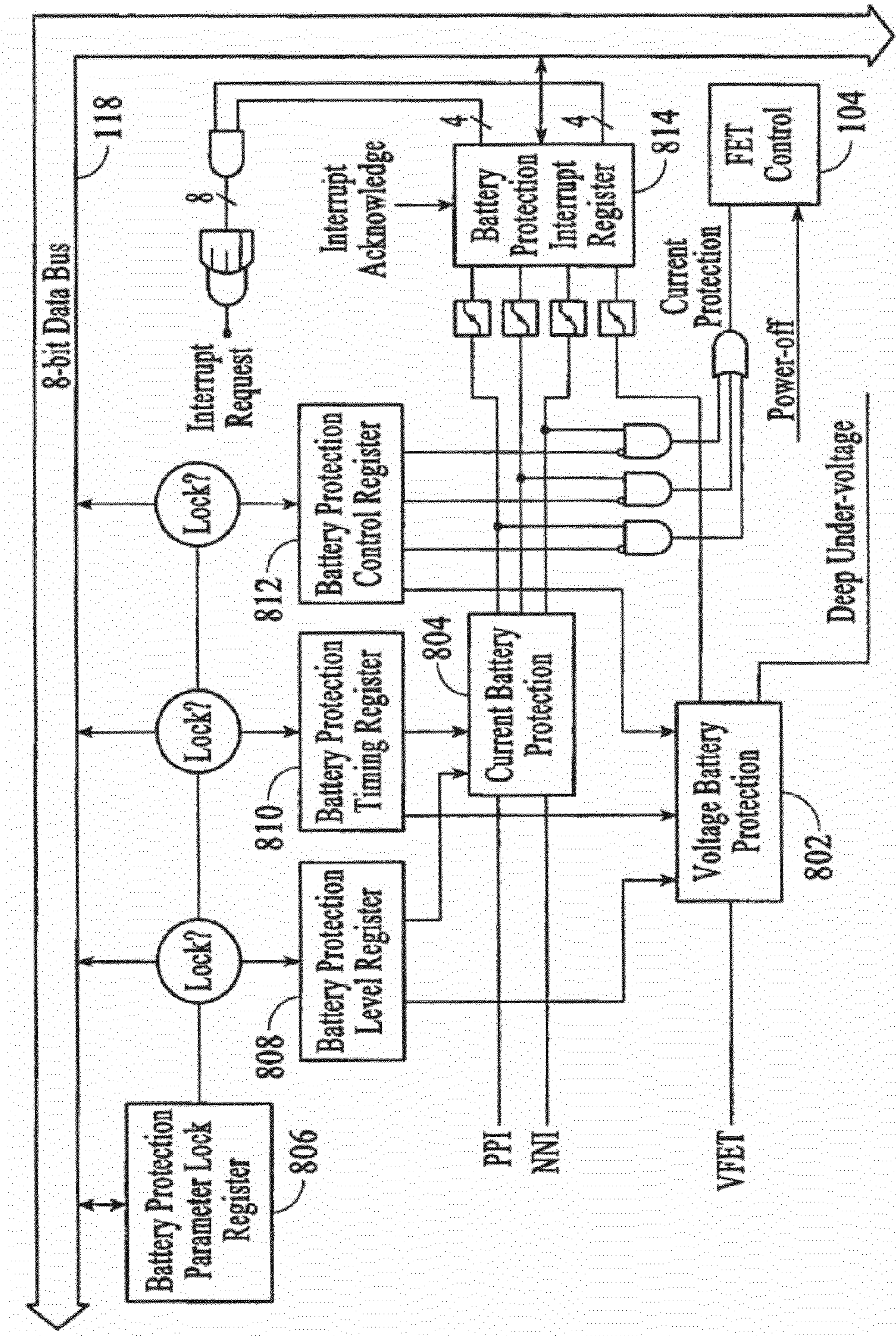


FIG. 8

1**SINGLE CHIP MICROCONTROLLER
INCLUDING BATTERY MANAGEMENT AND
PROTECTION**

RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/335,057, filed Jan. 18, 2006 now U.S. Pat. No. 7,759,902, which claims the benefit of U.S. Provisional Application No. 60/645,460, filed Jan. 19, 2005, which are incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

The present invention relates generally to a microcontroller and more specifically to a single chip microcontroller which includes a battery management and protection system.

BACKGROUND OF THE INVENTION

The demand for portable applications such as laptop PCs, cell phones, and digital cameras is ever-increasing. These applications keep getting smaller and more advanced with tougher price competition every day. No application component can escape these toughening requirements, and the vital application power source, the battery, is certainly no exception. Battery capacity development is lagging behind the increasing demands from the application and control of the chemical reaction inside the battery is subject to severe safety requirements, making it difficult to push the limits of the chemical technology. To make life even more difficult for battery vendors, the battery is. Expected to shrink in size and price along with the rest of the application.

Advanced battery packs, or smart batteries, contain a large amount of electronic components. This includes fail-safe circuitry to ensure that the battery cell is not damaged or dangerous to the user; monitoring capabilities and logic to interpret battery conditions and estimate charge left depending on battery load; and communication with the host application. Current smart battery applications are implemented using at least two integrated circuits: a microcontroller for battery management and an analog front-end to ensure battery protection and measurements. In addition, some require a third chip, an EEPROM containing data specific to the battery chemistry, necessary for charge left estimation and other monitoring parameters. These solutions are costly and take up board space.

In addition, rechargeable battery cells typically have a low current capability. For applications where high instant energy is needed, this problem is overcome by using many cells in series. This results in a higher voltage allowing a higher energy with a lower current. The higher voltage is a problem for standard semiconductors as these typically can handle voltages between 2-5 volts. Smart battery vendors solve the high voltage input/output problem by using separate driver circuits. This adds to the cost, weight, and complexity of the system.

Accordingly, what is needed is a system and method for overcoming the above-identified issues. The present invention addresses such a need.

SUMMARY OF THE INVENTION

A microcontroller is disclosed. The microcontroller comprises a processor system and a high voltage interface coupled to the processor system and adapted to be coupled to a battery. The microcontroller further includes a battery management

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system for monitoring the battery and managing the battery based upon the monitoring of the battery. The microcontroller is a single chip. This one-chip solution saves design cost and PCB space in addition to broadening the functionality of the smart battery application. With the accuracy of the microcontroller, the charge status of the battery can be predicted more accurately and therefore effectively increases actual battery capacity.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an embodiment of the microcontroller in accordance with the present invention.

FIG. 2 is a block diagram of an embodiment of a voltage regulator in accordance with the present invention.

FIG. 3 is a block diagram of one embodiment of an FET control system in accordance with the present invention.

FIG. 3A is a schematic diagram of an operating circuit utilizing the FET control system in accordance with the present invention.

FIG. 4 is one embodiment of a diagram of a cell balancing FETs in accordance with the present invention.

FIG. 5 is one embodiment of a voltage ADC in accordance with the present invention.

FIG. 6 is a block diagram of an embodiment of a CC-ADC.

FIG. 7 illustrates an embodiment of a low power band-gap voltage reference in accordance with the present invention.

FIG. 8 illustrates an embodiment of the battery protection CPU interface in accordance with the present invention.

DETAILED DESCRIPTION

The present invention relates generally to a microcontroller and more specifically to a single chip microcontroller which includes a battery management and protection system. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

A system and method in accordance with the present invention provides for a single chip device which includes battery management and protection. In a single die, the microcontroller includes a central processing unit and a voltage regulator capable of being powered directly from a multiple cell battery. The microcontroller also includes analog to digital converters tailored for battery monitoring, high voltage charge and discharge FET drivers, cell balancing capabilities, and independent battery protection circuitry. This one-chip solution saves design cost and PCB space in addition to broadening the functionality of the smart battery application. With the accuracy of the microcontroller, the charge status of the battery can be predicted more accurately. The more that is known about the charge status of the battery, the more the battery cell can be allowed to be depleted before reaching the level where the cell itself starts to be damaged. Accordingly, the actual capacity of the battery is increased.

The microcontroller features a high voltage input/output, which greatly helps reduce the total part count in the system. The microcontroller also includes an internal voltage regulator. The regulator enables operation of the microcontroller within a predetermined voltage range (i.e., from 4 volts to 25 volts). The analog to digital converter input channels can

measure battery cell voltages as high as 25 volts, eliminating an external high voltage analog front-end. The device also provides a plurality of internal FET drivers capable of computing 25V levels, so no external FET drivers are required.

The battery monitoring capabilities of the microcontroller are tailored to smart batteries. The battery monitoring capabilities include a voltage analog to digital converter that at 12 volts DC provides for ± 1 least significant (LSB) maximum error which provides good voltage measurements across the cells of the battery. A dedicated fuel gauging current sensing ADC provides continuous current monitoring at a high resolution (such as 18-bit resolution) and high accuracy. The high accuracy of the microcontroller battery monitoring is made possible by an on-chip voltage reference with $\pm 0.1\%$ error after calibration. An example of this type of calibration is described, for example, in U.S. application Ser. No. 10/795,027, entitled "Method and Apparatus of Temperature Compensation for an Integrated Circuit Chip Using On-Chip Sensor and Computation Means," filed on Mar. 4, 2004 and incorporated by reference in its entirety herein. The voltage and current measurements make it possible to estimate the charge left in the battery very accurately, allowing an application to draw more energy from the battery. It is known that a cell of the battery can be damaged if it is depleted below a certain voltage level. However, if this level is reliably known, it is safe to allow depletion very close to this level without risking cell damage. If the battery's state-of-charge is reliably known, it is possible to push the safe limit further towards depletion. With less refined measurement equipment, a guardband must be inserted into the estimate to ensure that the user will be able to shut down reliably. This guardband represents energy that could be used if the estimate really were to be trusted. A microcontroller in accordance with the present invention supplies the required accuracy to make use of this energy.

To describe the features of the present invention in more detail, refer now to the following discussion in conjunction with the accompanying figures. The present invention will be described in the context of a particular microcontroller; however, one of ordinary skill in the art recognizes that the features of the present invention could be utilized in a variety of devices and that use would be within the spirit and scope of the present invention. A device that incorporates the features of the present invention is a Smart Battery AVR (ATmega 406), manufactured by Atmel. The ATmega 406 is described in an ATmega 406 Preliminary Complete Document dated June 2005, which is incorporated by reference in its entirety herein.

FIG. 1 is a block diagram of an embodiment of the microcontroller **100** in accordance with the present invention. The microcontroller **100** in one embodiment includes the following elements: a processor, data bus **118**, in-system programmable Flash with read-while-write capabilities, an EEPROM **134**, an SRAM **132**, a plurality of general purpose working registers (not shown), a plurality of general purpose I/O lines (not shown), a plurality of high-voltage I/O lines (not shown), a JTAG interface **139** for on-chip debugging support and programming, two flexible timer/counters **147** and **148** with pulse width modulation and compare modes, a wake-up timer **136**, an SM-bus compliant two wire interface module **142**, internal and external interrupts, a programmable watchdog timer **124** with internal oscillator **122**, and four software selectable power saving modes. The microcontroller **100** also includes oscillator circuits/clock generation **120**, power supervision circuit **126**, and a charger detect circuit **128**. The data bus **118** is coupled to ports **138**, **140**, **144** and **142**.

The microcontroller **100** further includes a voltage regulator **102**, a FET control circuitry **104**, dedicated battery protection circuitry **106**, integrated cell balancing FETs **108**, high-voltage analog front-end, and two ADCs **110** and **114** with on-chip voltage reference **112** for battery fuel gauging.

In one embodiment, the CPU **116** combines a rich instruction set with the plurality of general purpose working registers. All of the registers are directly connected to the arithmetic logic unit (ALU) (not shown), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The idle mode stops the CPU **116** while allowing the other chip function to continue functioning. The power-down mode allows the voltage regulator **102**, battery protection circuitry **106**, watchdog timer **124**, and wake-up timer **136** to operate, while disabling all other chip functions until the next interrupt or hardware reset. In power-save mode, the wake-up timer **136**, battery protection circuitry **106** and the CC-ADC **114** continues to run.

The on-chip Flash memory **130** allows the program memory to be reprogrammed in-system, by a conventional non-volatile memory programmer or by an on-chip boot program running on the CPU **116**. A boot program can use any interface to download the application program in the Flash memory. Software in the boot Flash **130** will continue to run while the application Flash section is updated, providing true read-while-write operation. By combining the CPU **116** with the Flash memory **130**, ADCs **110** and **114**, dedicated battery protection circuitry **106**, cell balancing FETs **108**, and a voltage regulator **102** on a monolithic chip, the microcontroller **100** provides a highly flexible and cost effective solution for battery applications.

The voltage regulator **102** operates over a wide range of voltages, for example, 4.0-25 volts. This voltage is regulated to a constant supply voltage of nominally, for example, 3.3 volts for the integrated logic and analog functions.

The battery protection circuitry **106** monitors the battery voltage and charge/discharge current to detect illegal conditions and protect the battery from these when required. The illegal conditions are deep under-voltage during discharging, short-circuit during discharging and over-current during charging and discharging.

The integrated cell-balancing FETs **108** allow cell balancing algorithms to be implemented in software.

To describe the features of the microcontroller **100** in more detail, refer now to the following description in conjunction with the accompanying figures.

High Voltage I/O.

For battery monitoring and management devices several high voltage inputs and outputs are provided:

Input to voltage regulator. This input provides power to the device drawn directly from the battery, in the range of 4-25 volts.

Input to voltage ADC for individual cell voltage measurements.

Input to detect the presence of a battery charger.

High Voltage Open Drain Output (PCO).

Outputs to charge; discharge, and pre-charge FETs.

The high voltage technology makes it possible to integrate Flash program memory and logic as well as accurate analog circuitry on the same die as high-voltage tolerant I/O. The microcontroller **100** is high voltage (25 volts) tolerant, making it appropriate for multiple cell batteries.

Voltage Regulator 102

FIG. 2 is a block diagram of an embodiment of a voltage regulator 102 in accordance with the present invention. Modern semiconductors typically run at power supply in the range of 2 to 5 volts. A battery supplying up to 25 volts can thus not source the semiconductor directly. The microcontroller 100 is powered from the battery through the internal voltage regulator 102. The input to the regulator 102 is allowed to vary from 4 to 25 volts. This voltage is regulated down to 3.3 v internally, which is a suitable level for the internal logic, low voltage I/O lines, and analog circuitry.

To minimize power consumption during inactive periods, the voltage regulator optionally contains a power consumption control module 202. When the microcontroller 100 enters low power modes, the voltage regulator 102 will reduce the consumption in the regulator itself, further contributing to low power consumption. An external decoupling capacitor 206 of 1J-1F or larger is provided for operation of the voltage regulator 102.

Battery Management

A smart battery will not only monitor battery parameters, it will also manage the environment of the battery according to these parameters. The microcontroller 100 provides battery charging algorithms, cell balancing, and communication with the host application to manage and protect the battery pack. FET Control 104

FIG. 3 is a block diagram of one embodiment of an FET control 104 in accordance with the present invention. FIG. 3A is a schematic diagram of an operating circuit utilizing FED control system in accordance with the present invention. Referring to FIGS. 1, 3 and 3A together, in addition to the FET disable control signals from the battery protection circuitry 106, the CPU may disable the Charge FET (C-FET) 352, the Discharge FET (D-FET) 354, or both, by writing to the FET control and status register 302. Note that the CPU 116 is never allowed to enable a FET that is disabled by the battery protection circuitry 106.

The pulse width modulator (PWM) output from the 8-bit timer/counter 0, signal OC0B, can be configured to drive the C-FET 352 via FET driver 310, Precharge FET (PC-FET) driver 312 or both directly. This can be useful for controlling the charging of the battery cells. The PWM is configured by the 2:0 bits in the registers. Note that the OC0B pins do not need to be configured as an output. This means that the PWM output can be used to drive the C-FET 352 and/or the PC-FET 350 without occupying the OCOB-pin.

If C-FET 352 is disabled and D-FET 354 enabled, discharge current will run through the body-drain diode of the C-FET 352 and vice versa. To avoid the potential heat problem from this situation, software must ensure that D-FET 354 is not disabled when a charge current is flowing, and that C-FET 352 is not disabled when a discharge current is flowing.

If the battery has been deeply discharged, large surge currents may result when a charger is connected. In this case, it is recommended to first pre charge the battery through a current limiting resistor. For this purpose, the microcontroller 100 provides a Precharge FET 350 (PC-FET) control output. This output is default enabled.

If the microcontroller 100 has entered the power-off mode, all FET control outputs will be disabled. When a charger is connected, the CPU 116 will wake up. When waking up from power-off mode, the C-FET 352 and D-FET 354 control outputs will remain disabled while PC-FET 350 is default enabled. When the CPU 116 detects that the cell voltages have risen enough to allow normal charging, it should enable the C-FET 352 and D-FET 354 control outputs and disable the

PC-FET 350 control output. If the current battery protection (CBP) which will be described in detail hereinafter, has been activated, the current protection timer will ensure a hold-off time of 1 second before software can re-enable the external FETs.

Cell Balancing 108

FIG. 4 is one embodiment of a diagram of a cell balancing FETs 108 in accordance with the present invention. The microcontroller 100 incorporates cell-balancing FETs 402a-402d. The microcontroller 100 provides one cell balancing FET 402a-404d for each battery cell. The FETs 402a-402d are directly controlled by application software, allowing the cell balancing algorithms to be implemented in software. In one embodiment, the FETs 402a-404d are connected in parallel with the individual battery cells. The cell balancing FETs 402a-402d are disabled in the power-off mode.

Typical current through the cell balancing FETs 402a-402d (I_{CB}) is 2 mA. The cell balancing FETs 402a-402d are controlled by the cell balancing control register 406. In this embodiment, neighboring FETs cannot be simultaneously enabled. If trying to enable two neighboring FETs, both will be disabled.

SMBuS™ 118

In the PC battery pack application, SMBus (System Management Bus) is the standard for communication with the PC. The microcontroller 100 features a two-wire serial interface compatible with the SMBus standard.

Simple but powerful and flexible communication interface, only two bus lines needed

Both master and slave operation supported

Device can operate as transmitter or receiver

7-bit address space allows up to 128 different slave addresses

Multi-master arbitration support

Operates on 4 MHz clock, achieving up to 100 kHz data transfer speed

Slew-rate limited output drivers

Noise suppression circuitry rejects spikes on bus lines

Fully programmable slave address with general call support

Address recognition causes wake-up when the CPU is in sleep mode

The SMBus interface can be used to upgrade the program code using the CPU's self-programming capabilities.

Battery Parameters

As before described, the microcontroller 100 includes an EEPROM 134 for data storage. It is organized as a separate data space, in which single bytes can be read and written. This data space is intended for storage of key parameters vital to the battery application.

Voltage Measurements

Individual cell voltages within the battery require differential ADC measurements. To adjust the level of the measured cell voltage to that of the ADC, an internal gain is provided. Single-ended channels are utilized to measure other parameters such as the regulated voltage, and temperature at various locations inside the battery pack.

Voltage ADC 110

FIG. 5 is one embodiment of a voltage ADC 110 in accordance with the present invention. The V-ADC 110 of this embodiment comprises a plurality of differential channels, an input multiplexer 502 for receiving differential channels, a 12 bit sigma delta ADC 504, a V-ADC control system 506 for communicating with the input mux 502 and the sigma-delta ADC 504. V-ADC control and status register 508 receiving data from and providing data to the data bus 116. The V-ADC control and status register 508 also receives data from and

provides data to the V-ADC control **506**. The V-ADC **110** also includes a V-ADC data register **510** which receives data from the sigma-delta ADC **504** and provides data to the data bus **116**. The four differential channels for cell voltage measurements (PV1-NV, PV2-PV1, PV3-PV2, PV4-PV3) are scaled to comply with the full scale range of the V-ADC. In addition, there are six single ended channels referenced to signal ground. One channel is for measuring the internal die temperature sensor (VTEMP), four channels are for measuring the pins at port A for cell temperature monitoring (ADC3-ADC0) and one channel (ADC4) is for measuring the internal regulated voltage VREG. The ADC-4 input is also scaled to comply with the full scale range of the V-ADC.

To obtain accurate cell voltage measurements, calibration registers for the individual cell voltage gain in the analog front-end are provided. A factory calibration value is stored in the register, and a V-ADC conversion of a cell voltage is scaled with the corresponding calibration value to correct for gain error in the analog front-end. Typically this calibration occurs via software.

Counting Electrons

A PC battery pack is under constant abuse; it is constantly being depleted and then recharged at several levels of load. The smart battery is expected to tell how long it will be able to sustain the current load before it is depleted at any given time. In order to provide this service to the end user, the battery needs to know exactly how much energy has been drained from the battery so that this amount can be deducted from the full charge capacity of the pack. Once the remaining battery capacity is determined, a charge left algorithm can estimate the time left on the existing load. Calibration at various voltage points on the charge curve is not accurate enough; the smart battery has to actively log and count current charged into and discharged from the battery.

As before mentioned, the microcontroller **100** also includes a dedicated Coulomb counting analog-to-digital converter (CC-ADC) **114** optimized for Coulomb counting to sample the charge or discharge current flowing through the external sense resistor. This type of ADC is described in copending U.S. patent application Ser. No. 11/043,669 [3446P], entitled "Current Sensing Analog to Digital Converter and Method of Use," and assigned to the assignee of the present application.

FIG. 6 is a block diagram of an embodiment of a CC-ADC **114**. The CC-ADC **114** includes a sigma-delta modulator **602**, decimation filters **604** and **606**, a current comparator **608**, a regular current IRQ level **610**, a control and status register **612** and an 8-bit data bus **118**. The sigma-delta modulator **602** provides data to a decimation filter **604**. Decimation filter **604** provides data to decimation filter **606**, the current comparator **608** and the 8-bit databus **118**. The regular current IRQ level **610** receives data from the 8-bit databus **118** and provides data to the 8-bit databus **118** and the current comparator **608**. A control and status register **612** receives data from the 8-bit databus **118**, and provides data to decimation filters **604** and **606**. Decimation filter **606** receives data from the control and status register **612** and from decimation filter **604**, and provides data to the 8-bit databus **118**. Two different output values are provided: instantaneous current and accumulate current. The instantaneous current output has a short conversion time at the cost of lower resolution. The accumu-

late current output provides a highly accurate current measurement for Coulomb counting.

The accumulate current output is a high-resolution, high accuracy output with programmable conversion time. The converted value is an accurate measurement of the average current flow during one conversion period. The CC-ADC **114** generates an interrupt each time a new accumulate current conversion has finished if the interrupt is enabled.

While the CC-ADC **114** is converting, the CPU **116** can enter sleep mode and wait for an interrupt from the accumulate current conversion. After adding the new accumulate current value for Coulomb Counting, the CPU **116** can go back to sleep again. This reduces the CPU workload, and allows more time spent in low power modes, reducing power consumption.

The CC-ADC **114** can generate an interrupt if the result of an instantaneous current conversion is greater than a programmable threshold. This allows the detection of a regular current condition. This allows an ultra-low power operation, where the CC-ADC **114** can be configured to enter a regular current detection mode with a programmable current sampling interval. The CC-ADC **114** will repeatedly perform one instantaneous current conversion, before it is turned off for a timing interval specified by the user software. This allows operating the regular current detection while keeping the CC-ADC **114** off most of the time.

Internal Voltage Reference **112**

FIG. 7 illustrates an embodiment of a low power band-gap voltage reference **112** in accordance with the present invention. The low power band-gap voltage reference **112** provides the microcontroller with an accurate on-chip reference voltage (V_{REF}) of 1.100V. This V_{REF} is used as reference for the on-chip voltage regulator **102**, the V-ADC **110** and the CC-ADC **114** (FIG. 1). In a preferred embodiment, the reference to the two ADCs **110** and **114** uses a buffer **704** with external decoupling capacitor **706** to enable excellent noise performance with minimum power consumption. The reference voltage V_{REF_P}/V_{REF_N} to the CC-ADC **114** is scaled to match the full scale requirements at the current sense input pins. This configuration also enables concurrent operation of both V-ADC **110** and CC-ADC **114**.

To provide low temperature drift after factory calibration, the microcontroller **100** includes a two-step calibration algorithm. This algorithm is described, for example, in the before-mentioned U.S. application Ser. No. 10/795,027. The first predetermined temperature such as 85° and the second step is performed at a second predetermined temperature such as room temperature. By default, the factory calibration is 85°, and the result is stored in the Flash memory. The second calibration step can be implemented by a user as an instruction in their test flow. The step requires an accurate input voltage and a stable room temperature. The calibration register can also be altered runtime to implement temperature compensation in software. Accuracy for any temperature inside the temperature range can be achieved.

Also, in another embodiment the microcontroller **100** includes an on-chip temperature sensor (not shown) for monitoring the die temperature. A voltage proportional-to-absolute temperature, V_{PTAT} , is generated in the voltage reference circuit and connected to the multiplexer at the V-ADC input.

The temperature sensor can be used for runtime compensation of temperature drift in both the voltage reference and the on-chip oscillator **120**.

Battery Protection CPU Interface

FIG. **8** illustrates an embodiment of the battery protection CPU interface in accordance with the present invention. The battery protection CPU interface comprises current battery protection circuitry (CBPC) **804** and voltage battery protection circuitry (VBPC) **802**, and a plurality of battery protection parameter lockable registers **806**, **808**, **810**, **812** and **814**. The interface is coupled to the FET control **104** and the 8-bit data bus **118**.

Each protection has an interrupt flag. Each flag can be read and cleared by the CPU **116**, and each flag has an individual interrupt enable. All enabled flags are combined into a single battery protection interrupt request to the CPU **116**. This

level. The external filter at the PI/NI input pins will cause too large delay for short-circuit detection. Therefore the separate PPI/NNI inputs are used for current battery protection. There are two different programmable delays for activating current battery protection: short-circuit reaction time and over-current reaction time. After current battery protection has been activated, the application software must re-enable the FETs. In one embodiment, the battery protection circuitry **106** provides a hold-off time of, for example, one second before software can re-enable the discharge FET. This provides safety in case the application software should unintentionally re-enable the discharge FET too early.

The activation of a protection also issues an interrupt to the CPU **116**. The battery protection interrupts can be individually enabled and disabled by the CPU **116**.

The effect of the various battery protection types in this embodiment is provided in

TABLE 1

Table 1. Effect of Battery Protection Types						
Battery Protection Type	Interrupt Requests	C-FET	D-FET	PC-FET	Cell Balancing FETs	MCU
Deep under-voltage detected	CPU Reset on exit	Disabled	Disabled	Disabled	Disabled	Power-off
Discharge over-current protection	Entry and exit	Disabled	Disabled	Disabled	Operational	Operational
Charge over-current protection	Entry and exit	Disabled	Disable	Disabled	Operational	Operational
Short-circuit protection	Entry and exit	Disabled	Disabled	Disabled	Operational	Operational

interrupt can wake up the CPU **116** from any operation mode, except power-off. The interrupt flags are cleared by writing a logic '1' to their bit locations from the CPU **116**.

There are neither flags nor status bits indicating that the microcontroller **100** has entered the power off mode. This is because the CPU **116** is powered down in this mode. The CPU **116** will, however, be able to detect that it came from a power-off situation by monitoring CPU **116** reset flags when it resumes operation.

The over-current and short-circuit protection parameters are reprogrammable to adapt to different types of batteries. The parameters are set by writing to I/O registers. The parameter registers can be locked after the initial configuration, prohibiting any further updates until the next hardware reset. Secure Parameter Storage

In a preferred embodiment, the battery protection parameters set in the battery protection parameter registers and the disable function set in the battery protection disable register can be locked from any further software updates. Once locked, these registers cannot be accessed until the next hardware reset. This provides a safe method for protecting these registers from unintentional modification by software run-away. It is recommended that software sets these registers shortly after reset, and then protects these registers from any further updates.

The current battery protection circuitry (CBPC) **804** monitors the charge and discharge current and disables C-FET, PC-FET, and D-FET if an over-current or short-circuit condition is detected. There are three different programmable detection levels: discharge over-current detection level, charge over-current detection level and short-circuit detection

In order to reduce power consumption, both short-circuit and discharge over-current protection are automatically deactivated when the D-FET is disabled. The charge over-current protection is disabled when both the C-FET and the PC-FET are disabled. Note however that charge over-current protection is never automatically disabled when any of the C-FET or PC-FETs are controlled by PWM.

Each of these types of battery protections and their features are described in detail hereinbelow.

Deep Under-Voltage Protection

The deep under-voltage protection ensures that the battery cells will not be discharged deeper than the programmable deep under-voltage detection level. If the voltage at the VFET pin is below this level for a time longer than the programmable delay time, the FETs are automatically switched off and the microcontroller enters power-off mode. A deep under-voltage early warning interrupt flag (DUVIF) within the battery protection interrupt register will be set 250 ms before the microcontroller enters power-off. This will give the CPU **116** a chance to take necessary actions before the power is switched off.

The microcontroller **100** will remain in the power-off mode until a charger is connected. When a charger is detected, a normal power-up sequence is started and the microcontroller **100** initializes to default state.

The deep under-voltage delay time and deep under-voltage detection level are set in the battery protection deep under-voltage register (BPDUV) which is part of the battery protection level register. The parameter registers can be locked after the initial configuration, prohibiting any further updates until the next hardware reset.

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Discharge Over-Current Protection

The current battery protection current monitors the cell current by sampling the voltage at the PPI/NNI input pins. A differential operational amplifier amplifies the voltage with a suitable gain. The output from the operational amplifier is compared to an accurate, programmable on-chip voltage reference by an analog comparator. If the shunt resistor voltage is above the discharge over-current detection level for a time longer than over-current protection reaction time, the microcontroller **100** activates discharge over-current protection. A sampled system clocked by an internal ULP oscillator is used for over-current and short-circuit protection. This ensures a reliable clock source, off-set cancellation and low power consumption.

When the discharge over-current protection is activated, the external D-FET, PC-FET, and C-FET are disabled and a current protection timer is started. This timer ensures that the FETs are disabled for a predetermined period of time (i.e., one second). The application software must then set the DFE and CFE bits in the FET control and status register to re-enable normal operation when this is considered safe. If the D-FET is re-enabled while the loading of the battery still is too large, the discharge over-current protection will be activated again.

Charge Over-Current Protection

If the voltage at the PPI/NNI pins is above a charge over-current detection level for a time longer than over-current protection reaction time, the microcontroller **100** activates charge over-current protection.

When the charge over-current protection is activated, the external D-FET, PC-FET, and C-FET are disabled and a current protection timer is started. This timer ensures that the FETs are disabled for at least one second. The DFE and CFE bits in the FET control and status register **302** (FIG. 3) are set to re-enable normal operation when this is considered safe. If the C-FET is re-enabled and the charger continues to supply too high of a current, the charge over-current protection will be activated again.

Short-Circuit Protection

A second level of high current detection is provided to enable a faster response time to very large discharge currents. If a discharge current larger than the short-circuit detection level is present for a period longer than short-circuit reaction time, the short-circuit protection is activated.

When the short-circuit protection is activated, the D-FET, PC-FET, and C-FET are disabled and a current protection timer is started. This timer ensures that the D-FET, PC-FET, and C-FET are disabled for at least one second. The application software must then set the DFE and CFE bits in the FET control and status register **302** (FIG. 3) to re-enable normal operation when this is considered safe. If the D-FET is re-enabled before the cause of the short-circuit condition is removed, the short-circuit protection will be activated again.

Power Consumption

To avoid damaging the battery cells during long-term storage, it is important for the battery itself to consume as little power as possible. The single chip implementation helps reduce system power consumption by eliminating external components and collecting all functionality in one single package. In addition, the microcontroller **100** features various low-power modes called sleep modes. Sleep modes enable the application to shut down unused modules in the microcontroller **100**, thereby saving power. The microcontroller **100** provides four sleep modes allowing the user to tailor the power consumption to the application's requirement:

1. Idle mode, in which the CPU **116** is stopped but all peripheral functions continue operating.

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2. ADC noise reduction mode, which improves the noise environment for the ADC while saving power. If the V-ADC **110** (FIG. 1) is enabled, a conversion starts automatically once this mode is entered.

3. Power-save mode, in which a fast RC oscillator is stopped. Only the battery protection circuitry **106** and slow oscillators are kept running, as well as the CC-ADC **114** (FIG. 1) for current measurements.

4. Power-down mode, in which both the fast RC and slow RC clocks are halted. Battery protection, a watchdog timer **124** (FIG. 1) or external interrupt, or an SMBus address match can wake up the device.

5. Power-off mode enables the voltage regulator **102** (FIG. 1) to shut off power to the CPU **116**, leaving only the voltage regulator **102** and the charger detect circuitry **128** to be operational. In this mode the microcontroller **100** ensures that the battery cells are not damaged if the voltage is too low.

Table 2 shows key power consumption figures for one embodiment of the microcontroller **100**.

Condition	Current Draw
Active 1 MHz	1.2 mA
Idle 1 MHz	0.6 mA
Power-save	90 μ A
Power-down	20 μ A
Power-off	2 μ A

A system and method in accordance with the present invention provides for a microcontroller which includes battery management and protection. The microcontroller provides for a single chip device which includes battery protection and management. This one-chip solution saves design cost and PCB space in addition to broadening the functionality of the smart battery application. With the accuracy of the microcontroller, the charge status of the battery can be predicted more accurately and therefore effectively increases actual battery capacity.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

What is claimed is:

1. A battery controller comprising:

- a processor system including a data bus;
- a battery interface coupled to the processor system, wherein a battery to be coupled to the battery interface comprises a plurality of cells, wherein the battery interface includes a plurality of inputs to the battery controller capable of operating in a range of about 4 volts to about 25 volts; and
- a battery management system, including a plurality of cell-balancing field effect transistors coupled to the data bus, wherein a cell balancing field effect transistor is to be coupled to a cell of the plurality of cells, wherein the battery controller is a single integrated circuit chip.

2. The battery controller of claim 1, including a voltage regulator circuit coupled to the processor, wherein the battery interface includes an input to the voltage regulator circuit capable of operating in a range of about 4 volts to about 25 volts.

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3. The battery controller of claim 2, wherein the voltage regulator circuit includes a power consumption control module configured to:

detect when the battery controller enters a low power mode; and

place the voltage regulator circuit in a reduced power consumption mode when the low power mode of the battery controller is detected.

4. The battery controller of claim 1, including an analog-to-digital converter circuit coupled to the processor, wherein the battery interface includes an input to the analog-to-digital converter circuit capable of operating in a range of about 4 volts to about 25 volts.

5. The battery controller of claim 1, including a battery charger detect circuit coupled to the processor, wherein the battery interface includes an input to the battery charger detect circuit capable of operating in a range of about 4 volts to about 25 volts.

6. The battery controller of claim 1, wherein the battery interface includes an output from the battery controller capable of operating in a range of about 4 volts to about 25 volts.

7. The battery controller of claim 6, including a field effect transistor driver circuit coupled to the processor, wherein the battery interface includes an output from the field effect transistor driver circuit capable of operating in a range of about 4 volts to about 25 volts.

8. The battery controller of claim 7, wherein the field effect transistor driver circuit is configured to control a field effect transistor included in a battery charging circuit.

9. The battery controller of claim 7, wherein the field effect transistor driver circuit is configured to control a field effect transistor included in a battery discharging circuit.

10. The battery controller of claim 7, wherein the field effect transistor driver circuit is configured to control a field effect transistor included in a battery pre-charging circuit.

11. The battery controller of claim 7, wherein the field effect transistor driver circuit includes a pulse width modulation circuit.

12. The battery controller of claim 1, wherein each cell balancing field effect transistor of the plurality of cell-balancing field effect transistors is directly controlled by reprogrammable application software via a control register coupled to the data bus.

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13. A monolithic integrated circuit chip comprising:

a processor system including a data bus;

a battery interface coupled to the processor system, wherein a battery to be coupled to the battery interface comprises a plurality of cells, wherein the battery interface includes a plurality of inputs to the monolithic integrated circuit chip that are capable of operating in a range of about 4 volts to about 25 volts; and

a battery management system, including a plurality of cell-balancing field effect transistors coupled to the data bus, wherein a cell balancing field effect transistor is to be coupled to a cell of the plurality of cells.

14. The integrated circuit chip of claim 1, including a voltage regulator circuit coupled to the processor, wherein the battery interface includes an input to the voltage regulator circuit capable of operating in a range of about 4 volts to about 25 volts.

15. The integrated circuit chip of claim 1, including an analog-to-digital converter circuit coupled to the processor, wherein the battery interface includes an input to the analog-to-digital converter circuit capable of operating in a range of about 4 volts to about 25 volts.

16. The integrated circuit chip of claim 1, including a battery charger detect circuit coupled to the processor, wherein the battery interface includes an input to the battery charger detect circuit capable of operating in a range of about 4 volts to about 25 volts.

17. The integrated circuit chip of claim 1, wherein the battery interface includes an output from the integrated circuit chip capable of operating in a range of about 4 volts to about 25 volts.

18. The integrated circuit chip of claim 17, including a field effect transistor driver circuit coupled to the processor, wherein the battery interface includes an output from the field effect transistor driver circuit capable of operating in a range of about 4 volts to about 25 volts.

19. The integrated circuit chip of claim 18, wherein the field effect transistor driver circuit is configured to control a field effect transistor included in a battery charging circuit.

20. The integrated circuit chip of claim 18, wherein the field effect transistor driver circuit is configured to control a field effect transistor included in a battery discharging circuit.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 8,143,860 B2
APPLICATION NO. : 12/839249
DATED : March 27, 2012
INVENTOR(S) : Gunnar Gangstoe, Arne Aas and Runa Sorasen

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, Line 32 in the Specification, delete “is. Expected” and insert -- is expected --.

Column 3, Line 8 in the Specification, delete “+1” and insert -- ±1 --.

Column 3, Line 14 in the Specification, delete “+0.1” and insert -- ±0.1 --.

Column 4, Line 62 in the Specification, delete “charge;” and insert -- charge, --.

Column 5, Line 18 in the Specification, delete “IJ-IF” and insert -- 1μF --.

Column 5, Line 46 in the Specification, delete “OCOB” and insert -- OC0B --.

Column 5, Line 49 in the Specification, delete “C-FE T” and insert -- CFET --.

Column 6, Line 23 in the Specification, delete “SMBuS™” and insert -- SMBus™” --.

Column 8, Line 42 in the Specification, delete “ V_{REF_P}/V_{REF_N} ” and insert
-- V_{REF_P}/V_{REF_N} --.

Column 10, Line 18 in the Specification, after “in” delete “TABLE 1” and insert
-- Table 1. --.

Column 10, Table 1, Line 10 in the Specification, delete “Disable” and insert
-- Disabled --.

Column 11, Line 47 in the Specification, delete “PCFET” and insert -- PC-FET --.

Signed and Sealed this
Fourth Day of September, 2012



David J. Kappos
Director of the United States Patent and Trademark Office

CERTIFICATE OF CORRECTION (continued)
U.S. Pat. No. 8,143,860 B2

In the Claims:

In column 14, claim 14, line 13, delete "1," and insert -- 13, --.

In column 14, claim 15, line 18, delete "1," and insert -- 13, --.

In column 14, claim 16, line 23, delete "1," and insert -- 13, --.

In column 14, claim 17, line 28, delete "1," and insert -- 13, --.