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(54) **SEMICONDUCTOR DEVICE AND MEMORY**

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G11C 11/34 (2006.01)

(52) **U.S. Cl.** **365/177**; 365/185.18; 257/288

(58) **Field of Classification Search** 365/177, 365/185.18; 257/288

See application file for complete search history.

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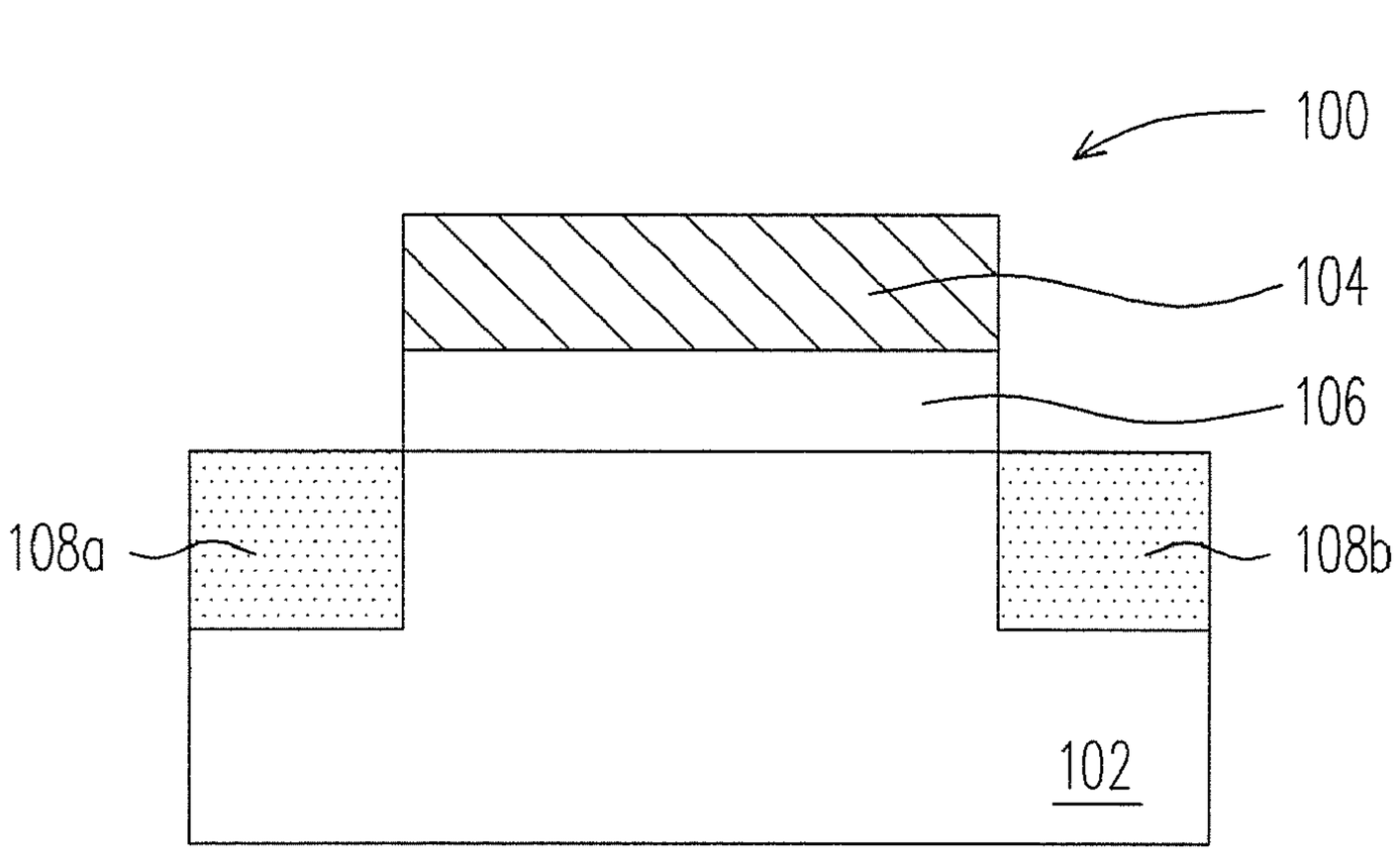
(57) **ABSTRACT**

A memory applicable to an embedded memory is provided. The memory includes a substrate, a gate, a charge-trapping gate dielectric layer, a source, and a drain. The gate is disposed above the substrate. The charge-trapping gate dielectric layer is disposed between the gate and the substrate. The source and the drain are disposed in the substrate beside the gate respectively.

8 Claims, 3 Drawing Sheets



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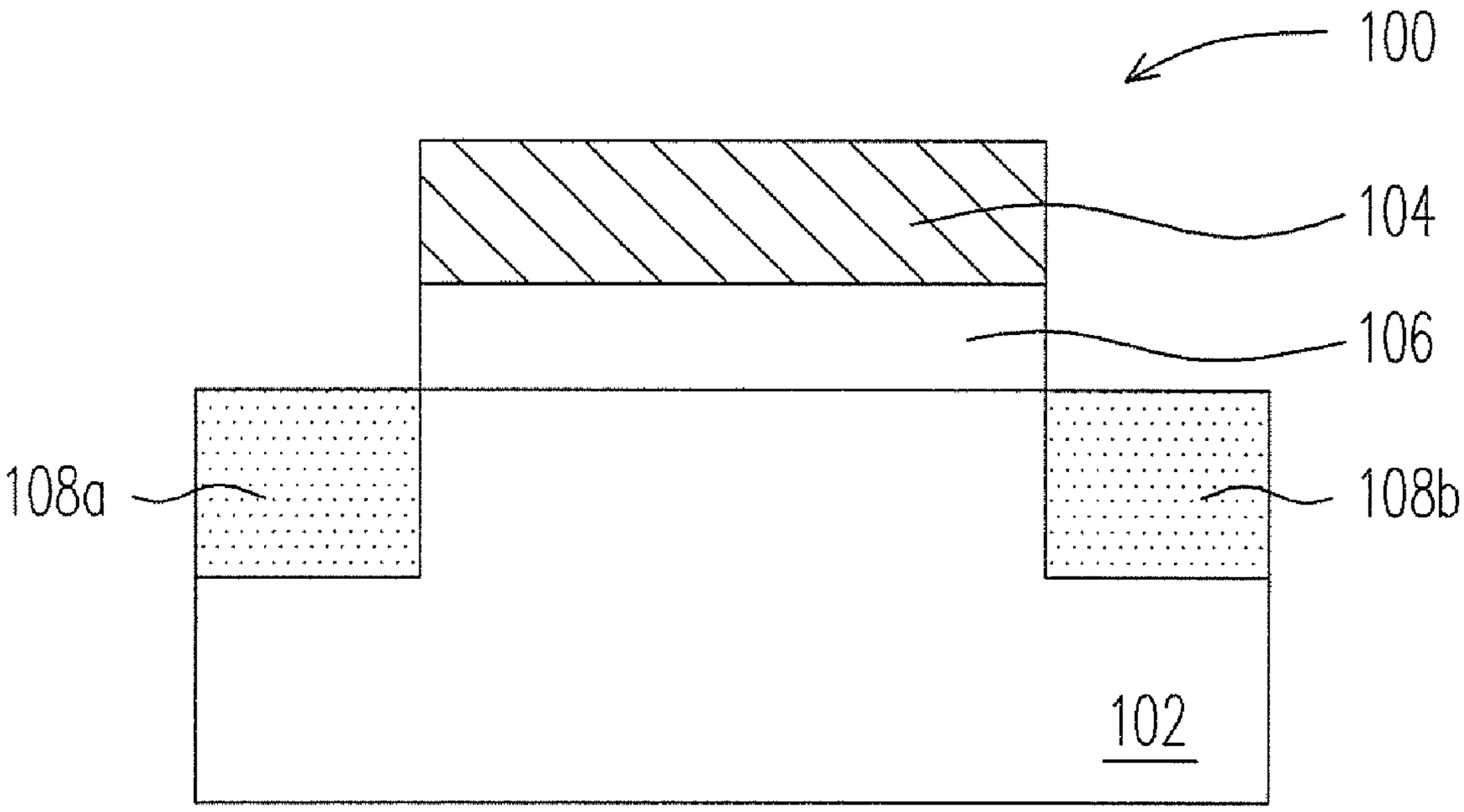


FIG. 1

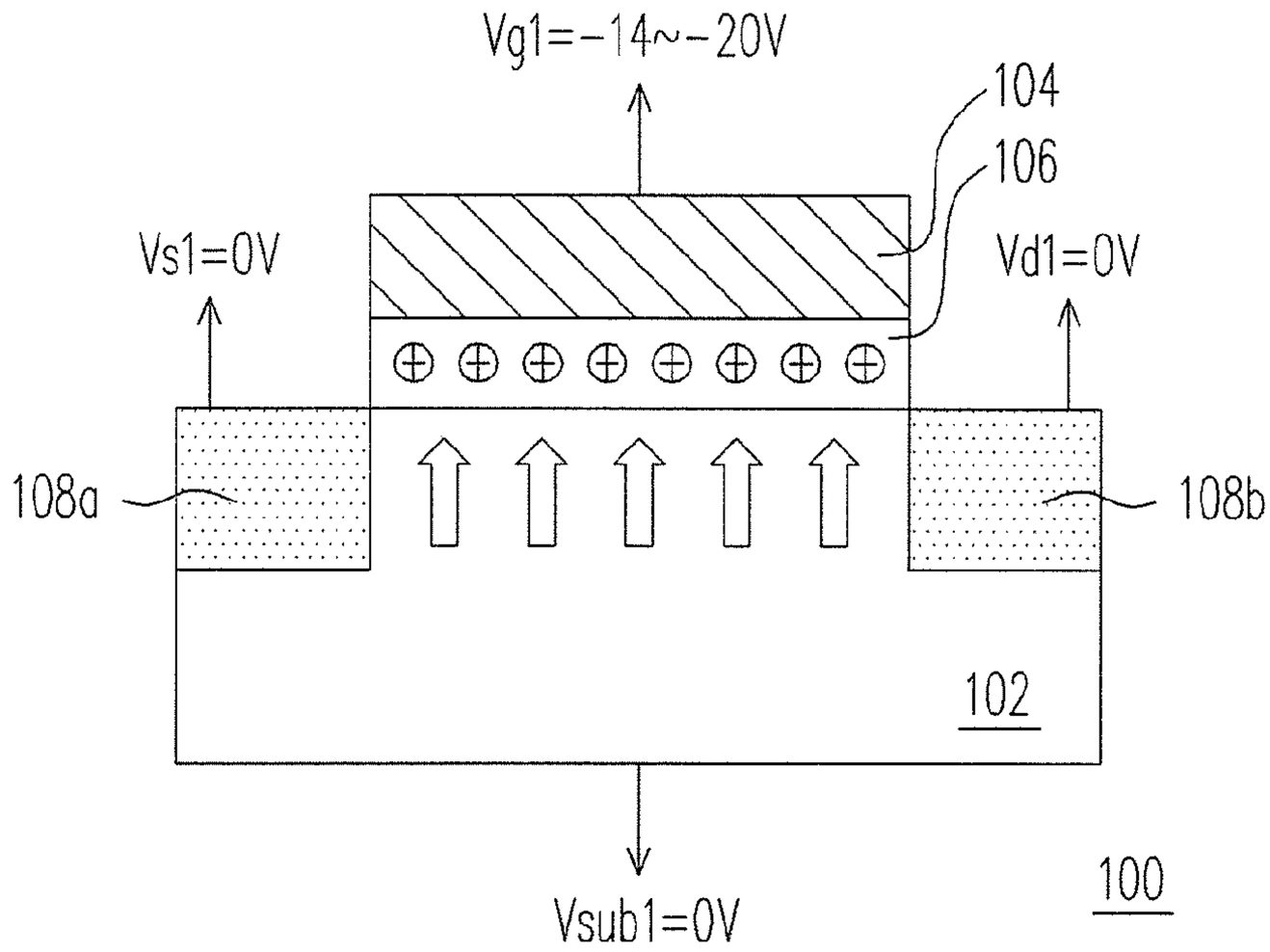
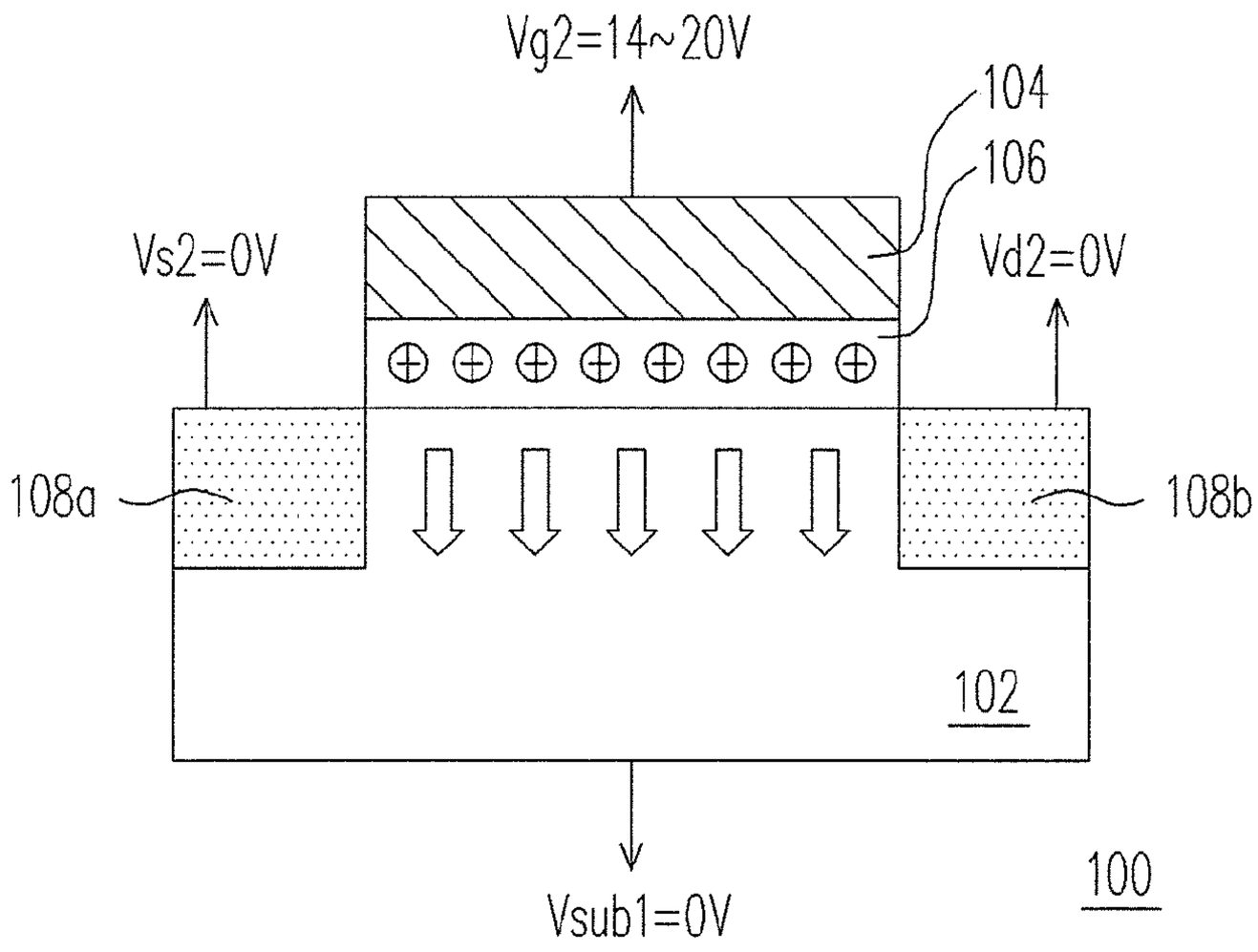

Vg1=−14~−20V
104
106
Vs1=0V
Vd1=0V
108a
108b
102
100
Vsub1=0V

FIG. 2A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104
106
Vs2=0V
Vd2=0V
108a
108b
102
100
Vsub1=0V

FIG. 2B

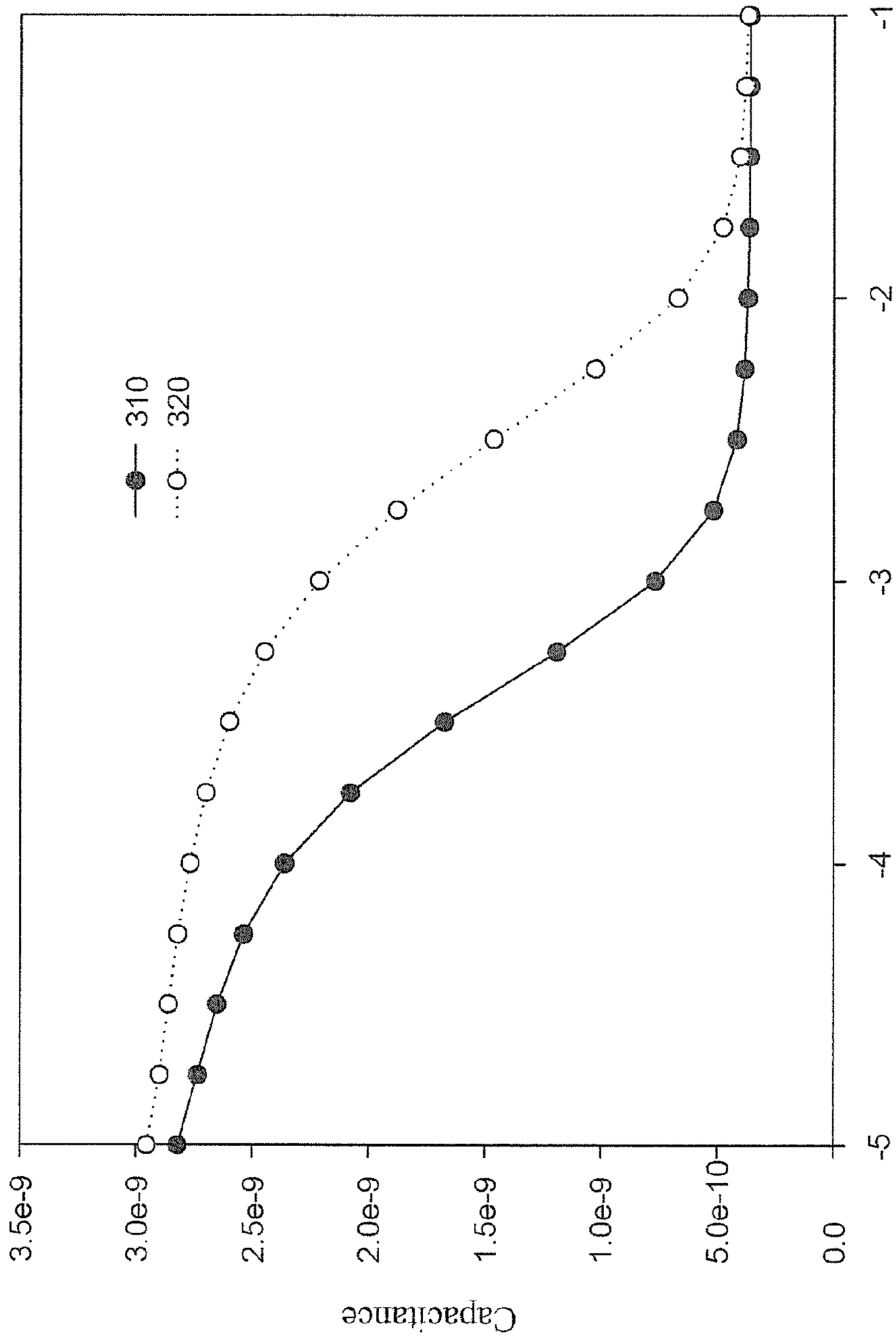
Capacitance
3.5e-9
3.0e-9
2.5e-9
2.0e-9
1.5e-9
1.0e-9
5.0e-10
0.0
-5
-4
-3
-2
-1
Voltage
310
320

FIG. 3

SEMICONDUCTOR DEVICE AND MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional application of and claims the priority benefit of application Ser. No. 11/670,600, filed on Feb. 2, 2007, now U.S. Pat. No. 7,652,923. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The embodiments of the invention relates to an integrated circuit. More particularly, the embodiments of the invention relates to a semiconductor device and a method of operating thereof.

2. Description of Related Art

Among various types of semiconductor devices, memories in which data can be stored, read out or erased and having the advantage that the data stored therein can be retained even after power is cut off has become a memory device widely applied in personal computers and electronic apparatuses.

Generally speaking, in order to reduce the manufacturing cost of the semiconductor device and simplify the process, it gradually becomes a trend to integrate elements of a memory and a logic circuit on the same system, which is also known as an embedded memory. To be specific, in a conventional embedded memory structure, the transistor used as the memory and the transistor used as the logic device are formed on the same system.

However, for the conventional embedded memory, the processes of fabricating the transistor in the memory region and the logic circuit region are two different transistor processes. Since the transistor used as the memory has two poly-Si layers to serve as a control gate and a floating gate, and the transistor used as the logic device has only one poly-Si layer to serve as a gate, the two transistors have different structures. Moreover, the transistor used as the memory and the transistor used as the logic device have different requirements on characteristics. Therefore, the process of manufacturing the embedded memory becomes difficult, thereby influencing the process yield.

SUMMARY OF THE INVENTION

The embodiments of the invention are directed to providing a semiconductor device. On the same system, a metal oxide semiconductor transistor and a memory in the semiconductor device are simultaneously forming. The process of manufacturing the semiconductor device becomes easy, thereby improving the process yield.

The embodiments of the invention are directed to providing a memory and an operating method thereof. The memory is applicable to an embedded memory, and has the function of storing data.

The embodiments of the invention provide a semiconductor device. The semiconductor device comprises a substrate, a metal oxide semiconductor transistor and a memory. The substrate has a logic circuit region and a memory region. The metal oxide semiconductor transistor is disposed in the logic circuit region, and the metal oxide semiconductor transistor comprising a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a gate dielectric layer disposed between the gate and the substrate. The memory is disposed in the memory region, the memory and the metal oxide semiconductor transistor are the same stacked structure having the same material, and the memory comprising a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a charge-trapping gate dielectric layer disposed between the gate and the substrate.

In the memory according to an embodiment of the invention, the thickness of the charge-trapping gate dielectric layer is between 20 Å and 200 Å. The charge-trapping gate dielectric layer comprises a doped silicon oxide layer, a nitrided silicon dioxide layer, a deposited silicon oxide layer, a silicon oxynitride layer, or a silicon nitride layer.

In the memory according to an embodiment of the invention, the gate comprises an N-type doped polysilicon layer or a P-type doped polysilicon layer. In addition, the gate is a metal gate.

In the memory according to an embodiment of the invention, the source and the drain are the same, which comprises an N-type doped region or a P-type doped region.

In the memory according to an embodiment of the invention, the memory is a one time programmable memory or an erasable/programmable memory.

The embodiments of the invention further provide a memory applicable to an embedded memory. The memory comprises a substrate, a gate, a charge-trapping gate dielectric layer, a source, and a drain. The gate is disposed above the substrate. The charge-trapping gate dielectric layer is disposed between the gate and the substrate. The source and the drain are disposed in the substrate beside the gate respectively.

In the memory according to an embodiment of the invention, the thickness of the charge-trapping gate dielectric layer is between 20 Å and 200 Å. The charge-trapping gate dielectric layer comprises a doped silicon oxide layer, a nitrided silicon dioxide layer, a deposited silicon oxide layer, a silicon oxynitride layer, or a silicon nitride layer.

In the memory according to an embodiment of the invention, the gate comprises an N-type doped polysilicon layer or a P-type doped polysilicon layer. In addition, the gate is a metal gate.

In the memory according to an embodiment of the invention, the source and the drain are the same, which comprises an N-type doped region or a P-type doped region.

In the memory according to an embodiment of the invention, the memory is a one time programmable memory or an erasable/programmable memory.

The embodiments of the invention further provide a method of operating a memory. The memory comprises a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a charge-trapping gate dielectric layer disposed between the gate and the substrate. The method of operating the invention comprises performing an erasing operation so as to inject holes into the charge-trapping gate dielectric layer to erase the memory, and performing a programming operation so as to pull the holes from the charge-trapping gate dielectric layer to the substrate to program the memory. The erase operation comprises applying a first gate voltage on the gate, applying a first drain voltage on the drain, applying a first source voltage on the source, and applying a first substrate voltage on the substrate. The program operation comprises applying a second gate voltage on the gate, applying a second drain voltage on the drain, applying a second source voltage on the source, and applying a second substrate voltage on the substrate.

In the method of operating a memory according to an embodiment of the invention, the first gate voltage is between −14 V and −20 V. The second gate voltage is between 14 V and 20 V. The first drain voltage, the first source voltage, and the first substrate voltage are 0 V. The second drain voltage, the second source voltage, and the second substrate voltage are 0 V.

In the method of operating a memory according to an embodiment of the invention, the thickness of the charge-trapping gate dielectric layer is between 20 Å and 200 Å. The charge-trapping gate dielectric layer comprises a doped silicon oxide layer, a nitrided silicon dioxide layer, a deposited silicon oxide layer, a silicon oxynitride layer, or a silicon nitride layer.

In the method of operating a memory according to an embodiment of the invention, the gate comprises an N-type doped polysilicon layer or a P-type doped polysilicon layer. In addition, the gate is a metal gate.

In the method of operating a memory according to an embodiment of the invention, the source and the drain are the same, which comprises an N-type doped region or a P-type doped region.

In the method of operating a memory according to an embodiment of the invention, the memory is a one time programmable memory or an erasable/programmable memory.

In the embodiments of the invention, the charge-trapping gate dielectric layer disposed between the gate and the substrate of the memory is used as a charge-trapping layer of the memory, such that the memory has the function of storing the data. On the other hand, the structure of the memory in the invention is similar to that of the transistor of a common logic device, and thus it can be applied into an embedded memory. In other words, on the same system a transistor of a logic device and a memory in the invention can be simultaneously forming, thereby increasing the process yield and simplifying the process.

In order to make the aforementioned and other objects, features and advantages of the invention comprehensible, embodiments accompanied with figures are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the embodiments of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the embodiments of the invention.

FIG. **1** is a schematic sectional view of a memory according to an embodiment of the invention.

FIG. **2**A is a schematic view of the erasing operation of the memory according to the invention.

FIG. **2**B is a schematic view of the programming operation of the memory according to the invention.

FIG. **3** is a capacitance-voltage relation diagram when operating the memory according to the invention.

DESCRIPTION OF EMBODIMENTS

Reference will now be made in detail to the embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

In integrated circuit of prior art, the elements of a memory and a logic circuit are integrated on the same system. And, the manufacturing process becomes difficult, thereby influencing the process yield. Therefore, a semiconductor device is provided to solve the above mentioned issues. The semiconductor device comprises a metal oxide semiconductor transistor disposed in the logic circuit region and a memory disposed in the memory region. The metal oxide semiconductor transistor comprising a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a gate dielectric layer disposed between the gate and the substrate. The memory comprising a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a charge-trapping gate dielectric layer disposed between the gate and the substrate.

In particular, the memory and the metal oxide semiconductor transistor are the same stacked structure having the same material so as to the process of manufacturing the semiconductor device in the invention becomes easy, thereby increasing the process yield.

Moreover, the metal oxide semiconductor transistor of the invention is a common metal oxide semiconductor transistor and that is all known to those skilled in the art, and will not be described herein. The memory in the semiconductor device of the invention is shown by using FIG. **1**.

FIG. **1** is a schematic sectional view of a memory according to an embodiment of the invention.

Referring to FIG. **1**, the memory **100** in this embodiment includes a substrate **102**, a gate **104**, a charge-trapping gate dielectric layer **106**, a source **108***a*, and a drain **108***b*. The substrate **102** is, for example, a P-type silicon substrate. The gate **104** is disposed above the substrate **102**. The gate **104** is, for example, an N-type doped polysilicon layer or a P-type doped polysilicon layer. In addition, the gate **104** is further, for example, a metal gate, and the material thereof is, for example, metal, metal alloy or metal silicide used by a common metal gate. The source **108***a* and the drain **108***b* are disposed in the substrate **102** beside the gate **104** respectively. The source **108***a* and the drain **108***b* are, for example, N-type doped regions.

In another embodiment, the substrate **102** of the memory **100** is, for example, an N-type silicon substrate, and the source **108***a* and the drain **108***b* are, for example, P-type doped regions.

The charge-trapping gate dielectric layer **106** of this embodiment is disposed between the gate **104** and the substrate **102**. The thickness of the charge-trapping gate dielectric layer **106** is between 20 Å and 200 Å, and preferably around 90 Å. Films having lower purity are using in the charge-trapping gate dielectric layer **106** so that the charge-trapping gate dielectric layer **106** has the function of trapping charges. In addition, the charge-trapping gate dielectric layer **106** is, for example, a doped silicon oxide layer, a nitrided silicon dioxide layer, or a deposited silicon oxide layer. That is, the charge-trapping gate dielectric layer **106** is, for example, a silicon oxide layer formed by ion implantation, nitridation, or deposition. The deposition is, for example, chemical vapor deposition (CVD). In addition, the charge-trapping gate dielectric layer **106** is, for example, a silicon oxynitride layer or a silicon nitride layer.

It should be noted that the memory **100** in this embodiment uses the charge-trapping gate dielectric layer **106** as a charge-trapping layer of the memory **100**, such that the memory has the function of storing data. On the other hand, the transistor of a common logic device includes a silicon oxide layer formed by thermal oxidation and disposed between the substrate and the gate, and the memory **100** of this embodiment includes a charge-trapping gate dielectric layer **106** disposed

between the gate **104** and the substrate **102**. It can be known that the structure of the memory **100** of this embodiment is similar to that of the transistor of the common logic device. Therefore, the memory **100** of this embodiment can be applied into an embedded memory. In other words, on the same system a transistor of a logic device and a memory in the invention can be simultaneously forming, thereby increasing the process yield and simplifying the process.

Moreover, the memory in the embodiments of the invention can be used as a one time programmable memory. In addition, the memory of the invention can also be sued as an erasable/programmable memory.

The operating method of a memory of the embodiments of the invention is illustrated by using the memory **100** of the above embodiment. The operating method of a memory of the embodiments of the invention includes performing an erasing operation (as shown in FIG. **2**A), and performing a programming operation (as shown in FIG. **2**B).

First, referring to FIG. **2**A, a schematic view of the erasing operation of the memory according to the embodiments of the invention is shown. When performing the erasing operation to the memory **100**, a first gate voltage Vg**1** is applied on the gate **104**, and the first gate voltage Vg**1** is, for example, between −14 V and −20 V. A first source voltage Vs**1** is applied on the source **108***a*, and the first source voltage Vs**1** is, for example, 0 V. A first drain voltage Vd**1** is applied on the drain **108***b*, and the first drain voltage Vd**1** is, for example, 0 V. A first substrate voltage Vsub**1** is applied on the substrate **102**, and the first substrate voltage Vsub**1** is, for example, 0 V. In this manner, when performing the erasing operation, holes are injected into the charge-trapping gate dielectric layer **106** from the substrate **102**, so as to erase the memory **100**.

Referring to FIG. **2**B, a schematic view of the programming operation of the memory according to the embodiments of the invention is shown. When performing the programming operation to the memory **100**, a second gate voltage Vg**2** is applied on the gate **104**, and the second gate voltage Vg**2** is, for example, between 14 V and 20 V. A second source voltage Vs**2** is applied on the source **108***a*, and the second source voltage Vs**2** is, for example, 0 V. A second drain voltage Vd**2** is applied on the drain **108***b*, and the second drain voltage Vd**2** is, for example, 0 V. A second substrate voltage Vsub**2** is applied on the substrate **102**, and the second substrate voltage Vsub**2** is, for example, 0 V. In this manner, when performing the programming operation, the holes are pulled from the charge-trapping gate dielectric layer **106** to the substrate **102**, so as to program the memory **100**.

Hereinafter, a capacitance-voltage relation diagram when operating the memory is used to illustrate that the memory in the embodiments of the invention has a memory function.

Referring to FIG. **3**, a capacitance-voltage relation diagram when operating the memory according to the embodiments of the invention is shown. In the figure, a curve **310** represents a capacitance-voltage curve (C-V curve) when performing the erasing operation to the memory. The erasing operation is performed under the condition that the first gate voltage Vg**1** is −18 V and the first source voltage Vs**1**, the first drain voltage Vd**1**, and the first substrate voltage Vsub**1** are 0 V. As such, the holes are injected into the charge-trapping gate dielectric layer **106**, thereby reducing the critical voltage of the memory. Moreover, the curve **320** in the figure represents a C-V curve when performing the programming operation to the memory. The programming operation is performed under the condition that the second gate voltage Vg**2** is 18 V and the second source voltage Vs**2**, the second drain voltage Vd**2**, and the second substrate voltage Vsub**2** are 0 V. As such, the holes can be pulled from the charge-trapping gate dielectric layer **106**, thereby increasing the critical voltage of the memory. Therefore, it can be known that the memory of the embodiments of the invention can perform erasing and programming operations after being applied with voltages.

In view of the above, the structure of the memory of the embodiments of the invention is similar to that of the transistor of a common logic device, so the memory can be applied into the embedded memory. In other words, on the same system a transistor of a logic device and a memory in the embodiments of the invention can be simultaneously framing, thereby increasing the process yield and simplifying the process. Moreover, the memory can be used as a one time programmable memory or an erasable/programmable memory.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the embodiments of the invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the embodiments of the invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A semiconductor device, comprising:

a substrate having a logic circuit region and a memory region;

a metal oxide semiconductor transistor, disposed in the logic circuit region, and comprising a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a gate dielectric layer disposed between the gate and the substrate; and

a memory, disposed in the memory region, wherein the memory and the metal oxide semiconductor transistor are the same stacked structure having the same materials, and the memory comprises a substrate, a drain and a source disposed in the substrate, a gate disposed between the drain and the source and above the substrate, and a charge-trapping gate dielectric layer disposed between the gate and the substrate.

2. The semiconductor device as claimed in claim **1**, wherein the thickness of the charge-trapping gate dielectric layer is between 20 Å and 200 Å.

3. The semiconductor device as claimed in claim **1**, wherein the charge-trapping gate dielectric layer comprises a doped silicon oxide layer, a nitrided silicon dioxide layer, a deposited silicon oxide layer, a silicon oxynitride layer, or a silicon nitride layer.

4. The semiconductor device as claimed in claim **1**, wherein the gate comprises an N-type doped polysilicon layer or a P-type doped polysilicon layer.

5. The semiconductor device as claimed in claim **1**, wherein the gate is a metal gate.

6. The semiconductor device as claimed in claim **1**, wherein the source and the drain are the same, which comprises an N-type doped region or a P-type doped region.

7. The semiconductor device as claimed in claim **1**, wherein the memory is a one time programmable memory.

8. The semiconductor device as claimed in claim **1**, wherein the memory is an erasable/programmable memory.

* * * * *