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Onishi et al.

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(54) **INTEGRATED CIRCUIT DEVICE AND ELECTRONIC INSTRUMENT**

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(51) **Int. Cl.**

H03K 19/173 (2006.01)
H01L 25/00 (2006.01)
G05F 1/00 (2006.01)

(57) **ABSTRACT**

(52) **U.S. Cl.** **326/47**; 326/101; 323/282; 323/283; 307/107; 307/104

An integrated circuit device includes a digital power supply regulation circuit, an analog power supply regulation circuit, a control logic circuit, an analog circuit, and a power supply wiring region. A digital power supply line which supplies a digital power supply voltage and an analog power supply line which supplies an analog power supply voltage are provided in the power supply wiring region. The digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit are disposed in a first direction with respect to the control logic circuit. The power supply wiring region is formed along a second direction in a region between the control logic circuit and the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit.

(58) **Field of Classification Search** 326/38-41, 326/47, 101; 323/282, 283; 307/104, 107
See application file for complete search history.

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19 Claims, 20 Drawing Sheets

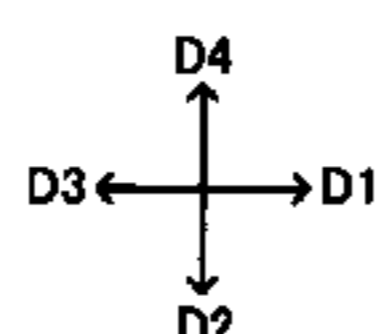
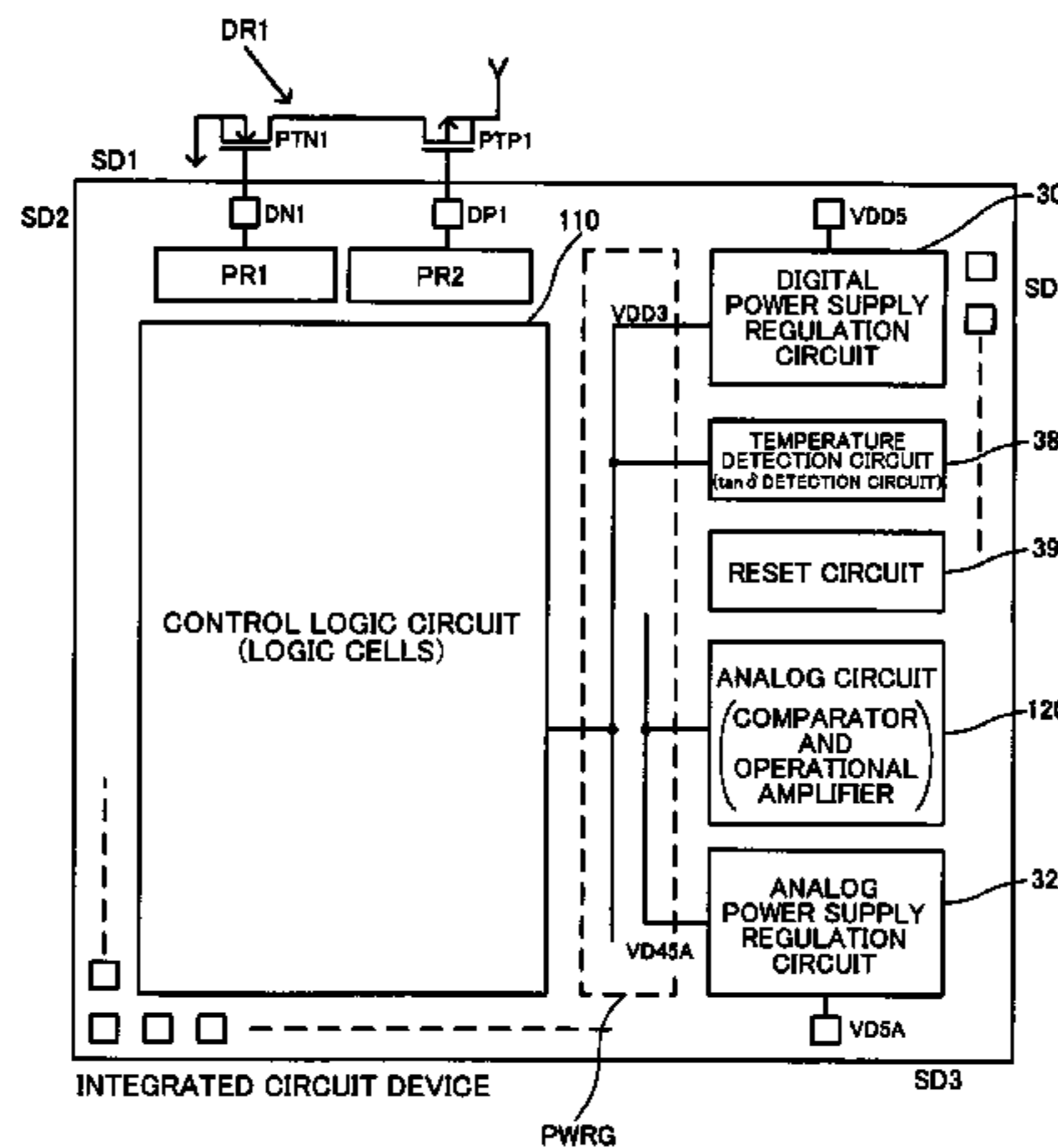


FIG. 1

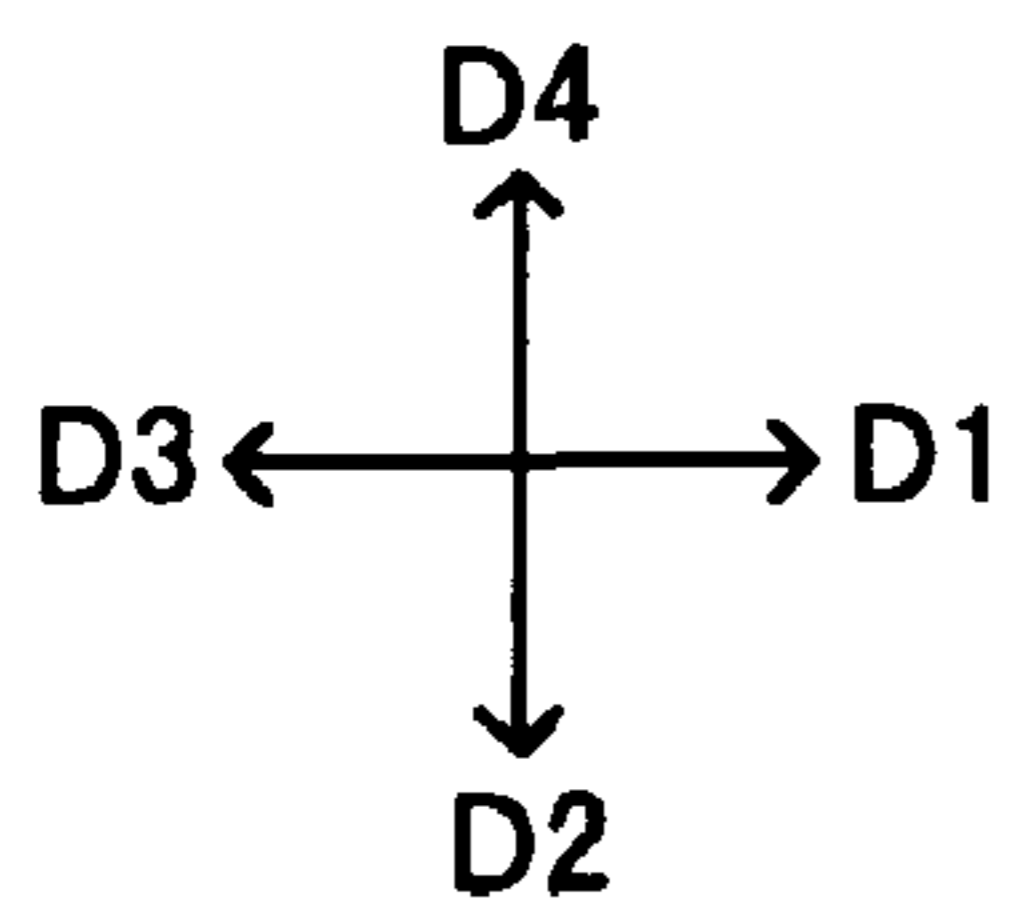
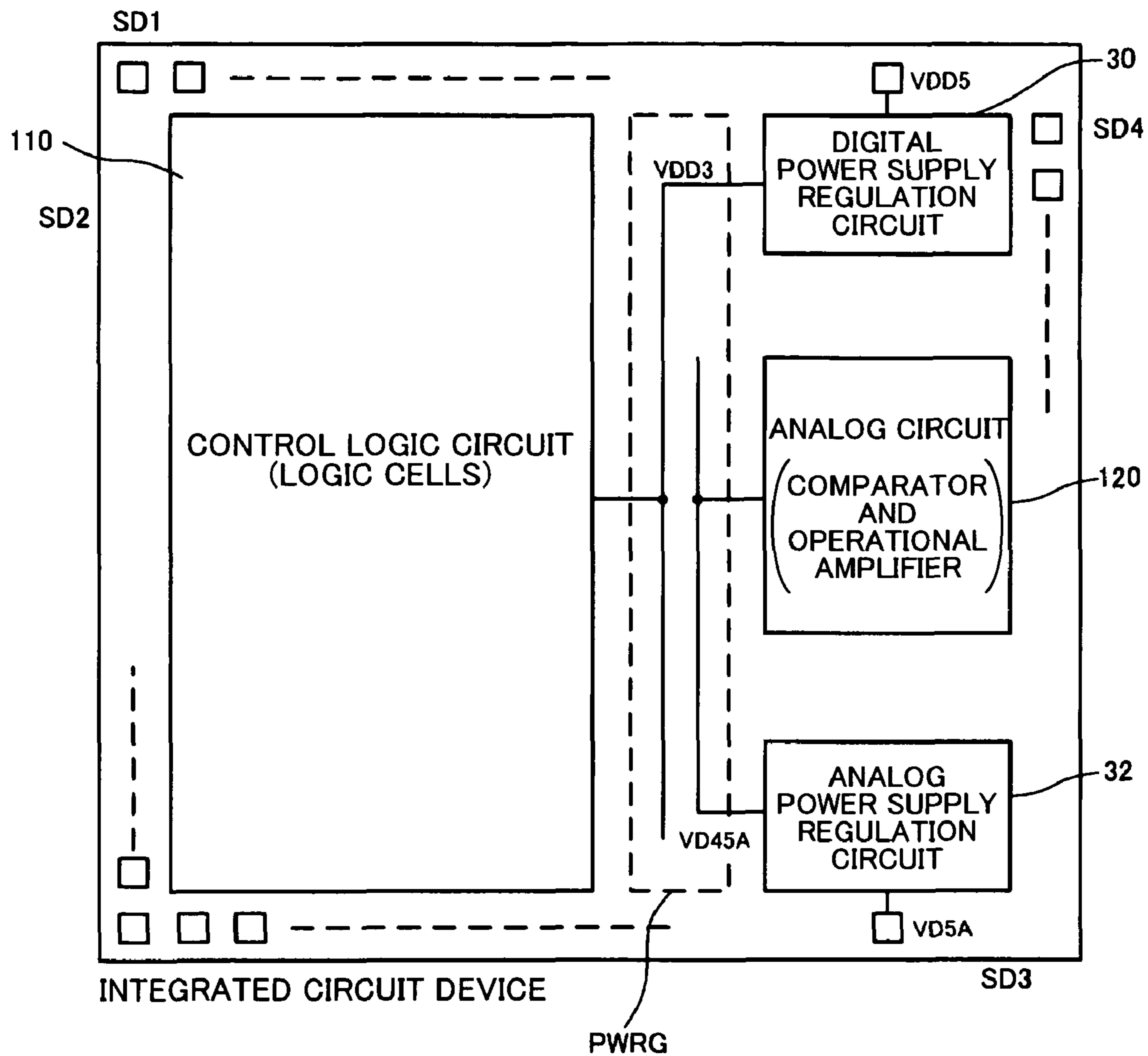


FIG. 2

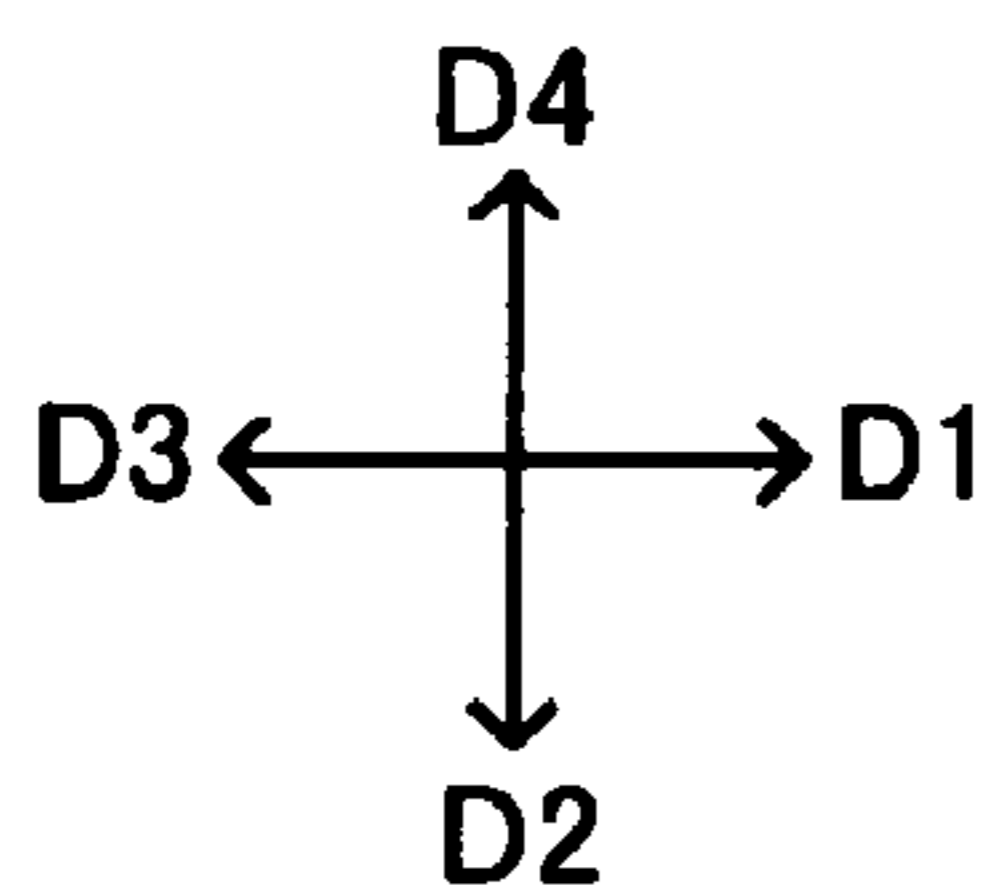
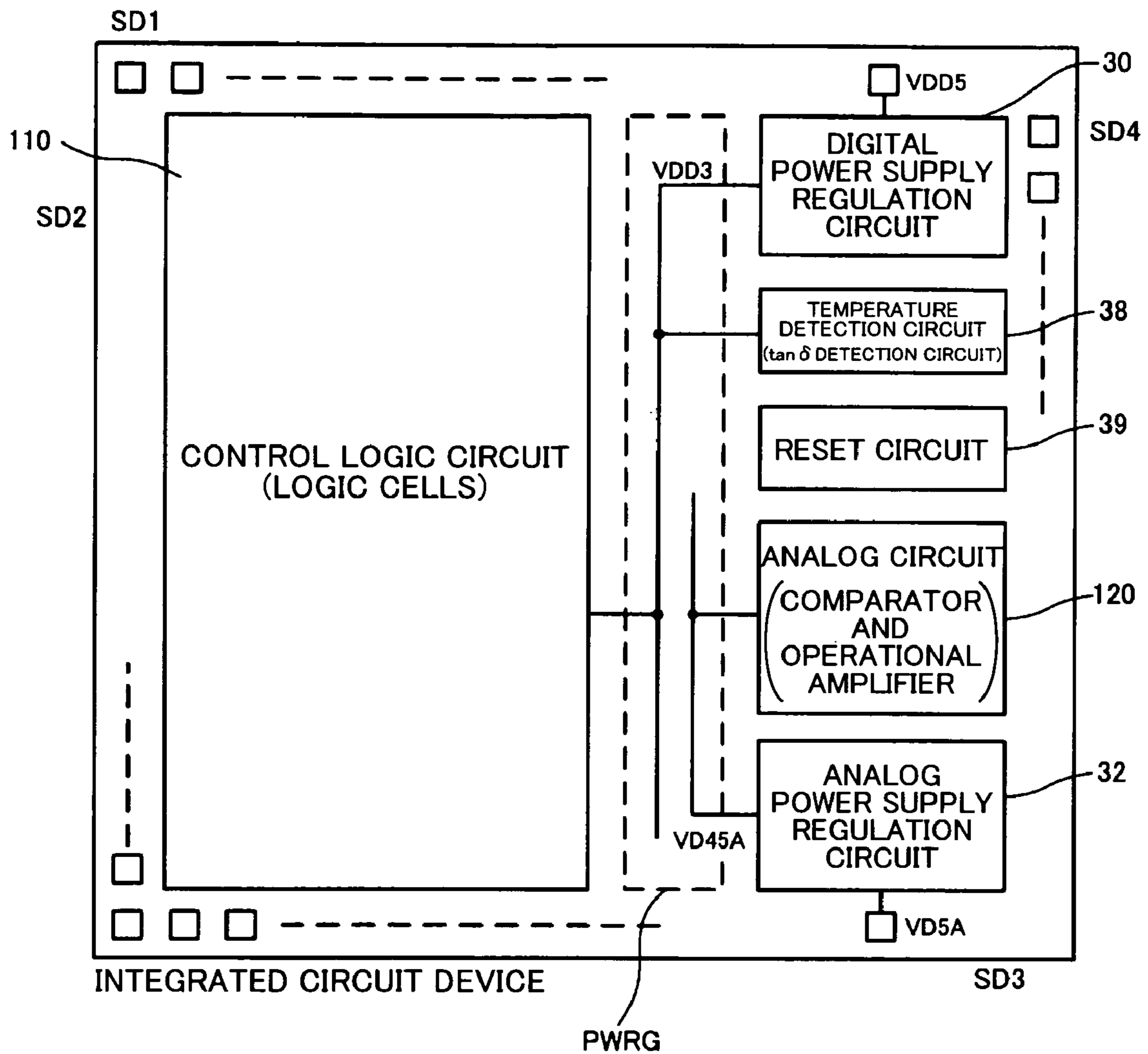


FIG. 3

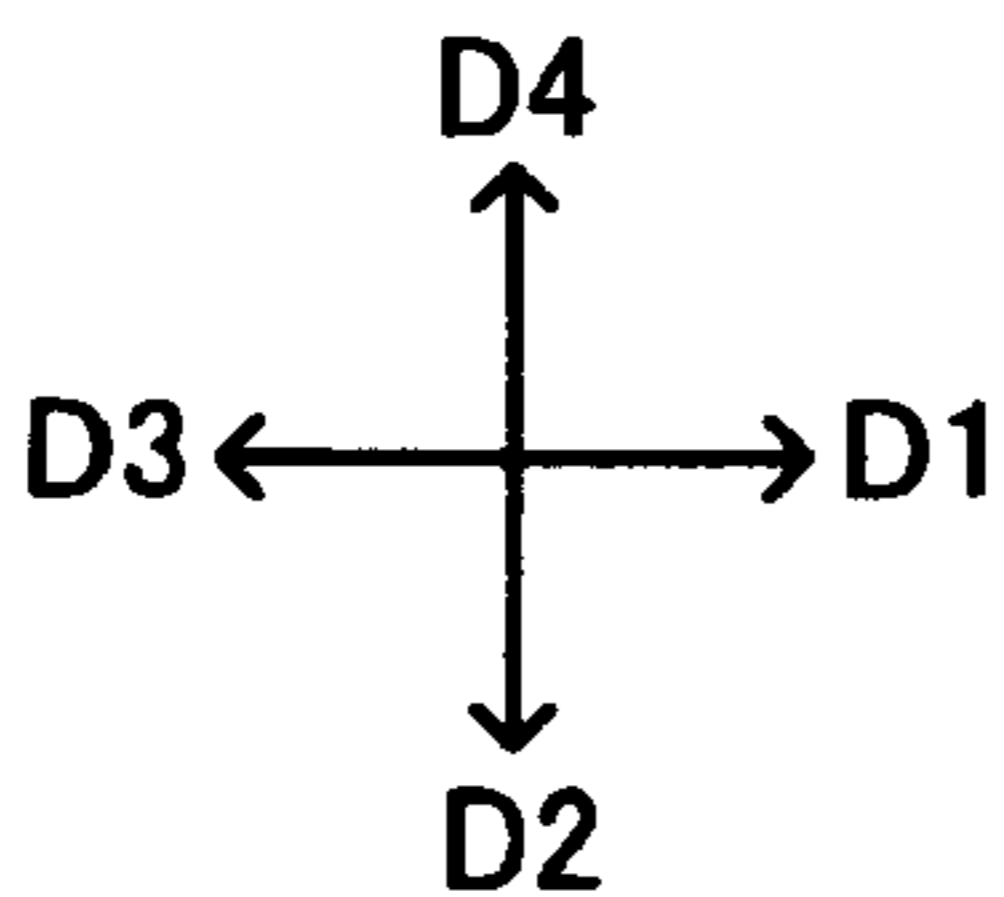
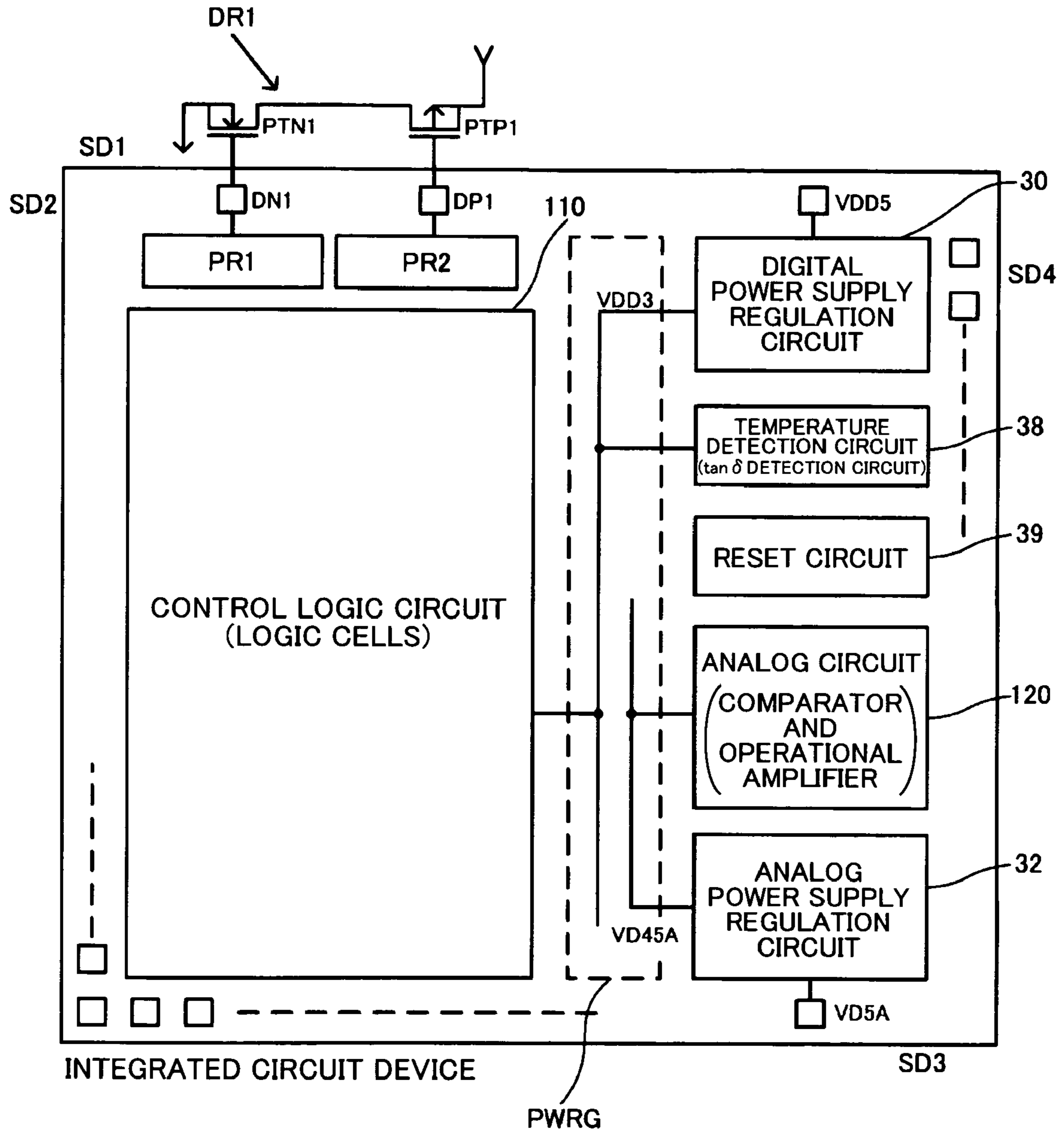


FIG. 4

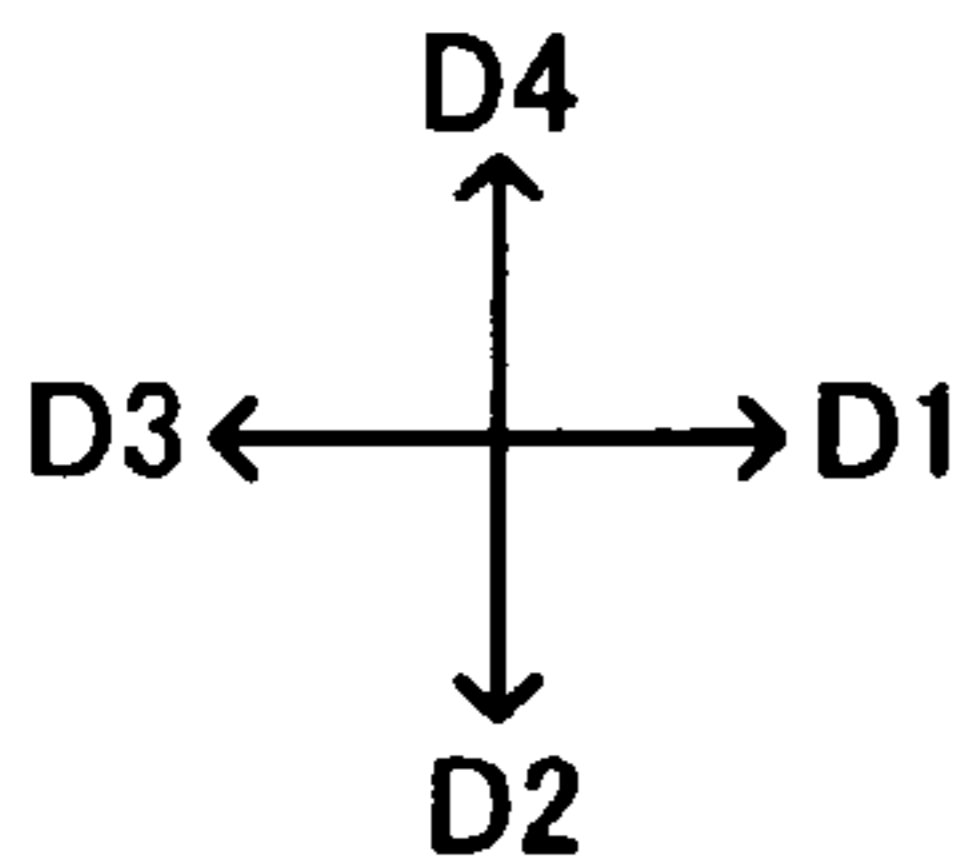
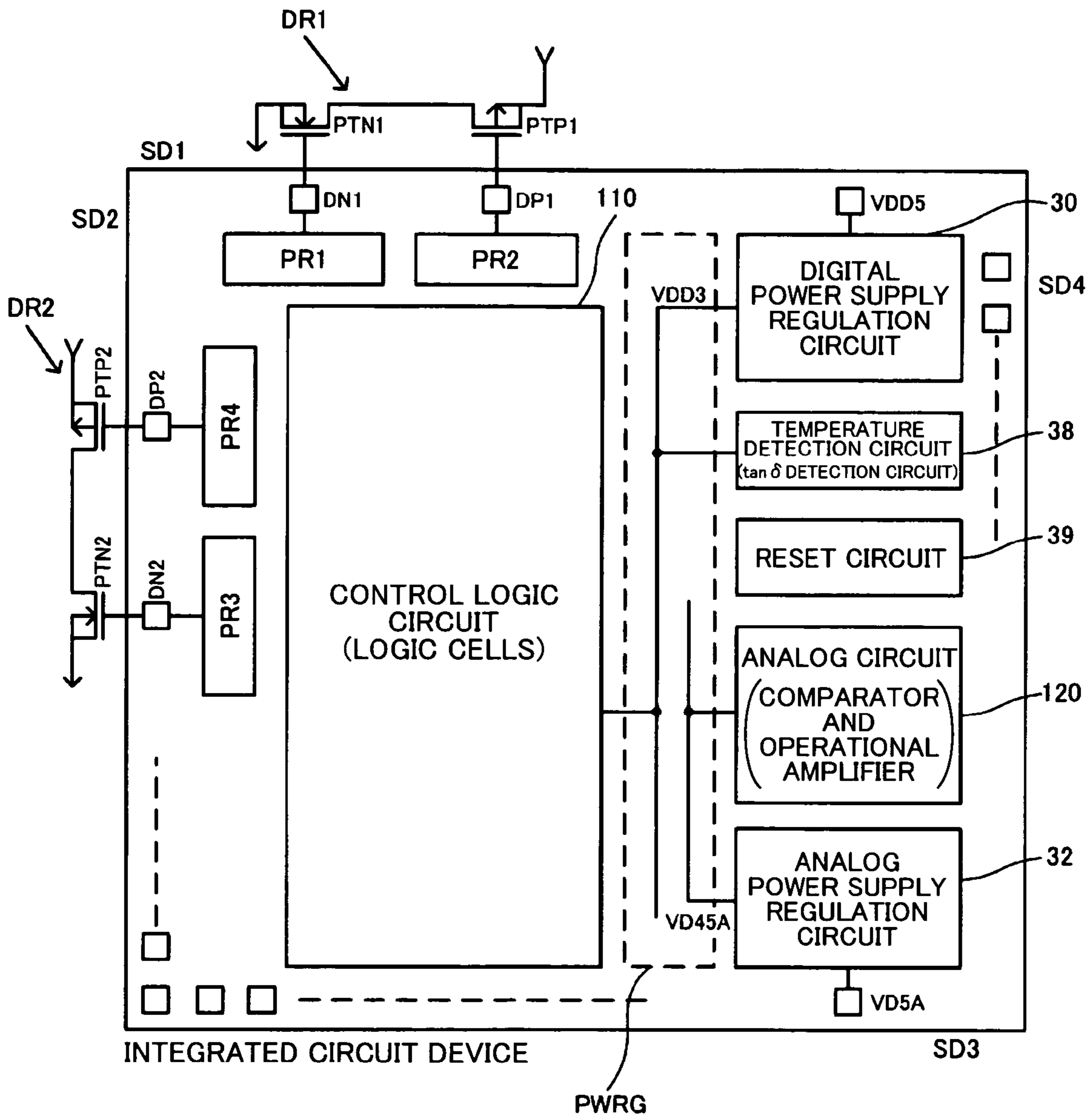


FIG. 5

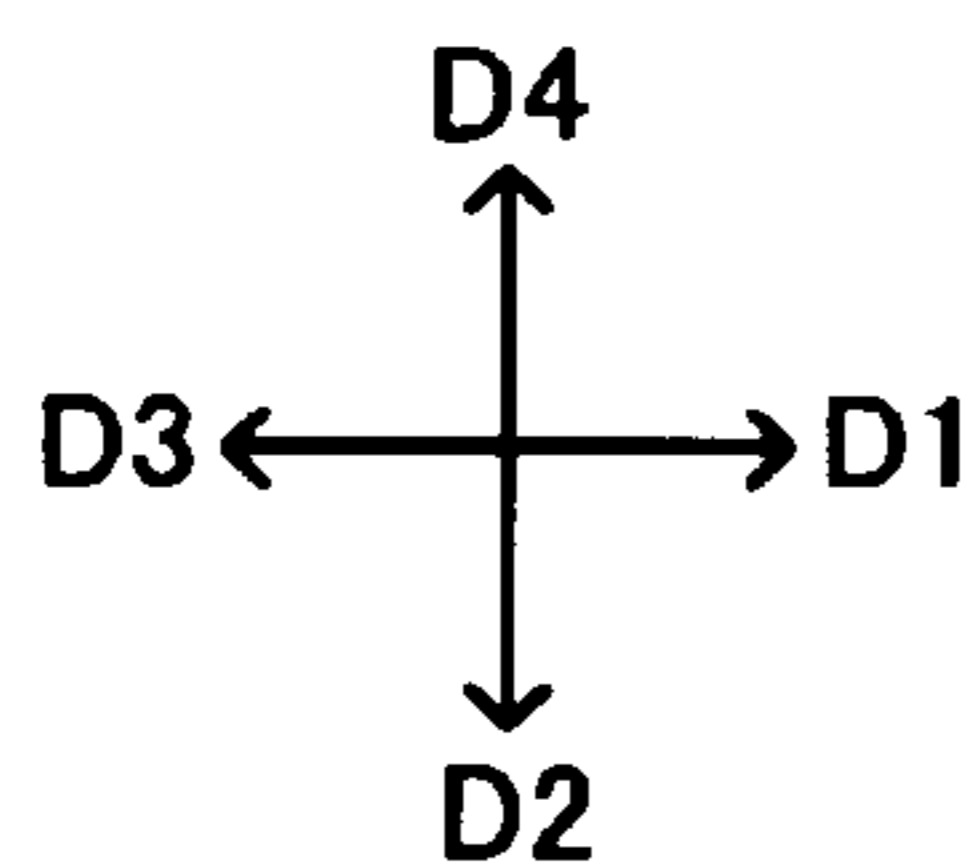
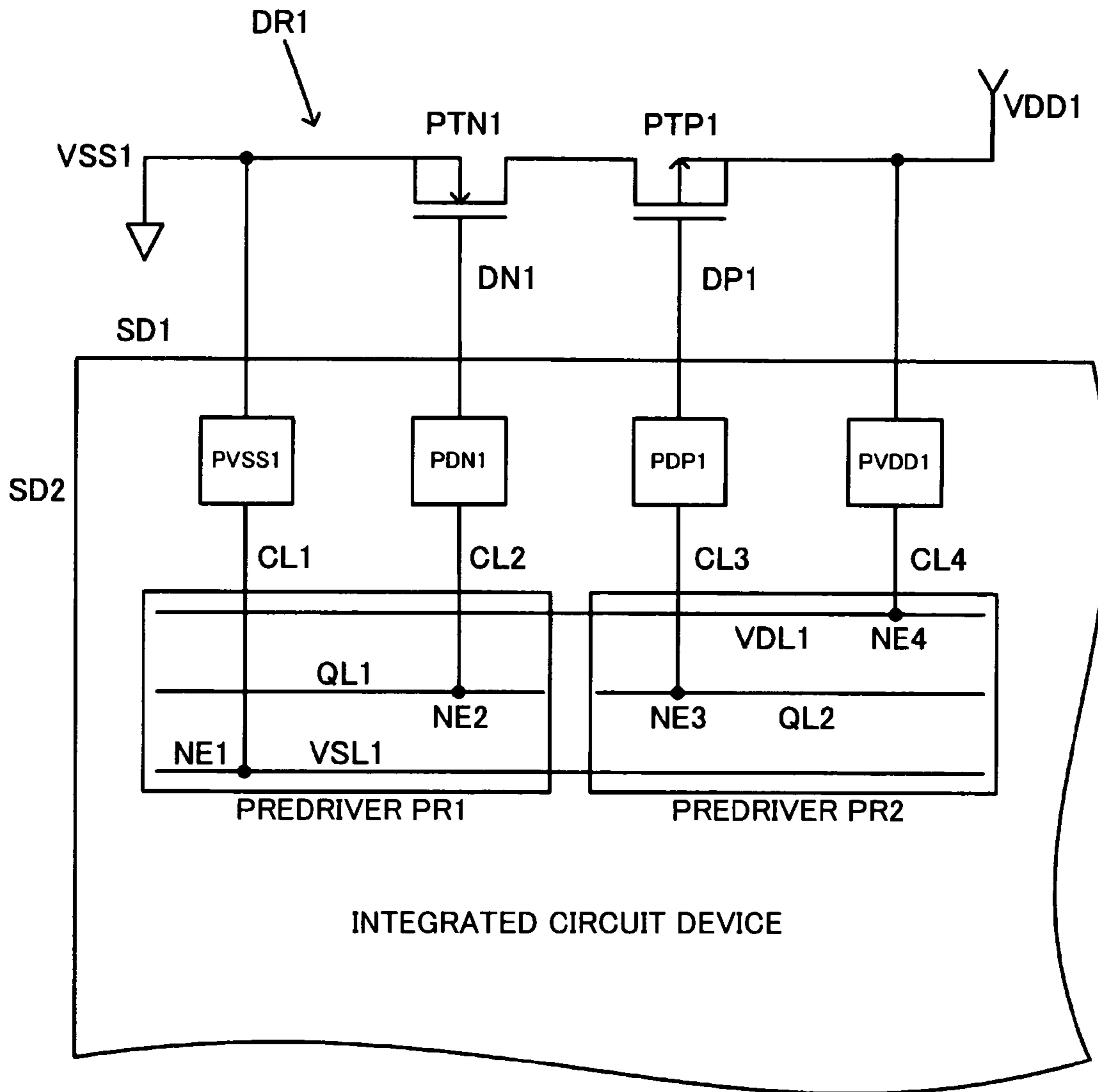


FIG. 6A

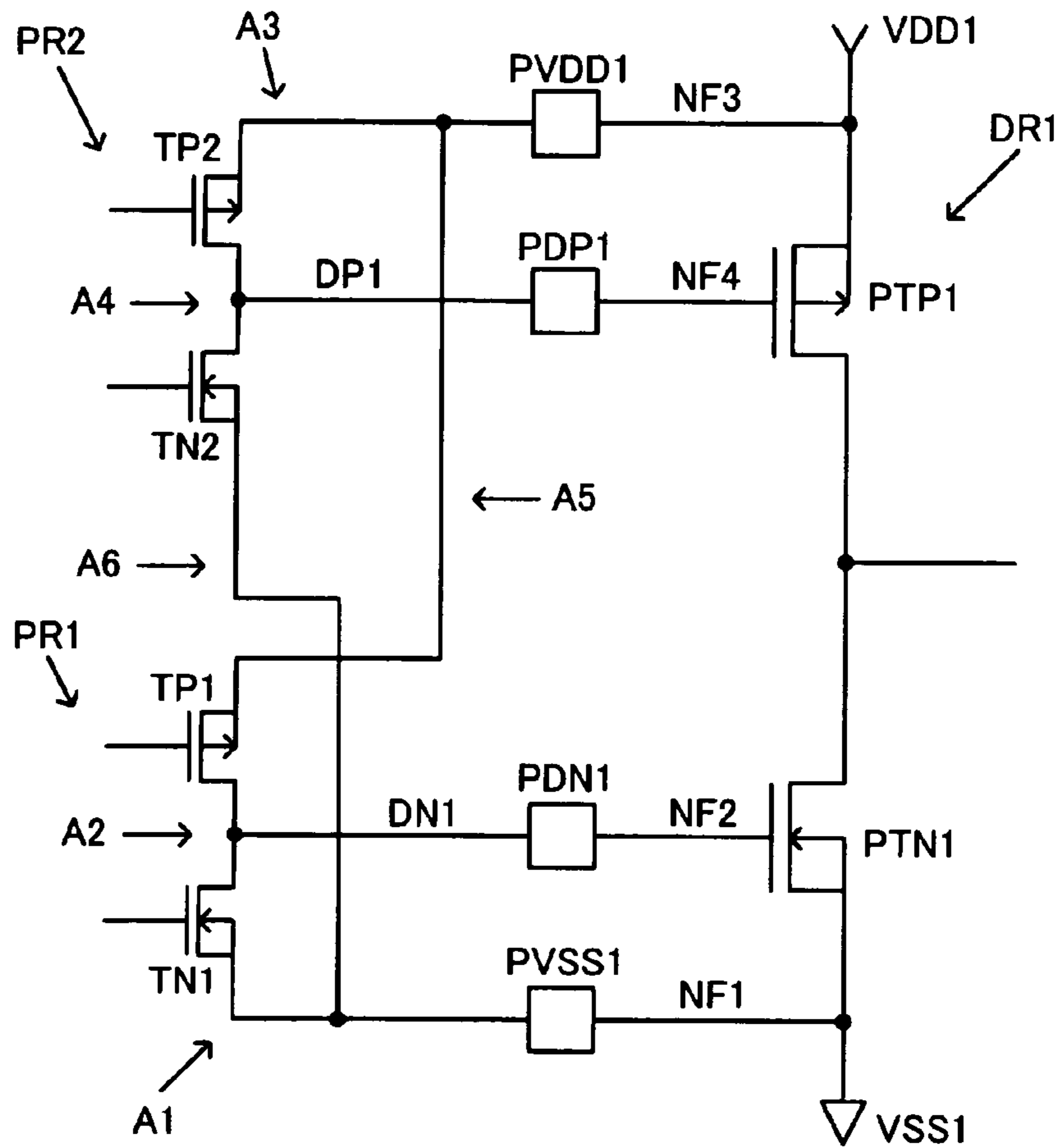


FIG. 6B

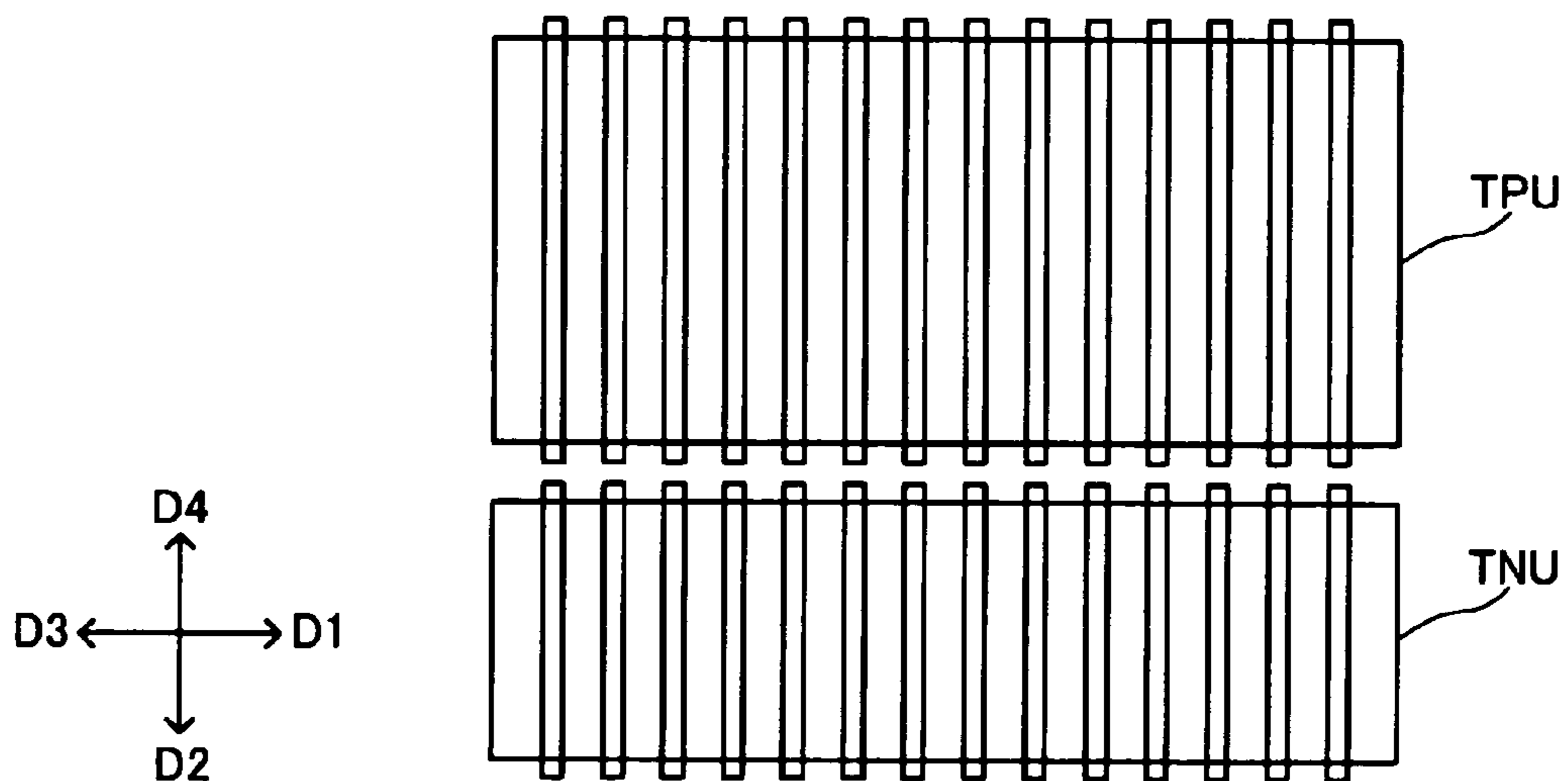


FIG. 7

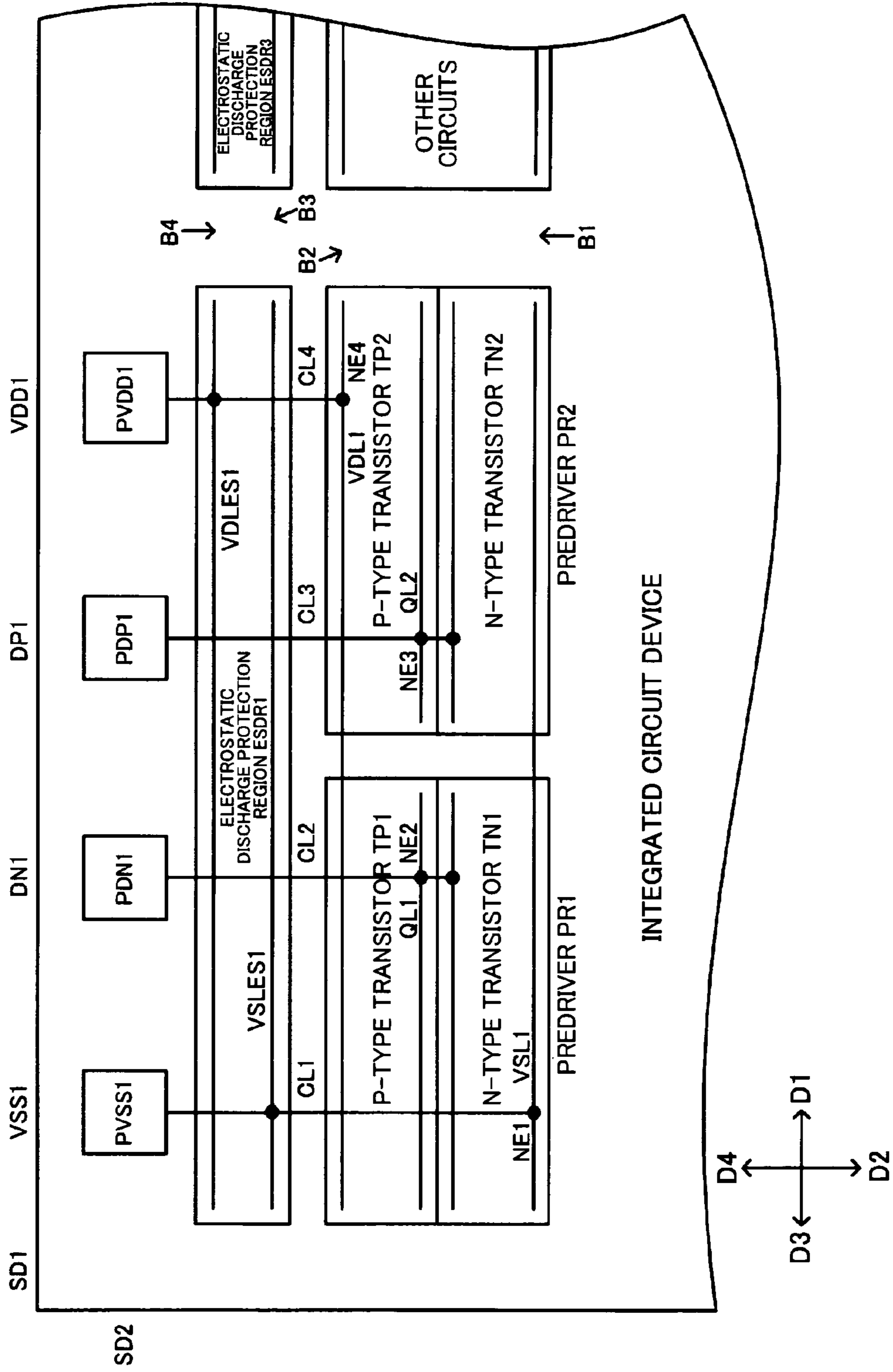


FIG. 8

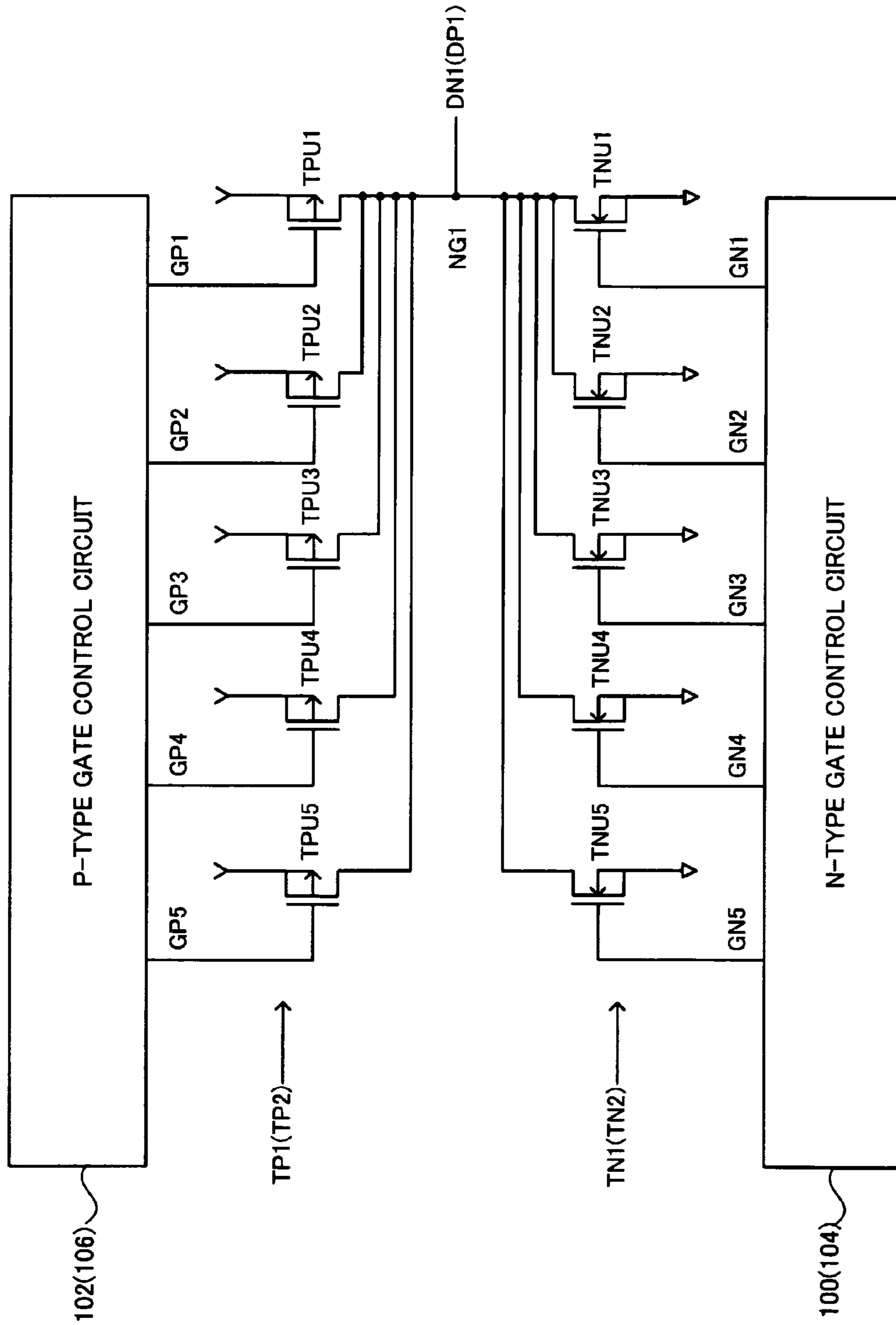


FIG. 9

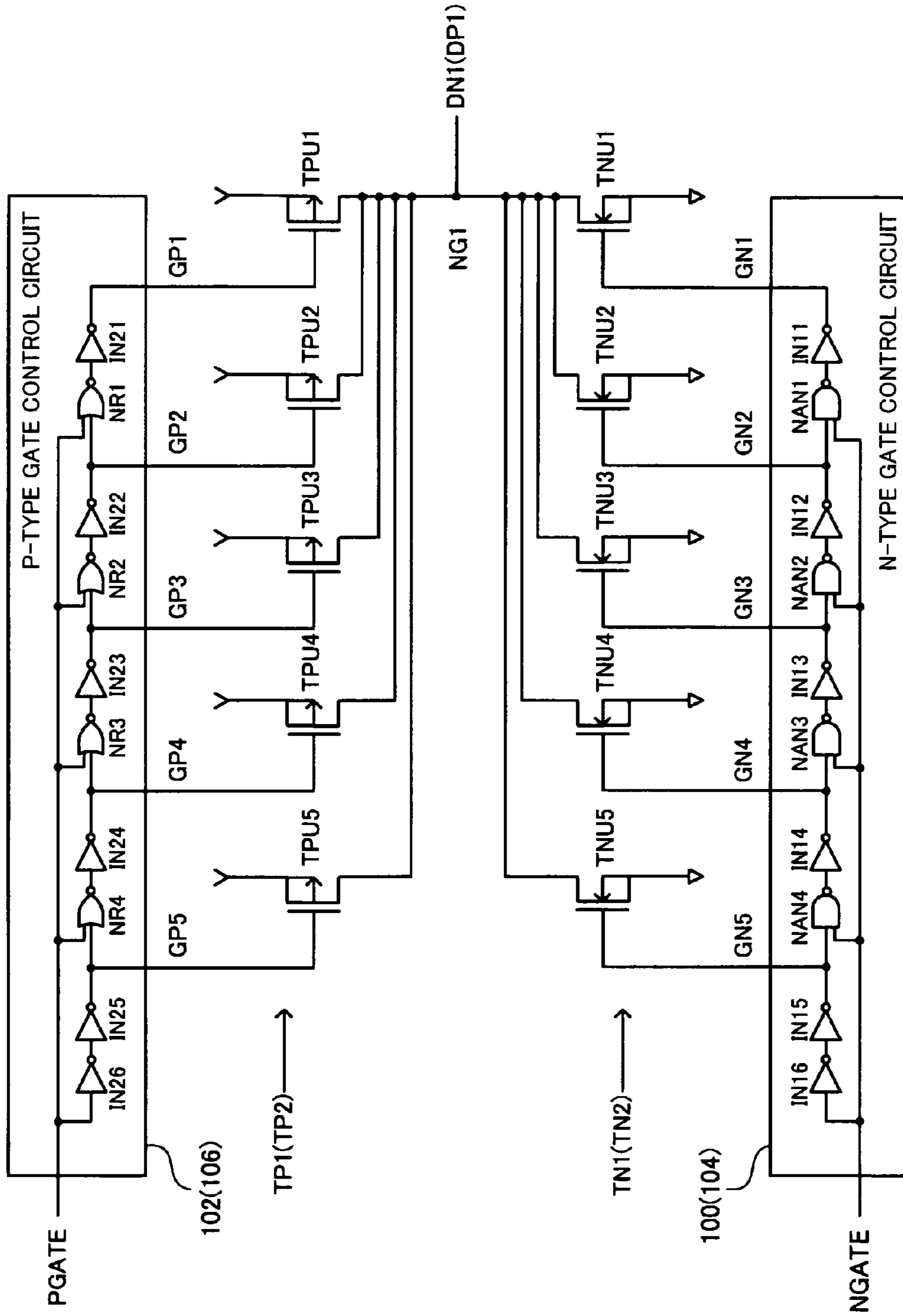


FIG. 11

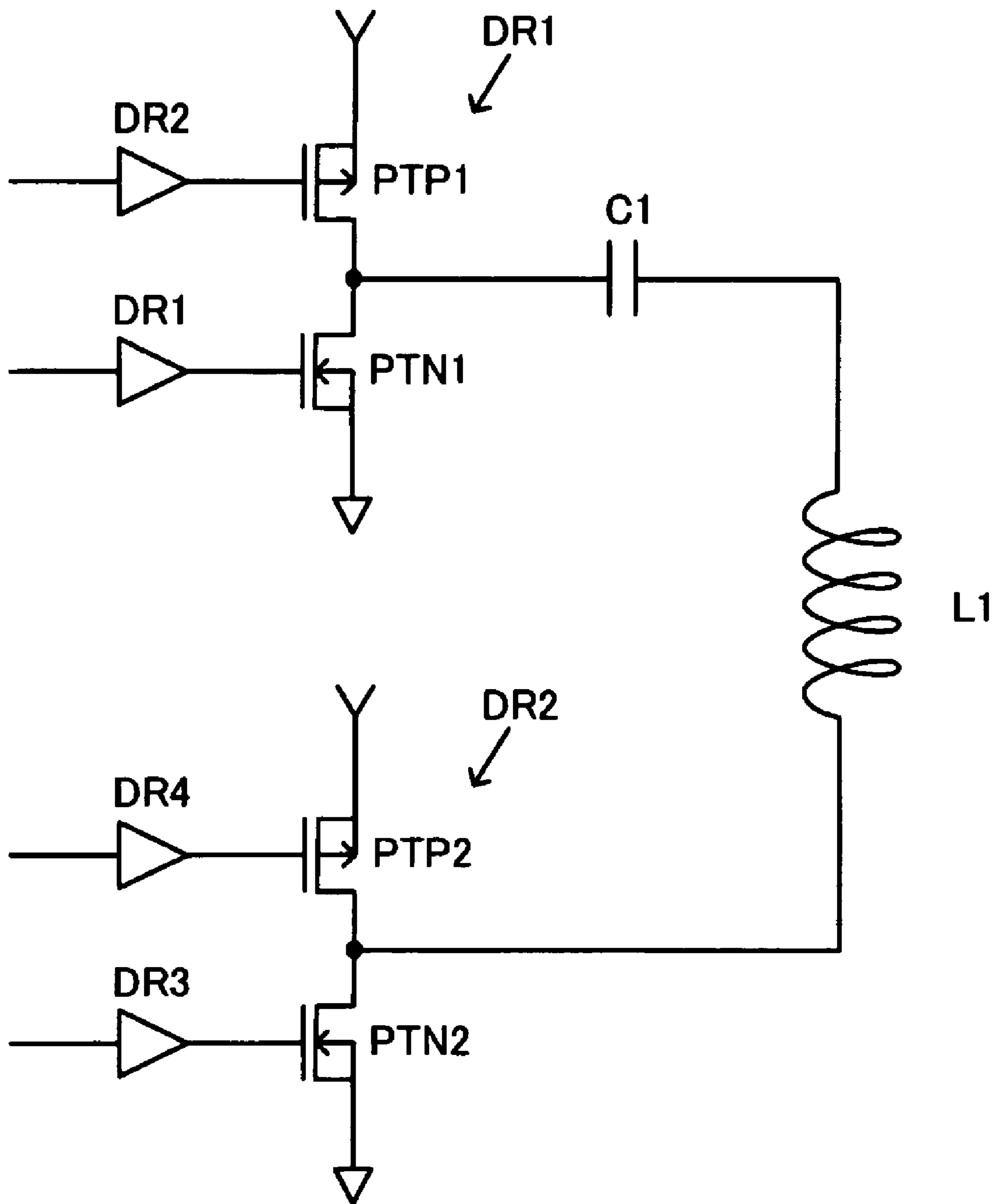


FIG. 12

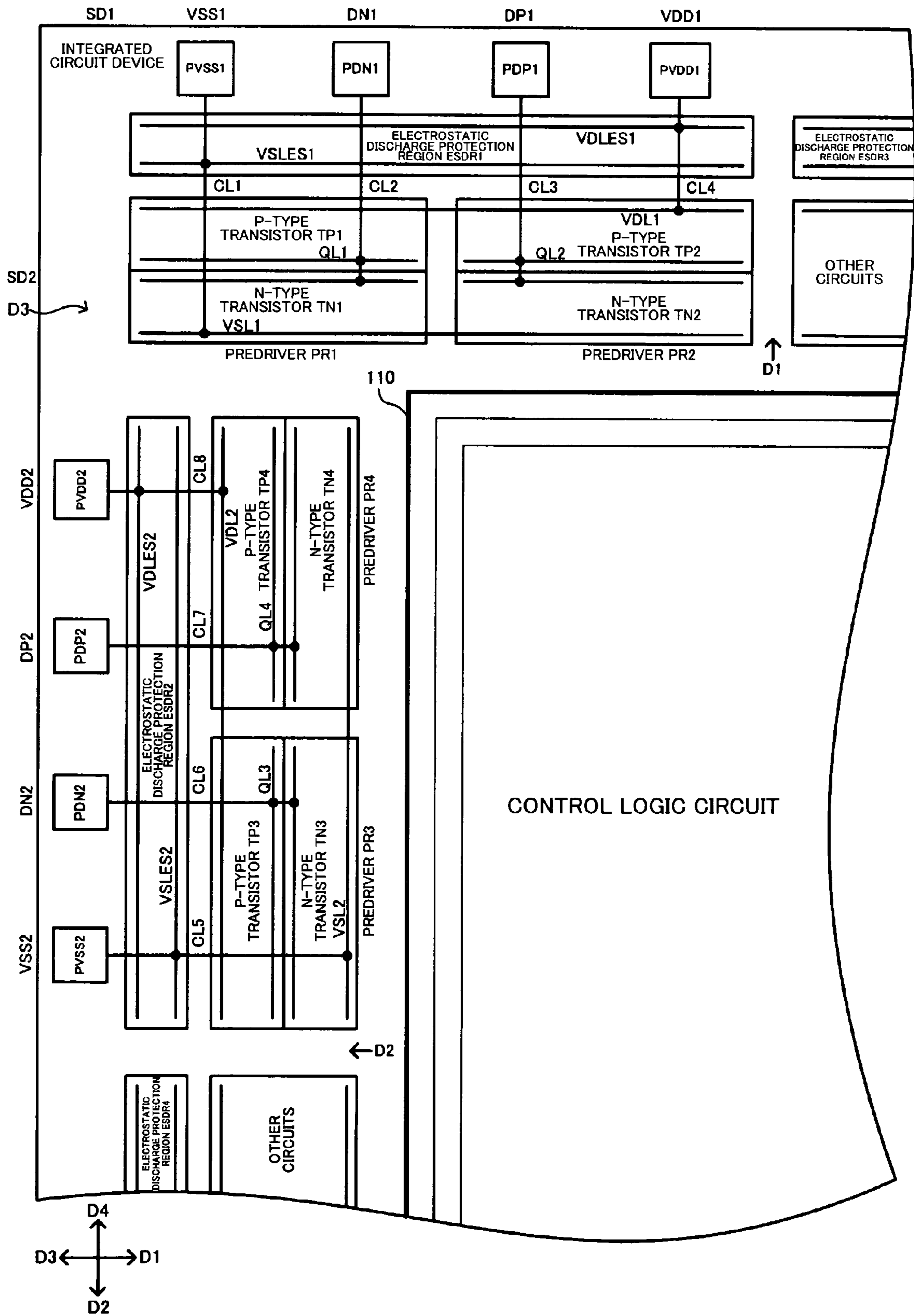


FIG. 13A

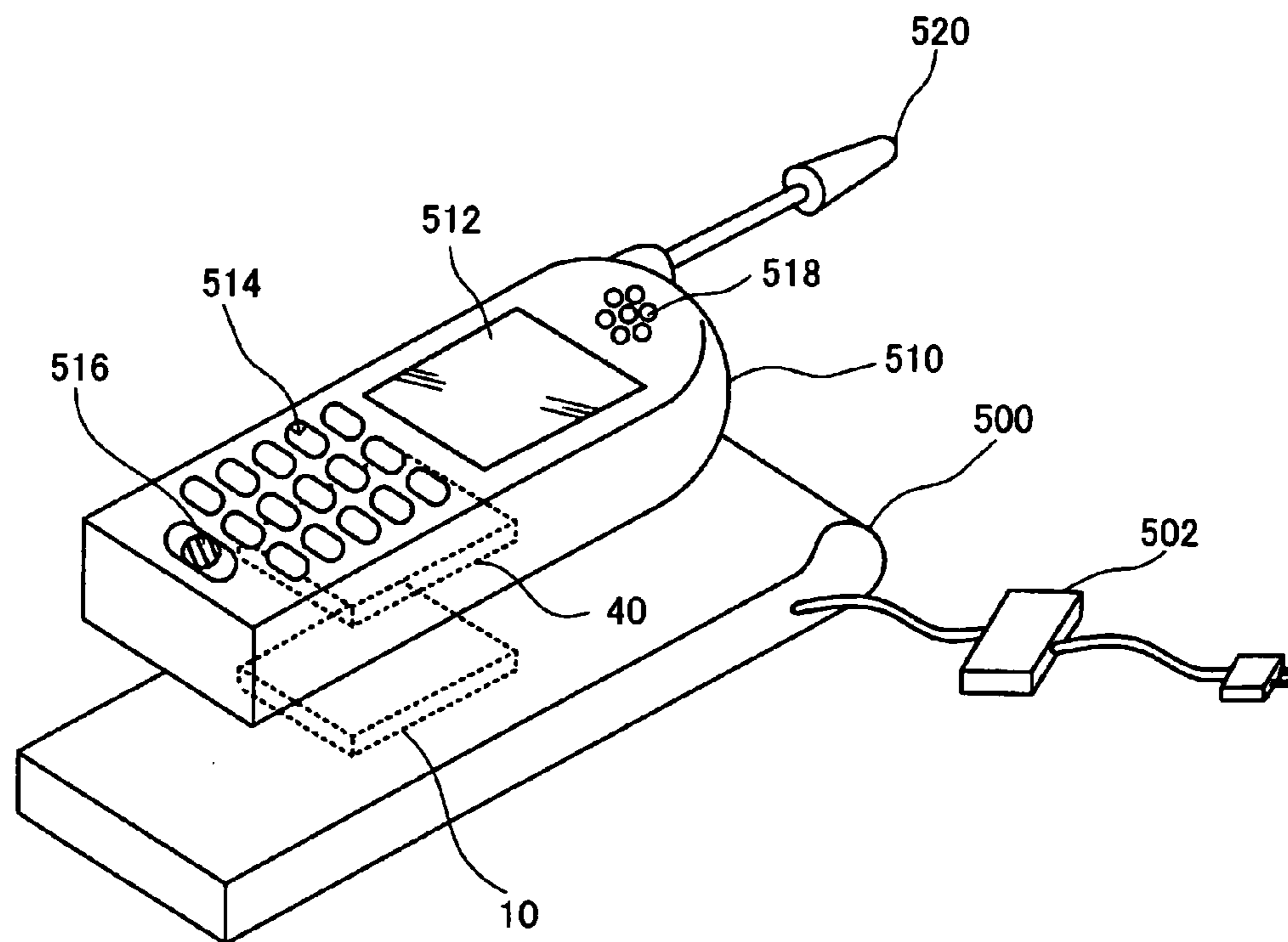


FIG. 13B

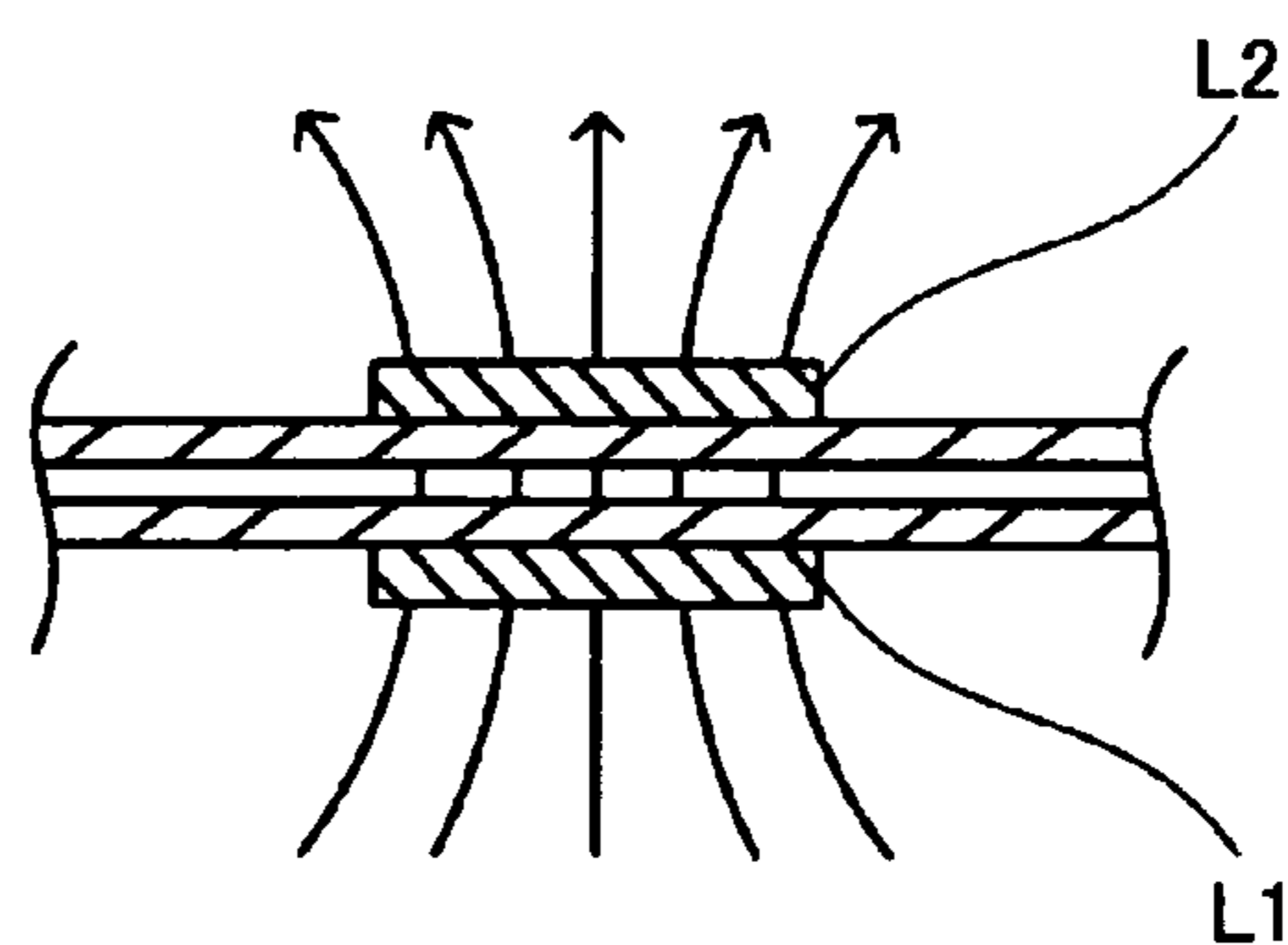


FIG. 14

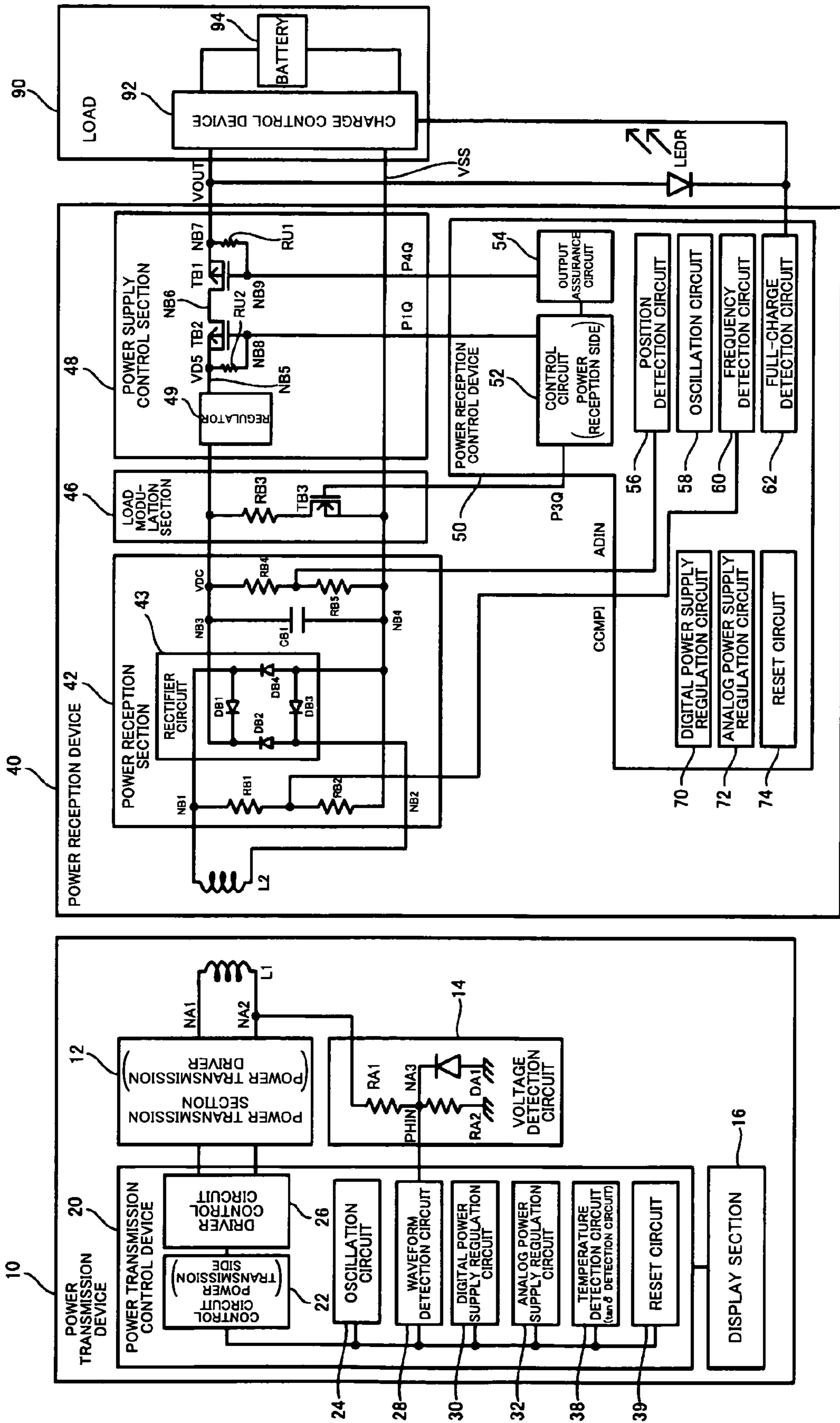


FIG. 15A

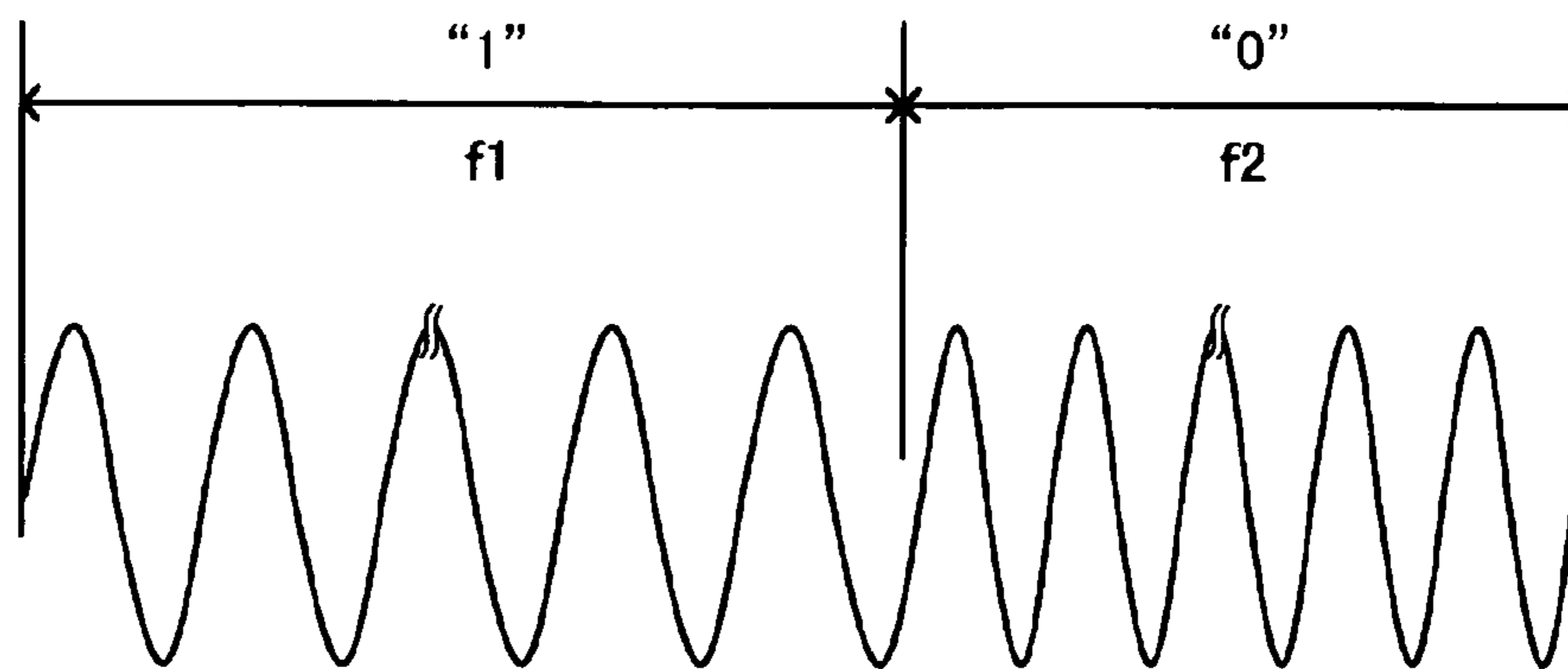


FIG. 15B

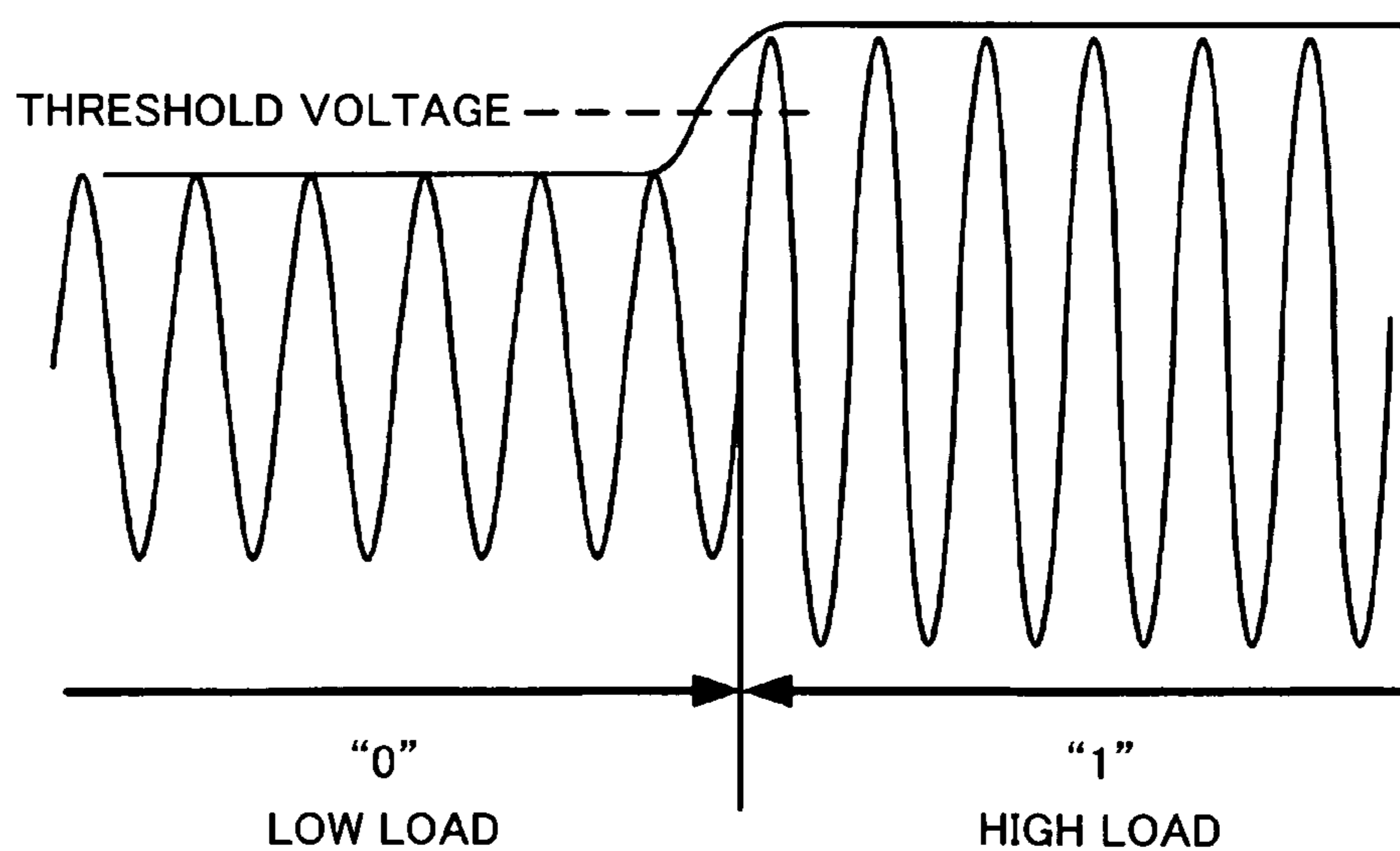


FIG. 16

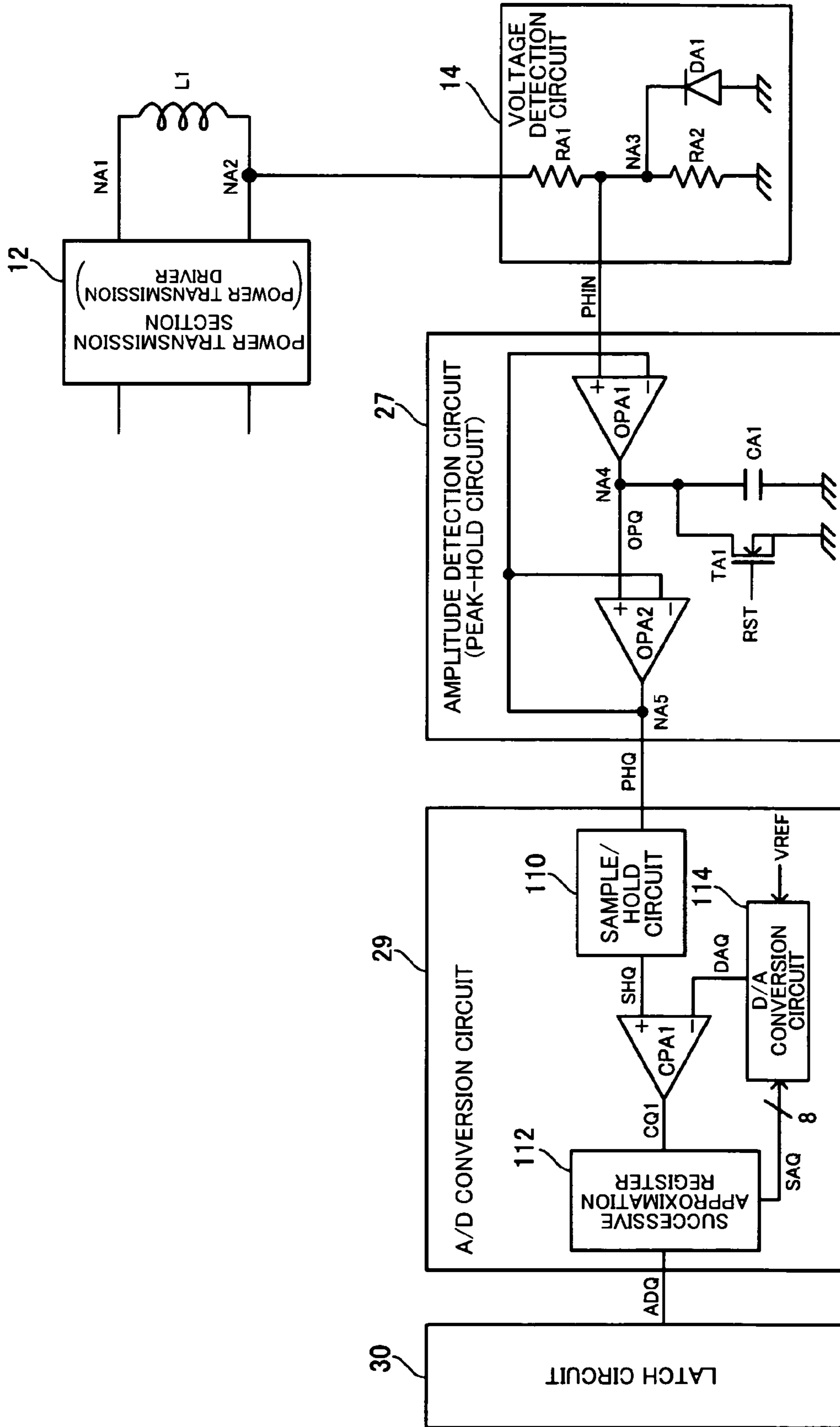


FIG. 17

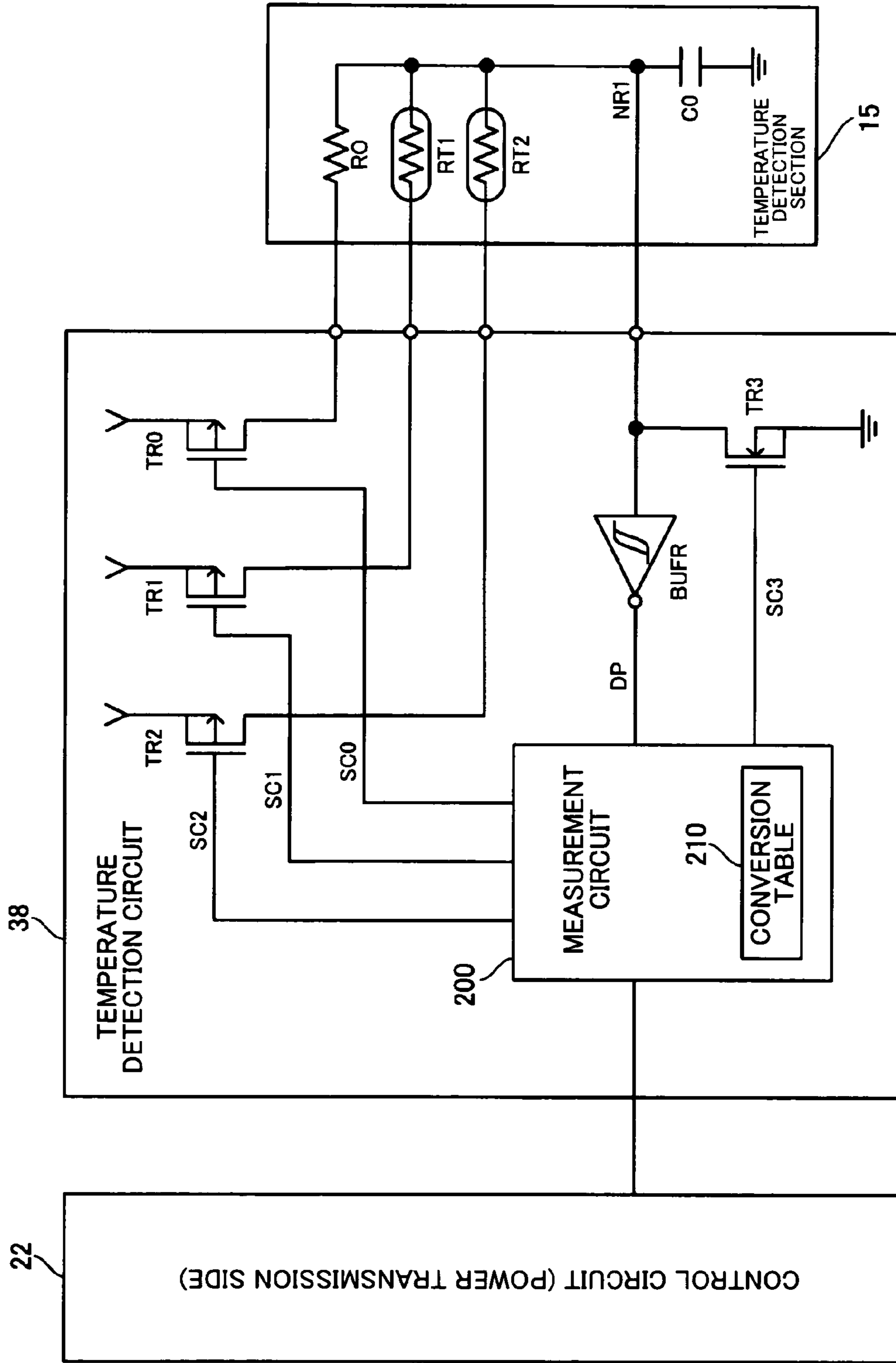


FIG. 18A

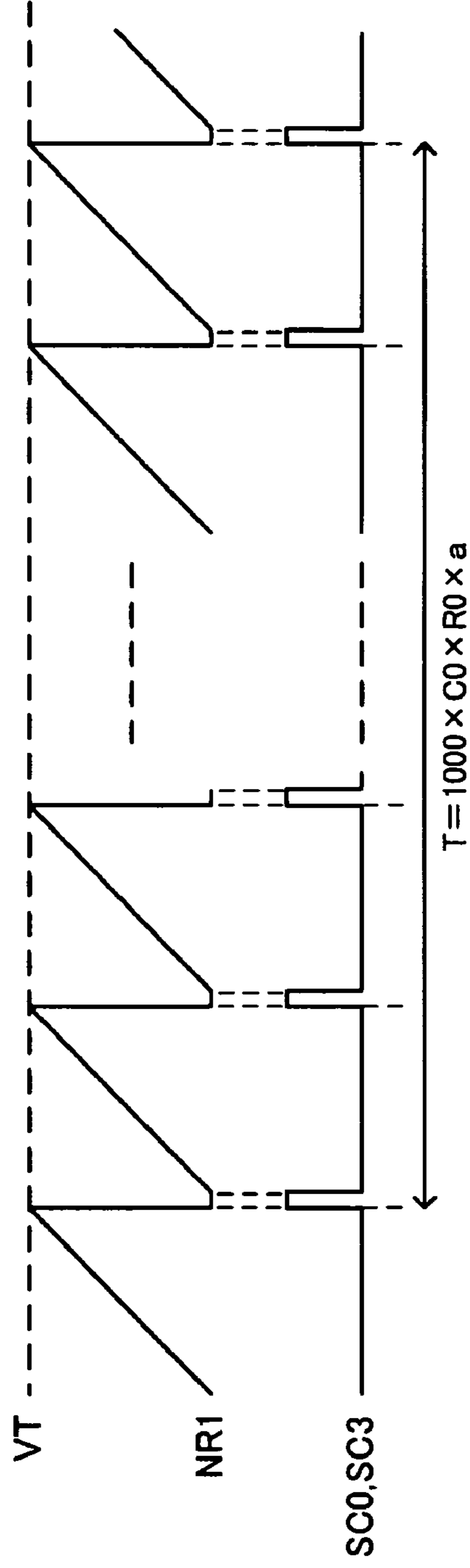


FIG. 18B

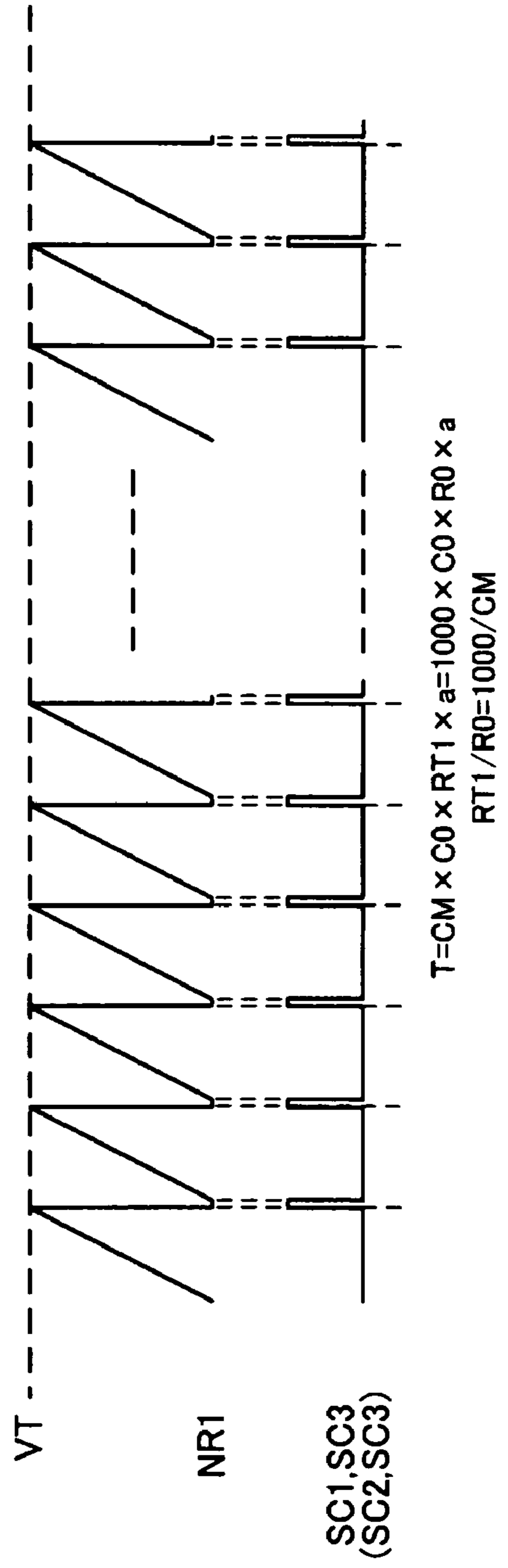


FIG. 19

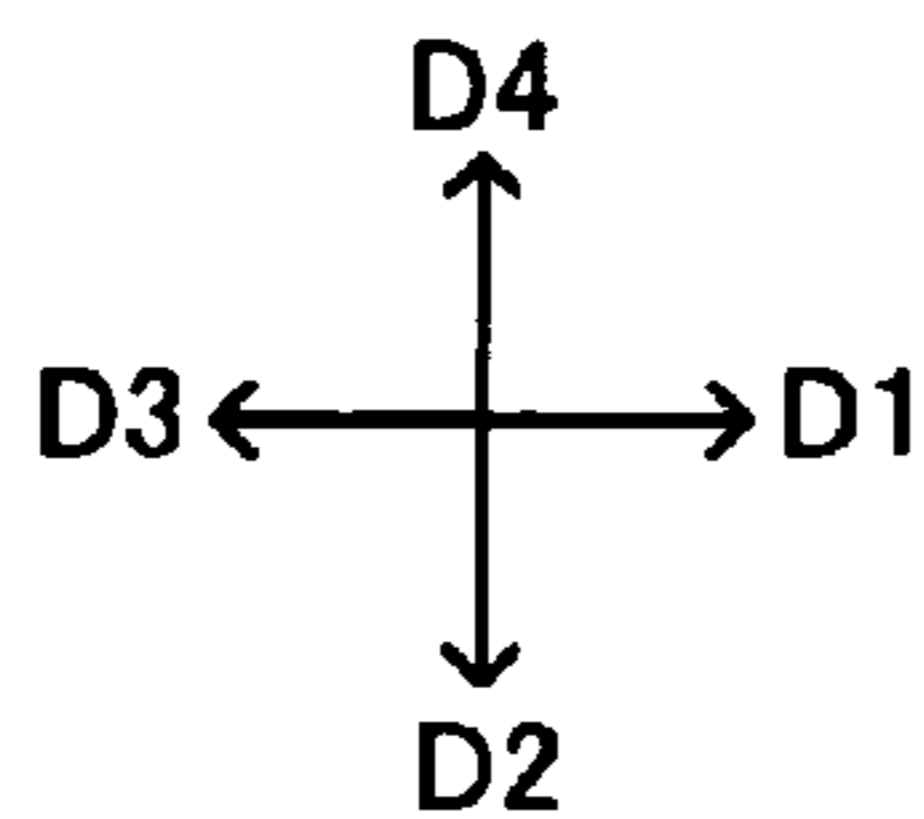
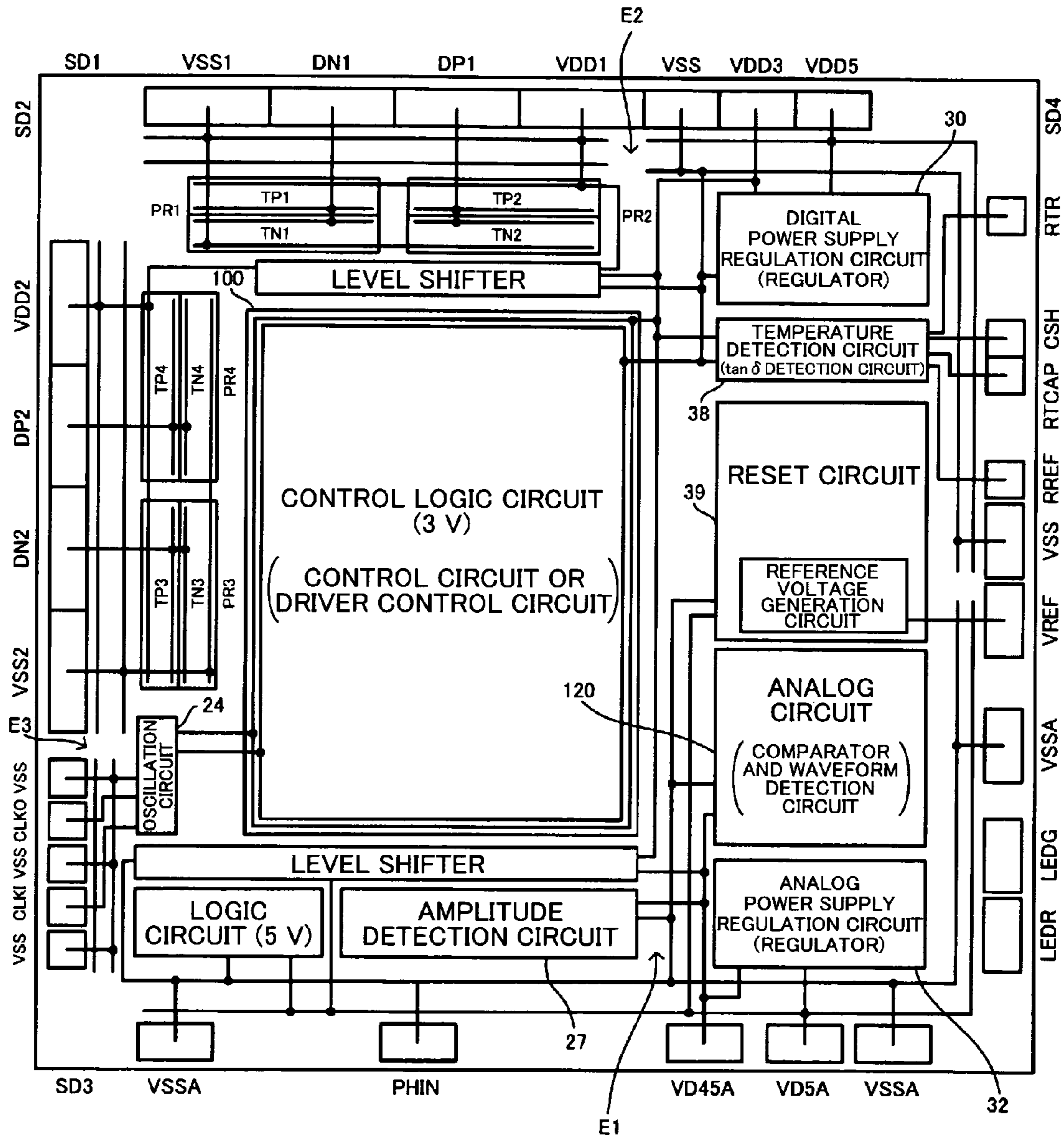
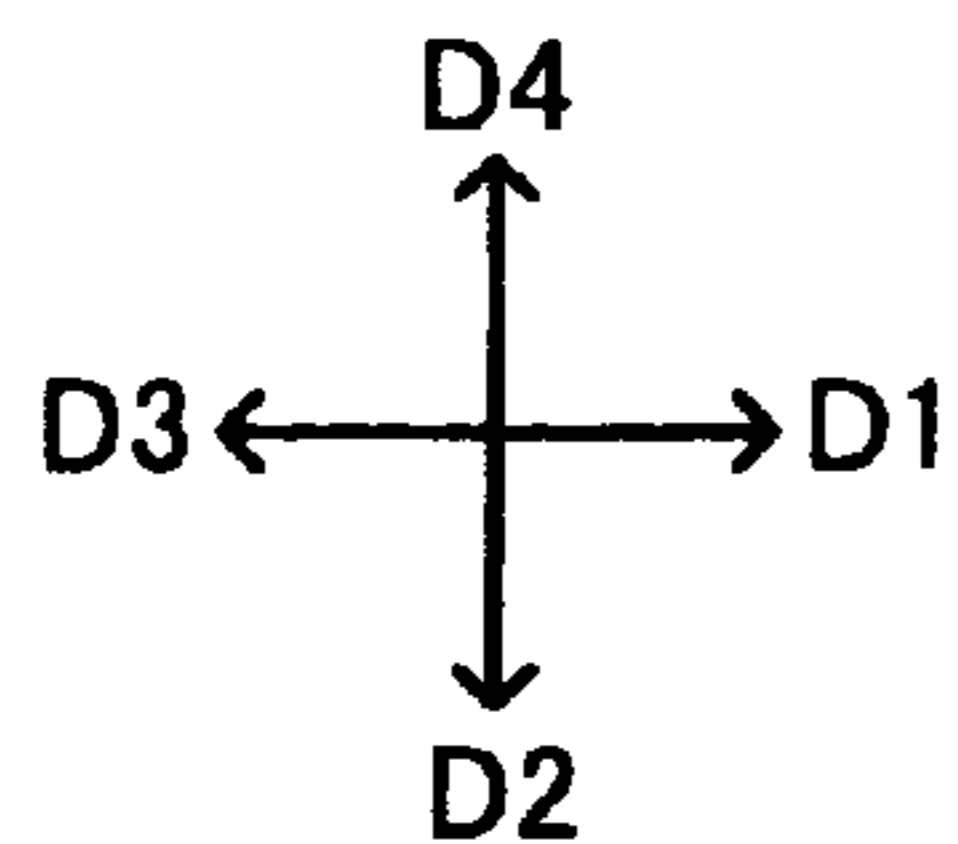
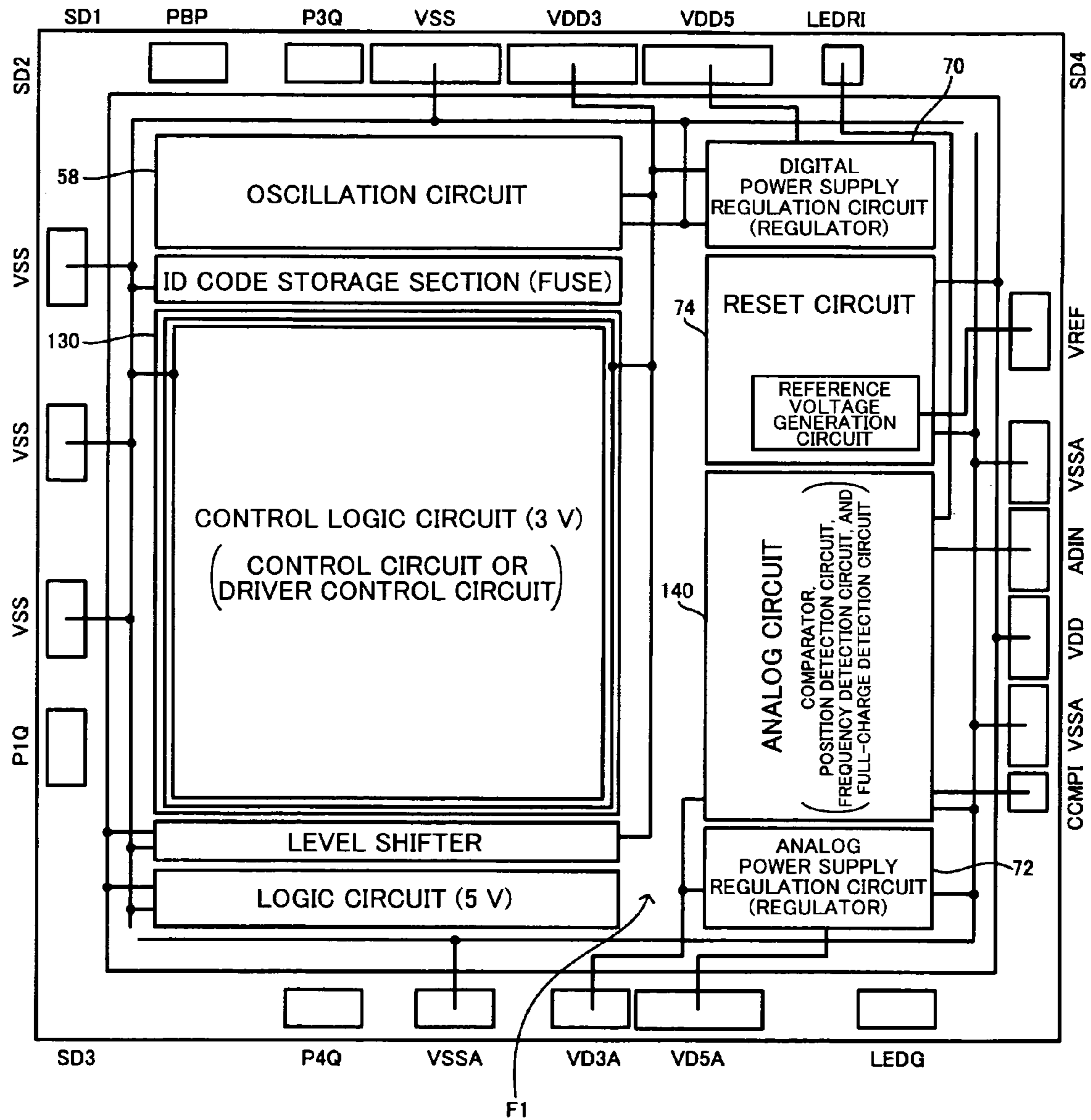


FIG. 20



INTEGRATED CIRCUIT DEVICE AND ELECTRONIC INSTRUMENT

Japanese Patent Application No. 2007-39654 filed on Feb. 20, 2007, is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to an integrated circuit device, an electronic instrument, and the like.

In recent years, non-contact power transmission (contactless power transmission) has attracted attention which utilizes electromagnetic induction to enable power transmission without metal-to-metal contact. As application examples of non-contact power transmission, charging a portable telephone, a household appliance (e.g., telephone handset), and the like has been proposed.

JP-A-2006-60909 discloses related-art non-contact power transmission. In JP-A-2006-60909, a resonant circuit is formed using a capacitor connected to an output of a power transmission driver and a primary coil so that power is supplied from a power transmission device (primary side) to a power reception device (secondary side). JP-A-6-21330 discloses a related-art semiconductor power module.

A power transmission control device disclosed in JP-A-2006-60909 is implemented by a digital-analog integrated circuit device. In this case, when noise from the digital circuit is transmitted to the analog circuit, the analog circuit may malfunction. On the other hand, when the distance between the digital circuit and the analog circuit is increased in order to reduce an adverse effect of noise, the area of the integrated circuit device increases.

SUMMARY

According to one aspect of the invention, there is provided an integrated circuit device comprising:

a digital power supply regulation circuit that regulates a digital power supply voltage;

an analog power supply regulation circuit that regulates an analog power supply voltage;

a control logic circuit that includes logic cells and operates based on the digital power supply voltage that is regulated by and supplied from the digital power supply regulation circuit;

an analog circuit that includes at least a comparator or an operational amplifier and operates based on the analog power supply voltage that is regulated by and supplied from the analog power supply regulation circuit; and

a power supply wiring region, at least a digital power supply line that supplies the digital power supply voltage that is regulated by the digital power supply regulation circuit and an analog power supply line that supplies the analog power supply voltage that is regulated by the analog power supply regulation circuit being provided in the power supply wiring region,

the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit being disposed in a first direction with respect to the control logic circuit; and

the power supply wiring region being formed along a second direction in a region between the control logic circuit and the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit, the second direction being a direction perpendicular to the first direction.

According to another aspect of the invention, there is provided an integrated circuit device comprising:

a control logic circuit that includes logic cells and operates based on a digital power supply voltage;

an analog circuit that includes at least a comparator or an operational amplifier and operates based on an analog power supply voltage;

a power supply wiring region, a power supply line being provided in the power supply wiring region;

a first predriver that drives a first N-type power MOS transistor of a first external driver, the first external driver including the first N-type power MOS transistor and a first P-type power MOS transistor;

a second predriver that drives the first P-type power MOS transistor of the first external driver,

the analog circuit being disposed in a first direction with respect to the control logic circuit;

the power supply wiring region being formed along a second direction in a region between the control logic circuit and the analog circuit, the second direction being a direction perpendicular to the first direction; and

the first predriver and the second predriver being disposed in a third direction with respect to the power supply wiring region, the third direction being a direction that is opposite to the first direction.

According to another aspect of the invention, there is provided an electronic instrument comprising the above integrated circuit device.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 shows an arrangement configuration example of an integrated circuit device according to one embodiment of the invention.

FIG. 2 shows an arrangement configuration example of an integrated circuit device according to a first modification.

FIG. 3 shows an arrangement configuration example of an integrated circuit device according to a second modification.

FIG. 4 shows an arrangement configuration example of an integrated circuit device according to a third modification.

FIG. 5 shows an arrangement configuration example of a predriver.

FIGS. 6A and 6B are views illustrative of an external driver, a predriver, and a unit transistor.

FIG. 7 shows a detailed arrangement configuration example of a predriver.

FIG. 8 is a view illustrative of a gate control circuit.

FIG. 9 shows a detailed configuration example of a gate control circuit.

FIG. 10 shows a detailed layout example of a predriver.

FIG. 11 is a view illustrative of a power transmission driver (external driver) and a resonant circuit.

FIG. 12 shows a detailed arrangement configuration example of a predriver.

FIGS. 13A and 13B are views illustrative of non-contact power transmission.

FIG. 14 is a configuration example of a power transmission device, a power transmission control device, a power reception device, and a power reception control device.

FIGS. 15A and 15B are views illustrative of data transfer by means of frequency modulation and load modulation.

FIG. 16 is a configuration example of a waveform detection circuit.

FIG. 17 shows a configuration example of a temperature detection circuit.

FIGS. 18A and 18B show signal waveform examples illustrative of the operation of a temperature detection circuit.

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FIG. 19 shows a layout example of an integrated circuit device which implements a power transmission control device.

FIG. 20 shows a layout example of an integrated circuit device which implements a power reception control device.

DETAILED DESCRIPTION OF THE EMBODIMENT

Some aspects of the invention may provide an integrated circuit device which enables an increase in layout efficiency while reducing an adverse effect of noise, and an electronic instrument including the same.

According to one embodiment of the invention, there is provided an integrated circuit device comprising:

a digital power supply regulation circuit that regulates a digital power supply voltage;

an analog power supply regulation circuit that regulates an analog power supply voltage;

a control logic circuit that includes logic cells and operates based on the digital power supply voltage that is regulated by and supplied from the digital power supply regulation circuit;

an analog circuit that includes at least a comparator or an operational amplifier and operates based on the analog power supply voltage that is regulated by and supplied from the analog power supply regulation circuit; and

a power supply wiring region, at least a digital power supply line that supplies the digital power supply voltage that is regulated by the digital power supply regulation circuit and an analog power supply line that supplies the analog power supply voltage that is regulated by the analog power supply regulation circuit being provided in the power supply wiring region,

the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit being disposed in a first direction with respect to the control logic circuit; and

the power supply wiring region being formed along a second direction in a region between the control logic circuit and the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit, the second direction being a direction perpendicular to the first direction.

According to this embodiment, the power supply wiring region is formed between the control logic circuit and the analog circuit. Therefore, the distance between the control logic circuit and the analog circuit can be increased effectively utilizing the width of the power supply wiring region in the first direction, whereby a reduction in adverse effect of noise and an increase in layout efficiency can be achieved in combination.

In the integrated circuit device,

the analog circuit may be disposed in the second direction with respect to the digital power supply regulation circuit, and the analog power supply regulation circuit may be disposed in the second direction with respect to the analog circuit.

This enables the power supply lines to be efficiently connected to the analog circuit and the control logic circuit.

In the integrated circuit device,

a first power supply pad may be disposed in a fourth direction with respect to the digital power supply regulation circuit, the fourth direction being a direction that is opposite to the second direction, a power supply voltage that is regulated by the digital power supply regulation circuit being input to the first power supply pad; and

a second power supply pad may be disposed in the second direction with respect to the analog power supply regulation

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circuit, a power supply voltage that is regulated by the analog power supply regulation circuit being input to the second power supply pad.

This enables the power supply lines from the first power supply pad and the second power supply pad to be connected to the digital power supply regulation circuit and the analog power supply regulation circuit along short paths, whereby layout efficiency can be increased.

In the integrated circuit device,

the integrated circuit device may further include a reset circuit that generates a reset signal and outputs the reset signal to each circuit of the integrated circuit device,

the reset circuit may be disposed between the digital power supply regulation circuit and the analog circuit.

This reduces an adverse effect of digital noise on the analog circuit utilizing the arrangement of the reset circuit.

In the integrated circuit device,

the integrated circuit device may further include a temperature detection circuit that operates based on the digital power supply voltage that is regulated by and supplied from the digital power supply regulation circuit and performs a temperature detection process,

the temperature detection circuit may be disposed between the digital power supply regulation circuit and the analog circuit.

This reduces the effect of noise from the temperature detection circuit on the analog circuit, whereby deterioration in performance of the analog circuit can be prevented.

In the integrated circuit device,

the temperature detection circuit may include:

a reference measurement transistor that is provided in series with a reference resistor between an oscillation node that is a node at one end of a reference capacitor and a digital power supply;

a capacitor temperature measurement transistor that is provided in series with a capacitor temperature measurement thermistor between the oscillation node and the digital power supply;

an ambient temperature measurement transistor that is provided in series with an ambient temperature measurement thermistor between the oscillation node and the digital power supply;

a discharge transistor, a drain of the discharge transistor being connected to the oscillation node; and

a detection circuit that outputs a detection pulse when a voltage of the oscillation node has exceeded a given threshold voltage.

According to this configuration, the capacitor temperature and the ambient temperature can be accurately measured by CR oscillation utilizing the reference resistor, the capacitor temperature measurement thermistor, and the ambient temperature measurement thermistor.

In the integrated circuit device,

the integrated circuit device may further include:

a first predriver that drives a first N-type power MOS transistor of a first external driver that includes the first N-type power MOS transistor and a first P-type power MOS transistor; and

a second predriver that drives the first P-type power MOS transistor of the first external driver,

the first predriver and the second predriver may be disposed in a third direction with respect to the power supply wiring region, the third direction being a direction that is opposite to the first direction.

According to another embodiment of the invention, there is provided an integrated circuit device comprising:

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a control logic circuit that includes logic cells and operates based on a digital power supply voltage;

an analog circuit that includes at least a comparator or an operational amplifier and operates based on an analog power supply voltage;

a power supply wiring region, a power supply line being provided in the power supply wiring region;

a first predriver that drives a first N-type power MOS transistor of a first external driver, the first external driver including the first N-type power MOS transistor and a first P-type power MOS transistor;

a second predriver that drives the first P-type power MOS transistor of the first external driver,

the analog circuit being disposed in a first direction with respect to the control logic circuit;

the power supply wiring region being formed along a second direction in a region between the control logic circuit and the analog circuit, the second direction being a direction perpendicular to the first direction; and

the first predriver and the second predriver being disposed in a third direction with respect to the power supply wiring region, the third direction being a direction that is opposite to the first direction.

According to this embodiment, since the first predriver, the second predriver, and the control logic circuit which produce noise can be collectively disposed in the third direction with respect to the power supply wiring region, a reduction in adverse effect of noise and an increase in layout efficiency can be achieved in combination.

In the integrated circuit device,

a low-potential-side power supply line and a high-potential-side power supply line of the first predriver and the second predriver may be separated from a low-potential-side power supply line and a high-potential-side power supply line of other circuits of the integrated circuit device.

This prevents a situation in which noise produced by the first predriver and the second predriver is transmitted to other circuits through the low-potential-side power supply line and the high-potential-side power supply line.

In the integrated circuit device,

a first N-type transistor and a first P-type transistor that form the first predriver may be disposed in an arrangement region of the first predriver;

a second N-type transistor and a second P-type transistor that form the second predriver may be disposed in an arrangement region of the second predriver;

each of the first N-type transistor, the first P-type transistor, the second N-type transistor, and the second P-type transistor may include a plurality of unit transistors that are connected in parallel; and

the integrated circuit device may further include:

a first N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first N-type transistor;

a first P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first P-type transistor;

a second N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second N-type transistor; and

a second P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second P-type transistor.

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This enables the first N-type transistor, the first P-type transistor, the second N-type transistor, and the second P-type transistor to be minutely ON/OFF-controlled using the gate control signals.

In the integrated circuit device,

the first N-type gate control circuit may output gate control signals that turn ON the plurality of unit transistors of the first N-type transistor at different timings when the first N-type transistor turns ON, and the first N-type gate control circuit may output gate control signals that turn OFF the plurality of unit transistors of the first N-type transistor at the same timing when the first N-type transistor turns OFF;

the first P-type gate control circuit may output gate control signals that turn ON the plurality of unit transistors of the first P-type transistor at different timings when the first P-type transistor turns ON, and the first P-type gate control circuit may output gate control signals that turn OFF the plurality of unit transistors of the first P-type transistor at the same timing when the first P-type transistor turns OFF;

the second N-type gate control circuit may output gate control signals that turn ON the plurality of unit transistors of the second N-type transistor at different timings when the second N-type transistor turns ON, and the second N-type gate control circuit may output gate control signals that turn OFF the plurality of unit transistors of the second N-type transistor at the same timing when the second N-type transistor turns OFF; and

the second P-type gate control circuit may output gate control signals that turn ON the plurality of unit transistors of the second P-type transistor at different timings when the second P-type transistor turns ON, and the second P-type gate control circuit may output gate control signals that turn OFF the plurality of unit transistors of the second P-type transistor at the same timing when the second P-type transistor turns OFF.

This reduces overshoot noise produced when the first N-type transistor, the first P-type transistor, the second N-type transistor, and the second P-type transistor are turned ON while preventing occurrence of a shoot-through current.

In the integrated circuit device,

the integrated circuit device may further include:

a third predriver that drives a second N-type power MOS transistor of a second external driver that includes the second N-type power MOS transistor and a second P-type power MOS transistor; and

a fourth predriver that drives the second P-type power MOS transistor of the second external driver,

the first predriver and the second predriver may be disposed along a first side of the integrated circuit device;

the third predriver and the fourth predriver may be disposed along a second side of the integrated circuit device, the second side intersecting the first side; and

the analog circuit may be disposed along a fourth side that is opposite to the second side.

This makes it possible to collectively dispose the first to fourth predrivers in the corner area of the integrated circuit device formed by the first and second sides. Therefore, the first to fourth predriver can be easily separated from other circuits with regard to the power supply or the like, whereby an adverse effect of noise produced by the first to fourth predrivers on other circuits can be suppressed.

In the integrated circuit device,

the control logic circuit may control the first predriver, the second predriver, the third predriver, and the fourth predriver, and the control logic circuit may be disposed in the second direction with respect to the first predriver and the second

pre-driver and in the first direction with respect to the third pre-driver and the fourth pre-driver.

This enables the signal lines to be provided between the control logic circuit and the first and second pre-drivers along short paths, whereby layout efficiency can be increased.

In the integrated circuit device,

the integrated circuit device may be provided in a power transmission device of a non-contact power transmission system, the non-contact power transmission system transmitting power from the power transmission device to a power reception device by electromagnetically coupling a primary coil and a secondary coil and supplying power to a load of the power reception device,

the first external driver may be a first power transmission driver that drives one end of the primary coil; and

the second external driver may be a second power transmission driver that drives the other end of the primary coil.

This enables the first and second power transmission drivers of the non-contact power transmission system to be efficiently driven, whereby an increase in power transmission efficiency and the like can be achieved.

According to another embodiment of the invention, there is provided an electronic instrument comprising one of the above integrated circuit devices.

Preferred embodiments of the invention are described in detail below. Note that the embodiments described below do not in any way limit the scope of the invention defined by the claims laid out herein. Note that all elements of the embodiments described below should not necessarily be taken as essential requirements for the invention.

1. Integrated Circuit Device

FIG. 1 shows a configuration example of an integrated circuit device according to one embodiment of the invention. In FIG. 1, a direction along a first side SD1 of the integrated circuit device is referred to as a first direction D1, and a direction perpendicular to the first direction is referred to as a second direction D2. A direction opposite to the first direction D1 is referred to as a third direction D3, and a direction opposite to the second direction D2 is referred to as a fourth direction D4. FIG. 1 shows an example in which the direction D1 is a rightward direction and the direction D3 is a leftward direction. Note that the direction D1 may be a leftward direction and the direction D3 may be a rightward direction. FIG. 1 shows an example in which the direction D2 is a downward direction and the direction D4 is an upward direction. Note that the direction D2 may be an upward direction and the direction D4 may be a downward direction.

The integrated circuit device shown in FIG. 1 includes a digital power supply regulation circuit 30, an analog power supply regulation circuit 32, a control logic circuit 110, an analog circuit 120, and a power supply wiring region PWRG.

The digital power supply regulation circuit 30 (digital power supply regulator or digital constant voltage generation circuit) regulates a digital power supply (digital power supply voltage or logic power supply voltage). Specifically, the digital power supply regulation circuit 30 regulates a 5 V digital power supply voltage VDD5 input from the outside, and outputs a digital power supply voltage VDD3 at a stable potential of 3 V, for example.

The analog power supply regulation circuit 32 (analog power supply regulator or analog constant voltage generation circuit) regulates an analog power supply (analog power supply voltage). Specifically, the analog power supply regulation circuit 32 regulates a 5 V analog power supply voltage VD5A input from the outside, and outputs an analog power supply voltage VD45A at a stable potential of 4.5 V, for example.

A series regulator may be employed as the digital power supply regulation circuit 30 and the analog power supply regulation circuit 32, for example. The series regulator may include a driver transistor which is provided between a high-potential-side power supply and an output node, a voltage divider circuit which is provided between the output node and a low-potential-side power supply and divides the output voltage using a resistor, an operational amplifier of which a first input terminal (e.g., non-inverting input terminal) is provided with a reference voltage, a second input terminal (e.g., inverting input terminal) is provided with the resistor-divided voltage from the voltage divider circuit, and an output terminal is connected to the gate of the driver transistor, and the like. The analog power supply regulation circuit 32 may be a circuit which generates an analog ground voltage GND and supplies the analog ground voltage GND to the analog circuit 120.

The control logic circuit 110 is a circuit which includes logic cells such as a NAND circuit, a NOR circuit, an inverter, and a D flip-flop, and operates based on the digital power supply voltage VDD3 which is regulated by and supplied from the digital power supply regulation circuit 30. The control logic circuit 110 may be implemented by a gate array, a microcomputer, or the like. The control logic circuit 110 performs sequence control and a determination process. The control logic circuit 110 controls each circuit of the integrated circuit device, and controls the entire integrated circuit device.

The analog circuit 120 is a circuit which includes a comparator, an operational amplifier, and the like, and operates based on the analog power supply voltage VD45A which is regulated by and supplied from the analog power supply regulation circuit 32. Specifically, the analog circuit 120 performs an analog process using one or more comparators and one or more operational amplifiers. More specifically, the analog circuit 120 may include a detection circuit which performs various detection processes such as amplitude detection (peak detection), pulse width detection, phase detection, and frequency detection, a determination circuit which performs a determination process using an analog voltage, an amplifier circuit which amplifies an analog signal, a current-mirror circuit, an A/D conversion circuit which converts an analog voltage into a digital voltage, and the like.

A digital power supply line which supplies the digital power supply voltage VDD3 regulated by the digital power supply regulation circuit 30 and an analog power supply line which supplies the analog power supply voltage VD45A regulated by the analog power supply regulation circuit 32 are provided in the power supply wiring region PWRG. A power supply line which supplies a power supply voltage at a potential differing from those of the digital power supply voltage VDD3 and the analog power supply voltage VD45A may also be provided in the power supply wiring region PWRG. For example, a low-potential-side digital power supply line and a low-potential-side analog power supply line may be provided in the power supply wiring region PWRG. A power supply line which supplies a power supply voltage at a potential higher than that of the digital power supply voltage VDD3 and a power supply line which supplies a power supply voltage at a potential higher than that of the analog power supply voltage VD45A may also be provided in the power supply wiring region PWRG.

In the integrated circuit device according to this embodiment, the digital power supply regulation circuit 30, the analog circuit 120, and the analog power supply regulation circuit 32 are disposed in the direction D1 with respect to the control logic circuit 110. For example, the analog circuit 120 is dis-

posed in the direction D2 with respect to the digital power supply regulation circuit 30, and the analog power supply regulation circuit 32 is disposed in the direction D2 with respect to the analog circuit 120. Note that modifications may be made such as disposing these circuits in an arrangement order differing from that shown in FIG. 1 or omitting some elements such as the digital power supply regulation circuit 30 and the analog power supply regulation circuit 32, for example.

The power supply wiring region PWRG is formed along the direction D2 in a region between the control logic circuit 110 and the digital power supply regulation circuit 30, the analog circuit 120, and the analog power supply regulation circuit 32. Specifically, the power supply wiring region PWRG is linearly formed along the direction D2 from the side SD1 toward a side SD3 of the integrated circuit device, for example. The power supply voltages branched from the power supply wiring region PWRG are supplied to the control logic circuit 110, the analog circuit 120, and various other circuits (not shown).

According to the configuration shown in FIG. 1, the power supply wiring region PWRG is formed between the control logic circuit 110 and the analog circuit 120. Therefore, the distance between the control logic circuit 110 and the analog circuit 120 can be increased utilizing the width of the power supply wiring region PWRG in the direction D1. Specifically, a region in the direction D3 with respect to the power supply wiring region PWRG is utilized as a digital circuit region and a region in the direction D1 with respect to the power supply wiring region PWRG is utilized as an analog circuit region so that the digital circuit and the analog circuit can be separately disposed at an increased distance. This prevents a situation in which switching noise from the digital circuit such as the control logic circuit 110 is transmitted to the analog circuit 120 and causes malfunction or deterioration in performance of the analog circuit 120, for example.

In FIG. 1, the power supply wiring region PWRG is utilized as a noise separation region between the digital circuit region and the analog circuit region. This configuration has an advantage in that an increase in layout efficiency and noise separation can be achieved in combination. Specifically, since the wiring resistance of the power supply line provided in the power supply wiring region PWRG must be reduced as compared with a normal signal line, the width of the power supply line provided in the power supply wiring region PWRG is greater than that of a normal signal line. Therefore, the width of the power supply wiring region PWRG in the direction D1 can be increased by providing a plurality of power supply lines having a large width in the direction D1 in the power supply wiring region PWRG along the direction D2. This makes it possible to sufficiently separate the digital circuit region and the analog circuit region by a distance necessary for noise separation. The distance for noise separation can be increased and the parasitic resistance of the power supply line can be reduced by increasing the width of the power supply line in the direction D1. Moreover, layout efficiency does not deteriorate because it is originally necessary to provide the power supply line along the direction D2.

Since necessary power supply lines can be efficiently provided to each circuit disposed on either side of the power supply wiring region PWRG by linearly forming the power supply wiring region PWRG from the first side SD1 of the integrated circuit device toward the third side SD3 opposite to the first side SD1, layout efficiency can be increased.

As a comparative example, a method may be considered in which a digital power supply line and an analog power supply line are provided in the shape of a ring around a core circuit of

the integrated circuit device. According to this method, since at least two power supply lines (high-potential-side power supply lines) must be provided as the digital power supply line and the analog power supply line along the four sides SD1, SD2, SD3, and SD4 of the integrated circuit device, the chip area of the integrated circuit device increases.

According to the arrangement method shown in FIG. 1, since the digital power supply line and the analog power supply line are provided in the power supply wiring region PWRG, the width of the integrated circuit device increases due to these power supply lines only in the direction D1. Therefore, the arrangement method shown in FIG. 1 can increase the layout efficiency as compared with the method in which the power supply lines are provided in the shape of a ring.

In FIG. 1, a first power supply pad, to which the power supply voltage VDD5 regulated by the digital power supply regulation circuit 30 is input, is disposed in the direction D4 with respect to the digital power supply regulation circuit 30. A second power supply pad, to which the power supply voltage VD5A regulated by the analog power supply regulation circuit 32 is input, is disposed in the direction D2 with respect to the analog power supply regulation circuit 32. This enables the power supply voltages VDD5 and VD5A to be respectively supplied to the digital power supply regulation circuit 30 and the analog power supply regulation circuit 32 along short paths. This makes it unnecessary to provide the power supply lines of the power supply voltages VDD5 and VD5A around the core region of the integrated circuit device, whereby layout efficiency can be increased.

Specifically, the power supply line of the power supply voltage VDD5 can be connected from the power supply pad to the digital power supply regulation circuit 30 along a short path. The power supply voltage VDD5 is regulated by the digital power supply regulation circuit 30, and the power supply voltage VDD3 obtained by regulation can be supplied along the direction D2 in the power supply wiring region PWRG. Likewise, the power supply line of the power supply voltage VD5A can be connected from the power supply pad to the analog power supply regulation circuit 32 along a short path. The power supply voltage VD5A is regulated by the analog power supply regulation circuit 32, and the power supply voltage VD45A obtained by regulation can be supplied along the direction D2 in the power supply wiring region PWRG. This minimizes the wiring region required for the power supply lines of the power supply voltages VDD5 and VD5A, whereby layout efficiency can be increased. In this case, the analog circuit 120 is disposed between the digital power supply regulation circuit 30 and the analog power supply regulation circuit 32. Therefore, the power supply lines of the power supply voltages VDD3 and VD45A obtained by regulation can be efficiently provided from the digital power supply regulation circuit 30 and the analog power supply regulation circuit 32 to the control logic circuit 110 and the analog circuit 120.

2. First Modification

FIG. 2 shows an arrangement configuration example of an integrated circuit device according to a first modification of this embodiment. FIG. 2 differs from FIG. 1 in that a temperature detection circuit 38 and a reset circuit 39 are further provided. Note that a modification may be made in which the temperature detection circuit 38 or the reset circuit 39 is omitted.

The temperature detection circuit 38 is a circuit which operates based on the digital power supply voltage VDD3 regulated by and supplied from the digital power supply regulation circuit 30, and performs a temperature detection pro-

cess. For example, the temperature detection circuit 38 detects the temperature of a capacitor to detect an abnormality (failure) in $\tan \delta$ of the capacitor. Examples of the capacitor include a capacitor which forms a resonant circuit with a primary coil in a non-contact power transmission system described later, and the like.

The reset circuit 39 generates a reset signal and outputs the generated reset signal to each circuit of the integrated circuit device. Specifically, the reset circuit 39 monitors the power supply voltage input from the outside, the digital power supply (logic power supply) voltage regulated by the digital power supply regulation circuit 30, and the analog power supply voltage regulated by the analog power supply regulation circuit 32. The reset circuit 39 cancels the reset signal when these power supply voltages have appropriately risen so that each circuit of the integrated circuit device starts an operation to implement a power-on reset.

In FIG. 2, the temperature detection circuit 38 is disposed between the digital power supply regulation circuit 30 and the analog circuit 120. Specifically, the temperature detection circuit 38 is disposed between the digital power supply regulation circuit 30 and the reset circuit 39. According to this configuration, since the temperature detection circuit 38 can be disposed near the digital power supply regulation circuit 30, the constant power supply voltage VDD3 from the digital power supply regulation circuit 30 can be stably supplied to the temperature detection circuit 38. For example, when employing an RF converter using a CR oscillation circuit described later as the temperature detection circuit 38, the measurement time changes when the power supply voltage VDD3 changes, whereby the measured temperature changes. On the other hand, the power supply line of the power supply voltage VDD3 from the digital power supply regulation circuit 30 can be provided to the temperature detection circuit 38 along a short path by disposing the temperature detection circuit 38 adjacently to the digital power supply regulation circuit 30, as shown in FIG. 2, whereby the parasitic resistance of the power supply line can be minimized. This prevents a change in measurement in the RF converter so that a temperature can be stably detected.

In FIG. 2, the reset circuit 39 is disposed between the digital power supply regulation circuit 30 and the analog circuit 120. The reset circuit 39 operates only during power-on reset (initialization), but does not operate during a normal operation. Therefore, even if the reset circuit 39 (i.e., digital circuit) is disposed near the analog circuit 120, the analog circuit 120 is adversely affected by digital noise to a minimum extent. In FIG. 2, the reset circuit 39 is disposed between the temperature detection circuit 38 and the analog circuit 120. Therefore, the distance between the analog circuit 120 and the temperature detection circuit 38 can be increased utilizing the width of the reset circuit 39 in the direction D2. This suppresses the analog circuit 120 from being affected by noise due to CR oscillation of the temperature detection circuit 38 or the like, whereby a deterioration in performance of the analog circuit 120 can be prevented.

3. Second Modification

FIG. 3 shows an arrangement configuration example of an integrated circuit device according to a second modification of this embodiment. FIG. 3 differs from FIGS. 1 and 2 in that predrivers PR1 and PR2 are further provided. FIG. 3 shows an example in which the predrivers PR1 and PR2 are disposed along the side SD1 of the integrated circuit device. Note that the predrivers may be disposed along the side SD2 perpendicular to the side SD1.

In FIG. 3, a first external driver DR1 is provided outside the integrated circuit device, for example. The external driver

DR1 includes an N-type power MOS transistor PTN1 (N-type transistor or N-type MOS transistor in a broad sense) and a P-type power MOS transistor PTP1 (P-type transistor or P-type MOS transistor in a broad sense) as external parts. The external driver DR1 may be various drivers such as a power transmission driver which drives a primary coil in non-contact power transmission or a motor driver which drives a motor.

The predriver PR1 drives the N-type power MOS transistor PTN1 of the external driver DR1. Specifically, an inverter circuit which includes an N-type transistor and a P-type transistor may be used as the predriver PR1. An output signal DN1 from the predriver PR1 is input to the gate of the N-type power MOS transistor PTN1 through an output pad so that the transistor PTN1 is ON/OFF-controlled.

The predriver PR2 drives the P-type power MOS transistor PTP1 of the external driver DR1. Specifically, an inverter circuit which includes an N-type transistor and a P-type transistor may be used as the predriver PR2. An output signal DP1 from the predriver PR2 is input to the gate of the P-type power MOS transistor PTP1 through an output pad so that the transistor PTP1 is ON/OFF-controlled.

The output signals DN1 and DP1 are non-overlap signals of which the active periods do not overlap. This prevents a situation in which a shoot-through current flows from the high-potential-side power supply to the low-potential-side power supply through the transistors.

In FIG. 3, when a direction opposite to the direction D1 is referred to as the direction D3, the analog circuit 120 is disposed in the direction D1 with respect to the power supply wiring region PWRG, and the first and second predrivers PR1 and PR2 are disposed in the direction D3 with respect to the power supply wiring region PWRG. Specifically, the predrivers PR1 and PR2 are disposed in a digital circuit region in the direction D3 with respect to the power supply wiring region PWRG together with the control logic circuit 110.

According to this configuration, the predrivers PR1 and PR2 and the control logic circuit 110 which generate digital switching noise can be collectively disposed in the direction D3 with respect to the power supply wiring region PWRG. Therefore, noise generated from the predrivers PR1 and PR2 and the control logic circuit 110 can be effectively prevented from being transmitted to the analog circuit 120 and the like utilizing the width of the power supply wiring region PWRG in the direction D1. Moreover, since the digital power supply lines with large switching noise can be collectively provided in the digital circuit region, layout efficiency can be increased. According to the arrangement configuration shown in FIG. 3, it becomes easy to mount the power MOS transistors PTN1 and PTP1 of the external driver DR1 on the circuit board and to provide lines on the circuit board, so that the size of the circuit board can be reduced.

4. Third Modification

FIG. 4 shows an arrangement configuration example of an integrated circuit device according to a third modification of this embodiment. FIG. 4 differs from FIG. 3 in that predrivers PR3 and PR4 are further provided.

In FIG. 4, a second external driver DR2 includes a second N-type power MOS transistor PTN2 and a second P-type power MOS transistor PTP2. The predriver PR3 drives the transistor PTN2 of the external driver DR2, and the predriver PR4 drives the transistor PTP2.

In FIG. 4, the first and second predrivers PR1 and PR2 are disposed along the first side SD1 of the integrated circuit device. The third and fourth predrivers PR3 and PR4 are disposed along the second side SD2 of the integrated circuit device. The side SD2 is a side which perpendicularly inter-

sects the side SD1. Specifically, the side SD1 is a side along the direction D1, and the side SD2 is a side along the direction D2. The corner of the integrated circuit device is formed by the sides SD1 and SD2. The predrivers PR1 to PR4 are disposed in the corner area of the integrated circuit device.

According to the arrangement shown in FIG. 4, the predrivers PR1, PR2, PR3, and PR4 can be easily separated from other circuits with regard to power supply. Therefore, layout efficiency relating to the power supply lines and the like can be increased, whereby the chip area can be reduced. Moreover, an adverse effect of noise on other circuits can be minimized by collectively disposing the predrivers PR1 to PR4 in the corner area.

5. Predriver

An arrangement configuration example of the predriver according to this embodiment is described below. In FIG. 5, the integrated circuit device includes the first and second predrivers PR1 and PR2. The integrated circuit device also includes a low-potential-side power supply pad PVSS1, a first output pad PDN1, a second output pad PDP1, and a high-potential-side power supply pad PVDD1. These pads (electrodes or terminals) are disposed along the first side SD1 of the integrated circuit device, for example.

The power supply pad PVSS1 is a pad through which a low-potential-side power supply voltage VSS1 is supplied to the predrivers PR1 and PR2. Specifically, a low-potential-side power supply line VSL1 of the predrivers PR1 and PR2 is connected to the power supply pad PVSS1 via a first connection line CL1. The power supply voltage VSS1 is also used as a low-potential-side power supply voltage of the external driver DR1. A power supply line of the power supply voltage VSS1 is connected to the source of the transistor PTN1 using a line provided on the circuit board.

The pad PDN1 is a pad through which the output signal DN1 from the predriver PR1 is output. Specifically, a first output line QL1 of the predriver PR1 is connected to the pad PDN1 through a second connection line CL2, and the signal DN1 is output to the outside through the first output line QL1, the second connection line CL2, and the pad PDN1.

The pad PDP1 is a pad through which the output signal DP1 from the predriver PR2 is output. Specifically, a second output line QL2 of the predriver PR2 is connected to the pad PDP1 through a third connection line CL3, and the signal DP1 is output to the outside through the second output line QL2, the third connection line CL3, and the pad PDP1.

The power supply pad PVDD1 is a pad through which a high-potential-side power supply VDD1 is supplied to the predrivers PR1 and PR2. Specifically, a high-potential-side power supply line VDL1 of the predrivers PR1 and PR2 is connected to the power supply pad PVDD1 through a fourth connection line CL4. The power supply voltage VDD1 is also used as a high-potential-side power supply voltage of the external driver DR1. A power supply line of the power supply voltage VDD1 is connected to the source of the transistor PTP1 using a line on the circuit board.

In this embodiment, the low-potential-side power supply pad PVSS1, the first and second output pads PDN1 and PDP1, and the high-potential-side power supply pad PVDD1 are disposed along the direction D1, as shown in FIG. 5. Specifically, the output pad PDN1 is disposed in the direction D1 with respect to the power supply pad PVSS1, the output pad PDP1 is disposed in the direction D1 with respect to the output pad PDN1, and the power supply pad PVDD1 is disposed in the direction D1 with respect to the output pad PDP1.

When a direction perpendicular to the direction D1 is referred to as the direction D2, the predriver PR1 is disposed in the direction D2 with respect to the power supply pad

PVSS1 and the output pad PDN1. The predriver PR2 is disposed in the direction D2 with respect to the output pad PDP1 and the power supply pad PVDD1.

FIG. 6A shows a circuit configuration example of the predrivers PR1 and PR2. The predriver PR1 includes a P-type transistor TP1 and an N-type transistor TN1. The power supply voltage VDD1 is supplied to the source of the transistor TP1, and the power supply voltage VSS1 is supplied to the source of the transistor TN1. The predriver PR2 includes a P-type transistor TP2 and an N-type transistor TN2. The power supply voltage VDD1 is supplied to the source of the transistor TP2, and the power supply voltage VSS1 is supplied to the source of the transistor TN2.

The power MOS transistors PTP1 and PTN1 of the external driver DR1 have a very large transistor size. Therefore, a very large shoot-through current flows when a period in which the transistors PTP1 and PTN1 are simultaneously turned ON occurs. Accordingly, the transistor PTN1 must be reliably turned OFF when the output signal DP1 from the predriver PR2 is set at the L level so that the transistor PTP1 is turned ON. In order to reliably turn OFF the transistor PTN1, nodes NF1 and NF2 must be set at the same potential. Therefore, it is desirable to minimize the parasitic resistances of lines indicated by A1 and A2.

Likewise, the transistor PTP1 must be reliably turned OFF when the output signal DN1 from the predriver PR1 is set at the H level so that the transistor PTN1 is turned ON. Therefore, nodes NF3 and NF4 must be set at the same potential. Accordingly, it is desirable to minimize the parasitic resistances of lines indicated by A3 and A4.

In this embodiment, the pads PVSS1, PDN1, PDP1, and PVDD1 are provided in that order along the direction D1, as shown in FIG. 5. The predriver PR1 is disposed in the direction D2 with respect to the pads PVSS1 and PDN1, and the predriver PR2 is disposed in the direction D2 with respect to the pads PDP1 and PVDD1. Therefore, the length of the line from the pad PVSS1 to the predriver PR1 and the length of the line from the pad PDN1 to the predriver PR1 can be reduced, whereby the parasitic resistances of the lines indicated by A1 and A2 in FIG. 6A can be minimized. This enables the transistor PTN1 to be reliably turned OFF in a period in which the transistor PTP1 is turned ON, whereby occurrence of a shoot-through current can be prevented.

Likewise, the length of the line from the pad PVDD1 to the predriver PR2 and the length of the line from the pad PDP1 to the predriver PR2 can be reduced, whereby the parasitic resistances of the lines indicated by A3 and A4 in FIG. 6A can be minimized. This enables the transistor PTP1 to be reliably turned OFF in a period in which the transistor PTN1 is turned ON, whereby occurrence of a shoot-through current can be prevented.

According to the arrangement configuration shown in FIG. 5, since the area occupied by the pads PVSS1, PDN1, PDP1, and PVDD1 and the predrivers PR1 and PR2 in the direction D2 can be reduced, layout efficiency can be increased.

According to the arrangement configuration shown in FIG. 5, since it is easy to mount the power MOS transistors PTN1 and PTP1 of the external driver DR1 on the circuit board and to provide the lines on the circuit board, a reduction in noise and a reduction in size of the circuit board can be achieved.

FIG. 7 shows a detailed arrangement configuration example of the integrated circuit device and the predriver according to this embodiment. As shown in FIG. 7, the first P-type transistor TP1 and the first N-type transistor TN1 of the first predriver PR1 are disposed along the direction D2 in the arrangement region of the first predriver PR1. Specifically, the transistors TP1 and TN1 are adjacently disposed

along the direction D2. The second P-type transistor TP2 and the second N-type transistor TN2 of the second predriver PR2 are disposed along the direction D2 in the arrangement region of the second predriver PR2. Specifically, the transistors TP2 and TN2 are adjacently disposed along the direction D2. The gates of the transistors TP1, TN1, TP2, and TN2 are provided along the direction D2, as shown in FIG. 6B.

FIG. 7 shows an example in which the P-type transistor and the N-type transistor are disposed in that order along the direction D2. Note that the N-type transistor and the P-type transistor may be disposed in that order along the direction D2.

In FIG. 7, the low-potential-side power supply line VSL1 which supplies the low-potential-side power supply voltage VSS1 to the predrivers PR1 and PR2 is provided in the arrangement regions of the predrivers PR1 and PR2 along the direction D1. The first connection line CL1 (lead line) which connects the low-potential-side power supply pad PVSS1 and the low-potential-side power supply line VSL1 is provided from the power supply pad PVSS1 to a low-potential-side power supply connection node NE1 of the predriver PR1 along the direction D2.

The first output line QL1 connected to the output of the predriver PR1 is provided in the arrangement region of the predriver PR1 along the direction D1. The second connection line CL2 which connects the first output pad PDN1 and the first output line QL1 is provided from the first output pad PDN1 to an output connection node NE2 of the predriver PR1 along the direction D2.

The second output line QL2 connected to the output of the predriver PR2 is provided in the arrangement region of the predriver PR2 along the direction D1. The third connection line CL3 which connects the second output pad PDP1 and the second output line QL2 is provided from the second output pad PDP1 to an output connection node NE3 of the predriver PR2 along the direction D2.

The high-potential-side power supply line VDL1 which supplies the high-potential-side power supply voltage VDD1 to the predrivers PR1 and PR2 is provided in the arrangement regions of the predrivers PR1 and PR2 along the direction D1. The fourth connection line CL4 which connects the high-potential-side power supply pad PVDD1 and the high-potential-side power supply line VDL1 is provided from the high-potential-side power supply pad PVDD1 to a high-potential-side power supply line connection node NE4 of the predriver PR2 along the direction D2.

Note that the connection lines CL1, CL2, CL3, and CL4 may be at least partially provided linearly along the direction D2. For example, the connection lines CL1, CL2, CL3, and CL4 may have a portion provided along the direction D1. The positions of the connection nodes NE1, NE2, NE3, and NE4 are not limited to those shown in FIG. 7. The positions where the power supply lines VSL1 and VDL1 and the output lines QL1 and QL2 are provided are not limited to those shown in FIG. 7. For example, the power supply lines VSL1 and VDL1 and the output lines QL1 and QL2 may be provided in a region outside the transistors TP1, TN1, TP2, and TN2.

The power supply voltage VSS1 can be supplied from the power supply pad PVSS1 to the source of the transistor TN1 along a short path by providing the connection lines CL1 and CL2, the power supply line VSL1, and the output line QL1 as shown in FIG. 7. Moreover, the signal DN1 can be output from the drains of the transistors TP1 and TN1 to the output pad PDN1 along a short path. Therefore, since the parasitic resistances of the lines indicated by A1 and A2 in FIG. 6A can be reduced, a shoot-through current and overshoot noise can be minimized.

The power supply voltage VDD1 can be supplied from the power supply pad PVDD1 to the source of the transistor TP1 along a short path by providing the connection lines CL3 and CL4, the power supply line VDL1, and the output line QL2 as shown in FIG. 7. Moreover, the signal DP1 can be output from the drains of the transistors TP2 and TN2 to the output pad PDP1 along a short path. Therefore, since the parasitic resistances of the lines indicated by A3 and A4 in FIG. 6A can be reduced, a shoot-through current and overshoot noise can be minimized.

Specifically, in order to prevent a shoot-through current while minimizing overshoot noise in the external driver DR1 which operates at a high driving frequency, it is desirable to increase an ON transition period in which the transistors PTP1 and PTN1 transition from an OFF state to an ON state and reduce an OFF transition period in which the transistors PTP1 and PTN1 transition from an ON state to an OFF state, as described later.

Therefore, it is desirable to increase an H level transition period of the signal DN1 in which the transistor TP1 of the predriver PR1 shown in FIG. 6A is turned ON to change the signal DN1 from the L level to the H level, and reduce an L level transition period of the signal DN1 in which the transistor TN1 is turned ON to change the signal DN1 from the H level to the L level. Likewise, it is desirable to increase an L level transition period of the signal DP1 in which the transistor TN2 of the predriver PR2 is turned ON to change the signal DP1 from the H level to the L level, and reduce an H level transition period of the signal DP1 in which the transistor TP2 is turned ON to change the signal DP1 from the L level to the H level.

According to the arrangement configuration shown in FIG. 7, the parasitic resistance of the line indicated by A5 in FIG. 6A increases, and the parasitic resistances of the lines indicated by A1 and A2 decrease. Therefore, since the H level transition period of the signal DN1 increases and the L level transition period of the signal DN1 decreases, the ON transition period of the transistor PTN1 of the external driver DR1 can be increased and the OFF transition period of the transistor PTN1 can be reduced. As a result, overshoot noise can be reduced while reducing a shoot-through current.

According to the arrangement configuration shown in FIG. 7, the parasitic resistance of the line indicated by A6 in FIG. 6A increases, and the parasitic resistances of the lines indicated by A3 and A4 decrease. Therefore, since the L level transition period of the signal DP1 increases and the H level transition period of the signal DP1 decreases, the ON transition period of the transistor PTP1 of the external driver DR1 can be increased and the OFF transition period of the transistor PTP1 can be reduced. As a result, overshoot noise can be reduced while reducing a shoot-through current.

In FIG. 7, the low-potential-side power supply line VSL1 and the high-potential-side power supply line VDL1 of the predrivers PR1 and PR2 are separated from a low-potential-side power supply line and a high-potential-side power supply line of other circuits of the integrated circuit device, as indicated by B1 and B2. Specifically, the power supply lines are disconnected at points indicated by B1 and B2. This prevents a situation in which switching noise (power supply noise) generated by the predrivers PR1 and PR2 through which a large current flows in order to charge/discharge a large parasitic capacitor of the external driver DR1 adversely affects other circuits, or switching noise generated by other circuits adversely affects the operations of the predrivers PR1 and PR2.

In FIG. 7, an electrostatic discharge protection region ESDR1 in which a plurality of predriver electrostatic dis-

charge protection elements are disposed is provided between a region which includes the power supply pad PVSS1, the output pads PDN1 and PDP1, and the power supply pad PVDD1 and a region which includes the predrivers PR1 and PR2. A diode, a thyristor, or the like may be used as the electrostatic discharge protection element, for example. The electrostatic discharge protection elements may be provided in pad units, for example.

An electrostatic discharge protection low-potential-side power supply line VSLES1 which is connected to the low-potential-side power supply pad PVSS1 and supplies the low-potential-side power supply VSS1 to the predriver electrostatic discharge protection element is provided in the electrostatic discharge protection region ESDR1 along the direction D1. An electrostatic discharge protection high-potential-side power supply line VDLES1 which is connected to the high-potential-side power supply pad PVDD1 and supplies the high-potential-side power supply VDD1 to the predriver electrostatic discharge protection element is provided in the electrostatic discharge protection region ESDR1 along the direction D1.

As indicated by B3 and B4 in FIG. 7, the electrostatic discharge protection low-potential-side power supply line VSLES1 and the electrostatic discharge protection high-potential-side power supply line VDLES1 are separated from an electrostatic discharge protection low-potential-side power supply line and an electrostatic discharge protection high-potential-side power supply line of other circuits. Specifically, the power supply lines are disconnected at points indicated by B3 and B4.

This prevents a situation in which switching noise generated by the predrivers PR1 and PR2 is transmitted through the power supply lines VSLES1 and VDLES1 and adversely affects other circuits, or switching noise generated by other circuits adversely affects the operations of the predrivers PR1 and PR2.

6. Gate Control Circuit

The N-type transistor TN1 shown in FIG. 7 may include a plurality of unit transistors TNU1 to TNU5 connected in parallel as shown in FIG. 8, and the P-type transistor TP1 may include a plurality of unit transistors TPU1 to TPU5 connected in parallel. This also applies to the N-type transistor TN2 and the P-type transistor TP2.

As shown in FIG. 6B, the unit transistors TNU1 to TNU5 and TPU1 to TPU5 are transistors of which the gate direction coincides with the direction D2. The power supply voltage VSS1 is supplied to the sources of the unit transistors TNU1 to TNU5, and the power supply voltage VDD1 is supplied to the sources of the unit transistors TPU1 to TPU5. The drains of the unit transistors TNU1 to TNU5 and the drains of the unit transistor TPU1 to TPU5 are connected to an output node NG1 of the signal DN1.

An N-type gate control circuit 100 generates and outputs gate control signals GN1 to GN5. Specifically, the N-type gate control circuit 100 outputs the gate control signals GN1 to GN5 respectively input to the gates of the unit transistors TNU1 to TNU5 of the N-type transistor TN1.

When the N-type gate control circuit 100 causes the N-type transistor TN1 to be turned ON, the N-type gate control circuit 100 outputs the gate control signals GN1 to GN5 which respectively cause the unit transistors TNU1 to TNU5 of the N-type transistor TN1 to be turned ON at different timings. For example, the N-type gate control circuit 100 successively changes the gate control signals GN5, GN4, GN3, GN2, and GN1 from the L level to the H level so that the unit transistors TNU5, TNU4, TNU3, TNU2, and TNU1 are successively turned ON.

When the N-type gate control circuit 100 causes the N-type transistor TN1 to be turned OFF, the N-type gate control circuit 100 outputs the gate control signals GN1 to GN5 which respectively cause the unit transistors TNU1 to TNU5 of the N-type transistor TN1 to be turned OFF at the same timing (including almost the same timing). Specifically, the N-type gate control circuit 100 changes the gate control signal GN1 to GN5 from the H level to the L level at the same timing so that the unit transistors TNU1 to TNU5 are turned OFF at the same timing.

A P-type gate control circuit 102 generates and outputs gate control signals GP1 to GP5. Specifically, the P-type gate control circuit 102 outputs the gate control signals GP1 to GP5 respectively input to the gates of the unit transistors TPU1 to TPU5 of the P-type transistor TP1.

When the P-type gate control circuit 102 causes the P-type transistor TP1 to be turned ON, the P-type gate control circuit 102 outputs the gate control signals GP1 to GP5 which respectively cause the unit transistors TPU1 to TPU5 of the P-type transistor TP1 to be turned ON at different timings. For example, the P-type gate control circuit 102 successively changes the gate control signals GP5, GP4, GP3, GP2, and GP1 from the H level to the L level so that the unit transistors TPU5, TPU4, TPU3, TPU2, and TPU1 are successively turned ON.

When the P-type gate control circuit 102 causes the P-type transistor TP1 to be turned OFF, the P-type gate control circuit 102 outputs the gate control signals GP1 to GP5 which respectively cause the unit transistors TPU1 to TPU5 of the P-type transistor TP1 to be turned OFF at the same timing (including almost the same timing). Specifically, the P-type gate control circuit 102 changes the gate control signal GP1 to GP5 from the L level to the H level at the same timing so that the unit transistors TPU1 to TPU5 are turned OFF at the same timing.

As shown in FIG. 10 described later, the N-type transistor TN2 and the P-type transistor TP2 respectively include unit transistors TNU6 to TNU10 and TPU6 to TPU10 connected in parallel in the same manner as in FIG. 8. The integrated circuit device includes a second N-type gate control circuit 104 which outputs a plurality of gate control signals to the unit transistors TNU6 to TNU10 of the N-type transistor TN2 and a second P-type gate control circuit 106 which outputs a plurality of gate control signals to the unit transistors TPU6 to TPU10 of the P-type transistor TP2. The second N-type gate control circuit 104 and the second P-type gate control circuit 106 are configured and operate in the same manner as the first N-type gate control circuit 100 and the first P-type gate control circuit 102 shown in FIG. 8.

FIG. 9 shows a detailed configuration example of the gate control circuits 100 and 102 (104 and 106). The N-type gate control circuit 100 includes NAND circuits NAN1 to NAN4 and inverter circuits IN11 to IN16. A signal NGATE which ON/OFF-controls the N-type unit transistors TNU1 to TNU5 is input to first input terminals of the NAND circuits NAN1 to NAN4 and the inverter circuit IN16. Outputs from the inverter circuits IN12 to IN15 in the preceding stage are respectively input to second input terminals of the NAND circuits NAN1 to NAN4. Outputs from the NAND circuits NAN1 to NAN4 are respectively input to the inverter circuits IN11 to IN14, and an output from the inverter circuit IN16 is input to the inverter circuit IN15. Outputs from the inverter circuits IN11 to IN15 are respectively used as the gate control signals GN1 to GN5.

The P-type gate control circuit 102 includes NOR circuits NR1 to NR4 and inverter circuits IN21 to IN26. A signal PGATE which ON/OFF-controls the P-type unit transistors

TPU1 to TPU5 is input to first input terminals of the NOR circuits NR1 to NR4 and the inverter circuit IN26. Outputs from the inverter circuits IN22 to IN25 in the preceding stage are respectively input to second input terminals of the NOR circuits NR1 to NR4. Outputs from the NOR circuits NR1 to NR4 are respectively input to the inverter circuits IN21 to IN24, and an output from the inverter circuit IN26 is input to the inverter circuit IN25. Outputs from the inverter circuits IN21 to IN25 are respectively used as the gate control signals GP1 to GP5.

The configuration of the gate control circuit is not limited to the configuration shown in FIG. 9. Various modifications may be made such as omitting some elements or adding other elements. For example, a plurality of stages (e.g., two stages) of inverter circuits which increase the element delay time may be further provided in the subsequent stage of the inverter circuits IN11 to IN15 and IN21 to IN25.

In FIG. 9, when the signal NGATE has changed from the L level to the H level, the signal GN5 changes from the L level to the H level after the element delay time due to the inverter circuits IN16 and IN15 has expired. As a result, since the first and second input terminals of the NAND circuit NAN4 are set at the H level, the signal GN4 changes from the L level to the H level after the element delay time due to the NAND circuit NAN4 and the inverter circuit IN14 has expired. As a result, since the first and second input terminals of the NAND circuit NAN3 are set at the H level, the signal GN3 changes from the L level to the H level after the element delay time due to the NAND circuit NAN3 and the inverter circuit IN13 has expired. In FIG. 9, when the signal NGATE has changed from the L level to the H level, the gate control signals GN5, GN4, GN3, GN2, and GN1 successively change from the L level to the H level in this manner. Therefore, the unit transistors TNU5, TNU4, TNU3, TNU2, and TNU1 are successively turned ON.

On the other hand, when the signal NGATE has changed from the H level to the L level, the signals GN1 to GN5 change from the H level to the L level at the same timing (including almost the same timing). Therefore, the unit transistors TNU1 to TNU5 are turned OFF at the same timing. Specifically, when the signal NGATE has changed from the H level to the L level, the unit transistors TNU1 to TNU5 are turned OFF immediately after the element delay time has expired.

In FIG. 9, when the signal PGATE has changed from the H level to the L level, the signal GP5 changes from the H level to the L level after the element delay time due to the inverter circuits IN26 and IN25 has expired. As a result, since the first and second input terminals of the NOR circuit NR4 are set at the L level, the signal GP4 changes from the H level to the L level after the element delay time due to the NOR circuit NR4 and the inverter circuit IN24 has expired. As a result, since the first and second input terminals of the NOR circuit NR3 are set at the L level, the signal GP3 changes from the H level to the L level after the element delay time due to the NOR circuit NR3 and the inverter circuit IN23 has expired. In FIG. 9, when the signal PGATE has changed from the H level to the L level, the gate control signals GP5, GP4, GP3, GP2, and GP1 successively change from the H level to the L level in this manner. Therefore, the unit transistors TPU5, TPU4, TPU3, TPU2, and TPU1 are successively turned ON.

On the other hand, when the signal PGATE has changed from the L level to the H level, the signals GP1 to GP5 change from the L level to the H level at the same timing (including almost the same timing). Therefore, the unit transistors TPU1 to TPU5 are turned OFF at the same timing. Specifically, when the signal PGATE has changed from the L level to the H

level, the unit transistors TPU1 to TPU5 are turned OFF immediately after the element delay time has expired.

In FIG. 9, when the transistors TP1 and TN1 are turned ON, the unit transistors TPU1 to TPU5 and TNU1 to TNU5 are turned ON at different timings. This reduces overshoot noise (switching noise) which occurs when the transistors TP1 and TN1 are turned ON.

In FIG. 9, when the transistors TP1 and TN1 are turned OFF, the unit transistors TPU1 to TPU5 and TNU1 to TNU5 are turned OFF at the same timing. This ensures that the ON period of the unit transistors TPU1 to TPU5 and the ON period of the unit transistors TPU1 to TPU5 do not overlap, whereby occurrence of a shoot-through current can be prevented.

When the unit transistors are turned ON at different timings, it takes time until all the unit transistors are turned ON. Therefore, a margin of time decreases when the driving frequency increases. On the other hand, a margin of time can be increased when the driving frequency increases by causing the unit transistors to be turned OFF at the same timing while causing the unit transistors to be turned ON at different timings.

FIG. 10 shows a detailed layout example of the predrivers PR1 and PR2. In FIG. 10, the first N-type gate control circuit 100 is disposed in the direction D2 with respect to the unit transistors TNU1 to TNU5 of the first N-type transistor TN1 and the unit transistors TPU1 to TPU5 of the first P-type transistor TP1, and the first P-type gate control circuit 102 is disposed in the direction D4 with respect to the unit transistors TNU1 to TNU5 of the first N-type transistor TN1 and the unit transistors TPU1 to TPU5 of the first P-type transistor TP1. FIG. 10 shows an example in which the transistors TP1 (TPU1 to TPU5) and TN1 (TNU1 to TNU5) are disposed in that order along the direction D2. Note that the transistors TN1 and TP1 may be disposed in that order along the direction D2. In this case, the first P-type gate control circuit 102 is disposed in the direction D2 with respect to the transistors TN1 and TP1, and the first N-type gate control circuit 100 is disposed in the direction D4 with respect to the transistors TN1 and TP1.

In FIG. 10, the second N-type gate control circuit 104 is disposed in the direction D2 with respect to the unit transistors TNU6 to TNU10 of the second N-type transistor TN2 and the unit transistors TPU6 to TPU10 of the second P-type transistor TP2, and the second P-type gate control circuit 106 is disposed in the direction D4 with respect to the unit transistors TNU6 to TNU10 of the second N-type transistor TN2 and the unit transistors TPU6 to TPU10 of the second P-type transistor TP2.

According to the arrangement shown in FIG. 10, gate control signal lines from the gate control circuits 100, 102, 104, and 106 can be connected to the unit transistors TNU1 to TNU5, TPU1 to TPU5, TNU6 to TNU10, and TPU6 to TPU10 along short paths. Therefore, the wiring region between the gate control circuit and the unit transistors can be minimized, whereby the layout area can be reduced. Moreover, since the parasitic resistance and the parasitic capacitance of the gate control signal line can be minimized, ON/OFF control of the transistors described with reference to FIGS. 8 and 9 can be optimized.

In FIG. 10, a plurality of (three) pads electrically connected through an aluminum layer or the like are respectively used as the pads PVSS1, PDN1, PDP1, and PVDD1. The arrangement pitch of the pads in the direction D1 is set to be the same (including almost the same) as the arrangement pitch of the unit transistors in the direction D1. The arrangement pitch of

the electrostatic discharge protection elements (ESD1 to ESD12) is also set to be the same as the arrangement pitch of the unit transistors.

This makes it possible to set the number of unit transistors which drive each power MOS transistor of the external driver at a number corresponding to the size of the power MOS transistor by simply changing the layout. For example, the number of unit transistors arranged in the direction D1 may be decreased when driving a power MOS transistor (external device in a broad sense) with a small size, and the number of unit transistors arranged in the direction D1 may be increased when driving a power MOS transistor with a large size. In FIG. 10, since the arrangement pitch of the pads is the same as the arrangement pitch of the unit transistors, power MOS transistors with various sizes can be driven by merely increasing or decreasing the number of units, each of which includes the pad and the unit transistor (and the electrostatic discharge protection element), arranged in the direction D1. Therefore, an increase in efficiency of the layout design and a reduction in design period can be achieved.

7. Arrangement of Predriver

In a non-contact power transmission system described later, a resonant circuit (series resonant circuit) is formed using a primary coil L1 and a capacitor C1, as shown in FIG. 11. This makes it necessary to provide the external driver DR1 (first power transmission driver) which drives one end of the primary coil L1 and the external driver DR2 (second power transmission driver) which drives the other end of the primary coil L1. Specifically, the capacitor C1 is provided between the output of the external driver DR1 and one end of the primary coil L1, and the output of the external driver DR2 is connected to the other end of the primary coil L1. Note that the configuration of the resonant circuit is not limited to the configuration shown in FIG. 11. For example, resonant capacitors may be provided on both ends of the primary coil L1.

In FIG. 11, the predriver PR1 drives the transistor PTN1 of the external driver DR1, and the predriver PR2 drives the transistor PTP1. The predriver PR3 drives the transistor PTN2 of the external driver DR2, and the predriver PR4 drives the transistor PTP2.

FIG. 12 shows an arrangement configuration example of the predrivers PR1 to PR4. In FIG. 12, the predrivers PR1 and PR2 are disposed along the first side SD1 of the integrated circuit device. The predrivers PR3 and PR4 are disposed along the second side SD2 of the integrated circuit device.

According to the arrangement shown in FIG. 12, the predrivers PR1, PR2, PR3, and PR4 can be easily separated from other circuits with regard to power supply. Specifically, a layout taking power supply separation into consideration is necessary only in areas indicated by D1 and D2 in FIG. 12, and power supply separation need not be taken into consideration in a corner area indicated by D3. Therefore, layout efficiency can be increased. For example, when the power supply is separated in the area indicated by D1, if other circuits are disposed in the area indicated by D3, power supply lines must be provided to these other circuits disposed in the area indicated by D3, whereby layout efficiency deteriorates. Moreover, noise generated by the predriver may adversely affect these other circuits.

In FIG. 12, the predrivers PR1 and PR2 are disposed along the side SD1 in the corner area indicated by D3, and the predrivers PR3 and PR4 are disposed along the side SD2 in the corner area indicated by D3. Therefore, layout efficiency relating to the power supply lines and the like can be increased, whereby the chip area can be reduced. Moreover,

an adverse effect of noise on other circuits can be minimized by collectively disposing the predrivers PR1 to PR4 in the corner area.

In FIG. 12, the control logic circuit 110 which controls the predrivers PR1 to PR4 is disposed in the direction D2 with respect to the predrivers PR1 and PR2 and in the direction D1 with respect to the predrivers PR3 and PR4. The control logic circuit 110 generates the signals NGATE and PGATE shown in FIG. 9 and the like to control the predrivers PR1 to PR4.

This arrangement enables signal lines to be provided between the control logic circuit 110 and the predrivers PR1 to PR4 along short paths, whereby layout efficiency can be increased. Moreover, since the predrivers PR1 to PR4 and the control logic circuit 110 which produce switching noise can be concentrated at a location apart from other circuits, an adverse effect of noise can be minimized. In FIG. 12, the power supply lines of the predrivers PR1 to PR4 are also electrically separated from the power supply lines of the control logic circuit so that a situation in which the predrivers PR1 to PR4 and the control logic circuit 110 are adversely affected by noise generated by the predrivers PR1 to PR4 or the control logic circuit 110 is prevented.

8. Electronic Instrument

FIG. 13A shows an example of electronic instruments in which the integrated circuit device according to this embodiment is used. These electronic instruments can perform non-contact power transmission.

A charger 500 (cradle) (i.e., electronic instrument) includes a power transmission device 10. A portable telephone 510 (i.e., electronic instrument) includes a power reception device 40. The portable telephone 510 includes a display section 512 such as an LCD, an operation section 514 which includes a button and the like, a microphone 516 (sound input section), a speaker 518 (sound output section), and an antenna 520.

Power is supplied to the charger 500 through an AC adaptor 502. The power supplied to the charger 500 is transmitted from the power transmission device 10 to the power reception device 40 by means of non-contact power transmission. This makes it possible to charge a battery of the portable telephone 510 or operate a device provided in the portable telephone 510.

The electronic instrument to which this embodiment is applied is not limited to the portable telephone 510. For example, this embodiment may be applied to various electronic instruments such as a wristwatch, a cordless telephone, a shaver, an electric toothbrush, a wrist computer, a handy terminal, a portable information terminal, and a power-assisted bicycle.

As schematically shown in FIG. 13B, power transmission from the power transmission device 10 to the power reception device 40 is implemented by electromagnetically coupling the primary coil L1 (transmitting coil) provided in the power transmission device 10 and a secondary coil L2 (receiving coil) provided in the power reception device 40 to form a power transmission transformer. This enables non-contact power transmission.

9. Power Transmission Device and Power Reception Device

FIG. 14 shows a configuration example of the power transmission device 10 and the power reception device 40. A power transmission-side electronic instrument such as the charger 500 shown in FIG. 13A includes at least the power transmission device 10 shown in FIG. 14. A power reception-side electronic instrument such as the portable telephone 510 includes at least the power reception device 40 and a load 90 (actual load). The configuration shown in FIG. 14 implements

a non-contact power transmission (contactless power transmission) system in which power is transmitted from the power transmission device **10** to the power reception device **40** by electromagnetically coupling the primary coil **L1** and the secondary coil **L2** and power (voltage **VOUT**) is supplied to the load **90** from a voltage output node **NB7** of the power reception device **40**.

The power transmission device **10** (power transmission module or primary module) may include the primary coil **L1**, a power transmission section **12**, a voltage detection circuit **14**, a display section **16**, and a power transmission control device **20**. The power transmission device **10** and the power transmission control device **20** are not limited to the configuration shown in FIG. **14**. Various modifications may be made such as omitting some elements (e.g., display section and voltage detection circuit), adding other elements, or changing the connection relationship.

The power transmission section **12** generates an alternating-current voltage at a given frequency during power transmission, and generates an alternating-current voltage at a frequency which differs depending on data during data transfer. The power transmission section **12** supplies the generated alternating-current voltage to the primary coil **L1**. As shown in FIG. **15A**, the power transmission section **12** generates an alternating-current voltage at a frequency **f1** when transmitting data "1" to the power reception device **40**, and generates an alternating-current voltage at a frequency **f2** when transmitting data "0" to the power reception device **40**, for example.

The power transmission section **12** may include the first power transmission driver **DR1** (first external driver) which drives one end of the primary coil **L1**, the second power transmission driver **DR2** (second external driver) which drives the other end of the primary coil **L1**, the capacitor **C1** which forms a resonant circuit together with the primary coil **L1**, and the like, as described with reference to FIG. **11**. Each of the first and second power transmission drivers **DR1** and **DR2** included in the power transmission section **12** is an inverter circuit (buffer circuit) which includes a power MOS transistor, for example, and is controlled by a driver control circuit **26** of the power transmission control device **20**.

The primary coil **L1** (power transmission-side coil) is electromagnetically coupled with the secondary coil **L2** (power reception-side coil) to form a power transmission transformer. For example, when power transmission is necessary, the portable telephone **510** is placed on the charger **500** so that a magnetic flux of the primary coil **L1** passes through the secondary coil **L2**, as shown in FIGS. **13A** and **13B**. When power transmission is unnecessary, the charger **500** and the portable telephone **510** are physically separated so that a magnetic flux of the primary coil **L1** does not pass through the secondary coil **L2**.

The voltage detection circuit **14** is a circuit which detects the induced voltage in the primary coil **L1**. The voltage detection circuit **14** includes resistors **RA1** and **RA2** and a diode **DA1** provided between a connection node **NA3** of the resistors **RA1** and **RA2** and **GND** (low-potential-side power supply in a broad sense), for example.

The voltage detection circuit **14** functions as a half-wave rectifier circuit for a coil end voltage signal of the primary coil **L1**. A signal **PHIN** (induced voltage signal or half-wave rectified signal) obtained by dividing the coil end voltage of the primary coil **L1** using the resistors **RA1** and **RA2** is input to a waveform detection circuit **28** (amplitude detection circuit or pulse width detection circuit) of the power transmission control device **20**. Specifically, the resistors **RA1** and **RA2** form

a voltage divider circuit (resistor divider circuit), and the signal **PHIN** is output from the voltage division node **NA3** of the resistors **RA1** and **RA2**.

The display section **16** displays the state (e.g., power transmission or ID authentication) of the non-contact power transmission system using a color, an image, and the like. The display section **16** is implemented by an LED, an LCD, or the like.

The power transmission control device **20** is a device which controls the power transmission device **10**. The power transmission control device **20** may be implemented by the integrated circuit device (IC) according to this embodiment, for example. The power transmission control device **20** may include a control circuit **22** (power transmission side), an oscillation circuit **24**, a driver control circuit **26**, a waveform detection circuit **28**, a digital power supply regulation circuit **30**, an analog power supply regulation circuit **32**, a temperature detection circuit **38**, and a reset circuit **39**.

The control circuit **22** (control section) controls the power transmission device **10** and the power transmission control device **20**. The control circuit **22** may be implemented by a gate array, a microcomputer, or the like. Specifically, the control circuit **22** performs sequence control and a determination process necessary for power transmission, load detection, frequency modulation, foreign object detection, detachment detection, and the like.

The oscillation circuit **24** includes a crystal oscillation circuit, for example. The oscillation circuit **24** generates a primary-side clock signal. The driver control circuit **26** generates a control signal at a desired frequency based on the clock signal generated by the oscillation circuit **24**, a frequency setting signal from the control circuit **22**, and the like, and outputs the generated control signal to the first and second power transmission drivers **DR1** and **DR2** of the power transmission section **12** to control the first and second power transmission drivers **DR1** and **DR2**.

The waveform detection circuit **28** monitors the waveform of the signal **PHIN** which corresponds to the induced voltage at one end of the primary coil **L1**, and detects a change in load on the secondary side (power reception device). This enables data (load) detection, foreign object (metal) detection, detachment (removal) detection, and the like. Specifically, the waveform detection circuit **28** (amplitude detection circuit) detects amplitude information (peak voltage, amplitude voltage, and root-mean-square voltage) relating to the signal **PHIN** which corresponds to the induced voltage at one end of the primary coil **L1**.

For example, when a load modulation section **46** of the power reception device **40** modulates load in order to transmit data to the power transmission device **10**, the signal waveform of the induced voltage in the primary coil **L1** changes as shown in FIG. **15B**. Specifically, the amplitude (peak voltage) of the signal waveform decreases when the load modulation section **46** reduces load in order to transmit data "0", and the amplitude of the signal waveform increases when the load modulation section **46** increases load in order to transmit data "1". Therefore, the waveform detection circuit **28** can determine whether the data from the power reception device **40** is "0" or "1" by determining whether or not the peak voltage has exceeded a threshold voltage as a result of a peak-hold process on the signal waveform of the induced voltage, for example.

The load change detection method performed by the waveform detection circuit **28** is not limited to the method shown in FIGS. **15A** and **15B**. The waveform detection circuit **28** may determine whether the power reception-side load has increased or decreased using a physical quantity other than

the peak voltage. For example, the waveform detection circuit **28** (pulse width detection circuit) may detect pulse width information (pulse width period in which the coil end voltage waveform is equal to or higher than given setting voltage) relating to the induced voltage signal PHIN of the primary coil **L1**. Specifically, the waveform detection circuit **28** receives a waveform adjusting (shaping) signal from a waveform adjusting circuit which generates a waveform adjusting signal for the signal PHIN and a drive clock signal from a drive clock signal generation circuit which supplies the drive clock signal to the driver control circuit **26**. The waveform detection circuit **28** may detect the pulse width information relating to the induced voltage signal PHIN by detecting pulse width information relating to the waveform adjusting signal to detect a change in load.

The digital power supply regulation circuit **30** regulates the digital power supply voltage. The control circuit **22** (circuit including logic cell) operates based on the digital power supply voltage regulated by and supplied from the digital power supply regulation circuit **30**. The analog power supply regulation circuit **32** regulates the analog power supply voltage. The analog circuit (circuit including comparator, operational amplifier, and the like) included in the power transmission control device **20** operates based on the analog power supply voltage regulated by and supplied from the analog power supply regulation circuit **32**.

The temperature detection circuit **38** detects the temperature of the capacitor **C1** shown in FIG. **11** or the like to detect an abnormality (failure) in $\tan \delta$ of the capacitor. The control circuit **22** suspends power transmission using the power transmission driver **DR1** and **DR2** of the power transmission section **12** when an abnormality in $\tan \delta$ of the capacitor has been detected. Specifically, the temperature detection circuit **38** detects an abnormality in $\tan \delta$ of the capacitor by calculating the difference between the capacitor temperature and the ambient temperature. The control circuit **22** suspends power transmission from the primary side to the secondary side when the control circuit **22** has determined that the difference between the capacitor temperature and the ambient temperature has exceeded a given temperature difference. The control circuit **22** may suspend power transmission from the primary side to the secondary side when the control circuit **22** has determined that the capacitor temperature has exceeded a given temperature.

The reset circuit **39** generates a reset signal and outputs the generated reset signal to each circuit of the power transmission control device **20** (integrated circuit device) to implement a power-on reset.

The power reception device **40** (power reception module or secondary module) may include the secondary coil **L2**, a power reception section **42**, the load modulation section **46**, a power supply control section **48**, and a power reception control device **50**. The power reception device **40** and the power reception control device **50** are not limited to the configuration shown in FIG. **14**. Various modifications may be made such as omitting some elements, adding other elements, or changing the connection relationship.

The power reception section **42** converts an alternating-current induced voltage in the secondary coil **L2** into a direct-current voltage. A rectifier circuit **43** included in the power reception section **42** converts the alternating-current induced voltage. The rectifier circuit **43** includes diodes **DB1** to **DB4**. The diode **DB1** is provided between a node **NB1** at one end of the secondary coil **L2** and a node **NB3** (direct-current voltage **VDC**), the diode **DB2** is provided between the node **NB3** and a node **NB2** at the other end of the secondary coil **L2**, the

diode **DB3** is provided between the node **NB2** and a node **NB4** (**VSS**), and the diode **DB4** is provided between the nodes **NB4** and **NB1**.

Resistors **RB1** and **RB2** of the power reception section **42** are provided between the nodes **NB1** and **NB4**. A signal **CCMP1** obtained by dividing the voltage between the nodes **NB1** and **NB4** using the resistors **RB1** and **RB2** is input to a frequency detection circuit **60** of the power reception control device **50**.

A capacitor **CB1** and resistors **RB4** and **RB5** of the power reception section **42** are provided between the node **NB3** (direct-current voltage **VDC**) and the node **NB4** (**VSS**). A signal **ADIN** obtained by dividing the voltage between the nodes **NB3** and **NB4** using the resistors **RB4** and **RB5** is input to a position detection circuit **56** of the power reception control device **50**.

The load modulation section **46** performs a load modulation process. Specifically, when the power reception device **40** transmits desired data to the power transmission device **10**, the load modulation section **46** variably changes the load in the load modulation section **46** (secondary side) depending on transmission data to change the signal waveform of the induced voltage in the primary coil **L1** as shown in FIG. **15B**. The load modulation section **46** includes a resistor **RB3** and a transistor **TB3** (N-type CMOS transistor) provided in series between the nodes **NB3** and **NB4**. The transistor **TB3** is ON/OFF-controlled based on a signal **P3Q** from a control circuit **52** of the power reception control device **50**. When performing the load modulation process by ON/OFF-controlling the transistor **TB3**, transistors **TB1** and **TB2** of the power supply control section **48** are turned OFF so that the load **90** is not electrically connected to the power reception device **40**.

For example, when reducing the secondary-side load (high impedance) in order to transmit data "0", as shown in FIG. **15B**, the signal **P3Q** is set at the L level so that the transistor **TB3** is turned OFF. As a result, the load in the load modulation section **46** becomes almost infinite (no load). On the other hand, when increasing the secondary-side load (low impedance) in order to transmit data "1", the signal **P3Q** is set at the H level so that the transistor **TB3** is turned ON. As a result, the load in the load modulation section **46** becomes the resistance **RB3** (high load).

The power supply control section **48** controls power supply to the load **90**. A regulator **49** regulates the voltage level of the direct-current voltage **VDC** obtained by conversion by the rectifier circuit **43** to generate a power supply voltage **VD5** (e.g., 5 V). The power reception control device **50** operates based on the power supply voltage **VD5** supplied from the power supply control section **48**, for example.

A transistor **TB2** (P-type CMOS transistor) is controlled based on a signal **P1Q** from the control circuit **52** of the power reception control device **50**. Specifically, the transistor **TB2** is turned ON when ID authentication has been completed (established) and normal power transmission is performed, and is turned OFF during load modulation or the like.

A transistor **TB1** (P-type CMOS transistor) is controlled based on a signal **P4Q** from an output assurance circuit **54**. Specifically, the transistor **TB1** is turned ON when ID authentication has been completed and normal power transmission is performed. The transistor **TB1** is turned OFF when connection of an AC adaptor has been detected or the power supply voltage **VD5** is lower than the operation lower limit voltage of the power reception control device **50** (control circuit **52**), for example.

The power reception control device **50** is a device which controls the power reception device **40**. The power reception control device **50** may be implemented by the integrated

circuit device (IC) according to this embodiment. The power reception control device 50 may operate based on a power supply voltage generated from the induced voltage in the secondary coil L2. The power reception control device 50 may include the control circuit 52 (power reception side), the output assurance circuit 54, the position detection circuit 56, an oscillation circuit 58, the frequency detection circuit 60, a full-charge detection circuit 62, a digital power supply regulation circuit 70, an analog power supply regulation circuit 72, and a reset circuit 74.

The control circuit 52 (control section) controls the power reception device 40 and the power reception control device 50. The control circuit 52 may be implemented by a gate array, a microcomputer, or the like. Specifically, the control circuit 22 performs sequence control and a determination process necessary for ID authentication, position detection, frequency detection, load modulation, full-charge detection, and the like.

The output assurance circuit 54 is a circuit which assures the output from the power reception device 40 when the voltage is low (0 V). The output assurance circuit 54 prevents a backward current flow from the voltage output node NB7 to the power reception device 40.

The position detection circuit 56 monitors the waveform of the signal ADIN which corresponds to the waveform of the induced voltage in the secondary coil L2, and determines whether or not the positional relationship between the primary coil L1 and the secondary coil L2 is appropriate. Specifically, the position detection circuit 56 converts the signal ADIN into a binary value using a comparator, and determines whether or not the positional relationship between the primary coil L1 and the secondary coil L2 is appropriate.

The oscillation circuit 58 includes a CR oscillation circuit, for example. The oscillation circuit 58 generates a secondary-side clock signal. The frequency detection circuit 60 detects the frequency (f_1 or f_2) of the signal CCMP1, and determines whether the data transmitted from the power transmission device 10 is "1" or "0", as shown in FIG. 15A.

The full-charge detection circuit 62 (charge detection circuit) is a circuit which detects whether or not a battery 94 (secondary battery) of the load 90 has been full-charged (charged).

The digital power supply regulation circuit 70 is a circuit which regulates a digital power supply voltage. The analog power supply regulation circuit 72 is a circuit which regulates an analog power supply voltage. The reset circuit 74 generates a reset signal and outputs the generated reset signal to each circuit of the power reception control device 50 (integrated circuit device) to implement a power-on reset.

The load 90 includes a charge control device 92 which controls charging the battery 94 and the like. The charge control device 92 (charge control IC) may be implemented by an integrated circuit device or the like. The battery 94 may be provided with the function of the charge control device 92 (e.g., smart battery).

10. Waveform Detection Circuit

FIG. 16 shows a configuration example of the waveform detection circuit 28 which corresponds to the analog circuit shown in FIGS. 1 to 4. The waveform detection circuit 28 includes an amplitude detection circuit 27 and an A/D conversion circuit 29.

The amplitude detection circuit 27 includes operational amplifiers OPA1 and OPA2, a hold capacitor CA1, and a reset N-type transistor TA1. The signal PHIN is input to a non-inverting input terminal of the operational amplifier OPA1, and an output node NA5 of the operational amplifier OPA2 is connected to an inverting input terminal of the operational

amplifier OPA1. The hold capacitor CA1 and the reset transistor TA1 are provided between a peak voltage hold node NA4 (i.e., output node of the operational amplifier OPA1) and the power supply VSS (low-potential-side power supply).

The hold node NA4 is connected to a non-inverting input terminal of the operational amplifier OPA2, and the output node NA5 of the operational amplifier OPA2 is connected to an inverting input terminal of the operational amplifier OPA2 so that the operational amplifier OPA2 forms a voltage-follower-connected operational amplifier.

The operational amplifiers OPA1 and OPA2, the hold capacitor CA1, and the reset transistor TA1 shown in FIG. 16 form a peak-hold circuit (peak detection circuit). Specifically, the peak voltage of the detection signal PHIN from the voltage detection circuit 14 is held by the hold node NA4, and the peak voltage signal held by the hold node NA4 is subjected to impedance conversion by the voltage-follower-connected operational amplifier OPA2 and is output to the node NA5.

The reset transistor TA1 is turned ON in a reset period to discharge the hold node NA4 toward the power supply VSS (GND). Specifically, the operational amplifier OPA1 is an operational amplifier which merely stores a charge in the hold capacitor CA1, but cannot discharge a charge toward the power supply VSS. Therefore, the operational amplifier OPA1 can follow an increase in the peak voltage of the signal PHIN, but cannot follow a decrease in the peak voltage of the signal PHIN. A leakage current exists in a charge-storage P-type transistor provided in an output section of the operational amplifier OPA1. Therefore, even if the P-type transistor is turned OFF, the voltage of the hold node NA4 increases with the lapse of time. Accordingly, it is necessary to reset the voltage of the hold node NA4 regularly. In FIG. 16, the reset transistor TA1 is provided for the hold node NA4 for the above reasons.

The A/D conversion circuit 29 includes a sample/hold circuit 110, a comparator CPA1, a successive approximation register 112, and a D/A conversion circuit 114. The sample/hold circuit 110 samples and holds a signal PHQ. The comparator CPA1 compares a D/A-converted analog signal DAQ from the D/A conversion circuit 114 with a sample/hold signal SHQ from the sample/hold circuit 110. The successive approximation register 112 (successive approximation type control circuit) stores data relating to an output signal CQ1 from the comparator CPA1. The D/A conversion circuit 114 subjects digital data SAQ (e.g., eight bits) from the successive approximation register 112 to D/A conversion, and outputs an analog signal DAQ.

Note that the A/D conversion circuit 29 is not limited to the configuration shown in FIG. 16. For example, the A/D conversion circuit 29 may be a successive approximation type A/D conversion circuit having a different circuit configuration, or may be a servo-balancing type, parallel comparison type, or dual-slope type A/D conversion circuit. A plurality of comparators to which the signal PHQ is input at a first input terminal and a plurality of different determination reference voltages are input at a second input terminal may be provided instead of the A/D conversion circuit 29.

11. Temperature Detection Circuit

FIG. 17 shows a detailed configuration example of the temperature detection circuit 38 (tan δ detection circuit). The temperature detection circuit 38 shown in FIG. 17 includes a reference measurement transistor TR0, a capacitor temperature measurement transistor TR1, and an ambient temperature measurement transistor TR2. The temperature detection circuit 38 may also include a discharge transistor TR3, a detection circuit BUFR, and a measurement circuit 200. The

transistors TR0, TR1, and TR2 are P-type CMOS transistors, and the transistor TR3 is an N-type CMOS transistor, for example.

The reference measurement transistor TR0 is provided in series with a reference resistor R0 between an oscillation node NR1 (i.e., node at one end of reference capacitor C0) and the power supply VDD3 (high-potential-side power supply). For example, the power supply voltage VDD3 is supplied to the source of the transistor TR0, and the other end of the reference resistor R0, of which one end is connected to the oscillation node NR1, is connected to the drain of the transistor TR0. A control signal SC0 from the measurement circuit 200 is input to the gate of the transistor TR0. The reference capacitor C0 is provided between the oscillation node NR1 and the power supply VSS (low-potential-side power supply).

The capacitor temperature measurement transistor TR1 is provided in series with a capacitor temperature measurement thermistor RT1 between the oscillation node NR1 and the power supply VDD3. For example, the power supply voltage VDD3 is supplied to the source of the transistor TR1, and the other end of the thermistor RT1, of which one end is connected to the oscillation node NR1, is connected to the drain of the transistor TR1. A control signal SC1 from the measurement circuit 200 is input to the gate of the transistor TR1.

The ambient temperature measurement transistor TR2 is provided in series with an ambient temperature measurement thermistor RT2 between the oscillation node NR1 and the power supply VDD3. For example, the power supply voltage VDD3 is supplied to the source of the transistor TR2, and the other end of the thermistor RT2, of which one end is connected to the oscillation node NR1, is connected to the drain of the transistor TR2. A control signal SC2 from the measurement circuit 200 is input to the gate of the transistor TR2.

The discharge transistor TR3 is provided between the oscillation node NR1 and the power supply VSS (GND). For example, the power supply voltage VSS is supplied to the source of the transistor TR3, and the drain of the transistor TR3 is connected to the oscillation node NR1. A control signal SC3 from the measurement circuit 200 is input to the gate of the transistor TR3.

The detection circuit BUFR is a circuit which outputs a detection pulse DP when the voltage of the oscillation node NR1 has exceeded a given threshold voltage. The detection circuit BUFR may be implemented by a Schmidt Trigger inverter circuit, for example.

The measurement circuit 200 receives the detection pulse DP from the detection circuit BUFR, and measures the temperature. The measurement circuit 200 generates the control signals SC0 to SC3 to ON/OFF-control the transistors TR0 to TR3.

FIGS. 18A and 18B show signal waveform examples illustrative of the operation of the circuit shown in FIG. 17. A reference measurement time T is measured, as shown in FIG. 18A. Specifically, the measurement circuit 200 outputs the control signals SC0 and SC3 shown in FIG. 18A to the transistors TR0 and TR3 when measuring the reference measurement time T. When the control signals SC0 and SC3 are set at the L level, the transistor TR0 is turned ON, and the transistor TR3 is turned OFF. Therefore, a charge is stored in the reference capacitor C0 via the oscillation node NR1 from the power supply VDD3 through the transistor TR0 and the reference resistor R0. As a result, the voltage of the oscillation node NR1 increases with a slope determined by a time constant C0×R0. In this specification, symbols (e.g., C0 and R0) which indicate a capacitor and a resistor are also used as symbols which indicate capacitance and resistance, respectively.

When the voltage of the oscillation node NR1 has exceeded a threshold voltage VT, the detection circuit BUFR outputs the detection pulse DP. This causes the control signals SC0 and SC3 to be set at the H level so that the transistor TR0 is turned OFF and the transistor TR3 is turned ON. As a result, the voltage of the oscillation node NR1 decreases to 0 V. The control signals SC0 and SC3 are then set at the L level so that the voltage of the oscillation node NR1 again increases by the time constant C0×R0.

The measurement circuit 200 counts the number of detection pulses DP from the buffer circuit BUFR when the above CR oscillation is repeated. When the number of detection pulses has reached 1000 (N), for example, the measurement circuit 200 finishes measuring the reference measurement time T. Therefore, the reference measurement time is expressed by $T=1000 \times C0 \times R0 \times a$. Note that a is an arbitrary coefficient.

The capacitor temperature is then measured, as shown in FIG. 18B. Specifically, the measurement circuit 200 outputs the control signals SC1 and SC3 shown in FIG. 18B to the transistors TR1 and TR3 when measuring the capacitor temperature. When the control signals SC1 and SC3 are set at the L level, the transistor TR1 is turned ON, and the transistor TR3 is turned OFF. Therefore, the voltage of the oscillation node NR1 increases with a slope determined by a time constant C0×RT1. When the voltage of the oscillation node NR1 has exceeded the threshold voltage VT, the detection circuit BUFR outputs the detection pulse DP. This causes the control signals SC1 and SC3 to be set at the H level so that the transistor TR1 is turned OFF and the transistor TR3 is turned ON. As a result, the voltage of the oscillation node NR1 decreases to 0 V. The control signals SC1 and SC3 are then set at the L level so that the voltage of the oscillation node NR1 again increases by the time constant C0×RT1.

The measurement circuit 200 counts the number of detection pulses during the reference measurement time T measured as shown in FIG. 18A. The measurement circuit 200 determines the number of detection pulses counted within the reference measurement time T to be a first count value CM. Therefore, the following equations are satisfied.

$$T=CM \times C0 \times RT1 \times a=1000 \times C0 \times R0 \times a \quad (1)$$

$$RT1/R0=1000/CM \quad (2)$$

The measurement circuit 200 then measures the ambient temperature by ON/OFF-controlling the transistors TR2 and TR3 using the control signals SC2 and SC3 according to the method shown in FIG. 18B to obtain a second count value CM. In this case, the following equations are satisfied.

$$T=CM \times C0 \times RT2 \times a=1000 \times C0 \times R0 \times a \quad (3)$$

$$RT2/R0=1000/CM \quad (4)$$

According to the circuit shown in FIG. 17, the reference measurement time T is determined as described with reference to FIG. 18A. The number of detection pulses within the reference measurement time T is counted as described with reference to FIG. 18B, and resistance ratio information (RT1/R0 and RT2/R0) is determined based on the count value CM. The capacitor temperature and the ambient temperature are specified based on the resistance ratio information.

According to this configuration, even if the capacitance of the reference capacitor C0 has changed, the count value CM which absorbs the change can be obtained, whereby a more accurate capacitor temperature and ambient temperature can be measured.

12. Layout of Integrated Circuit Devices of Power Transmission Control Device and Power Reception Control Device

FIG. 19 shows a detailed layout example of an integrated circuit device which implements the power transmission control device 20 shown in FIG. 14.

The control logic circuit 110 shown in FIG. 19 is a logic circuit which includes logic cells such as a NAND circuit, a NOR circuit, an inverter, and a D flip-flop, and implements the control circuit 22 and the like shown in FIG. 14. The control logic circuit 110 operates based on the digital power supply voltage (e.g., 3 V) regulated by the digital power supply regulation circuit 30 (series regulator). The driver control circuit 26 shown in FIG. 14 is implemented by the control logic circuit 110, the predrivers PR1 to PR4, and the like shown in FIG. 19.

The analog circuit 120 is a circuit which includes comparators and operational amplifiers of various detection circuits such as the waveform detection circuit. The analog circuit 120 operates based on the analog power supply voltage (e.g., 4.5 V) regulated by the analog power supply regulation circuit 32 (series regulator).

The power supply wiring region in which at least the digital power supply line which supplies the digital power supply voltage and the analog power supply line which supplies the analog power supply voltage are provided is formed in an area indicated by E1 in FIG. 19. The digital power supply regulation circuit 30, the analog circuit 120, and the analog power supply regulation circuit 32 are disposed in the direction D1 with respect to the control logic circuit 110. Specifically, the analog circuit 120 is disposed in the direction D2 with respect to the digital power supply regulation circuit 30, and the analog power supply regulation circuit 32 is disposed in the direction D2 with respect to the analog circuit 120.

The power supply wiring region indicated by E1 is formed along the direction D2 in a region between the control logic circuit 110 and the digital power supply regulation circuit 30, the analog circuit 120, and the analog power supply regulation circuit 32. Specifically, the power supply wiring region is formed linearly along the direction D2.

In FIG. 19, the first power supply pad, to which the power supply voltage VDD5 regulated by the digital power supply regulation circuit 30 is input, is disposed in the direction D4 with respect to the digital power supply regulation circuit 30. The second power supply pad, to which the power supply voltage VD5A regulated by the analog power supply regulation circuit 32 is input, is disposed in the direction D2 with respect to the analog power supply regulation circuit 32.

In FIG. 19, the predrivers PR1 and PR2 are disposed along the side SD1 of the integrated circuit device, and the predrivers PR3 and PR4 are disposed along the side SD2. The predrivers PR1 to PR4 are disposed in the logic circuit region in the direction D3 with respect to the power supply wiring region indicated by E1. Therefore, the VDD1 and VSS1 power supply lines for the predrivers PR1 and PR2 and the VDD2 and VSS2 power supply lines for the predrivers PR3 and PR4 can be easily separated from the power supply lines for other circuits, as indicated by E2 and E3 in FIG. 19. This prevents a situation in which switching noise produced by the predrivers PR1 to PR4 adversely affects other circuits.

The temperature detection circuit 38 operates based on the power supply voltage VDD3 from the digital power supply regulation circuit 30 disposed adjacently to the temperature detection circuit 38 along the direction D2. Therefore, the CR oscillation operation shown in FIGS. 18A and 18B can be stabilized so that temperature detection measurement accuracy can be increased.

Since the control logic circuit 110 is disposed around the center of the chip, lines from the peripheral circuits can be easily routed to the control logic circuit 110.

Since the oscillation circuit 24 is disposed at the lower left of the integrated circuit device and the pads of the clock signal terminals CLKI and CLKO are positioned between the VSS power supply pads, noise is reduced. Since the oscillation circuit 24 is disposed adjacently to the control logic circuit 110 along the direction D2, lines routed to the control logic circuit 110 can be reduced.

A test circuit (5 V logic circuit) which does not operate during a normal operation is disposed at the lower left of the integrated circuit device, and the amplitude detection circuit 27 is disposed at the lower center of the integrated circuit device. According to this arrangement, the oscillation circuit 24 and the predrivers which produce noise can be separated from the analog circuit 120, whereby an adverse effect of noise can be reduced.

The A/D conversion circuit 29 (or a plurality of detection determination comparators) and the like of the waveform detection circuit 28 shown in FIG. 16 are disposed in the region of the analog circuit 120. Note that the entire waveform detection circuit 28 may be disposed in the region of the analog circuit 120.

The analog power supply lines (VD5A and VSSA) are provided along the lower side SD3 and the lower portion of the right side SD4 of the integrated circuit device, and the digital power supply lines (VDD5 and VSS) are provided along the upper portion of the right side SD4 and the arrangement region of the oscillation circuit 24. The predriver power supply lines (VDD1, VSS1, VDD2, and VSS2) are provided at the upper left of the integrated circuit device. An adverse effect of noise from the predrivers can be reduced by separating the power supply lines in this manner.

FIG. 20 shows a detailed layout example of an integrated circuit device which implements the power reception control device 50 shown in FIG. 14.

The power supply wiring region in which at least the digital power supply line which supplies the digital power supply voltage and the analog power supply line which supplies the analog power supply voltage are provided is formed in an area indicated by F1 in FIG. 20. The digital power supply regulation circuit 70, an analog circuit 140, and the analog power supply regulation circuit 72 are disposed in the direction D1 with respect to a control logic circuit 130 (e.g., control circuit 52 shown in FIG. 14). Specifically, the analog circuit 140 is disposed in the direction D2 with respect to the digital power supply regulation circuit 70, and the analog power supply regulation circuit 72 is disposed in the direction D2 with respect to the analog circuit 140. The comparators and operational amplifiers which implement the position detection circuit 56, the frequency detection circuit 60, and the full-charge detection circuit 62 shown in FIG. 14 are disposed in the region of the analog circuit 140.

In FIG. 20, since the control logic circuit 130 is disposed around the center of the integrated circuit device, lines from the peripheral circuits can be easily routed to the control logic circuit 130. A test circuit (5 V logic circuit) is disposed at the lower left of the integrated circuit device. Specifically, the logic circuits are concentrated at the left of the integrated circuit device.

The oscillation circuit 58 is disposed at the upper left of the integrated circuit device, and the VSS and VDD3 power supply lines are provided near the oscillation circuit 58. The digital power supply regulation circuit 70 which outputs the power supply voltage VDD3 for the control logic circuit 130 and the oscillation circuit 58 is disposed near the oscillation

circuit **58** at the upper right of the integrated circuit device. This suppresses a change in power supply voltage so that the operation of the oscillation circuit **58** can be stabilized.

The analog power supply line (VSSA) is provided along the lower side SD3 and the right side SD4 of the integrated circuit device, and the digital power supply line (VSS) is provided along the upper side SD1 and the left side SD2. The VDD5 and VD5A power supply lines are separated from the VDD power supply line (other power supply lines), and the VDD power supply line is provided around the core circuit of the integrated circuit device in the shape of a ring. Noise can be reduced by separating the power supplies in this manner.

Since the P1Q, P3Q, P4Q, and PBQ pads are disposed when mounting the peripheral components, the peripheral components can be easily mounted.

Although only some embodiments of the invention have been described in detail above, those skilled in the art would readily appreciate that many modifications are possible in the embodiments without materially departing from the novel teachings and advantages of the invention. Accordingly, such modifications are intended to be included within the scope of the invention. Any term (e.g., P-type power MOS transistor, N-type power MOS transistor, and external driver) cited with a different term (e.g., P-type transistor, N-type transistor, and external device) having a broader meaning or the same meaning at least once in the specification and the drawings can be replaced by the different term in any place in the specification and the drawings. The invention also includes any combination of the embodiments and the modifications. The configurations, arrangements, and operations of the integrated circuit device, the predriver, the power transmission device, the power transmission control device, the power reception device, and the power reception control device and the power supply line wiring method are not limited to those described relating to the above embodiments. Various modifications and variations may be made.

What is claimed is:

1. An integrated circuit device comprising:

a digital power supply regulation circuit that regulates a digital power supply voltage;

an analog power supply regulation circuit that regulates an analog power supply voltage;

a control logic circuit that includes logic cells and operates based on the digital power supply voltage that is regulated by and supplied from the digital power supply regulation circuit;

an analog circuit that includes at least a comparator or an operational amplifier and operates based on the analog power supply voltage that is regulated by and supplied from the analog power supply regulation circuit; and

a power supply wiring region, at least a digital power supply line that supplies the digital power supply voltage that is regulated by the digital power supply regulation circuit and an analog power supply line that supplies the analog power supply voltage that is regulated by the analog power supply regulation circuit being provided in the power supply wiring region,

the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit being disposed in a first direction with respect to the control logic circuit; and

the power supply wiring region being formed along a second direction in a region between the control logic circuit and the digital power supply regulation circuit, the analog circuit, and the analog power supply regulation circuit, the second direction being a direction perpendicular to the first direction.

2. The integrated circuit device as defined in claim 1, the analog circuit being disposed in the second direction with respect to the digital power supply regulation circuit, and the analog power supply regulation circuit being disposed in the second direction with respect to the analog circuit.

3. The integrated circuit device as defined in claim 2, a first power supply pad being disposed in a fourth direction with respect to the digital power supply regulation circuit, the fourth direction being a direction that is opposite to the second direction, a power supply voltage that is regulated by the digital power supply regulation circuit being input to the first power supply pad; and a second power supply pad being disposed in the second direction with respect to the analog power supply regulation circuit, a power supply voltage that is regulated by the analog power supply regulation circuit being input to the second power supply pad.

4. The integrated circuit device as defined in claim 2, the integrated circuit device further including a reset circuit that generates a reset signal and outputs the reset signal to each circuit of the integrated circuit device, the reset circuit being disposed between the digital power supply regulation circuit and the analog circuit.

5. The integrated circuit device as defined in claim 2, the integrated circuit device further including a temperature detection circuit that operates based on the digital power supply voltage that is regulated by and supplied from the digital power supply regulation circuit and performs a temperature detection process, the temperature detection circuit being disposed between the digital power supply regulation circuit and the analog circuit.

6. The integrated circuit device as defined in claim 5, the temperature detection circuit including: a reference measurement transistor that is provided in series with a reference resistor between an oscillation node that is a node at one end of a reference capacitor and a digital power supply;

a capacitor temperature measurement transistor that is provided in series with a capacitor temperature measurement thermistor between the oscillation node and the digital power supply;

an ambient temperature measurement transistor that is provided in series with an ambient temperature measurement thermistor between the oscillation node and the digital power supply;

a discharge transistor, a drain of the discharge transistor being connected to the oscillation node; and

a detection circuit that outputs a detection pulse when a voltage of the oscillation node has exceeded a given threshold voltage.

7. The integrated circuit device as defined in claim 1, the integrated circuit device further including: a first predriver that drives a first N-type power MOS transistor of a first external driver that includes the first N-type power MOS transistor and a first P-type power MOS transistor; and

a second predriver that drives the first P-type power MOS transistor of the first external driver, the first predriver and the second predriver being disposed in a third direction with respect to the power supply wiring region, the third direction being a direction that is opposite to the first direction.

8. An integrated circuit device comprising: a control logic circuit that includes logic cells and operates based on a digital power supply voltage;

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an analog circuit that includes at least a comparator or an operational amplifier and operates based on an analog power supply voltage;
 a power supply wiring region, a power supply line being provided in the power supply wiring region;
 a first predriver that drives a first N-type power MOS transistor of a first external driver, the first external driver including the first N-type power MOS transistor and a first P-type power MOS transistor;
 a second predriver that drives the first P-type power MOS transistor of the first external driver,
 the analog circuit being disposed in a first direction with respect to the control logic circuit;
 the power supply wiring region being formed along a second direction in a region between the control logic circuit and the analog circuit, the second direction being a direction perpendicular to the first direction; and
 the first predriver and the second predriver being disposed in a third direction with respect to the power supply wiring region, the third direction being a direction that is opposite to the first direction.

9. The integrated circuit device as defined in claim 7, a low-potential-side power supply line and a high-potential-side power supply line of the first predriver and the second predriver being separated from a low-potential-side power supply line and a high-potential-side power supply line of other circuits of the integrated circuit device.

10. The integrated circuit device as defined in claim 8, a low-potential-side power supply line and a high-potential-side power supply line of the first predriver and the second predriver being separated from a low-potential-side power supply line and a high-potential-side power supply line of other circuits of the integrated circuit device.

11. The integrated circuit device as defined in claim 7, a first N-type transistor and a first P-type transistor that form the first predriver being disposed in an arrangement region of the first predriver;

a second N-type transistor and a second P-type transistor that form the second predriver being disposed in an arrangement region of the second predriver;

each of the first N-type transistor, the first P-type transistor, the second N-type transistor, and the second P-type transistor including a plurality of unit transistors that are connected in parallel; and

the integrated circuit device further including:

a first N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first N-type transistor;

a first P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first P-type transistor;

a second N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second N-type transistor; and

a second P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second P-type transistor.

12. The integrated circuit device as defined in claim 8, a first N-type transistor and a first P-type transistor that form the first predriver being disposed in an arrangement region of the first predriver;

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a second N-type transistor and a second P-type transistor that form the second predriver being disposed in an arrangement region of the second predriver;

each of the first N-type transistor, the first P-type transistor, the second N-type transistor, and the second P-type transistor including a plurality of unit transistors that are connected in parallel; and

the integrated circuit device further including:

a first N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first N-type transistor;

a first P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the first P-type transistor;

a second N-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second N-type transistor; and

a second P-type gate control circuit that outputs a plurality of gate control signals that are respectively input to gates of the plurality of unit transistors of the second P-type transistor.

13. The integrated circuit device as defined in claim 12, the first N-type gate control circuit outputting gate control signals that turn ON the plurality of unit transistors of the first N-type transistor at different timings when the first N-type transistor turns ON, the first N-type gate control circuit outputting gate control signals that turn OFF the plurality of unit transistors of the first N-type transistor at the same timing when the first N-type transistor turns OFF;

the first P-type gate control circuit outputting gate control signals that turn ON the plurality of unit transistors of the first P-type transistor at different timings when the first P-type transistor turns ON, the first P-type gate control circuit outputting gate control signals that turn OFF the plurality of unit transistors of the first P-type transistor at the same timing when the first P-type transistor turns OFF;

the second N-type gate control circuit outputting gate control signals that turn ON the plurality of unit transistors of the second N-type transistor at different timings when the second N-type transistor turns ON, the second N-type gate control circuit outputting gate control signals that turn OFF the plurality of unit transistors of the second N-type transistor at the same timing when the second N-type transistor turns OFF; and

the second P-type gate control circuit outputting gate control signals that turn ON the plurality of unit transistors of the second P-type transistor at different timings when the second P-type transistor turns ON, the second P-type gate control circuit outputting gate control signals that turn OFF the plurality of unit transistors of the second P-type transistor at the same timing when the second P-type transistor turns OFF.

14. The integrated circuit device as defined in claim 7, the integrated circuit device further including:

a third predriver that drives a second N-type power MOS transistor of a second external driver that includes the second N-type power MOS transistor and a second P-type power MOS transistor; and

a fourth predriver that drives the second P-type power MOS transistor of the second external driver, the first predriver and the second predriver being disposed along a first side of the integrated circuit device;

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the third predriver and the fourth predriver being disposed along a second side of the integrated circuit device, the second side intersecting the first side; and the analog circuit being disposed along a fourth side that is opposite to the second side.

15. The integrated circuit device as defined in claim 8, the integrated circuit device further including:

a third predriver that drives a second N-type power MOS transistor of a second external driver that includes the second N-type power MOS transistor and a second P-type power MOS transistor; and

a fourth predriver that drives the second P-type power MOS transistor of the second external driver,

the first predriver and the second predriver being disposed along a first side of the integrated circuit device;

the third predriver and the fourth predriver being disposed along a second side of the integrated circuit device, the second side intersecting the first side; and

the analog circuit being disposed along a fourth side that is opposite to the second side.

16. The integrated circuit device as defined in claim 15, the control logic circuit controlling the first predriver, the second predriver, the third predriver, and the fourth pre-

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driver, and the control logic circuit being disposed in the second direction with respect to the first predriver and the second predriver and in the first direction with respect to the third predriver and the fourth predriver.

17. The integrated circuit device as defined in claim 15, the integrated circuit device being provided in a power transmission device of a non-contact power transmission system, the non-contact power transmission system transmitting power from the power transmission device to a power reception device by electromagnetically coupling a primary coil and a secondary coil and supplying power to a load of the power reception device,

the first external driver being a first power transmission driver that drives one end of the primary coil; and

the second external driver being a second power transmission driver that drives the other end of the primary coil.

18. An electronic instrument comprising the integrated circuit device as defined in claim 1.

19. An electronic instrument comprising the integrated circuit device as defined in claim 8.

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