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Bakker

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(54) **POWER-UP AND POWER-DOWN CIRCUIT FOR SYSTEM-ON-A-CHIP INTEGRATED CIRCUIT**

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G05F 1/00 (2006.01)
G05F 5/00 (2006.01)

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See application file for complete search history.

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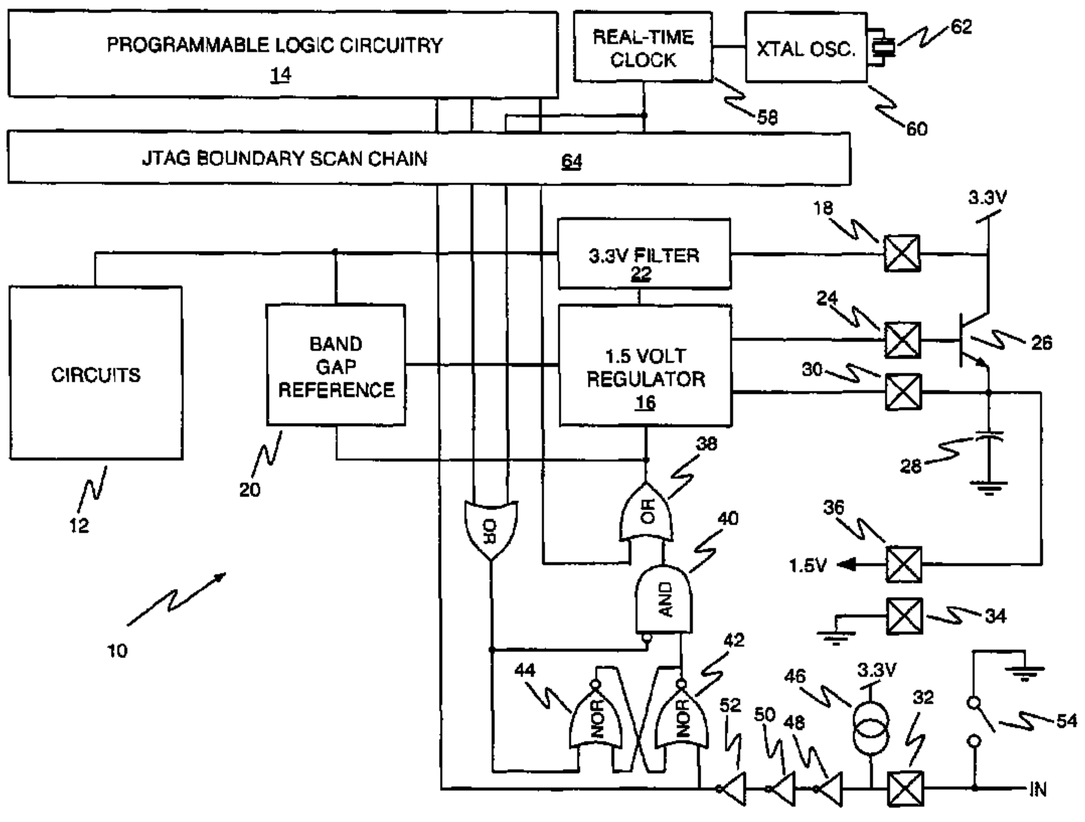
(57) **ABSTRACT**

A power-up and power-down circuit for an integrated circuit includes a voltage regulator set for a first voltage. A first I/O pad is coupled internally to an input to the voltage regulator and to first internal circuits. The second voltage is externally coupled to the first I/O pad. A second I/O pad is coupled internally to an output of the voltage regulator configured to drive the base of an external transistor. A third I/O pad of the integrated circuit is coupled internally to a reference-voltage input of the voltage regulator. A fourth I/O pad is coupled to a feedback input of the voltage regulator. A fifth I/O pad of the integrated circuit is coupled internally to logic circuitry that controls power-up and power down of the integrated circuit from internal signals including internal signals from a real-time clock circuit disposed on the integrated circuit.

6 Claims, 1 Drawing Sheet



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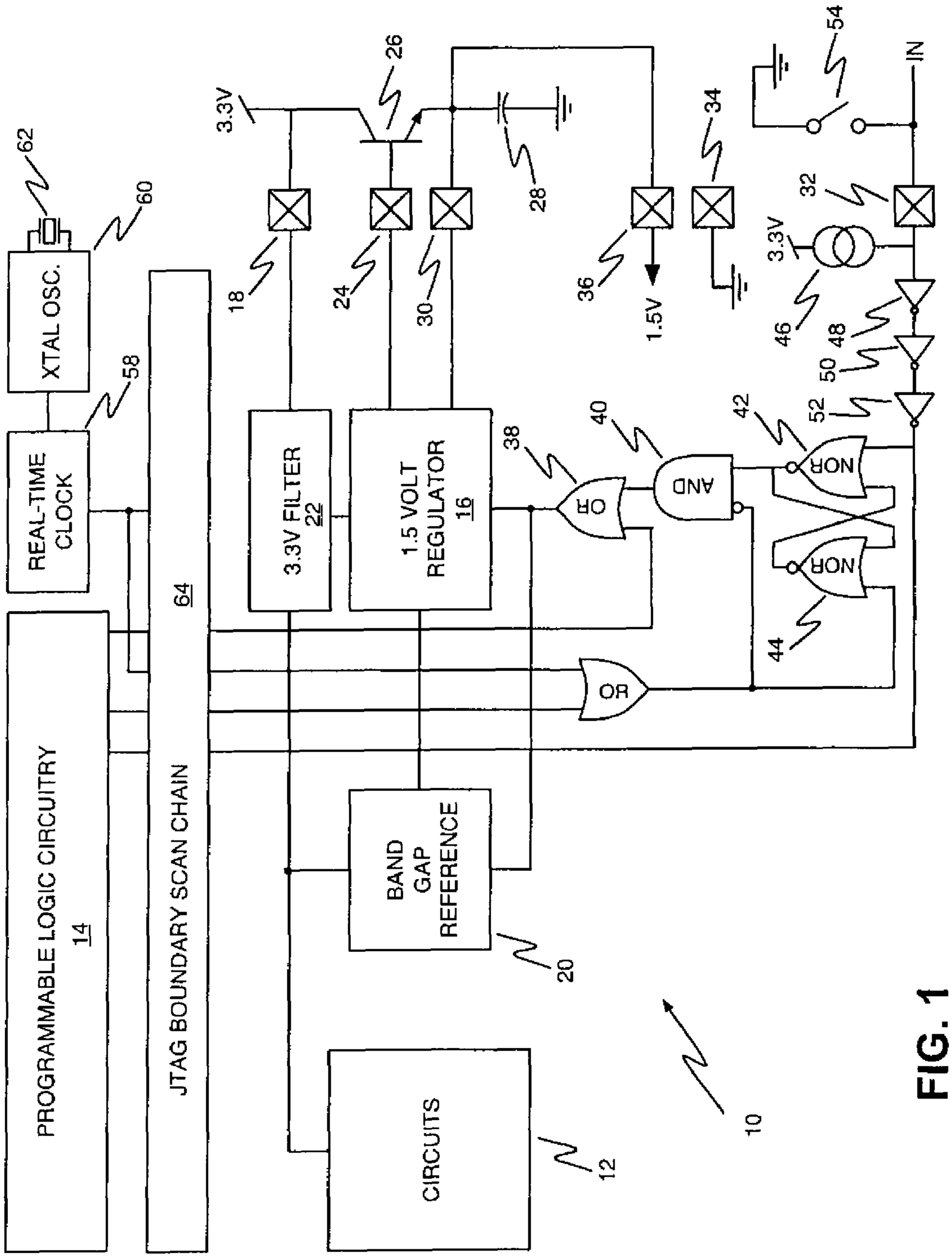
62
60
XTAL OSC.
58
REAL-TIME CLOCK
64
PROGRAMMABLE LOGIC CIRCUITRY 14
JTAG BOUNDARY SCAN CHAIN
3.3V FILTER 22
1.5 VOLT REGULATOR 16
BAND GAP REFERENCE
20
CIRCUITS
12
10
3.3V
26
18
24
30
28
36
1.5V
34
54
IN
32
3.3V
46
48
50
52
38
40
42
44
OR
AND
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FIG. 1

POWER-UP AND POWER-DOWN CIRCUIT FOR SYSTEM-ON-A-CHIP INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/021,092, filed Dec. 22, 2004, now issued as U.S. Pat. No. 7,119,398.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to integrated circuits. More particularly, the present invention relates to integrated circuits having multiple voltage power supply requirements and to a power-up and power-down circuit for use on such an integrated circuit.

2. The Prior Art

As integrated circuit functions become more complex, the power-supply requirements for the integrated circuits also increase in complexity. For example, an emerging trend is to provide both analog and digital functions on the same integrated circuit die. The power supply requirements for an integrated circuit including both analog and digital functions include provision for more than one voltage to be supplied to the integrated circuit. Typical requirements for such an integrated circuit fabricated according to presently-practiced technology may include the requirement to supply both 1.5 volts and 3.3 volts for circuitry internal to the integrated circuit.

BRIEF DESCRIPTION OF THE INVENTION

A power-up and power-down circuit for use on an integrated circuit includes a voltage regulator set for a first voltage used by circuits in the integrated circuit. A first I/O pad of the integrated circuit is coupled internally to an input to the voltage regulator and to circuits in the integrated circuit that use a second voltage. The second voltage used by the integrated circuit is externally coupled to the first I/O pad. A second I/O pad is coupled internally to an output of the voltage regulator that is configured to drive the base of an external emitter-follower transistor. A third I/O pad of the integrated circuit is coupled internally to a feedback input of the internal voltage regulator. In operation, an external transistor will have its collector coupled to the first I/O pad, its base coupled to the second I/O pad and its emitter coupled to the third I/O pad. An external filter capacitor will be coupled between the emitter of the transistor and ground. A fourth I/O pad of the integrated circuit is coupled internally to logic circuitry that controls power-up and power down of the integrated circuit from internal signals including internal signals from a real-time clock circuit disposed on the integrated circuit. A fifth I/O pad provides the first voltage to internal circuits on the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

FIG. **1** is a block diagram illustrating the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

Referring to FIG. **1**, an exemplary embodiment of a power-up and power-down circuit according to the present invention is shown. Integrated circuit **10** requires a first power-supply voltage and a second power-supply voltage different from the first power-supply voltage. In the exemplary embodiment discussed with reference to FIG. **1**, the first and second power-supply voltages will be 1.5 VDC and 3.3 VDC, respectively, although persons of ordinary skill in the art will appreciate that the present invention is not limited to these particular values and will function with other voltages as well. In the exemplary embodiment of FIG. **1**, 3.3 volts is used to drive circuits such as analog circuits **12**, and 1.5 volts is used to drive logic circuits **14** such as programmable logic in the form of an FPGA array or similar programmable circuitry.

As may be seen from FIG. **1**, a voltage regulator **16** is set to provide the first power supply voltage. The second power supply voltage is provided directly to the integrated circuit on a first I/O pad **18**. The second power-supply voltage is coupled to the input of voltage regulator **16**. A bandgap circuit **20** provides a reference voltage to a reference input of the voltage regulator **16**. Bandgap reference circuit **20**, as well as the circuits **12**, is powered directly by the second power-supply voltage through a power-supply filter **22** for the second power-supply voltage that is coupled to the first I/O pad **18**.

A reference input of voltage regulator **16** is coupled to the output of bandgap reference circuit **20**. An output of the voltage regulator circuit **16** is coupled to a second I/O pad **24**. The output of the voltage regulator **16** is designed to drive the base of an external NPN transistor, shown at reference numeral **26** connected as an emitter-follower. The collector of external transistor **26** may be coupled to the second power-supply voltage that is supplied to the first I/O pad **18**. The emitter of external transistor **26** supplies the regulated first power-supply voltage and is coupled to a filter capacitor **28**, the other plate of which is referenced to ground as is known in the art. The second power-supply voltage at the emitter of the external transistor **26** is fed back to voltage regulator **16** via third I/O pad **30** as is known in the art.

Voltage regulator circuit **16** has an enable input that may be controlled from circuits inside integrated circuit **10**, such as a real-time clock or programmable logic circuits **14**. The enable input to voltage regulator **16** may also be controlled from an external source through fourth I/O pad **32**. The regulated voltage from the emitter of transistor **26** is provided to the integrated circuit through a fifth I/O pad **36** through a connection external to the device. As is customary, ground is provided to integrated circuit **10** through a sixth I/O pad **34**.

More particularly, in the exemplary embodiment of FIG. **1**, the enable input of voltage regulator **16** is driven by OR gate **38**. A first input of OR gate **38** is driven by the output of AND gate **40**. One input of AND gate **40** is driven from the output of NOR gate **42**. NOR gate **42** is cross coupled with NOR gate **44** to form a latch as is known in the art. The other input of NOR gate **42** is controlled from fourth I/O pad **32**. In the exemplary embodiment of FIG. **1**, a small current source **46** drives a triple low-power inverter string including cascaded inverters **48**, **50**, and **52**. As shown in FIG. **1**, inverter **48** may have an input conditioned to reject contact bounce in the event that an external mechanical switch **54** is used to activate the power control function. Switch **54** is preferably a momentary switch, but other switches can be employed. Persons of ordinary skill in the art will appreciate that fourth I/O pad **32** may be driven from either or both of a mechanical switch and a

low-going signal from a device external to integrated circuit **10**. The output of inverter **52** drives the free input of NOR gate **42**.

The free input of NOR gate **44** is coupled to the output of OR gate **56**. One input of OR gate **56** is driven by the output of real-time clock **58**. Real-time clock **58**, and the crystal oscillator **60** that drives it using an external crystal **62** as is known in the art, are driven from the second power-supply voltage at first I/O pad **18**. Real-time clock **58**, and crystal oscillator **60** are always running so long as the second power-supply voltage is present on first I/O pad **18**. The second input of OR gate **56** may be driven from programmable logic circuit **14** if a portion of it is programmed (or hardwired) to provide a power-supply control function.

Boundary-scan register chain **64** may be provided in the circuit of FIG. **1**. As will be understood by persons of ordinary skill in the art, boundary-scan register chain **64** may be configured according to the well-known JTAG standard and may be used to load data, perform diagnostic routines, etc. The signal and control lines passing between logic circuitry **14** and the other elements of FIG. **1** may all pass through boundary-scan register chain **64**.

Normally, the free inputs of both NOR gates **42** and **44** are held at a logic low level. Initially, the output of NOR gate **42** will be at a logic high level, forcing the output of NOR gate **44** (and the other input of NOR gate **42** which it drives) to be at a logic low level. This can be accomplished by selecting the relative sizing of NOR gates **42** and **44** or by assuring that a logic high level is provided to the free input of NOR gate **44** at power-up of the second power-supply voltage.

The inverting input of AND gate **40** will be at a logic low level and its output will thus be at a logic high level. The second input of OR gate **38** will be at a logic low level and its output will be at a logic high level, disabling voltage regulator **16**.

If switch **54** is closed, fourth I/O pad **32** goes to a logic low level, forcing the free input of NOR gate **42** to a high logic level through the output of inverter **52**. The output of NOR gate **42** will be forced to a logic low level, driving the output of NOR gate **44** to a logic high level since its other input is also at a logic low level. This will latch the output of NOR gate **42** to the logic low state, enabling voltage regulator **16**. Once this occurs, further activation of switch **54** will have no effect on the voltage regulator **16** through NOR gate **42**.

As shown in FIG. **1**, the output of inverter **52** may also be coupled into the programmable logic circuitry **14** to indicate the state of the switch **54**. Programmable logic circuitry **14** may be configured to provide a signal to an input of OR gate **56** to provide a signal to NOR gate **44** to disable voltage regulator **16** once it detects that switch **54** has been closed for a second time.

Control circuits or state machines for implementing particular power-up and power-down control functions may be appropriately implemented in programmable logic circuitry **14**. Persons of ordinary skill in the art know how to implement such circuits in programmable logic to provide particular control functions that are simply a matter of design choice and are beyond the scope of the present invention.

Persons of ordinary skill in the art will appreciate that the control gates discussed in the preceding text are powered from first I/O pad **18**, to allow immediate control of the power-up and power-down circuit of the present invention.

The power-up and power-down circuit of the present invention is versatile and allows significant control over the first power-supply voltage. In its initial state when the second power-supply voltage is applied to first I/O pad **18**, voltage regulator **16** is disabled. A low-going signal from an external source at fourth I/O pad **32** will enable the voltage regulator **16** as previously disclosed herein.

Voltage regulator **16** may be disabled as a result of any one of several events. First, a second low-going signal at fourth I/O pad **32** may be sensed by logic circuitry **14**, which can then provide a disable signal through OR gate **56**. In addition, logic circuits disposed inside logic circuitry **14** may provide a disable signal through OR gate **56** in response to any number of internal or external conditions being met. The range of possibilities in this regard is vast, being limited only by the requirements of any particular design and the imagination of the application designer. The operation of the present invention is thus not limited to operating in response to any particular internal or external conditions.

Finally, the operation of the power-up and power-down circuit of the present invention may be controlled by real-time clock **58** through the other input of OR gate **56**. Persons of ordinary skill in the art will recognize that voltage regulator **16** may be both enabled and disabled when the output of OR gate **56** is controlled by real-time clock **58**. As will be appreciated by persons of ordinary skill in the art, real-time clock **58** may be programmed to issue "sleep" or "wake-up" signals at preselected intervals and may provide a logic high input to OR gate **56** during periods when voltage regulator **16** is to be disabled. The output of OR gate **56** is coupled to the inverting input of AND gate **40**. A logic high level is first sent to the inverting input of AND gate **40** and the free input of NOR gate **44**. A high level is latched at the output of NOR gate **42** while the voltage regulator **16** is still enabled because the inverting input of AND gate **40** is high. Then the signal to the inverting input of AND gate **40** and to the free input of NOR gate **44** is changed to a low logic level by the real-time clock due to the occurring of some event, consequently the voltage regulator **16** is disabled.

According to one exemplary aspect of the present invention, the other input of OR gate **38** may be coupled to a boundary-scan register chain **64** so that the voltage regulator **16** may be turned off for diagnostic purposes. Normally, this input of OR gate is held at a logic low level. If it is desired to disable voltage regulator **16** for diagnostic purposes, a logic high level is presented to this input via the boundary scan register.

According to another exemplary aspect of the present invention, bandgap reference circuit **20** has a first enable input coupled to the output of OR gate **38** to allow it to be disabled when voltage regulator **16** is disabled. A second enable input may be provided in bandgap reference circuit **20** to allow it to be separately enabled by boundary scan register chain **64** for diagnostic purposes.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is:

1. A power-up and power-down circuit for use on an integrated circuit having circuits using a first power-supply voltage and a second power-supply voltage comprising:

a first I/O pad;

a second I/O pad;

a third I/O pad;

a fourth I/O pad;

a fifth I/O pad coupled to circuits in the integrated circuit that use the second voltage;

a bandgap reference;

a voltage regulator set for the first voltage, having an input coupled to the first I/O pad and to circuits in the integrated circuit that use the second voltage, an output coupled to the second I/O pad, a reference input of the internal voltage regulator coupled to the bandgap reference, a first-voltage feedback input coupled to the third I/O pad, and an enable input;

logic circuitry coupled to the fourth I/O pad and configured to drive the enable input of the voltage regulator in response to logic signals from the fifth I/O pad; and

a transistor having a first terminal coupled to the first I/O pad, a gate coupled to the second I/O pad, and a second terminal coupled to the third I/O pad.

2. The power-up and power-down circuit of claim **1** further including:

a real-time clock powered by the second voltage; and

wherein the logic circuitry is coupled to the real-time clock and the fourth I/O pad, and is configured to drive the enable input of the voltage regulator in response to logic signals from at least one of the real-time clock and the fourth I/O pad.

3. The power-up and power-down circuit of claim **1** further including:

programmable logic; and

wherein the logic circuitry is coupled to the programmable logic and the fourth I/O pad, and is configured to drive the enable input of the voltage regulator in response to logic signals from at least one of the programmable logic and the fourth I/O pad.

4. The power-up and power-down circuit of claim **3** wherein:

the programmable logic is powered by the first voltage.

5. The power-up and power-down circuit of claim **1** wherein:

the transistor is an external NPN transistor connected as an emitter follower with the first terminal the collector, the gate the base, and the second terminal the emitter.

6. The power-up and power-down circuit of claim **5** which further comprises:

a filter capacitor coupled between the second terminal of the transistor and ground.

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