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(54) **INTERFACE APPARATUS AND METHODS OF TESTING INTEGRATED CIRCUITS USING THE SAME**

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**G01R 31/26** (2006.01)

(52) **U.S. Cl.** ..... **324/765**; 324/754; 324/158.1

(58) **Field of Classification Search** ..... 324/754-765, 324/158.1; 703/23

See application file for complete search history.

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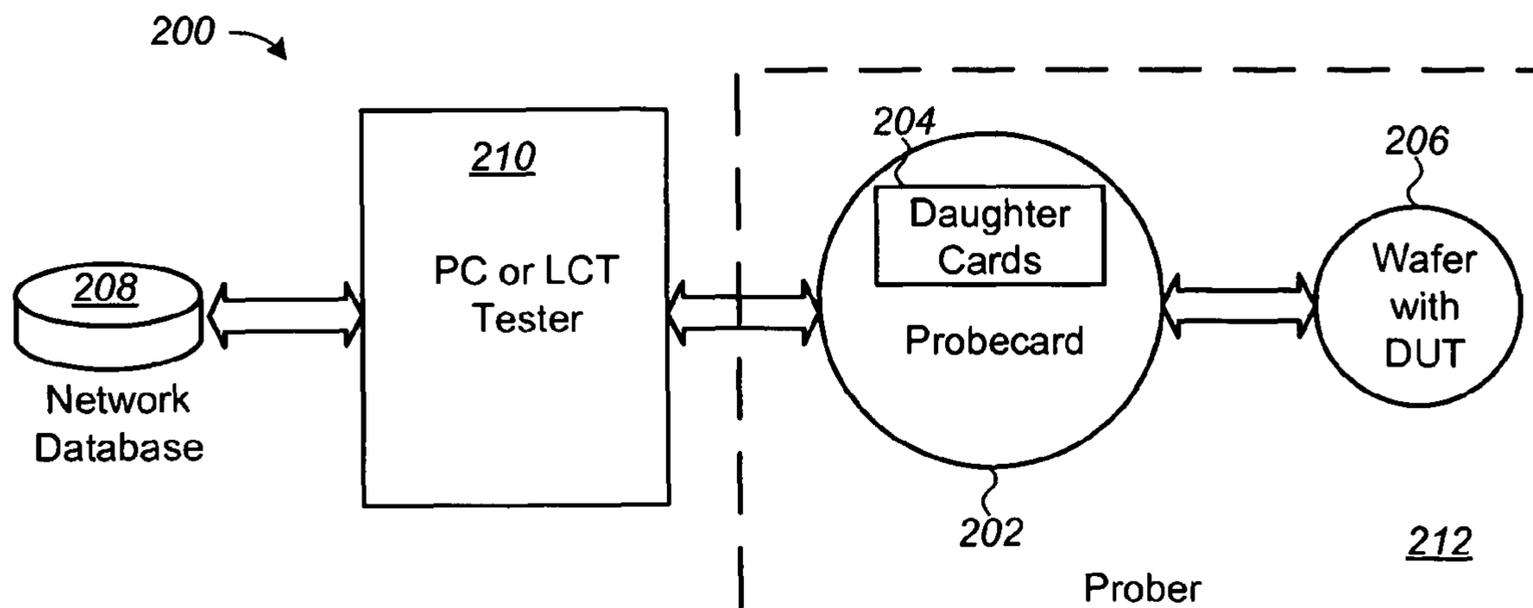
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(57) **ABSTRACT**

An apparatus and method are provided for testing a semiconductor device (DUT). Generally, the apparatus includes an interface board with conductive elements adapted to electrically couple with the DUT and connected to a number of test circuits. Each test circuit resides on one of a number of daughter cards on the interface board, and provides test input signals to and receives output signals from the DUT to generate a result based on a program loaded to the daughter cards before testing begins. The apparatus further includes a controller to drive the interface board and store test results. In one embodiment, the interface board is a load board for back end testing. In another embodiment, the interface board is a probe card for front end testing. Preferably, the apparatus is capable of testing DUTs including memory arrays, logic circuits or both, and the daughter cards are capable of being re-programmed and re-used on different DUTs.

**19 Claims, 3 Drawing Sheets**



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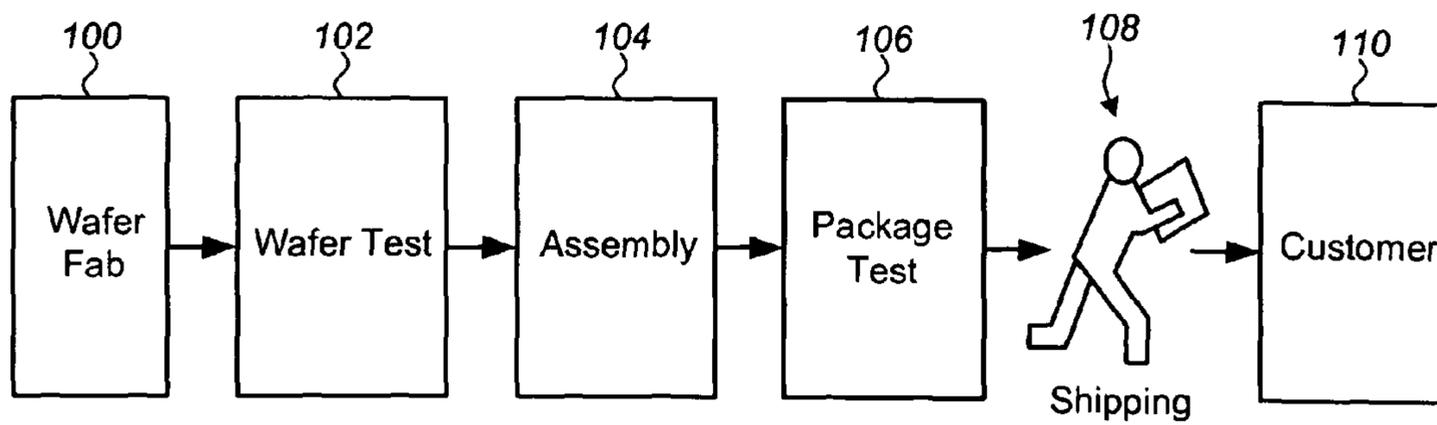


FIG. 1

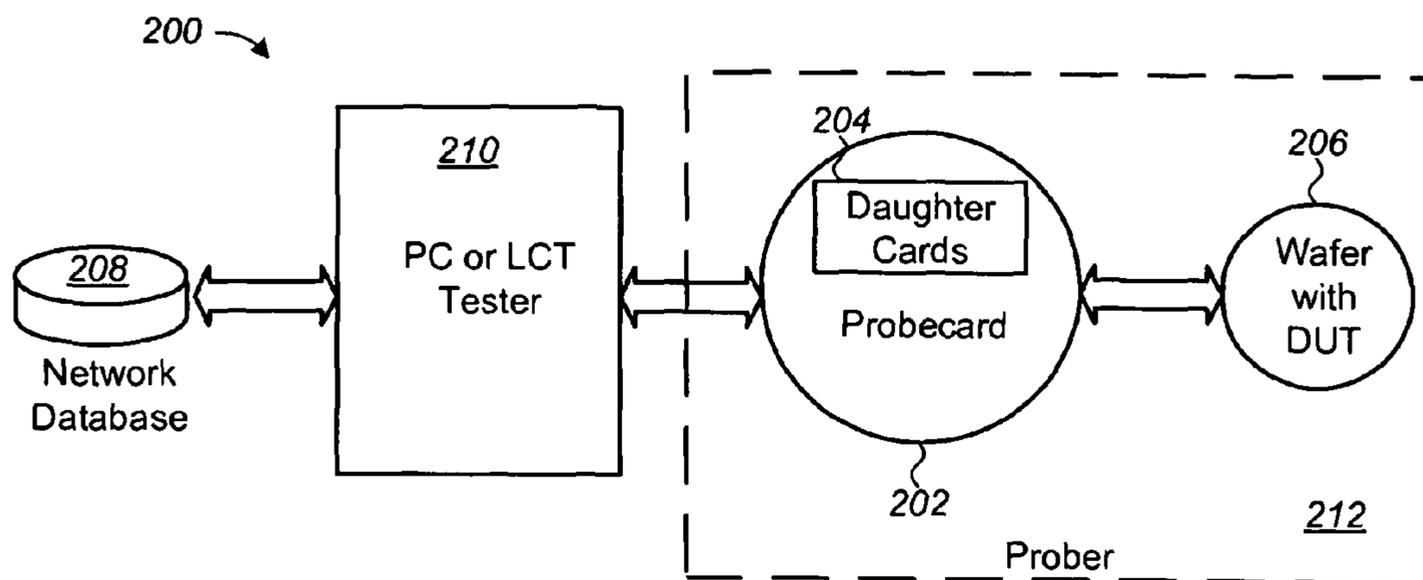


FIG. 2

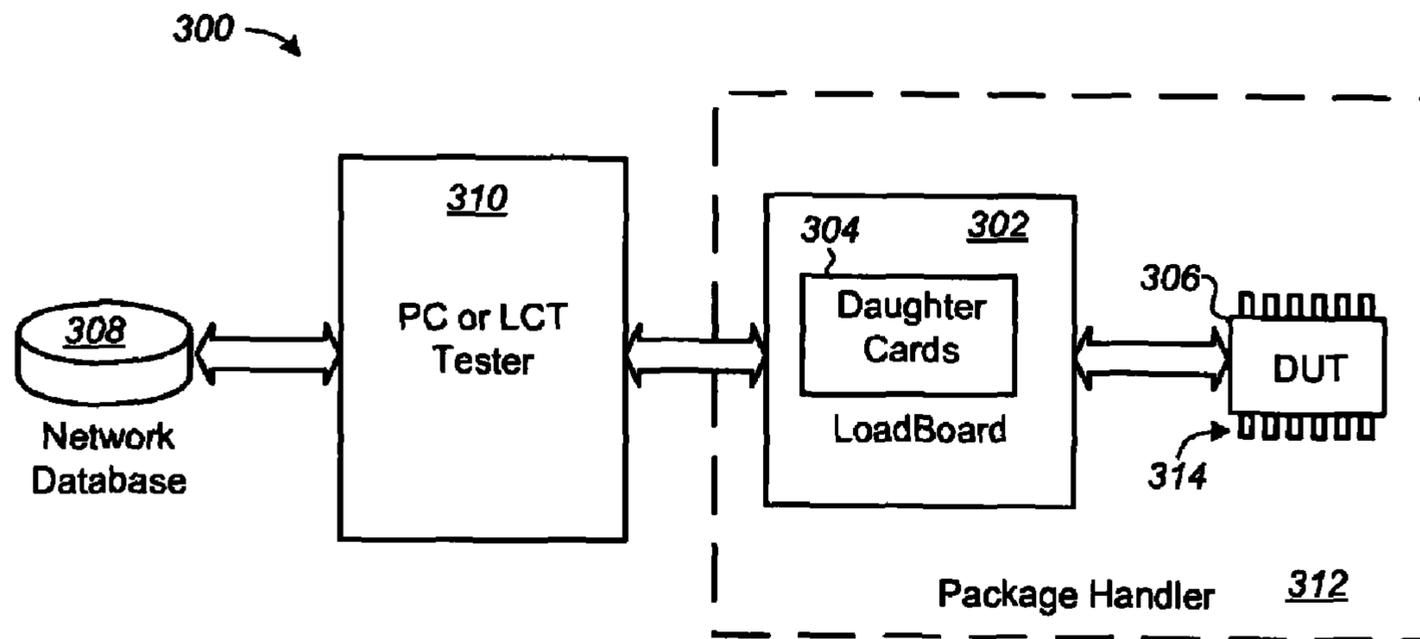


FIG. 3

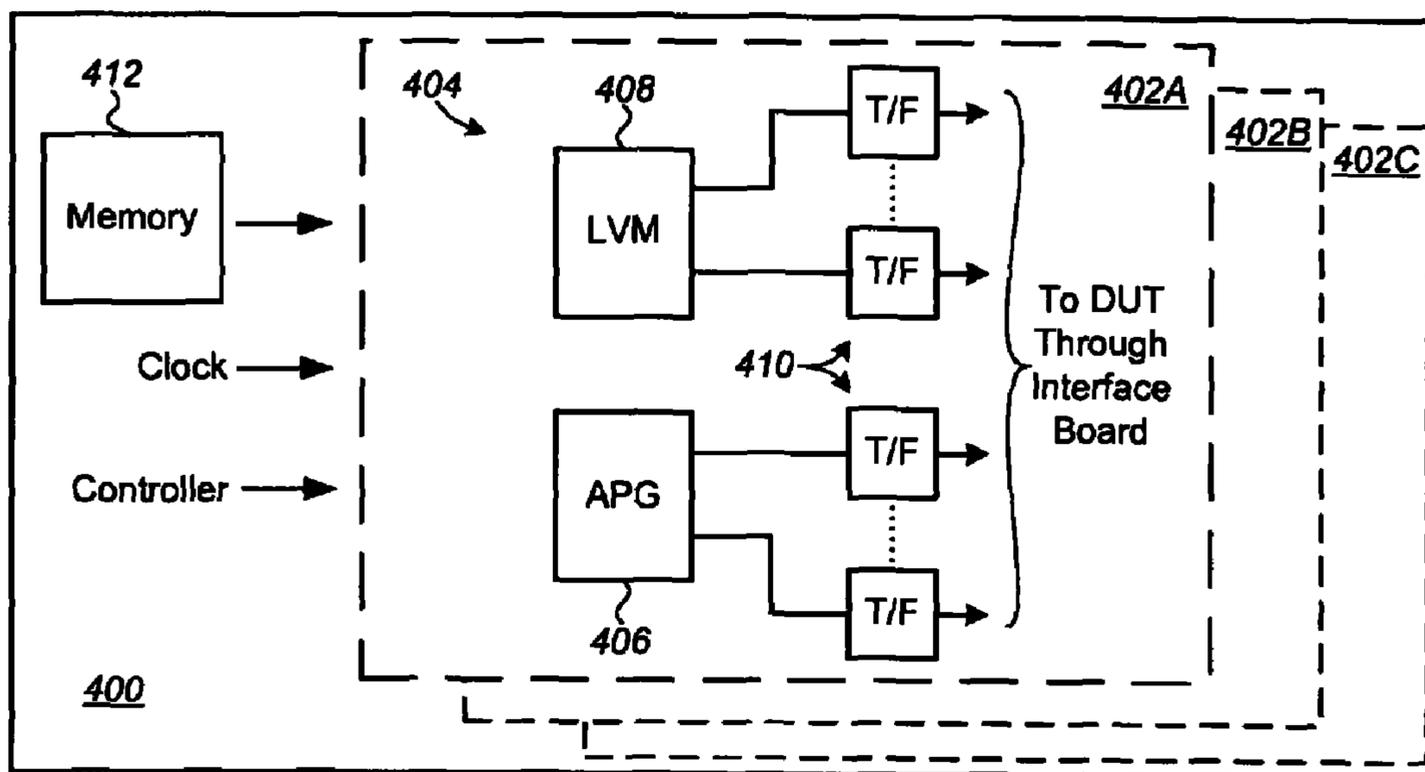


FIG. 4

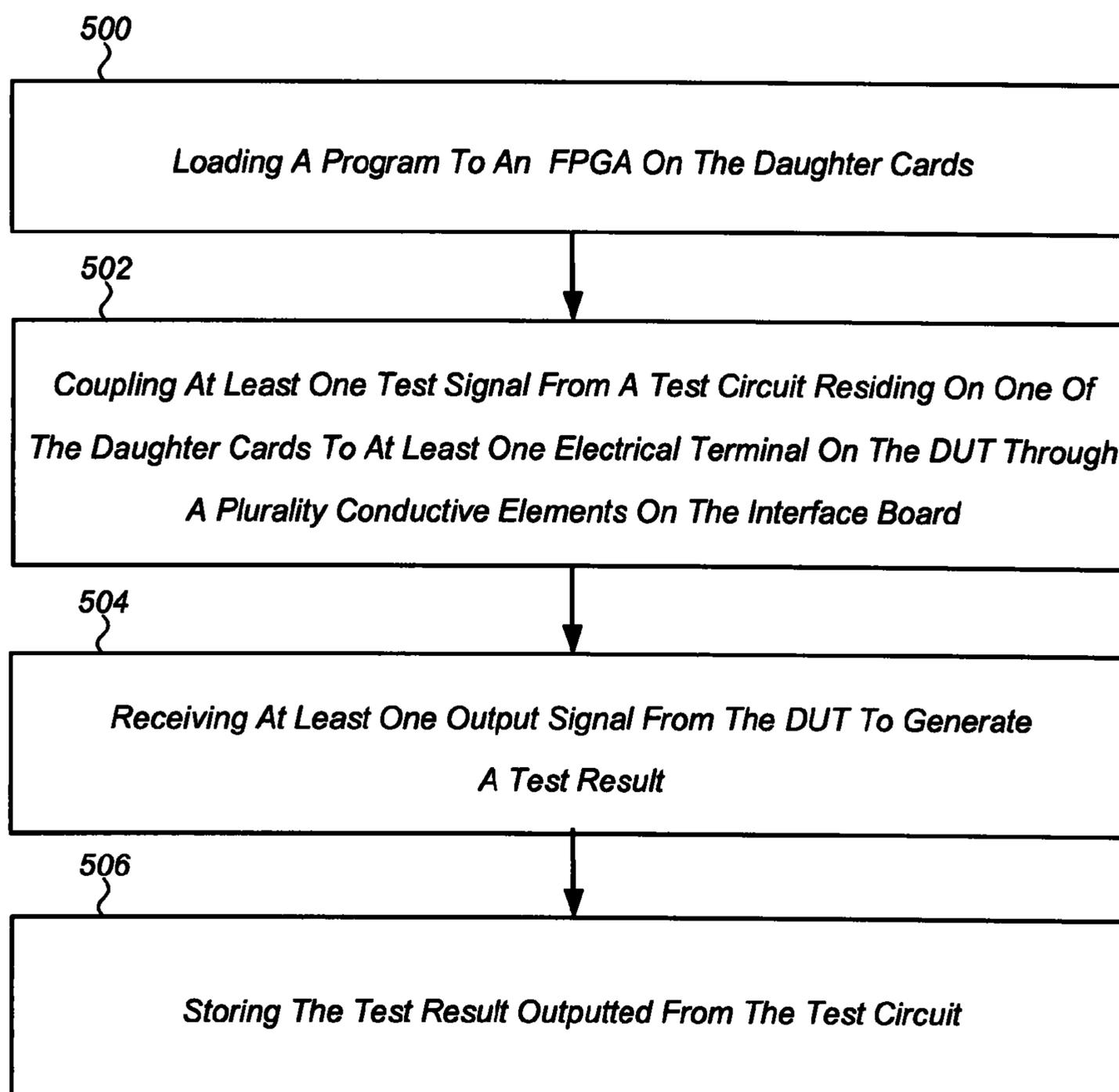


FIG. 5

## INTERFACE APPARATUS AND METHODS OF TESTING INTEGRATED CIRCUITS USING THE SAME

### CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 60/777,584 filed Feb. 28, 2006, entitled Smart Load board And Probe card And Methods Of Testing Semiconductor Wafers And Integrated Circuits Using The Same; which application is hereby incorporated by reference.

### TECHNICAL FIELD

The present invention relates generally to semiconductor fabrication, and more particularly to apparatus and methods for testing devices on semiconductor wafers and integrated circuits using the same.

### BACKGROUND OF THE INVENTION

Manufacturers in the electronic industry use test systems to automatically test various electronic components and integrated circuits (ICs) to weed out defective devices or ICs. Generally, it is desirable to test the ICs at several points during the manufacturing process including while they are still part of a wafer or substrate and after packaging the devices before they are mounted or assembled on modules, cards or boards.

Conventional methods for testing devices in the front end (FE), that is before assembly and packaging, are commonly referred to as FE tests and use a low-end, slow tester and a probe card to electrically couple to devices under test (DUTs) in an undiced wafer. Although this approach has the advantages of using a relatively inexpensive tester and of weeding out defective devices prior to incurring the expense of assembly and packaging, it is limited in that these testers can only perform functional tests at low speed and parametric tests.

Because of the limitations of conventional FE testing, it is generally necessary to perform additional back end (BE) tests following assembly and packaging using an expensive, fast high-end tester. These high-end testers, commonly referred to as "big iron" testers, are capable of performing both high speed functional tests and parametric tests. For example, full speed datasheet tests are typically performed in the back end on Big Iron testers.

Conventional BE testing methods have not been wholly satisfactory for a number of reasons. First, the trend in the electronic industry has been to further increase the miniaturization of electronic devices and circuits, thereby leading to an increase in the complexity of the ICs tested. Thus, as ICs become more complex, the complexity and cost of these Big Iron back end testers has increased correspondingly. Moreover, because BE testing is performed only after assembly and packaging, money is wasted on packing "bad" devices, significantly reducing the cost efficiency of the manufacturing process. Attempts have been made at reducing the money wasted on packing defective devices by moving speed tests from the back end to the front end by testing at the wafer level, that is while the devices or ICs are still part of an undiced wafer, using slow, inexpensive testers with an "offset" introduced to compensate for the difference in speed. However, this approach results in the culling of "good" devices at wafer level, leading to yield overkill and again reduces the cost efficiency of the manufacturing process. Moreover, due to setup and hold times on faster synchronous devices even this

technique cannot enable full speed datasheet testing using the slower, inexpensive testers typically used in the front end.

Accordingly, there is a need for an apparatus and method for high-speed testing of devices and ICs at the wafer level in the front end. There is a further need for an apparatus and method that enables high-speed, datasheet testing of assembled and packaged devices and ICs in the back end, which eliminates the need for complex and expensive testers.

The present invention provides a solution to these and other problems, and offers further advantages over conventional testing apparatus and methods.

### BRIEF DESCRIPTION OF THE DRAWINGS

These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

FIG. 1 is a process flow of a method for testing wafers and integrated circuits (ICs) using a test set-up according to an embodiment of the present invention;

FIG. 2 is a functional block diagram of a test set-up using an advanced or smart probe card having a number of Field Programmable Gate Array (FPGA) daughter cards according to an embodiment of the present invention to test a device under test (DUT) on a semiconductor wafer;

FIG. 3 is a functional block diagram of a test set-up using an advanced or smart load board having a number of FPGA daughter cards according to another embodiment of the present invention to test a DUT;

FIG. 4 is a functional block diagram of an FPGA daughter card having a number of test circuits according to an embodiment of the present invention; and

FIG. 5 is flow chart of a method for testing a DUT using a test apparatus including an interface board with a number of FPGA daughter cards according to an embodiment of the present invention.

### DETAILED DESCRIPTION

The following description is directed to apparatus and methods for testing devices on semiconductor wafers and integrated circuits (ICs), and more particularly to advanced probe cards and load boards and to methods of front end (FE) and back end (BE) testing of a device under test (DUT) using the same.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures, and techniques are not shown in detail or are shown in block diagram form in order to avoid unnecessarily obscuring an understanding of this description.

Reference in the description to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment. The term "to couple" as used herein may include both to directly connect and to indirectly connect through one or more intervening components.

By DUT it is meant any electronic component module or an IC having logic circuits, memory arrays or both. DUT can be

one of a number of die or devices on an undiced substrate, an individual die or device, or a packaged device. A DUT can be coupled to test apparatus via a number of pins or via probes contacting pads on the die.

Broadly, there are two types of test systems or apparatus, those suitable for testing memory arrays or circuits, such as flash memory or Random Access Memories (RAM), and those suitable for testing logic circuits, such as Micro Controllers, Application Specific ICs (ASICs), and Programmable Logic Devices (PLDs). Often devices or DUTs include both memory arrays and logic circuits. Moreover, it is generally desirable to test the ICs at several points during the manufacturing process including while they are still part of a wafer or substrate and after packaging the devices before they are mounted or assembled on modules, cards or boards.

Preferably, the test system and method of the present invention are capable of testing ICs while they are still part of a wafer in the front end and after packaging in the back end. More preferably, the test system and method of the present invention are capable of DUTs including memory arrays or circuits, logic circuits or both.

Briefly, the test system or apparatus of the present invention includes an interface board coupled to a number of test circuits and having a number of conductive elements adapted to electrically couple with electrical terminals on the DUT. Each test circuit resides on one of a number of daughter cards physically and electrically connected to the interface board, and can include a combination of memory chips, clock chips, level drivers, and comparators. In a preferred embodiment, the daughter card is implemented using a programmable logic circuit, such as a Field Programmable Gate Array (FPGA). Each test circuit is arranged to provide test input signals to and receive output signals from the DUT through the interface board to generate a test result based on a program loaded to an FPGA on a daughter card before testing begins, and which then executes the code. Generally, the test system further includes a controller to drive the interface board and store test results outputted from the test circuits.

In one embodiment, the controller is a Personal Computer (PC) or a Low-Cost-Tester (LCT), and the program is loaded directly from the PC or LCT to the FPGA before testing begins. The FPGA then executes the code to test the DUTs. This embodiment is particularly useful for lot test, a test or series of tests performed at the wafer level, that is on undiced wafers or substrates, to cull out defective dies in a process commonly referred to as die purification, thereby saving packaging costs and improving back end yield.

Alternatively, the daughter cards can further include a memory to store a program, which is loaded to the FPGA on the daughter card before testing begins. This embodiment is particularly advantageous when a large amount of memory is needed, as in the case where extremely complex testing is required.

The test system and method of the present invention will now be described in greater detail with reference to FIGS. 1 to 5.

FIG. 1 shows a process flow for testing ICs according to the present invention. Referring to FIG. 1 following fabrication, the process or test method generally begins when finished die are moved from the wafer fabrication laboratory or fab 100 to wafer test 102, in which DUTs in die on an uncut wafer or substrate are tested, FE testing, either simultaneously or sequentially. Results of these FE tests are used to cull out defective dies in a process commonly referred to as die purification, thereby saving packaging costs and improving back end yield. Optionally, the test results can be used to identify

bin1 or bin 2 materials etc at the wafer level in a process commonly known as Speed Binning.

Following wafer test 102 passing dies are assembled or bonded to electrical connections or pins of a lead frame or a package substrate (in the case of Ball grid arrays), and packaged in a process commonly referred to as assembly 104. Next, following assembly, the packaged DUTs are tested subjected to high-speed functional and speed BE tests in a process commonly referred to as package test 106. The packaged DUTs are subjected to high-speed functional and speed BE tests in a process commonly referred to as package test. As noted above, such BE tests were conventionally performed using expensive "big iron" testers. However, in accordance with the present invention, the BE tests are performed using an advanced or smart load board having a number of daughter cards with test circuits implemented using one or more FPGAs.

The fully tested device is then shipped 108 to an internal or external customer 110.

In one aspect or embodiment, the interface board is an advanced or smart probe card adapted for performing FE tests on the wafer, including functional and speed testing. For purposes of clarity, many of the details of semiconductor testing in general, and probe cards in particular that are widely known and are not relevant to the present invention have been omitted from the following description. Semiconductor testing and probe cards are also disclosed in commonly assigned U.S. Pat. Nos. 6,847,218, 6,759,865, and 7,112,975, which are incorporated herein by reference in their entirety.

A functional block diagram of a test set-up or system 200 using an advanced or smart probe card 202 having a number of daughter cards 204 each with a number of FPGAs to test a DUT in a die on a semiconductor wafer 206 is shown in FIG. 2. Referring to FIG. 2, datasheet specification or parameters are provided from a network database 208 to a test system controller 210, such as a PC or a LCT, to drive or control the probe card 202 and a prober 212 in which the probe card 202 is installed. The probe card 202 includes multiple probes (not shown) to align with and contact electrical pads of the DUT(s) on the wafer 206, and a number of test circuits (not shown in this figure), each resident on or implemented using one or more of the FPGAs on the daughter cards 204. The test circuits on the daughter cards 204 are adapted to provide test input signals to the DUT(s), and to receive output signals therefrom to generate a test result based on a program loaded directly from the controller 210 before testing begins. The FPGAs on the daughter cards 204 then execute the program code to test the DUTs, and the test results are transferred to and stored in the controller 210. Optionally, the test results can be transferred through the controller 210 to the network database 208.

Alternatively, the daughter cards 204 could further include a memory (not shown) to store a program, which is then loaded to an FPGA on the daughter card before testing begins. This embodiment is particularly advantageous when a large amount of memory is needed, as in the case of extremely complex testing is required.

The program can provide test signals or vectors including vectors from a Logic Vector Memory (LVM) for testing logic circuits, and vectors generated by an algorithmic pattern generator (APG) for testing memory arrays. The test system 200 with the probe card 202 of the present invention is capable of testing DUTs including memory arrays, logic circuits or both at speeds of up to that of the FPGAs of the daughter cards 204. Preferably, the probe card 202 is capable of testing DUTs at speeds of up to about 333 MHz, and more preferably, up to

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about 500 MHz. Most preferably, the FPGA on the daughter cards **204** are capable of being re-programmed and re-used with a number of different interface boards or probe cards **202** to test a number of different DUTs.

In another aspect or embodiment of the present invention the interface board is an advanced or smart load board adapted for performing BE tests on the DUT(s). A functional block diagram of a test set-up or system **300** using an advanced or smart load board **302** having a number of daughter cards **304** each with a number of FPGAs to test a packaged DUT **306** is shown in FIG. 3. Referring to FIG. 3, datasheet specification or parameters are provided from a network database **308** to a test system controller **310**, such as a PC or a LCT, to drive or control the load board **302** and a package handler **312** in which the load board is installed. The load board **302** includes a number of conductive elements (not shown) to electrically couple with electrical terminals or connectors, such as pins **314**, coming out of the packaged DUT **306**. As in the probe card embodiment described above, the load board **302** further includes a number of test circuits (not shown in this figure), each resident on or implemented using one or more of the FPGAs on the daughter cards **304**, and each adapted to provide test input signals to the DUT(s) and to receive output signals therefrom to generate a test result based on a program loaded to the FPGA before testing begins. The FPGAs on the daughter cards **304** then execute the program code to test the DUTs, and the test results are transferred to and stored in the controller **310**. Optionally, the test results can be transferred through the controller **310** to the network database **308**.

Also as described above, the daughter cards **304** could further include a memory (not shown) to store a program, which is then loaded to an FPGA on the daughter card before testing begins. This embodiment is particularly advantageous when a large amount of memory is needed, as in the case of extremely complex testing is required.

Preferably, the load board **302** is capable of testing DUTs at speeds of up to about 333 MHz, and more preferably, up to about 500 MHz. Most preferably, the daughter cards **304** are capable of being re-programmed and re-used with a number of different interface boards or load boards **302** to test a number of different DUTs **306**.

A functional block diagram of an FPGA daughter card having a number of test circuits according to an embodiment of the present invention is shown in FIG. 4. Referring to FIG. 4, the daughter card **400** generally includes one or more FPGAs **402A-C** on which is resident or implemented one or more test circuits **404**. Generally, each test circuit **404** has a number of functional blocks or sub-circuits including an APG **406** for executing algorithms and generating patterns for testing DUTs including memory circuits or arrays, an LVM **408** for providing logic test vectors for testing DUTs including logic circuits, and multiple timing and formatting circuits (T/F **410**) to adjust the timing and formatting of signals received from the LVM and the APG, and to couple the LVM and the APG to the DUT. Each test circuit **404** is coupled through the interface card, i.e., the probe card or the load board, to the controller (not shown in this figure) to receive a program before testing begins. The program can include test parameters or device specifications as well as a test algorithm or vector. In addition, each test circuit **404** may receive a clock input or signal from the controller or from a separate clock (not shown) located on the daughter card **400**. Optionally, the daughter card **400** could further include a memory **412**, such as a flash memory, to store more complex test vectors or programs loaded from the controller before testing begins.

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The memory **412** can also be used to store test results prior to transferring them to the controller.

Methods for testing a DUT using a test apparatus including an interface board with a number of daughter cards in accordance with the present invention will now be described in greater detail with reference to the flowchart of FIG. 5. Referring to FIG. 5, generally the method of the present invention begins with loading a program to an FPGA on the daughter cards (step **500**). Next, at least one test signal from a test circuit residing on one of the daughter cards is coupled to at least one electrical terminal on the DUT through multiple conductive elements on the interface board (step **502**). Following this, at least one output signal from the DUT is received in by the test circuit to generate a test result (step **504**). Finally, the test result outputted from the test circuit is stored in the controller or uploaded to the network database (step **506**).

The advantages of the over previous or conventional methods include: (i) cost reduction—uses a computer or LCT to drive handler and smart load board and/or prober and smart probe card; (ii) FPGA based daughter cards are re-useable on multiple products or DUT types; (iii) enables inexpensive testing at class test in back end, thereby reducing the need for expensive “big iron” testers; (iv) capable of testing DUTs including memory arrays or circuits, logic circuits or both; (v) capable of testing DUTs or products at low and high speeds up to about 500 Mhz; and (vi) with in-house speed test speed failures are caught at wafer level, saving packaging costs and providing faster feedback to fab engineers, thereby improving yield.

The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents. The scope of the present invention is defined by the claims, which includes known equivalents and unforeseeable equivalents at the time of filing of this application.

What is claimed is:

1. An apparatus for performing electrical tests on at least one device under test (DUT), the apparatus comprising an interface board provided with a plurality conductive elements adapted to electrically couple with electrical terminals on the DUT and connected to a number of test circuits, each of said test circuits residing on one of a plurality of Field Programmable Gate Array (FPGA) daughter cards on said interface board, and arranged to provide test input signals to said DUT and receive output signals from said DUT to generate a test result based on a program loaded to the FPGA daughter cards before testing begins; a controller to control said interface board and store therein said test result outputted from said test circuit; and wherein each of the plurality of FPGA daughter cards include a plurality of FPGAs, and a memory to store the test results, and at least one of the plurality of FPGAs include a logic vector memory (LVM) to test logic circuits in the DUT.

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2. An apparatus according to claim 1, wherein the interface board is a load-board, and wherein the plurality of conductive elements comprise sockets to receive pins out of a packaged DUT.

3. An apparatus according to claim 1, wherein the interface board is a probe card, and wherein the plurality of conductive elements comprise probes to align with and contact electrical pads of the DUT in a die in a semiconductor wafer.

4. An apparatus according to claim 1, wherein the controller comprises a Personal Computer (PC) or a Low-Cost-Tester (LCT).

5. An apparatus according to claim 4, wherein a program is loaded to the memory of at least one of the plurality of FPGA daughter cards before testing begins.

6. An apparatus according to claim 5, wherein the program is loaded directly from the PC or LCT to the memory before testing begins.

7. A method for testing a device under test (DUT) using an apparatus including an interface board with a plurality of Field Programmable Gate Array (FPGA) daughter cards physically and electrically connected thereto, the method comprising:

loading a program to a memory on at least one of the plurality of FPGA daughter cards;

configuring at least one of a number of FPGAs on at least one of the plurality of FPGA daughter cards with the program loaded in the memory before testing begins;

transmitting at least one test signal from a test circuit residing on one of the FPGA daughter cards to at least one electrical terminal on the DUT through a plurality of conductive elements on the interface board;

receiving at least one output signal from the DUT to generate a test result; and

storing the test result in the memory.

8. A method according to claim 7, wherein the apparatus comprises a controller to control the interface board.

9. A method according to claim 8, wherein the controller comprises a Personal Computer (PC) or a Low-Cost-Tester (LCT).

10. A method according to claim 7, wherein the interface board is a load-board, and wherein the plurality of conductive elements on the interface board comprise sockets to receive pins out of a packaged DUT.

11. A method according to claim 7, wherein the interface board is a probe card, and wherein the plurality of conductive

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elements on the interface board comprise probes to align with and contact electrical pads of the DUT in a die in a semiconductor wafer.

12. A system comprising:

an interface board including a plurality of conductive elements adapted to electrically couple with terminals on a device under test (DUT); and

a number of Field Programmable Gate Array (FPGA) daughter cards electrically connected to the plurality of conductive elements, each of said FPGA daughter cards including a number of FPGAs configured to provide test input signals to terminals on the DUT through the plurality of conductive elements and to receive output signals therefrom to generate a test result based on a program loaded to the FPGA daughter cards before testing begins, and a memory electrically connected to the number of FPGAs to store the test results, wherein at least one of the number of FPGAs include a logic vector memory (LVM) to test logic circuits in the DUT.

13. A system according to claim 12, wherein at least one of the number of FPGAs further include an algorithmic pattern generator (APG) to test memory arrays in the DUT.

14. A system according to claim 12, further including a controller electrically coupled to the number of FPGA daughter cards to control the number of FPGAs.

15. A system according to claim 14, wherein the controller is further electrically coupled to the memory to receive from the memory the test results stored therein.

16. A system according to claim 14, wherein the memory is electrically coupled to the controller to store programs from the controller, and is configured to program the number of FPGAs.

17. A system according to claim 15, wherein the memory is configured to store test vectors used to test logic circuits in the DUT.

18. A system according to claim 12, wherein the interface board is a load-board, and wherein the plurality of conductive elements comprise sockets to receive pins out of a packaged DUT.

19. A system according to claim 12, wherein the interface board is a probe card, and wherein the plurality of conductive elements comprise probes to align with and contact electrical pads of the DUT in a die in a semiconductor wafer.

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