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**Lee et al.**

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(54) **SUBSTRATE FOR SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

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(52) **U.S. Cl.** ..... **257/698**; 257/700; 257/E21.507

(58) **Field of Classification Search** ..... 257/698
See application file for complete search history.

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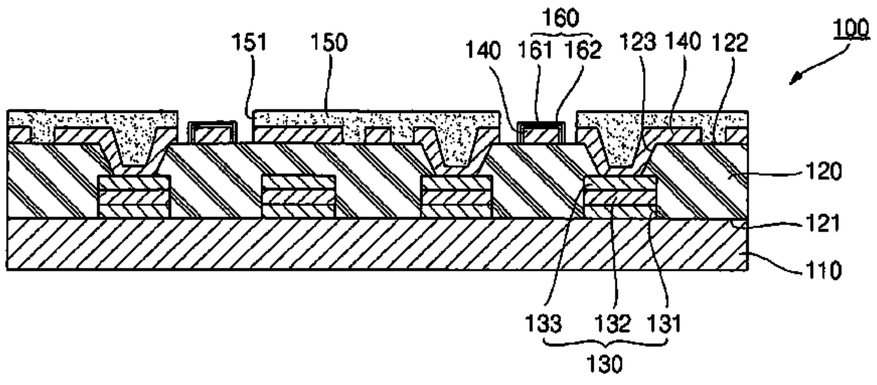
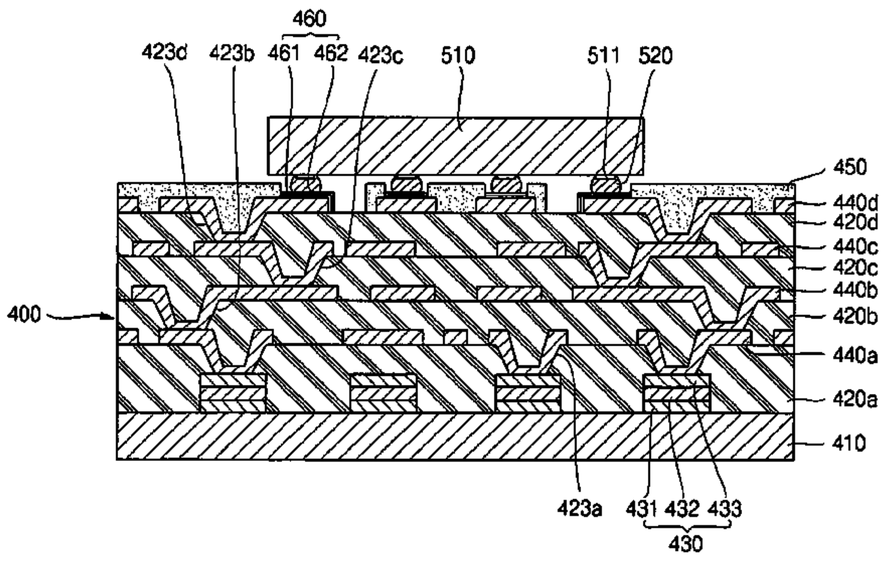
(57) **ABSTRACT**

A substrate for a semiconductor device and a manufacturing thereof, and a semiconductor device using the same and a manufacturing method thereof are disclosed. For example, in the substrate according to the present invention, a core is eliminated, so that the substrate has a very thin thickness, as well, the length of electrically conductive patterns becomes shorter, whereby the electrical efficiency thereof is improved. Moreover, since a carrier having a stiffness of a predetermined strength is bonded on the substrate, it can prevent a warpage phenomenon during the manufacturing process of the semiconductor device. Furthermore, the carrier is removed from the substrate, whereby a solder ball fusing process or an electrical connecting process of the semiconductor die can be easily performed.

**15 Claims, 24 Drawing Sheets**



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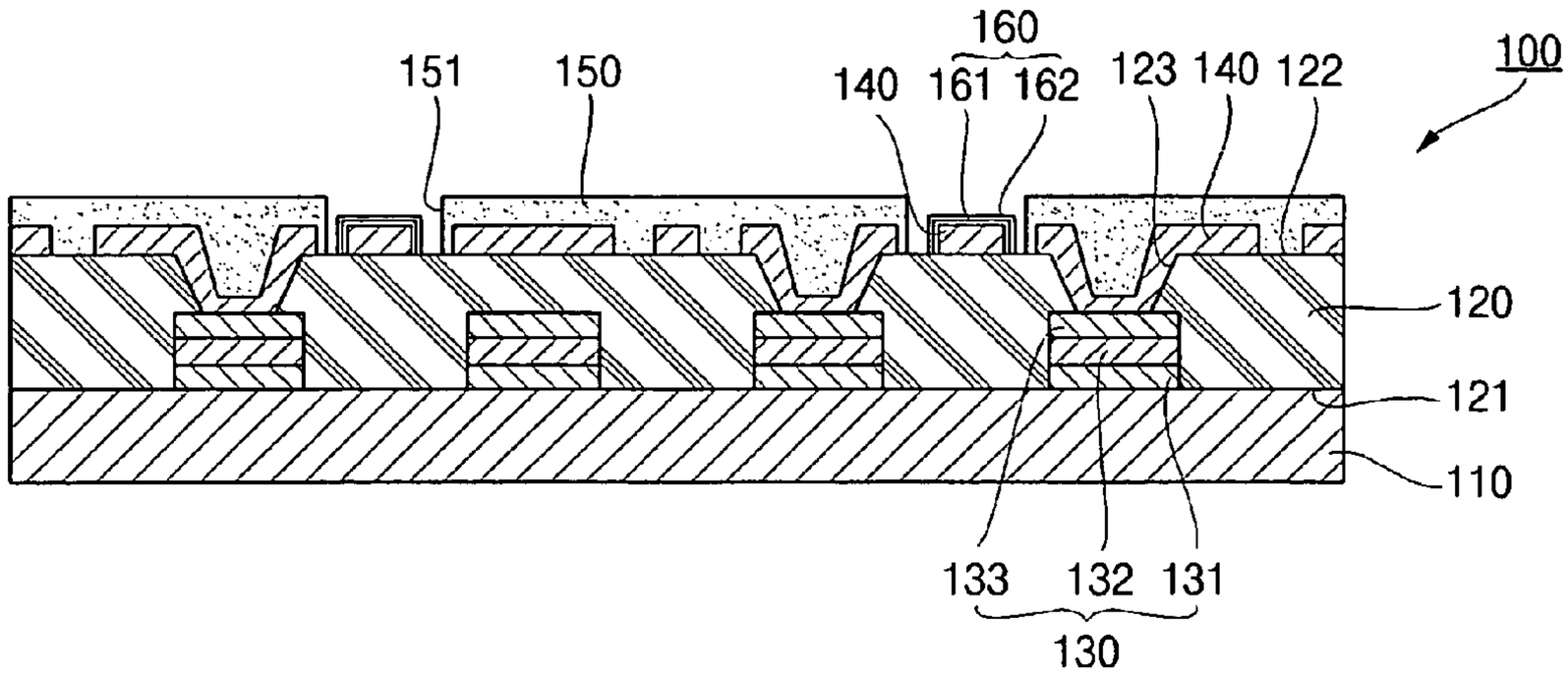



FIG.1

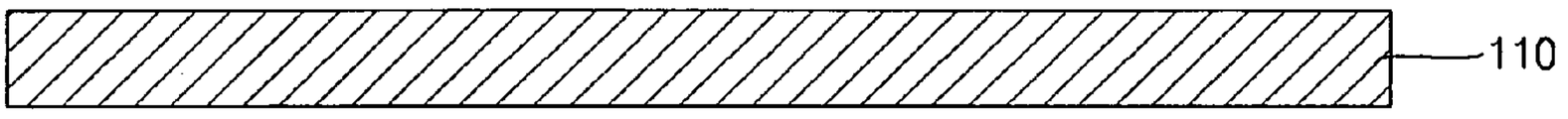



FIG.1A

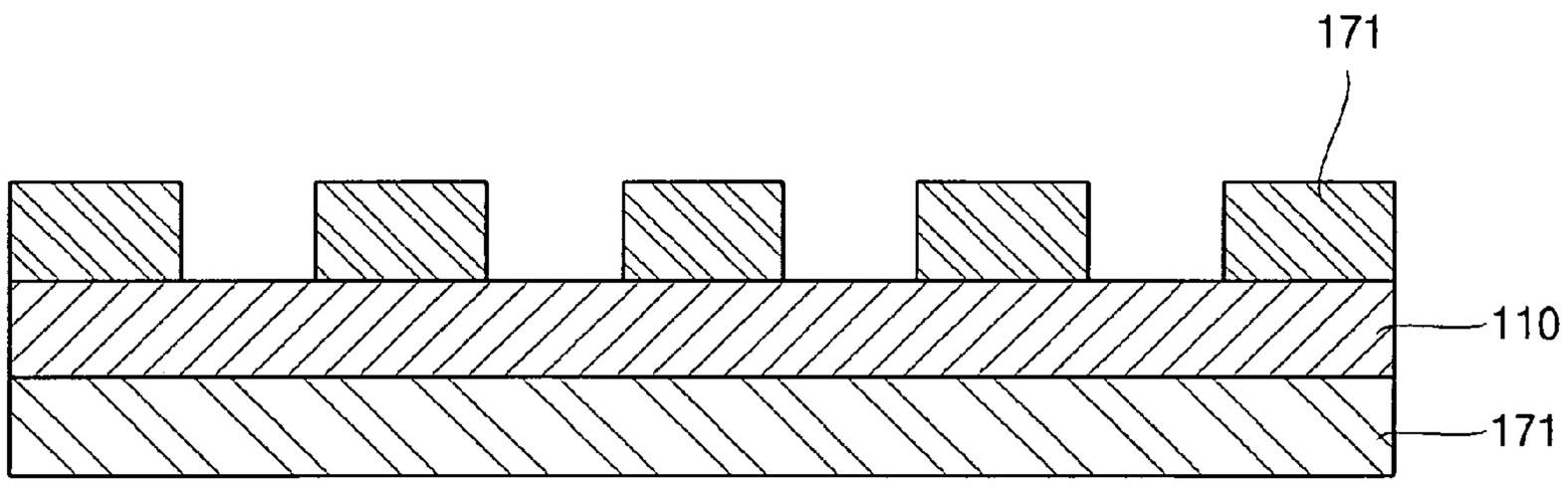



FIG.1B

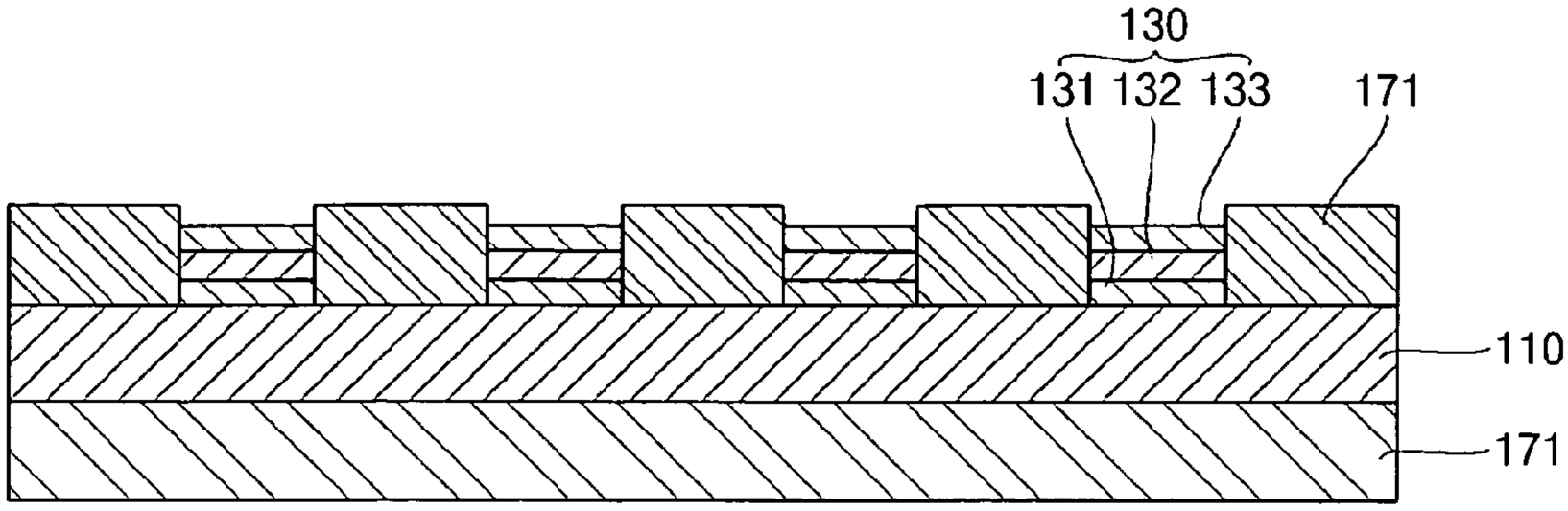



FIG.1C

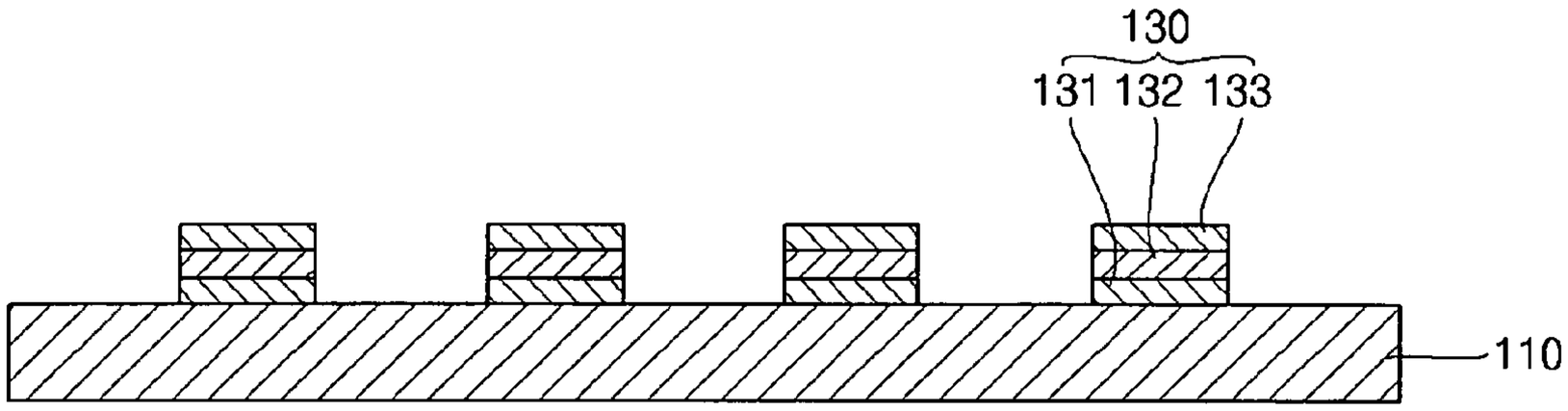



FIG.1D

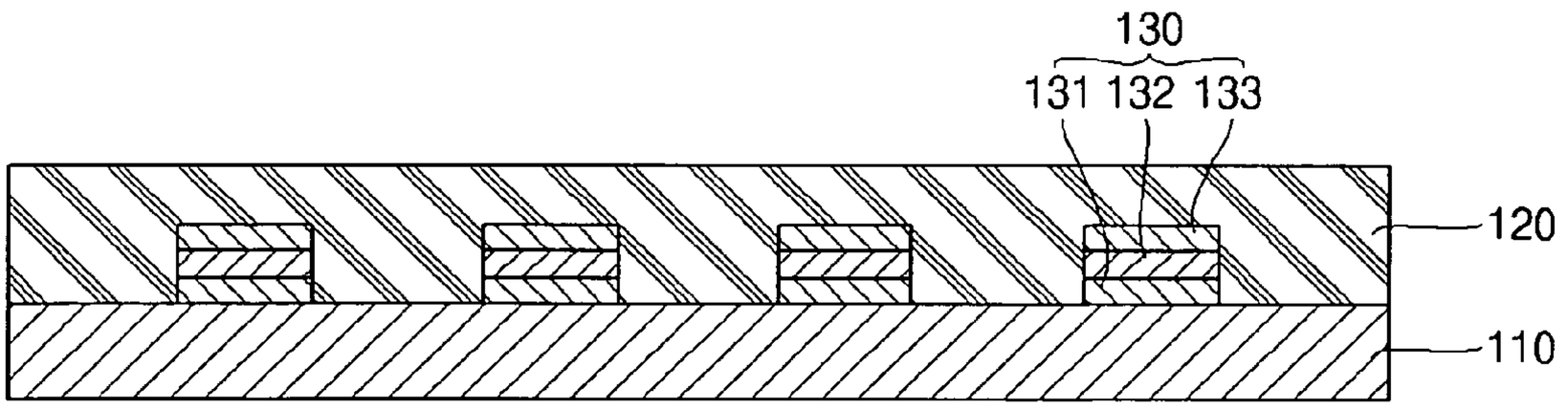



FIG.1E

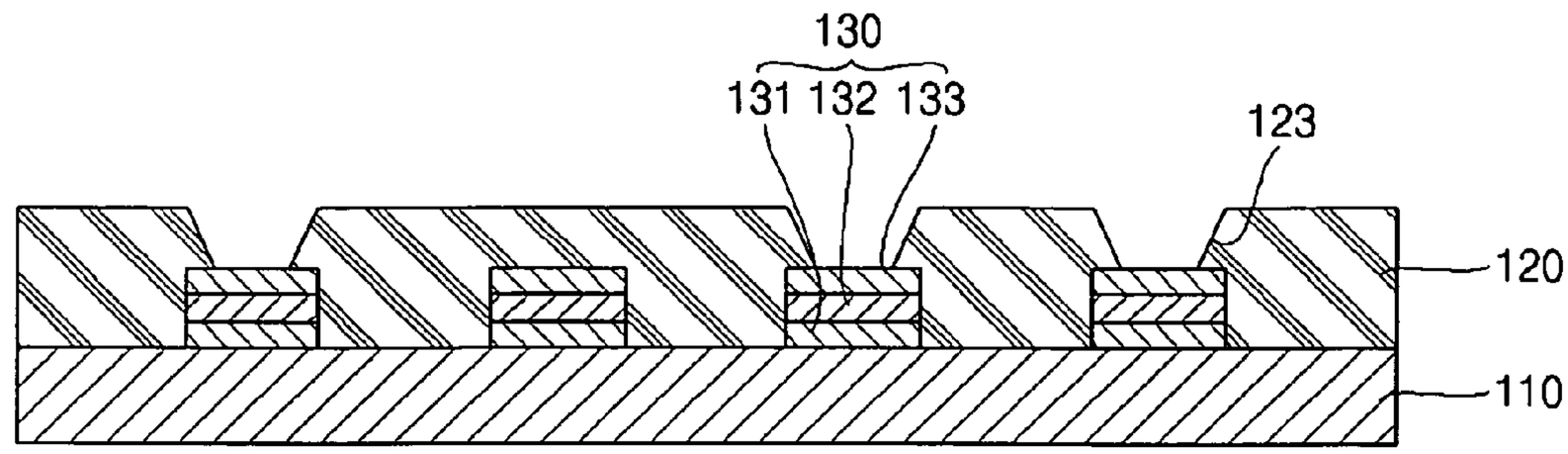



FIG.1F

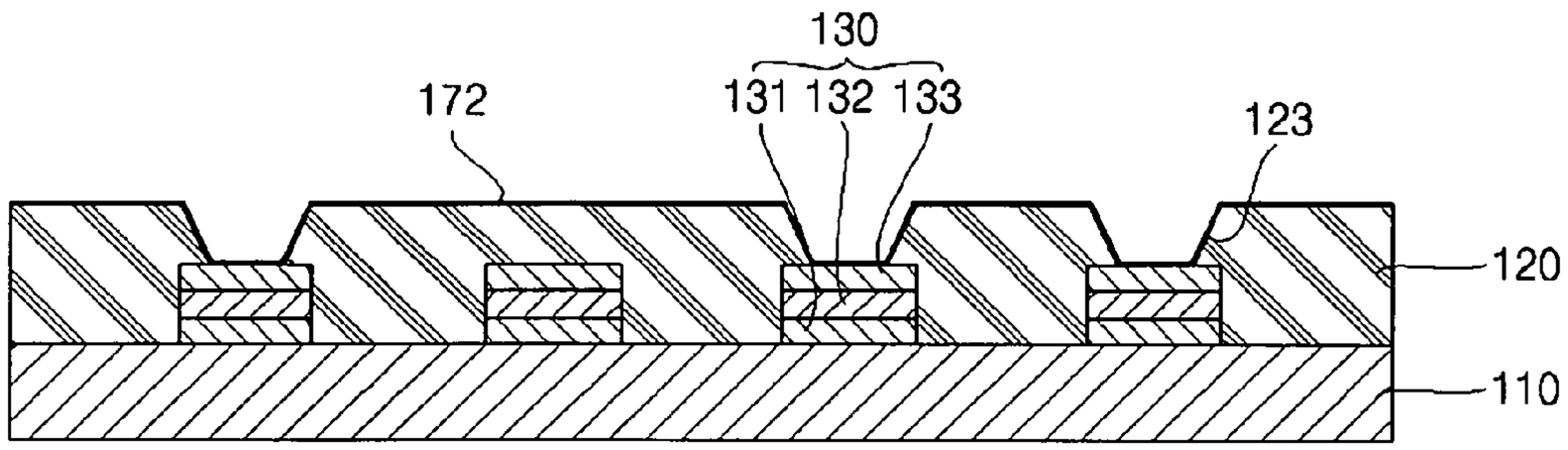



FIG.1G

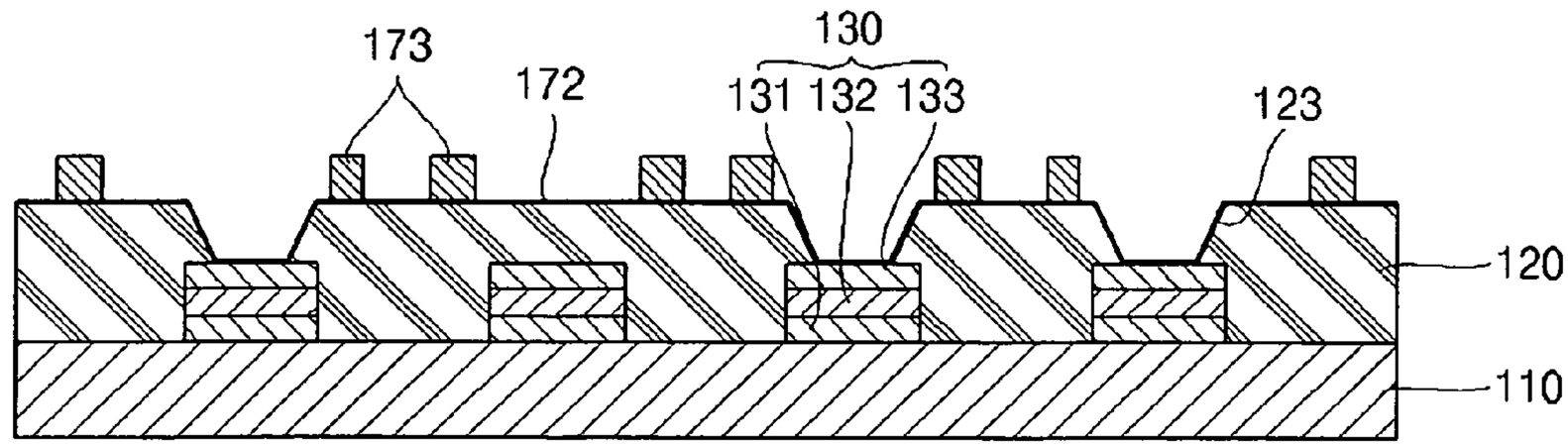



FIG.1H

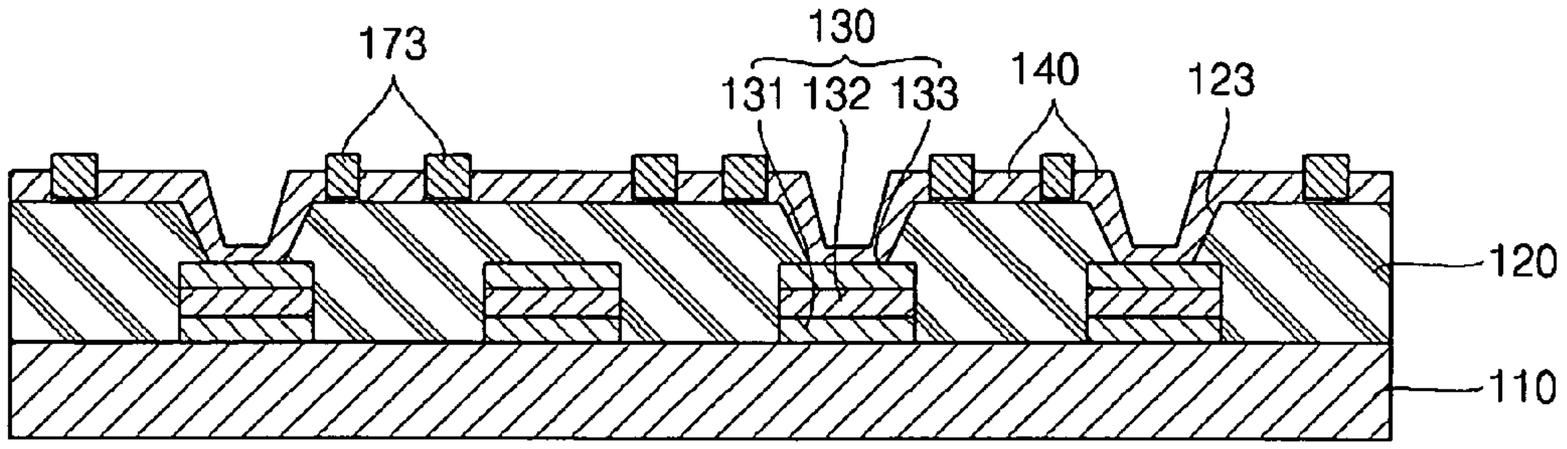
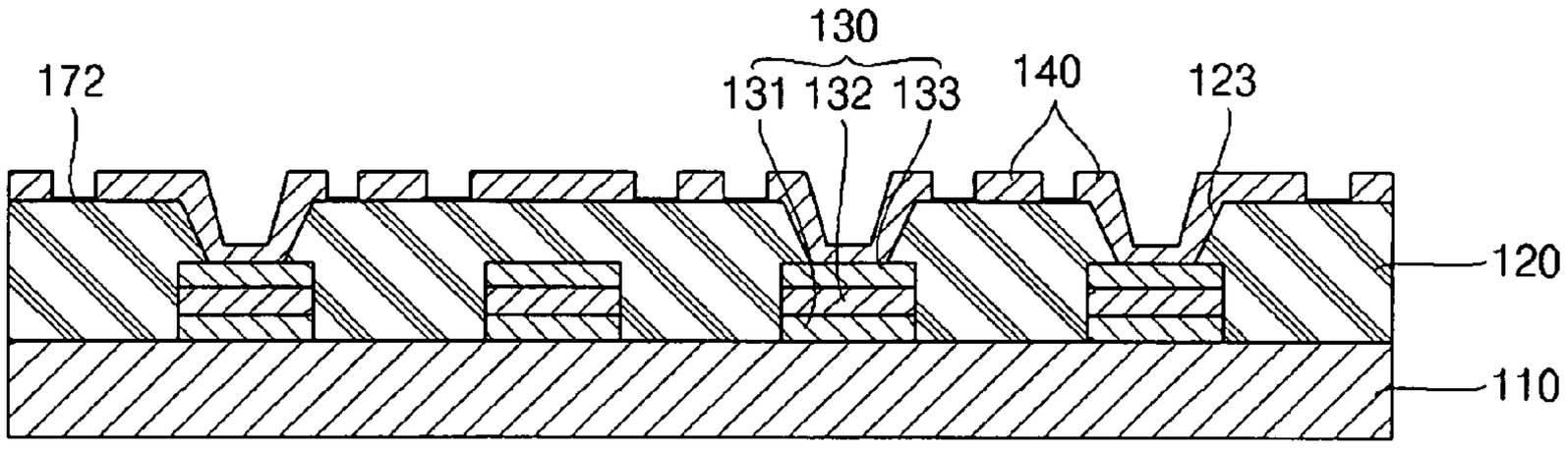



FIG.1I

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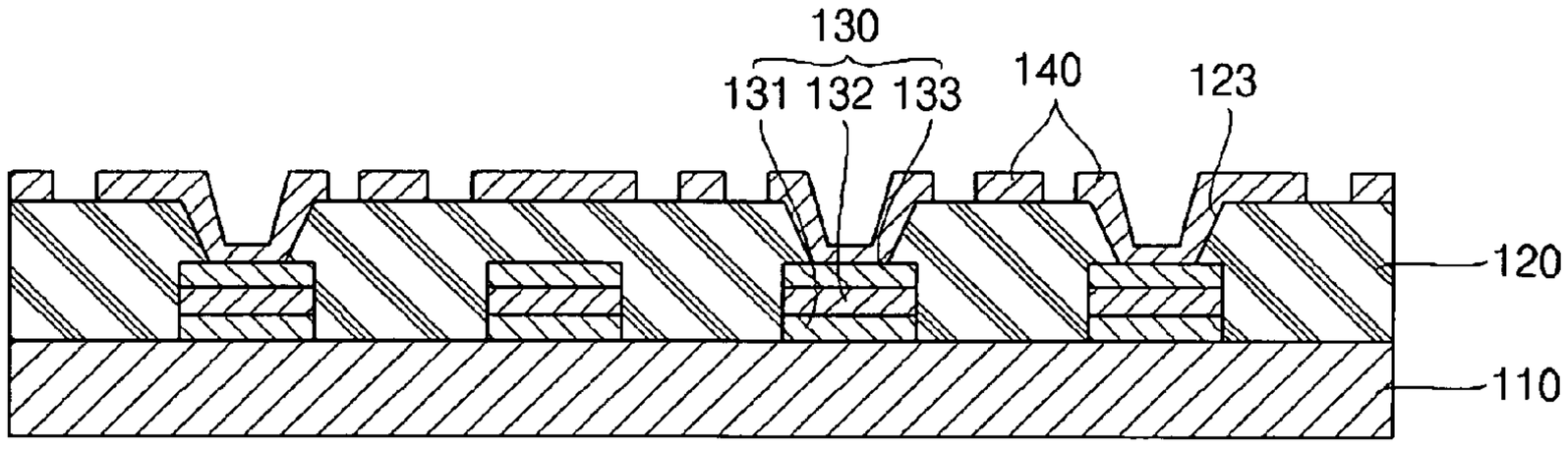


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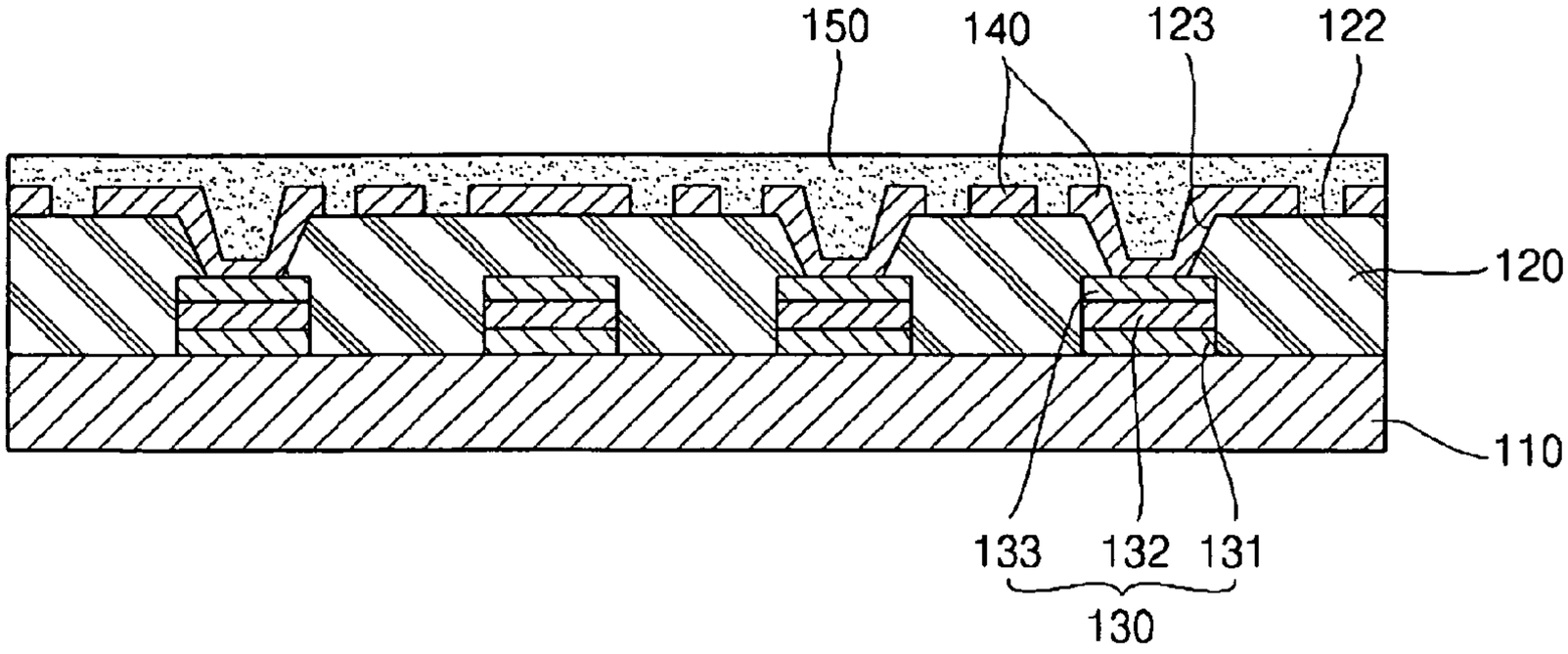
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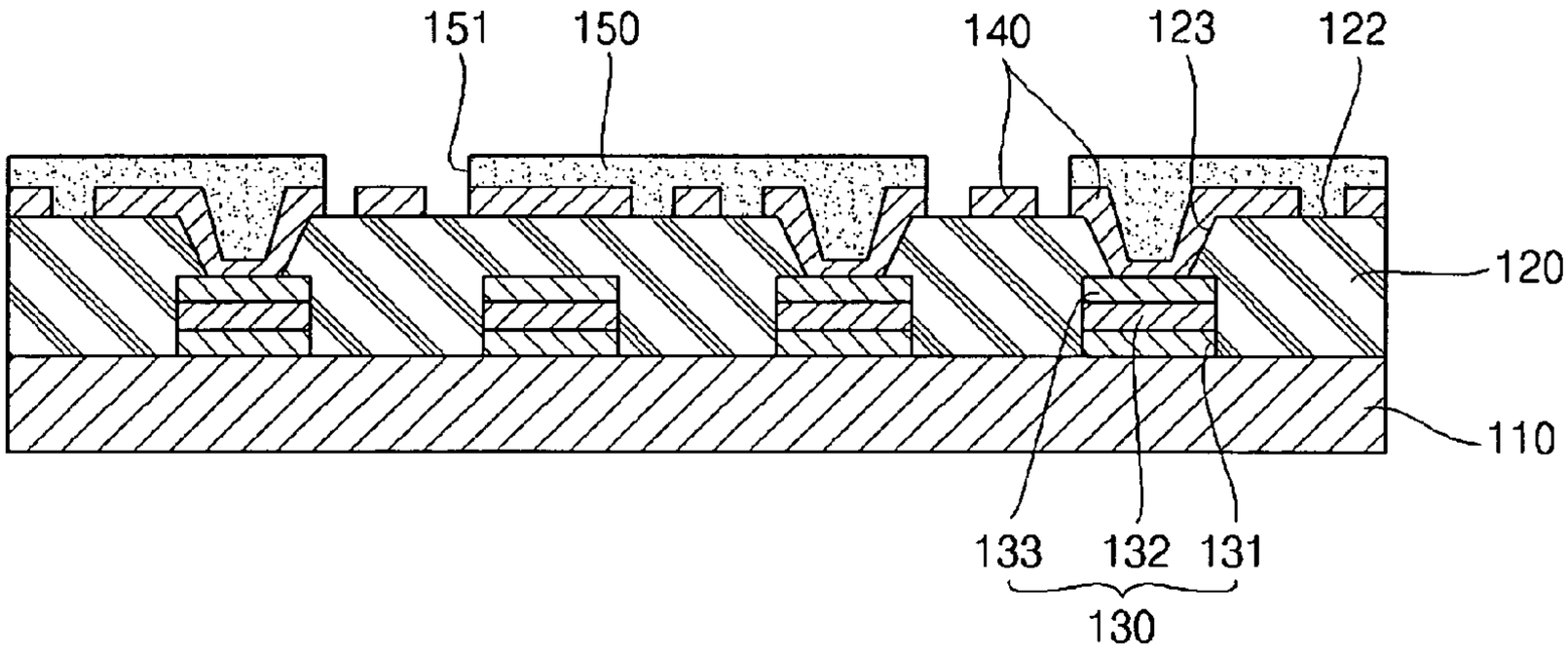
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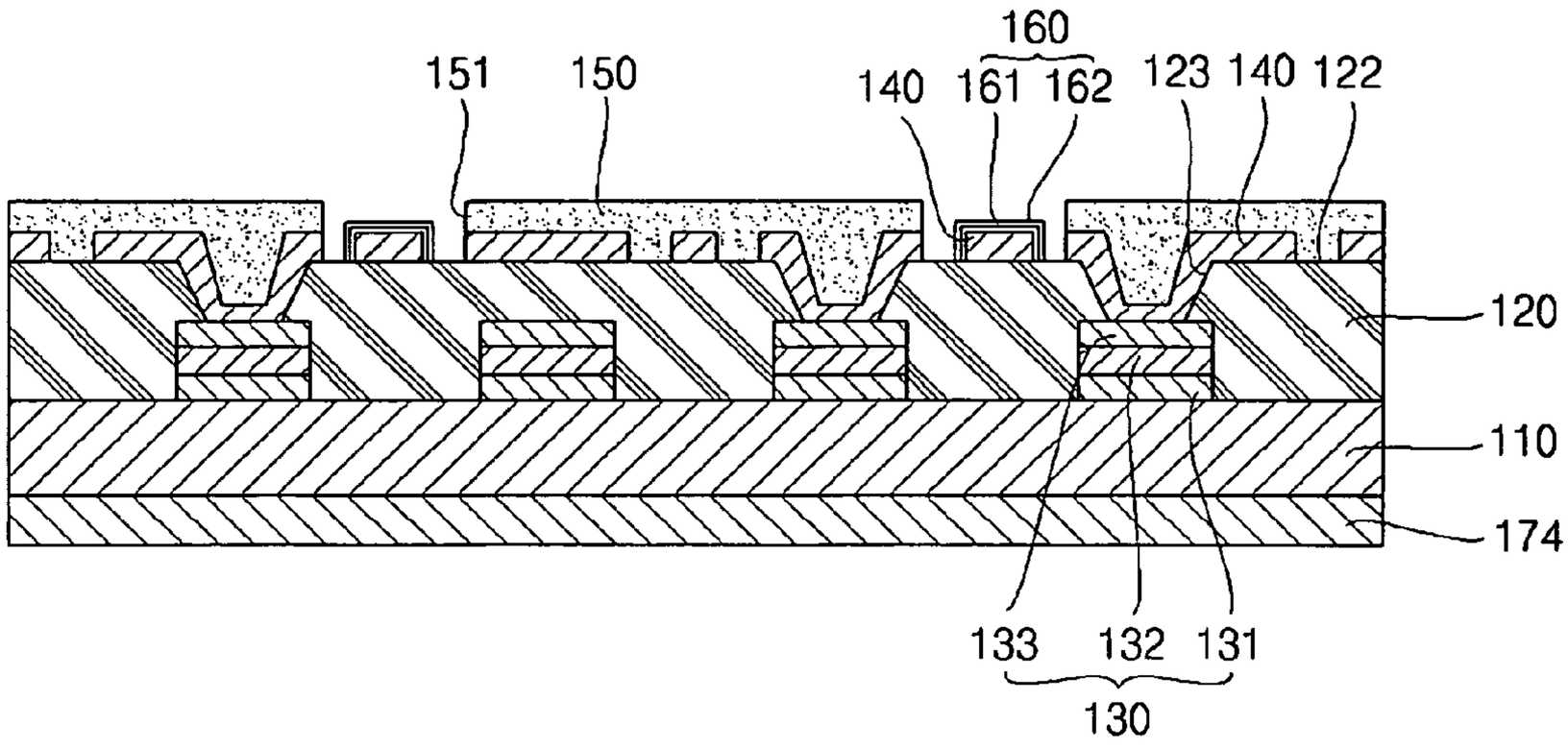
FIG.1M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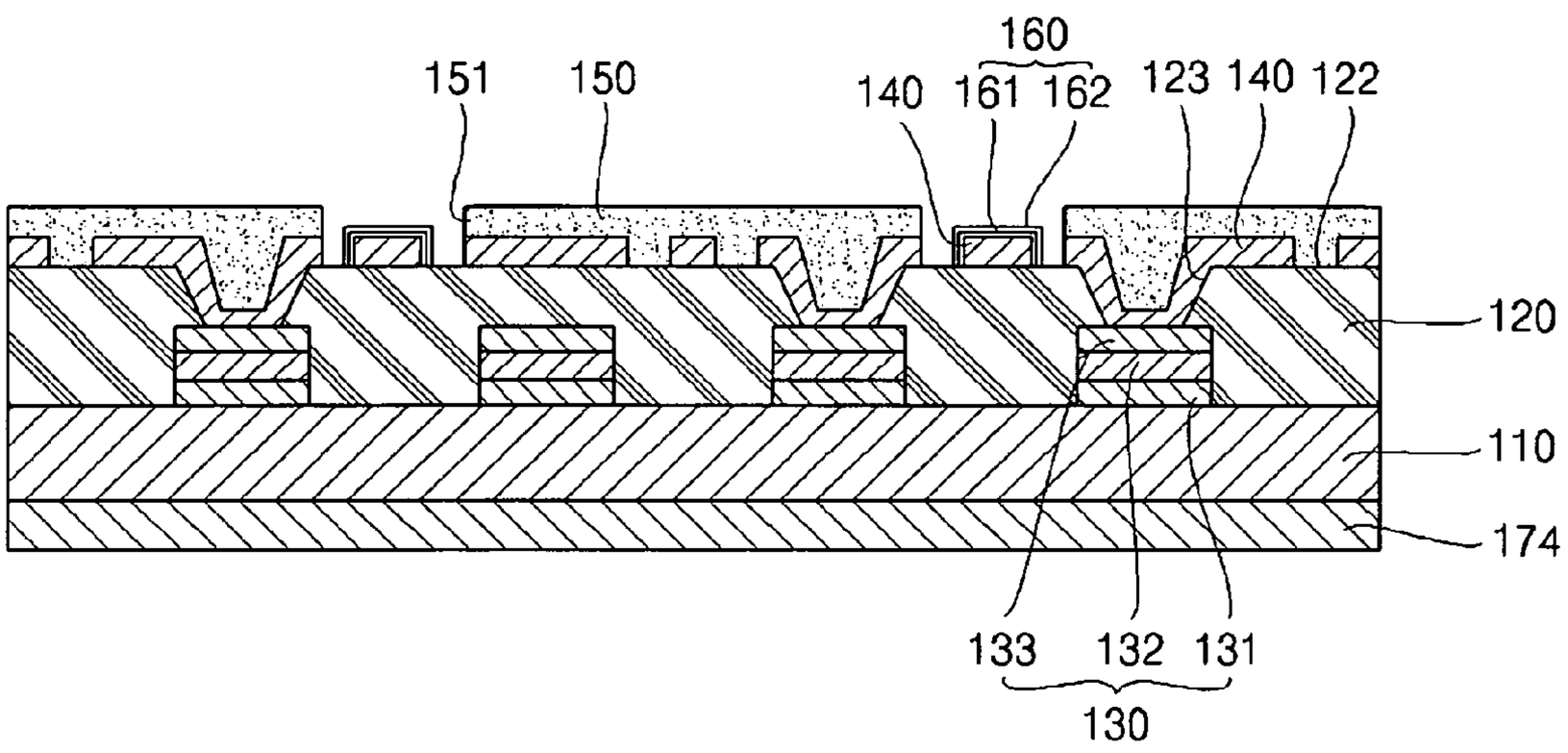
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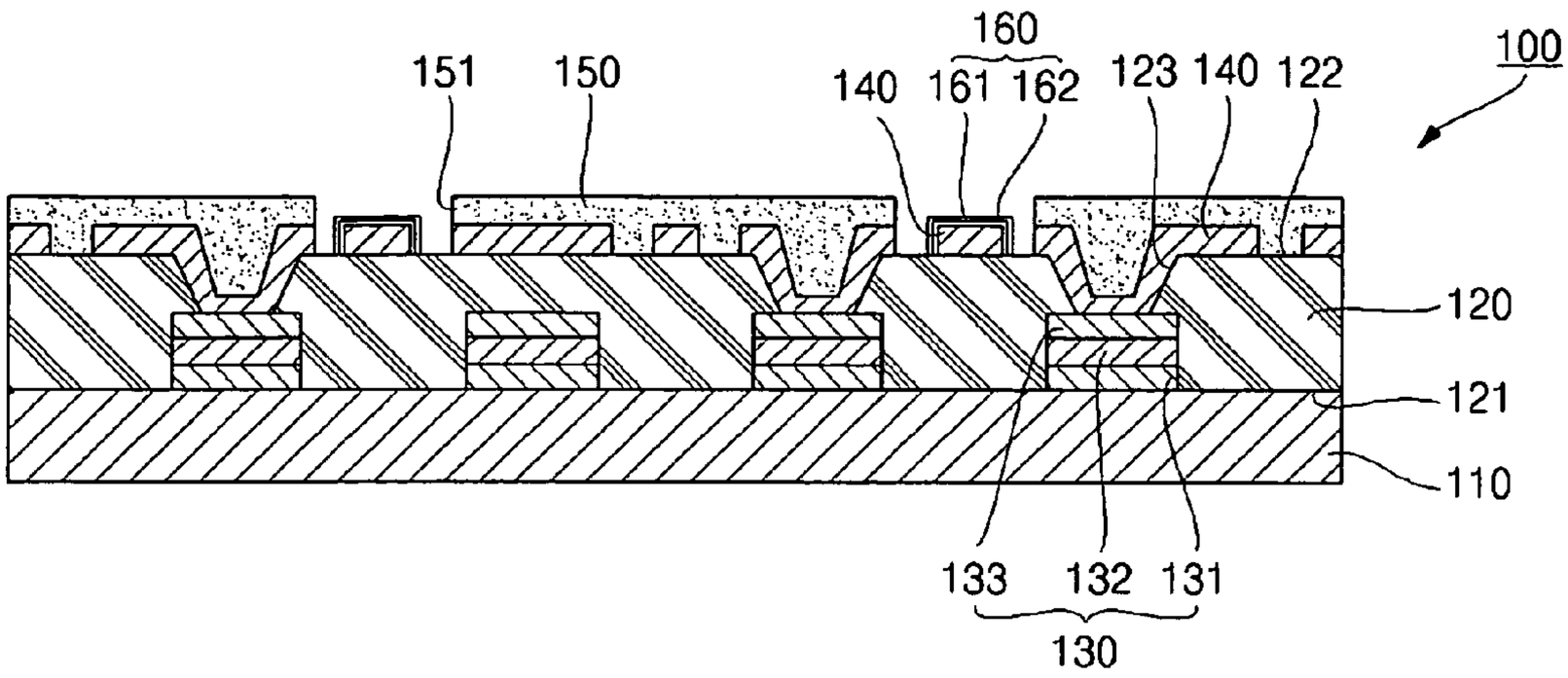
FIG.1O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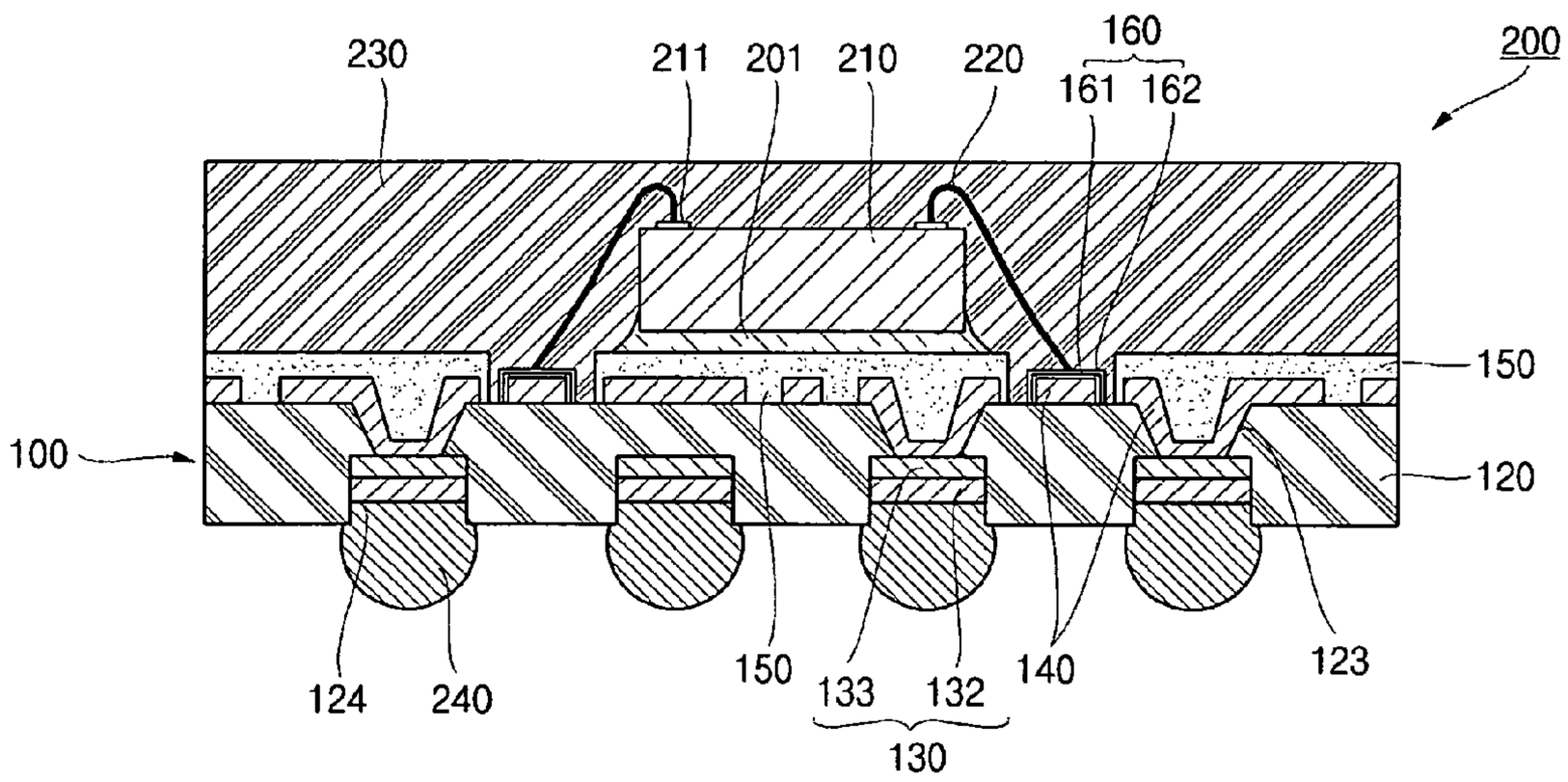
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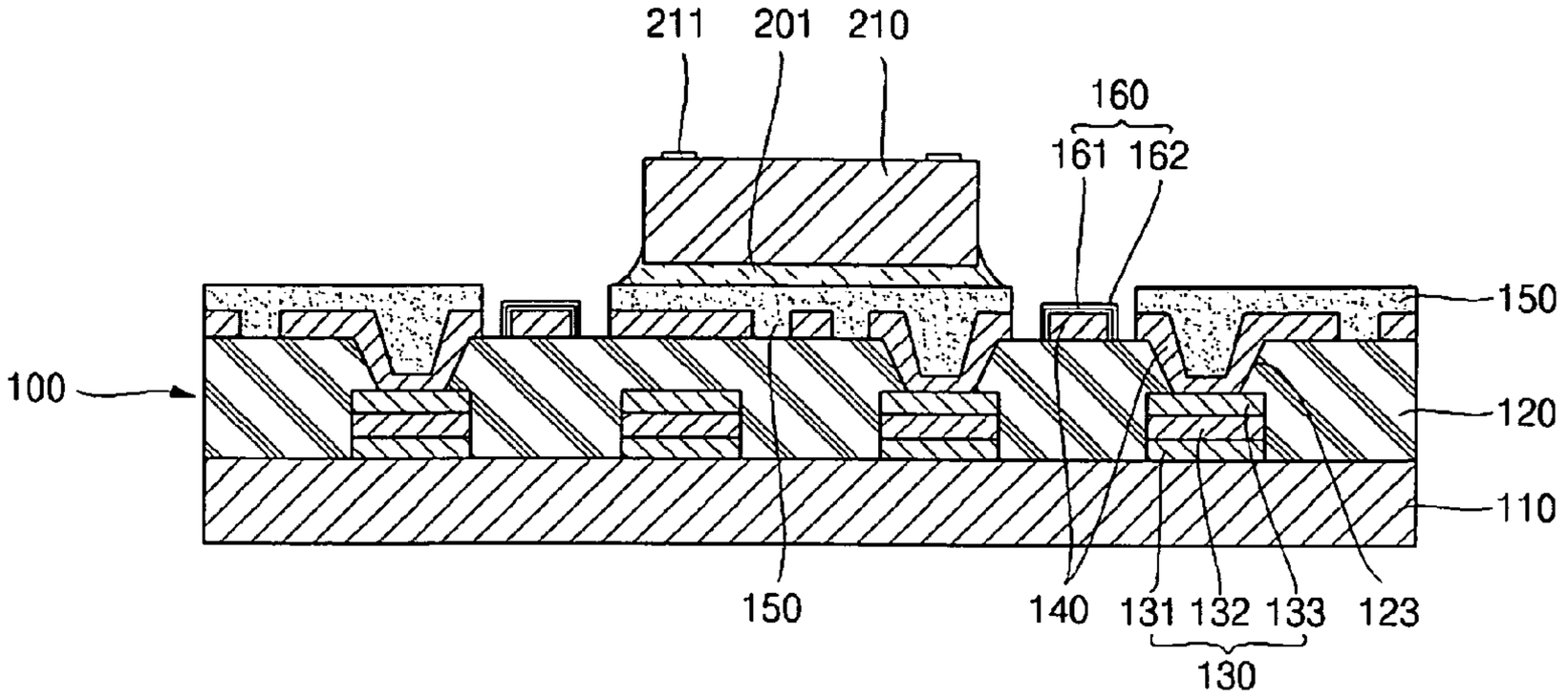
FIG.2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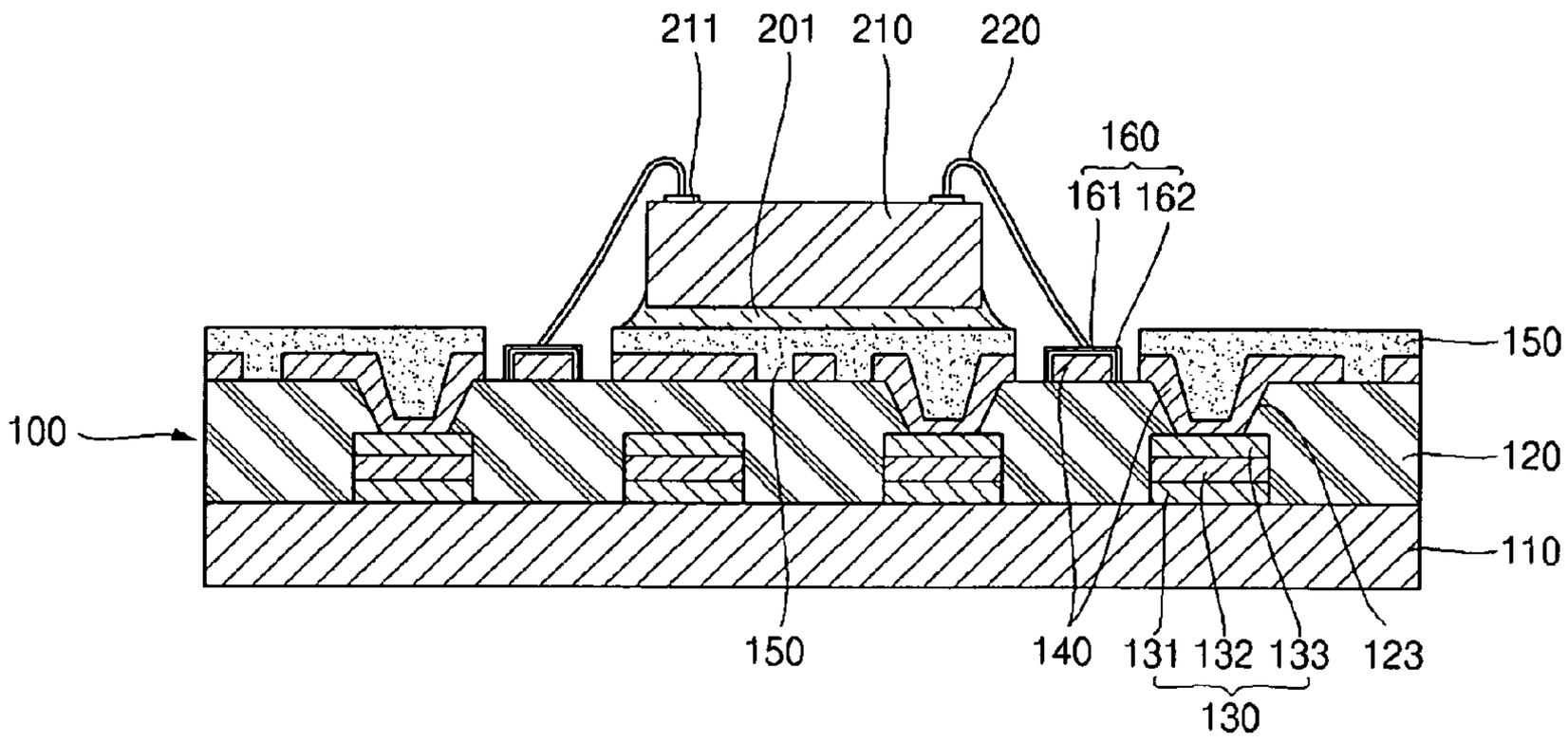
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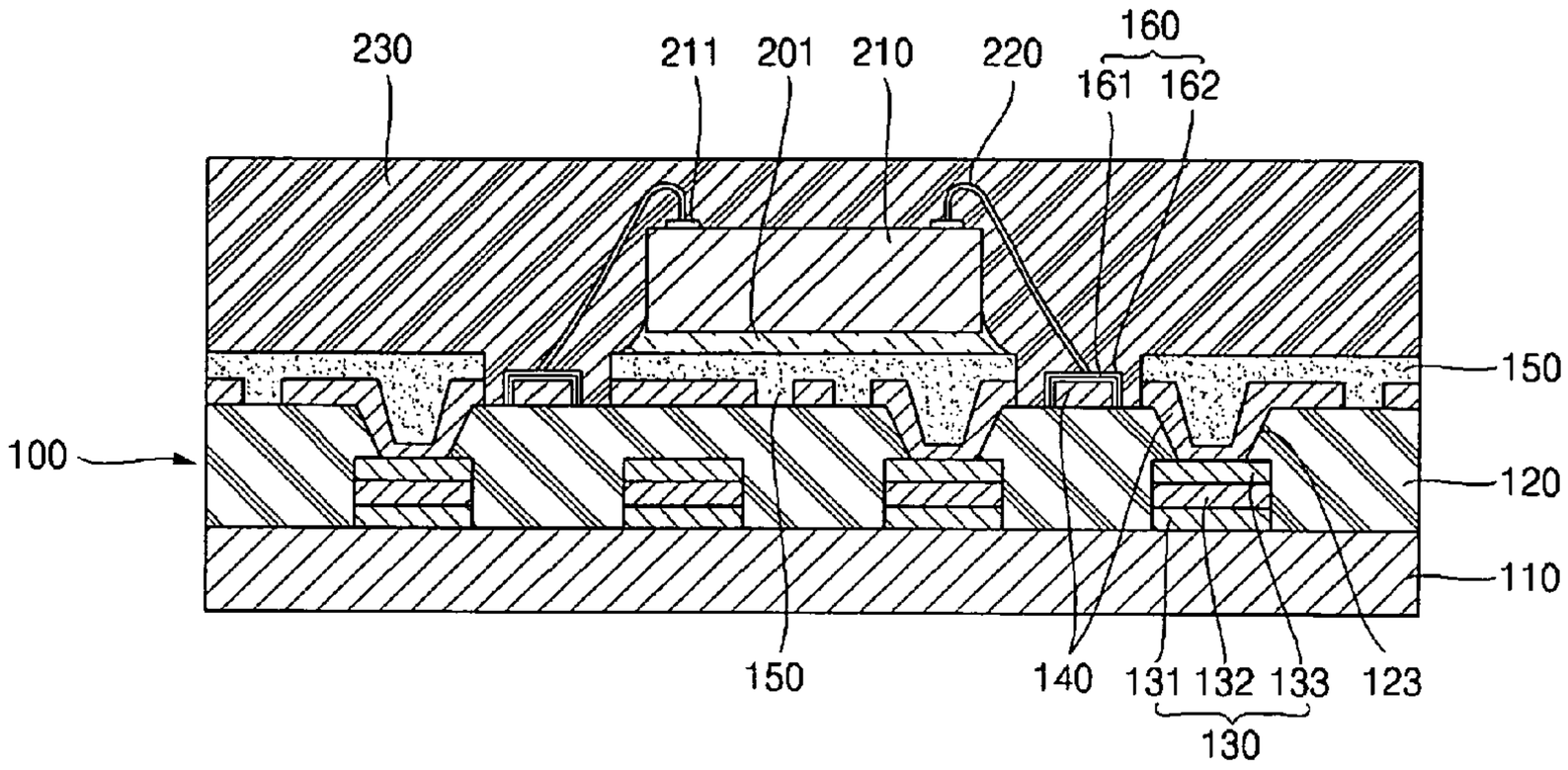
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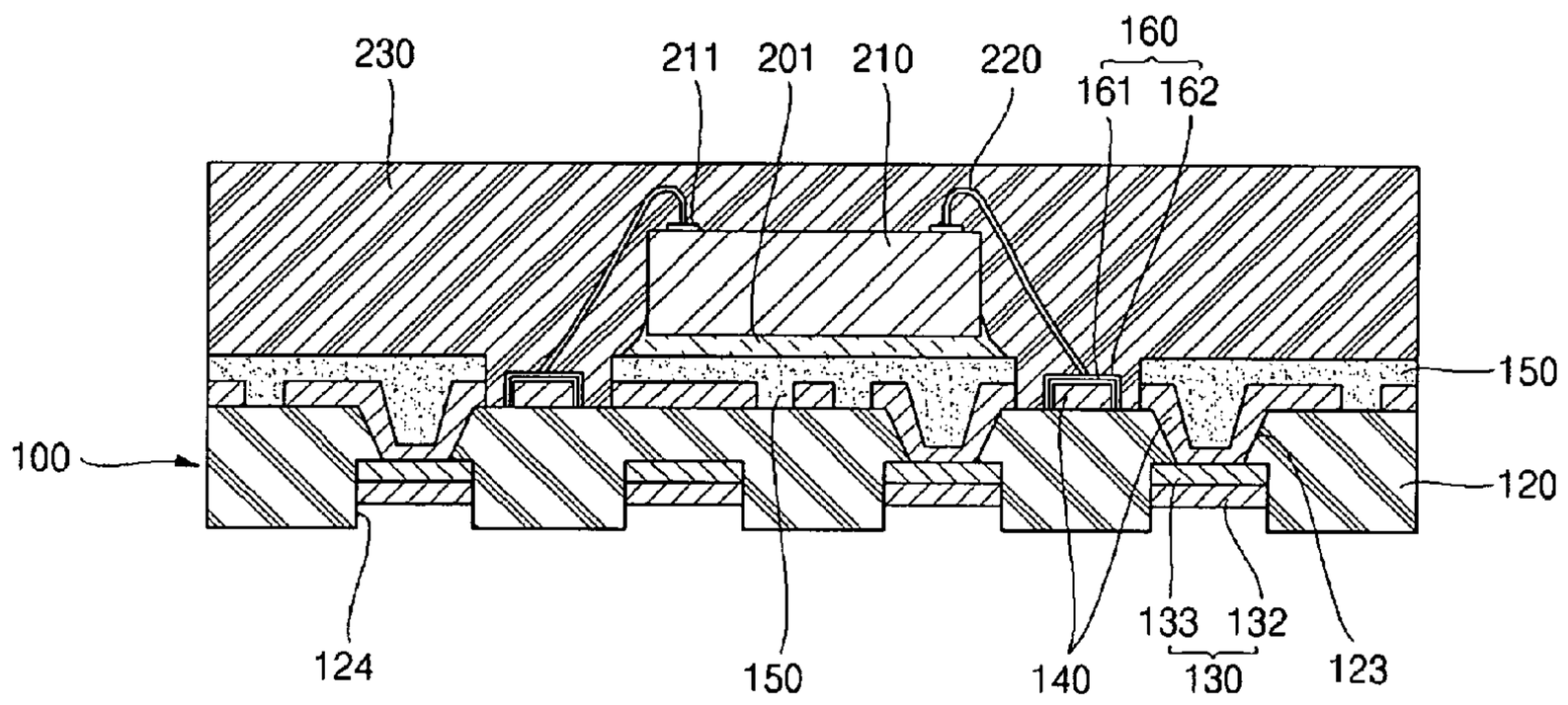
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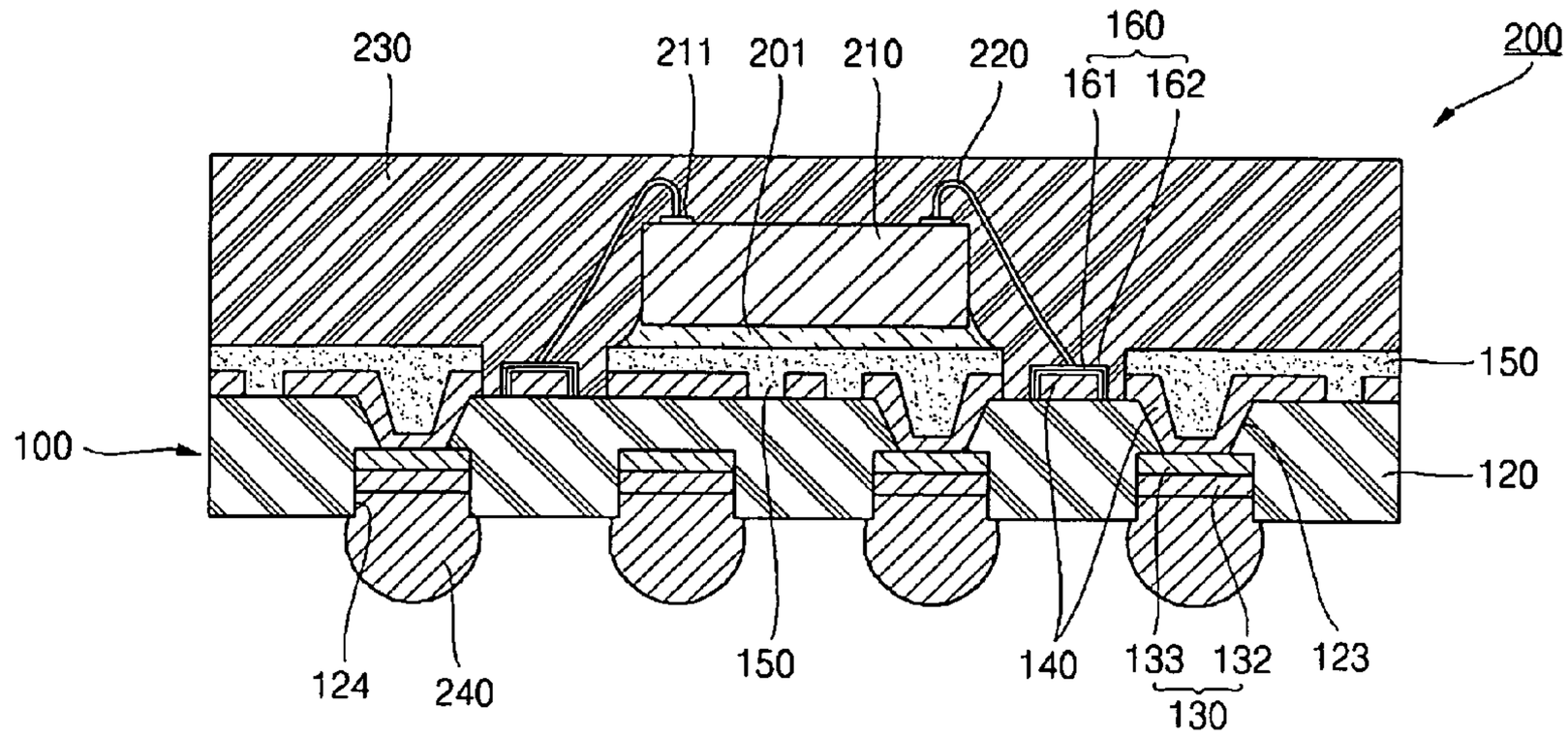
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FIG.2E

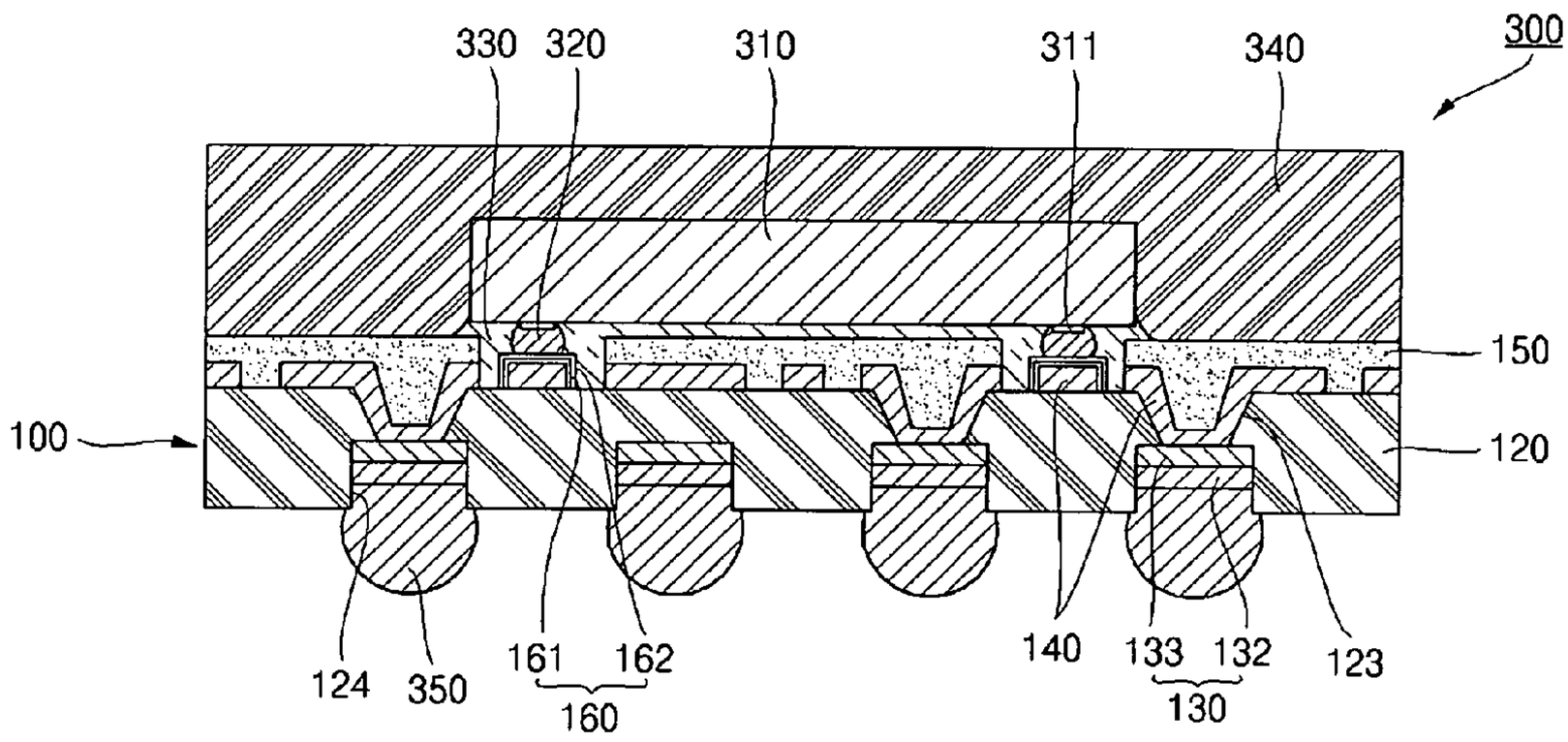
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FIG.3

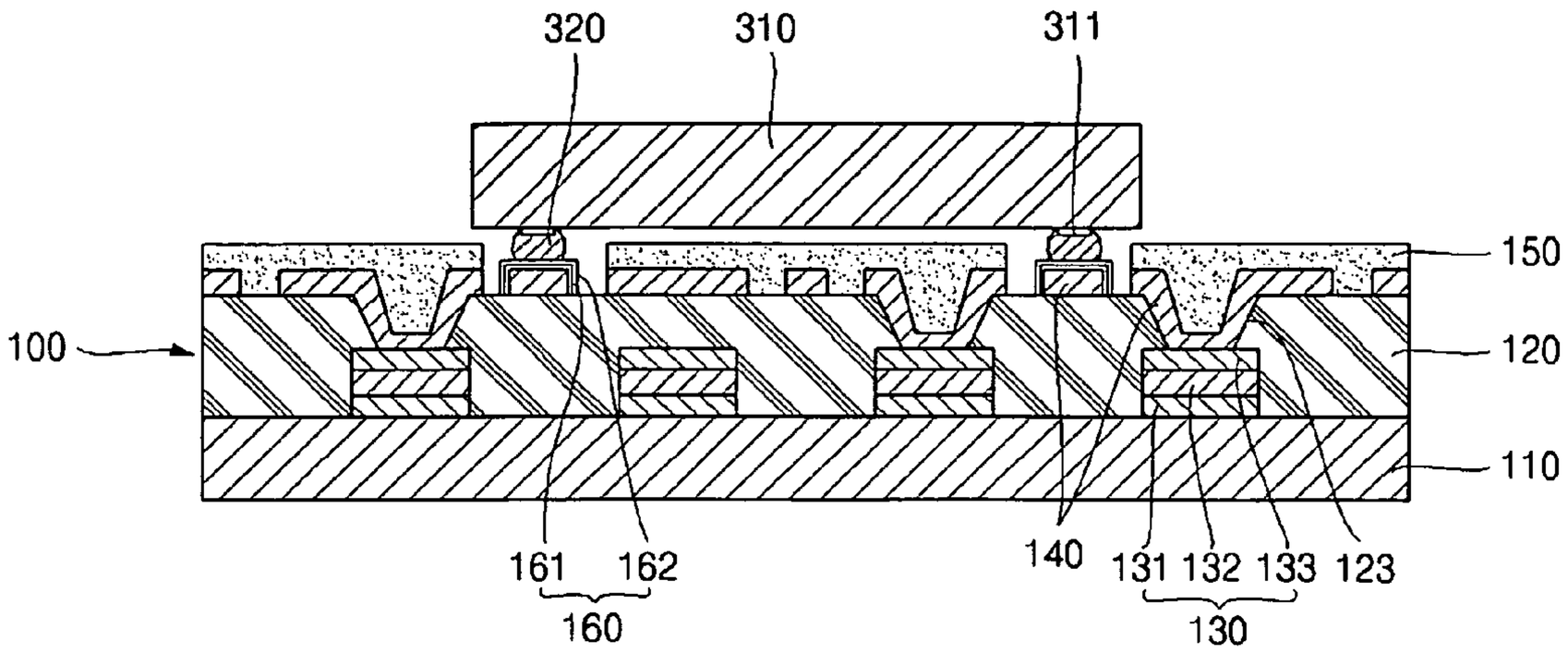
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FIG.3A

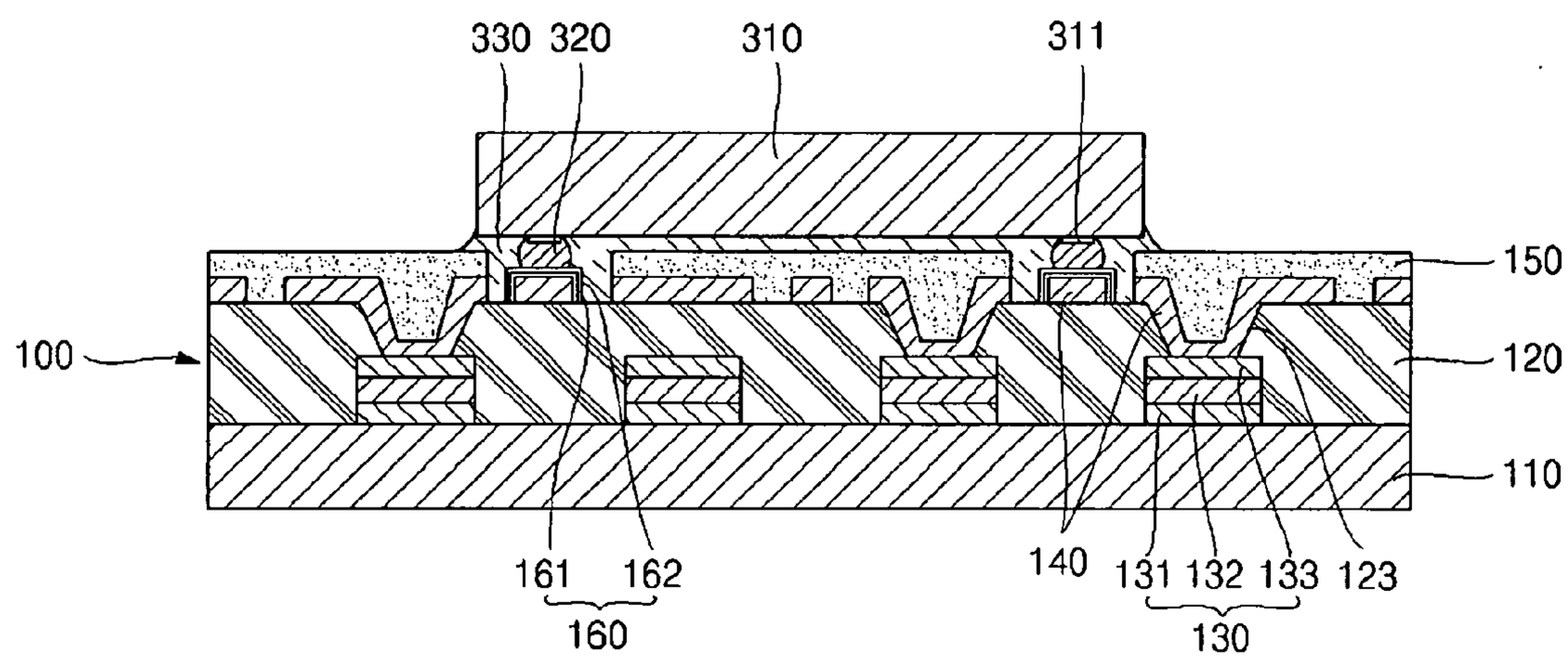
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FIG.3B

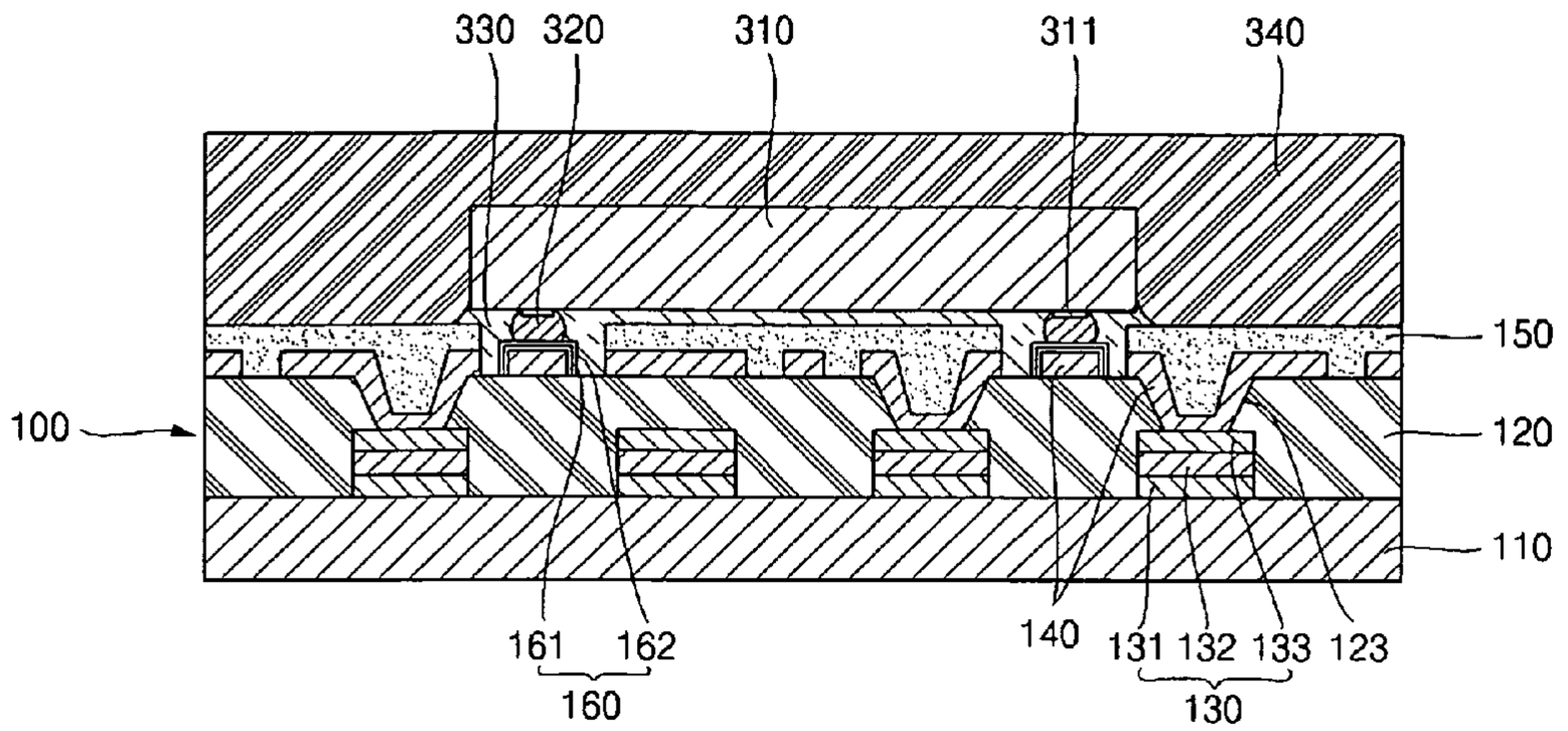
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FIG.3C

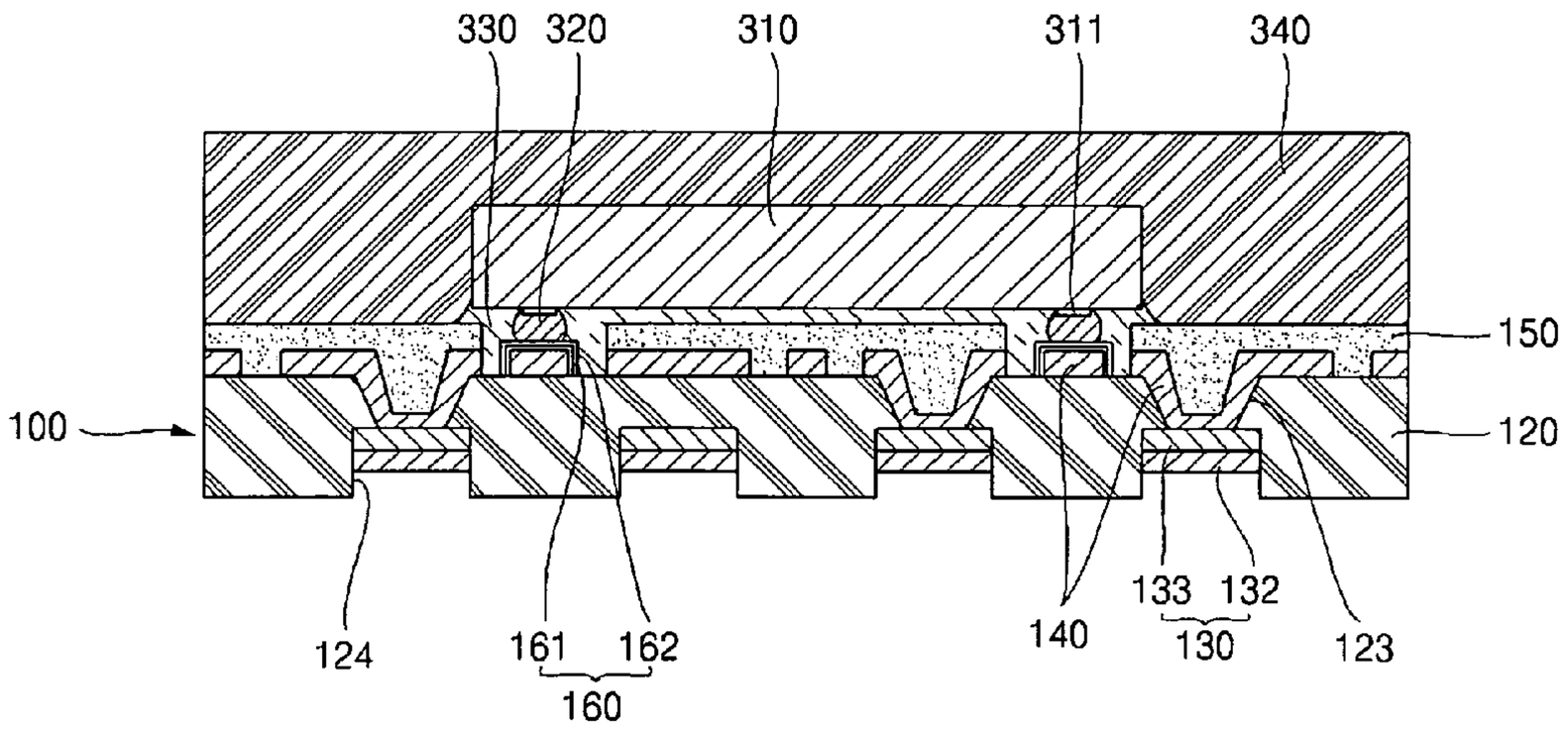
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FIG.3D

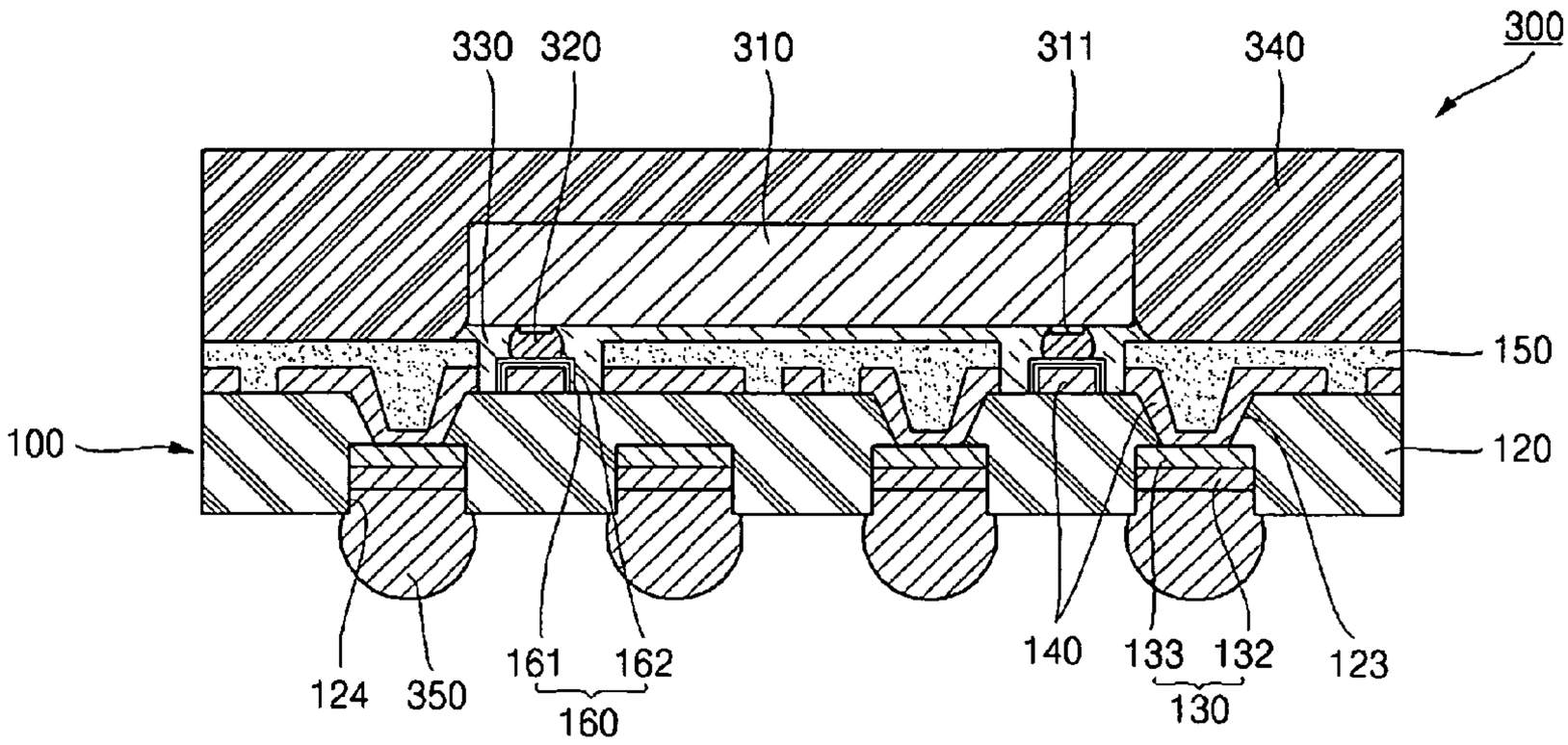
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FIG.3E

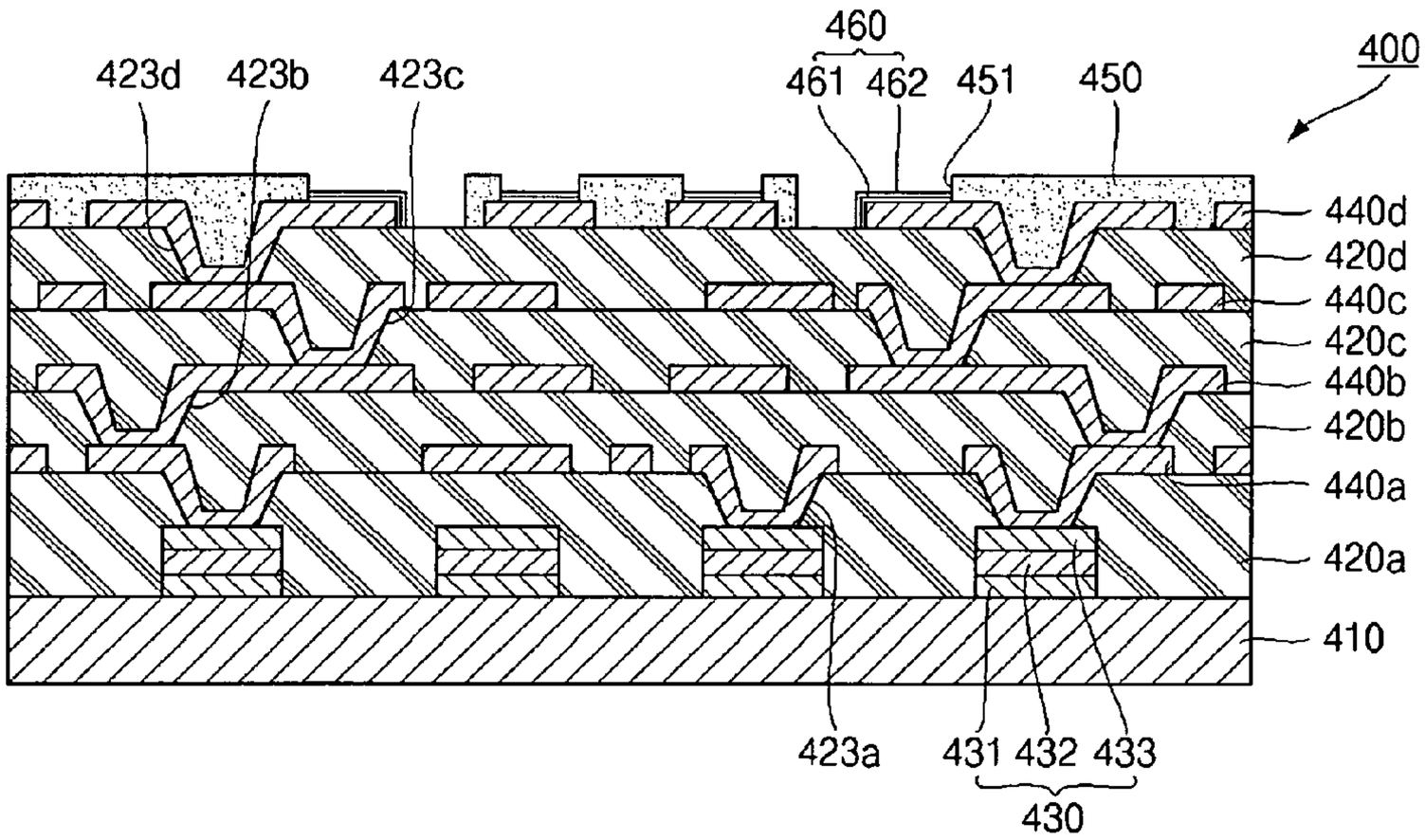
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FIG.4

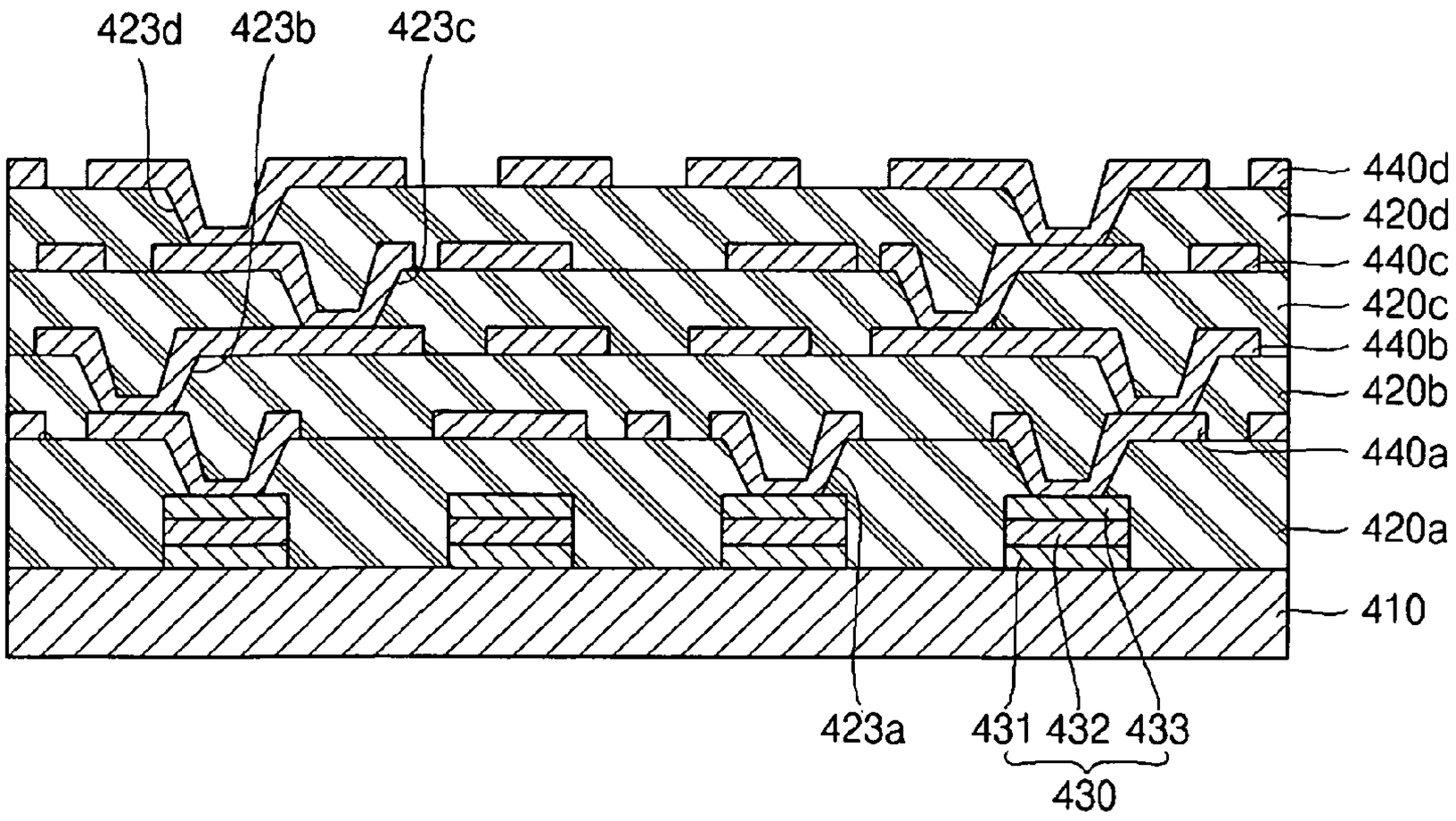
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FIG.4A

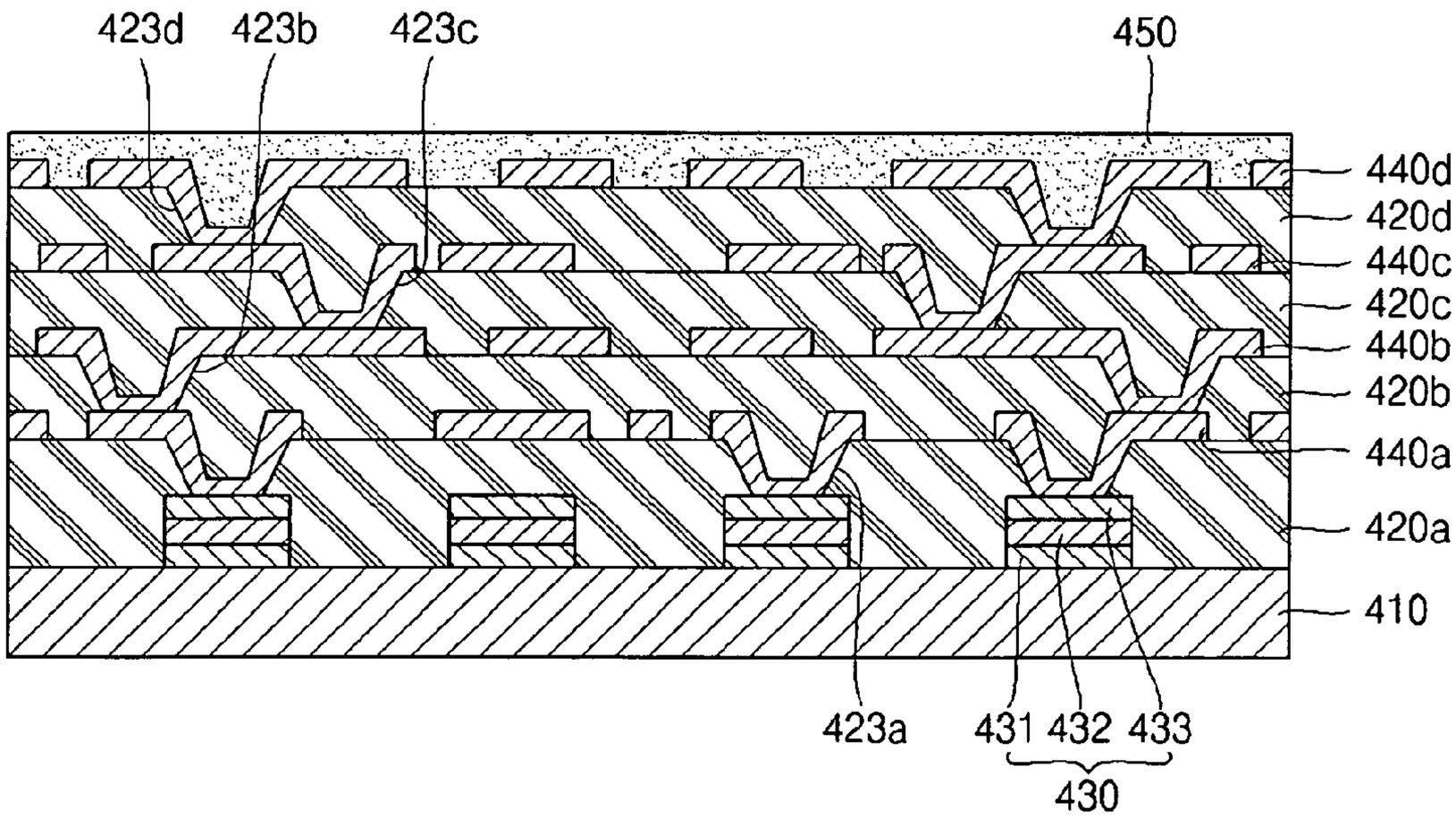
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FIG.4B

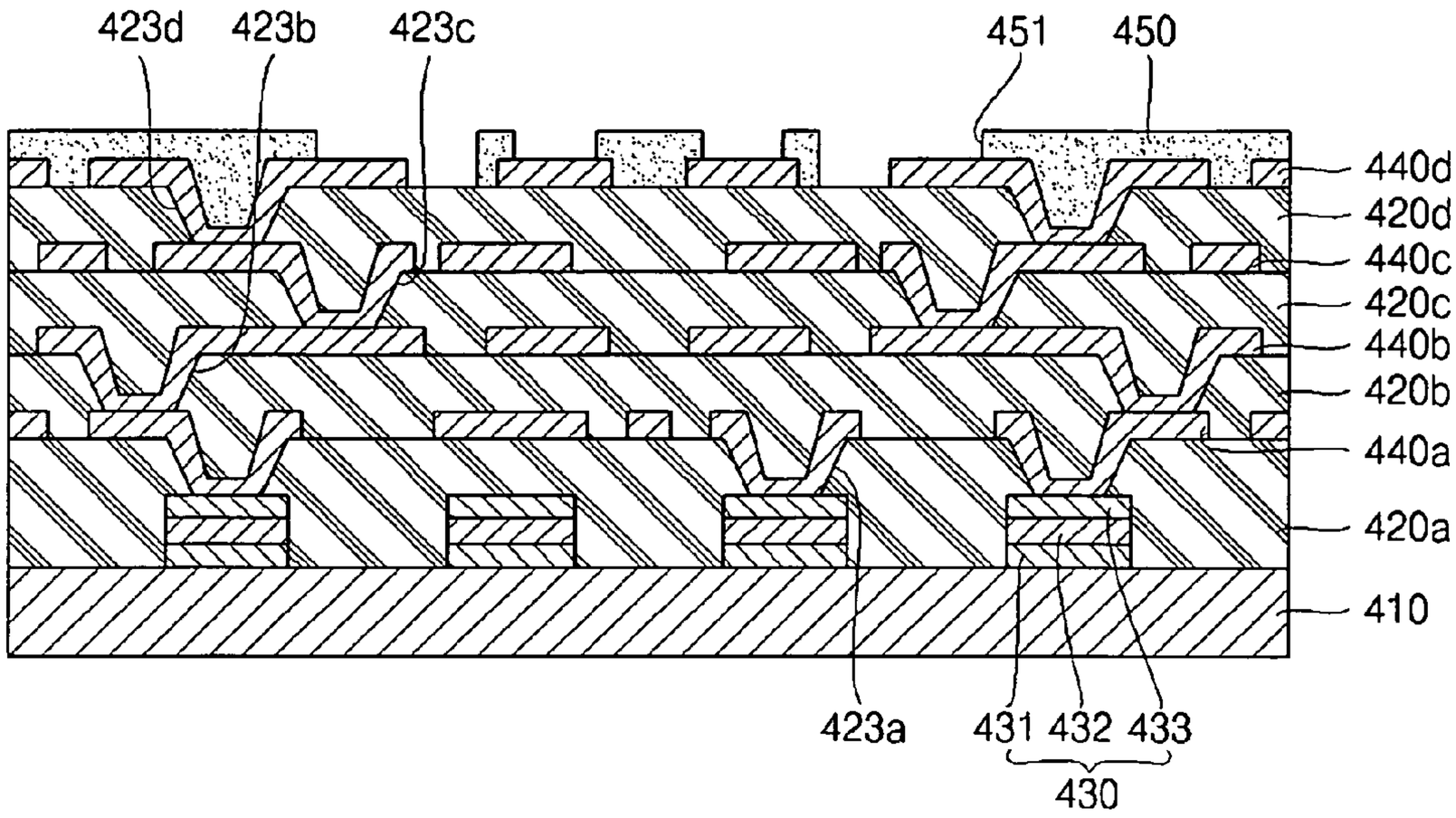
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FIG.4C

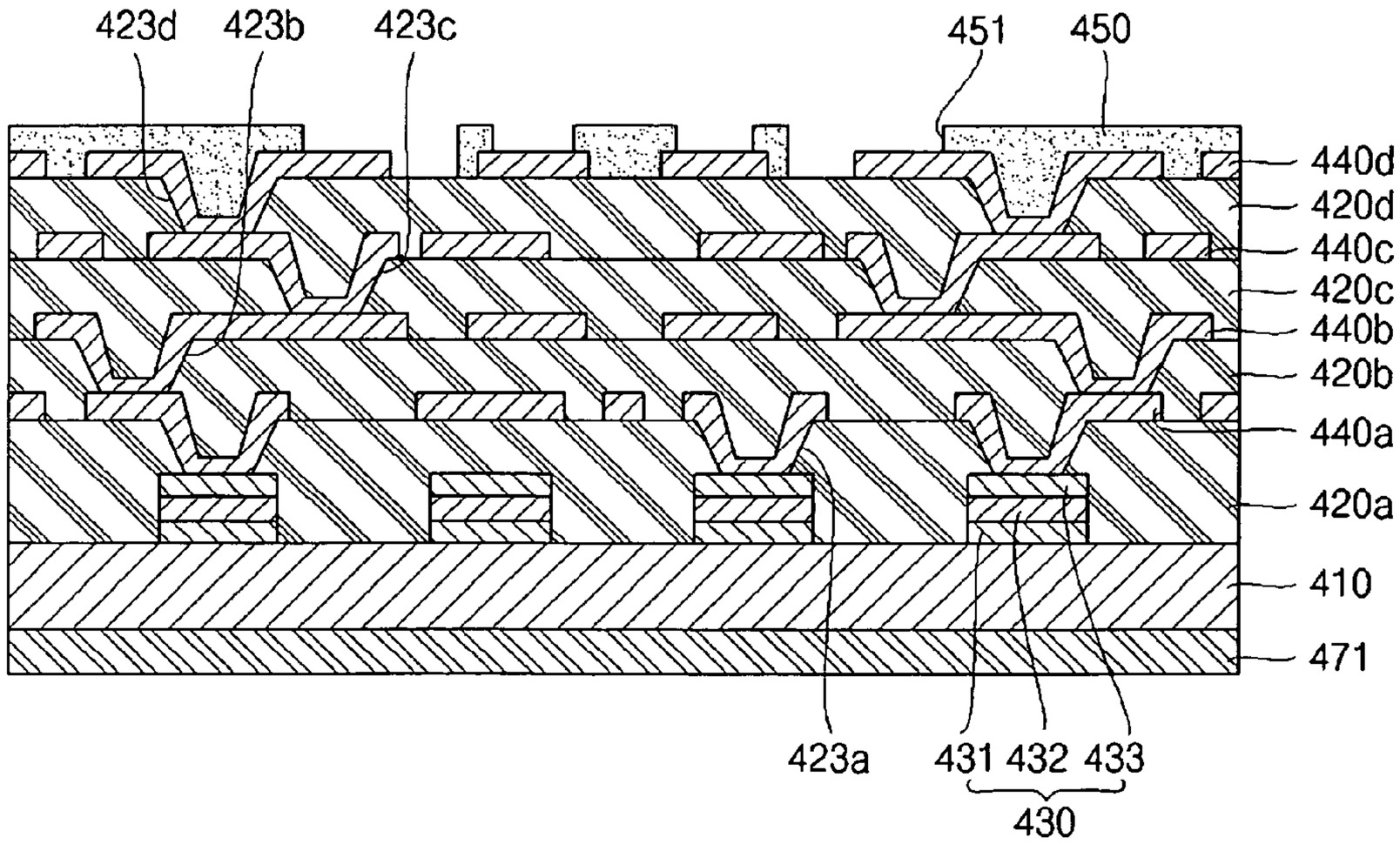
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FIG.4D

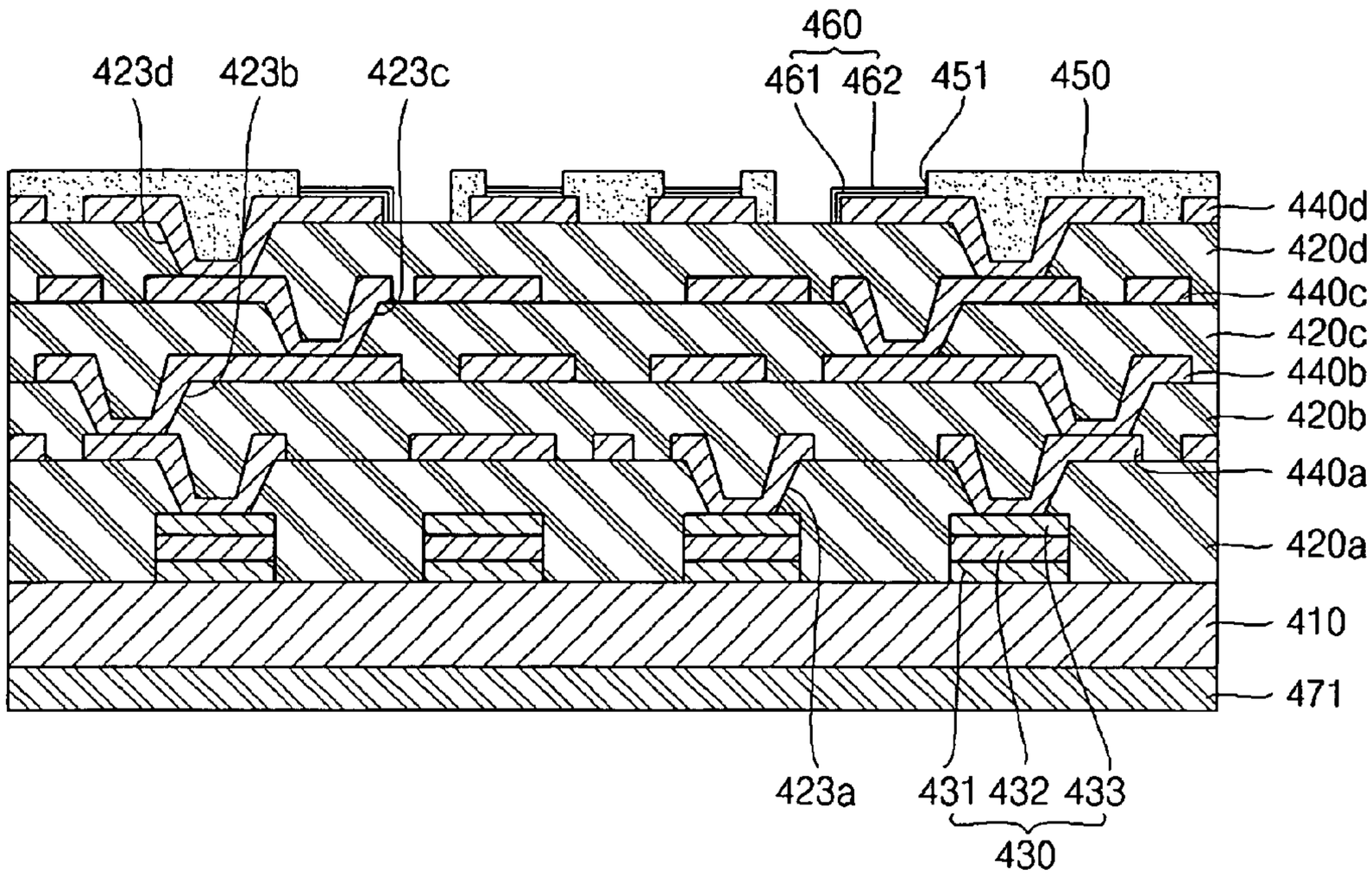
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FIG.4E

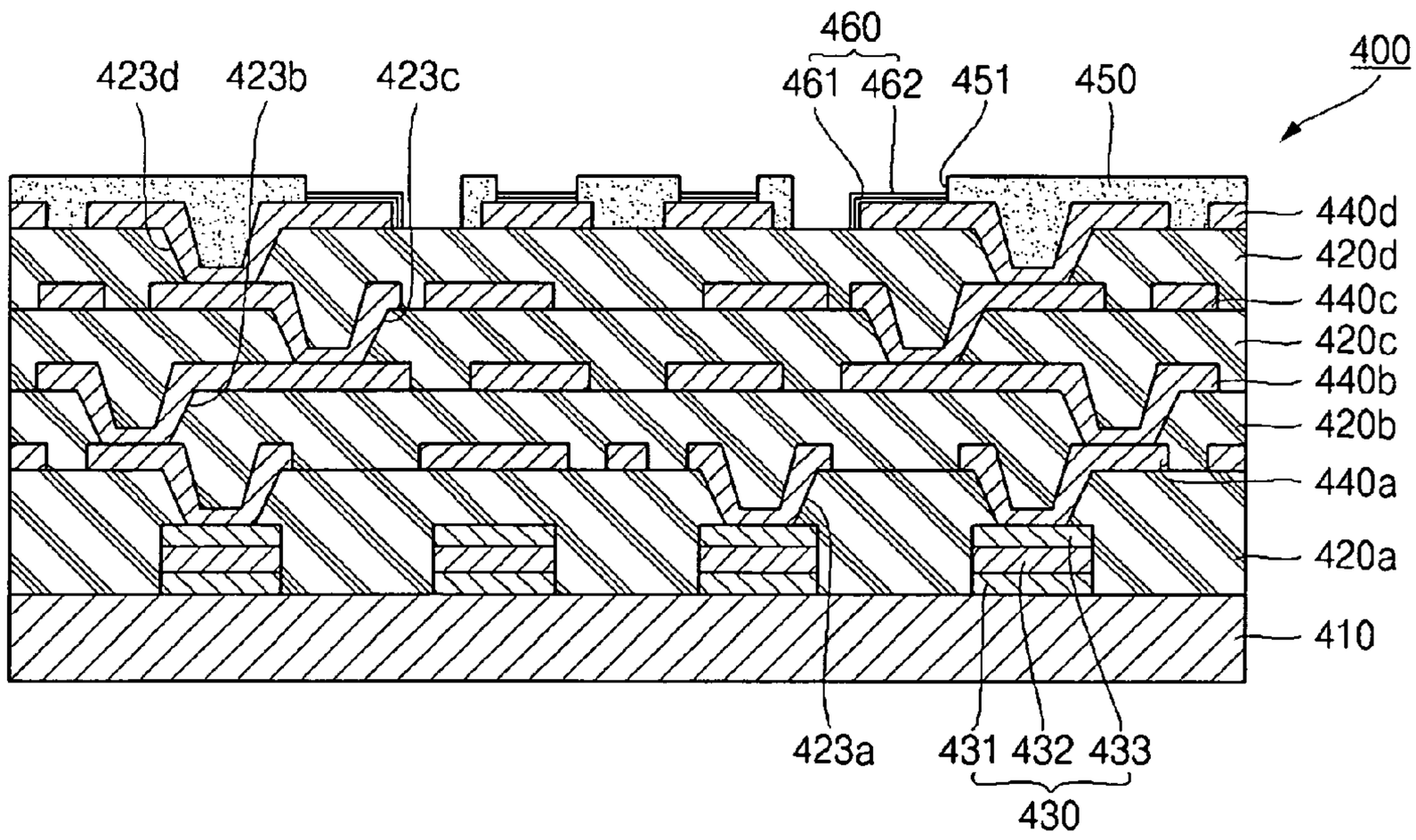
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FIG.4F

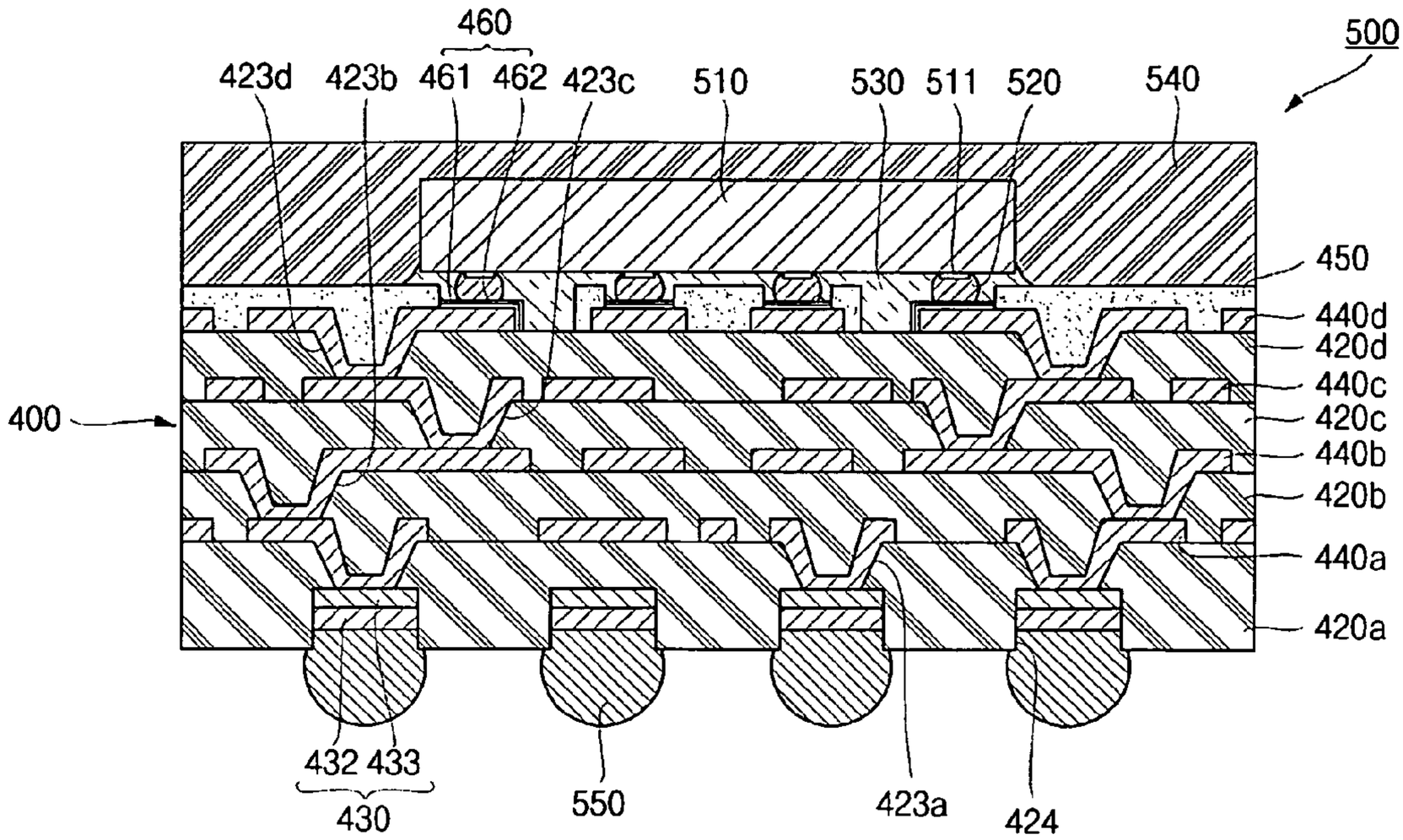
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FIG.5

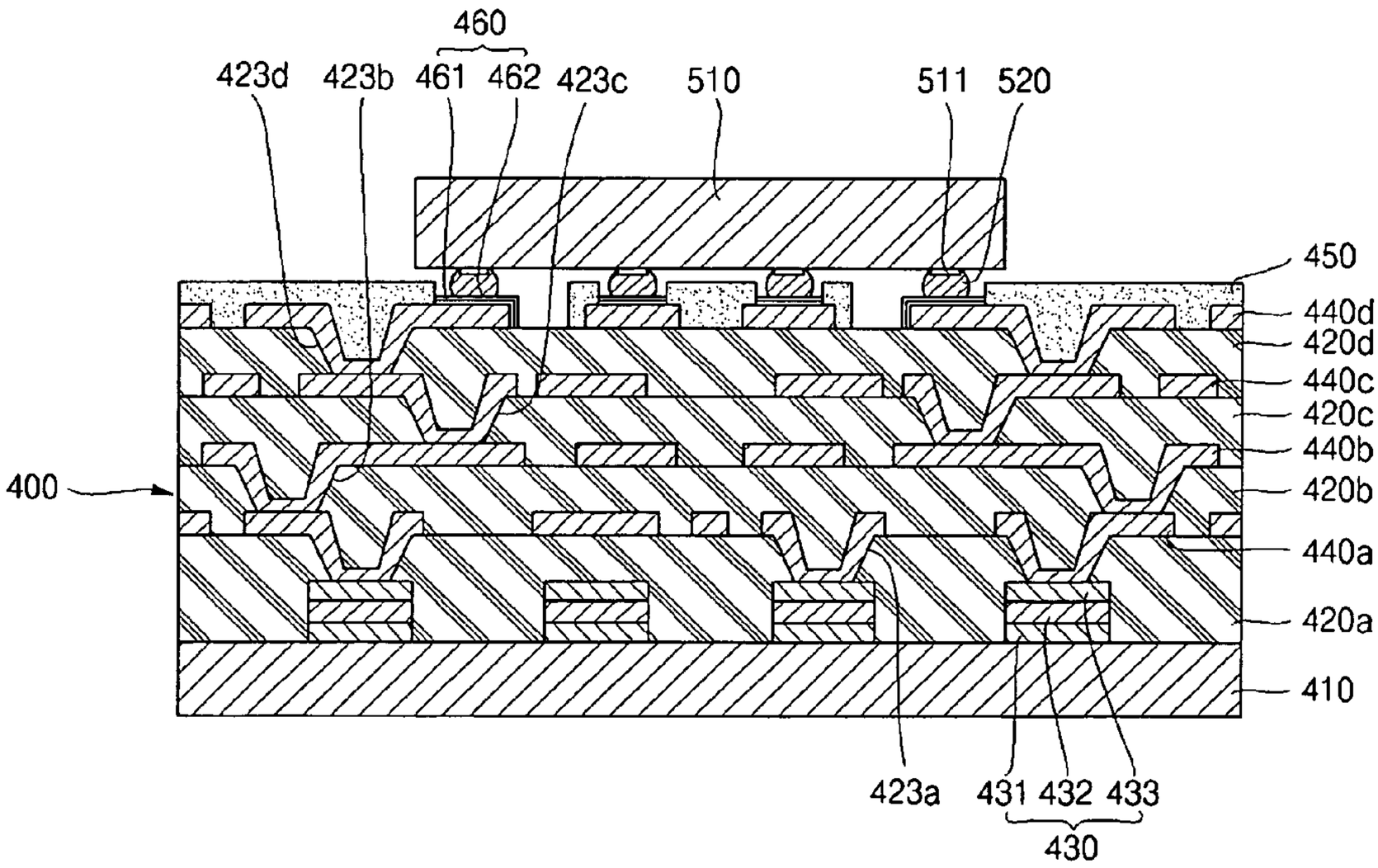
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FIG.5A

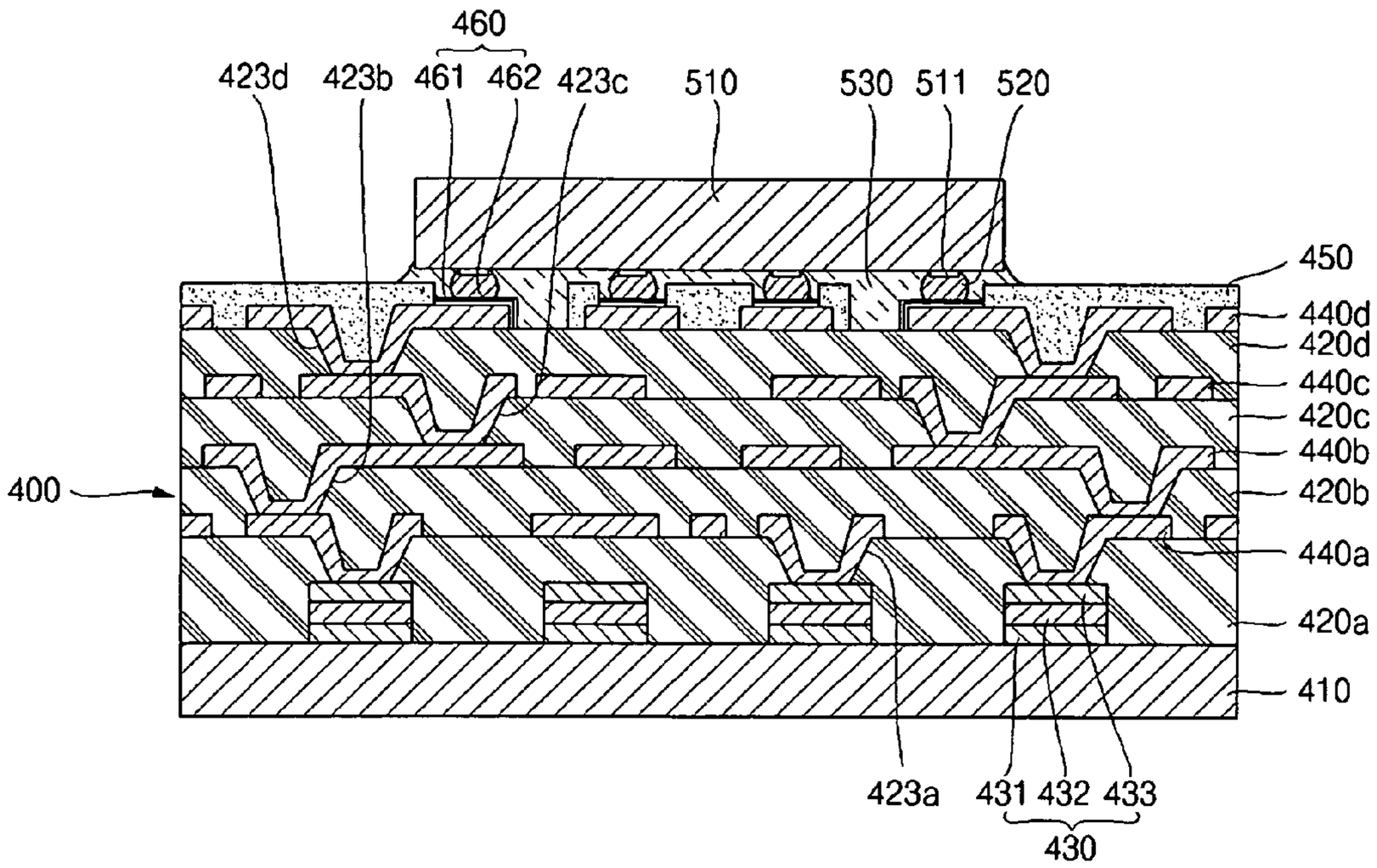
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FIG.5B

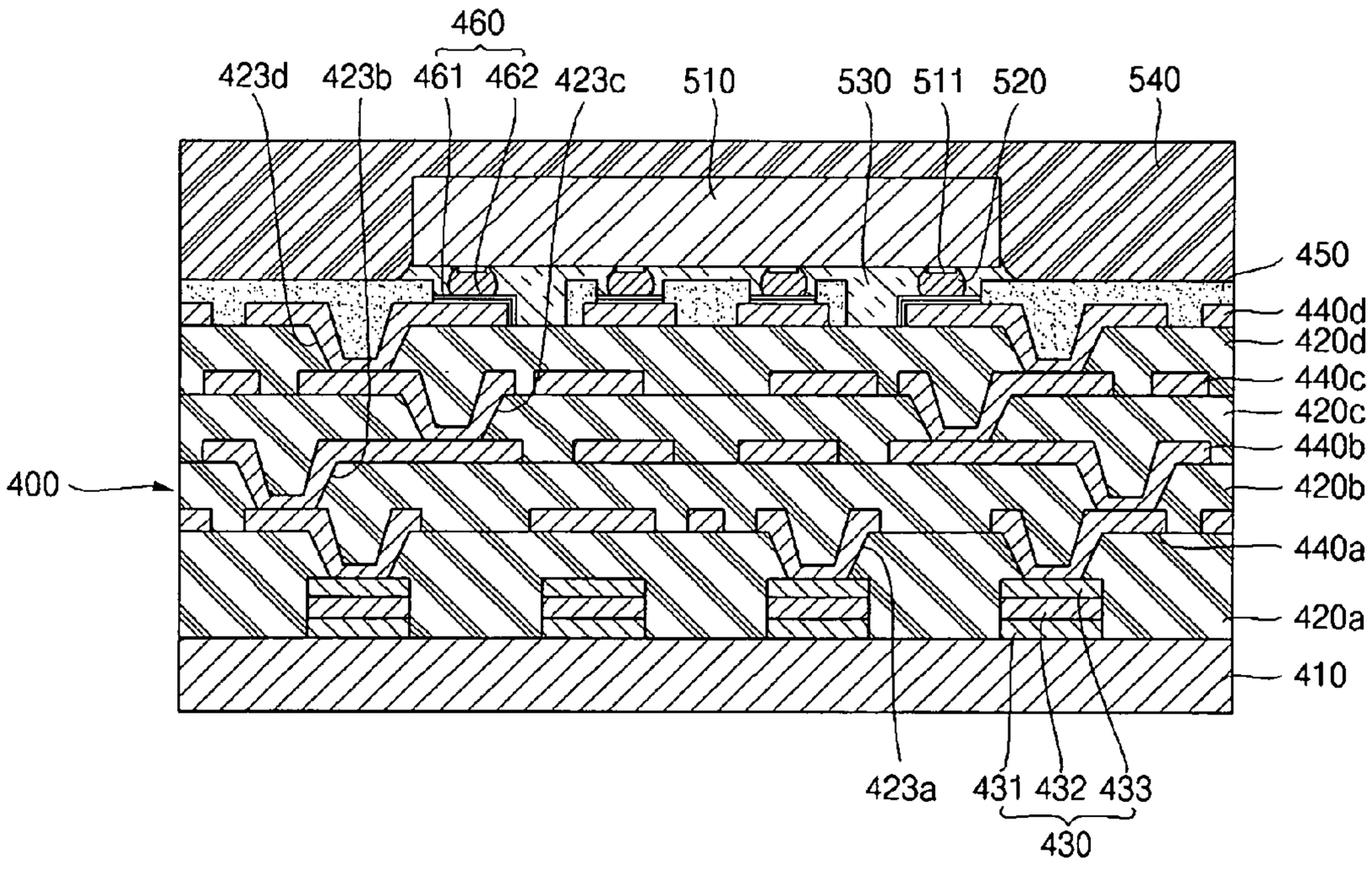
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FIG.5C

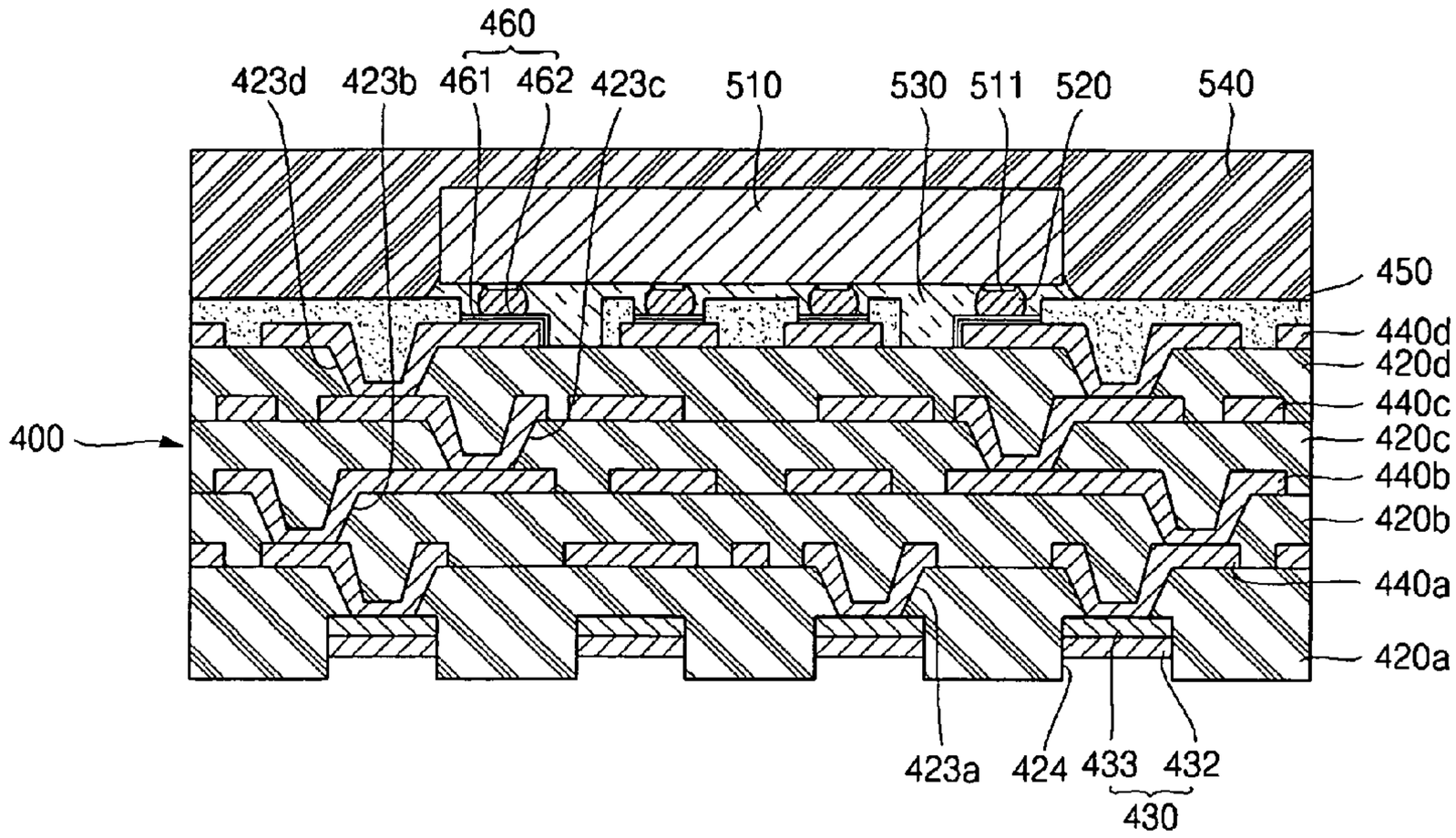
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FIG.5D

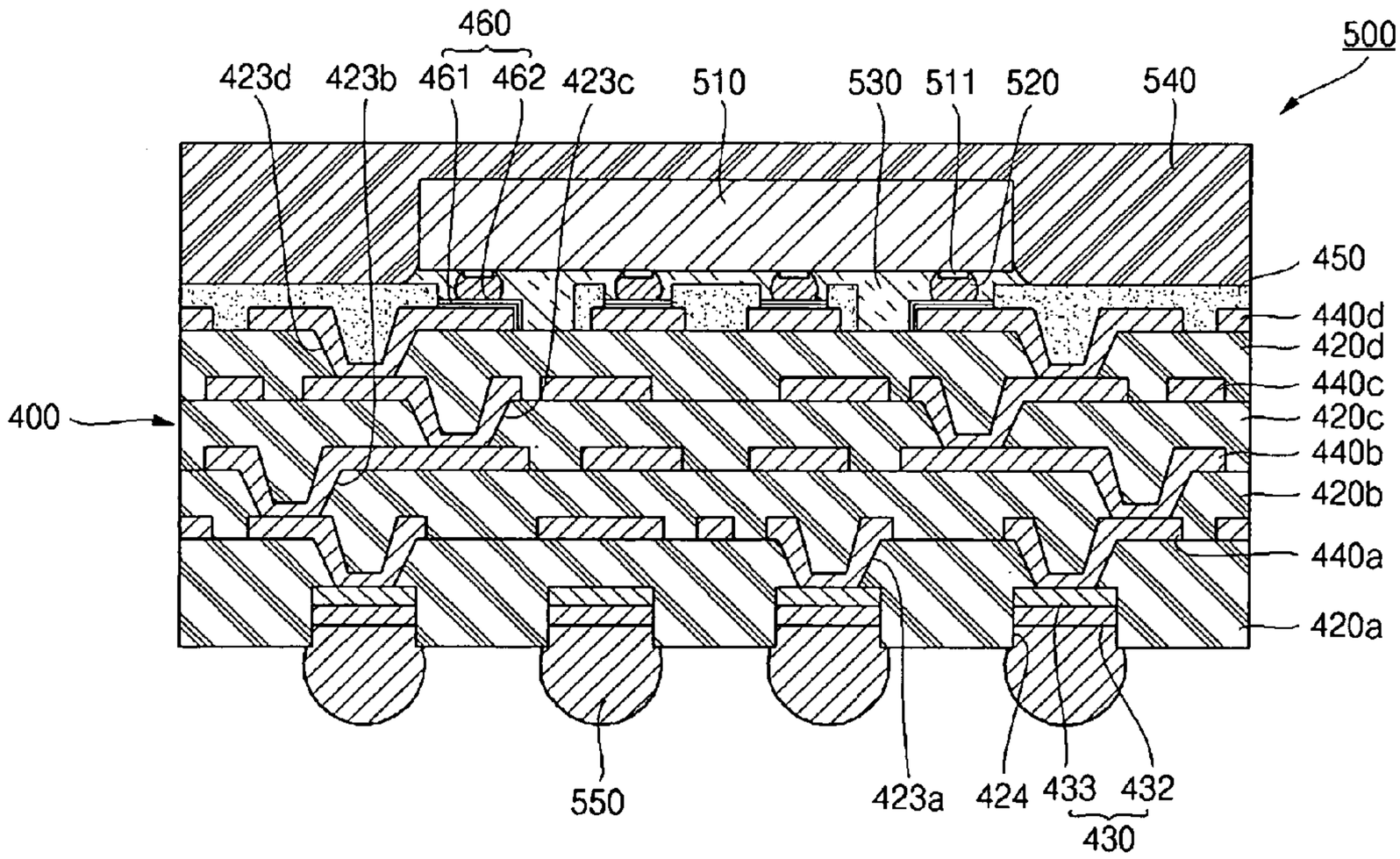
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FIG.5E

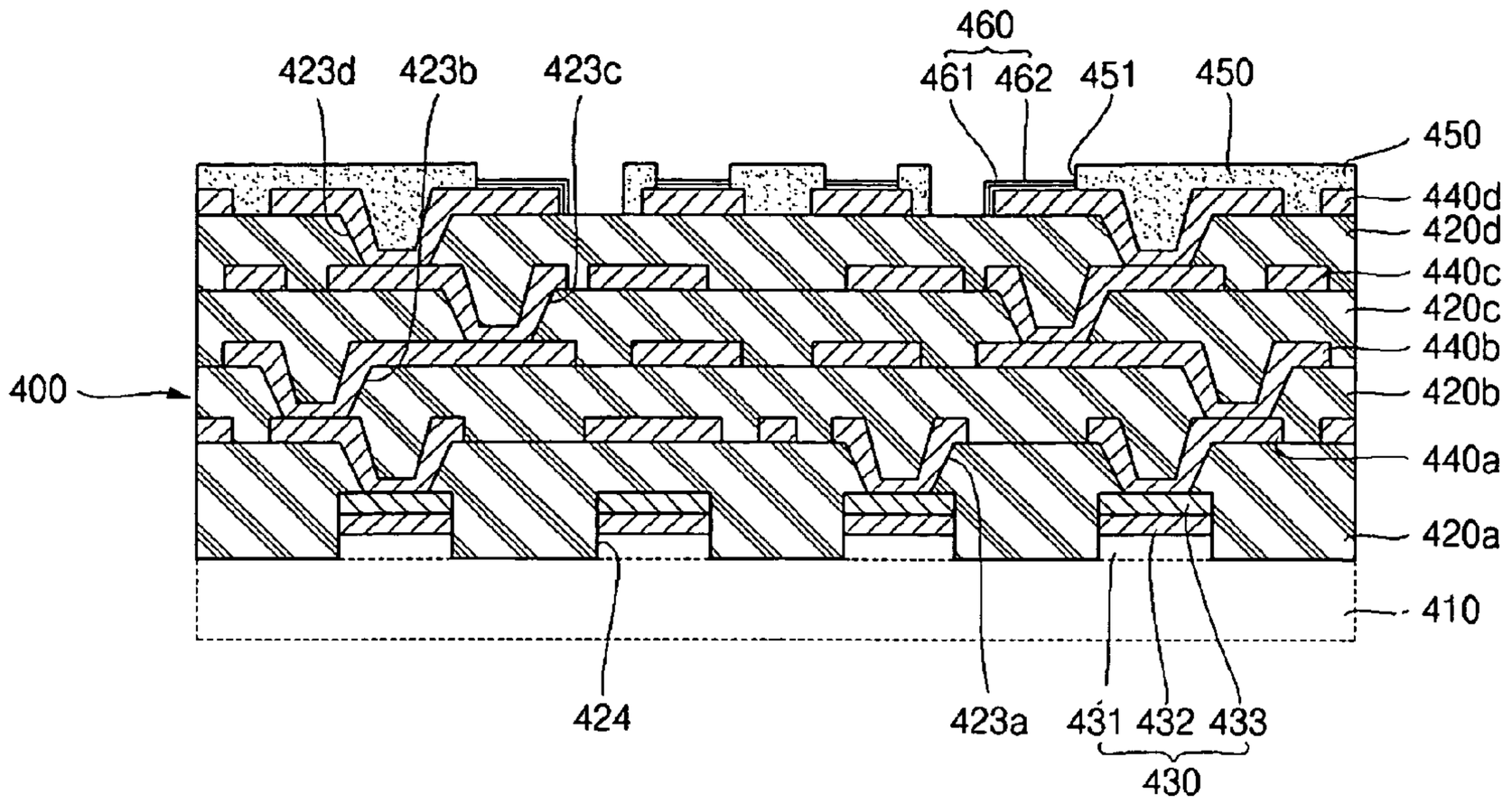
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FIG.6A

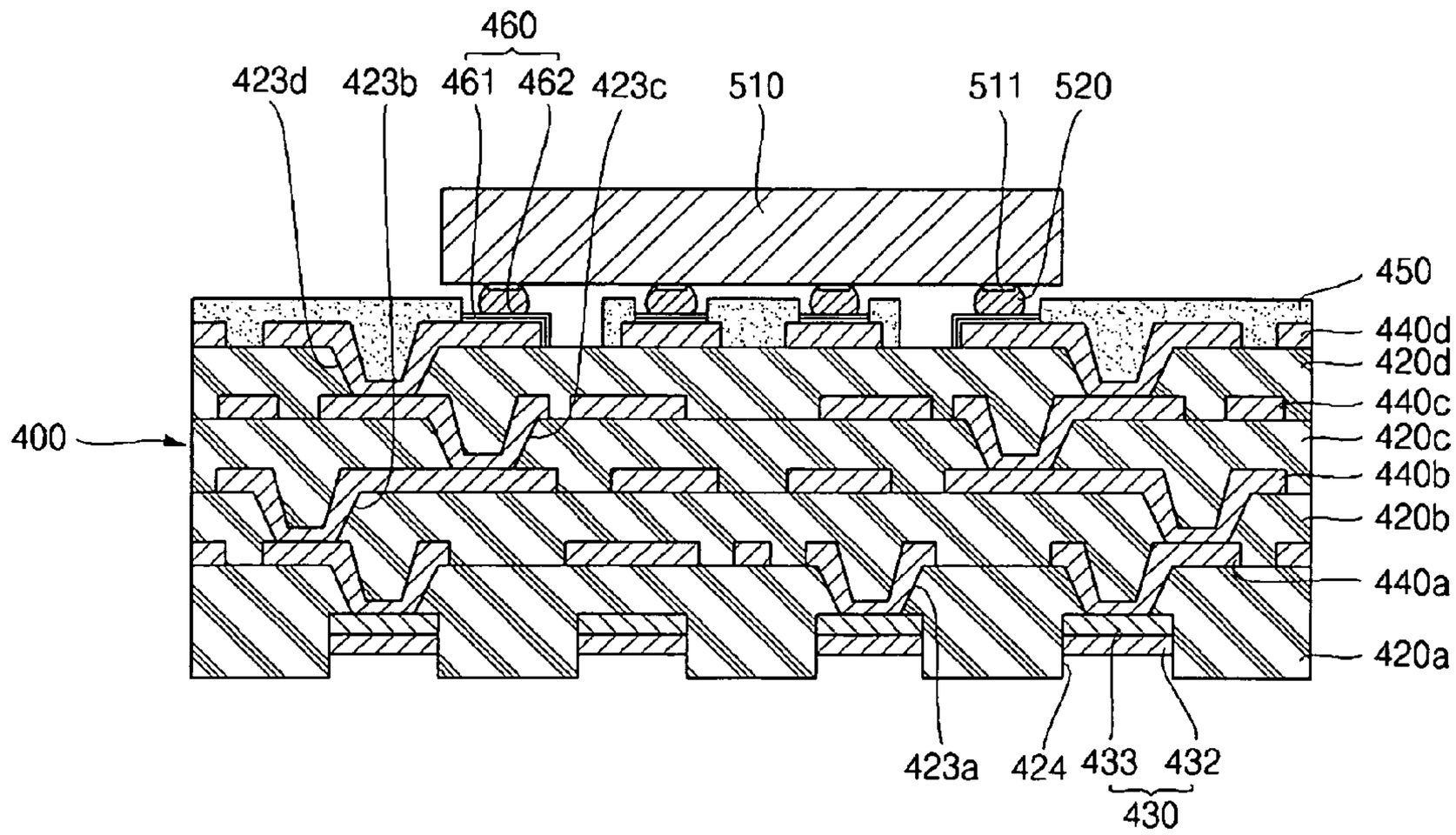
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FIG.6B

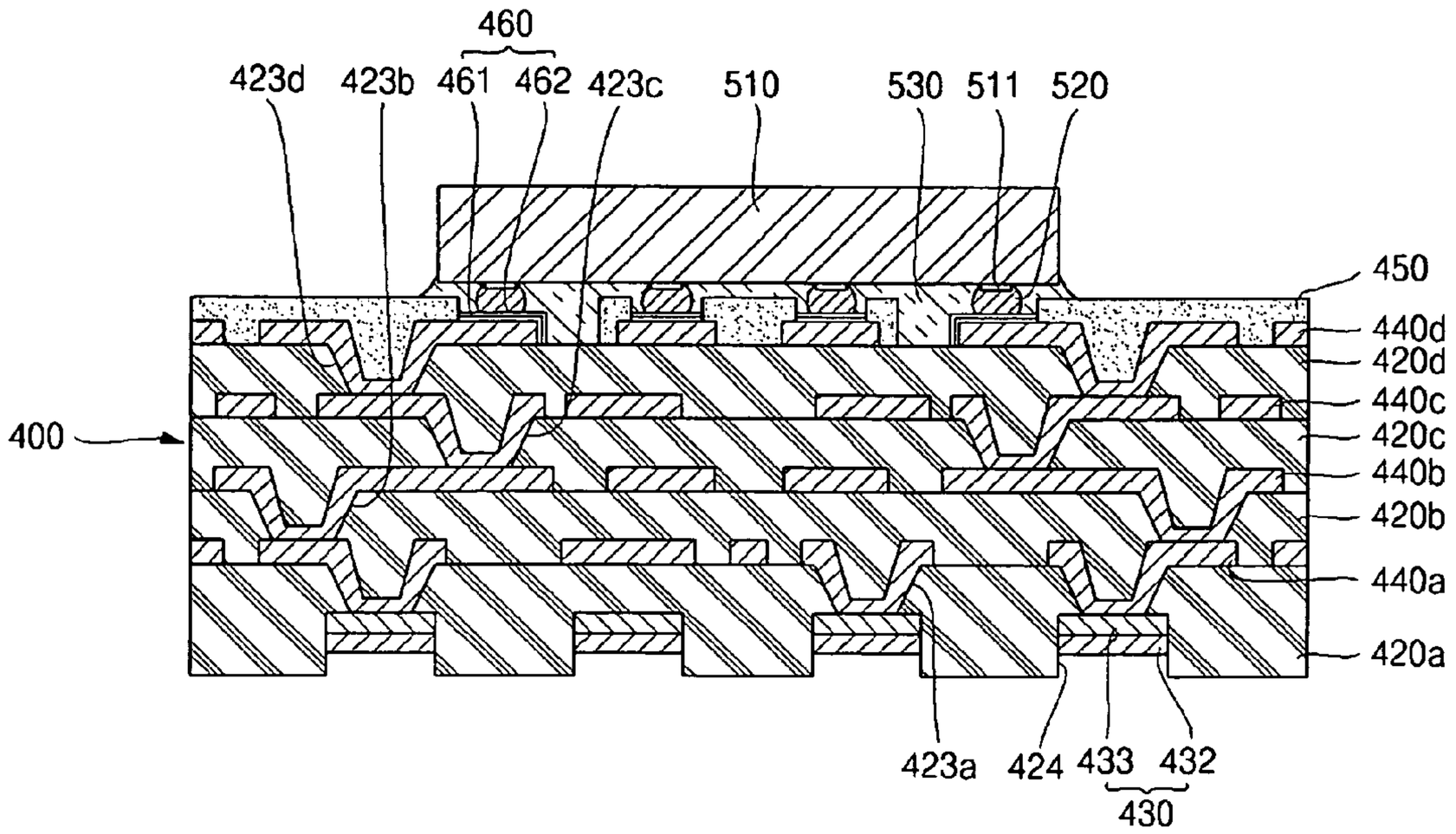
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FIG.6C

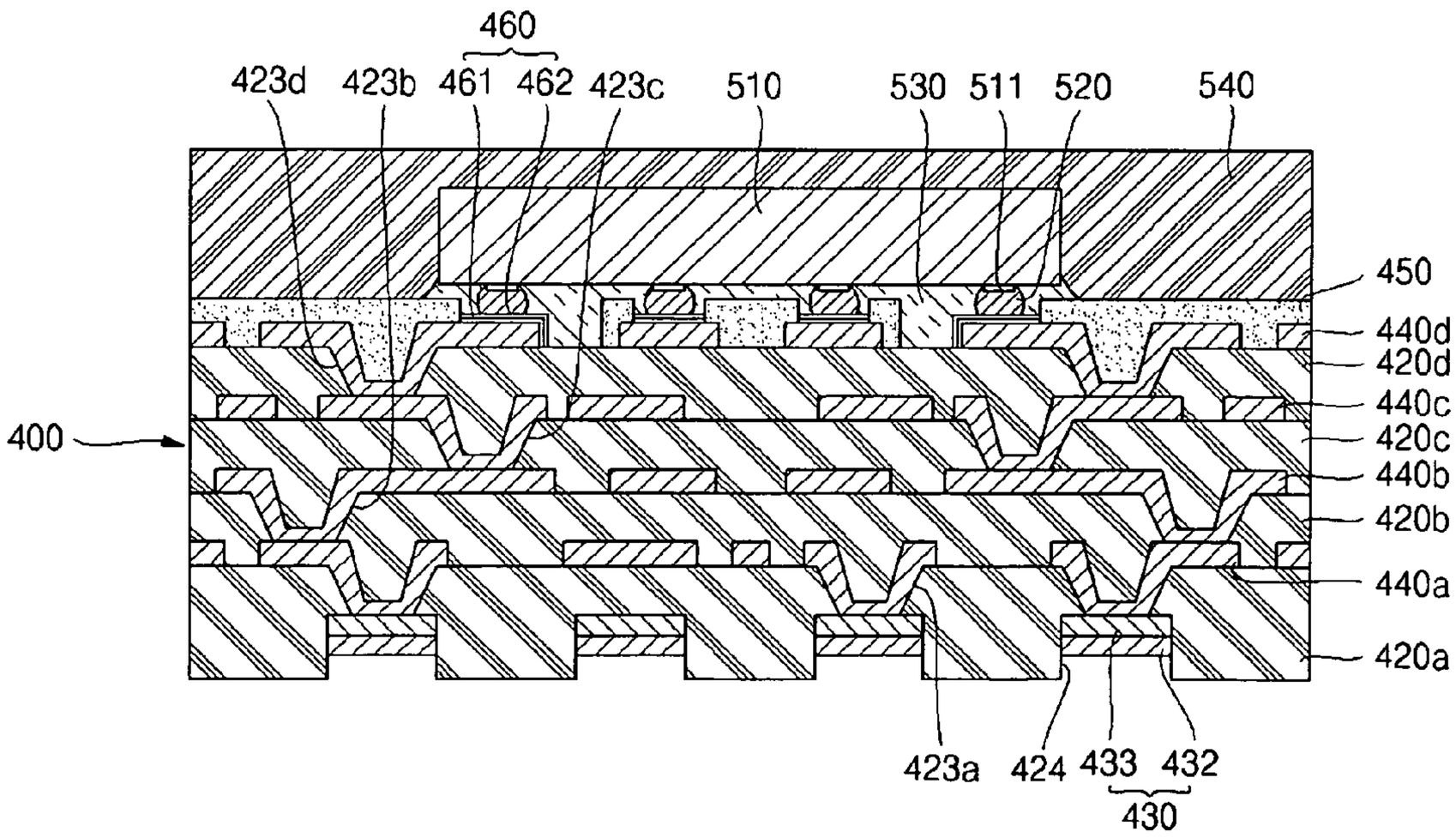
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FIG.6D

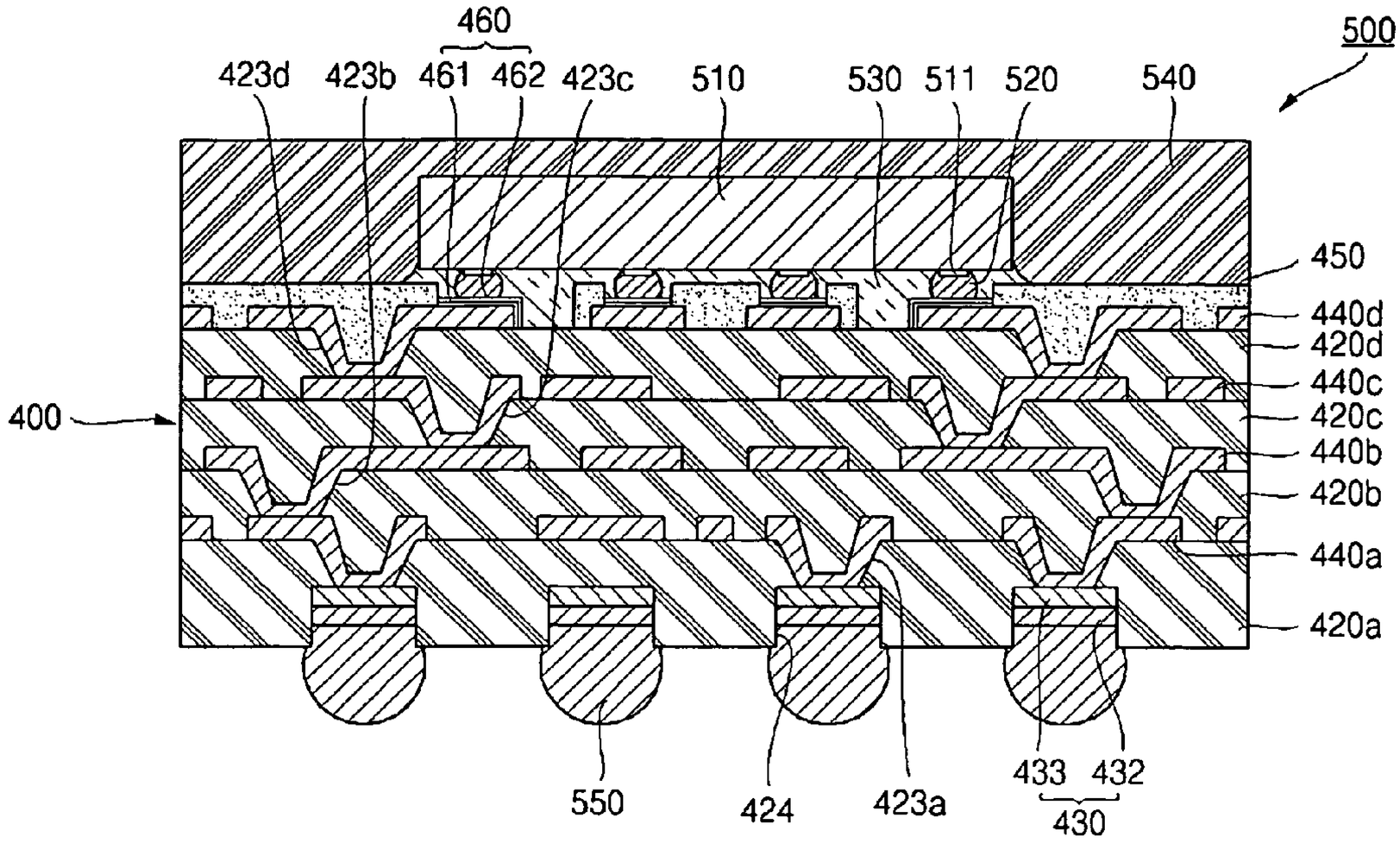
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FIG.6E

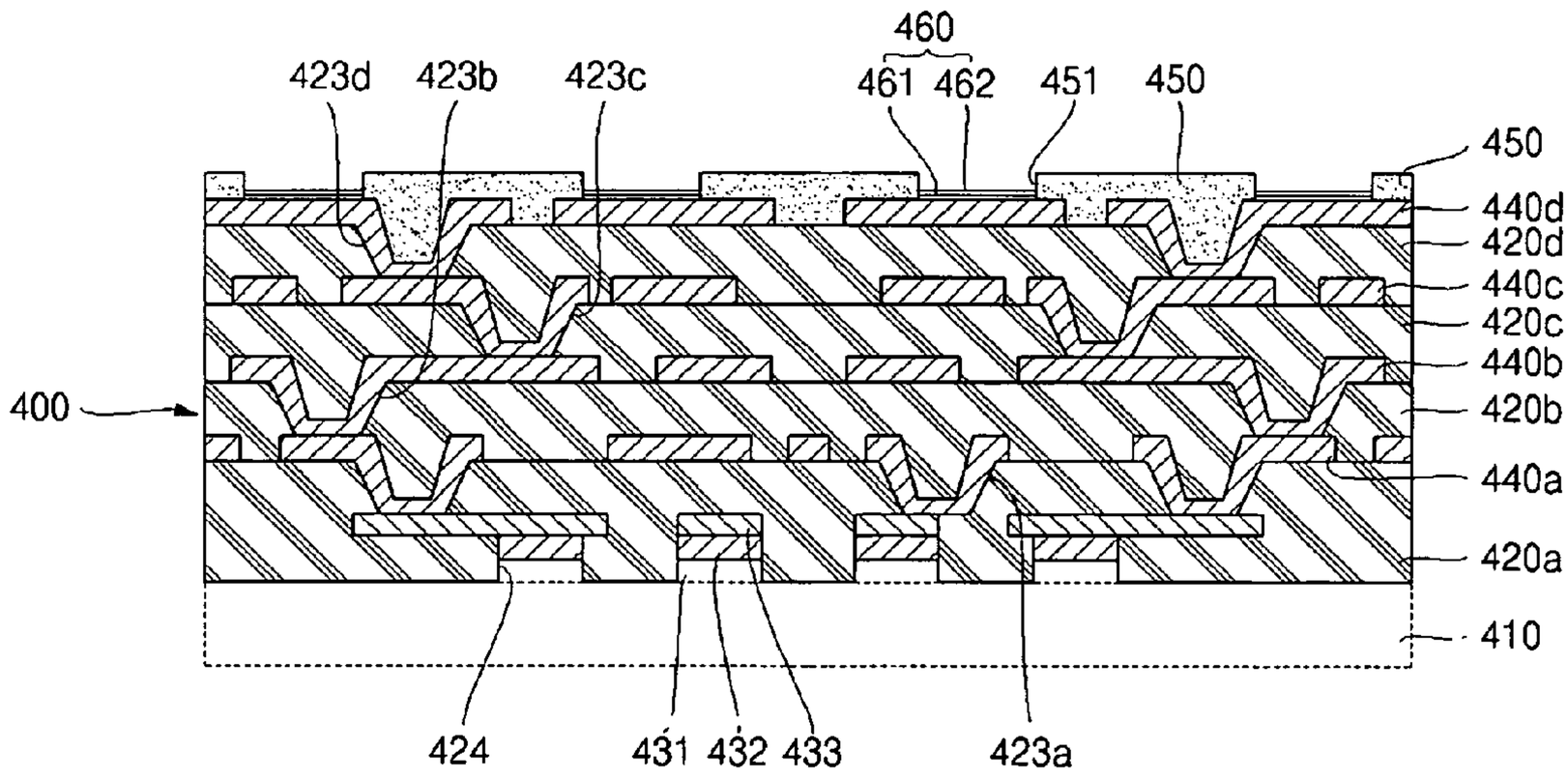
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FIG.7A

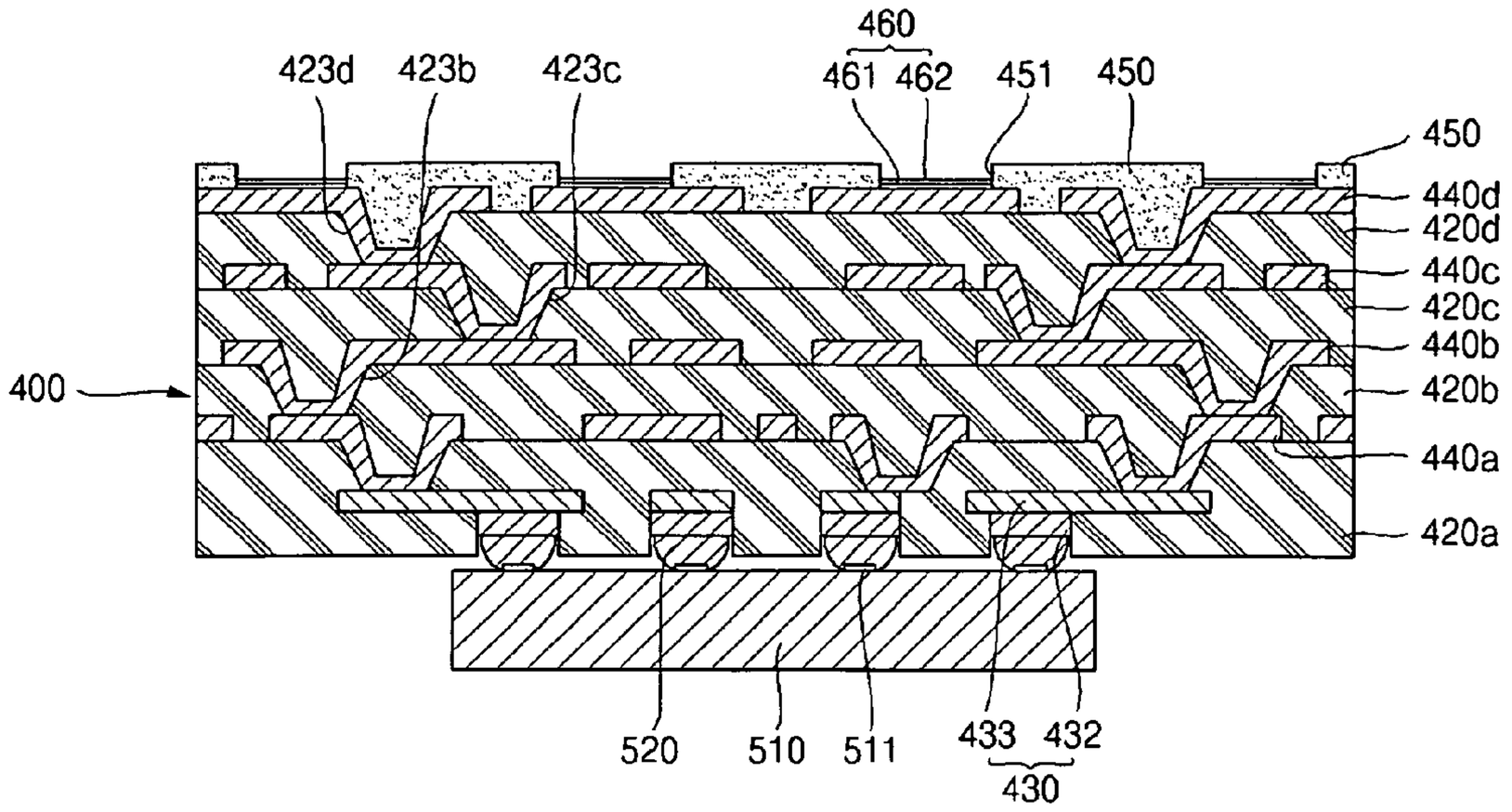
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FIG.7B

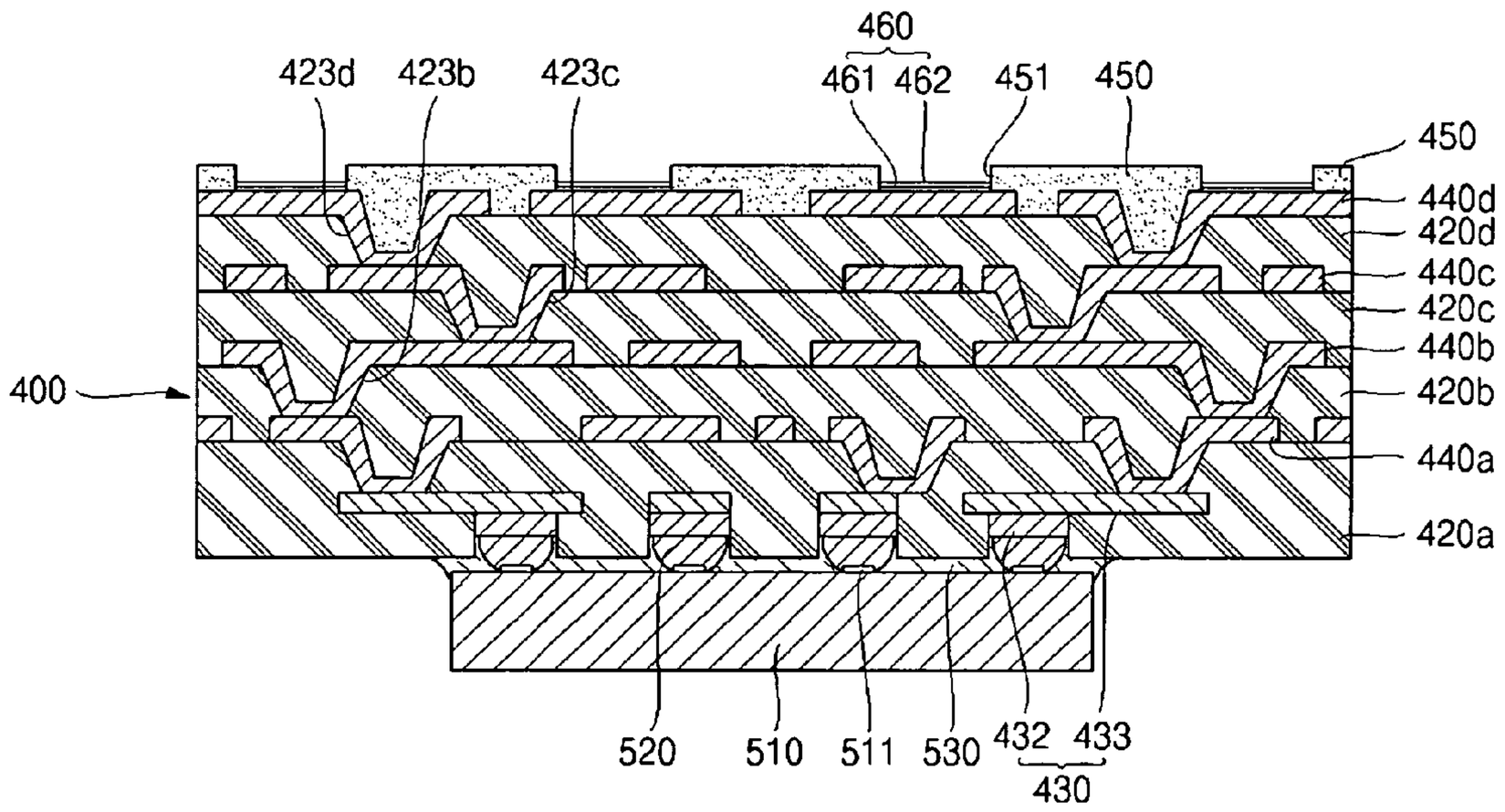
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FIG.7C

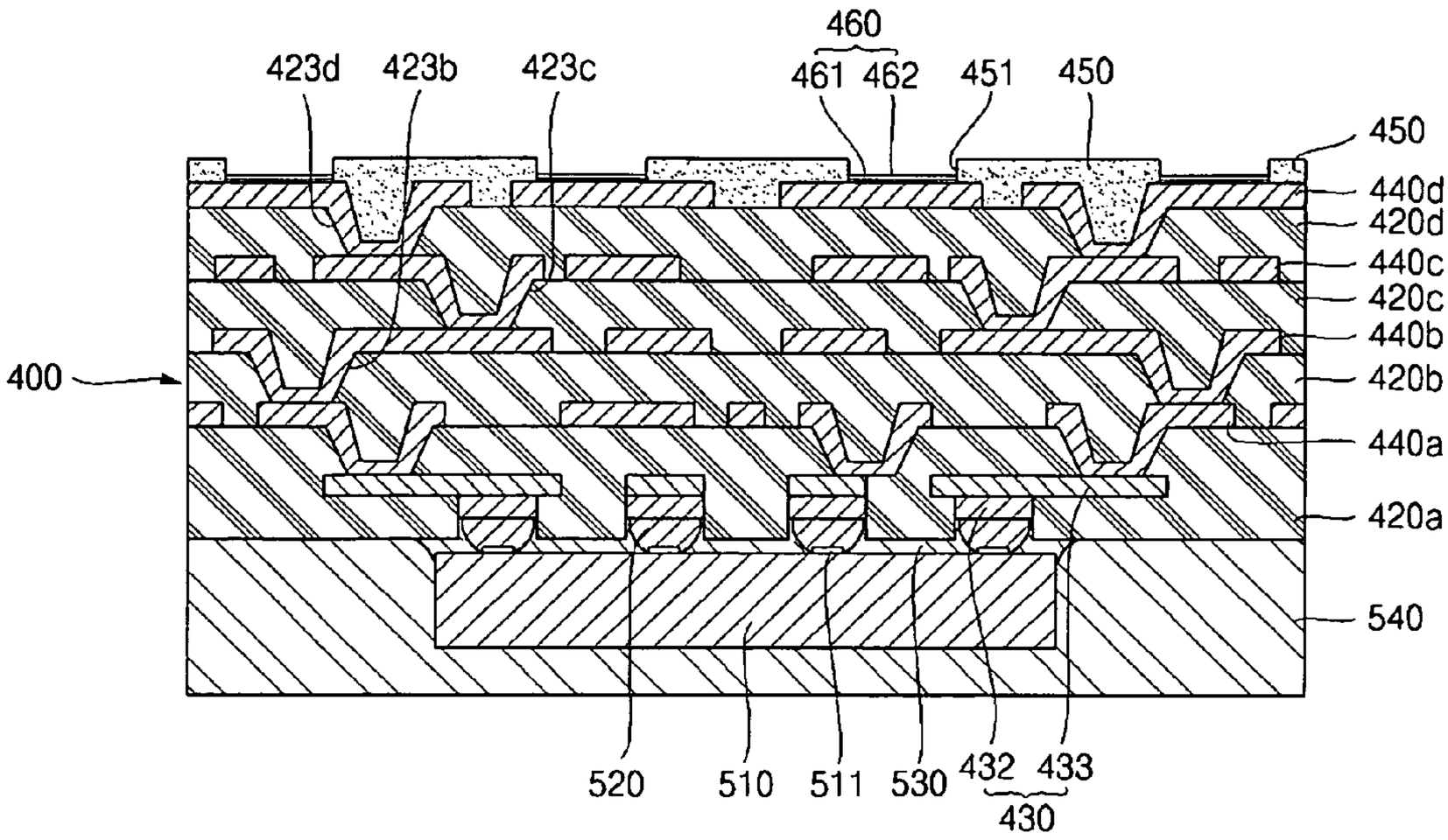
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FIG.7D

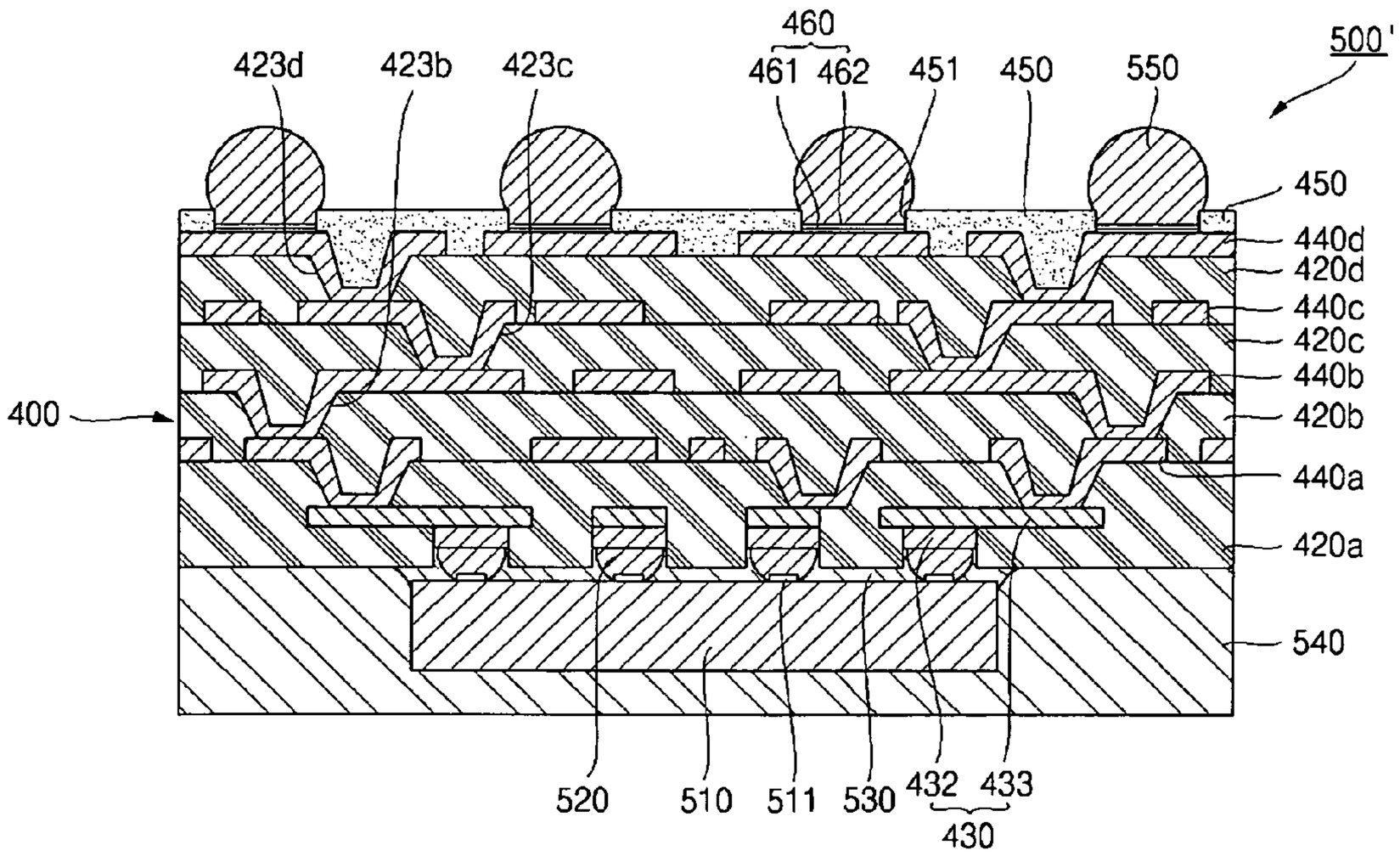
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FIG.7E

# SUBSTRATE FOR SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to substrate for semiconductor device and manufacturing method thereof, and semiconductor device using the same and manufacturing method thereof.

2. Description of the Related Art

Generally, a semiconductor device includes a substrate having a plurality of electrically conductive patterns thereon, a semiconductor die located on the substrate, a plurality of conductive connecting means for electrically connecting the substrate to the semiconductor die, and an encapsulant for encapsulating the semiconductor die and the conductive connecting means. Here, a plurality of solder balls can be further fused to the substrate so as to electrically connect the semiconductor device to an external device.

Meanwhile, a relatively thick core layer is formed at the substrate of the semiconductor device, in order that a warpage is not generated during the manufacturing process of the semiconductor device. That is, the general substrate includes the core layer having a thickness of approximately 800 μm formed at the center thereof and a plurality of relatively thin build-up layers formed at top and bottom surfaces of the core layer. Here, a plurality of electrically conductive patterns is formed at the core layer and the build-up layers. Also, a plurality of via holes passes through the core layer and the build-up layers in order to electrically connect the electrically conductive pattern layers to each other.

However, since such substrate is comparatively thicker, there is a defect in that the thickness of the semiconductor device using the substrate becomes thicker. Also, because each electrically conductive pattern of the substrate is comparatively longer, there is a defect in that the electrical efficiency of the semiconductor device using the electrically conductive patterns is deteriorated. Especially, recent semiconductor devices have been required to have a wide bandwidth, fast data transferring, and higher density structure. However, it is difficult for the general substrate to implement recent trends thereof.

Here, it can solve the problems by eliminating the core layer from the substrate. However, where the core layer is eliminated from the substrate, since the warpage phenomenon is very higher during the manufacturing process of the semiconductor, it is difficult to manufacturer the semiconductor device. Also, it is difficult to manufacture and handle the substrate owing to the low stiffness thereof.

## SUMMARY OF THE INVENTION

A substrate for a semiconductor device and a manufacturing thereof, and a semiconductor device using the same and a manufacturing method thereof are disclosed. For example, in the substrate according to the present invention, a core is eliminated, so that the substrate has a very thin thickness, as well, the length of electrically conductive patterns becomes shorter, whereby the electrical efficiency thereof is improved. Moreover, since a carrier having a stiffness of a predetermined strength is bonded on the substrate, it can prevent a warpage phenomenon during the manufacturing process of the semiconductor device. Furthermore, the carrier is removed from the substrate, whereby a solder ball fusing process or an electrical connecting process of the semiconductor die can be easily performed.



The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanied drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a sectional view of a substrate for a semiconductor device according to one embodiment of the present invention;

FIG. **1**A through FIG. **1**P are sectional views showing a fabrication method of the substrate for a semiconductor device according to one embodiment of the present invention where:

FIG. **1**A illustrates a carrier providing operation;

FIG. **1**B illustrates a first photo sensitive film providing operation;

FIG. **1**C illustrates a first plating operation;

FIG. **1**D illustrates a first photo sensitive film eliminating operation;

FIG. **1**E illustrates a dielectric layer forming operation;

FIG. **1**F illustrates a via hole forming operation;

FIG. **1**G illustrates a second plating operation;

FIG. **1**H illustrates a second photo sensitive film providing operation;

FIG. **1**I illustrates a third plating operation;

FIG. **1**J illustrates a second photo sensitive film eliminating operation;

FIG. **1**K illustrates an etching operation;

FIG. **1**L illustrates a solder mask printing operation;

FIG. **1**M illustrates a solder mask exposing/developing operation;

FIG. **1**N illustrates a third photo sensitive film providing operation;

FIG. **1**O illustrates a fourth plating operation;

FIG. **1**P illustrates a third photo sensitive film eliminating operation;

FIG. **2** is a sectional view of a semiconductor device according to one embodiment of the present invention;

FIG. **2**A through FIG. **2**E are sectional views showing a fabrication method of the semiconductor device according to one embodiment of the present invention where:

FIG. **2**A illustrates a semiconductor die attaching operation;

FIG. **2**B illustrates a wire bonding operation;

FIG. **2**C illustrates an encapsulating operation;

FIG. **2**D illustrates a carrier eliminating operation;

FIG. **2**E illustrates a solder ball fusing operation;

FIG. **3** is a sectional view of a semiconductor device according to another embodiment of the present invention;

FIG. **3**A through FIG. **3**E are sectional views showing a fabrication method of the semiconductor device according to anther embodiment of the present invention where:

FIG. **3**A illustrates a flip chip bonding operation;

FIG. **3**B illustrates an underfilling operation;

FIG. **3**C illustrates an encapsulating operation;

FIG. **3**D illustrates a carrier eliminating operation;

FIG. **3**E illustrates a solder ball fusing operation;

FIG. **4** is a sectional view of a substrate for a semiconductor device according to another embodiment of the present invention;

FIG. **4**A through FIG. **4**F is a flow chart showing a fabrication method of a semiconductor device according to another embodiment of the present invention;

FIG. **4**A illustrates a multi layer forming operation;

FIG. **4**B illustrates a solder mask printing operation;

FIG. **4**C illustrates a solder mask exposing/developing operation;

FIG. **4**D illustrates a photo sensitive film providing operation;

FIG. **4**E illustrates a plating operation;

FIG. **4**F illustrates a photo sensitive film eliminating operation;

FIG. **5** is a sectional view of a semiconductor device according to another embodiment of the present invention;

FIG. **5**A through FIG. **5**E are sectional views showing a fabrication method of a semiconductor device according to another embodiment of the present invention where:

FIG. **5**A illustrates a flip chip bonding operation;

FIG. **5**B illustrates an underfilling operation;

FIG. **5**C illustrates an encapsulating operation;

FIG. **5**D illustrates a carrier eliminating operation;

FIG. **5**E illustrates a solder ball fusing operation;

FIG. **6**A through FIG. **6**E are sectional views showing a fabrication method of a semiconductor device according to another embodiment of the present invention where:

FIG. **6**A illustrates a carrier eliminating operation;

FIG. **6**B illustrates a flip chip bonding operation;

FIG. **6**C illustrates an underfilling operation;

FIG. **6**D illustrates an encapsulating operation;

FIG. **6**E illustrates a solder ball fusing operation;

FIG. **7**A through FIG. **7**E are sectional views showing a fabrication method of a semiconductor device according to another embodiment of the present invention where:

FIG. **7**A illustrates a carrier eliminating operation;

FIG. **7**B illustrates a flip chip bonding operation;

FIG. **7**C illustrates an underfilling operation;

FIG. **7**D illustrates an encapsulating operation; and

FIG. **7**E illustrates a solder ball fusing operation.

Common reference numerals are used throughout the drawings as well, detailed descriptions are used to indicate like elements.

## DETAILED DESCRIPTION

Referring to FIG. **1**, a sectional view of a substrate **100** for a semiconductor device according to one embodiment of the present invention is illustrated.

As shown in FIG. **1**, the substrate **100** for a semiconductor device includes a carrier **110** having a predetermined stiffness, a dielectric layer **120** formed on the carrier **110**, a plurality of conductive lands **130** electrically connected to the carrier **110** at the inside of the dielectric layer **120**, a plurality of electrically conductive patterns **140** electrically connected to the conductive lands **130** at the surface of the dielectric layer **120**, and a solder mask **150** for covering the dielectric layer **120** and the electrically conductive patterns **140**, a predetermined area of each conductive pattern **140** being exposed to outside.

The carrier **110** is in the form of an approximately planar plate. The material of the carrier **110** may be a metal, a film or its equivalent, in order that a warpage is not generated during the manufacturing process of the semiconductor device. However, the present invention is not limited to any material of the carrier **110**. Moreover, in case of the metal as the material of the carrier **110**, the material of the carrier **110** may be a copper, an aluminum, a nickel or its equivalent. However, the present invention is not limited to any metal material of the carrier **110**.

The dielectric layer **120** of a predetermined thickness is formed on the surface of one side of the carrier **110**. The dielectric layer **120** includes a first surface **121** of an approximate planar surface bonded on the carrier **110** and a second surface **122** of an approximate planar surface opposed to the first surface **121**. Also, a plurality of via holes **123** of a predetermined depth is further formed at the second surface **122** of the dielectric layer **120**, in order to electrically connect the electrically conductive patterns **140** to the conductive lands **130**. The material of the dielectric layer **120** may be a prepreg and an ABF (Ajinomoto Buildup Film) of a low dielectric constant or its equivalent, in order to decrease the capacitance of the electrically conductive patterns **140** and so on. However, the present invention is not limited to any material of the dielectric layer **120**. Moreover, the thickness of the dielectric layer **120** is approximately 10~150 μm, so that it has a very thin thickness in comparison with the conventional substrate having a core layer.

Each of conductive lands **130** formed at the inside of the dielectric layer **120** have a bottom surface flush (substantially coplanar) with the first surface **121** of the dielectric layer **120**. That is, the conductive lands **130** are electrically connected to the carrier **110**. Also, the conductive land **130**, that is, a copper layer **131**, a gold layer **132**, another copper layer **133** may be plated on the carrier **110** in order. However, the present invention is not limited to any material of the conductive land **130**.

The plurality of electrically conductive patterns **140** are formed at the second surface **122** of the dielectric layer **120**. Here, the plurality of electrically conductive patterns **140** is electrically connected to the conductive lands **130** through the via holes **123** formed at the dielectric layer **120**. The material of electrically conductive patterns **140** may be a copper or its equivalent. However, the present invention is not limited to any material of the electrically conductive patterns **140**.

The solder mask **150** is coated on the second surface **122** of the dielectric layer **120** in order to cover the electrically conductive patterns **140**. Here, a plurality of openings **151** are formed at the solder mask **150**, so that a predetermined area of each electrically conductive pattern **140** is exposed to outside. Also, a plurality of bonding pads **160** are formed at the electrically conductive patterns **140** exposed to outside through the openings **151**. A semiconductor die will be electrically connected to the bonding pad **160** in future. Also, the bonding pad **160**, that is, a nickel layer **161** and a gold layer **162** may be plated on the electrically conductive pattern **140** in order. However, the present invention is not limited to any material of the bonding pad **160**.

Referring to FIG. **1**A through FIG. **1**P, sectional views showing a fabrication method of the substrate **100** for a semiconductor device according to one embodiment of the present invention is illustrated.

As shown in the drawings, the fabrication method of the substrate **100** for a semiconductor device according to the present invention includes a carrier providing operation, a first photo sensitive film providing operation, a first plating operation, a first photo sensitive film eliminating operation, a dielectric layer forming operation, a via hole forming operation, a second plating operation, a second photo sensitive film providing operation, a third plating operation, a second photo sensitive film eliminating operation, an etching operation, a solder mask printing operation, a solder mask exposing/developing operation, a third photo sensitive film providing operation, a fourth plating operation, and a third photo sensitive film eliminating operation.

As shown in FIG. **1**A, in the carrier providing operation, the carrier **110** of an approximately planar plate is provided. The material of the carrier **110** may be a metal, a film or its equivalent, in order that a warpage is not generated during the manufacturing process of the semiconductor device, as described above. However, the present invention is not limited to any material of the carrier **110**. Moreover, in case of the

metal as the material of the carrier **110**, the material of the carrier **110** may be a copper, an aluminum, a nickel or its equivalent. However, the present invention is not limited to any metal material of the carrier **110**.

As shown in FIG. **1**B, in the first photo sensitive film providing operation, the photo sensitive film **171** of a predetermined pattern is formed at the top surface and the bottom surface of the carrier **110**. That is, the photo sensitive film **171**, on which any pattern is not formed, is bonded or coated on the top surface and the bottom surface of the carrier **110** and then, only the photo sensitive film **171** having a predetermined pattern is left over the top surface of the carrier **110** through the exposing/developing process. Here, the predetermined region of the carrier **110** is exposed to outside through the photo sensitive film **171**.

As shown in FIG. **1**C, in the first plating operation, the plurality of conductive lands **130** are formed. That is, the copper layer **131**, the gold layer **132** and another copper layer **133** are plated on the top surface of the carrier **110** exposed to outside through the photo sensitive film **171** in order, thereby forming the conductive lands **130** of a predetermined thickness.

As shown in FIG. **1**D, in the first photo sensitive film eliminating operation, the photo sensitive film **171** left over the carrier **110** is eliminated by a chemical etching and the like. Here, like this, only the plurality of conductive lands **130** is left over the carrier **110**. Also, the carrier **110** except for the conductive lands **130** is exposed to outside.

As shown in FIG. **1**E, in the dielectric layer forming operation, the dielectric layer **120** of a predetermined thickness is coated and hardened so as to cover the conductive lands **130** formed at the carrier **110** all together. Here, the material of the dielectric layer **120** may be a prepreg and an ABF (Ajinomoto Buildup Film) of a low dielectric constant or its equivalent, in order to decrease the capacitance of the electrically conductive patterns **140** and so on. However, the present invention is not limited to any material of the dielectric layer **120**. Moreover, the carrier **110** has an adequate stiffness, so that the warpage is not generated during the manufacturing process of the semiconductor device, thereby the dielectric layer **120** has very thin thickness of 10~150 μm.

As shown in FIG. **1**F, in the via hole forming operation, the via holes **123** of a predetermined depth are formed in such a manner that the conductive lands **130** formed at both the surface of the carrier **110** and the inside of the dielectric layer **120** are exposed to outside. That is, the dielectric layer **120** corresponding to the conductive lands **130** is eliminated by a laser drilling, a mechanical drilling or an etching and so on, so that the via holes **123** of a predetermined depth are formed. Here, the predetermined region of each conductive lands **130** is exposed to outside through the via holes **123**.

As shown in FIG. **1**G, in the second plating operation, an electroless plating layer **172**, sometimes called a seed layer, of a thin thickness is formed at the surface of the dielectric layer **120** and the surface of the conducive lands **130** exposed to outside through the via holes **123**. The electroless plating layer **172** can be formed by means of a conventional electroless plating process. Also, the thickness of the electroless plating layer **172** is in the range of several μm.

As shown in FIG. **1**H, in the second photo sensitive film providing operation, the photo sensitive film **173** of a predetermined pattern is formed at the surface of the electroless plating layer **172** again. Here, it is suited that the photo sensitive film **173** is not formed at the regions corresponding to the via holes **123**, so as to electrically connect the electrically conductive patterns **140** and the conductive lands **130** each other. Also, the photo sensitive film **173**, on which any pattern is not formed, is bonded or coated on the surface of the electroless plating layer **172** and then, only the photo sensitive film **173** having a predetermined pattern is left over the surface of the electroless plating layer **172** through the exposing/developing process. Here, the predetermined region of the electroless plating layer **172** is exposed to outside through the photo sensitive film **173**.

As shown in FIG. **1**I, in the third plating operation, an electrolytic plating layer of a predetermined thickness is formed at the electroless plating layer exposed to outside through the photo sensitive film **173**. The electrolytic plating layer is the electrically conductive pattern **140** in fact. The electrolytic plating layer can be formed by means of a conventional electrolytic plating process, thereby obtaining the electrically conductive pattern **140** of desiring thickness.

As shown in FIG. **1**J, in the second photo sensitive film eliminating operation, the photo sensitive film **173** formed on the electroless plating layer **172** is eliminated by a chemical etching and the like. Here, like this, the electroless plating layer **172** located at the lower portion of the photo sensitive film **173** is exposed to outside. Also, all of the electrically conductive patterns **140** continuously maintain a short status on account of the electroless plating layer **172**.

As shown in FIG. **1**K, in the etching operation, all electroless plating layers **172** left between the electrically conductive patterns **140** are eliminated by the chemical etching process. Here, since the electroless plating layer **172** has very thin thickness of several μm, it can be easily eliminated through a weak acid.

As shown in FIG. **1**L, in the solder mask printing operation, the solder mask **150** of a predetermined thickness is printed on the dielectric layer **120** in order to cover the electrically conductive patterns **140**. The material of the solder mask **150** may be photosensitivity or insensitivity. The solder mask **150** serves to prevent the oxidation of the electrically conductive patterns **140** and its damage from the external impact during the manufacturing process of the semiconductor device.

As shown in FIG. **1**M, in the solder mask exposing/developing operation, a predetermined region of the solder mask **150** is eliminated by the exposing/developing process. That is, the plurality of openings **151** are formed at the solder mask **150**, so that a predetermined area of each electrically conductive pattern **140** is exposed to outside.

As shown in FIG. **1**N, in the third photo sensitive film providing operation, the photo sensitive film **174** of a predetermined pattern is formed at the bottom surface of the carrier **110**. Here, since the photo sensitive film **174** serves to prevent the plating layer from formed at the bottom surface of the carrier **110** during the plating process, the material of the photo sensitive film **174** may not be photosensitivity.

As shown in FIG. **1**O, in the fourth plating operation, the plurality of bonding pads **160** is formed at predetermined regions of the electrically conductive patterns **140** exposed to outside through the solder mask **150**. The plurality of bonding pads **160** can be formed by means of the electrolytic plating process. That is, the nickel layer **161** and the gold layer **162** may be plated on the electrically conductive pattern **140** of a predetermined region exposed to outside through the solder mask **150**, thereby forming the bonding pad **160** of a predetermined thickness. The bonding pad **160** serves to electrically connect with the semiconductor die during manufacturing process of the semiconductor device.

As shown in FIG. **1**P, in the third photo sensitive film eliminating operation, the photo sensitive film **174** formed on the bottom surface of the carrier **110** is eliminated by a chemical etching and the like, thereby completing the substrate **100** according to the present invention. Here, the bottom surface

of the carrier **110** is exposed to outside through the photo sensitive film elimination process.

Referring to FIG. **2**, a sectional view of a semiconductor device **200** according to one embodiment of the present invention is illustrated.

As shown in FIG. **2**, the semiconductor device **200** includes the above substrate **100**, a semiconductor die **210** bonded to the substrate **100**, a plurality of conductive connecting means **220** for electrically connecting the substrate **100** to the semiconductor die **200**, an encapsulant **230** for encapsulating the semiconductor die **200** and the conductive connecting means **220**, and a plurality of solder balls **240** fused to the substrate **100**.

Firstly, the substrate **100** is actually similar to that of FIG. **1**. However, the carrier **110** is removed from the substrate **100** and a predetermined region (the copper layer **131**) is etched and eliminated. Accordingly, each conductive land **130** includes only the gold layer **132** and the copper layer **133**. As described above, the substrate includes the dielectric layer **120**, the plurality of conductive lands **130**, the plurality of electrically conductive patterns **140**, the bonding pads **160**, and the solder mask **150**. Since the structure and method of the substrate **100** is explained in full as described above, further description is omitted here.

The semiconductor die **210** is bonded to the surface of the solder mask **150** of the substrate **100** by means of an adhesive **201**. Here, a plurality of I/O pads **211** is formed at the top surface of the semiconductor die **210**.

The plurality of conductive connecting means **220** may be a conventional conductive wire. More concretely, it may be a gold wire, an aluminum wire or its equivalent. The connecting means **220** serves to electrically connect the bonding pads **160** of the substrate **100** to the I/O pads of the semiconductor die **210** each other.

The encapsulant **230** covers the semiconductor die **210** and the conductive connecting means **220**, so that it serves to protect them from an external impact. Here, the encapsulant **230** covers the whole top surface of the substrate **100**. Also, the material of the encapsulant **230** may be a plastic resin, a thermosetting resin, a ceramic, an epoxy molding compound or its equivalent. However, the present invention is not limited to any material of the encapsulant **230**.

The plurality of solder balls **240** is fused to the conductive lands **130**, that is, the gold layer **132** formed at the substrate **100**. The solder ball **240** serves to mechanically and electrically connect the semiconductor device **200** to an external device, as well known. The bottom surface of the conductive land **130** is not flush with the substrate **100**, that is, the bottom surface of the dielectric layer **120**. That is, the bottom surface of the conductive land **130** is located at the inside of the dielectric layer **120**. In other words, a recess **124** of a predetermined depth is formed at the inside of the dielectric layer **120** and the conductive land **130** is formed at the inside of the recess **124**. Accordingly, the solder ball **240** is combined with the recess **124** and fused to the conductive land **130**, the fusing status of the solder balls **240** is more strongly.

Referring to FIG. **2**A through FIG. **2**E, sectional views showing a fabrication method of the semiconductor device **200** according to one embodiment of the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device **200** includes a substrate providing operation, a semiconductor die attaching operation, a connecting operation, an encapsulating operation, a carrier eliminating operation, and a solder ball fusing operation.

As shown in FIG. **2**A, in the substrate providing operation and the semiconductor die attaching operation, the substrate **100** having the carrier **110** at bottom surface thereof is provided. The semiconductor die **210** is bonded to the top surface of the substrate **100** by means of the adhesive **201**. Here, The carrier **110** provides a predetermined stiffness, so that the warpage is not generated during the manufacturing process of the semiconductor device.

As shown in FIG. **2**B, in the connecting operation, the bonding pads **160** of the substrate **100** and the I/O pads **211** of the semiconductor die **210** are electrically connected to each other by means of the connecting means **220**, that is, conductive wires.

As shown in FIG. **2**C, in the encapsulating operation, the semiconductor die **210** and the conductive connecting means **220** are encapsulated by the encapsulant **230**. Here, the encapsulant **230** also, covers the whole top surface of the substrate **100**.

FIG. **2**D shows carrier eliminating operation. If the carrier **110** is a metal, then the carrier **110** is completely eliminated by the chemical etching process. Accordingly, the bottom surface of the dielectric layer **120** of the substrate **100** is exposed to outside. Also, in the carrier eliminating operation by the chemical etching process, even the copper layer **131** of the conductive lands **130** of the substrate **100** is eliminated, so that the recess **124** of a predetermined depth is naturally formed at the dielectric layer **120** of the substrate **100**. At this time, only the gold layer **132** and the copper layer **133** as the conductive land **130** are left over the inside of the recess **124**.

However, if the carrier **110** is a film, then the carrier **110** is completely eliminated by the peeling off process (not shown). Accordingly, the bottom surface of the dielectric layer **120** of the substrate **100** is exposed to outside. Also, in the carrier eliminating operation by the peeling off process, the copper layer **131** of the conductive lands **130** of the substrate **100** is exposed to outside, unlike the above embodiment (not shown). That is, the recess **124** is not formed. Therefore, a bottom surface of the dielectric layer **120** may be flushed with a bottom surface of the copper layer **131**.

As shown in FIG. **2**E, in the solder ball fusing operation, the plurality of solder balls **240** is fused to the recess **124** and the conductive lands **130** of the substrate **100**, thereby completing the semiconductor device **200** according to the present invention. The solder ball fusing operation includes a flux applying process for applying a sticky flux to the conductive lands **130**, an attaching process for temporarily attaching the solder balls **240** to the flux, and a reflowing process of high temperature.

Referring to FIG. **3**, a sectional view of a semiconductor device **300** according to another embodiment of the present invention is illustrated.

Here, the semiconductor device **300** of FIG. **3** is almost similar to that of FIG. **2**, the description of the similar parts is omitted here.

As shown in FIG. **3**, the semiconductor die **310** can be connected to the substrate **100** in the form of a flip chip. That is, after solder bumps **320** are fused to I/O pads **311** of the semiconductor die, in a state that the semiconductor die **310** turns upside down, the solder bumps **320** can be connected to the bonding pads **160** of the substrate **100**. Here, an underfill **330** is filling between the semiconductor die **310** and the substrate **100**, so as to prevent the oxidation of the solder bump **320** and strength bonding force between the semiconductor die **310** and the substrate **100**. Also, the peripheral of the semiconductor die **310** and the underfill **330** are encapsulated by an encapsulant **340**, it can protect the semiconductor die **310** and so forth from the external impact. Here, a plurality of solder balls **350** is fused to conductive lands **130** of the substrate **100**.

Referring to FIG. **3**A through FIG. **3**E, sectional views showing a fabrication method of the semiconductor device **300** according to another embodiment of the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device **300** includes a substrate providing operation/a flip chip bonding operation, an underfilling operation, an encapsulating operation, a carrier eliminating operation, and a solder ball fusing operation.

As shown in FIG. **3**A, in the substrate providing operation/the flip chip bonding operation, the substrate **100** having the carrier **110** at bottom surface thereof is provided. Thereafter, the semiconductor die **310** is bonded on the top surface of the substrate **100** in the form of a flip chip. That is, after the solder bumps **320** are fused to I/O pads **311** of the semiconductor die **310**, the solder bumps **320** are electrically connected to the bonding pads **160** of the substrate **100** in a state that the semiconductor die **310** turns upside down.

As shown in FIG. **3**B, in the underfilling operation, the underfill **330** is injected into the gap between the semiconductor die **310** and the substrate **100**. Here, where the underfill **330** is injected into the gap between the semiconductor die **310** and the substrate **100**, the gap between the semiconductor die **310** and the substrate **100** completely fills with the underfill **330** through a capillary phenomenon.

As shown in FIG. **3**C, in the encapsulating operation, the peripherals of the semiconductor die **310** and the underfill **330** are encapsulated by the encapsulant **340**.

FIG. **3**D shows carrier eliminating operation. If the carrier **110** is a metal, then the carrier **110** completely eliminated by the chemical etching process. Accordingly, the bottom surface of the dielectric layer **120** of the substrate **100** is exposed to outside. Also, in the carrier eliminating operation by the chemical etching process, even the copper layer **131** of the conductive lands **130** of the substrate **100** is eliminated, so that the recess **124** of a predetermined depth is naturally formed at the dielectric layer **120** of the substrate **100**. At this time, only the gold layer **132** and the copper layer **133** as the conductive land **130** are left over the inside of the recess **124**.

However, if the carrier **110** is a film, then the carrier **110** is completely eliminated by the peeling off process (not shown). Accordingly, the bottom surface of the dielectric layer **120** of the substrate **100** is exposed to outside. Also, in the carrier eliminating operation by the peeling off process, the copper layer **131** of the conductive lands **130** of the substrate **100** is exposed to outside, unlike the above embodiment (not shown). That is, the recess **124** is not formed. Therefore, a bottom surface of the dielectric layer **120** may be flushed with a bottom surface of the copper layer **131**.

As shown in FIG. **3**E, in the solder ball fusing operation, the carrier **110** is eliminated and the plurality of solder balls **350** is fused to the conductive lands **130** exposed to outside through the dielectric layer **120**, thereby completing the semiconductor device **300** according to the present invention.

Referring to FIG. **4**, a sectional view of a substrate **400** for a semiconductor device according to another embodiment of the present invention is illustrated.

As shown in FIG. **4**, the substrate **400** for semiconductor device includes a carrier **410** having a predetermined stiffness, a first dielectric layer **420***a* having first electrically conductive patterns **440***a* and conductive lands **430**, a second dielectric layer **420***b* having second electrically conductive patterns **440***b*, a third dielectric layer **420***c* having third electrically conductive patterns **440***c*, a fourth dielectric layer **420***d* having fourth electrically conductive patterns **440***d* and bonding pads **460**, and a solder mask **450**.

The carrier **410** is in the form of an approximately planar plate. The material of the carrier **410** may be a metal, a ceramics, a glass or its equivalent, in order that the warpage is not generated during the manufacturing process of the semiconductor device. Moreover, in case of the metal as the material of the carrier **410**, the material of the carrier **410** may be a copper, an aluminum, a nickel or its equivalent.

The first dielectric layer **420***a* of a predetermined thickness is formed on the top surface of the carrier **410**. The plurality of conductive lands **430** connected to the carrier **410** is formed at the inside of the first dielectric layer **420***a*. The conductive land **430**, that is, a copper layer **431**, a gold layer **432**, another copper layer **433** may be plated on the carrier **410** in order. Also, the plurality of first electrically conductive patterns **440***a* is formed at the top surface of the first dielectric layer **420***a* and is electrically connected to the conductive lands **430** through via holes **423***a* formed at the first dielectric layer **420***a*.

The second dielectric layer **420***b* of a predetermined thickness is formed on the top surface of the first dielectric layer **420***a*. Also, the plurality of second electrically conductive patterns **440***b* is formed at the top surface of the second dielectric layer **420***b* and is electrically connected to the first electrically conductive patterns **440***a* through via holes **423***b* formed at the second dielectric layer **420***b*.

The third dielectric layer **420***c* of a predetermined thickness is formed on the top surface of the second dielectric layer **420***b*. Also, the plurality of third electrically conductive patterns **440***c* is formed at the top surface of the third dielectric layer **420***c* and is electrically connected to the second electrically conductive patterns **440***b* through via holes **423***c* formed at the third dielectric layer **420***c*.

The fourth dielectric layer **420***d* of a predetermined thickness is formed on the top surface of the third dielectric layer **420***c*. Also, the plurality of fourth electrically conductive patterns **440***d* is formed at the top surface of the fourth dielectric layer **420***d* and is electrically connected to the third electrically conductive patterns **440***c* through via holes **423***d* formed at the fourth dielectric layer **420***d*. Moreover, the bonding pads **460** including a nickel layer **461** and the gold layer **462** may be plated on predetermined regions of the fourth electrically conductive pattern **440***d* formed at the fourth dielectric layer **420***d*.

Meanwhile, in the illustrated case, the dielectric layer has only four layers. However, the present invention is not limited to the dielectric layer having only four layers. In accordance with the present invention, the dielectric layer may have three, four or more dielectric layer.

The solder mask **450** is formed on the top surface of the fourth dielectric layer **420***d* in order to cover the fourth electrically conductive patterns **440***d*. Accordingly, the solder mask **450** serves to protect the fourth electrically conductive patterns **440***d* from the external impact. However, the solder mask **450** does not cover the bonding pads **460**. That is, the bonding pads **460** are exposed to outside through the openings **451**.

Referring to FIG. **4**A through FIG. **4**F, sectional views showing a fabrication method of the semiconductor device according to another embodiment of the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device includes a multi layer forming operation, a solder mask printing operation, a solder mask exposing/developing operation, a photo sensitive film providing operation, a plating operation, and a photo sensitive film eliminating operation.

As shown in FIG. **4**A, in the multi layer forming operation, the first dielectric layer **420***a* having the first electrically conductive patterns **440***a* and conductive lands **430**, the second dielectric layer **420***b* having the second electrically conductive patterns **440***b*, the third dielectric layer **420***c* having the third electrically conductive patterns **440***c*, and the fourth dielectric layer **420***d* having the fourth electrically conductive patterns **440***d* are laminated on the carrier **410** in order. Here, the number of the layer may be less than 4 or more than 5. However, the present invention is not limited to the number of the layer.

As shown in FIG. **4**B, in the solder mask printing operation, the solder mask **450** of a predetermined thickness is printed on the fourth dielectric layer **420***d* in order to cover the fourth electrically conductive patterns **440***d* formed at the surface of the fourth dielectric layer **420***d*. The material of the solder mask **450** may be photosensitivity or insensitivity. The solder mask **450** serves to prevent the oxidation of the fourth electrically conductive patterns **440***d* and its damage from the external impact during the manufacturing process of the semiconductor device.

As shown in FIG. **4**C, in the solder mask exposing/developing operation, a predetermined region of the solder mask **450** is eliminated by the exposing/developing process. That is, the plurality of openings **451** is formed at the solder mask **450**, so that a predetermined area of each fourth electrically conductive pattern **440***d* is exposed to outside.

As shown in FIG. **4**D, in the photo sensitive film providing operation, the photo sensitive film **471** of a predetermined thickness is formed at the bottom surface of the carrier **410**. Here, since the photo sensitive film **471** serves to prevent the plating layer from being formed at the bottom surface of the carrier **410** during the plating process, the material of the photo sensitive film **471** may not be photosensitivity.

As shown in FIG. **4**E, in the plating operation, the plurality of bonding pads **460** is formed at predetermined regions of the fourth electrically conductive patterns **440***d* exposed to outside through the solder mask **450**. The plurality of bonding pads **460** can be formed by means of the electrolytic plating process. That is, the nickel layer **461** and the gold layer **462** may be plated on the fourth electrically conductive pattern **440***d* of a predetermined region exposed to outside through the opening **451** of the solder mask **450**, thereby forming the bonding pad **460** of a predetermined thickness. The bonding pad **460** serves to electrically connect with the semiconductor die **310** during manufacturing process of the semiconductor device.

As shown in FIG. **4**F, in the photo sensitive film eliminating operation, the photo sensitive film **471** formed on the bottom surface of the carrier **410** is eliminated by a chemical etching and the like thereby completing the substrate **400** according to the present invention. Here, the bottom surface of the carrier **410** is exposed to outside through the photo sensitive film elimination process.

Referring to FIG. **5**, a sectional view of a semiconductor device **500** according to another embodiment of the present invention is illustrated.

As shown in FIG. **5**, a semiconductor die **510** can be connected to the above substrate **400** in the form of a flip chip. That is, I/O pads **511** of the semiconductor die **510** are electrically connected to the bonding pads **460** formed at the fourth dielectric layer **420***d* of the substrate **400** by means of solder bumps **520**. Here, an underfill **530** is filling between the semiconductor die **510** and the fourth dielectric layer **420***d*. Also, the underfill **530** covers the solder bumps **520**, the solder mask **450**, the bonding pads **460** and the fourth dielectric layer **420***d* corresponding to the lower portion of the semiconductor die **510**.

In the meantime, the peripheral of the semiconductor die **510** and the underfill **530** are encapsulated by an encapsulant **540**. Here, the encapsulant **540** covers the solder mask **450** formed at the fourth dielectric layer **420***d*.

In the illustrated case, the semiconductor die **510** is connected to the substrate **400** in the form of the flip chip. However, the semiconductor die **510** can be connected to the substrate **400** by means of a wire bonding method.

Also, a plurality of solder balls **550** is fused to the substrate **400**, that is, the conductive lands **430** formed at the first dielectric layer **420***a*. Here, The solder ball **550** serves to mechanically and electrically connect the semiconductor device **500** to the external device. Also, each conductive land **430** includes a gold layer **432** and only one copper layer **433**.

Referring to FIG. **5**A through FIG. **5**E, sectional views showing a fabrication method of the semiconductor device **500** according to another embodiment of the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device **500** includes a substrate providing operation/a flip chip bonding operation, an underfilling operation, an encapsulating operation, a carrier eliminating operation and a solder ball fusing operation.

As shown in FIG. **5**A, in the substrate providing operation/the flip chip bonding operation, the substrate **400** of the multi layer having the carrier **410** at bottom surface thereof is provided. Thereafter, the semiconductor die **510** is bonded on the top surface of the substrate **400** in the form of the flip chip. That is, That is, after the solder bumps **520** are fused to the I/O pads **511** of the semiconductor die **510**, the solder bumps **520** are electrically connected to the bonding pads **460** of the substrate **400** in a state that the semiconductor die **510** turns upside down.

As shown in FIG. **5**B, in the underfilling operation, the underfill **530** is injected into the gap between the semiconductor die **510** and the substrate **400**. Here, where the underfill **530** is injected into the gap between the semiconductor die **510** and the substrate **400**. The gap between the semiconductor die **510** and the substrate **400** completely fills with the underfill **530** through a capillary phenomenon.

As shown in FIG. **5**C, in the encapsulating operation, the peripherals of the semiconductor die **510** and the underfill **530** are encapsulated by the encapsulant **540**. Also, the encapsulant **540** covers the solder mask **450** of the substrate **400**.

FIG. **5**D shows carrier eliminating operation. If the carrier **410** is a metal, then the carrier **410** completely eliminated by the chemical etching process. Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the chemical etching process, even the copper layer **431** of the conductive lands **430** of the substrate **400** is eliminated, so that the recess **424** of a predetermined depth is naturally formed at the dielectric layer **420***a* of the substrate **400**. At this time, only the gold layer **432** and the copper layer **433** as the conductive land **430** are left over the inside of the recess **424**.

However, if the carrier **410** is a film, then the carrier **410** is completely eliminated by the peeling off process (not shown). Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the peeling off process, the copper layer **431** of the conductive lands **430** of the substrate **400** is exposed to outside, unlike the above embodiment (not shown). That is, the recess **424** is not formed. Therefore, a

bottom surface of the dielectric layer **420***a* may be flushed with a bottom surface of the copper layer **431**.

As shown in FIG. **5**E, in the solder ball fusing operation, the carrier **410** is eliminated and the plurality of solder balls **550** is fused to the conductive lands **430** exposed to outside through the first dielectric layer **420***a*, thereby completing the semiconductor device **500** according to the present invention.

In the meantime, the semiconductor device **500** may be manufactured by another method.

That is, referring to FIG. **6**A through FIG. **6**E, sectional views showing another fabrication method of the semiconductor device **500** according to the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device **500** includes a carrier eliminating operation, a flip chip bonding operation, an underfilling operation, an encapsulating operation, and a solder ball fusing operation.

FIG. **6**A shows carrier eliminating operation. If the carrier **410** is a metal, then the carrier **410** completely eliminated by the chemical etching process. Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the chemical etching process, even the copper layer **431** of the conductive lands **430** of the substrate **400** is eliminated, so that the recess **424** of a predetermined depth is naturally formed at the dielectric layer **420***a* of the substrate **400**. At this time, only the gold layer **432** and the copper layer **433** as the conductive land **430** are left over the inside of the recess **424**.

However, if the carrier **410** is a film, then the carrier **410** is completely eliminated by the peeling off process (not shown). Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the peeling off process, the copper layer **431** of the conductive lands **430** of the substrate **400** is exposed to outside, unlike the above embodiment (not shown). That is, the recess **424** is not formed. Therefore, a bottom surface of the dielectric layer **420***a* may be flushed with a bottom surface of the copper layer **431**.

As shown in FIG. **6**B, in the flip chip bonding operation, the substrate, the semiconductor die **510** is bonded on the top surface of the substrate **400** in the form of the flip chip. That is, That is, after the solder bumps **520** are fused to the I/O pads **511** of the semiconductor die **510**, the solder bumps **520** are electrically connected to the bonding pads **460** of the substrate **400** in a state that the semiconductor die **510** turns upside down.

As shown in FIG. **6**C, in the underfilling operation, the underfill **530** is injected into the gap between the semiconductor die **510** and the substrate **400**. Here, where the underfill **530** is injected into the gap between the semiconductor die **510** and the substrate **400**, the gap between the semiconductor die **510** and the substrate **400** completely fills with the underfill **530** through a capillary phenomenon.

As shown in FIG. **6**D, in the encapsulating operation, the peripherals of the semiconductor die **510** and the underfill **530** are encapsulated by the encapsulant **540**. Also, the encapsulant **540** covers the solder mask **450** of the substrate **400**.

As shown in FIG. **6**E, in the solder ball fusing operation, the plurality of solder balls **550** is fused to the conductive lands **430** exposed to outside through the first dielectric layer **420***a*, thereby completing the semiconductor device **500** according to the present invention.

In the meantime, the semiconductor device **500** may be manufactured by another method. In other words, dissimilarly with the above methods, the semiconductor die **510** can be bonded on the bottom surface of the substrate **400** in the form of the flip chip and the plurality of solder balls **550** can be the top surface of the substrate **400**.

That is, referring to FIG. **7**A through FIG. **7**E, sectional views showing fabrication method of another semiconductor device **500'** according to the present invention is illustrated.

As shown in the drawings, the fabrication method of the semiconductor device **500'** includes a carrier eliminating operation, a flip chip bonding operation, an underfilling operation, an encapsulating operation, and a solder ball fusing operation.

FIG. **7**A shows carrier eliminating operation. If the carrier **410** is a metal, then the carrier **410** is completely eliminated by the chemical etching process. Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the chemical etching process, even the copper layer **431** of the conductive lands **430** of the substrate **400** is eliminated, so that the recess **424** of a predetermined depth is naturally formed at the dielectric layer **420***a* of the substrate **400**. At this time, only the gold layer **432** and the copper layer **433** as the conductive land **430** are left over the inside of the recess **424**.

However, if the carrier **410** is a film, then the carrier **410** is completely eliminated by the peeling off process (not shown). Accordingly, the bottom surface of the dielectric layer **420***a* of the substrate **400** is exposed to outside. Also, in the carrier eliminating operation by the peeling off process, the copper layer **431** of the conductive lands **430** of the substrate **400** is exposed to outside, unlike the above embodiment (not shown). That is, the recess **424** is not formed. Therefore, a bottom surface of the dielectric layer **420***a* may be flushed with a bottom surface of the copper layer **431**.

As shown in FIG. **7**B, in the flip chip bonding operation, the substrate, the semiconductor die **510** is bonded on the conductive lands **430**, that is, the gold layer **432** exposed to outside through the recesses **424** in the form of the flip chip. That is, after the solder bumps **520** are fused to the I/O pads **511** of the semiconductor die **510**, the solder bumps **520** are electrically connected to the conductive lands **430** of the substrate **400**.

As shown in FIG. **7**C, in the underfilling operation, the underfill **530** is injected into the gap between the semiconductor die **510** and the substrate **400**. Here, where the underfill **530** is injected into the gap between the semiconductor die **510** and the first dielectric layer **420***a* corresponding to the semiconductor die **510**, the gap between the semiconductor die **510** and the first dielectric layer **420***a* completely fills with the underfill **530** through a capillary phenomenon. Here, the underfill **530** completely covers the solder bumps **520**, thereby preventing the oxidation of the solder bump **520**.

As shown in FIG. **7**D, in the encapsulating operation, the semiconductor die **510** and the underfill **530** are encapsulated by the encapsulant **540**. Also, the encapsulant **540** covers the bottom surface of the first dielectric layer **420***a*, not the solder mask.

As shown in FIG. **7**E, in the solder ball fusing operation, the plurality of solder balls **550** is fused to the bonding pads **460**, not the conductive lands **430**. That is, the plurality of solder balls **550**, not the semiconductor die **510** is fused to the bonding pads **460** exposed to outside through the openings **451** of the solder mask **450** and formed at the fourth dielectric layer **420***d*. Here, after a flux is applied on the bonding pads **460***d*, the solder balls are temporarily attached on the bonding pads **460***d* and then, the solder balls are thoroughly fixed to the bonding pads **460***d* by means of a reflow process of a high temperature, thereby completing the semiconductor device **500'**.

This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for or implied by the specification, such as variations in structure, dimension and type of material and the manufacturing process may be implemented by one who is skilled in the art, in view of this disclosure.

What is claimed is:

**1**. A substrate for a semiconductor package comprising:

a dielectric layer having a first surface and a second surface opposed to the first surface;

a plurality of conductive lands having a surface substantially coplanar with the first surface of the dielectric layer at an inside of the dielectric layer, wherein the conductive lands comprise a copper layer, a gold layer, another copper layer in order;

a metal carrier of an approximately planar plate bonded at the first surface of the dielectric layer and connected to the conductive lands;

a plurality of electrically conductive patterns electrically connected to the conductive lands at the second surface of the dielectric layer; and

a solder mask covering the dielectric layer and the electrically conductive patterns and having a plurality of openings, a predetermined area of each conductive pattern being exposed to outside through the openings.

**2**. The substrate for a semiconductor package as claimed in claim **1**, wherein a plurality of via holes of a predetermined depth is further formed at the second surface of the dielectric layer facing the first surface thereof and the electrically conductive patterns are electrically connected to the conductive lands through the via holes.

**3**. The substrate for a semiconductor package as claimed in claim **1**, wherein a plurality of bonding pads is formed at the electrically conductive patterns exposed to outside through the openings of the solder mask.

**4**. The substrate for a semiconductor package as claimed in claim **3**, wherein each bonding pad comprises a nickel layer and a gold layer in order.

**5**. The substrate for a semiconductor package as claimed in claim **1**, wherein the dielectric layer has a plurality of layers stacked up on one another and each layers has the electrically conductive patterns.

**6**. A semiconductor package comprising:

a substrate comprising a single layer dielectric layer, a plurality of conductive lands formed inside of the dielectric layer at a bottom surface of the dielectric layer, wherein the dielectric layer comprises a plurality of recesses at the bottom surface of the dielectric layer, the conductive lands being formed inside of the recesses, and a plurality of electrically conductive patterns formed at a top surface of the dielectric layer and connected to the plurality of conductive lands, wherein a plurality of bonding pads is formed at the electrically conductive patterns;

a solder mask covering the dielectric layer and the electrically conductive patterns and having a plurality of openings, the bonding pads being located within the openings and being spaced apart from the solder mask so that portions of the top surface of the dielectric layer around the bonding pads are exposed through the openings;

a semiconductor die attached to a top surface of the substrate and connected to the electrically conductive patterns;

an encapsulant for encapsulating the top surface of the substrate and the semiconductor die; and

a plurality of solder balls fused to the conductive lands of the substrate, wherein each solder ball of the plurality of solder balls extends into only a single respective recess of the plurality of recesses, wherein the conductive lands comprise:

a copper layer; and

a gold layer on the copper layer, the solder balls being fused to the gold layer.

**7**. The semiconductor package as claimed in claim **6**, wherein the semiconductor die is connected to the electrically conductive patterns by conductive connecting means selected from the group consisting of conductive wires and solder bumps.

**8**. A substrate for a semiconductor package, comprising:

a metal carrier of a planar plate;

a plurality of conductive lands on a surface of the carrier, wherein the conductive lands comprise a copper layer, a gold layer, another copper layer in order;

a dielectric layer on the surface of the carrier covering the conductive lands;

a plurality of electrically conductive patterns on a surface of the dielectric layer electrically connected to the conductive lands; and

a solder mask on surfaces of the dielectric layer and the electrically conductive patterns, a predetermined area of each conductive pattern being exposed to outside through openings of the solder mask.

**9**. The substrate for a semiconductor package as claimed in claim **8**, wherein the dielectric layer comprises a first surface and a second surface opposed to the first surface, the first surface of the dielectric layer being bonded to the surface of the carrier.

**10**. The substrate for a semiconductor package as claimed in claim **9**, wherein a plurality of via holes of a predetermined depth is further formed at the second surface of the dielectric layer facing the first surface thereof and the electrically conductive patterns are electrically connected to the conductive lands through the via holes.

**11**. The substrate for a semiconductor package as claimed in claim **8**, wherein a plurality of bonding pads is formed at the electrically conductive patterns exposed to outside through the openings of the solder mask.

**12**. The substrate for a semiconductor package as claimed in claim **11**, wherein each bonding pad comprises a nickel layer and a gold layer in order.

**13**. The substrate for a semiconductor package as claimed in claim **1**, wherein the carrier comprises copper.

**14**. The substrate for a semiconductor package as claimed in claim **8**, wherein the carrier comprises copper.

**15**. A semiconductor package comprising:

a substrate comprising a single layer dielectric layer, a plurality of conductive lands formed inside of the dielectric layer at a bottom surface of the dielectric layer, wherein the dielectric layer comprises a plurality of recesses at the bottom surface of the dielectric layer, the conductive lands being formed inside of the recesses, and a plurality of electrically conductive patterns formed at a top surface of the dielectric layer and connected to the plurality of conductive lands, wherein a plurality of bonding pads is formed at the electrically conductive patterns;

a solder mask covering the dielectric layer and the electrically conductive patterns and having a plurality of openings, the bonding pads being located within the openings and being spaced apart from the solder mask so that portions of the top surface of the dielectric layer around the bonding pads are exposed through the openings;

a semiconductor die attached to a top surface of the substrate and connected to the electrically conductive patterns, wherein the semiconductor die is connected to top surfaces of the bonding pads by conductive wires;

an encapsulant for encapsulating the top surface of the substrate and the semiconductor die, wherein the encapsulant encapsulates the conductive wires, the top and side surfaces of the bonding pads, and the portions of the top surface of the dielectric layer around the bonding pads exposed through the openings; and

a plurality of solder balls fused to the conductive lands of the substrate, wherein each solder ball of the plurality of solder balls extends into only a single respective recess of the plurality of recesses.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO. : 7,902,660 B1
APPLICATION NO. : 11/440548
DATED : March 8, 2011
INVENTOR(S) : Kyu Won Lee, Doo Hyun Park and Dong Hee Kang

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 15, Line 43, Claim 5, replace "each layers" with --each layer--.

Signed and Sealed this
Twentieth Day of September, 2011

David J. Kappos
*Director of the United States Patent and Trademark Office*