



US007880660B2

(12) **United States Patent**
Sutardja

(10) **Patent No.:** **US 7,880,660 B2**
(45) **Date of Patent:** ***Feb. 1, 2011**

(54) **PIPELINED ANALOG-TO-DIGITAL CONVERTERS**

(75) Inventor: **Sehat Sutardja**, Los Altos Hills, CA (US)

(73) Assignee: **Marvell World Trade Ltd.**, St. Michael (BB)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/475,947**

(22) Filed: **Jun. 1, 2009**

(65) **Prior Publication Data**

US 2009/0231174 A1 Sep. 17, 2009

Related U.S. Application Data

(63) Continuation of application No. 11/333,935, filed on Jan. 18, 2006, now Pat. No. 7,541,962.

(51) **Int. Cl.**
H03M 1/38 (2006.01)

(52) **U.S. Cl.** **341/161**; 341/155

(58) **Field of Classification Search** 341/155, 341/118, 120, 161, 156
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,179,687 A * 12/1979 van de Plassche et al. ... 341/162

4,611,196 A *	9/1986	Fernandez	341/158
5,394,148 A	2/1995	Matsuura et al.		
5,682,163 A	10/1997	Hsu		
5,771,012 A *	6/1998	Shu et al.	341/118
5,784,016 A	7/1998	Nagaraj		
5,966,088 A	10/1999	Matsumoto et al.		
6,606,048 B1	8/2003	Sutardja		
6,710,735 B1	3/2004	Lin		
6,839,015 B1	1/2005	Sutardja et al.		
6,882,297 B2	4/2005	Wada et al.		
6,914,550 B2	7/2005	Cai		
7,158,066 B2	1/2007	Lee		
7,161,521 B2	1/2007	Nandi et al.		
7,183,962 B1 *	2/2007	Roo et al.	341/155

OTHER PUBLICATIONS

Communication from the European Patent Office dated Feb. 21, 2007 with the extended European Search Report for Application No. 06024141.1—2206; 6 pages.

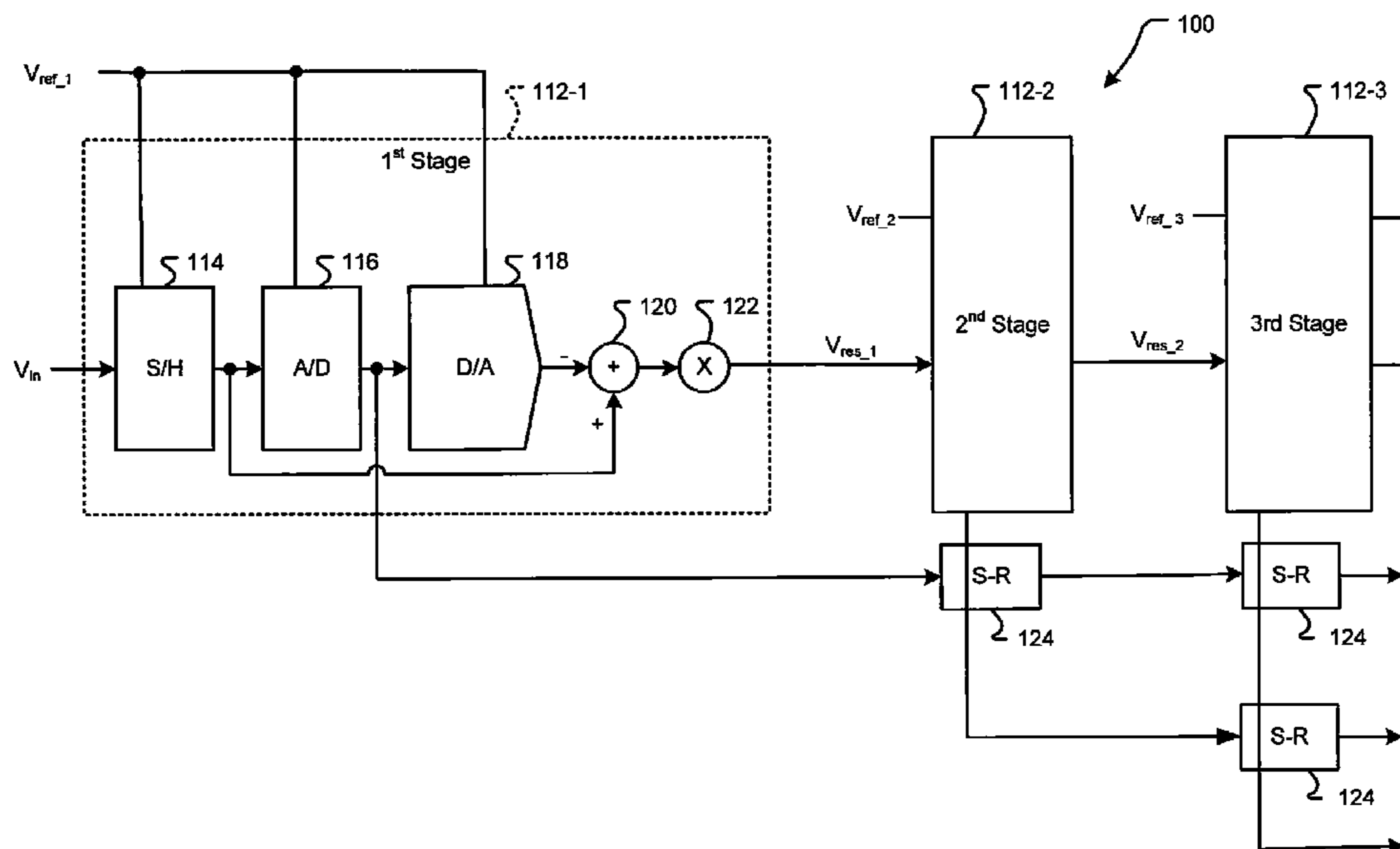
* cited by examiner

Primary Examiner—Peguy JeanPierre

(57) **ABSTRACT**

An analog-to-digital converter including a first stage and a second stage. The first stage receives a first reference voltage and a first analog input voltage, generates a first digital signal by quantizing the first analog input voltage, and generates a first analog output voltage based on the first digital signal and the first analog input voltage. The second stage receives a second reference voltage and the first analog output voltage, in which the second reference voltage is lower than the first reference voltage. The second stage further generates a second digital signal by quantizing the first analog output voltage, and generates a second analog output voltage based on the second digital signal and the first analog output voltage.

13 Claims, 9 Drawing Sheets



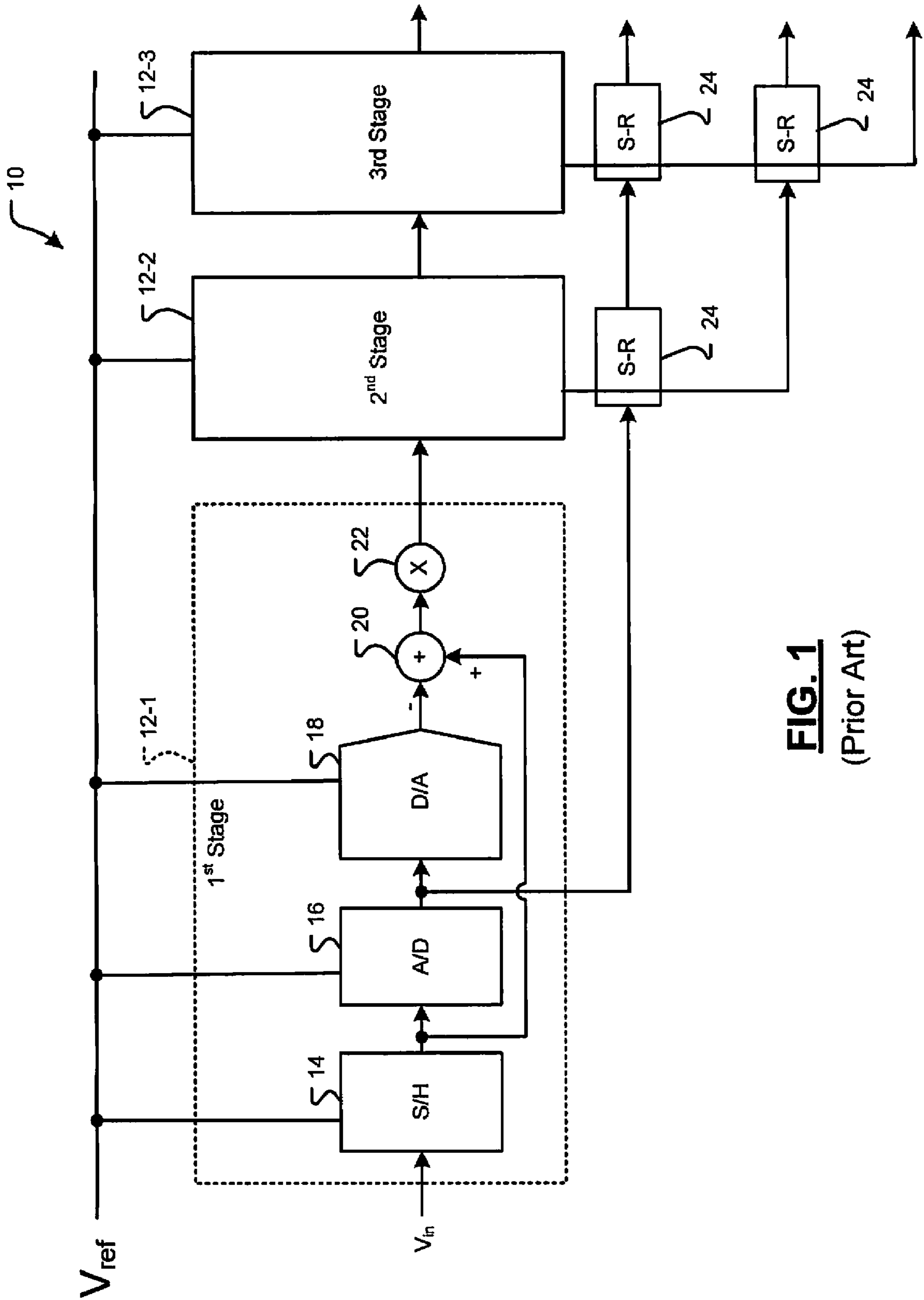


FIG. 1
(Prior Art)

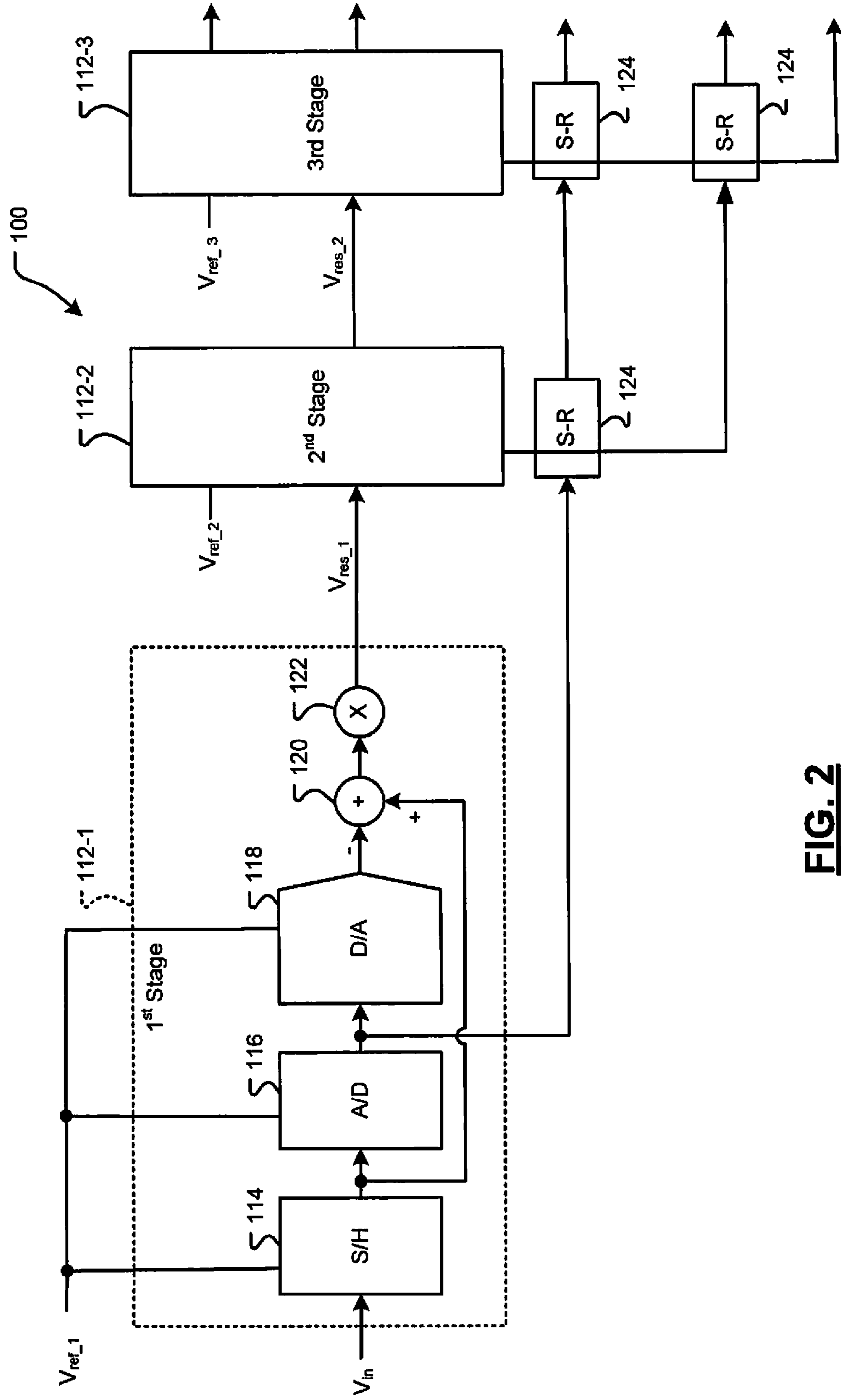


FIG. 2

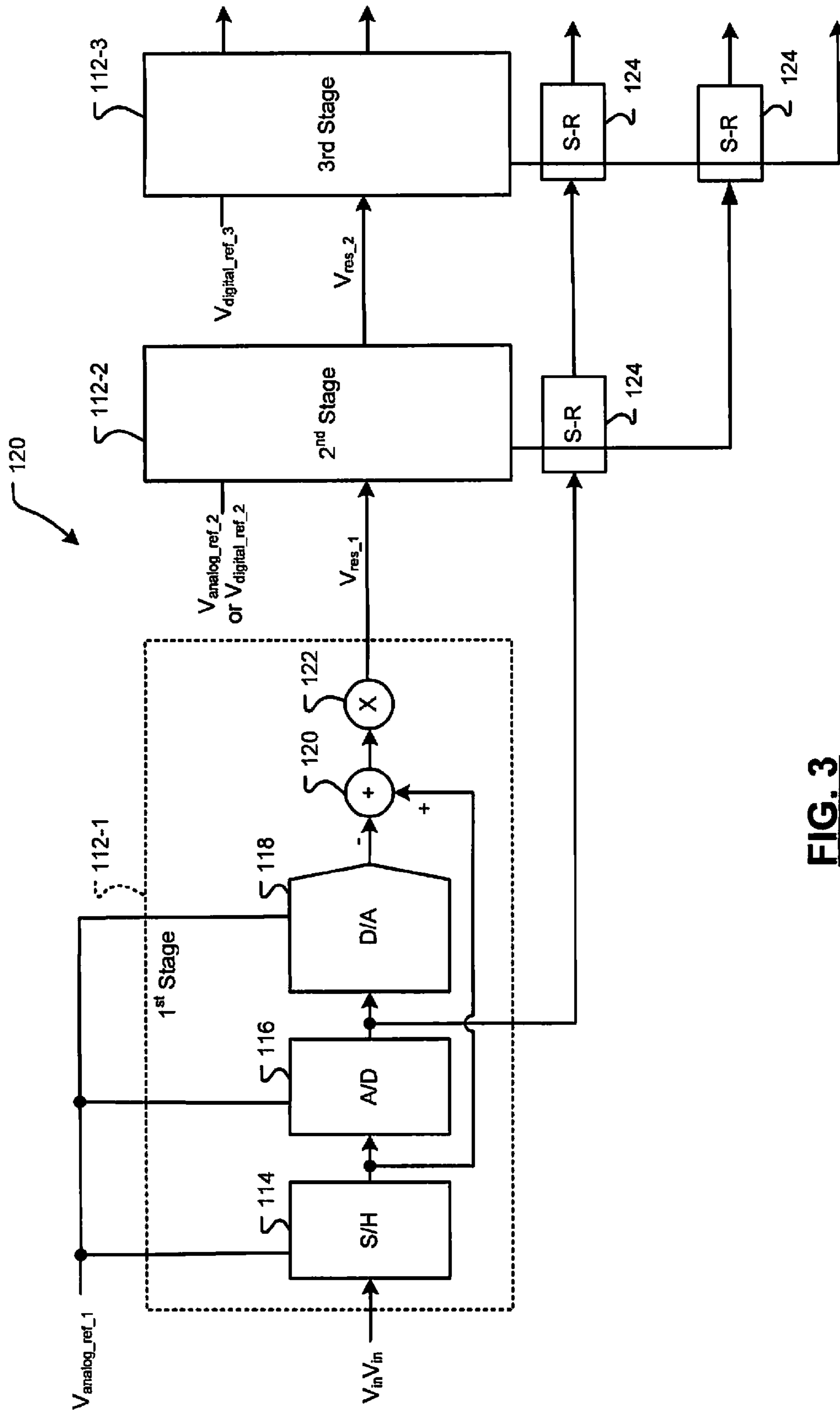


FIG. 3

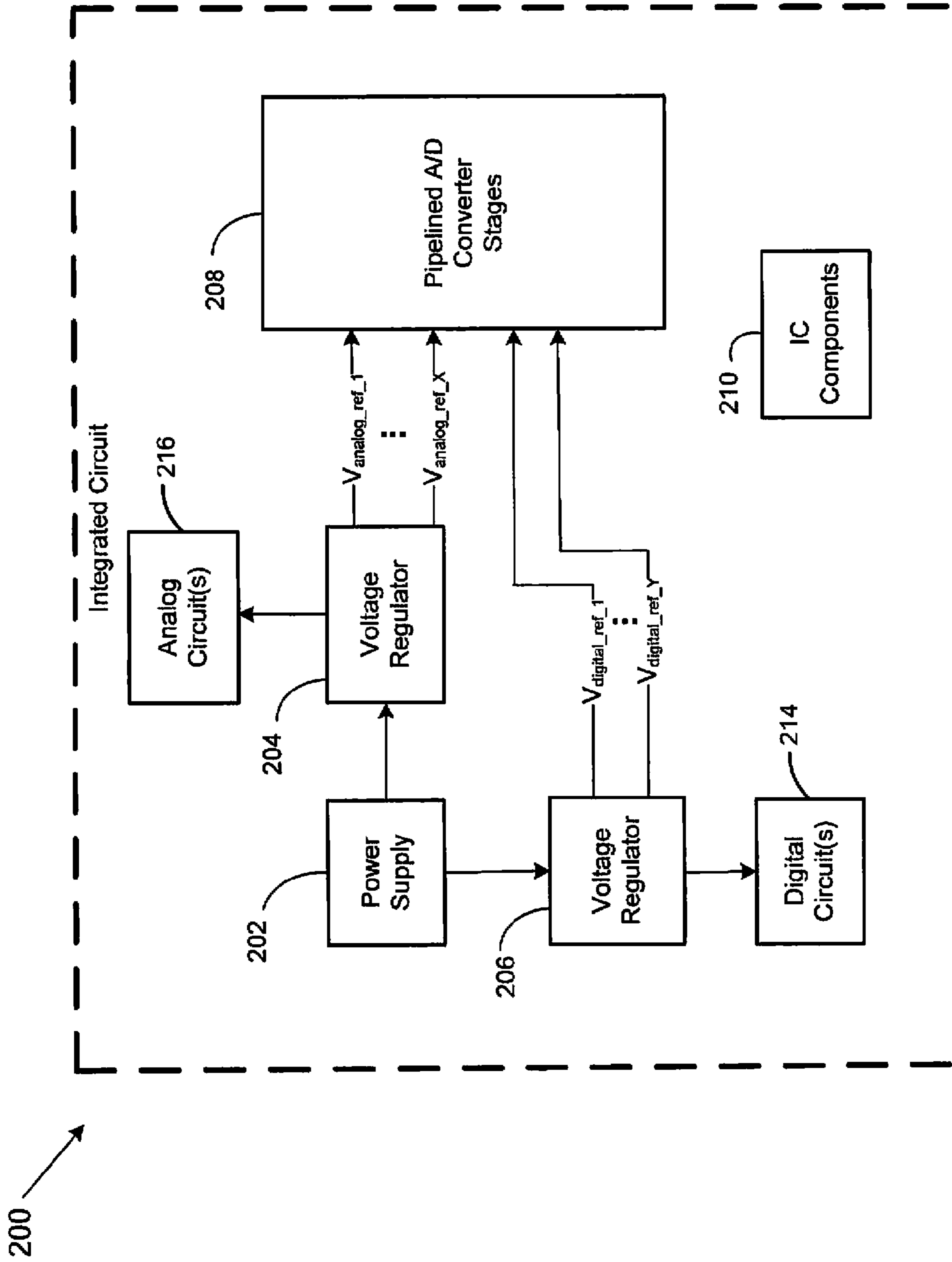


FIG. 4

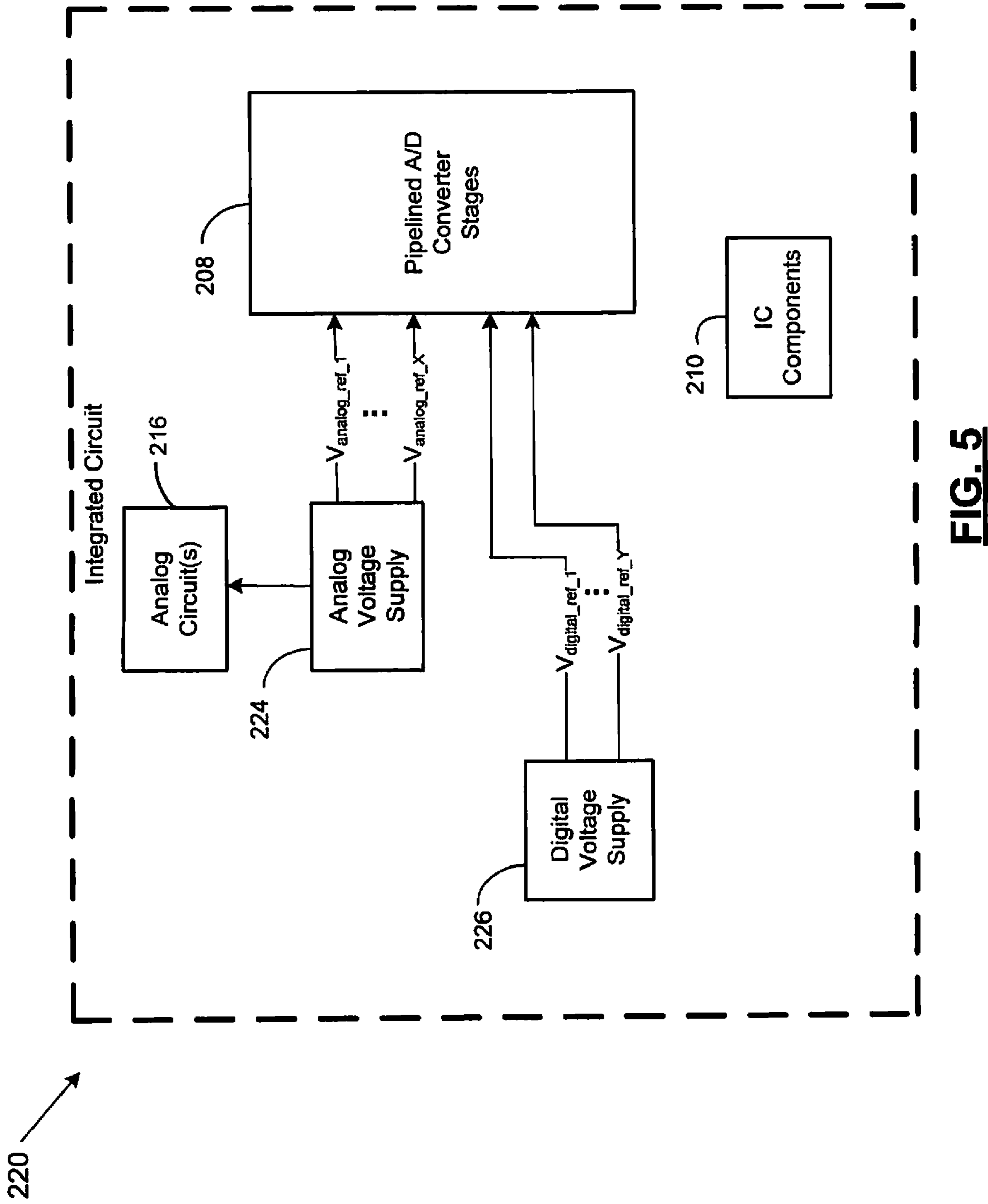


FIG. 5

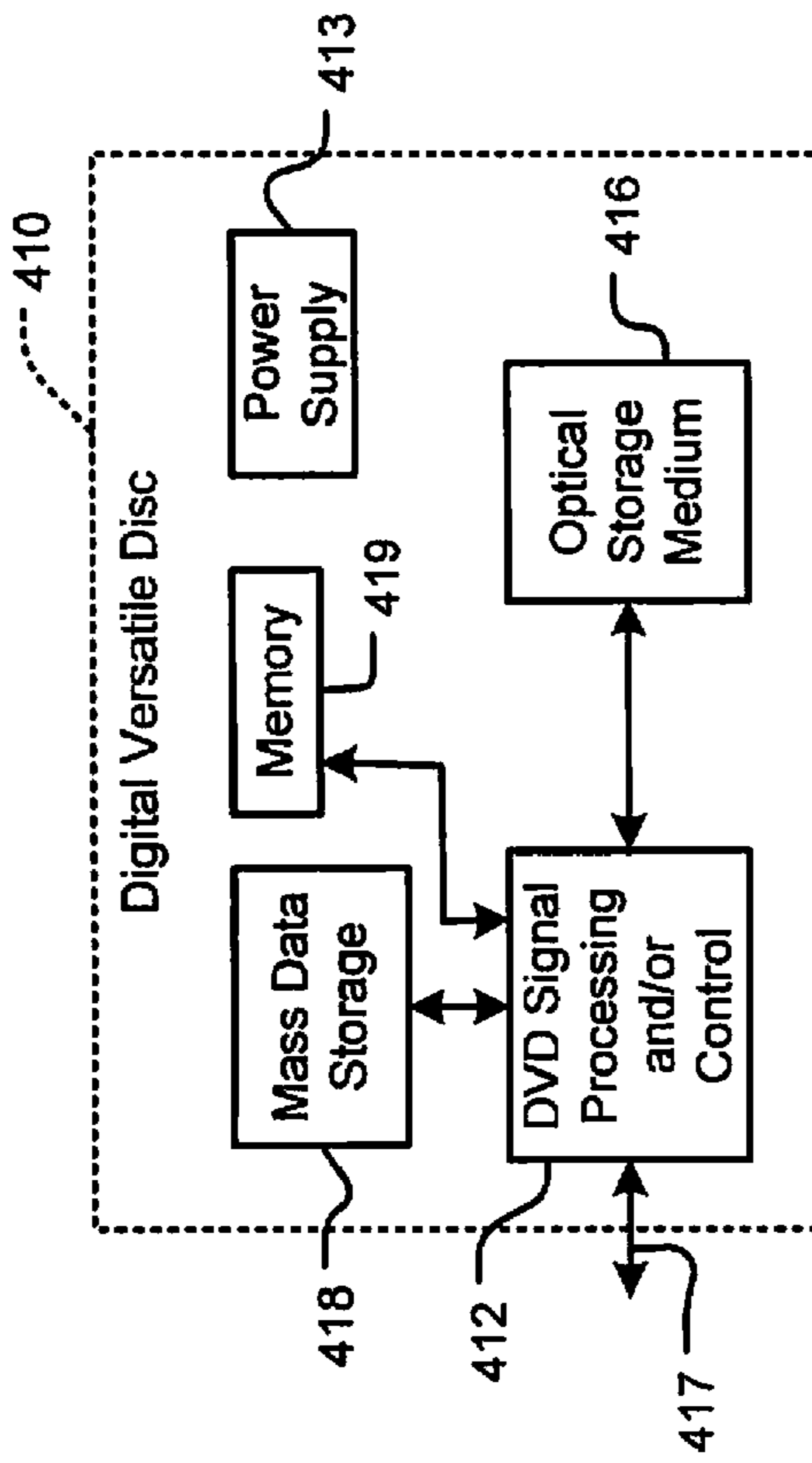


FIG. 6B

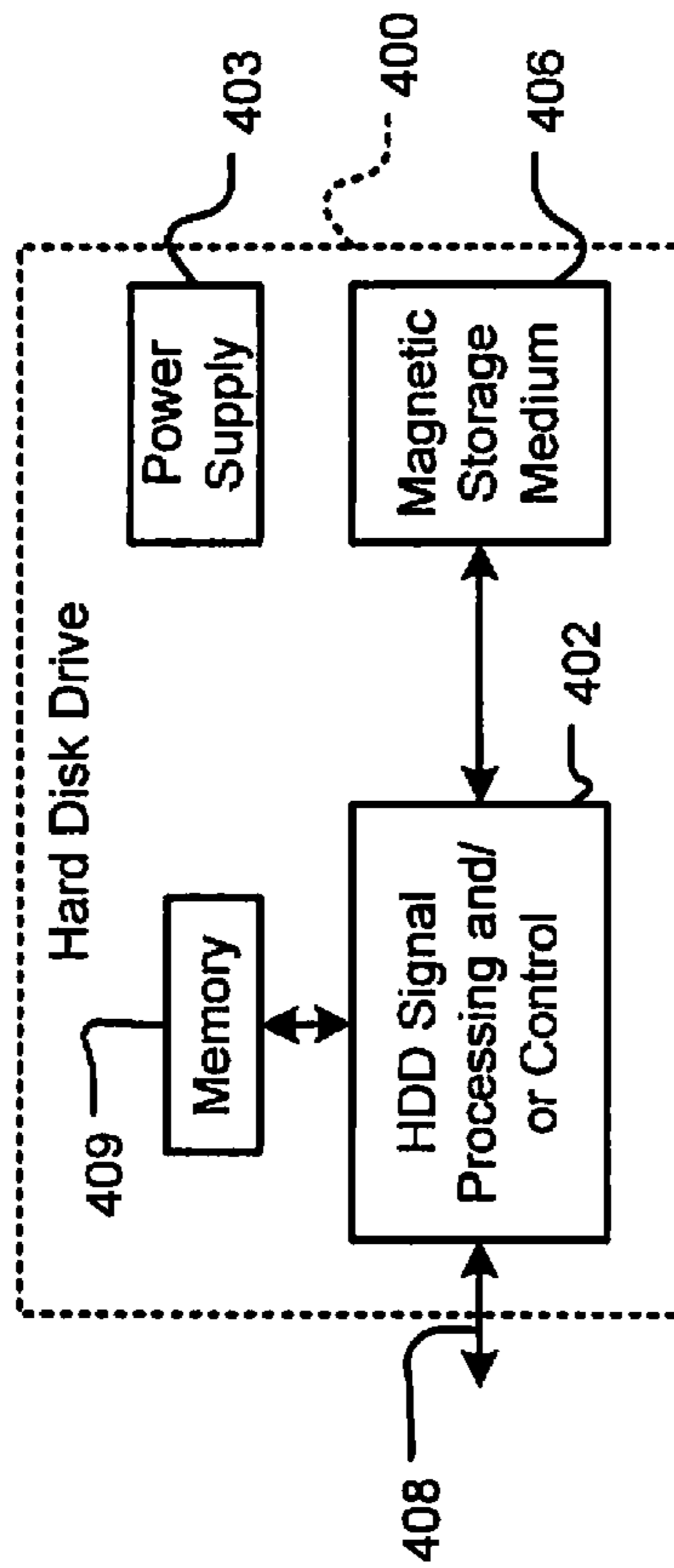


FIG. 6A

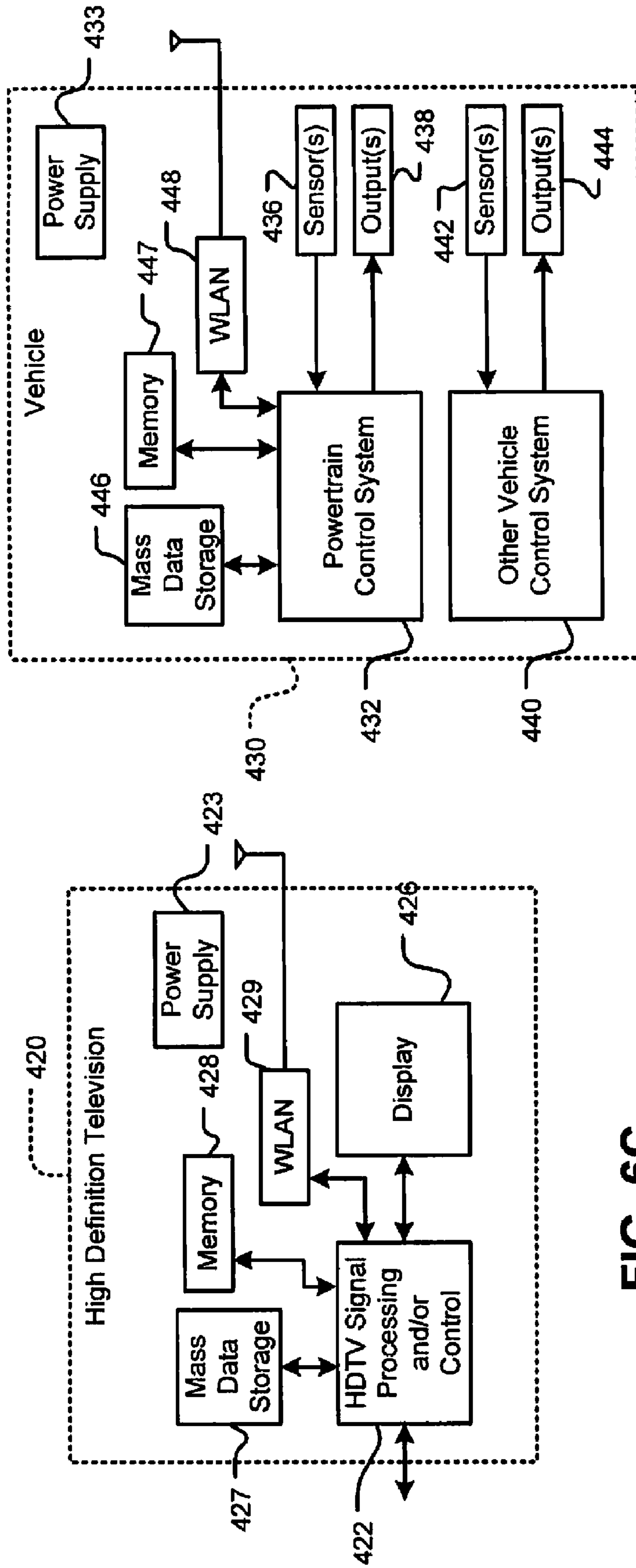


FIG. 6C

FIG. 6D

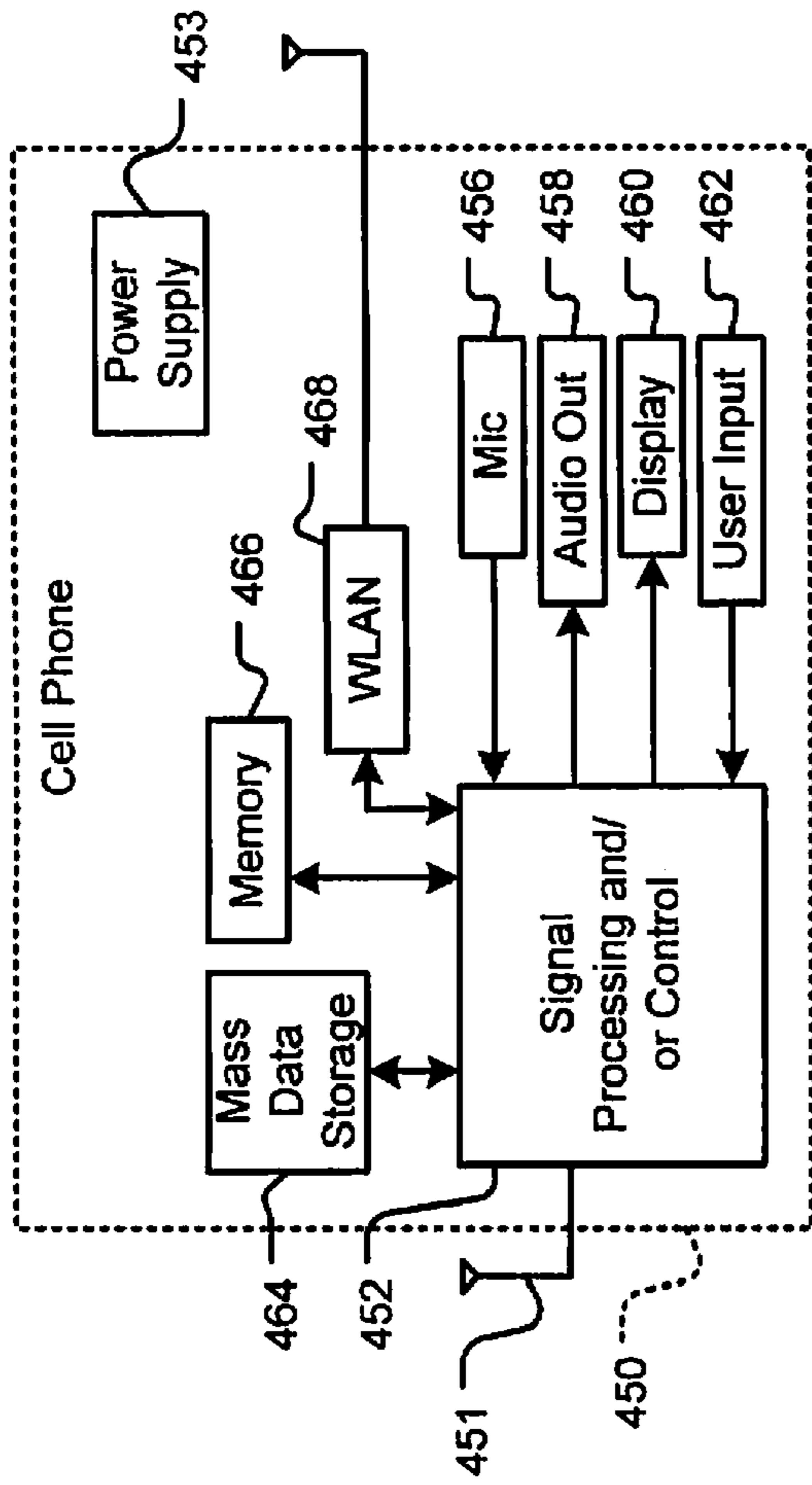


FIG. 6E

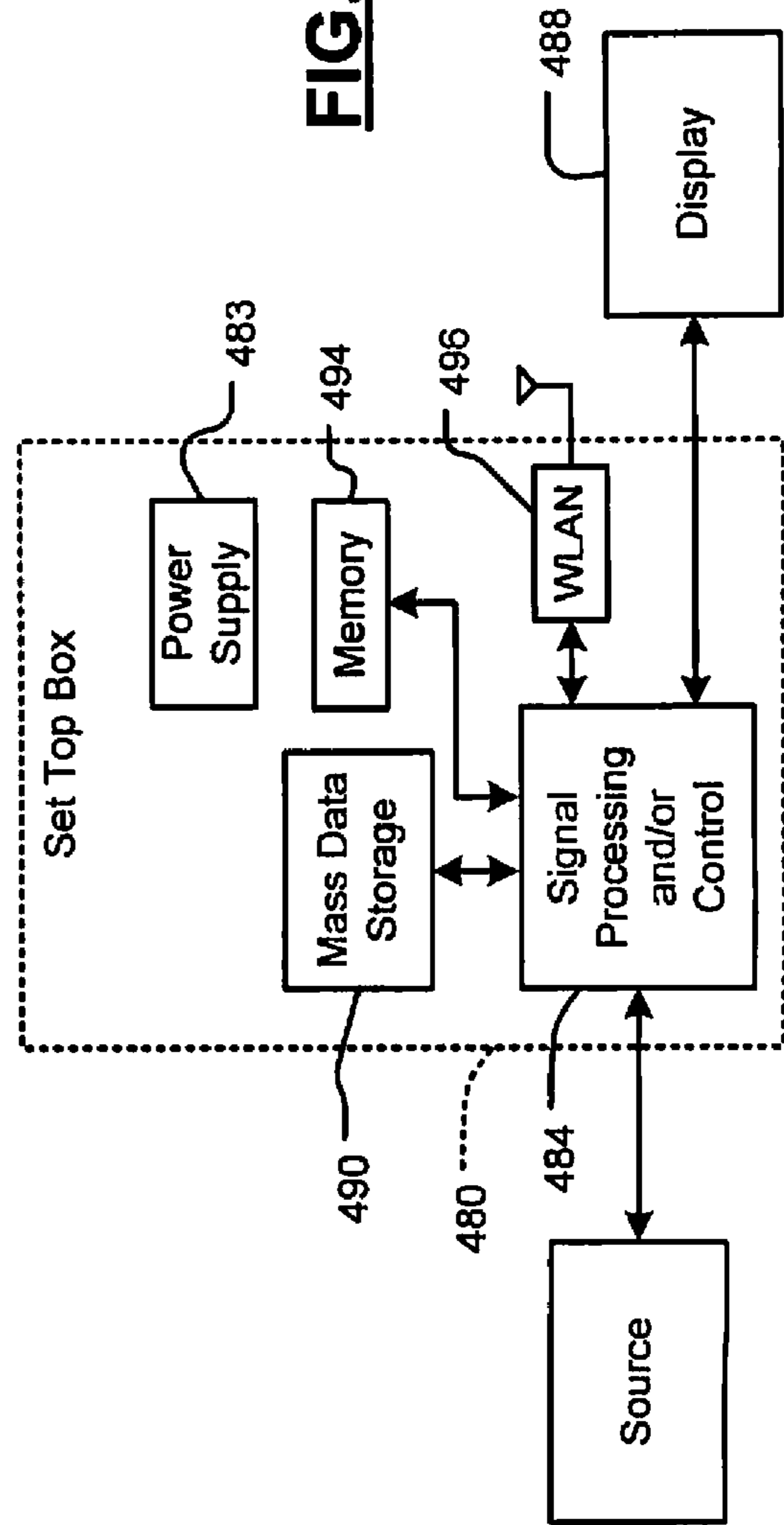


FIG. 6F

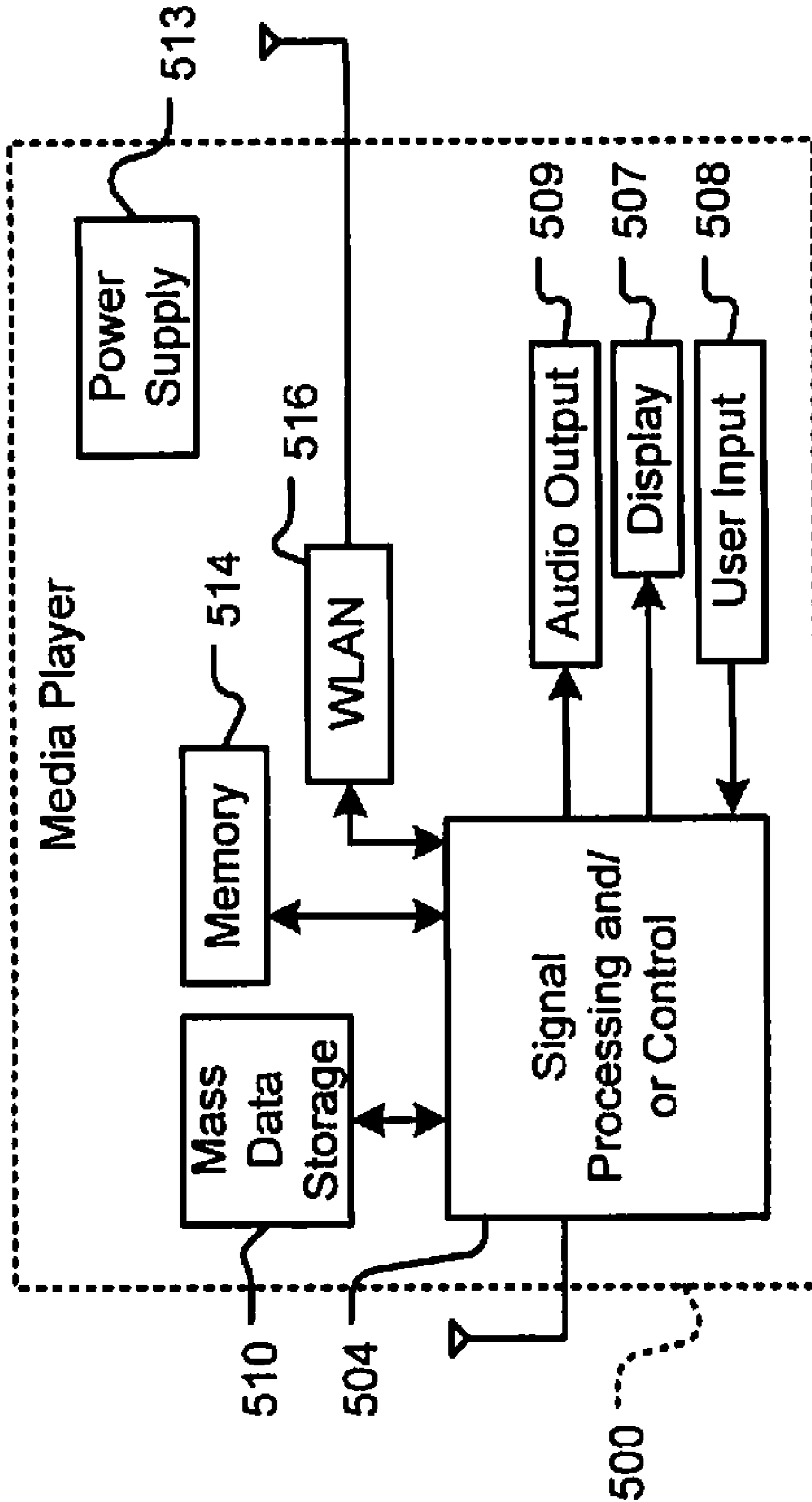


FIG. 6G

1

PIPELINED ANALOG-TO-DIGITAL CONVERTERS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 11/333,935 (now U.S. Pat. No. 7,541,962), filed Jan. 18, 2006. The disclosure of the above application is incorporated herein by reference.

FIELD

The present disclosure relates to pipelined analog-to-digital converters (ADCs).

BACKGROUND

Reducing power consumption of electronic devices has become increasingly important, particularly for battery powered devices such as laptop computers, personal digital assistants, cellular phones, MP3 players and other devices. Analog-to-digital converters (ADCs) are commonly used in these electronic devices to transform analog signals to digital signals. The ADC may include a pipelined ADC that utilizes multiple stages. Each stage employs a sample and hold circuit that samples an analog input voltage V_{in} to the pipelined ADC or a residue voltage V_{res} from a prior stage. In addition, each of the stages receives a reference voltage V_{ref} .

Referring now to FIG. 1, a typical pipelined ADC **10** is shown. The ADC **10** includes a plurality of stages **12-1**, **12-2**, and **12-3** (collectively stages **12**) that are cascaded in series. Although three stages **12-1**, **12-2**, and **12-3** are shown, the pipelined ADC **10** may include additional or fewer stages. Some of the A/D converter stages **12** include a sample and hold module **14** that samples and holds the analog input signal V_{in} or the residue signal V_{res} from a prior stage. A low resolution A/D subconverter module **16** quantizes the held analog signal to a resolution of B_i bits where i corresponds to the current stage of the pipelined A/D converter **10**. The number of bits per stage B_i and/or the number of stages may be determined in part by the desired sampling rate and resolution. The output of the A/D subconverter module **16** is supplied to a low-resolution D/A subconverter module **18** that converts the resulting digital output signal back into an analog representation.

The D/A subconverter module **18** may have a resolution that is equivalent to that of the corresponding A/D subconverter module **16** of the same stage. A difference module **20** subtracts the analog output from the D/A subconverter module **18** from the voltage input V_{in} to generate a residue signal V_{res} . The residue signal V_{res} is equal to the difference between the held analog signal (V_{in} or V_{res} from the prior stage) and the reconstructed analog signal.

An analog interstage difference module **22** may be used to amplify the residue signal. The amplified residue signal is output to the next stage **12-2** of the pipelined ADC **10**. The first ADC stage **12-1** of the pipelined ADC **10** operates on a most current analog input sample while the second ADC stage **12-2** operates on the amplified residue of the prior input sample. The third stage **12-3** operates on the amplified residue output by the second ADC stage **12-2**.

The concurrency of operations allows a conversion speed that is determined by the time it takes in one stage. Once a current stage has completed operating on the analog input sample received from the prior stage, the current stage is available to operate on the next sample.

2

SUMMARY

In general, in one aspect, this specification describes an analog-to-digital converter. The analog-to-digital converter includes a first stage and a second stage. The first stage receives a first reference voltage and a first analog input voltage, generates a first digital signal by quantizing the first analog input voltage, and generates a first analog output voltage based on the first digital signal and the first analog input voltage. The second stage receives a second reference voltage and the first analog output voltage, in which the second reference voltage is lower than the first reference voltage. The second stage further generates a second digital signal by quantizing the first analog output voltage, and generates a second analog output voltage based on the second digital signal and the first analog output voltage.

In general, in another aspect, this specification describes a method for converting an analog signal to a digital signal. The method includes receiving a first analog input voltage, using a first reference voltage to generate a first digital signal by quantizing the first analog input voltage, generating a first analog output voltage based on the first digital signal and the first analog input voltage, and using a second reference voltage to generate a second digital signal by quantizing the first analog output voltage. The second reference voltage is lower than the first reference voltage.

Further areas of applicability of the present disclosure will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the disclosure, are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure will become more fully understood from the detailed description and the accompanying drawings.

FIG. 1 is a functional block diagram of a pipelined analog to digital converter (ADC) according to the prior art.

FIG. 2 is a functional block diagram of an exemplary pipelined ADC according to the present invention.

FIG. 3 is a functional block diagram of another exemplary pipelined ADC according to the present invention.

FIG. 4 is a functional block diagram of an integrated circuit including a pipelined ADC according to the present invention.

FIG. 5 is a functional block diagram of an integrated circuit including an analog voltage supply, a digital voltage supply, and a pipelined ADC according to the present invention.

FIG. 6A is a functional block diagram of a hard disk drive.

FIG. 6B is a functional block diagram of a digital versatile disk (DVD).

FIG. 6C is a functional block diagram of a high definition television.

FIG. 6D is a functional block diagram of a vehicle control system.

FIG. 6E is a functional block diagram of a cellular phone.

FIG. 6F is a functional block diagram of a set top box.

FIG. 6G is a functional block diagram of a media player.

DETAILED DESCRIPTION

The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar

elements. As used herein, the term module, circuit and/or device refers to an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical or. It should be understood that steps within a method may be executed in different order without altering the principles of the present disclosure.

Referring now to FIG. 2, a pipelined ADC 100 according to the present invention including multiple reference voltages V_{ref_i} is shown, where i corresponds to the current stage of the pipelined ADC 100. The pipelined ADC 100 includes stages 112-1, 112-2, and 112-3 (collectively stages 112). Stage 112-1 includes a sample and hold module 114, an ADC module 116, a digital to analog converter (DAC) module 118, a difference module 120 and an amplifier module 122. While three stages are shown, additional or fewer stages can be used. In FIG. 2, $V_{ref_1} \cong V_{ref_2}$ and $V_{ref_1} > V_{ref_3}$. The quantization of bits by a subsequent stage of the pipelined ADC 100 does not require the same signal to noise levels (SNR) as the current stage and therefore a lower reference voltage can be used for at least one of the second and third stages.

The power consumed by stages 112-1, 112-2, and 112-3 of the pipelined ADC 100 is related to the reference voltage of each stage. As a result, the pipelined ADC 100 tends to consume less power than a pipelined ADC having stages supplied with the same reference voltage as shown in FIG. 1.

Referring now to FIG. 3, a pipelined ADC 120 including different reference voltages, V_{ref_i} is shown, where i corresponds to the current stage of the pipelined A/D converter 120. At least one of the reference voltages V_{ref_i} is derived from an analog supply voltage V_{analog_ref} for analog circuits in the system containing the ADC 120 and at least one of the reference voltages is derived from a digital supply voltage $V_{digital_ref}$ for digital circuit in the system containing the ADC 120.

Referring now to FIG. 4, an integrated circuit (IC) 200 is shown. One or more power supply 202 supplies unregulated voltage to voltage regulators 204, 206. A first voltage regulator 204 provides analog supply voltages, $V_{analog_ref_1}$, $V_{analog_ref_2}$, . . . and $V_{analog_ref_X}$, where X is an integer greater than zero. A second voltage regulator 206 provides digital supply voltages, $V_{digital_ref_1}$, $V_{digital_ref_2}$, . . . , and $V_{digital_ref_Y}$, where Y is an integer greater than zero. The IC 200 may also include IC components 210 to perform additional circuit functions. The first voltage regulator 204 also supplies one or more analog circuits 216 in the IC 200. The second voltage regulator 206 also supplies one or more digital circuits 214.

Referring now to FIG. 5, an integrated circuit (IC) 220 is shown. An analog voltage supply 224 generates analog supply voltages, $V_{analog_ref_1}$, $V_{analog_ref_2}$, . . . , and $V_{analog_ref_X}$, where X is an integer greater than zero. A digital voltage supply 226 generates digital supply voltages, $V_{digital_ref_1}$, $V_{digital_ref_2}$, . . . , and $V_{digital_ref_Y}$, where Y is an integer greater than zero. The IC 220 may also include IC components 210 to perform additional circuit functions. The analog voltage supply 224 also supplies one or more analog circuits 216 in the IC 200. The digital voltage supply 226 also supplies one or more digital circuits 214.

Referring now to FIGS. 6A-6G, various exemplary implementations of the device are shown. Referring now to FIG. 6A, the device can be implemented in one of more ADCs in a hard disk drive 400. The device may implement and/or be

implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. 6A at 402 and/or in a power supply 403. In some implementations, the signal processing and/or control circuit 402 and/or other circuits (not shown) in the HDD 400 may process data, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium 406.

The HDD 400 may communicate with a host device (not shown) such as a computer, mobile computing devices such as personal digital assistants, cellular phones, media or MP3 players and the like, and/or other devices via one or more wired or wireless communication links 408. The HDD 400 may be connected to memory 409 such as random access memory (RAM), low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage.

Referring now to FIG. 6B, the device can be implemented in one of more ADCs in a digital versatile disc (DVD) drive 410. The device may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. 6B at 412, mass data storage of the DVD drive 410 and/or a power supply 413. The signal processing and/or control circuit 412 and/or other circuits (not shown) in the DVD 410 may process data, perform coding and/or encryption, perform calculations, and/or format data that is read from and/or data written to an optical storage medium 416. In some implementations, the signal processing and/or control circuit 412 and/or other circuits (not shown) in the DVD 410 can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

The DVD drive 410 may communicate with an output device (not shown) such as a computer, television or other device via one or more wired or wireless communication links 417. The DVD 410 may communicate with mass data storage 418 that stores data in a nonvolatile manner. The mass data storage 418 may include a hard disk drive (HDD). The HDD may have the configuration shown in FIG. 6A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The DVD 410 may be connected to memory 419 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage.

Referring now to FIG. 6C, the device can be implemented in one of more ADCs in a high definition television (HDTV) 420. The device may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. 6E at 422, a WLAN interface, mass data storage of the HDTV 420 and/or a power supply 423. The HDTV 420 receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display 426. In some implementations, signal processing circuit and/or control circuit 422 and/or other circuits (not shown) of the HDTV 420 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

The HDTV 420 may communicate with mass data storage 427 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices. At least one HDD may have the configuration shown in FIG. 6A and/or at least one DVD may have the configuration shown in FIG. 6B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The HDTV 420 may be connected to memory 428 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or

other suitable electronic data storage. The HDTV **420** also may support connections with a WLAN via a WLAN network interface **429**.

Referring now to FIG. **6D**, the device may implement and/or be implemented in one of more ADCs in a control system of a vehicle **430**, a WLAN interface, mass data storage of the vehicle control system and/or a power supply **433**. In some implementations, the device implement a powertrain control system **432** that receives inputs from one or more sensors such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals such as engine operating parameters, transmission operating parameters, and/or other control signals.

The device may also be implemented in other control systems **440** of the vehicle **430**. The control system **440** may likewise receive signals from input sensors **442** and/or output control signals to one or more output devices **444**. In some implementations, the control system **440** may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

The powertrain control system **432** may communicate with mass data storage **446** that stores data in a nonvolatile manner. The mass data storage **446** may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **6A** and/or at least one DVD may have the configuration shown in FIG. **6B**. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The powertrain control system **432** may be connected to memory **447** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The powertrain control system **432** also may support connections with a WLAN via a WLAN network interface **448**. The control system **440** may also include mass data storage, memory and/or a WLAN interface (all not shown).

Referring now to FIG. **6E**, the device can be implemented in one of more ADCs in a cellular phone **450** that may include a cellular antenna **451**. The device may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. **6E** at **452**, a WLAN interface, mass data storage of the cellular phone **450** and/or a power supply **453**. In some implementations, the cellular phone **450** includes a microphone **456**, an audio output **458** such as a speaker and/or audio output jack, a display **460** and/or an input device **462** such as a keypad, pointing device, voice actuation and/or other input device. The signal processing and/or control circuits **452** and/or other circuits (not shown) in the cellular phone **450** may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

The cellular phone **450** may communicate with mass data storage **464** that stores data in a nonvolatile manner such as optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **6A** and/or at least one DVD may have the configuration shown in FIG. **6B**. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The cellular phone **450** may be connected to memory **466** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The cellular

phone **450** also may support connections with a WLAN via a WLAN network interface **468**.

Referring now to FIG. **6F**, the device can be implemented in one of more ADCs in a set top box **480**. The device may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. **6F** at **484**, a WLAN interface, mass data storage of the set top box **480** and/or a power supply **483**. The set top box **480** receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display **488** such as a television and/or monitor and/or other video and/or audio output devices. The signal processing and/or control circuits **484** and/or other circuits (not shown) of the set top box **480** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

The set top box **480** may communicate with mass data storage **490** that stores data in a nonvolatile manner. The mass data storage **490** may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **6A** and/or at least one DVD may have the configuration shown in FIG. **6B**. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The set top box **480** may be connected to memory **494** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The set top box **480** also may support connections with a WLAN via a WLAN network interface **496**.

Referring now to FIG. **6G**, the device can be implemented in one of more ADCs in a media player **500**. The device may implement and/or be implemented in either or both signal processing and/or control circuits, which are generally identified in FIG. **6G** at **504**, a WLAN interface, mass data storage of the media player **500** and/or a power supply **503**. In some implementations, the media player **500** includes a display **507** and/or a user input **508** such as a keypad, touchpad and the like. In some implementations, the media player **500** may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via the display **507** and/or user input **508**. The media player **500** further includes an audio output **509** such as a speaker and/or audio output jack. The signal processing and/or control circuits **504** and/or other circuits (not shown) of the media player **500** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

The media player **500** may communicate with mass data storage **510** that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include optical and/or magnetic storage devices for example hard disk drives HDD and/or DVDs. At least one HDD may have the configuration shown in FIG. **6A** and/or at least one DVD may have the configuration shown in FIG. **6B**. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The media player **500** may be connected to memory **514** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The media player **500** also may support connections with a WLAN via a WLAN network interface **516**. Still other implementations in addition to those described above are contemplated.

7

Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification and the following claims.

What is claimed is:

1. An analog-to-digital converter comprising:
 - a first stage configured to
 - receive a first reference voltage and a first analog input voltage,
 - generate a first digital signal by quantizing the first analog input voltage, and
 - generate a first analog output voltage based on the first digital signal and the first analog input voltage; and
 - a second stage configured to
 - receive a second reference voltage and the first analog output voltage, wherein the second reference voltage is less than the first reference voltage,
 - generate a second digital signal by quantizing the first analog output voltage, and
 - generate a second analog output voltage based on the second digital signal and the first analog output voltage,
 wherein the first reference voltage is derived from an analog supply voltage, and
 - wherein the second reference voltage is derived from a digital supply voltage.
2. The analog-to-digital converter of claim 1, wherein:
 - the first stage comprises a first sample and hold circuit configured to sample and hold the first analog input voltage to generate a held analog input voltage; and
 - the second stage comprises a second sample and hold circuit configured to sample and hold the first analog output voltage to generate a held analog output voltage.
3. The analog-to-digital converter of claim 2, wherein:
 - the first analog output voltage is equal to a difference between the held analog input voltage and a first reconstructed analog signal, the first reconstructed analog signal being an analog representation of the first digital signal; and
 - the second analog output voltage is equal to a difference between the held analog output voltage and a second reconstructed analog signal, the second reconstructed analog signal being an analog representation of the second digital signal.
4. An integrated circuit comprising:
 - the analog-to-digital converter of claim 1;
 - a first voltage regulator configured to provide the analog supply voltage to the analog-to-digital converter; and
 - a second voltage regulator configured to provide the digital supply voltage to the analog-to-digital converter.
5. A device comprising the analog-to-digital converter of claim 1.
6. The device of claim 5, wherein the device comprises a battery powered device.

8

7. The device of claim 6, wherein the battery powered device comprises a laptop computer, a personal digital assistant, a cellular phone, or a digital audio player.

8. The device of claim 5, comprising a hard disk drive, a digital versatile disc drive, a high definition television, a vehicle, a set top box, or a media player.

9. A method for converting an analog signal to a digital signal, the method comprising:

receiving a first analog input voltage;

using a first reference voltage to generate a first digital signal by quantizing the first analog input voltage;

generating a first analog output voltage based on the first digital signal and the first analog input voltage;

generating a second reference voltage via a digital voltage supply; and

using the second reference voltage to generate a second digital signal by quantizing the first analog output voltage, wherein the second reference voltage is less than the first reference voltage.

10. The method of claim 9, further comprising generating a second analog output voltage based on the second digital signal and the first analog output voltage.

11. The method of claim 10, further comprising:

sampling and holding the first analog input voltage to generate a held analog input voltage; and

sampling and holding the first analog output voltage to generate a held analog output voltage.

12. The method of claim 11, wherein:

the first analog output voltage is equal to a difference between the held analog input voltage and a first reconstructed analog signal, the first reconstructed analog signal being an analog representation of the first digital signal; and

the second analog output voltage is equal to a difference between the held analog output voltage and a second reconstructed analog signal, the second reconstructed analog signal being an analog representation of the second digital signal.

13. A method for converting an analog signal to a digital signal, the method comprising:

receiving a first analog input voltage;

using a first reference voltage to generate a first digital signal by quantizing the first analog input voltage;

generating a first analog output voltage based on the first digital signal and the first analog input voltage;

using a second reference voltage to generate a second digital signal by quantizing the first analog output voltage;

generating a second analog output voltage based on the second digital signal and the first analog output voltage; and

using a third reference voltage to generate a third digital signal by quantizing the second analog output voltage, wherein the third reference voltage is less than the second reference voltage,

wherein the third reference voltage is a digital reference.

* * * * *