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(54) SYSTEM AND METHOD FOR CMOS IMAGE SENSING

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H01L 29/16	(2006.01)
H01L 31/12	(2006.01)
H01L 33/00	(2006.01)
H01L 29/161	(2006.01)
H01L 31/153	(2006.01)
H01L 29/735	(2006.01)
H01L 31/0328	(2006.01)
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H01L 31/109	(2006.01)
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(58) **Field of Classification Search** 257/83–84, 257/187, 290–292, 461–462, 464, E33.045, 257/E33.076, E33.077
See application file for complete search history.

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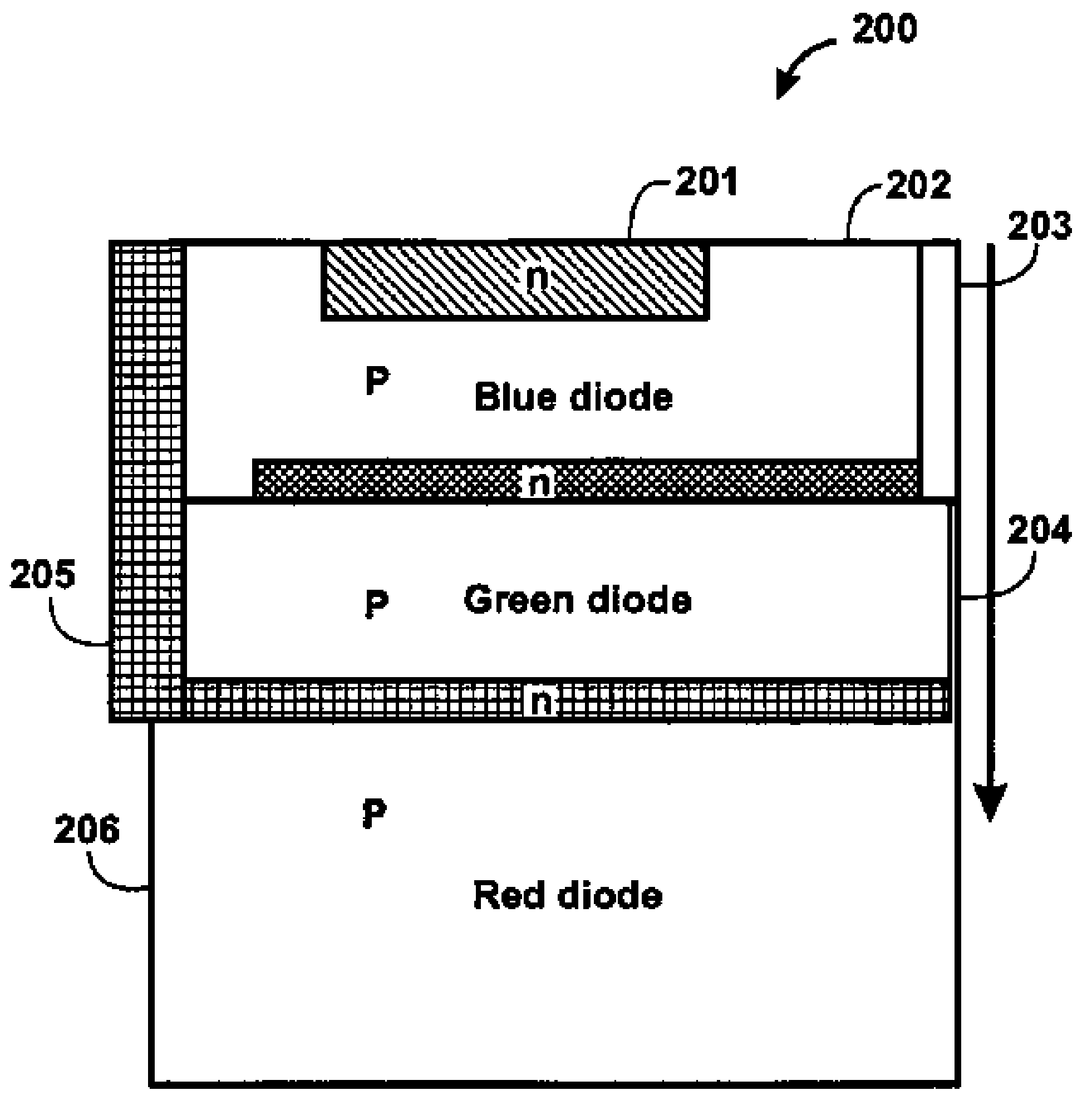
(57) ABSTRACT

A system and method for sensing image on CMOS. According to an embodiment, the present invention provide a CMOS image sensing pixel. The pixel includes an n-type substrate, which includes a first width and a first thickness. The pixel also includes a p-type epitaxy layer overlying the n-type substrate. The p-type epitaxy layer includes a second width and a second thickness. The second width is associated with one or more characteristics of a colored light. The pixel additionally includes an n-type layer overlying the p-type epitaxy layer. The n-type layer is associated with a third width and a third thickness. Additionally, the pixel includes an pn junction formed between the p-type epitaxy layer and the n-type layer. Moreover, the pixel includes a control circuit being coupled to the CMOS image sensing pixel.

19 Claims, 11 Drawing Sheets



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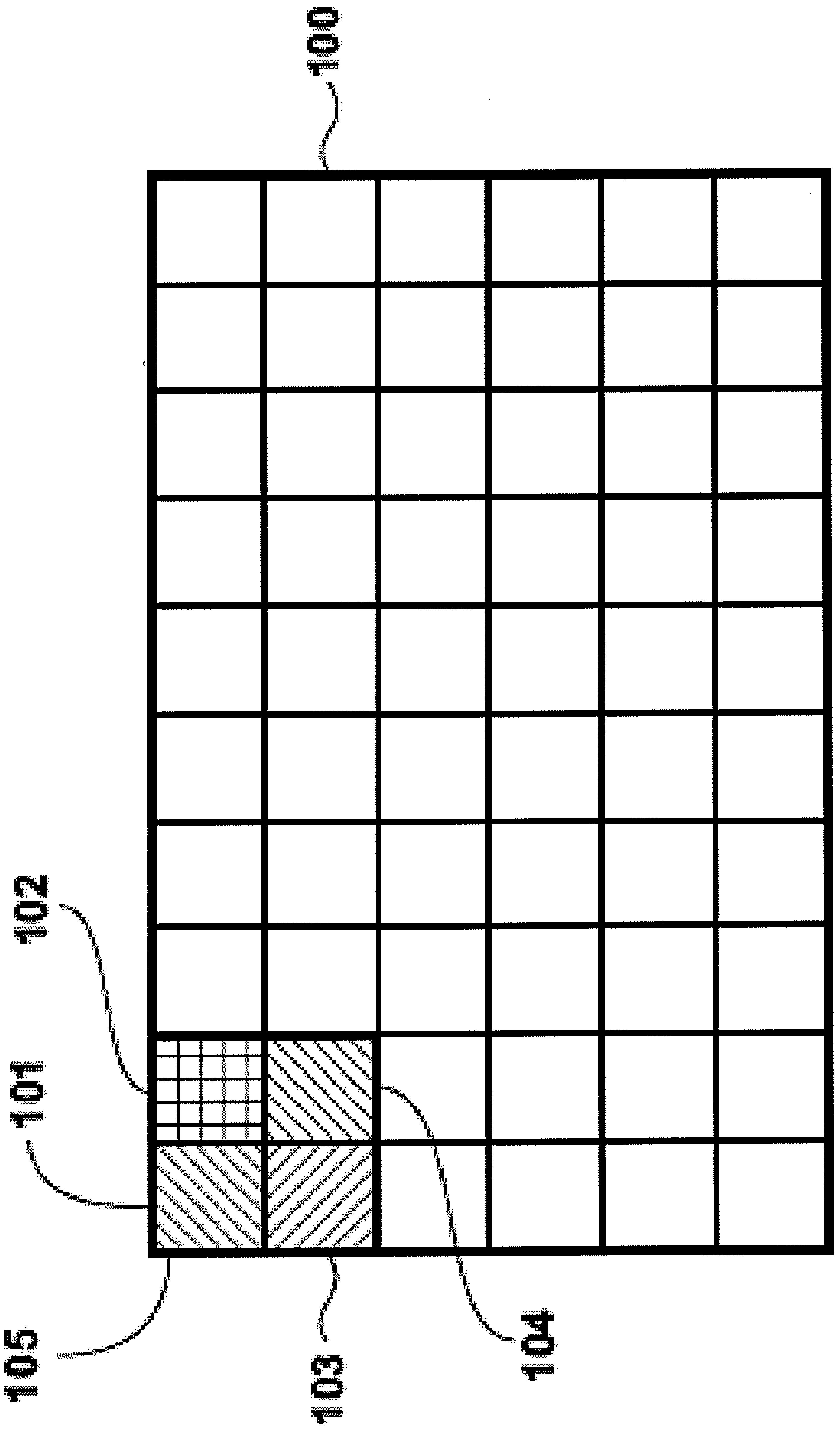

FIGURE 1
(Bayer Mask)

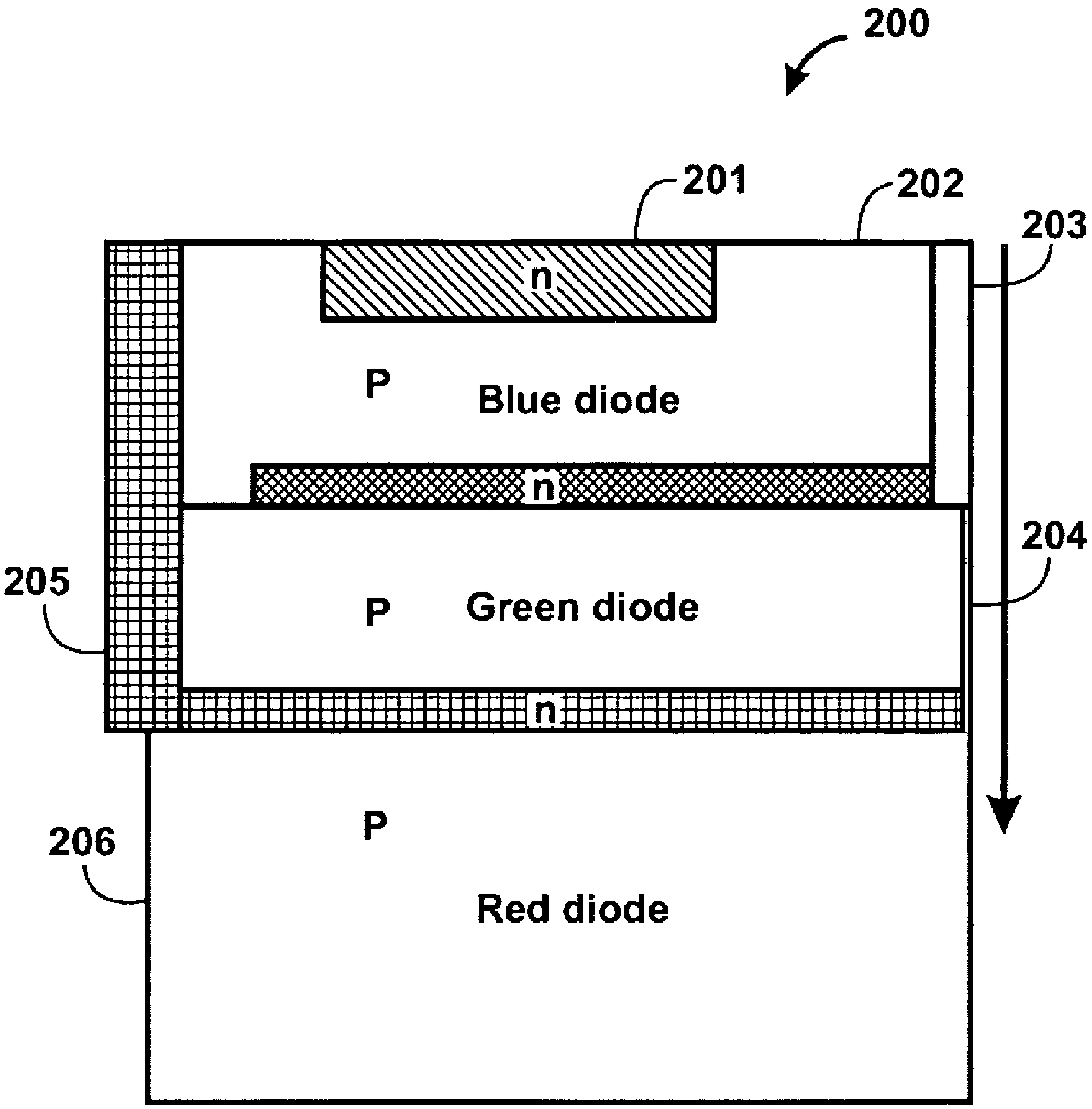
200
201
202
203
n
P
Blue diode
n
204
205
P
Green diode
n
P
206
Red diode

FIGURE 2A

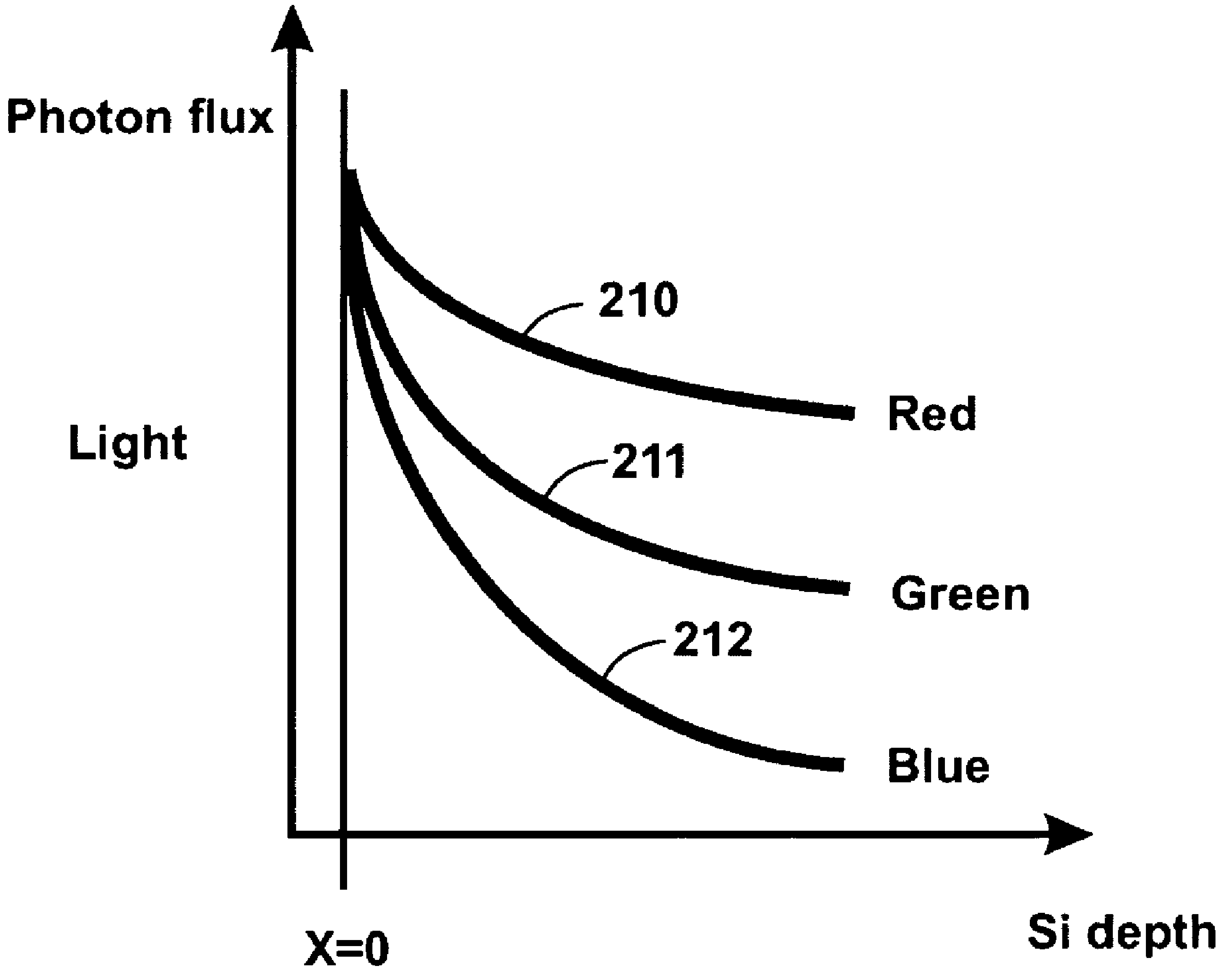

FIGURE 2B

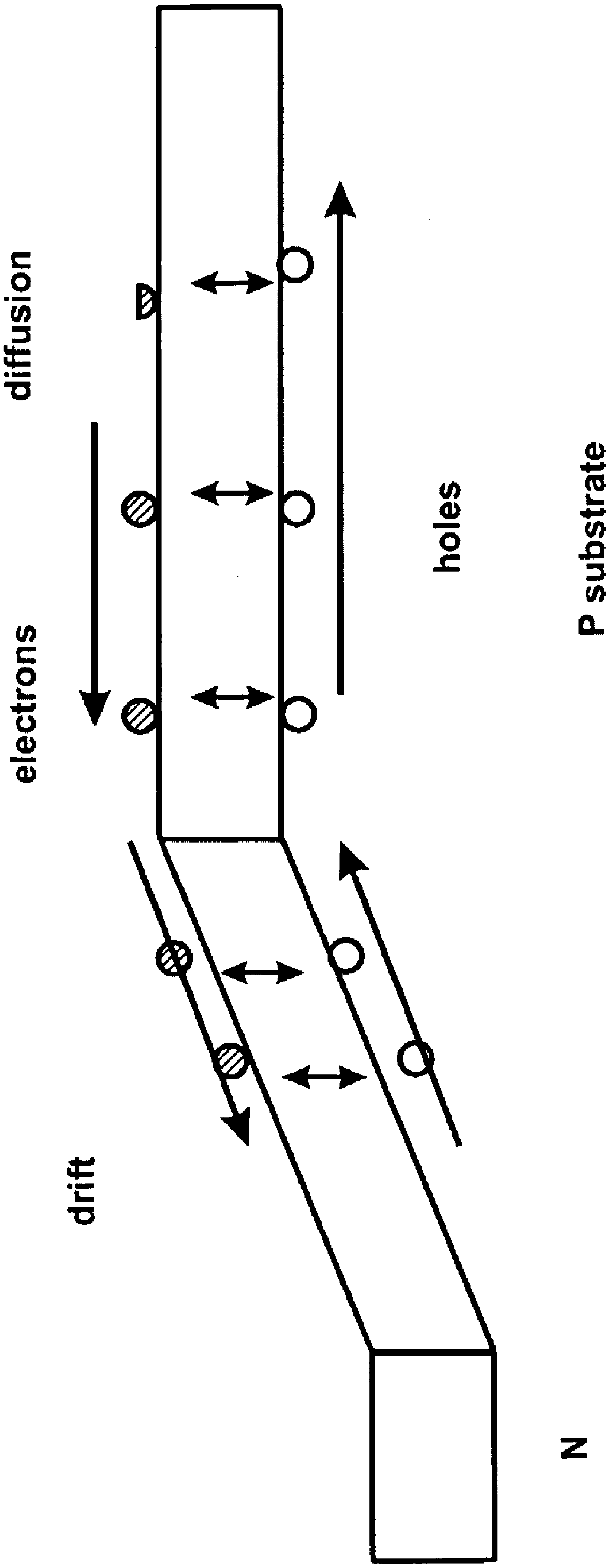

FIGURE 3

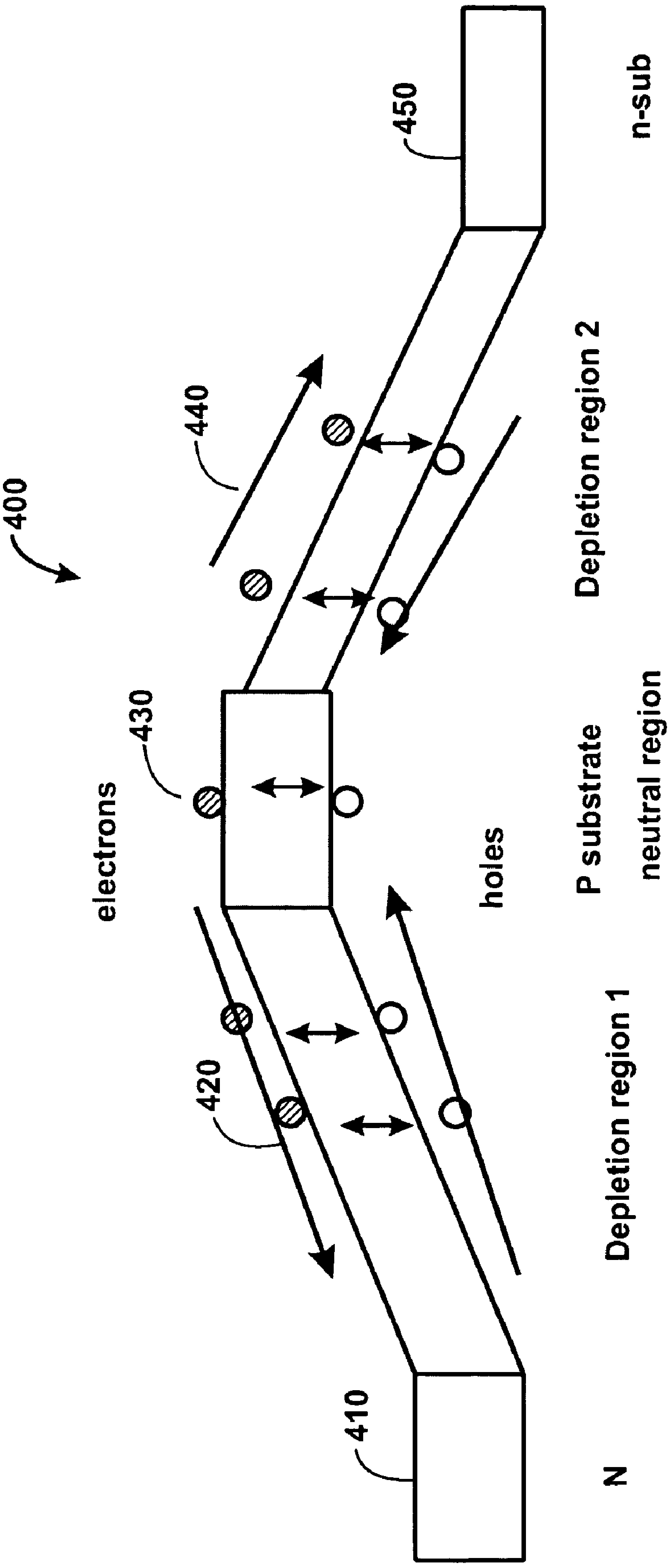
400
410
N
420
Depletion region 1
electrons
holes
430
P substrate
neutral region
440
Depletion region 2
450
n-sub

FIGURE 4

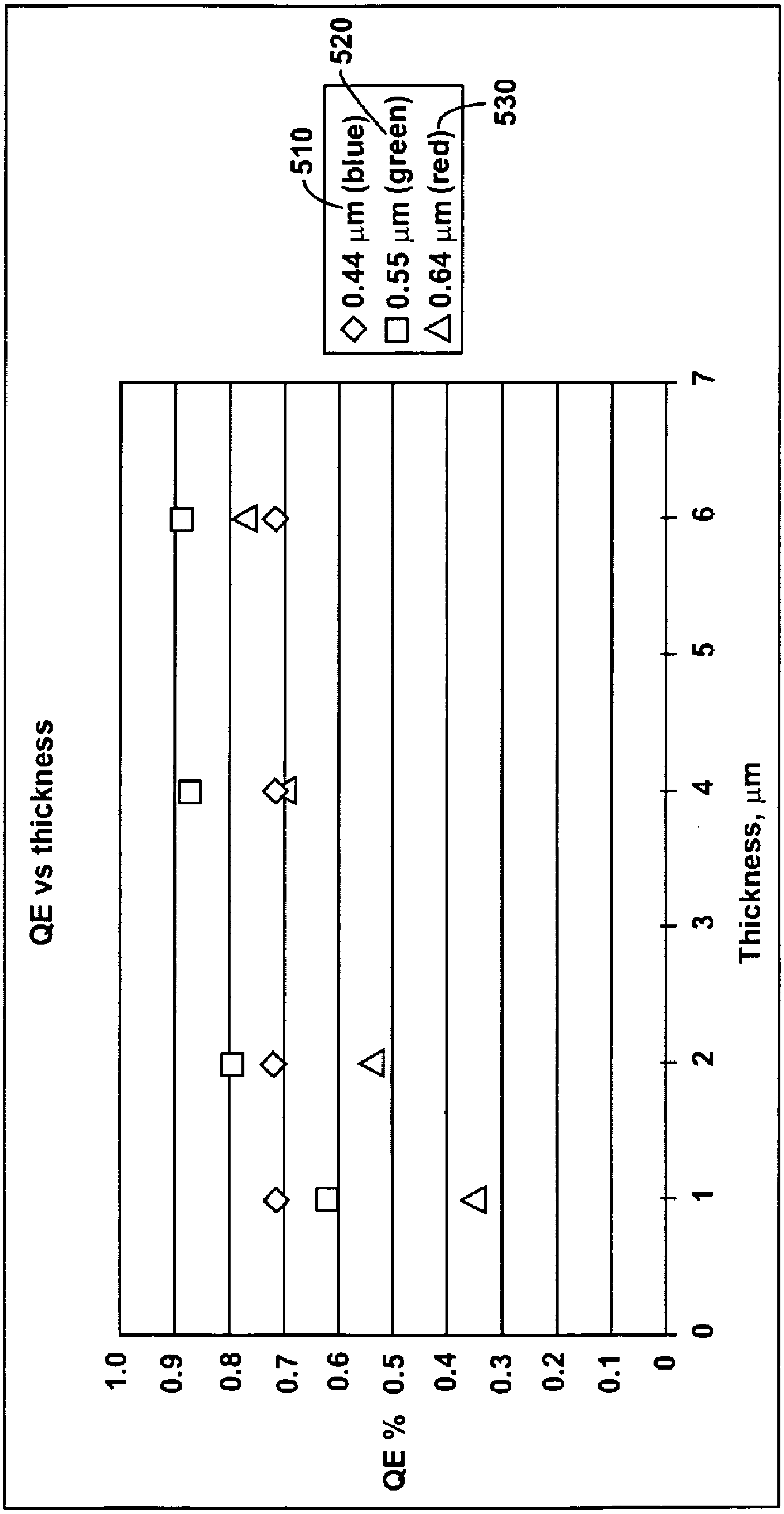
QE vs thickness
QE %
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
4
5
6
7
Thickness, µm
◇ 0.44 µm (blue)
□ 0.55 µm (green)
△ 0.64 µm (red)
510
520
530

FIGURE 5

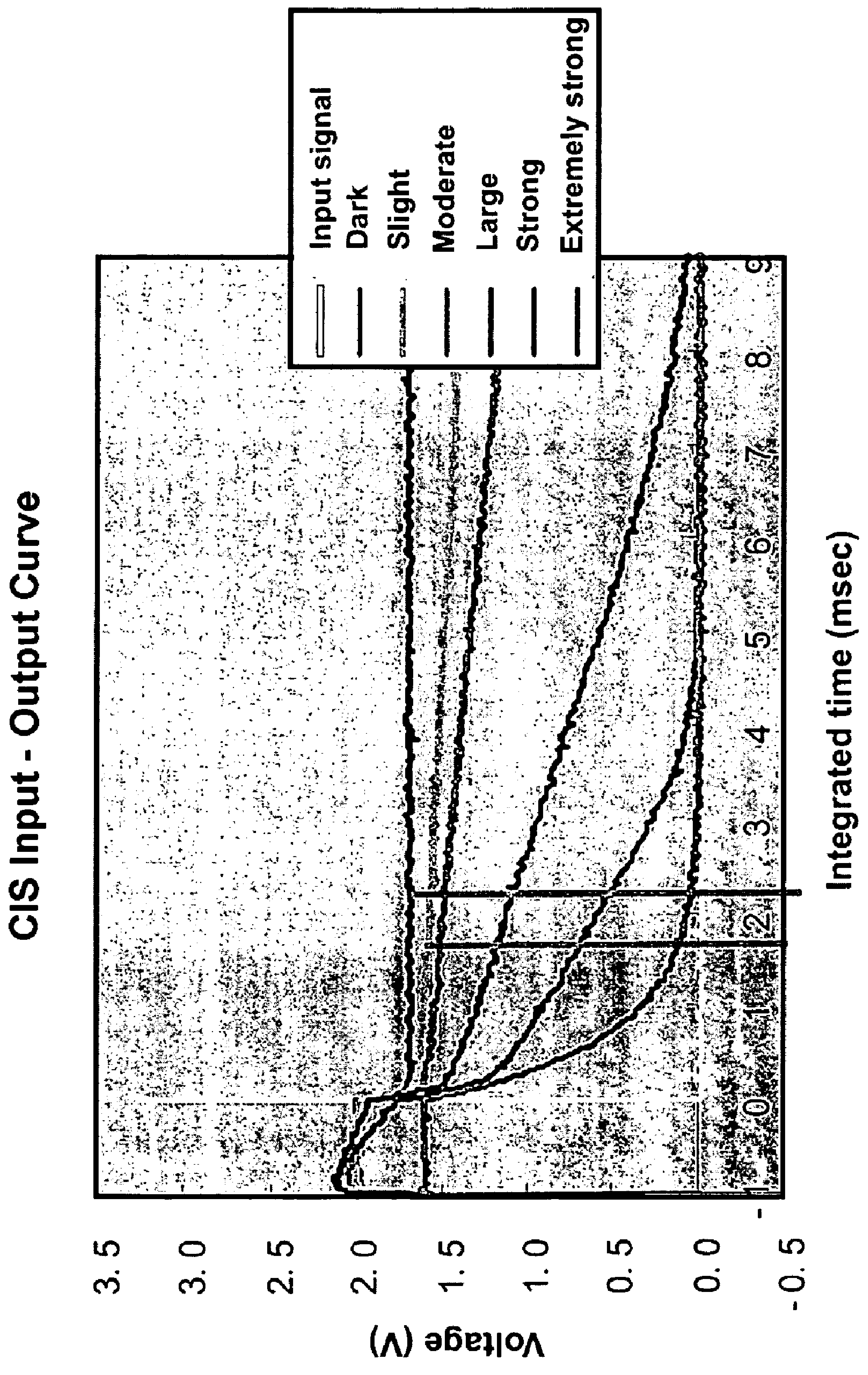
CIS Input - Output Curve
Input signal
Dark
Slight
Moderate
Large
Strong
Extremely strong
Voltage (V)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
Integrated time (msec)
-1
0
1
2
3
4
5
6
7
8
9

FIGURE 6

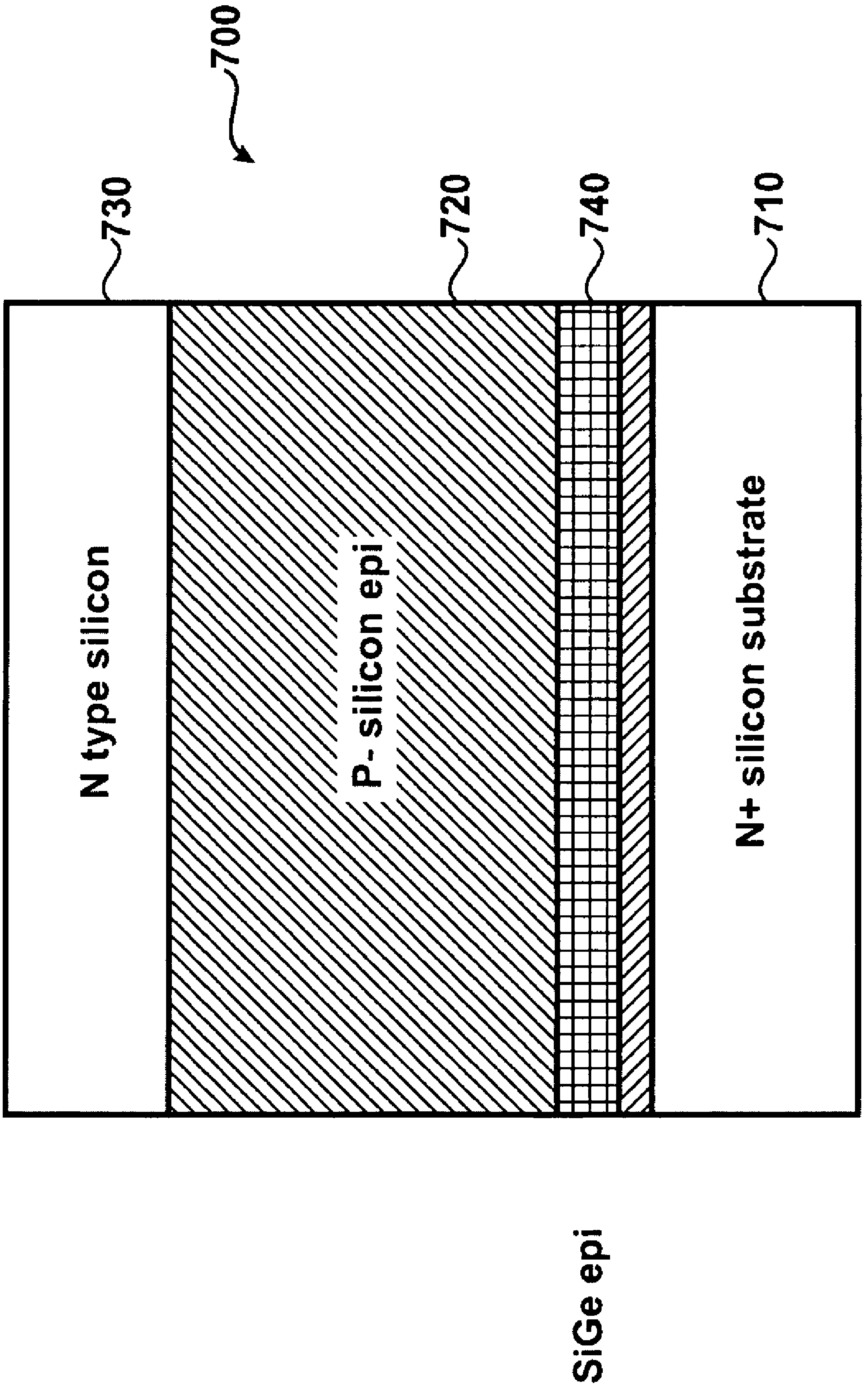
700
730
720
740
710
N type silicon
P- silicon epi
N+ silicon substrate
SiGe epi

FIGURE 7

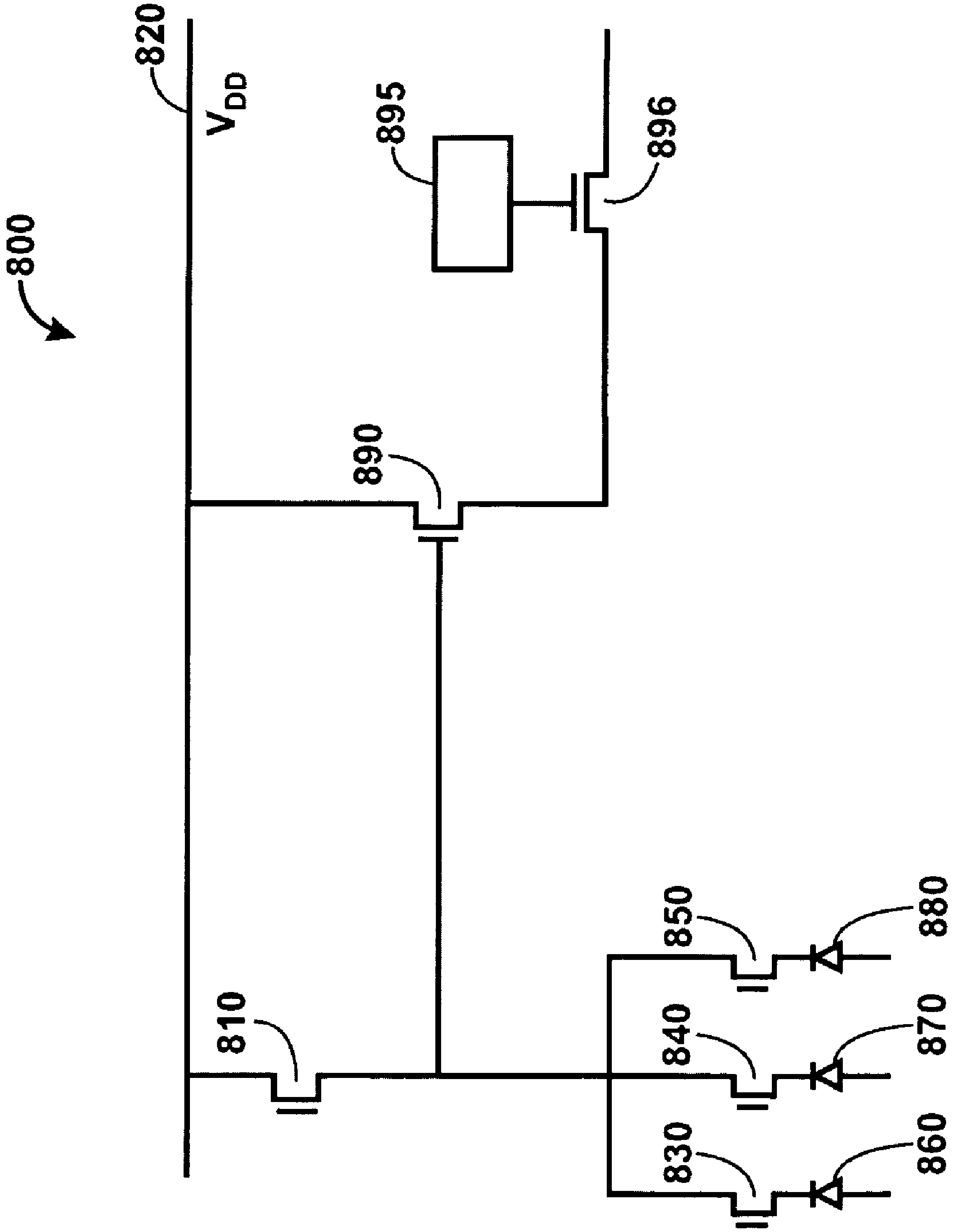

FIGURE 8

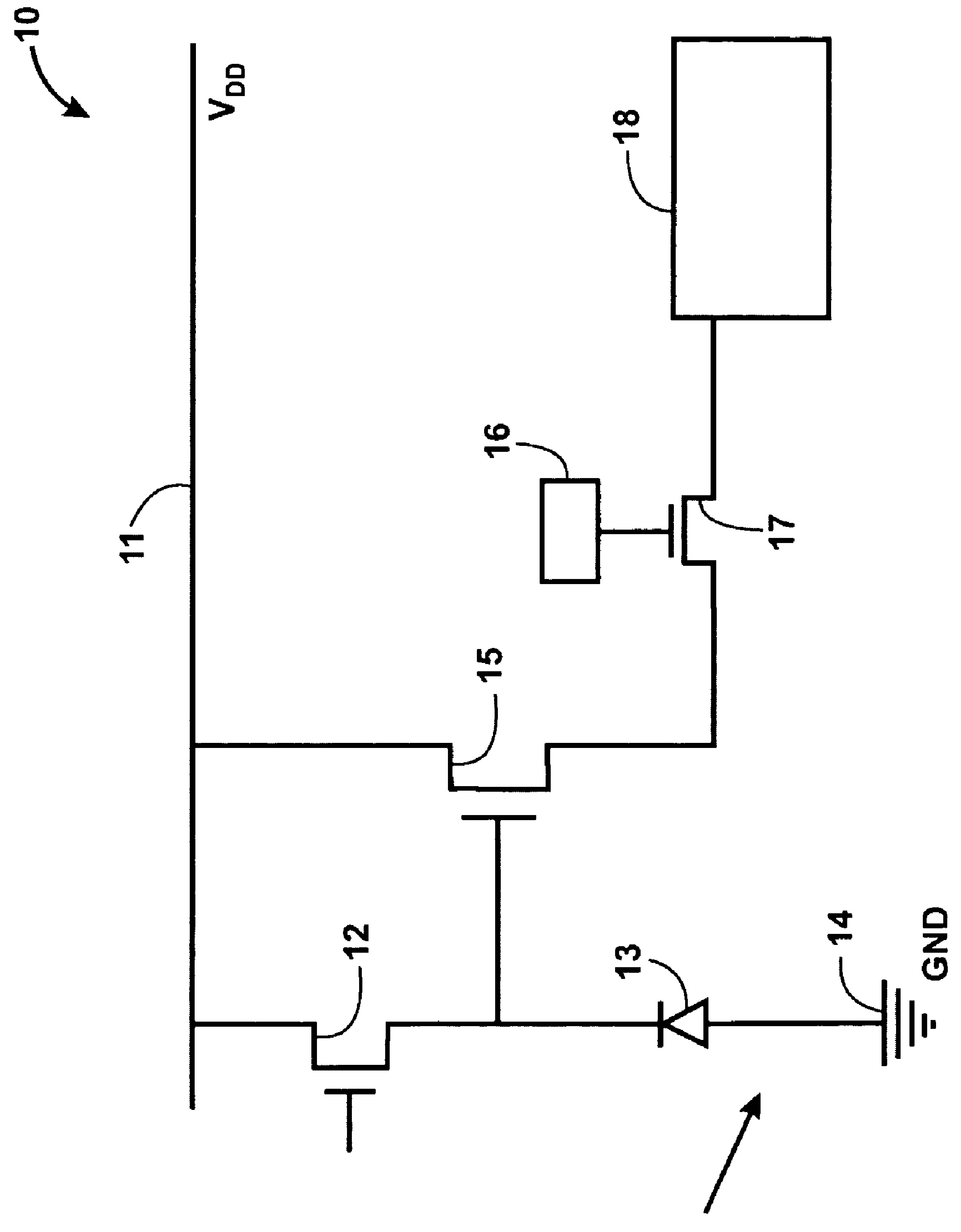

FIGURE 9

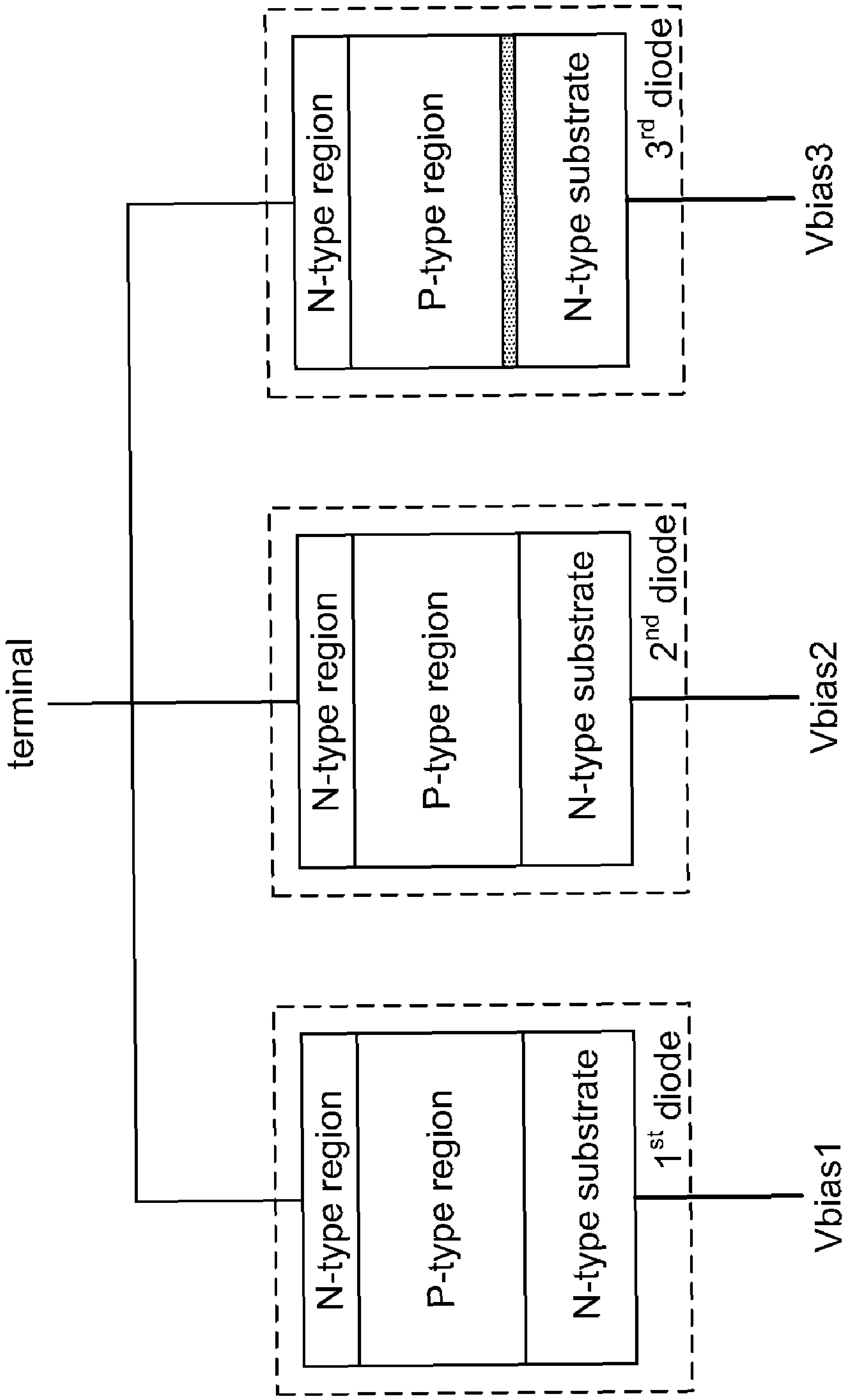
terminal
N-type region
P-type region
N-type substrate
3rd diode
Vbias3
N-type region
P-type region
N-type substrate
2nd diode
Vbias2
N-type region
P-type region
N-type substrate
1st diode
Vbias1

FIGURE 10

SYSTEM AND METHOD FOR CMOS IMAGE SENSING

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to Chinese Patent Application No. 200710094550, filed Dec. 13, 2007, commonly assigned and hereby incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

This invention is directed to imaging techniques. More particularly, the invention provides a method and system for capturing images on CMOS color sensors. Merely by way of example, the invention has been used to capture true color information on each pixel of an N-type substrate CMOS sensor. But it would be recognized that the invention has a much broader range of applicability.

To capture vivid imageries have been long been an endeavor that persisted as long as the human race itself. As early as the Stone Age, people tried to capture of what they see with cave drawings. Over the thousands of years, artists developed techniques for capture images with paint brushes and canvases. With oil paintings, artists have been able to capture real world images with accuracy, but the fidelity of paintings is no match to photography.

In 1826, a French inventor Nicéphore Niépce produced the first photographic image on polished pewter plate covered with a petroleum derivative. Since then, the technique for photographic imaging evolved. Better techniques and equipment improved image quality over the next hundred of years. Over the last fifty years, techniques for color photography improved and consummated. In the last decade, with the introduction of the first commercially available digital camera by Kodak in 1990, a new type of image capturing technique, digital imaging, has rapidly become a popular way for capturing images.

For digital imaging, the image sensor (or digital equivalent of film negatives) is one of the most important components for digital imaging devices, such as digital cameras, camera phones, etc. For a long time, image sensors have been based on charge-coupled device (CCD) technology that has been developed by George Smith and Willard Boyle at Bell Labs. In the past, CCD based imaging devices dominated. Recently, CMOS based image sensors have become more popular.

The CMOS image sensor technology typically includes millions of sensor pixels (light sensing units), each of the sensor pixel includes two to four transistors and a photodiode. Typically, conventional techniques for CMOS image sensing use one np junction, with very shallow p+ layer applied on top of N region to reduce noise and enhance blue response in image capturing process. In a way, the CMOS sensor unit **10** works in a similar manner as a capacitor. The more charge stored in the electrode, the higher the voltage drop across the depletion region of the CMOS. Light, which is a energy source, generates free carriers. The free carriers under electric field run towards the N type region of the CMOS sensor and neutralized the charge and reduce potential. The voltage difference before and after the integration of energy provides a signal level. The signal level is then used as a reading as the amount of light being detected and used for forming an image.

Depending upon applications, CMOS sensor often have advantages over CCD sensors. For example, compared to CCD image sensors, CMOS sensors usually provide lower

costs and longer battery life. As a result, CMOS is often preferred for portable imaging devices such as camera phone and point and shoot cameras. At the high end, CCD image sensors are often behind CMOS images sensors in terms of noise level and sensitivity. Because of various advantages of CMOS image sensors, the technologies for CMOS image sensors have been rapidly developing. The resolution of CMOS image sensor has been increasing as pixel size shrink together with the MOS transistor channel length. While the increase resolution of image sensors often improve image resolution, the decreased pixel size and increase noise level have become obstacles for improved image quality. Various techniques, such as improvements on structure and circuitry, have been developed to improve performance at level. For example, various systems and methods have been developed to provide color separation. In the past, three major approaches have been used to provide color separation: color filter, stack junction photo diode, and junction separation. Unfortunately, the abovementioned techniques for image sensing and color separation are often inadequate. These and other limitations of the conventional techniques have been overcome, at least in part, by the invention that has been fully described below.

Therefore, it is desirable to have an improved method and system for a CMOS image sensing device.

BRIEF SUMMARY OF THE INVENTION

This invention is directed to imaging techniques. More particularly, the invention provides a method and system for capturing images on CMOS color sensors. Merely by way of example, the invention has been used to capture true color information on each pixel of an N-type substrate CMOS sensor. But it would be recognized that the invention has a much broader range of applicability.

According to an embodiment, the present invention provide a CMOS image sensing pixel. The pixel includes an n-type substrate, which includes a first width and a first thickness. The pixel also includes a p-type epitaxy layer overlying the n-type substrate. The p-type epitaxy layer includes a second width and a second thickness. The second width is associated with one or more characteristics of a colored light. The pixel additionally includes an n-type layer overlying the p-type epitaxy layer. The n-type layer is associated with a third width and a third thickness. Additionally, the pixel includes a pn junction formed between the p-type epitaxy layer and the n-type layer. Moreover, the pixel includes a control circuit being coupled to the CMOS image sensing pixel.

According to another embodiment, the present invention provides a method for determining color using a CMOS image sensor. The CMOS image sensor includes an n-type substrate and a p-type layer, the p-type layer overlaying the n-type substrate. The method includes a step for applying a first voltage on the n-type substrate. The method also includes a step for obtaining a first output, which is associated with the first voltage. The method additionally includes a step for applying a second voltage on the n-type substrate. Additionally, the method includes a step for obtaining a second output, which is associated with the first voltage. In addition, the method includes a step for applying a third voltage on the n-type substrate. The method additionally includes a step for obtaining a third output, which is associated with the first voltage. The method also includes a step for providing a plurality of weighting factors. The method includes determining a color based on the plurality of weighting factors, the first output, the second output, and the third output.

According to an alternative embodiment, the present invention provides a method for forming a CMOS image sensing pixel, which is configured for determining a color. The method includes a step for providing an n-type substrate that includes a first thickness and a first width. The method also includes a step for forming a p-type layer, the p-type layer overlaying the n-type substrate. The p-type layer includes a second thickness and a second width. The second thickness and the second width are associated with a light characteristic. The method additionally includes a step for forming an n-type layer, the n-type layer overlaying the p-type layer. The n-type layer includes a third thickness and a third width. In addition, the method includes a step for forming a pn junction between the p-type layer and the n-type layer. The pn junction includes a fourth width. The method also includes a step for providing a control circuit. The control circuit is electrically coupled to the n-type substrate.

According to yet another embodiment, the present invention provides an imaging capturing device. The image capturing devices includes a user interface being configured to facilitate an image capturing process. The image capture device also includes a first input being configured to receive a user input. The user input is a command for capturing an image. The image capturing device additionally includes an image sensor being configured to capture an image. Additionally, the image capturing device includes an optical device being positioned to provide a light to form an image on the image sensor. The image capturing device further includes a processor being configured to process images. The image sensor includes an n-type substrate, which includes a first width and a first thickness. The image sensor also includes a p-type layer overlying the n-type substrate. The p-type layer includes a second width and a second thickness. The second width is associated with one or more characteristics of a colored light. The image sensor also includes an n-type layer overlying the p-type layer. The n-type layer is associated with a third width and a third thickness. The image sensor further includes a pn junction formed between the p-type layer and the n-type layer.

It is to be appreciated that the present invention provides various advantages over conventional technologies. As compared to color filter techniques. The present invention provides a method and system for capturing images with true color and pixels. Compared to stacked junction techniques, the present invention is more cost effective and offers better imaging capability. For example, the present invention allows costs savings from the color filtering process and minimum circuit design. According to an embodiment, only three transistors are needed for implement an imaging pixel.

Depending upon embodiment, one or more of these benefits may be achieved. These benefits and various additional objects, features and advantages of the present invention can be fully appreciated with reference to the detailed description and accompanying drawings that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a Bayer pattern mask filter used to produce color for an image sensor.

FIG. **2**A is a simplified diagram illustrating a conventional image sensor implemented with stack junction technology.

FIG. **2**B is a graph illustrating the absorption coefficient associated with color.

FIG. **3** is a simplified diagram illustrating the diffusion principle utilized in conventional CMOS image sensors.

FIG. **4** is a simplified diagram illustrating a working principle of a CMOS image sensor according to an embodiment of the present invention.

FIG. **5** is a simplified diagram illustrating the relationship between quantum efficiency and thickness according to an embodiment of the present invention.

FIG. **6** is a simplified diagram illustrating the relationship between voltage level and integration time according to an embodiment of the present invention.

FIG. **7** is a simplified diagram illustrating an image sensor according to an embodiment of the present invention.

FIG. **8** is a simplified diagram illustrating an image sensor circuit according to an embodiment of the present invention.

FIG. **9** is a simplified diagram illustrating an image sensor circuit according to an embodiment of the present invention.

FIG. **10** is a simplified diagram illustrating an image sensing pixel device having a first photodiode, a second photodiode, and a third photodiode according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

This invention is directed to imaging techniques. More particularly, the invention provides a method and system for capturing images on CMOS color sensors. Merely by way of example, the invention has been used to capture true color information on each pixel of an N-type substrate CMOS sensor. But it would be recognized that the invention has a much broader range of applicability.

As discussed above, various techniques have been developed to provide color separation for CMOS based image sensors. Conventional techniques involved using color filter, stack junction photo diode, and junction separation. However, convention techniques are often inadequate.

Separating color using color filter has been a popular technique. This technique is based on the concept of additive properties of three primary colors red, green and blue (RGB). When the three primary colors combine, they are capable of producing any other colors. To use color filter technique, a color filter is used to produce colors. FIG. **1** illustrates a Bayer pattern mask filter used to produce color for an image sensor. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The Bayer mask **100** is divided into many pixels to allow light with certain wavelength to pass down to specific pixel. For example, a group **105** of four pixel filters includes three color filters arranged into a square, which includes a red filter **101**, a green filter **102**, a blue filter **103**, and a red filter **104**. Each underlying pixel under the color filters essentially captures only the light level associated with that particular color. The final image that is eventually formed is the result of calculation and interpolation of value of the pixel and its surround pixels. For example, the red signal from the pixel underlying the red filter **101** is the average of surrounding green pixels. However, sine the color of each pixel is a result of calculation and interpolation instead of actual color that is directed to the particular pixel, the true color value for that pixel is not obtained. As a result, the color of a captured image may be off, and sometimes the filtering and interpolations produce undesirable artifacts.

To produce "true" color on each pixel, other color separation techniques have been developed. For example, stack junction technology is sometimes used to provide color separation. FIG. **2**A is a simplified diagram illustrating conventional a image sensor implemented with stack junction technology. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The stack junction image sensor **200** includes three color layers. A blue diode **202** overlays a green diode **204**, which overlays a red diode **206**. Each diode is underneath an n-type region so that pn junctions are formed. During an image sensing and color separation process, photon or light passes through the blue diode **202** first, the green diode **204** next, and finally the red diode **206**.

The structure of the stack junction image sensor **200** is relatively more complex compared that of images sensors using color filtering. Consequently, it is often more expensive and difficult to produce stack junction image sensors. For example, the manufacturing of stack junction image sensor requires additionally epitaxy processes to form color layers and additionally structures to make connection and isolation. In addition, stack junction image sensors are often vulnerable to noise due to limited junction capacitance. For example, junction expansion along in silicon junction has little effect in changing the collecting efficiency since the life-time of minority carrier is usually long in silicon.

The principle of stack junction technology is based on the absorption decays associated with silicon depth governed by absorption coefficient. The higher the absorption coefficient, the faster it decays. For example, blue photons are associated with higher absorption coefficient and therefore decays faster than green and red photos. FIG. **2**B is a graph illustrating the absorption coefficient associated with color. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As show in FIG. **2**B, the blue photon flux curve **212** drops the most as the silicon depth increases. And since green has an absorption coefficient that is between absorption coefficients of blue and red, the green photon flux curve **211** is between the blue photon flux curve **212** and the red photon flux curve **210**.

As analyzed above, conventional techniques for image sensing are often inadequate. Therefore, it is desirable to have an improved color separation scheme.

It is to be appreciated that the present invention utilizes a novel operating principle as compared to conventional technologies. For example, conventional CMOS sensor is implemented with the diffusion principle. FIG. **3** is a simplified diagram illustrating the diffusion principle utilized in conventional CMOS image sensors. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As illustrated according to FIG. **3**, photodiode used in CMOS image sensor a np junction is formed and electrons are collected by electric field and diffusion. However, silicon is a usually associated with poor photon absorption characteristics. As a result, most carriers are generated far deeper in the depletion region, especially the red light.

In contrast, the present invention operates, among other things, under a different principle. FIG. **4** is a simplified diagram illustrating a working principle of a CMOS image sensor according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. According to an embodiment, the present invention utilizes two depletion regions **420** and **440** as illustrated in FIG. **4**. An image sensor **400** includes an n-type region **410**, a depletion region **420**, a p substrate neutral region **430**, a depletion region **440**, and a n-type substrate **450**. As compared to the conventional techniques, an np junction between the n-type region **410** and the p substrate neutral region **430** is formed. For the image sensor **400** to work properly, the reverse bias of the n-type substrate **450** to the p substrate neutral region **430** can be changed to adjust the width of the depletion region **440**. When the n-type substrate **450** is reverse biased, photon-generated carriers beyond the p substrate neutral region **430** can not be collected by the photodiode in the front, therefore, contribute no extra voltage. By changing the width of the depletion region **440**, the quantum efficiency of red or green light can be adjusted, since they are absorbed deeper in the silicon toward the n-type substrate **450**.

FIG. **5** is a simplified diagram illustrating the relationship between quantum efficiency and thickness according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As illustrated in FIG. **5**, green usually carries the highest quantum efficient, while red generally carries the lowest quantum efficiency. In addition, quantum efficiency is directly proportional to the thickness. For example, the quantum efficiency increases as the thickness increases.

FIG. **6** is a simplified diagram illustrating the relationship between voltage level and integration time according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications.

FIG. **7** is a simplified diagram illustrating an image sensor according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The image sensor **700** includes a n-type substrate **710** at the bottom. For example, the n-type substrate is made of silicon. On top of the n-type substrate **710** overlays a p-type epitaxy layer **720**. According to an embodiment, the p-type epitaxy layer **720** is formed with adjustable doping concentration and thickness. As an example, the p-type epitaxy layer **720** consists of p-type silicon. For example, the p-type epitaxy layer **720** has a thickness ranging from 2 um to 7 um. On top of the p-type epitaxy layer **720** overlays an n-type layer **230** to so that a pn junction between the p-type epitaxy layer **720** and the n-type layer **230** is formed. For example, the n-type layer **230** has a thickness of less than 0.5 um. According to certain embodiments, an epitaxy layer **740** is formed between the n-type substrate **710** and the p-type epitaxy layer **720**. For example, the epitaxy layer **740** consists of silicon germanium material. Depending upon application, the silicon germanium material is used to enhance the red light absorption. For example, because the absorption coefficient of silicon for red light is poor, and sometimes implantation of thick p-type epitaxy device could lead to high voltage, the silicon germanium material is added to boost photon absorption. As merely an example, a silicon germanium epitaxy layer has a thickness ranges from 0.1 um to 1 um depending on germanium concentration.

According to an embodiment, the present invention applies different bias voltages on the n-type substrate **710** to obtain different colors. Bias voltages are based on the light absorption properties of RGB color as explained above. According to an embodiment, high bias voltage is used for blue light, medium bias voltage is used for blue and green light, and zero voltage bias voltage is used for blue, green, and red light.

The operation of an embodiment of the present invention may be describe in three steps. At the first step, the p-type epitaxy layer **720** region is short. As a result, the only carriers collected are those generated in deletion region formed between the p-type epitaxy layer **720** and the n-type layer **730**. During the first step, the voltage response from the image sensor is primarily due to the blue light. The voltage response at the first step may be expressed according to the following equation.

$$\Delta V\text{response}=B\Delta Vb+g1\Delta Vg+r1\Delta Vr \qquad \text{(Equation 1)}$$

According to Equation 1, B is the weighting factor for blue color. The term ΔVb represents the response due to the blue color. The term g1ΔVg represents the voltage response due to green color. The term r1ΔVr represents the voltage response due to red color.

In the second step, a bias voltage that is associated with green color is applied. The voltage response at the first step may be expressed according to the following equation.

$$\Delta V\text{response}=B\Delta Vb+b2\Delta Vb1+G\Delta Vg+g1\Delta Vg+(r1+r2)\Delta Vr \qquad \text{(Equation 2)}$$

According to Equation 2, B is the weighting factor for blue color. G is the weighting factor for green color. The term BΔVb represents the response due to the blue color. The term GΔVg represents the response due to the green color. The term g2ΔVg represents the voltage response due to green color. The term r2ΔVr represents the voltage response due to red color. It is noted that green color at the second step contributes greatly to the voltage response. Furthermore, the voltage response for the green color may be obtained by subtracting the Equation 2 from Equation 1.

In the third step, a bias voltage that is associated with red color is applied. For example, the bias voltage for red color is zero. The voltage response at the first step may be expressed according to the following equation.

$$\Delta V\text{response}=B\Delta Vb+b3\Delta Vb1+G\Delta Vg+(g1+g3)\Delta Vg+(r1+r2)\Delta Vr+R\Delta Vr \qquad \text{(Equation 3)}$$

According to Equation 2, B is the weighting factor for blue color. G is the weighting factor for green color. R is the weighting factor for red color. The term BΔVb represents the response due to the blue color. The term GΔVg represents the response due to the green color. The term RΔVr represents the response due to the red color. The term g2ΔVg represents the voltage response due to green color. The term r2ΔVr represents the voltage response due to red color. It is noted that green color at the second step contributes greatly to the voltage response. Furthermore, the voltage response for the green color may be obtained by subtracting the Equation 3 from Equation 2.

It is to be appreciated that the weighting factors B, G, R can be determined and calibrated for specific image sensors. According to various embodiments, the present invention provide color separation schemes with fixed photodiode depletion, which could simplify the circuit design and process. FIG. **8** is a simplified diagram illustrating an image sensor circuit according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As illustrated according to FIG. **8**, three transistors **830**, **840**, and **850** are used for blue, green, and red color based on voltage.

FIG. **9** is a simplified diagram illustrating an image sensor circuit according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. The CMOS sensor unit **10** includes a photo detector **13**, a source follow transistor **15**, a row select transistor **16**, and a CMOS circuit **18**. As merely an example, the transistors in the CMOS sensor unit **10** control the on and off states to read light signal at proper time. According to an embodiment, typical operation involves three steps, each step is for capture an individual color: blue, green, or red. The back side is a reverse biased pn junction. When doing blue light absorption, a high voltage is used, so that red and green photons will not be collected. When doing green light absorption, a reduced bias is used and green photons will be added to the response. Finally, all the back side bias is removed to collect all. As merely an example, the back side bias is synchronized with the mainly circuit signal process timing.

According to an embodiment, the present invention provides a CMOS image sensing pixel. The pixel includes an n-type substrate, which includes a first width and a first thickness. The pixel also includes a p-type epitaxy layer overlying the n-type substrate. The p-type epitaxy layer includes a second width and a second thickness. The second width is associated with one or more characteristics of a colored light. The pixel additionally includes an n-type layer overlying the p-type epitaxy layer. The n-type layer is associated with a third width and a third thickness. Additionally, the pixel includes an pn junction formed between the p-type epitaxy layer and the n-type layer. Moreover, the pixel includes a control circuit being coupled to the CMOS image sensing pixel.

According to another embodiment, the present invention provides a method for determining color using a CMOS image sensor. The CMOS image sensor includes an n-type substrate and a p-type layer, the p-type layer overlaying the n-type substrate. The method includes a step for applying a first voltage on the n-type substrate. The method also includes a step for obtaining a first output, which is associated with the first voltage. The method additionally includes a step for applying a second voltage on the n-type substrate. Additionally, the method includes a step for obtaining a second output, which is associated with the first voltage. In addition, the method includes a step for applying a third voltage on the n-type substrate. The method additionally includes a step for obtaining a third output, which is associated with the first voltage. The method also includes a step for providing a plurality of weighting factors. The method includes determining a color based on the plurality of weighting factors, the first output, the second output, and the third output. For example, the embodiment is illustrated according to FIG. **7**.

According to an alternative embodiment, the present invention provides a method for forming a CMOS image sensing pixel, which is configured for determining a color. The method includes a step for providing an n-type substrate that includes a first thickness and a first width. The method also includes a step for forming a p-type layer, the p-type layer overlaying the n-type substrate. The p-type layer includes a second thickness and a second width. The second thickness and the second width are associated with a light characteristic. The method additionally includes a step for forming an n-type layer, the n-type layer overlaying the p-type layer. The n-type layer includes a third thickness and a third width. In addition, the method includes a step for forming a pn junction between the p-type layer and the n-type layer. The pn junction includes a fourth width. The method also includes a step for providing a control circuit. The control circuit is electrically coupled to the n-type substrate. For example, the embodiment is illustrated according to FIG. **7**.

According to yet another embodiment, the present invention provides an imaging capturing device. The image capturing devices includes a user interface being configured to facilitate an image capturing process. The image capture device also includes a first input being configured to receive a user input. The user input is a command for capturing an image. The image capturing device additionally includes an image sensor being configured to capture an image. Additionally, the image capturing device includes an optical device being positioned to provide a light to form an image on the image sensor. The image capturing device further includes a processor being configured to process images. The image sensor includes an n-type substrate, which includes a first width and a first thickness. The image sensor also includes a p-type layer overlying the n-type substrate. The p-type layer includes a second width and a second thickness. The second width is associated with one or more characteristics of a colored light. The image sensor also includes an n-type layer overlying the p-type layer. The n-type layer is associated with a third width and a third thickness. The image sensor further includes an pn junction formed between the p-type layer and the n-type layer. For example, the embodiment is illustrated according to FIG. **7**.

It is to be appreciated that the present invention offers an improvement over both the color filtering technique and stack junction techniques in many ways. For example, integrating color separation capability into one pixel has great advantage over using several pixels with color filter. Capturing true color with each individual pixel has better color resolution and result in better image quality. Thus stack junction technique often provide better image quality. However, to accomplish this resolution, the stack junction technique usually sacrifice area and cost. Typically, the stack junction technique requires three more transistors to individually control blue, green and red photodiode. Such hardware requirement diminishes the ability to shrink the pixel size compared to the conventional three transistor design. For example, the connecting plugs and contacts for green and red diode occupy valuable pixel area. As a result, pixel becomes difficult to shrink beyond certain size. Moreover, the extra two epitaxy layers not only add cost, but also bring difficulty to control yield and uniformity during the manufacturing process. More transistors make the circuitry even more difficult to design and process. For example, the embodiment is illustrated according to FIGS. **7** and **9**.

Among other things, the present invention provides a better color separation capability and lower noise level in the image capturing process. Often, the color separation capability is intrinsic characteristic associated with long diffusion length. Generally, diode quantum efficiency has very little dependency on the depletion width.

Noise level is often associated with junction capacitance. For example, junction capacitance is inversely related to the reverse bias voltage. Usually, the capacitance is described according to the following equation:

$$V=1/C^2 \qquad \text{(Equation 4)}$$

As illustration by Equation 4, small capacitance leads to large ΔV since $\Delta V=\Delta Q/C$. Even with fixed noise level ΔQ, AV will be larger. Typically ΔQ increases as the reverse bias increases.

The present invention provides improved and better solution in terms of color separation capability and lower noise level. The reversed biased depletion region between the n-type substrate and the p-type layer acts as a valve that controls the photon generated carriers flowing into the active pixel region. For example, the present invention allows changing the photodiode quantum efficiency significantly by shrinking or expanding the width of the p-type layer. According to various embodiments, the present invention does not require adjusting bias voltage of the active pixel or the capacitance change. As a result, noise level can be kept constant.

It is understood the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

What is claimed is:

1. A CMOS image sensing pixel comprising:

an n-type substrate, the n-type substrate including a first width and a first thickness;

a p-type epitaxy layer overlying the n-type substrate, the p-type epitaxy layer including a second width and a second thickness, the second width including an adjustable depletion region between the n-type substrate and the p-type epitaxy layer, the adjustable depletion region being associated with one or more characteristics of a colored light;

an n-type layer overlying the p-type epitaxy layer, the n-type layer being associated with a third width and a third thickness;

a pn junction formed between the p-type epitaxy layer and the n-type layer; and

a control circuit being coupled to the CMOS image sensing pixel.

2. The CMOS image sensing pixel of claim **1** wherein the p-type epitaxy layer includes a silicon material.

3. The CMOS image sensing pixel of claim **1** wherein the p-type epitaxy layer has a thickness range of 2 um to 7 um.

4. The CMOS image sensing pixel of claim **1** wherein the control circuit includes a color selecting component.

5. The CMOS image sensing pixel of claim **1** wherein the n-type substrate includes a silicon material.

6. The CMOS image sensing pixel of claim **1** wherein the second width is associated with a quantum efficiency.

7. The CMOS image sensing pixel of claim **1** wherein the second width is associated with a quantum efficiency, the quantum efficiency being associated with a color.

8. The CMOS image sensing pixel of claim **1** wherein the third width is associated with a depletion region caused by the n-type layer and the p-type epitaxy layer.

9. The CMOS image sensing pixel of claim **1** wherein the control circuit comprises a voltage source for applying a first voltage, a second voltage, and a third voltage to the n-type substrate, wherein:

the first voltage is configured for resulting in a first output, the first output being associated with a first color;

the second voltage is configured for resulting in a second output, the second output being associated with a second color, and

the third voltage is configured for resulting in a third output, the third output being associated with a third color;

wherein the first color, the second color, and the third color are further determined using a first weighting factor, a second weighting factor, and a third weighting factor.

10. The CMOS image sensing pixel of claim **1** further comprising a first epitaxy layer, the first epitaxy layer being positioned between the n-type substrate and the p-type silicon epitaxy layer.

11. The CMOS image sensing pixel of claim **10** wherein the first epitaxy layer includes a silicon germanium material.

12. An image sensing pixel, comprising:

an n-type silicon substrate, the n-type semiconductor substrate including a first width;

a p-type silicon layer overlying the n-type substrate, the p-type silicon layer including a second width;

an n-type silicon layer overlying the p-type silicon layer, the n-type silicon layer being associated with a third width;

a pn junction formed between the p-type silicon layer and the n-type silicon layer; and

a silicon germanium layer in the p-type silicon layer, the silicon germanium layer being positioned away from the pn junction.

13. The image sensing pixel of claim **12** wherein the silicon germanium layer is free from pn junctions.

14. The image sensing pixel of claim **12** wherein the silicon germanium layer is configured for absorption of red light.

15. An image sensing pixel device, comprising:

a first photodiode having a first p-type region and a first n-type region forming a first pn junction overlying a first n-type substrate;

a second photodiode having a second p-type region and a second n-type region forming a second pn junction overlying a second n-type substrate;

a third photodiode having a third p-type region and a third n-type region forming a third pn junction overlying a third n-type substrate;

a terminal coupled to the first n-type region, the second n-type region, and the third n-type region;

a first bias voltage coupled to the first n-type substrate;

a second bias voltage coupled to the second n-type substrate; and

a third bias voltage coupled to the third n-type substrate.

16. The image sensing pixel device of claim **15**, wherein:

the third p-type region further comprising a silicon germanium region disposed away from the third pn junction.

17. The image sensing pixel device of claim **15**, wherein the first bias voltage is configured for absorption of blue light.

18. The image sensing pixel device of claim **15**, wherein the second bias voltage is configured for absorption of green light.

19. The image sensing pixel device of claim **15**, wherein the third bias voltage is configured for absorption of red light.

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