

US007864079B1

(12) **United States Patent**
Lablans

(10) **Patent No.:** **US 7,864,079 B1**
(45) **Date of Patent:** **Jan. 4, 2011**

(54) **TERNARY AND HIGHER MULTI-VALUE DIGITAL SCRAMBLERS/DESCRAMBLERS**

(75) Inventor: **Peter Lablans**, Morris Township, NJ (US)

(73) Assignee: **Ternarylogic LLC**, Morristown, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

- 3,649,915 A 3/1972 Mildonian
- 3,656,117 A 4/1972 Maley et al.
- 3,660,678 A 5/1972 Maley et al.
- 3,663,837 A 5/1972 Epstein et al.
- 3,671,764 A 6/1972 Maley et al.
- 3,718,863 A 2/1973 Fletcher et al.
- 3,760,277 A 9/1973 Whang
- 3,988,538 A 10/1976 Patten
- 3,988,676 A 10/1976 Whang

(Continued)

(21) Appl. No.: **12/868,874**

(22) Filed: **Aug. 26, 2010**

Related U.S. Application Data

(63) Continuation of application No. 12/264,728, filed on Nov. 4, 2008, which is a continuation of application No. 10/912,954, filed on Aug. 6, 2004, now Pat. No. 7,505,589, and a continuation of application No. 10/936,181, filed on Sep. 8, 2004, now Pat. No. 7,002,490.

(60) Provisional application No. 60/501,335, filed on Sep. 9, 2003.

(51) **Int. Cl.**
H03M 7/38 (2006.01)

(52) **U.S. Cl.** **341/51**; 341/56; 365/168

(58) **Field of Classification Search** 341/50, 341/51, 57, 56; 365/168; 708/491-492
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

- 3,129,340 A 4/1964 Baskin
- 3,142,037 A 7/1964 Gazale
- 3,210,529 A 10/1965 Hanson
- 3,283,256 A 11/1966 Hurowirz
- 3,492,496 A 1/1970 Callan
- 3,515,805 A 6/1970 Fracassi et al.
- 3,586,022 A 6/1971 Bauer

OTHER PUBLICATIONS

Peter Lablans, The Logic of More, "http://ternarylogic.home.att.net", made available on Internet Mar. 20, 2003.

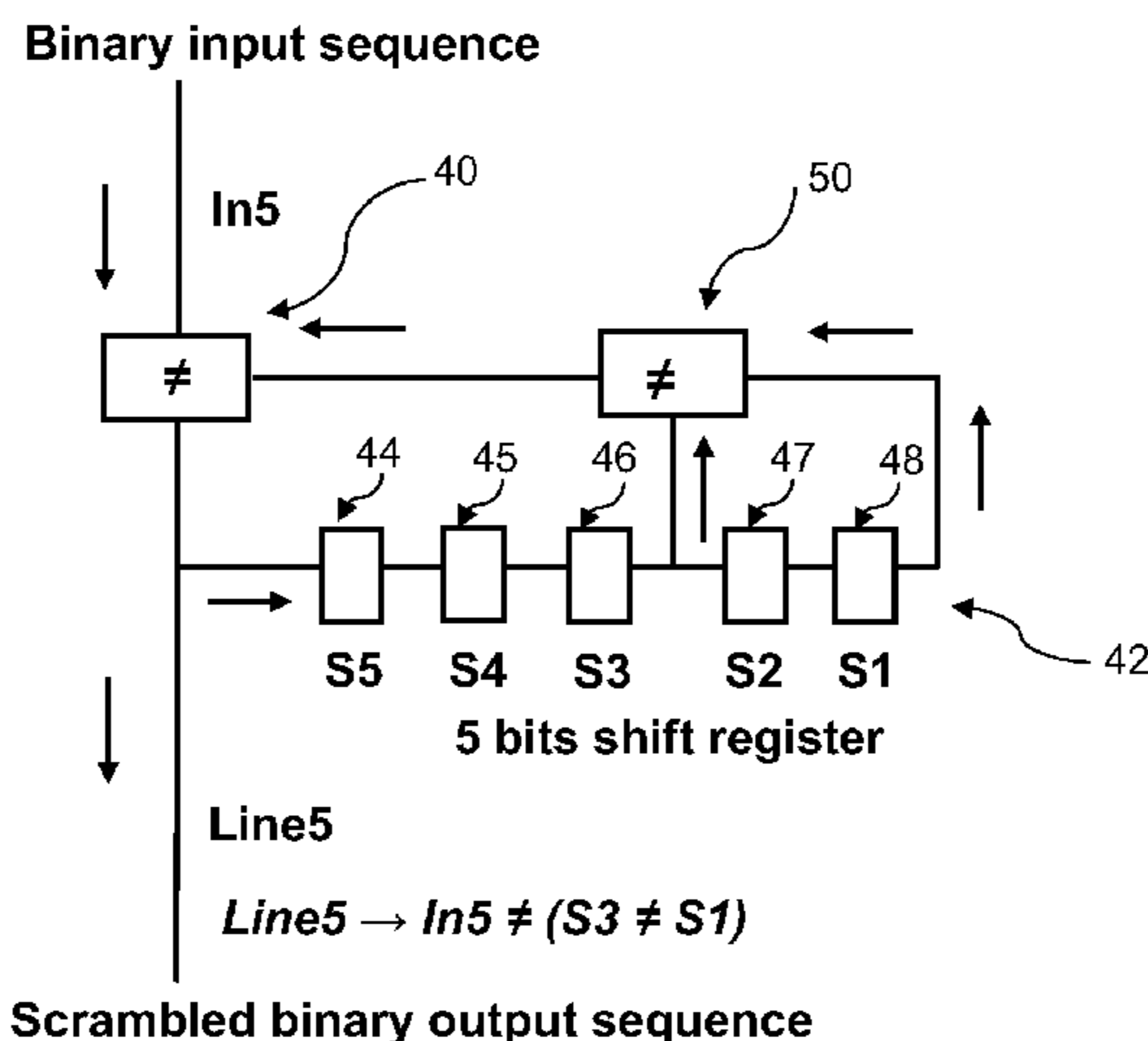
(Continued)

Primary Examiner—Brian Young
(74) *Attorney, Agent, or Firm*—Diehl Servilla LLC

(57) **ABSTRACT**

Ternary (3-value) and higher, multi-value digital scramblers/descramblers in digital communications. The method and apparatus of the present invention includes the creation of ternary (3-value) and higher value truth tables that establish ternary and higher value scrambling functions which are its own descrambling functions. The invention directly codes by scrambling ternary and higher-value digital signals and directly decodes by descrambling with the same function. A disclosed application of the invention is the creation of composite ternary and higher-value scrambling devices and methods consisting of single scrambling devices or functions combined with ternary or higher value shift registers. Another disclosed application is the creation of ternary and higher-value spread spectrum digital signals. Another disclosed application is a composite ternary or higher value scrambling system, comprising an odd number of scrambling functions and the ability to be its own descrambler.

19 Claims, 18 Drawing Sheets



U.S. PATENT DOCUMENTS

4,304,962 A 12/1981 Fracassi et al.
 4,378,595 A 3/1983 Current
 4,383,322 A 5/1983 Halpern et al.
 4,775,984 A 10/1988 Jaffre et al.
 4,808,854 A 2/1989 Reinagel
 4,815,130 A 3/1989 Lee
 4,984,192 A 1/1991 Flynn
 4,990,796 A 2/1991 Olson
 5,017,817 A 5/1991 Yamakawa
 5,230,003 A 7/1993 Dent et al.
 5,412,687 A 5/1995 Sutton et al.
 5,563,530 A 10/1996 Frazier
 5,621,580 A 4/1997 Cruz et al.
 5,714,892 A 2/1998 Bowers et al.
 5,724,383 A 3/1998 Gold et al.
 5,745,522 A 4/1998 Heegard
 5,761,239 A 6/1998 Gold et al.
 5,790,265 A 8/1998 Shikakura
 5,790,591 A 8/1998 Gold et al.
 5,856,980 A 1/1999 Doyle
 5,917,914 A 6/1999 Shaw et al.
 5,959,871 A 9/1999 Pierzchala et al.
 5,978,412 A 11/1999 Takai
 5,999,542 A 12/1999 Turner et al.
 6,122,376 A 9/2000 Rao
 6,133,753 A 10/2000 Thomson et al.
 6,133,754 A 10/2000 Olson
 6,188,714 B1 2/2001 Yamaguchi
 6,192,257 B1 2/2001 Ray
 6,320,897 B1 11/2001 Fattouche et al.
 6,430,246 B1 8/2002 Ozluturk
 6,452,958 B1 9/2002 van Nee
 6,463,448 B1 10/2002 Mo
 6,477,205 B1 11/2002 Dobljar et al.
 6,510,228 B2 1/2003 Rose
 6,519,275 B2 2/2003 Callaway et al.
 6,763,363 B1 7/2004 Driscoll
 6,907,062 B2 6/2005 Carlson
 7,002,490 B2 * 2/2006 Lablans 341/10
 7,177,424 B1 2/2007 Furuya et al.
 7,286,669 B2 * 10/2007 Nishizaki 380/255

7,668,312 B2 * 2/2010 Lecomte et al. 380/210
 2002/0054682 A1 5/2002 Di Bernardo et al.
 2002/0089364 A1 7/2002 Goldgeisser et al.
 2003/0072449 A1 4/2003 Myszne
 2003/0099359 A1 5/2003 Hui
 2003/0165184 A1 9/2003 Welborn et al.
 2004/0021829 A1 2/2004 Griffin
 2004/0032918 A1 2/2004 Shor et al.
 2004/0032949 A1 2/2004 Forest
 2004/0037108 A1 2/2004 Notani
 2004/0042702 A1 3/2004 Akimoto
 2004/0068164 A1 4/2004 Diab et al.
 2004/0085937 A1 5/2004 Noda
 2004/0091106 A1 5/2004 Moore et al.

OTHER PUBLICATIONS

Peter Lablans, The Logic of More, "http://ternarylogic.home.att.net", made available on Internet Sep. 3, 2003.
 Deavours, et al., Machine Cryptography and Modern Cryptanalysis, 181-182, Artech House, Inc. 1985.
 Wicker, Stephen "Error Control Systems of Digital Communication and Storage", Prentice Hall (1995) pp. 109-121.
 Mathworks, "Communications Blockset Descrambler", http://www.mathworks.de/access/helpdesk_r13/help/toolbox/commblks/ref/descrambler.html, website,(1994-2007).
 Mathworks, "Communications Blockset Scrambler", http://www.mathworks.de/access/helpdesk.r13/help/toolbox/commblks/ref/scrambler.html, (before 2003), 1-2.
 Mathworks, "Descrambler Blocks (Communications Blockset)", *Matlab 7.1.0 R14 Help Screen*, (2005).
 Selected pages from Communications Blockset for use with Simulink, Reference, version 2, 2002, The Mathworks, 11 pages, Natick, MA 01760-2098, downloaded from Internet.
 Rogers, Derek P., "Non-Binary Spread-Spectrum Multiple-Access Communications", Derek Rogers, Ph. D. Thesis, 213 pages, The University of Adelaide, Faculty of Engineering, Adelaide, Australia, Mar. 1995, 213 pages.
 Sklar, Bernard "Reed-Solomon Codes", Downloaded from URL http://www.informit.com/content/images/art_sklar7_reed-solomon/elementLinks/art_sklar7_reed-solomon.pdf, (unknown pub date), pp. 1-33.

* cited by examiner

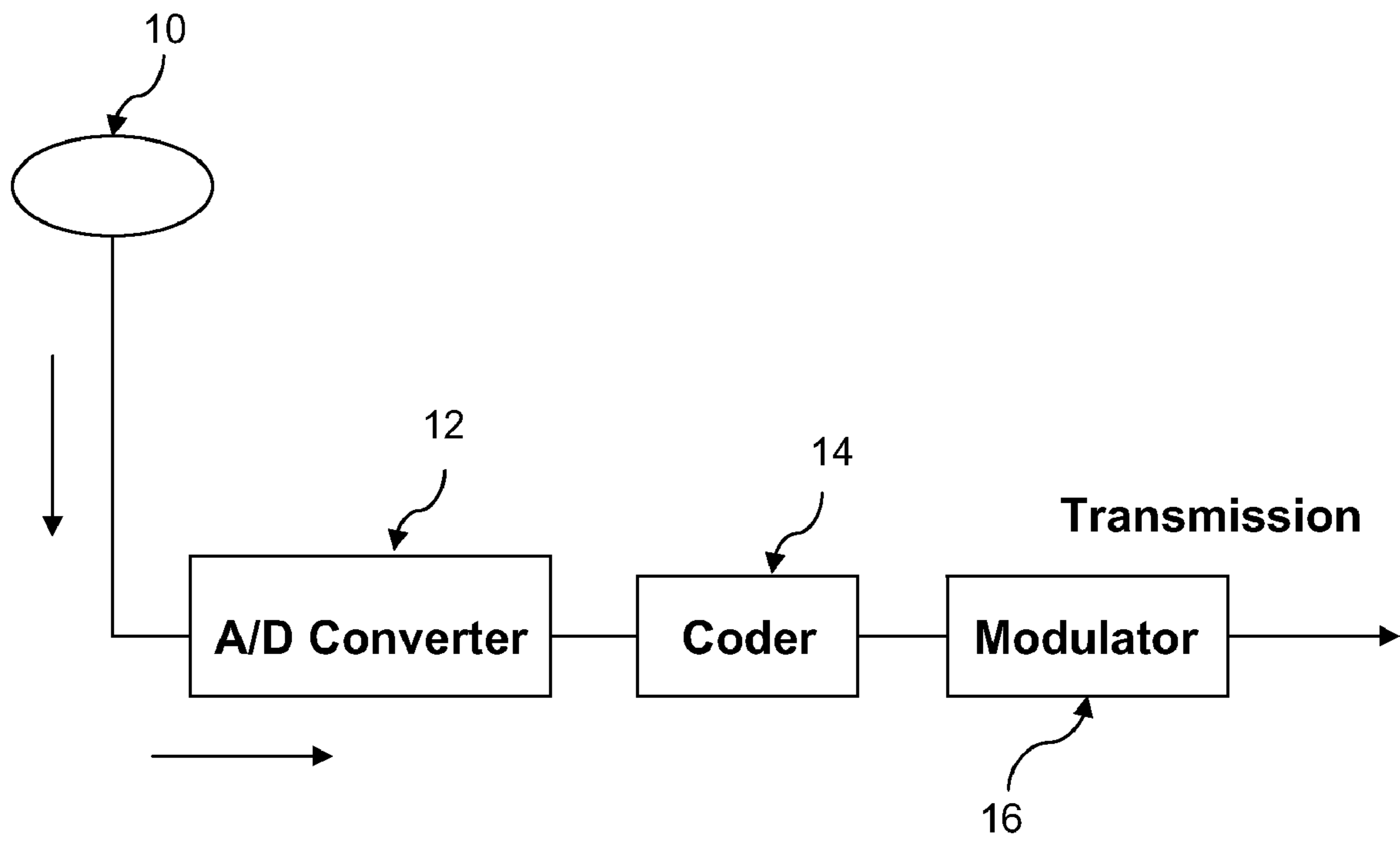


Figure 1.

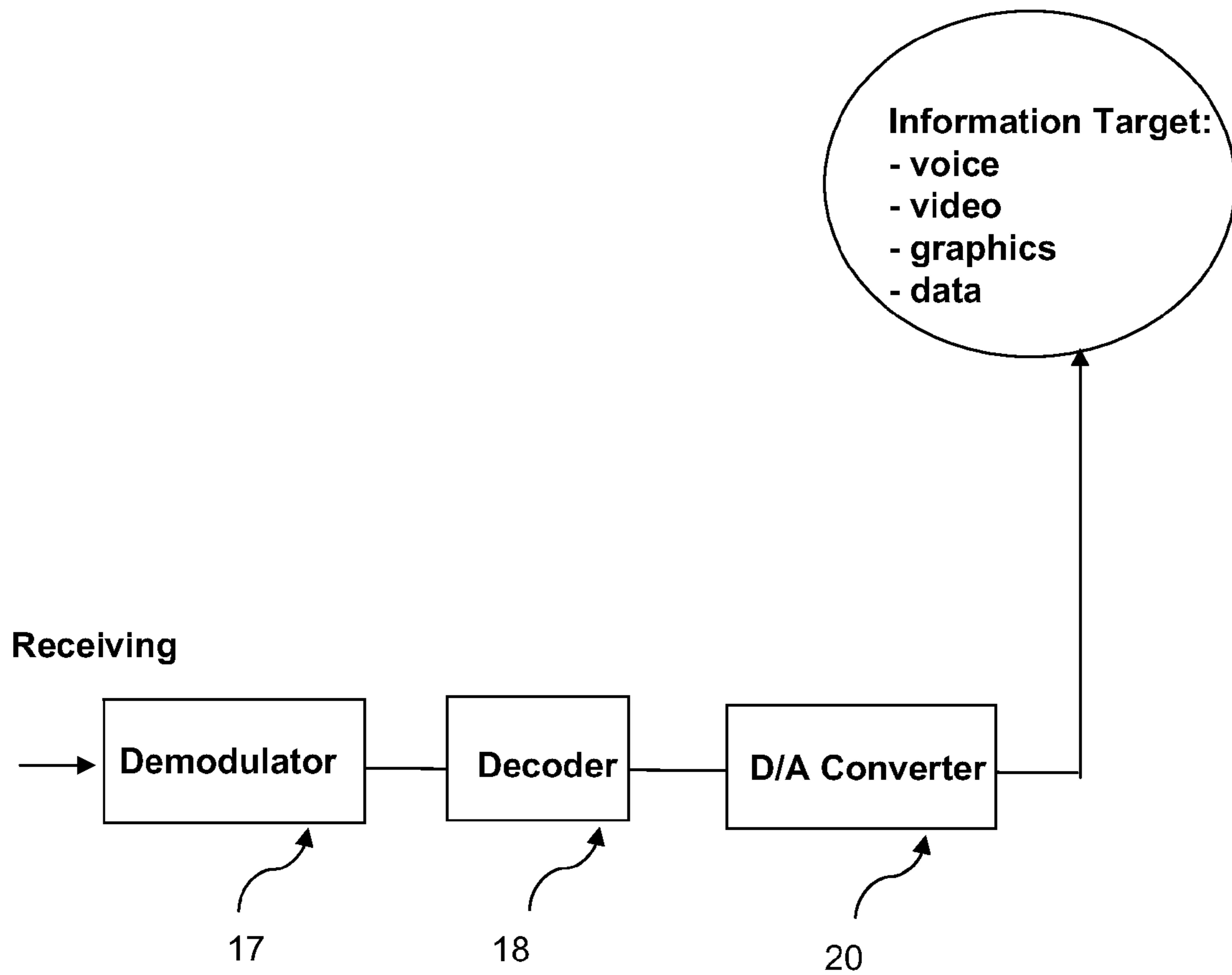


Figure 2.

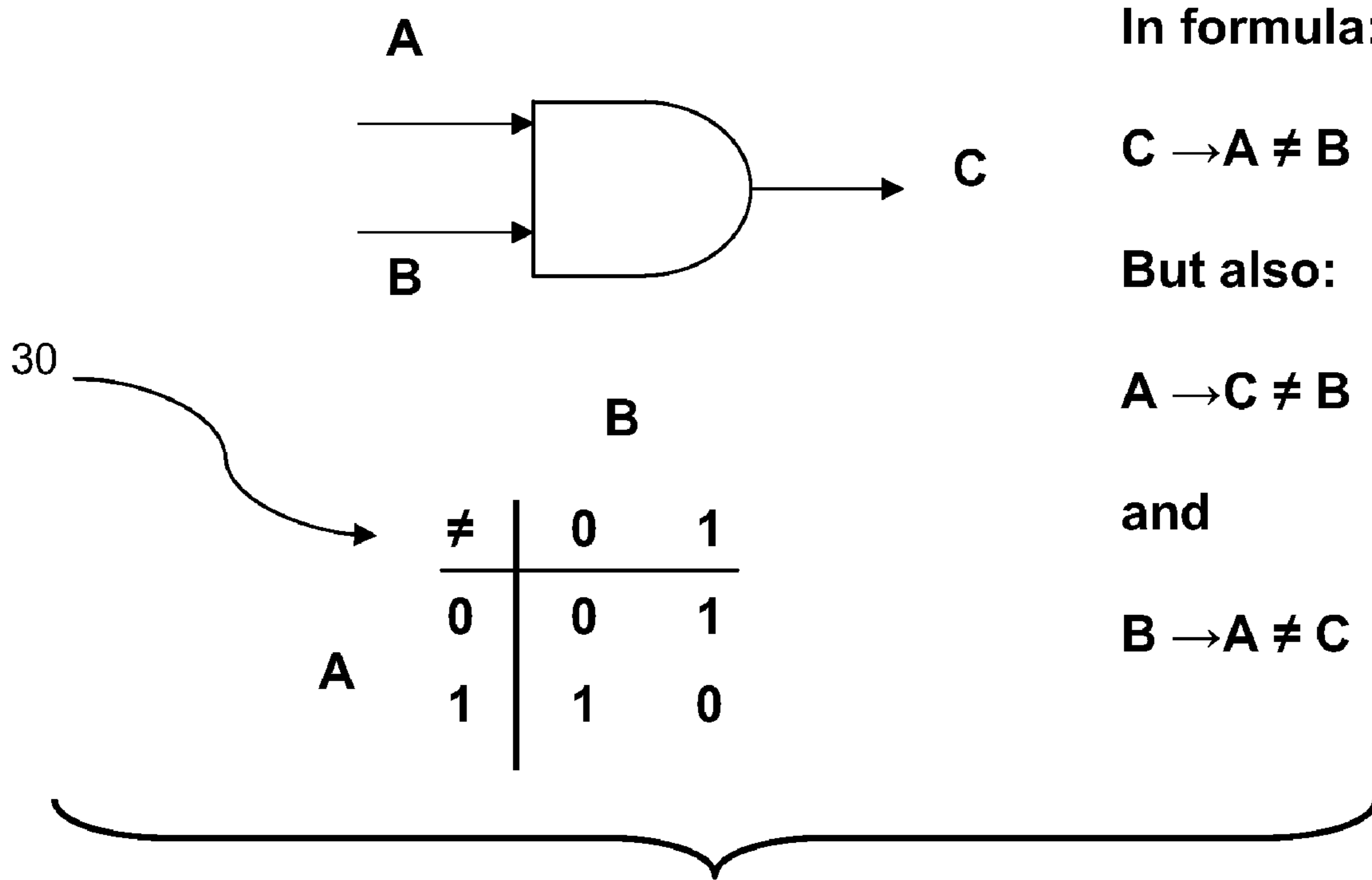


Figure 3.

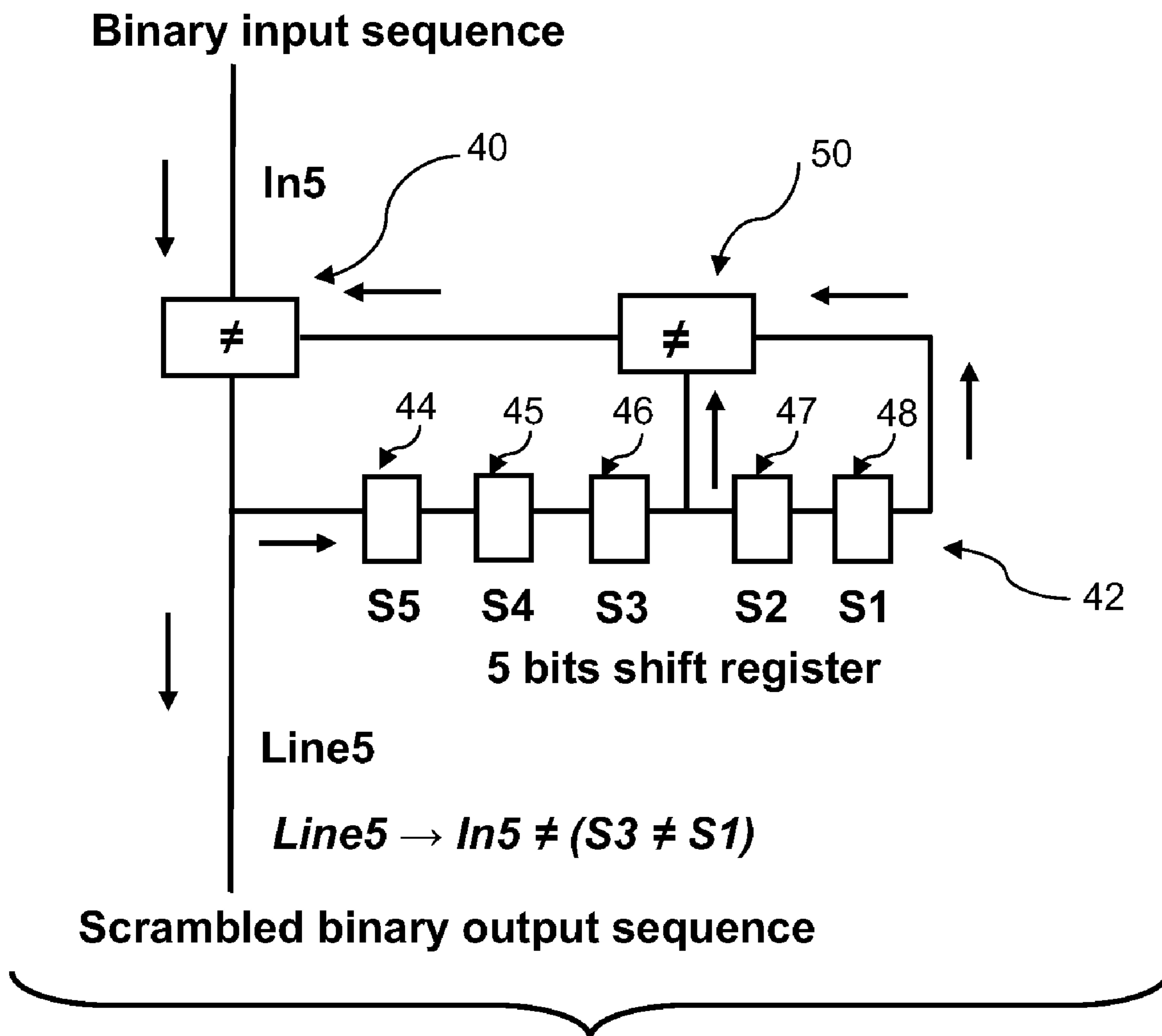


Figure 4.

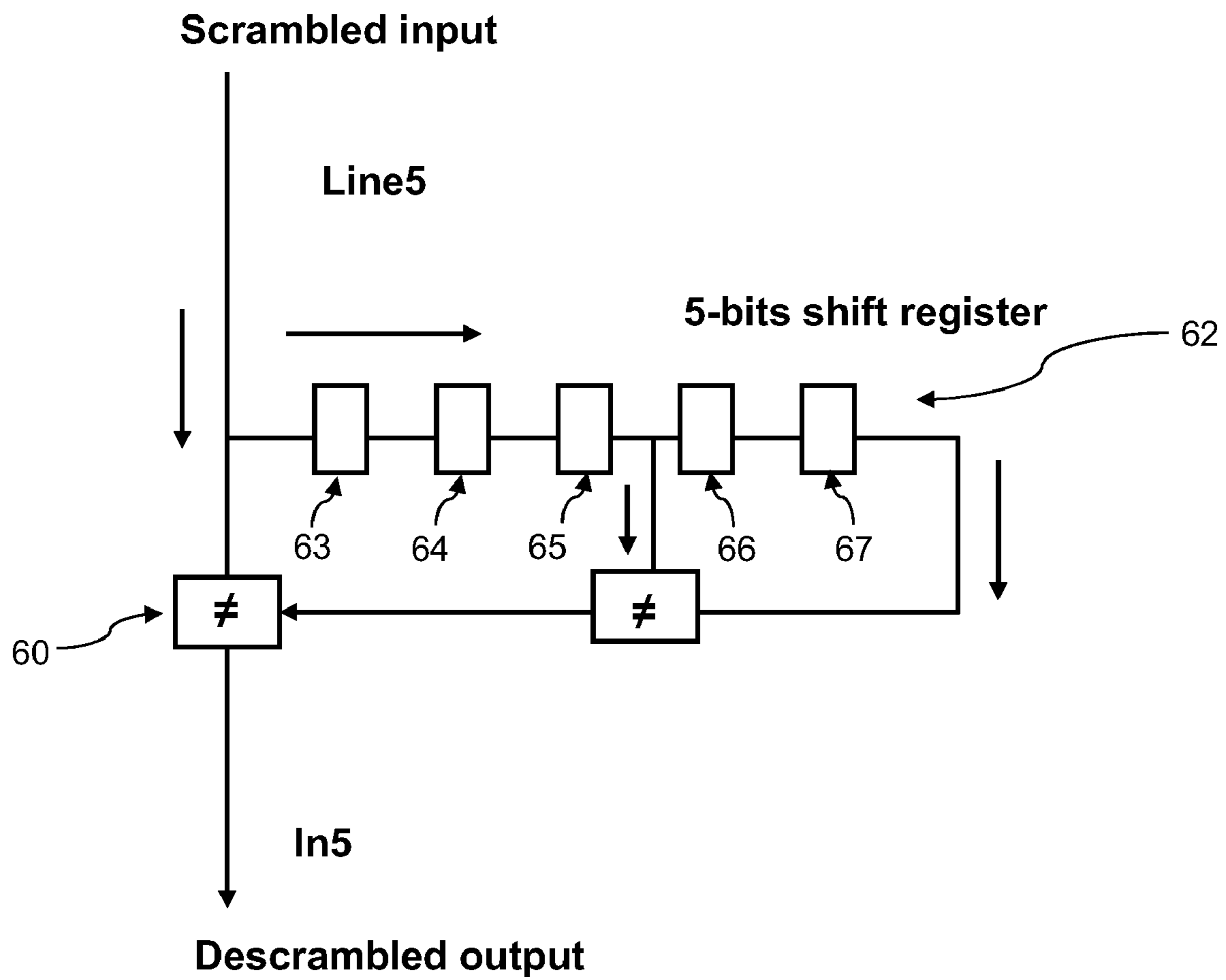
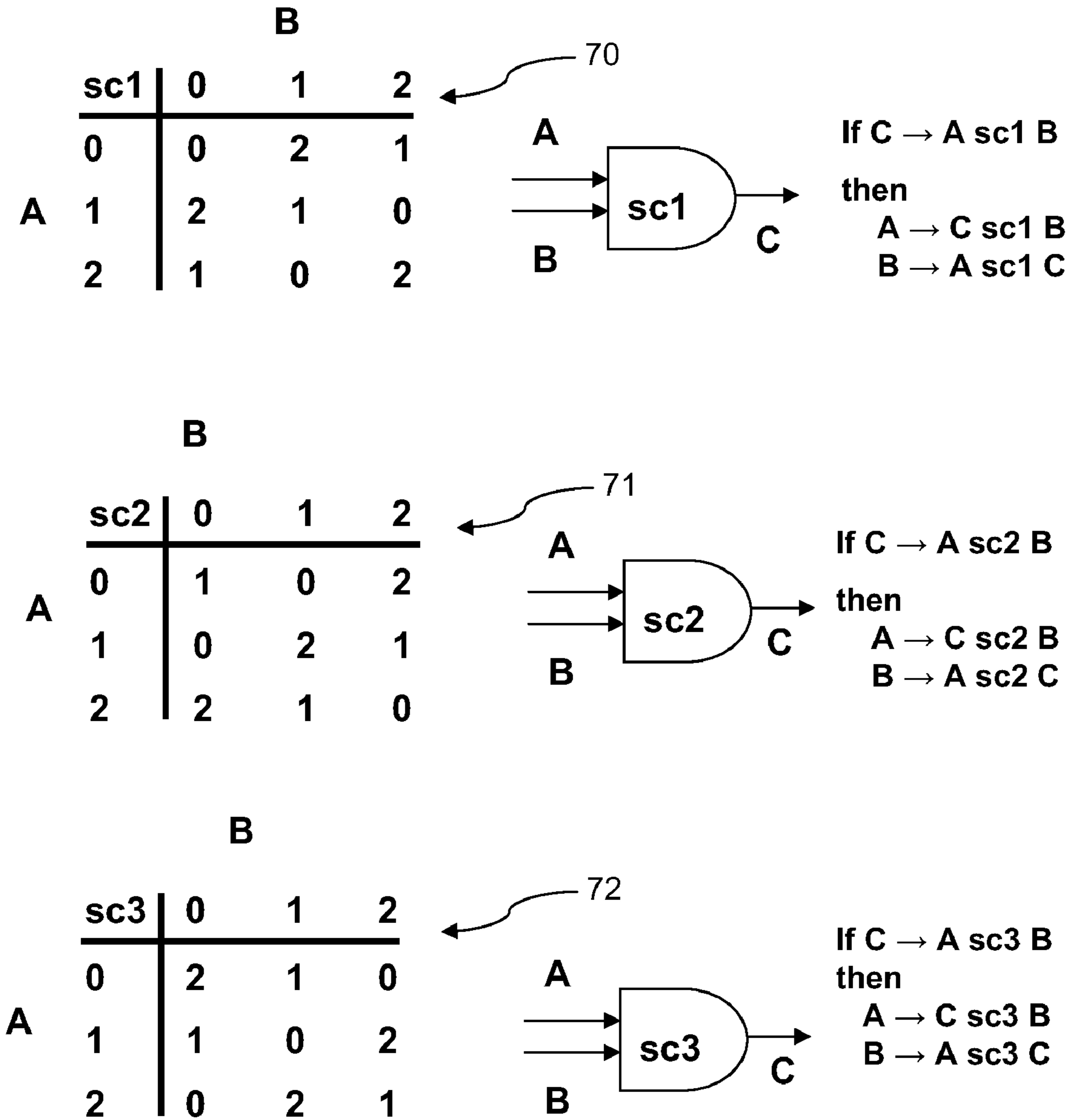
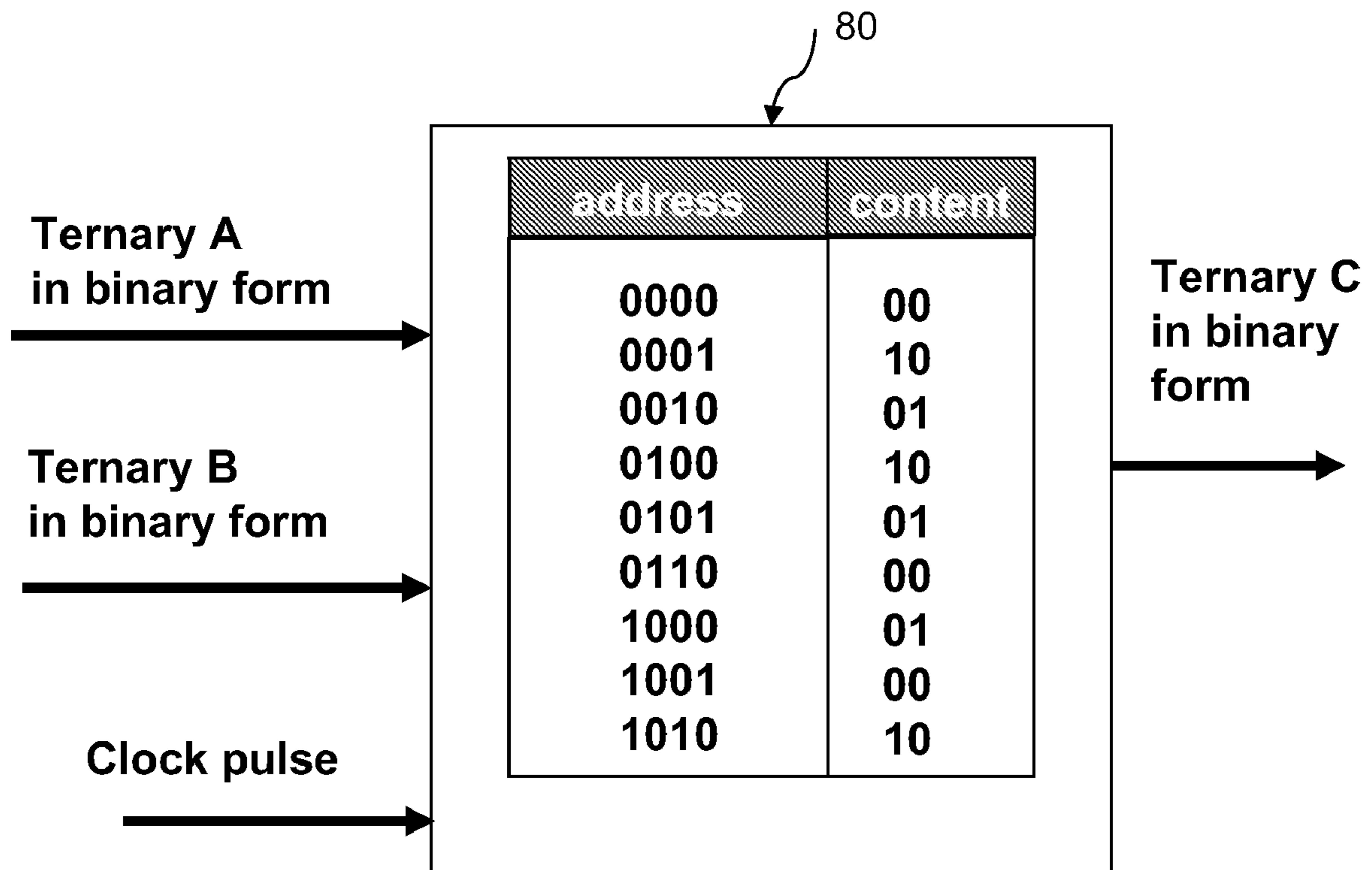


Figure 5.





		B		
	sc1	0	1	2
0	0	2	1	
1	2	1	0	
2	1	0	2	

Figure 7.

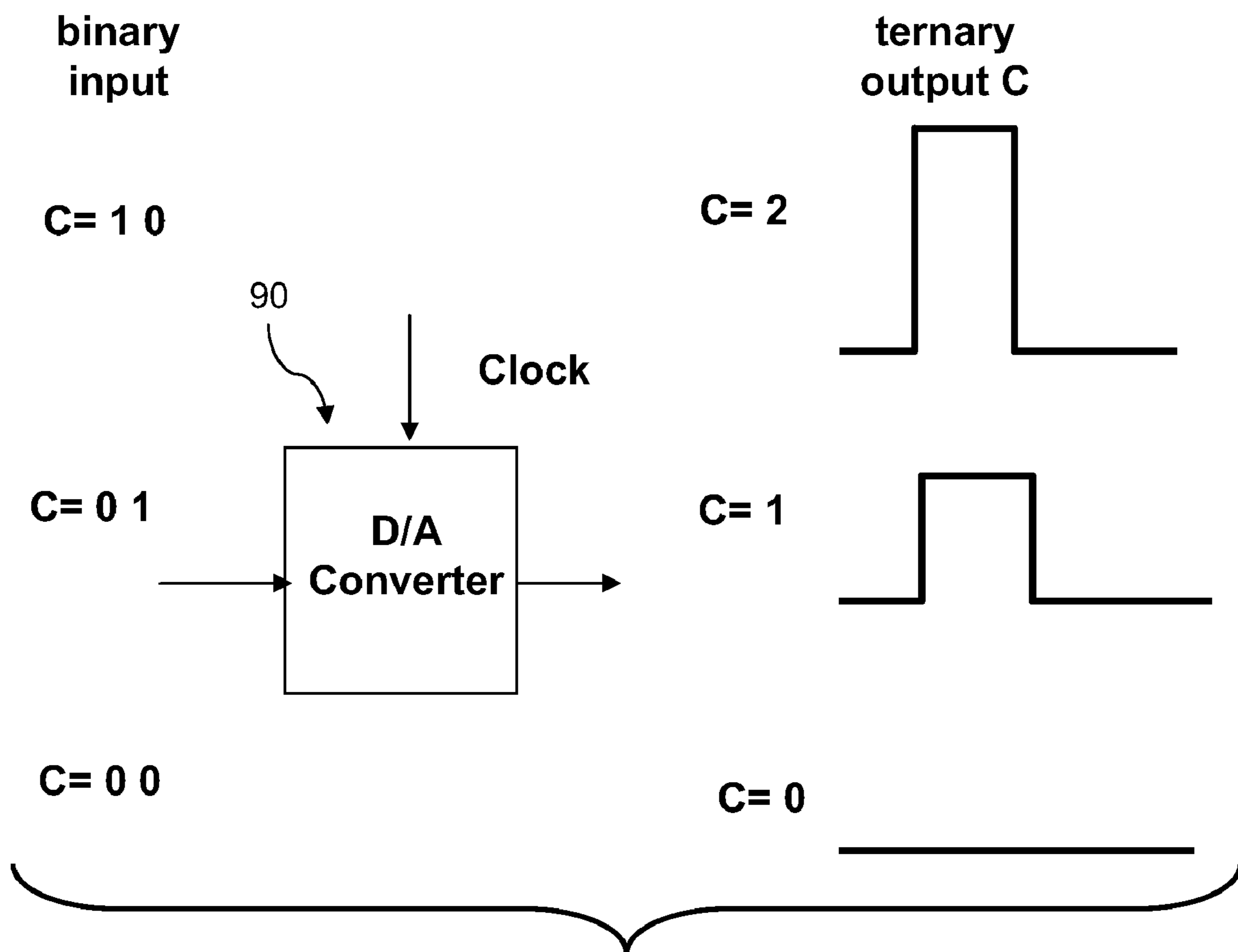


Figure 8.

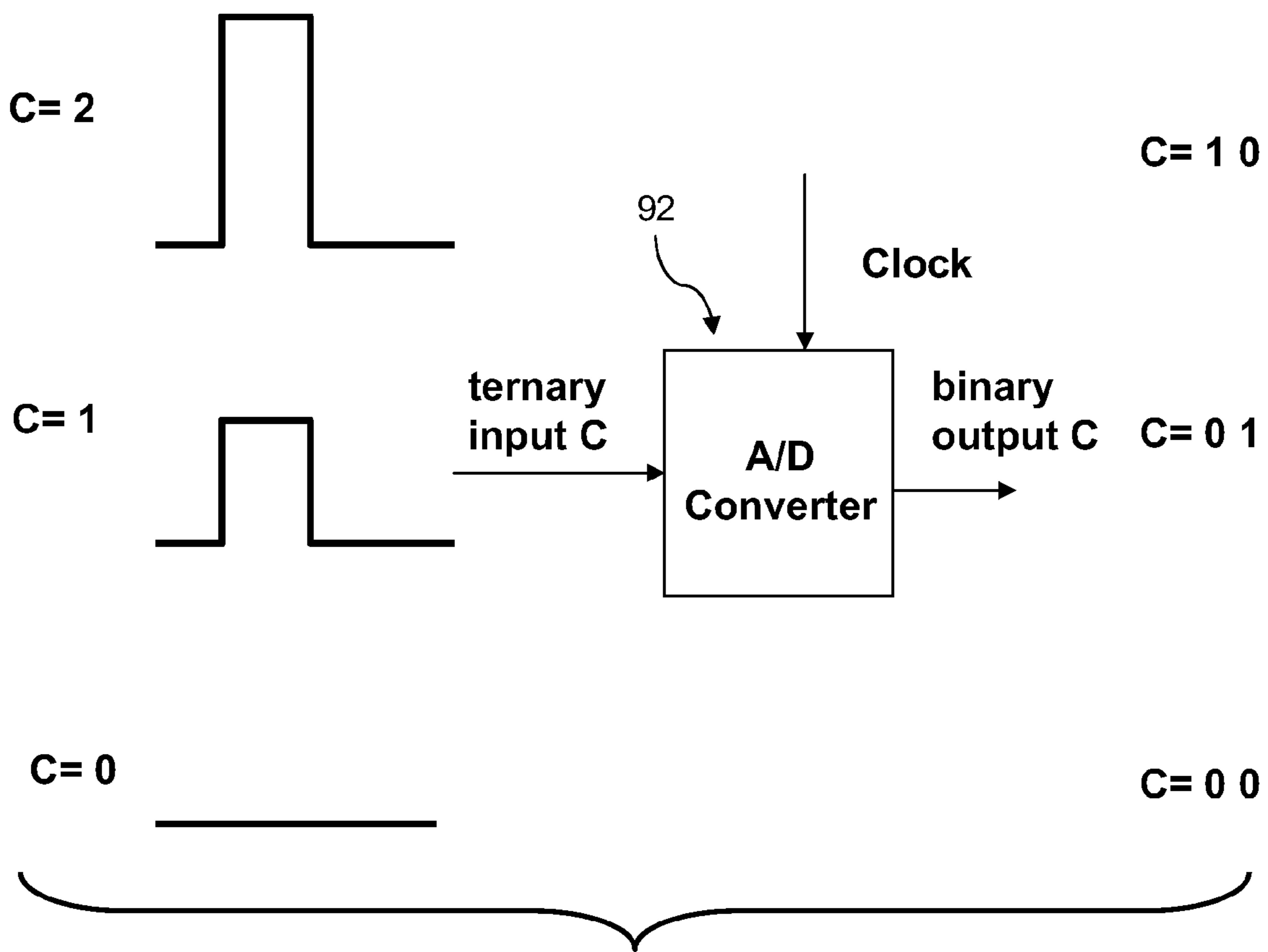
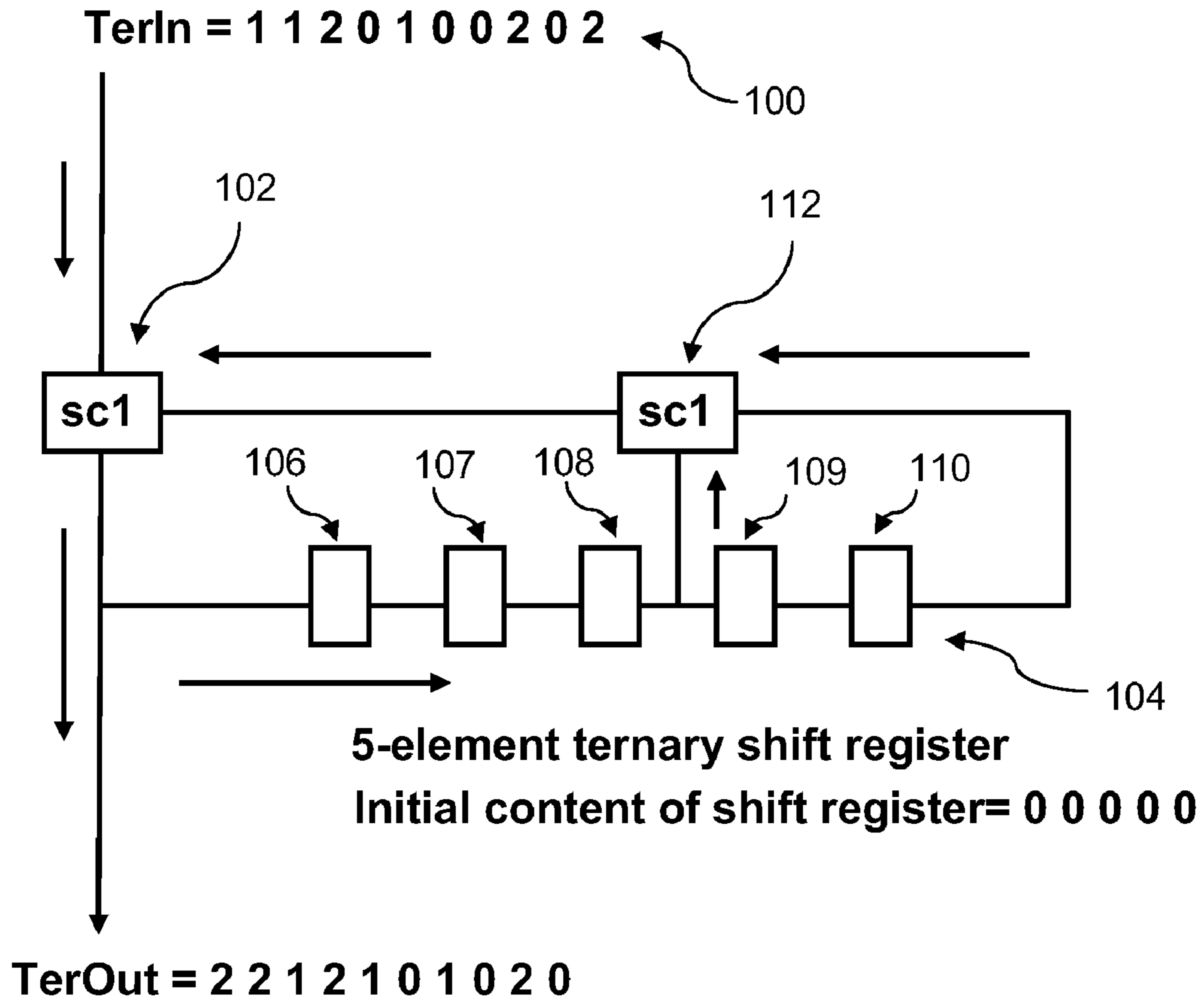


Figure 9.



sc1	0	1	2
0	0	2	1
1	2	1	0
2	1	0	2

Figure 10.

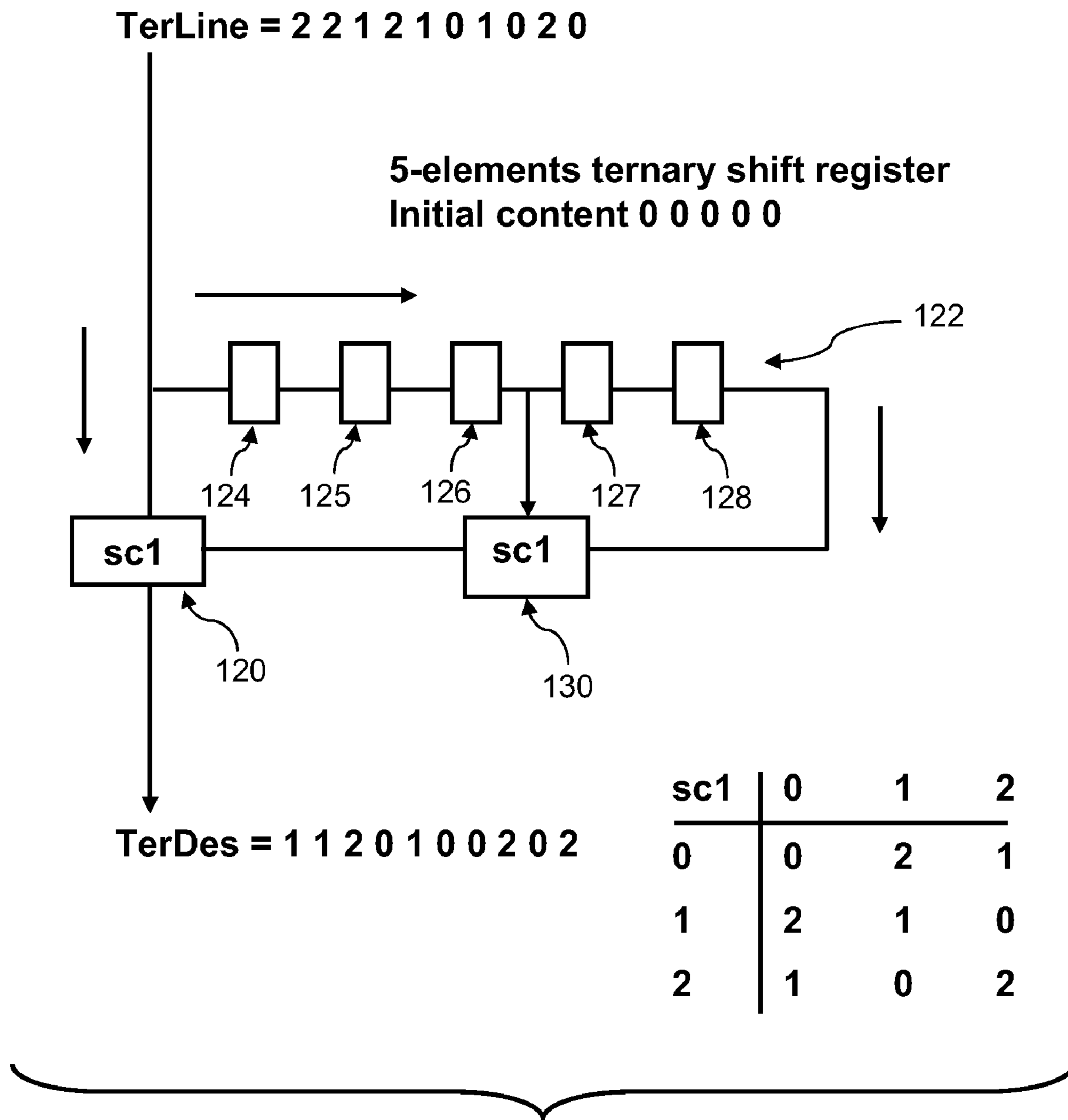
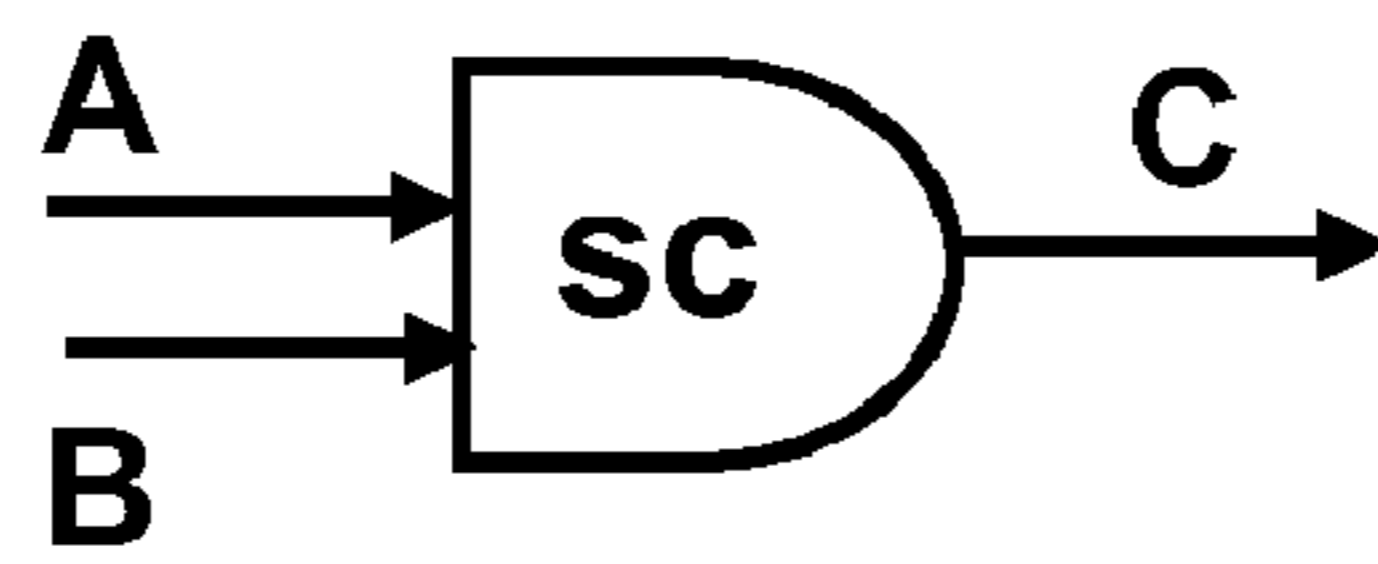


Figure 11.



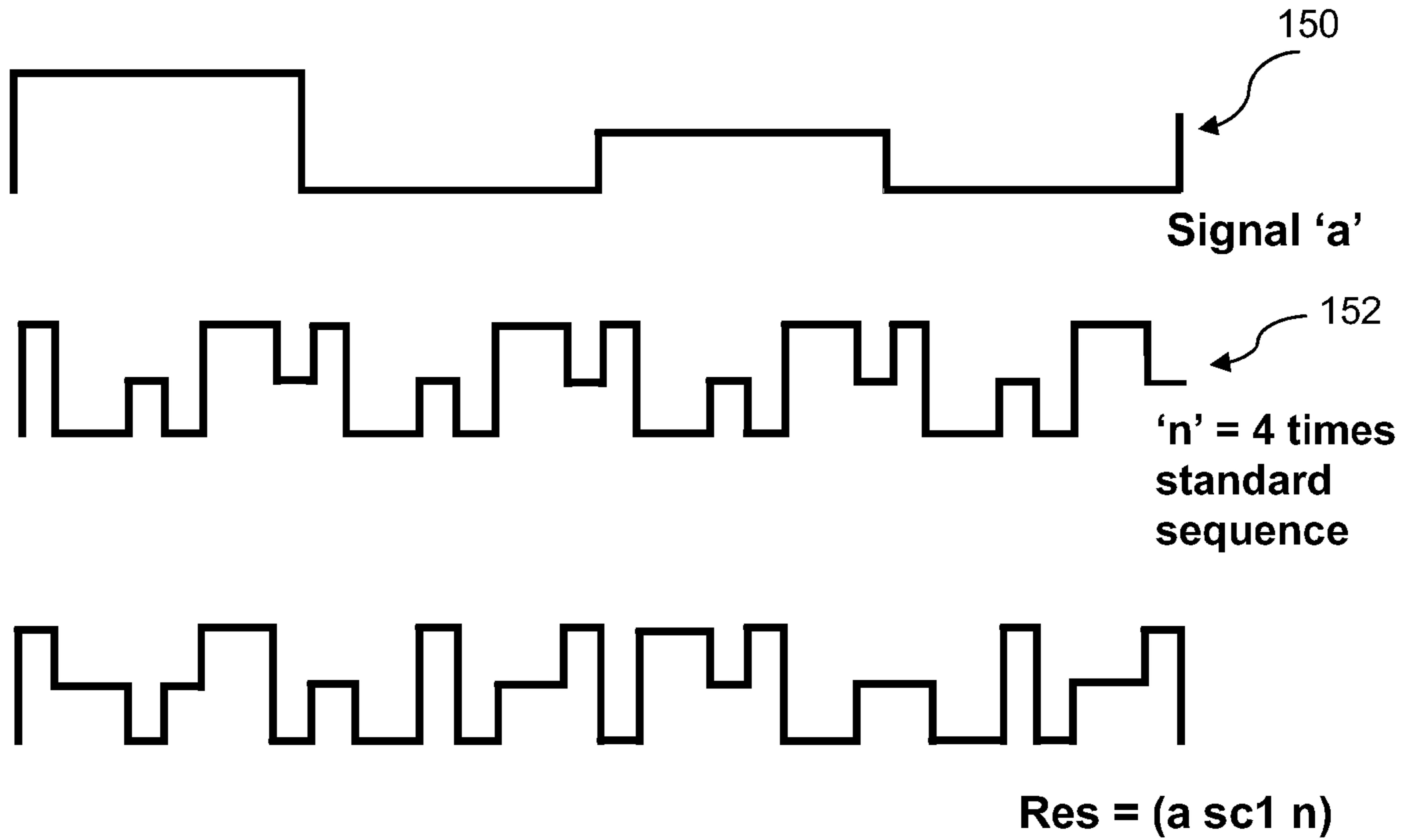
If $C \rightarrow A \text{ sc } B$
 then
 $A \rightarrow C \text{ sc } B$
 and
 $B \rightarrow A \text{ sc } C$

		B						
		sc	0	1	.	.	.	m
A	0		m	m-1	.	.		0
	1		m-1	m-2	.	.	0	.
	0	.	.

	.		1	0
	m		0	m	.	.	.	1

140

Figure 12.



Signal a = 2 2 2 2 2 2 2 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0

Sequence n = 2 0 0 1 0 2 2 1 2 0 0 1 0 2 2 1 2 0 0 1 0 2 2 1 2 0 0 1 0 2 2 1

Sequence Res = 2 1 1 0 1 2 2 0 1 0 0 2 0 1 1 2 0 2 2 1 2 0 0 1 1 0 0 2 0 1 1 2

sc1	0	1	2
0	0	2	1
1	2	1	0
2	1	0	2

154

Figure 13.

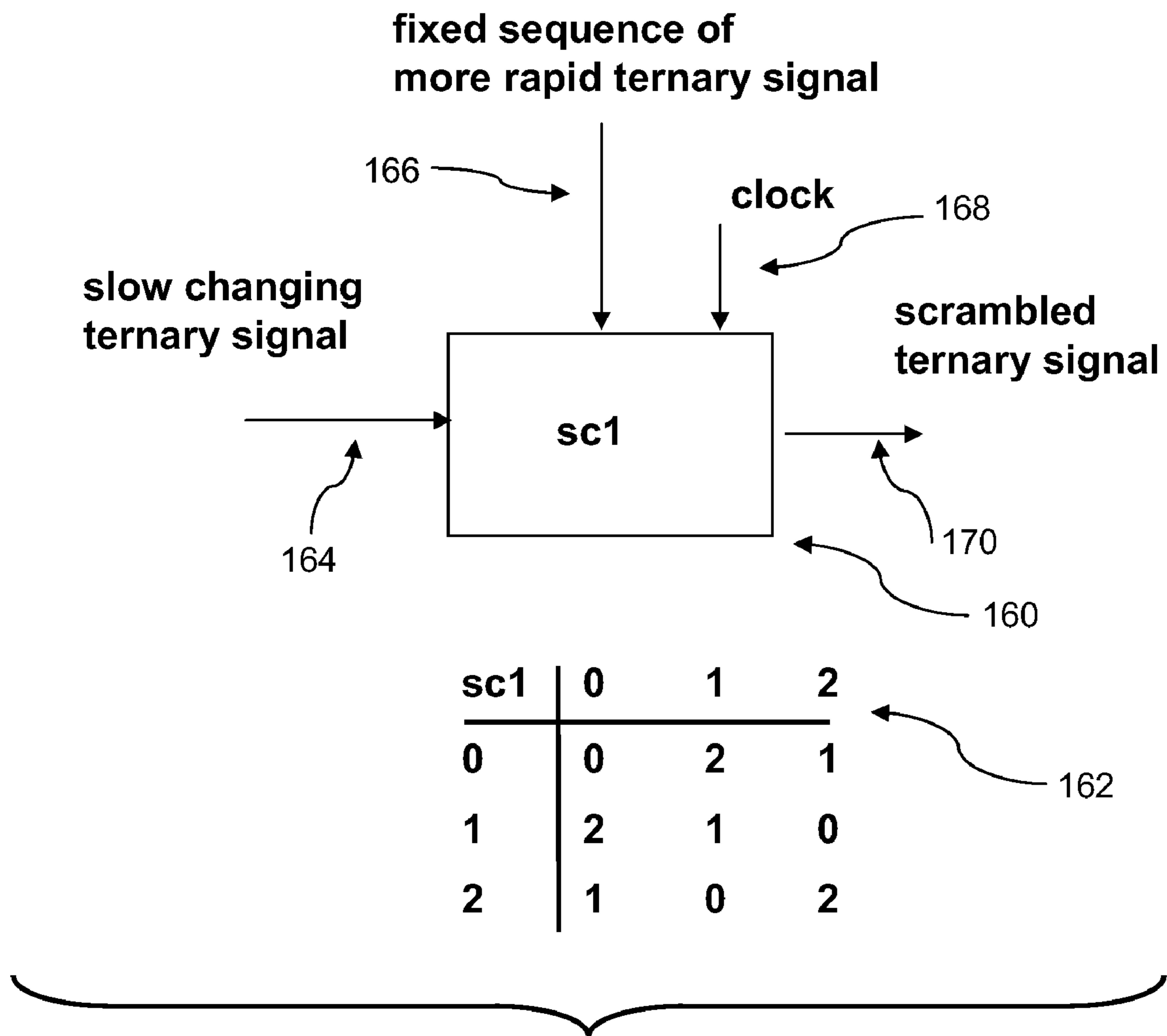


Figure 14.

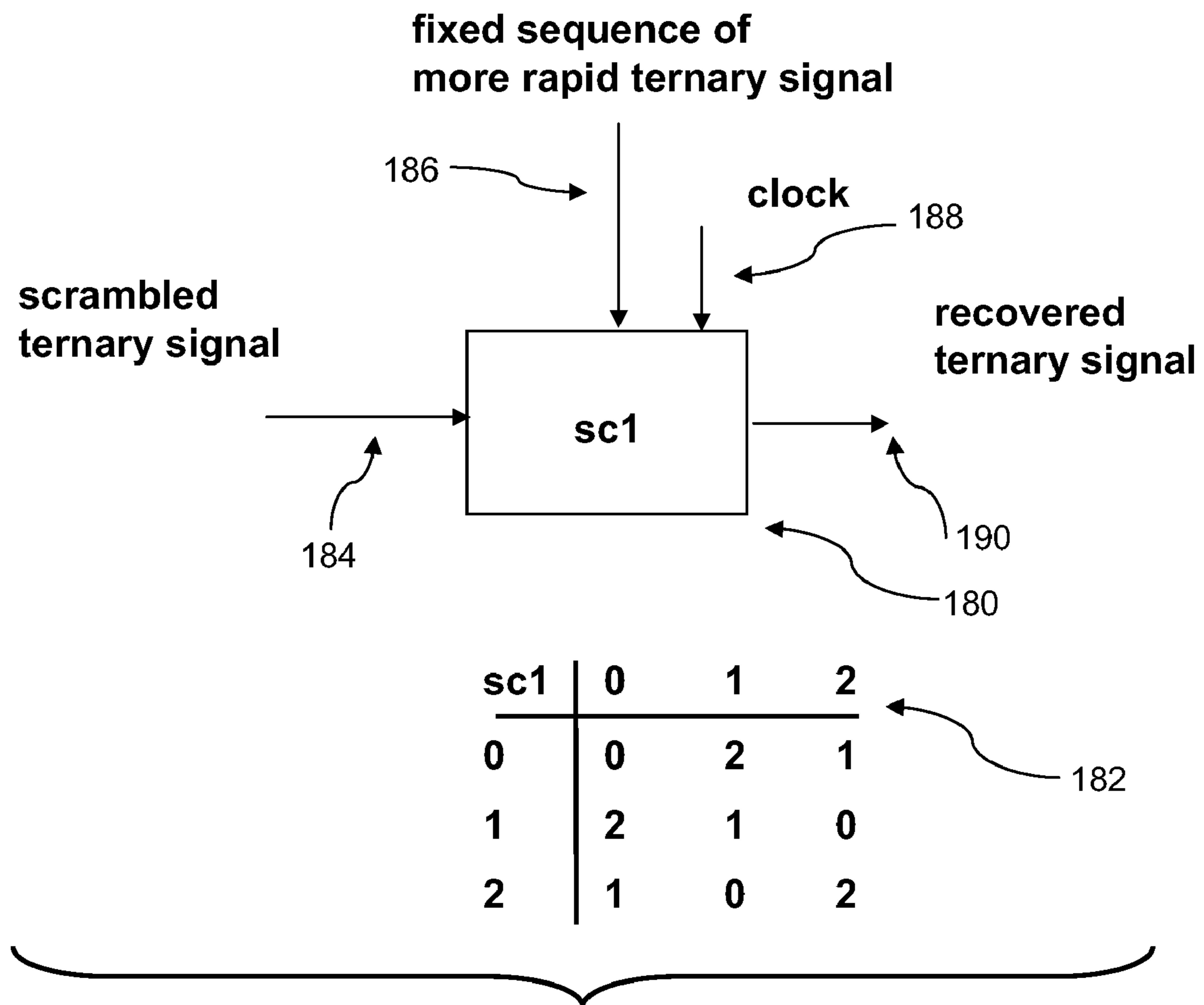


Figure 15.

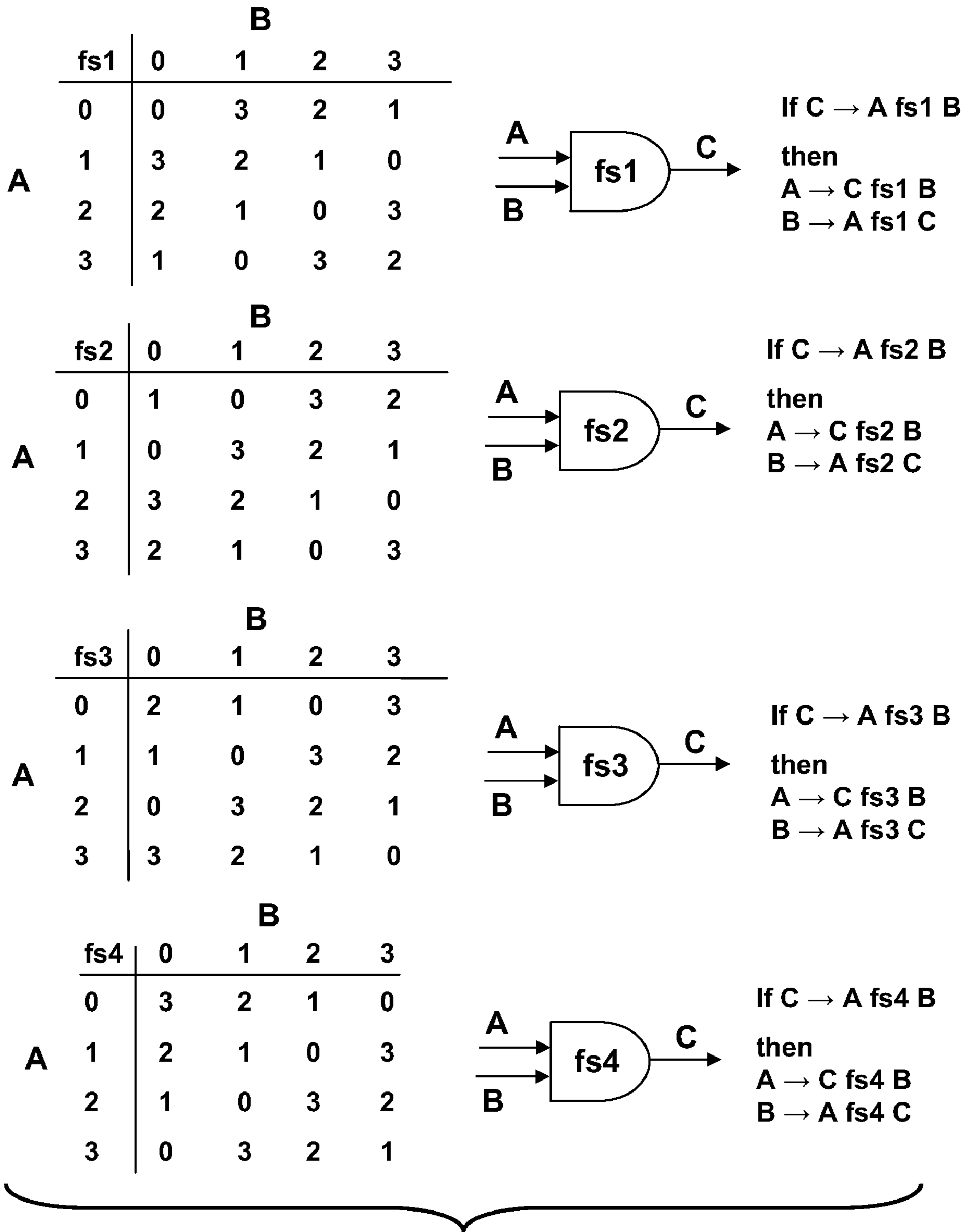
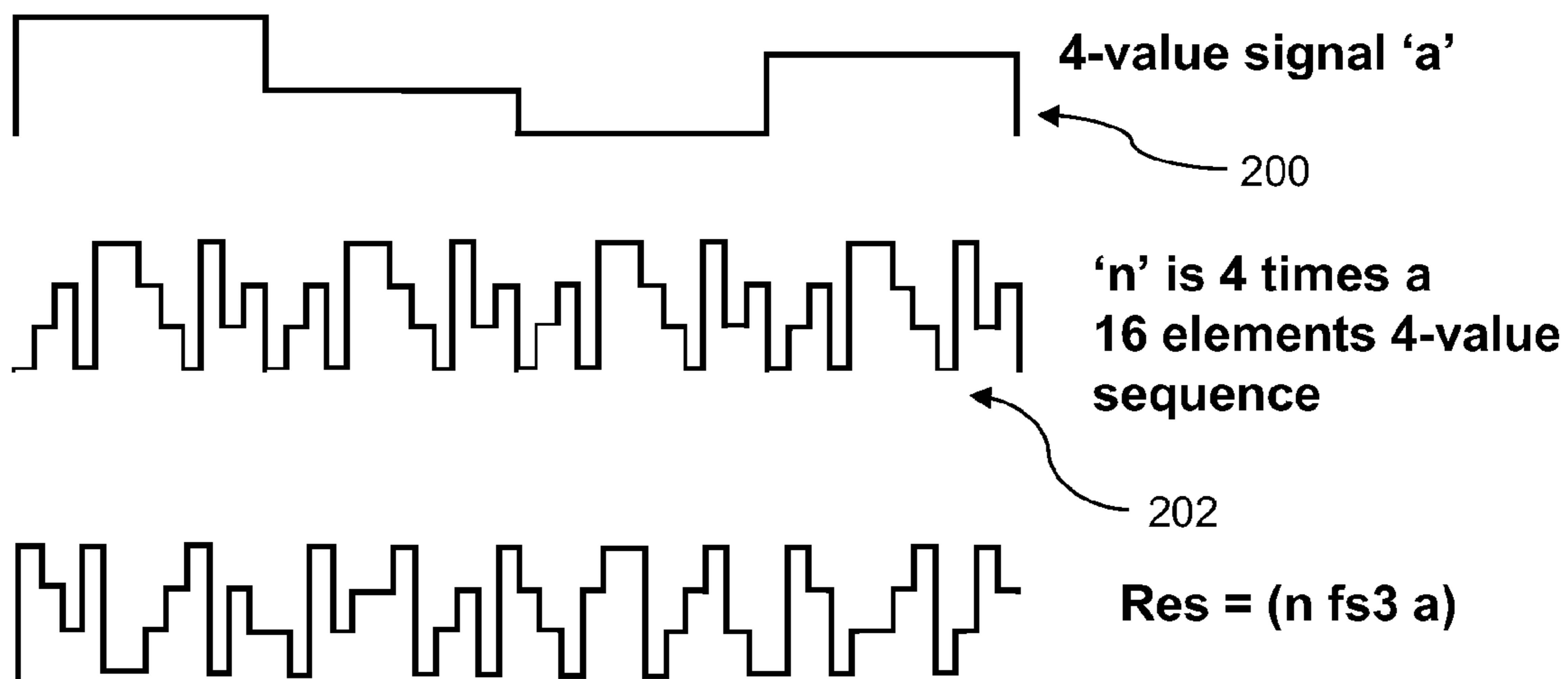


Figure 16.



signal a = 3102

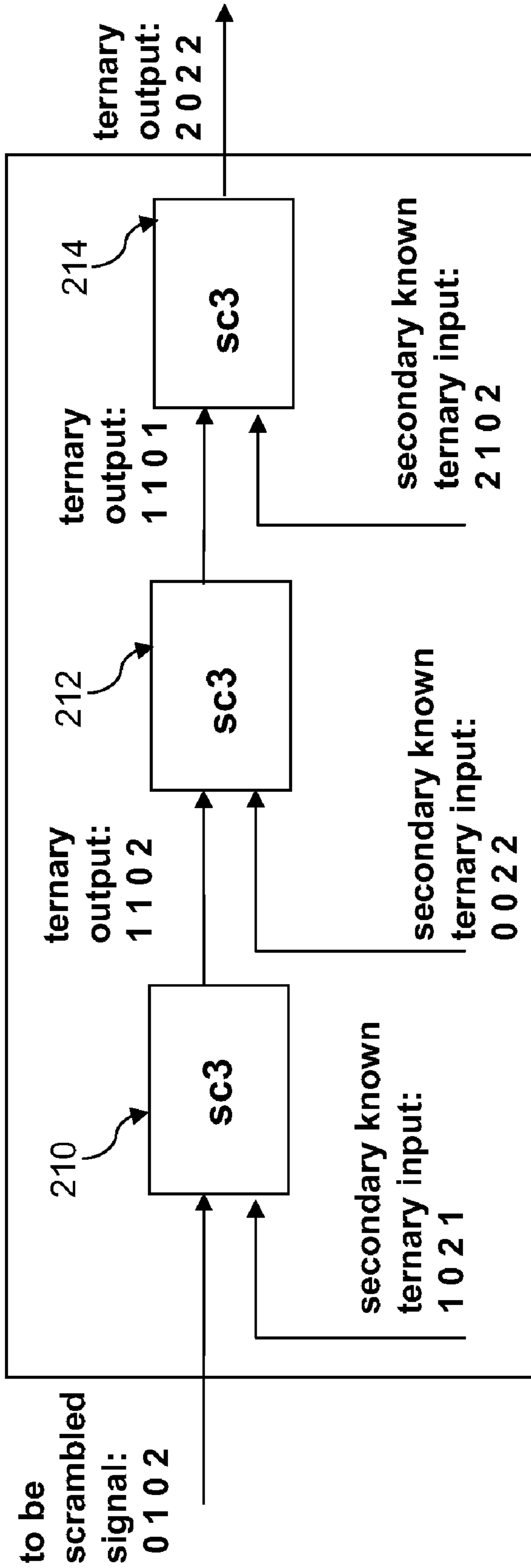
Sequence n = 012033210312

sequence Res = 321300123021103122301203210233012310032011230132

		B				
		fs3	0	1	2	3
A	0	2	2	1	0	3
	1	1	1	0	3	2
	2	0	0	3	2	1
	3	3	3	2	1	0

204

Figure 17.



216

	B			
sc3	0	1	2	
0	2	1	0	
1	1	0	2	
2	0	2	1	
A				

Figure 18.

TERNARY AND HIGHER MULTI-VALUE DIGITAL SCRAMBLERS/DESCRAMBLERS

STATEMENT OF RELATED CASES

This application is a continuation and claims the benefit of U.S. patent application Ser. No. 12/264,728 filed on Nov. 4, 2008 which is a continuation of U.S. patent application Ser. No. 10/912,954 filed on Aug. 6, 2004 now U.S. Pat. No. 7,505,589 issued Mar. 17, 2009, and of U.S. patent application Ser. No. 10/936,181 filed Sep. 8, 2004, now U.S. Pat. No. 7,002,490 issued Feb. 21, 2006 which are incorporated herein by reference in their entirety. Both patent application Ser. No. 10/912,954 filed on Aug. 6, 2004 now U.S. Pat. No. 7,505,589 issued Mar. 17, 2009, and of U.S. patent application Ser. No. 10/936,181 filed Sep. 8, 2004 claim the benefit of U.S. Provisional Patent Application No. 60/501,335, filed on Sep. 9, 2003 which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to telecommunications of digital signals. In particular, the present invention relates to coding a digital signal and decoding of the coded digital signal without error and loss of information.

Digital coding is applied widely for the transmission of signals over optical, cable, radio connections and other transmission media. Coding is applied to transmitted signals for several reasons. For example, coding helps retain the quality of the digitally coded signal after transmission. It can also hide the content of the coded message or signal. Coding can also protect the coded message against interference or jamming, and can increase the capacity of the transmission medium to allow the medium to handle a greater number of messages or signals.

More particularly, the present invention relates to the area of ternary and higher, multi-value digital scrambling methods and apparatus as well as descrambling methods and apparatus. The method and apparatus of the present invention which applies methods that generate digital sequences which are the coded form of digital message to be transmitted or which form a substantial basis for creating coded messages.

Typical digital transmission systems have transmitters and receivers. The original message to be transmitted can be any type of signal, such as voice, video, text or any other data format. The signal is digitized, coded and then modulated to be transmitted over the transmission medium. At the receiving end, the signal is demodulated, decoded and then applied to some device to re-constitute the original message format.

The digitized message has been generally represented in binary (or 2-value) format. This means that the signal provided to the coder is a binary signal and the signal provided to the decoder is also a binary signal.

There are different ways to implement binary coding and decoding. In the prior art, a well established way to code a binary message is by applying a binary scrambler. A binary scrambler is an electronic device or an executed method that has as its input a series or sequence of binary digits, which will be guided through a finite length shift register or a computer program that acts as such. The content of pre-established cells of the shift register will be tapped and connected to an element that will conduct a specific binary operation on two binary elements. In the prior art, this operation is overwhelmingly Modulo-2 addition. The result of the Modulo-2 addition can be fed back into the shift register, fed into a next Modulo-2 addition or being sent to the modulation stage of the transmission.

If the input to a binary scrambler is a sequence of binary digits, the output of a binary scrambler is also a series or sequence of binary digits. The input and output of a scrambler are in general and preferably dissimilar. The dissimilarity of the input and the output sequences depends on the input sequence, the length of the shift register, the number and place of taps and applied Modulo-2 add operations and initial content of the shift register.

The descrambler has as its input the output of the scrambler. The descrambler reverses the operation of the scrambler and can recover, without mistakes, the original uncoded digital message that formed the input to the scrambler.

The common element in all binary scramblers and descramblers are the binary Modulo-2 additions. The binary logical operation is also known under its binary logic designation: Exclusive OR or XOR or \neq .

Scramblers and descramblers are currently binary methods or devices that are composed of binary XOR functions. Binary XOR functions have the property of Modulo-2 addition. Modulo-2 addition is identical to Modulo-2 subtraction. In general, a binary signal is scrambled by adding it to another known binary signal under Modulo-2 rules. The original binary signal can be recovered from the scrambled signal by Modulo-2 subtraction of the known binary signal from the scrambled signal. Because Modulo-2 addition and Modulo-2 subtraction are both represented by the binary logic XOR function, binary scrambling and descrambling take place by the same binary logic function. While Modulo-2 addition is identical to Modulo-2 subtraction, that identity is not true for Modulo-3 and higher Modulo-n addition and subtraction. It is apparent to the inventor that the more fundamental description of identical scrambling/descrambling functions is that two binary inputs A and B generate a binary output C. If A and C are the inputs to the function, the output B is generated. Or if B and C are the inputs to the function, A is generated as the output. Binary scrambling functions can also be applied in binary Direct Sequence Spread Spectrum coding where an initial binary digital sequence is combined with a secondary, binary sequence with substantially more digits through a binary scrambling function.

In many cases it would be beneficial, either to the performance, quality or capacity of the telecommunication system to transmit modulated digital signals that represent higher value digits. For instance a cable system may transmit 3-value or ternary signals to balance the Direct Current component of the signals in the transmission system. These ternary signals can assume one of three states. The use of multi-value (greater than 2) signals also can increase the capacity (in information rate, or number of users) of a communication system. Nevertheless, many systems limit themselves to operating in a binary fashion. This is because of the availability and pervasiveness of binary technology and the lack of ternary and higher multi-value methods and technologies.

The availability of ternary (or 3-value) methods (even if executed in binary fashion) would greatly improve the performance of digital systems. Signal coding is an example of an area that would be greatly improved by the use of ternary or multi-value scrambling techniques. Also, as higher value scramblers have a greater number of scrambling functions, the application of ternary and higher value scramblers can make a spread-spectrum signal much harder to decode for un-authorized users and equipment. Application of ternary and higher-value scramblers can substantially improve the performance, capacity and security of digital communication systems.

In these respects and in others, the ternary and multi-value scrambling methods according to the present invention sub-

stantially depart from the conventional concepts, and provide a method primarily developed to conduct ternary and multi-value scrambling and descrambling of digital signals.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, method and apparatus for scrambling a ternary signal with a scrambler is provided. The ternary signal is able to assume one of three states. The scrambler has a first scrambling ternary logic device that implements a ternary logic function, sc , and a scrambling logic circuit.

In accordance with the method of the present invention, the ternary signal and an output from the scrambling logic circuit are input to the first scrambling ternary logic device. An output from the first scrambling ternary logic device is provided to the scrambling logic circuit.

The ternary logic function, sc , satisfies the following equations: (1) $A\ sc\ B=C$, where A is a first input to the scrambling ternary logic device, such as the ternary signal, B is a second input to the scrambling ternary logic device, such as the output from the scrambling logic circuit and C is the output from the first scrambling ternary logic device; (2) $C\ sc\ B=A$, if C and B were input to the first scrambling ternary logic device; and (3) $A\ sc\ C=B$; if A and C were input to the first scrambling ternary logic device.

A scrambled version of the ternary signal is output on the first ternary logic device.

The ternary logic function, sc , is defined by one of the following truth tables:

		In2		
In1		0	1	2
0	0	0	2	1
1	2	2	1	0
2	1	1	0	2

		In2		
In1		0	1	2
0	1	0	2	2
1	0	2	2	1
2	2	2	1	0

		In2		
In1		0	1	2
0	2	1	0	0
1	1	0	2	2
2	0	2	2	1

In accordance with another aspect of the present invention, the scrambling logic circuit includes a scrambling n -length shift register having n elements and a second scrambling ternary logic device. The scrambling n -length shift register has outputs from two of the n elements that are provided to two inputs of the second scrambling ternary logic device. The output from the first scrambling ternary logic device is provided to an input of the n -length shift register and an output of the second scrambling ternary logic device is provided to an input of the first scrambling ternary logic device.

In accordance with another aspect of the present invention, in the n -length shift register, n is equal to five and the outputs from the third and fifth elements are input to the second ternary logic device.

In accordance with another aspect of the present invention, the scrambled ternary signal is descrambled with a descrambler. The descrambling device has a first descrambling ternary logic device and a descrambling logic circuit. The scrambled version of the ternary signal is input to the first descrambling ternary logic device and to the descrambling logic circuit. An output from the descrambling logic circuit is provided to the first descrambling ternary logic device. A descrambled ternary signal is provided on an output of the first descrambling ternary logic device.

The scrambler and descrambler used in the method of the present invention are related and use corresponding devices. In accordance with one aspect of the present invention, the scrambling logic circuit includes a scrambling n -length shift register having n elements and a second scrambling ternary logic device, the scrambling n -length shift register having outputs from two of the n elements that are provided to two inputs of the second scrambling ternary logic device, and wherein the output from the first scrambling ternary logic device is provided to an input of the n -length shift register and an output of the second scrambling ternary logic device is provided to an input of the first scrambling ternary logic device, and the descrambling logic circuit includes a descrambling n -length shift register having n elements and a second descrambling ternary logic device, the scrambling n -length shift register having outputs from two of the n elements that are provided to two inputs of the second descrambling ternary logic device, and wherein the output from the second descrambling ternary logic device is provided to an input of the first descrambling ternary logic device and the scrambled version of the ternary signal is input to the descrambling n -length shift register.

The present invention also includes corresponding apparatus for scrambling a ternary signal that can assume one of three states. The apparatus includes a first scrambling ternary logic device that implements a ternary logic function, sc , the first scrambling ternary logic device having a first and second input and an output. The apparatus also includes a scrambling logic circuit having an input and an output. The ternary signal is input to the first input of the first scrambling ternary logic device, the output of the scrambling logic circuit is input to the second input of the first scrambling ternary logic device and the output of the first scrambling ternary logic device is provided to the input of the scrambling logic circuit.

As mentioned earlier, the ternary logic function, sc , implemented by the scrambling ternary logic device satisfies the following equations: (1) $A\ sc\ B=C$, where A is the ternary signal, B is the output from the scrambling logic circuit and C is the output from the first scrambling ternary logic device; (2) $C\ sc\ B=A$, if C and B were input to the first scrambling ternary logic device; and (3) $A\ sc\ C=B$; if A and C were input to the first scrambling ternary logic device.

A scrambled ternary signal is provided on the output of the first scrambling ternary logic device.

The ternary logic function, sc , used in the apparatus can also be defined by one of truth tables previously set forth with respect to sc .

In accordance with another aspect of the present invention, the scrambling logic circuit in the scrambler includes a scrambling n -length shift register having n elements and a second scrambling ternary logic device. The scrambling n -length shift register having outputs from two of the n elements that are provided to two inputs of the second scrambling ternary logic device. The output from the first scrambling ternary logic device is provided to an input of the

5

n-length shift register and an output of the second scrambling ternary logic device is provided to an input of the first scrambling ternary logic device.

Apparatus to descramble the scrambled ternary signal is also provided. The descrambler includes a first descrambling ternary logic device that implements the ternary logic function, sc . The first descrambling ternary logic device has a first and second input and an output. The descrambler has a descrambling logic circuit having an input and an output. The scrambled ternary signal is input to the first input of the first descrambling ternary logic device and to the input of the descrambling logic device. The output of the descrambling logic device is input to the second input of the first descrambling ternary logic device. A descrambled ternary signal is provided on the output of the first descrambling ternary logic device.

As was the case with the method of the present invention, the scrambler and the descrambler of the present invention have corresponding structures. Thus, if the scrambler includes a ternary logic device and a scrambling logic circuit, the descrambler also includes a ternary logic device and a descrambling logic circuit that corresponds to the scrambling logic circuit. In accordance with one aspect of the present invention, the scrambling logic circuit includes a scrambling n-length shift register having n elements and a second scrambling ternary logic device, the scrambling n-length shift register having outputs from two of the n elements that are provided to two inputs of the second scrambling ternary logic device, and the output from the first scrambling ternary logic device is provided to an input of the n-length shift register and an output of the second scrambling ternary logic device is provided to an input of the first scrambling ternary logic device. The descrambling logic circuit includes a descrambling n-length shift register having n elements and a second descrambling ternary logic device, the scrambling n-length shift register having outputs from two of the n elements that are provided to two inputs of the second descrambling ternary logic device, and the output from the second descrambling ternary logic device is provided to an input of the first descrambling ternary logic device and the scrambled version of the ternary signal is input to the descrambling n-length shift register.

The present invention also provides method and apparatus for scrambling and descrambling multi-value signals that can assume one of x states, wherein x is greater than or equal to 4. The method and apparatus used to scramble and descramble multi-value signals is similar to that previously discussed with respect to ternary signals. The method and apparatus used to scramble and descramble multi-value signals involves the use of a multi-value logic device that implements a multi-value logic function, fc , and a scrambling logic circuit. Generally, the multi-value logic device is substituted for the ternary logic device in the methods and apparatus previously discussed to implement the scrambling and descrambling of multi-value signal. Further, the multi-value logic function, fc , satisfies the same equations previously set forth: (1) $A fc B=C$, where A is the multi-value signal, B is the output from the scrambling logic circuit and C is the output from the first scrambling multi-value logic device; (2) $C fc B=A$, if C and B were input to the first scrambling multi-value logic device; and (3) $A fc C=B$; if A and C were input to the first scrambling multi-value logic device.

Also, the multi-value logic function, fc , can also satisfy one of the following truth tables:

6

In1	In2			
	0	1	2	3
0	0	3	2	1
1	3	2	1	0
2	2	1	0	3
3	1	0	3	2

In1	In2			
	0	1	2	3
0	1	0	3	2
1	0	3	2	1
2	3	2	1	0
3	2	1	0	3

In1	In2			
	0	1	2	3
0	2	1	0	3
1	1	0	3	2
2	0	3	2	1
3	3	2	1	0

In1	In2			
	0	1	2	3
0	3	2	1	0
1	2	1	0	3
2	1	0	3	2
3	0	3	2	1

It is noted that the truth tables set forth above are extendable to cases where multi-value signals that can assume five or more values are being scrambled and descrambled. The generic n-value logic function is defined by the following truth table and by variations thereof:

In 1	In2							
	0	1	2	3	n-2	n-1
0	0	n-1	n-2	2	1
1	n-1	n-2	n-3	1	0
2	n-2	n-3	n-4	0	n-1
...
...
...
n-2	2	1	0	4	3
n-1	1	0	n-1	3	2

DESCRIPTION OF THE DRAWINGS

Various other objects, features and advantages of the present invention will become fully appreciated as the same becomes better understood when considered in conjunction with the accompanying drawings, wherein:

FIG. 1 illustrates a block diagram of the sending side of a digital communication system describing the general position of a coder;

FIG. 2 is a block diagram of the receiving side of a digital communication system describing the general position of a decoder;

FIG. 3 is a diagram and truth table of binary scrambling function;

FIG. 4 illustrates a known application of a binary scrambler consisting of a binary shift register and binary Exclusive Or functions;

FIG. 5 illustrates a known application of a binary descrambler consisting of a binary shift register and binary Exclusive Or functions that can recover the original signal from a scrambled binary sequence;

FIG. 6 illustrates a diagram illustrating the ternary scrambling and descrambling properties and apparatus of the present invention;

FIG. 7 illustrates a diagram showing an embodiment of a binary ROM of the present invention that can be used to achieve ternary scrambling properties of the present invention;

FIG. 8 is a diagram showing an embodiment of the present invention that can be used to generate scrambled ternary signals of the present invention;

FIG. 9 is a diagram showing an embodiment of the present invention that can generate a binary representation of a signal from a ternary signal;

FIG. 10 is a diagram showing an embodiment of the present invention to scramble a ternary signal sequence;

FIG. 11 is a diagram showing an embodiment of the present invention to descramble a scrambled ternary signal sequence;

FIG. 12 is a diagram showing an embodiment of the n-value scrambling function of the present invention;

FIG. 13 is a diagram showing an embodiment of the present invention to generate a ternary spread spectrum signal sequence;

FIG. 14 is a block diagram showing an embodiment of the present invention to generate a spread spectrum ternary signal sequence from which the original ternary signal can be recovered by ternary scrambling of the coded sequence with the original pre-determined ternary sequence used to create the coded ternary sequence;

FIG. 15 is a block diagram showing an embodiment of the present invention that recover the original ternary signal from a spread spectrum ternary signal sequence;

FIG. 16 is a diagram showing a 4-value scrambling and descrambling realization of the present invention;

FIG. 17 is a block diagram showing an embodiment of the present invention to generate a spread spectrum 4-value signal sequence from which the original 4-value signal can be recovered by 4-value scrambling of the coded sequence with the original pre-determined 4-value sequence used to create the coded 4-value sequence; and

FIG. 18 is a block diagram of a composite ternary scrambling and descrambling system consisting of an odd number (3) of consecutive individual ternary scrambling devices, with each of these individual devices having a known secondary ternary signal as input. The first individual ternary scrambling device has also the to be scrambled ternary signal as input. The other ternary scrambling devices have the output of the preceding scrambling device as primary input. The output of the last scrambling device of scrambling devices is the output of the composite ternary scrambling system. If the number of scrambling devices is odd, the shown composite scrambling system also acts as the descrambling system, thus recovering the original ternary input.

DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a digital transmission system. The input signal 10 can be from a variety of information sources, such as voice, video, graphics or data. The signal is converted to

digital form by A/D converter 12. Typically, the signal is coded by a coder 14. The signal is modulated by a modulator 16 and then transmitted.

FIG. 2 illustrates a digital receiving system. The signal transmitted by the transmission system is received and demodulated by a demodulator 17. The signal is decoded by a decoder 18. The signal can then be converted by a D/A converter 20.

FIG. 3 illustrates a known binary scrambling function that is typically used to scramble signals in a binary scrambling system. The binary scrambling function is known as the exclusive or function. It is also known as the modulo-2 adder. This function is also used in binary descrambling.

The state table for the binary scrambling function is illustrated at 30. This state table is the exclusive (XOR) function.

In digital communications, the coder 14 often performs scrambling functions and the decoder often performs a corresponding descrambling function. The scrambling is performed for a variety of reasons, as previously discussed. FIG. 4 illustrates a known binary scrambler and FIG. 5 illustrates a known binary descrambler. In FIG. 4, a binary sequence is input to the XOR device 40. An output from the XOR device 40 is provided to a n-length shift register 42. In the case of FIG. 4, n is equal to five, so there are five elements 44 to 48 in the n-length shift register 42. Two outputs from the n-length shift register 42 are provided to a second XOR device 50. The outputs from the n-length shift register 42 are from the final element 48 and from an intermediate element 46. The output from the second XOR device 50 is provided to the first XOR device 40. A scrambled signal is provided at the output of the first XOR device 40 on Line 5.

FIG. 5 illustrates the descrambler that corresponds to the scrambler of FIG. 4. Thus, the descrambler of FIG. 5 can be used to descramble the signal scrambled by the system of FIG. 4. The scrambled signal is input on Line 5 to a first XOR device 60 and to a descrambling n-length shift register 62. In the case of FIG. 5, n is equal to five, so there are five elements 63 to 67 in the shift register 62. The output from elements 64 and 66 are provided to a second XOR device 68. The output from the second XOR device 68 is provided to an input to the first XOR device 60. A descrambled signal is provided at the output of the first XOR device 68.

These binary scrambling and descrambling structures are known. The shift registers may have any number of elements. It is also known that the outputs from any of the intermediate elements from the shift register may be used or alternatively, only the output from the final stage can be used.

Today's systems, such as the ones illustrated in FIGS. 4 and 5, are binary systems, so that binary signals that can assume one of two values are processed. Binary systems have limitations when compared to ternary systems or multi-value systems that use signals that can assume one of three and one of many states, respectively. By way of example only, a ternary signal can hold more information than a binary signal, and therefore potentially provides a system with greater throughput.

In view of the limitations inherent in binary scrambling and descrambling now present in the prior art, the present invention provides a new method and apparatus to conduct ternary and multi-value scrambling and descrambling of ternary and multi-value signals.

There is currently no method that allows for the creation of scramblers and descramblers consisting of elements that would directly conduct higher value (3-value, 4-value, . . . m-value) scrambling functions that also act as descrambling functions. The general purpose of the invention is to provide a new method for scrambling and descrambling of ternary and

multi-value signals that has many of the advantages of the binary scramblers mentioned heretofore.

Binary scrambling is often designated as Modulo-2 addition. Modulo-3, however, can not serve the purpose of a ternary scrambling/descrambling function. A different approach is needed.

One aspect of the present invention is illustrated in FIG. 6. FIG. 6 illustrates three truth tables or logic tables that implement ternary logic functions that are useful in achieving an executable ternary or multi-value scrambling/descrambling function. The truth table shows as possible inputs A the most left column at the left side of the vertical line of the table and all possible inputs B as the upper row, on top of the horizontal line of the truth table. The value of output C is determined by the number found in the truth table at the intersecting virtual lines, drawn horizontally through a selected value of A and vertically through a selected value for B. In accordance with one aspect of the present invention, the truth tables illustrated in FIG. 6 are used to provide ternary scrambling as shown in FIG. 6 and for multi-value scrambling as shown in FIG. 12.

As illustrated in FIG. 6, each of the truth tables 70, 71 and 72 satisfies the equations:

- (1) $A \text{ sc } B=C$, where A and B are inputs to a ternary logic device implementing the function, sc, and C is an output from the ternary logic device;
- (2) $C \text{ sc } B=A$, if C and B where input to the ternary logic device; and
- (3) $A \text{ sc } C=B$; if A and C were input to the ternary logic device; and

Thus, the logic function associated with each truth table 70, 71 and 72 are designated sc1, sc2 and sc3, respectively. Each of the logic functions, however, satisfies the equations set forth above. Further, when sc is used, it is understood to designate any of the ternary logic functions sc1, sc2 or sc3.

Ternary and multi-value scrambling can be executed mechanically, electronically or optically. In digital communication systems scrambling is mainly executed electronically. The advantage of ternary and multi-value digital signals is in their better use of the transmission spectrum or bandwidth compared to binary signals. The actual processing of the numbers for scramblers and descramblers can take place in binary digital electronic systems.

A dedicated ternary electronic scrambling system consisting of a digital Read Only Memory (ROM) circuit 80 is shown in FIG. 7. The inputs A and B to the scrambling truth table form combined an address to a memory location in the ROM circuit. Thus, the signal provided on A might form the first part of an address and the signal provided on B might form the second part of the address. The content of the memory location corresponds with the equivalent value at the corresponding ternary truth table. Thus, the output of the truth table, C, is provided at the output of the ROM 80. As such, any of the truth tables 70, 71 or 72 can be implemented by a ROM 80. For example, the truth table 82 is implemented by the ROM 80.

A digital-to-analog converter, synchronized by an external clock, can generate the ternary or multi-value signal, as shown in FIG. 8. In FIG. 8, a binary input is provided to the D/A converter 90. The input signal can assume one of three binary values: 00 (or 0), 01 (or 1) and 10 (or 2). The D/A converter 90 converts the input signal to an analog signal, or a ternary signal, that can assume one of three values: 0, 1 and 2.

At the receiving side the incoming ternary or multi-value signal can be converted to binary representation by an analog-to-digital circuit, as shown in FIG. 9. In FIG. 9, the operation is the reverse as just describer with respect to FIG. 8. The

incoming analog or ternary signal can assume one of three values: 0, 1 and 2. The A/D converter 92, outputs one of three binary signals: 00 (or 0), 01 (or 1) and 10 (or 2).

General programmable micro-processors or digital signal processors can also be programmed to execute the ternary or multi-value scrambling/descrambling methods.

It is an object of the present invention to provide a 3-value or ternary scrambling function or method and apparatus using a ternary logic device that implements one of a set of ternary logic functions. The ternary logic device has two inputs A and B and one output C. A, B and C each can have one out of three different values, for example, 0, 1 or 2. However, the general requirement for the values of A, B and C is that there are 3 distinct values that each A, B and C can assume and these values may symbolically be represented in a number of ways, such as by 0, 1, or 2 or by -, 0 and +.

FIG. 10 illustrates a ternary scrambler in accordance with one aspect of the present invention. A ternary signal 100 is provided on an input of a first ternary logic device 102. The first ternary logic device 102 provides an output to the input of an n-length shift register 104. The variable n may be any length, but in the case of FIG. 10 is illustrated as being five. Thus, there are five elements 106 to 110 in the shift register 104.

An output from the final element 110 of the shift register 104 and from an intermediate element 108 is provided to the inputs of a second ternary logic device 112. In FIG. 10, outputs from the third element 108 and the final element 110 are used, but one of ordinary skill in the art will appreciate that outputs from other elements (or taps) in the shift register 104 can also be used and that other configurations of the shift register and the logic devices can be used.

The output from the second ternary logic device 112 is provided to an input of the first ternary logic device 102. A scrambled ternary signal is provided at the output of the first ternary logic device 102.

In FIG. 10, the ternary input sequence is illustrated as 1 1 2 0 1 0 0 2 0 2. If the initial content of the shift register 104 is 0 0 0 0, then the scrambled output signal is 2 2 1 2 1 0 1 0 2 0. Of course, the final output depends on the initialization of the shift register 104.

Any of the ternary logic functions illustrated in FIG. 6 can be used to implement the first ternary logic device 102 and the second ternary logic device 112. As previously discussed, the method is such that ternary inputs A and B to the ternary logic function generate a ternary output C. The additional property of the logic function is that if the ternary inputs are C and A, the output is B. Further, if the ternary inputs are C and B, the ternary output from the logic function is A.

In accordance with another aspect of the present invention, the scrambling function has the dual property of also performing the descrambling function. Thus, the ternary logic function used to scramble a ternary signal is also used to descramble the scrambled ternary signal. A descrambling circuit is illustrated in FIG. 11. The descrambling circuit corresponds to the scrambling circuit. Thus, if the scrambler has a five element shift register with an intermediate output being provided from the third element in the shift register, the descrambling circuit will have a corresponding structure. Thus, the descrambler will also have a five element shift register with an intermediate output being provided from the third element in the shift register. Similarly, if two ternary logic devices are used in the scrambler, then two ternary logic devices are used in the descrambler. Also, if a single ternary logic device is used in the scrambler, then a single ternary logic device is used in the descrambler.

11

Referring to FIG. 11, a scrambled ternary signal is input to a first ternary logic device 120 and to an n-length shift register 122. The n-length shift register 122 has five elements 124 to 128, the same number as in the shift register in the scrambler of FIG. 10. The output from the final element 128 and the output from the third element 126 of the n-length shift register are output to a second ternary logic device 130. The output from the second ternary logic device 130 is input to the first ternary logic device 120. A descrambled signal is provided at the output of the first ternary logic device 120.

FIG. 11 illustrates a scrambled ternary input sequence of 2 1 2 1 0 1 0 2 0 being input to the descrambler. Assuming that the shift register is initialized to 0 0 0 0 0, the descrambled ternary output is 1 1 2 0 1 0 0 2 0 2. This is the same ternary sequence that was input to the scrambler of FIG. 10.

The present invention is also applicable to multi-value signals that can assume one of x states wherein x is equal to or greater than four. In this case, as illustrated in FIG. 12, a multi-value logic function is used. A truth table 140 illustrates one of the available multi-value logic functions, sc, that can be used. For n-value logic, the value of m is n-1. Thus, if 4-value logic is used, m is equal to three. Once again, the truth table must satisfy the equations: (1) $A \text{ sc } B=C$; (2) $C \text{ sc } B=A$ and (3) $A \text{ sc } C=B$, where A and B are the inputs to a multi-value logic device and C is the output from the ternary logic device. As before, equations (2) and (3) are interpreted to be if B and C and A and C, respectively, were applied to a multi-value logic device.

As previously mentioned, there are truth tables other than the one 140 illustrated in FIG. 12 that can be used to implement a multi-value scrambler in accordance with the present invention. Other truth tables for applicable multi-value logic functions can be derived by moving the top p rows down a number p and the lower p rows are moved to the top of the truth table. Thus, for example, if p is equal to one, then the top row can be moved down one row and the bottom row can be moved to the top row. This process can be cycled through until duplicate truth tables are generated. In this way, n n-value commutative scrambling/descrambling logic functions can be generated.

The scrambling circuit and the descrambling circuit illustrated in FIGS. 10 and 11 can be used to implement multi-value signal scrambling and descrambling. The devices implementing the ternary logic functions that are illustrated in FIGS. 10 and 11 are simply replaced with the multi-value logic functions described in FIG. 12. The operation of the scrambler and descrambler circuits of FIGS. 10 and 11 are the same whether ternary or higher multi-value signals are being scrambled and descrambled.

FIG. 13 illustrates another method of scrambling a ternary or a higher multi-value signal. In this method, the signal to be scrambled is provided to an input of a device that implements a ternary or multi-value logic function. Another known, pre-determined ternary or multi-value sequence is input to the other input of the device that implements a ternary or multi-value logic function. The device implements any of the logic functions described with respect to FIG. 6 or 10. Once again, the logic function must satisfy the equations: (1) $A \text{ sc } B=C$; (2) $C \text{ sc } B=A$ and (3) $A \text{ sc } C=B$, as previously discussed.

Referring to FIG. 13, the ternary digital signal at line 150 is to be scrambled with a known sequence to create a ternary spread spectrum signal. The signal sequence is 2 0 1 0, and is provided to one input of the logic device. The known, pre-determined sequence that is applied to the other input of the logic device is illustrated on line 152. That sequence is 2 0 0 1 0 2 2 1. The known, pre-determined sequence has a higher clock frequency than the signal to be scrambled. In the case of

12

FIG. 13, the frequency of the known, pre-determined signal is eight times faster than the frequency of the signal to be scrambled. It is easily seen that while the signal to be scrambled maintains a certain value or state during a finite time, the known sequence has eight states and achieves a spreading factor of 8.

A logic table illustrated at 154 is used in the example illustrated in FIG. 13 to scramble the signal. Thus, the logic device that the signal at line 150 and the signal at line 152 are applied to implements a logic function defined by the logic table 154. The scrambled signal can be recovered by applying the scrambled signal and the known, pre-determined sequence to a device that implements the same multi-value logic function that was used in the scrambling procedure.

FIG. 14 illustrates a system that generates a spread spectrum ternary scrambled signal. This system can also be used to generate the scrambled signal of FIG. 13. A scrambling device 160 implements any of the ternary logic functions previously discussed, for example, with respect to FIG. 6. One of the available ternary logic functions that the device 160 can implement is illustrated in the truth table 162. As previously discussed, a slow changing ternary signal that is to be scrambled or spread is input at 164 to the device 160. A fixed sequence of more rapidly changing ternary signals is input at 166 to the device 160. A clock 168 synchronizes the process. A scrambled ternary signal is output at 170 of the device 160.

This spread spectrum or scrambling device can also be used with higher multi-value signals. In this case, a higher, multi-value function, such as those previously discussed with respect to FIG. 10, is used.

FIG. 15 illustrates a system that can recover a signal from a spread spectrum ternary scrambled signal. A descrambling device 180 implements one of the ternary logic functions previously discussed. In this case, the logic function 182 is implemented, although any of the previously described ternary logic functions, for example, those described in FIG. 6, can also be implemented. The same ternary logic function used to scramble the signal is used to descramble the signal.

The scrambled ternary signal is input at 184 to the device 180. The known, pre-determined fixed sequence of more rapidly changing ternary signals is input at 186 to the device 180. A clock is input at 188 to the device 180. A descrambled ternary signal is provided at the output 190 of the device 180.

FIG. 16 illustrates four logic functions—fs1, fs2, fs3, and fs4—that can be used when processing four-state signals. Each of these functions can be created using the steps described with respect to FIG. 12. Further, each of these functions must satisfy the following equations: (1) $A \text{ fc } B=C$; (2) $C \text{ fc } B=A$ and (3) $A \text{ fc } C=B$, as previously discussed. Each of these functions can be used in any of the scrambling, descrambling or spread spectrum technologies described herein. For example, each of the functions can be used in the circuits of FIGS. 10 and 11.

The scrambling procedure for a ternary signal, as described with respect to FIGS. 13 and 14, can also be applied to higher, multi-value signals. FIG. 17 illustrates the application of the scrambling procedure to scramble a four-state signal. The ternary signal at line 200 is to be scrambled. The signal sequence is 3 1 0 2, and is provided to one input of a logic device. The known, pre-determined sequence that is applied to the other input of the logic device is illustrated on line 202. That sequence is 0 1 2 0 3 3 2 1 0 3 1 2. For spread spectrum applications, it is preferred that the known, pre-determined sequence have a higher frequency than the signal to be scrambled, as is illustrated in FIG. 13.

13

A logic table illustrated at **204** is used in the example illustrated in FIG. **17** to scramble the signal. Thus, the logic device that the signal at line **200** and the signal at line **202** are applied to a logic device that implements a logic function defined by the logic table **204**. The scrambled signal can be recovered by applying the scrambled signal and the known, pre-determined sequence to a device that implements the same multi-value logic function that was used in the scrambling procedure. In FIG. **17**, the known sequence on line **202** has a clock speed of 12 times the signal to be scrambled and spread on line **200**.

FIG. **18** illustrates another ternary scrambling system. The system has an odd number of individual scramblers **210**, **212** and **214**. The inputs to first scrambler **210** are provided with the signal to be scrambled and with a first known ternary input. The inputs to the second scrambler **212** are provided with the output from the first scrambler **210** and with a second known ternary input. The inputs to the third scrambler **214** are provided with the output from the second scrambler **212** and with a third known ternary input. Each of the scramblers **210**, **212** and **214** implements one of the ternary logic functions previously discussed. In the example of FIG. **18**, the logic function that is implemented is shown in logic table **216**. Note that any of the previously discussed logic functions can be used. Further, the scramblers can implement different ternary logic functions. The scrambled signals can be descrambled with a descrambler that uses the same logic devices that implement the same logic functions and having the same known, pre-determined sequences as inputs.

It is noted that this ternary scrambling method is not an extension of the binary scrambling method. Binary scrambling is basically a Modulo-2 arithmetical operation. Considering Modulo-3 addition, it is clear that addition of 2 ternary numbers is not the same as Modulo-3 subtraction. So ternary signals, scrambled with Modulo-3 addition cannot be recovered by again applying Modulo-3 addition.

It is an object of the present invention to provide one or more composite ternary scrambling methods that consist of a ternary shift register, taps in designated cells of the ternary shift register that connect to ternary scrambling functions and that will establish a self synchronizing ternary scrambler method that will create a scrambled ternary digit sequence that can be descrambled to its original ternary sequence.

It is another object of the present invention to provide a m-value (with m being an integer greater than 3) scrambling function or method with two m-value inputs A and B (with A and B having values that can be represented by integers 0, 1, 2, . . . , m-1) and a m-value output C (having one of the same values as possible for A and B). The method is such that m-value inputs A and B generate an m-value output C. The additional property of the method is that if the m-value inputs are C and A the m-value output is B and if the m-value inputs are C and B the output is m-value A.

It is another object of the present invention to provide one or more composite m-value scrambling methods that consist of a m-value shift register, taps in designated cells of the m-value shift register that connect to m-value scrambling functions and that will establish a self synchronizing m-value scrambler method that will create a scrambled m-value digit sequence that can be descrambled to its original m-value sequence.

It is another object of the present invention to provide a method to create a ternary Direct Sequence Spread Spectrum sequence from an initial ternary digital signal by applying a second, longer ternary sequence and applying the ternary scrambling method to the initial and the secondary ternary digital sequences.

14

It is another object of the present invention to provide a method to recover the initial ternary sequence from a scrambled Direct Sequence Spread Spectrum sequence by applying the ternary scrambling function to the second, longer ternary sequence and the ternary Direct Sequence Spread Spectrum sequence.

Another novel application is the creation of higher value scrambling functions.

Another novel application is the creation of 4-value or higher value coded signals such as applicable in spread spectrum coding and as shown in FIG. **17**. The 4-value coded spread spectrum signal can be recovered by again applying the 4-value scrambling method on the coded signal with the pre-determined 4-value sequence with which the original signal was coded.

It is another object of the present invention to provide a method to create a m-value Direct Sequence Spread Spectrum sequence from an initial m-value digital signal by applying a second, longer m-value sequence and applying the m-value scrambling method to the initial and the secondary m-value digital sequences.

It is another object of the present invention to provide a method to recover the initial m-value sequence from a scrambled Direct Sequence Spread Spectrum sequence by applying the m-value scrambling function to the second, longer m-value sequence and the m-value Direct Sequence Spread Spectrum sequence.

It is another object of the present invention to increase the security of scrambling a ternary digital signal by applying an odd number of consecutive scrambling stages of which the secondary input is a known ternary signal and the input to the first ternary scrambler is the to be scrambled ternary signal and the primary input to the consecutive ternary scramblers is the output of the preceding ternary scrambler as shown in FIG. **18**.

It is another object of the invention to provide a recovery or descrambling system of the signal scrambled by a system like or similar to the ternary scrambling system as shown in FIG. **18**, which is the system as shown in FIG. **18**. Only ternary scrambling systems like shown in FIG. **18**, with an odd number of scrambling stages can act as their own descramblers.

It is another object of the present invention to increase the security of scrambling an m-value (with m and integer greater than 3) digital signal by applying an odd number of consecutive m-value scrambling stages of which the secondary input is a known m-value signal and the input to the first m-value scrambler is the to be scrambled m-value signal and the primary input to the consecutive m-value scramblers is the output of the preceding m-value scrambler.

It is another object of the invention to provide a recovery or descrambling system of the signal scrambled by an m-value scrambling system comprised of an odd number of consecutive m-value scramblers with known m-value inputs. Such an m-value descrambling system is the system which created the scrambled m-value signal, only if that scrambling system consists of an odd number of m-value scramblers.

Other objects and advantages of the present invention will become obvious to the reader and it is intended that these objects and advantages are within the scope of the present invention. To the accomplishment of the above and related objects, this invention may be embodied in the form illustrated in the accompanying drawings, attention being called to the fact, however, that the drawings are illustrative only, and that changes may be made in the specific applications illustrated.

15

With respect to the descriptions and drawings of the invention then, it is to be realized that the application, formatting, selection, configuration, implementation and realization of the scrambler functions depend upon their application and are deemed readily apparent to one skilled in the art, and all equivalent relationships to those illustrated in the drawings and described in this document are intended to be encompassed by the present invention.

Therefore, the foregoing is considered as illustrative only of the principles of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact configurations and operation shown and described, and accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

The invention claimed is:

1. A method of descrambling a sequence of p scrambled n -state symbols with $n > 2$ and $p > 1$ into a sequence of p descrambled n -state symbols, an n -state symbol being able to assume one of n states, comprising:

inputting a first scrambled n -state symbol of the sequence of p scrambled n -state symbols on a first input of a descrambling n -state function;

inputting a second n -state symbol on a second input of the descrambling n -state function;

generating by a processor of a descrambled n -state symbol in accordance with the descrambling n -state function, wherein a truth table representing the descrambling n -state function is implemented in a memory that is accessed by the processor;

wherein a relationship between the first scrambled n -state symbol which may be called A , the second n -state symbol which may be called B and the descrambled n -state symbol which may be called C is defined by the n -state truth table that is commutative and self reversing and that satisfies the following equations for all possible states of A and B :

$$A \text{ sc } B=C; \quad (1)$$

$$C \text{ sc } B=A; \text{ and} \quad (2)$$

$$A \text{ sc } C=B; \text{ and} \quad (3)$$

repeating the previous steps until all symbols of the sequence of p scrambled n -state symbols have been descrambled by the processor.

2. The method of claim 1, further comprising:

generating the second n -state symbol on an output of an n -state Linear Feedback Shift Register.

3. The method of claim 1, wherein a lowest of n states is a first state and the descrambled n -state symbol does not have the first state when first scrambled n -state symbol and the second n -state symbol have a same state.

4. The method of claim 1, wherein the sequence of p scrambled n -state symbols has been created by scrambling a sequence of p n -state symbols by a scrambling method that applies the descrambling n -state logic function.

5. The method of claim 1, wherein n is an odd integer.

6. The method of claim 1, wherein the processor is part of a communication system.

7. An apparatus for descrambling a plurality of scrambled n -state symbols including a first scrambled n -state symbol, each n -state symbol enabled to assume one of n states with $n > 2$, comprising:

a descrambling device having a first and a second input and an output, the first input enabled to receive a signal

16

representing the first scrambled n -state symbol, the second input enabled to receive a signal representing a second n -state symbol and the output providing a signal representing a descrambled n -state symbol;

wherein a relationship between the first scrambled n -state symbol which may be called A , the second n -state symbol which may be called B and the descrambled n -state symbol which may be called C is determined by a commutative self reversing n -state logic function sc , that satisfies the following equations for all possible states of A and B :

$$A \text{ sc } B=C; \quad (1)$$

$$C \text{ sc } B=A; \text{ and} \quad (2)$$

$$A \text{ sc } C=B; \text{ and} \quad (3)$$

wherein the descrambling device includes a memory that implements a truth table that defines the commutative self reversing n -state logic function sc .

8. The apparatus as claimed in claim 7, further comprising: an n -state Linear Feedback Shift Register (LFSR) including an output that provides the signal representing the second n -state symbol.

9. The apparatus as claimed in claim 7, wherein the first scrambled n -state symbol and the second n -state symbol are represented by a first and a second plurality of binary signals.

10. The apparatus as claimed in claim 7, wherein the commutative self reversing n -state logic function is realized by implementing its truth table in a memory.

11. The apparatus as claimed in claim 7, further comprising a corresponding scrambling apparatus, including:

a scrambling device, having a first input enabled to receive a signal representing a first n -state symbol, a second input enabled to receive a signal representing the second symbol, and an output enabled to provide the first scrambled n -state symbol;

wherein the scrambling device implements the commutative self reversing n -state logic function sc .

12. The apparatus of claim 11, wherein the corresponding scrambler has an identical structure as the descrambler.

13. The apparatus of claim 7, wherein the descrambler is part of a communication system.

14. The apparatus of claim 7, wherein a signal representing the first scrambled n -state symbol is part of a spread spectrum signal.

15. A method for scrambling a sequence of p n -state symbols with $p > 1$, including a first n -state symbol, each n -state symbol enabled to assume one of n states with $n > 2$, each n -state symbol being represented by a signal, comprising:

inputting the first n -state symbol of the sequence of p n -state symbols on a first input of a scrambling n -state function;

inputting a second n -state symbol on a second input of the scrambling n -state function;

generating by a processor of a scrambled n -state symbol in accordance with the scrambling n -state function, wherein a truth table representing the scrambling n -state function is implemented in a memory that is accessed by the processor;

17

wherein a relationship between the first n-state symbol which may be called A, the second n-state symbol which may be called B and the scrambled n-state symbol which may be called C is defined by the n-state truth table that is commutative and self reversing and that satisfies the following equations for all possible states of A and B:

$$A \text{ sc } B=C; \quad (1)$$

$$C \text{ sc } B=A; \text{ and} \quad (2)$$

$$A \text{ sc } C=B; \text{ and} \quad (3)$$

repeating the previous steps until all symbols of the sequence of p n-state symbols have been scrambled by the processor.

18

16. The method of claim **15**, further comprising: inputting the scrambled n-state symbol on an input of an n-state Linear Feedback Shift Register.

17. The method of claim **15**, wherein a lowest of n states is a first state and the scrambled n-state symbol does not have the first state when first scrambled n-state symbol and the second n-state symbol have a same state.

18. The method of claim **15**, wherein the processor is part of a communication system.

19. The method of claim **15**, wherein a signal representing the scrambled n-state symbol is part of a spread spectrum signal.

* * * * *