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(54) EPITAXIAL DEPOSITION OF DOPED SEMICONDUCTOR MATERIALS

(75) Inventor: **Matthias Bauer**, Phoenix, AZ (US)

(73) Assignee: **ASM America, Inc.**, Phoenix, AZ (US)

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(58) **Field of Classification Search** .... None
See application file for complete search history.

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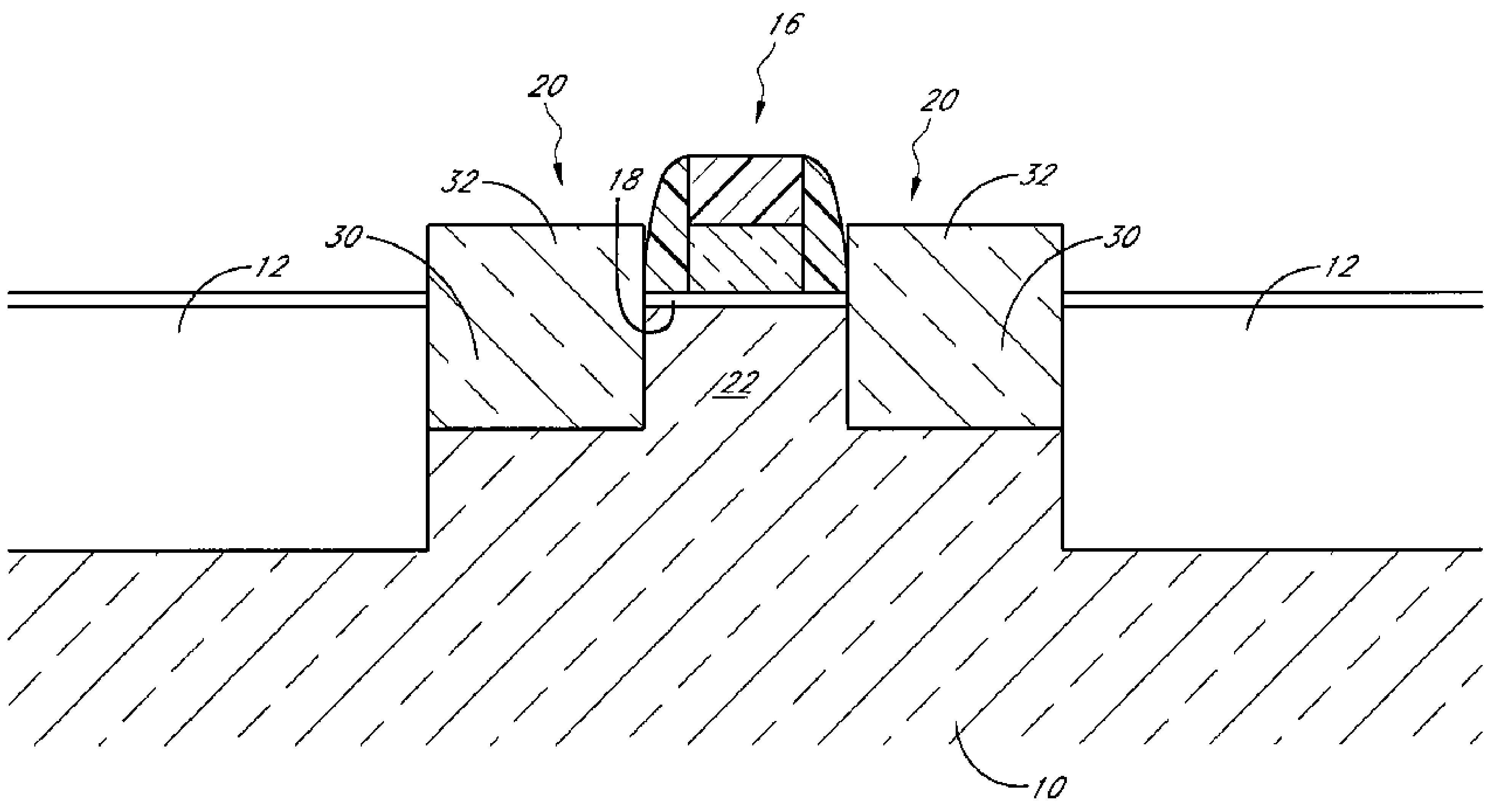
Primary Examiner—Matthew S Smith
Assistant Examiner—Shaka Scarlett
(74) *Attorney, Agent, or Firm*—Knobbe Martens Olson & Bear LLP

(57) ABSTRACT

A method for depositing a carbon doped epitaxial semiconductor layer comprises maintaining a pressure of greater than about 700 torr in a process chamber housing a patterned substrate having exposed single crystal material. The method further comprises providing a flow of a silicon source gas to the process chamber. The silicon source gas comprises dichlorosilane. The method further comprises providing a flow of a carbon precursor to the process chamber. The method further comprises selectively depositing the carbon doped epitaxial semiconductor layer on the exposed single crystal material.

39 Claims, 7 Drawing Sheets



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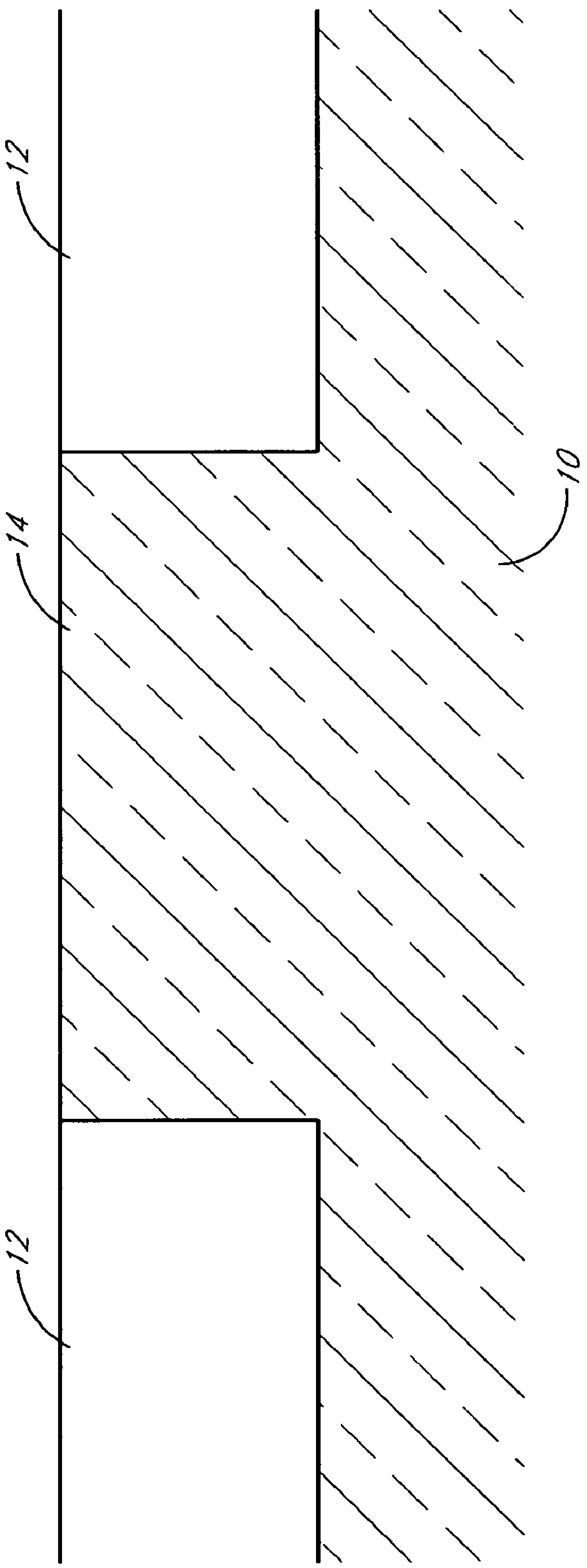

FIG. 1

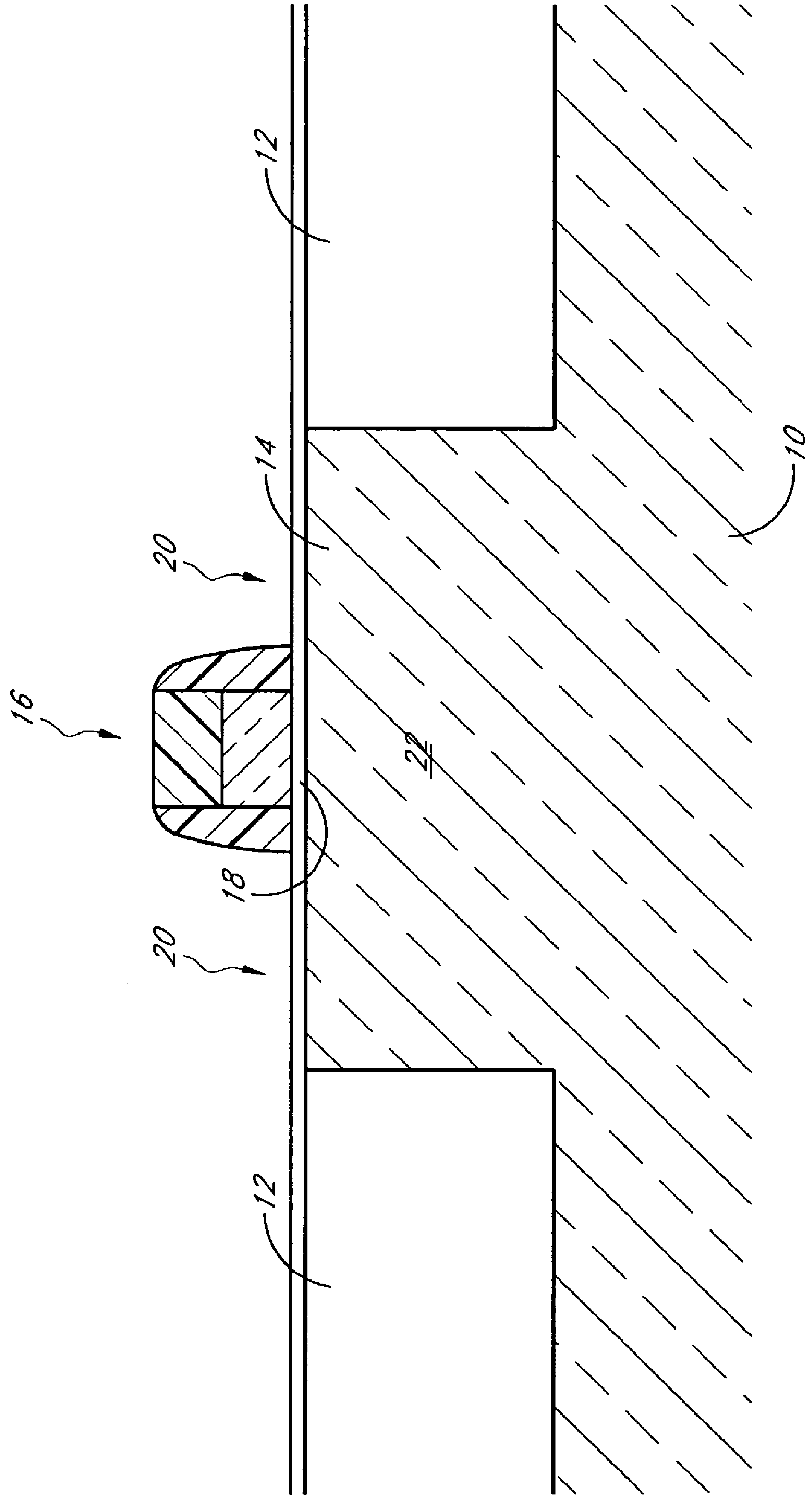

FIG. 2

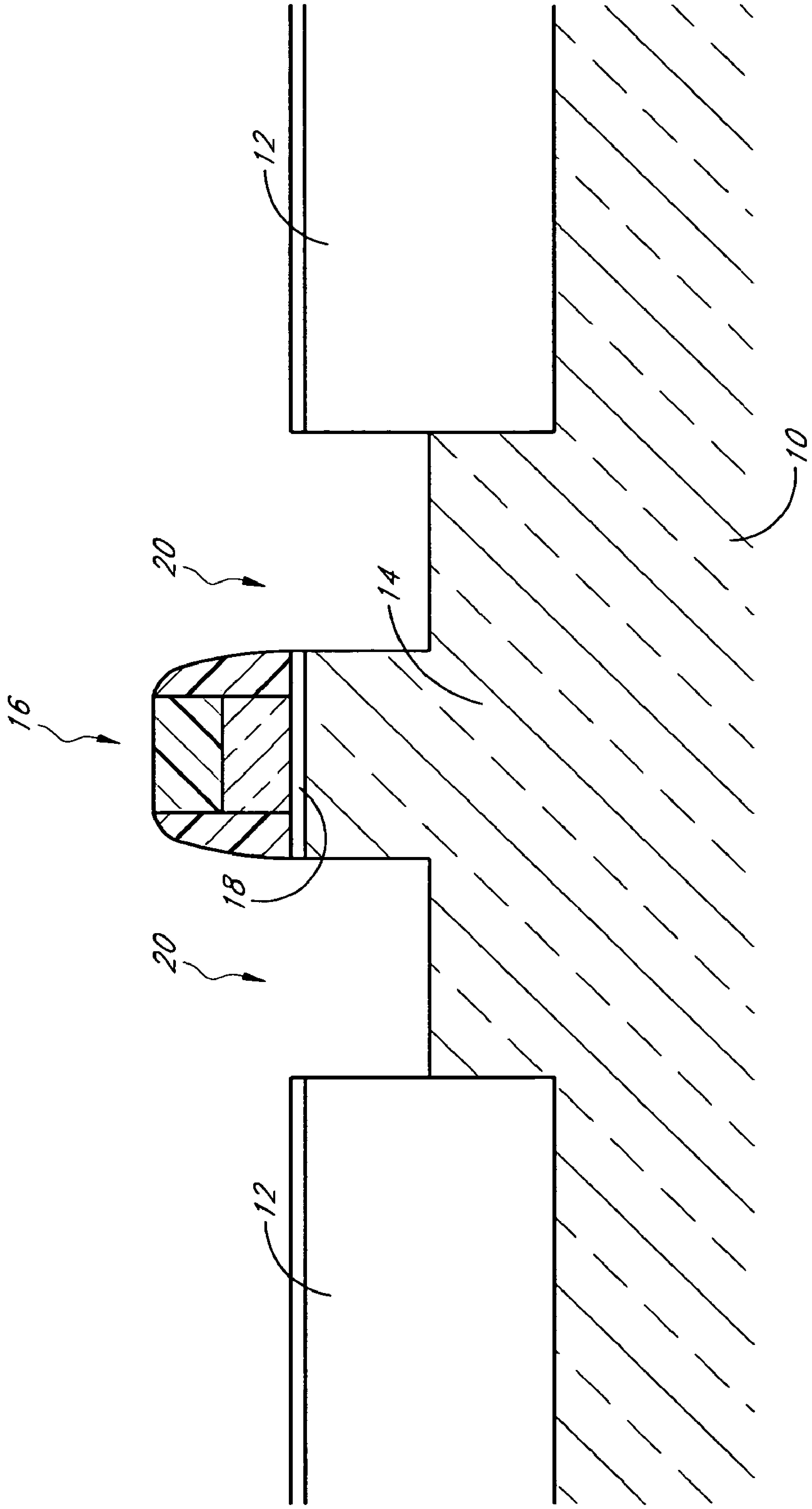

FIG. 3

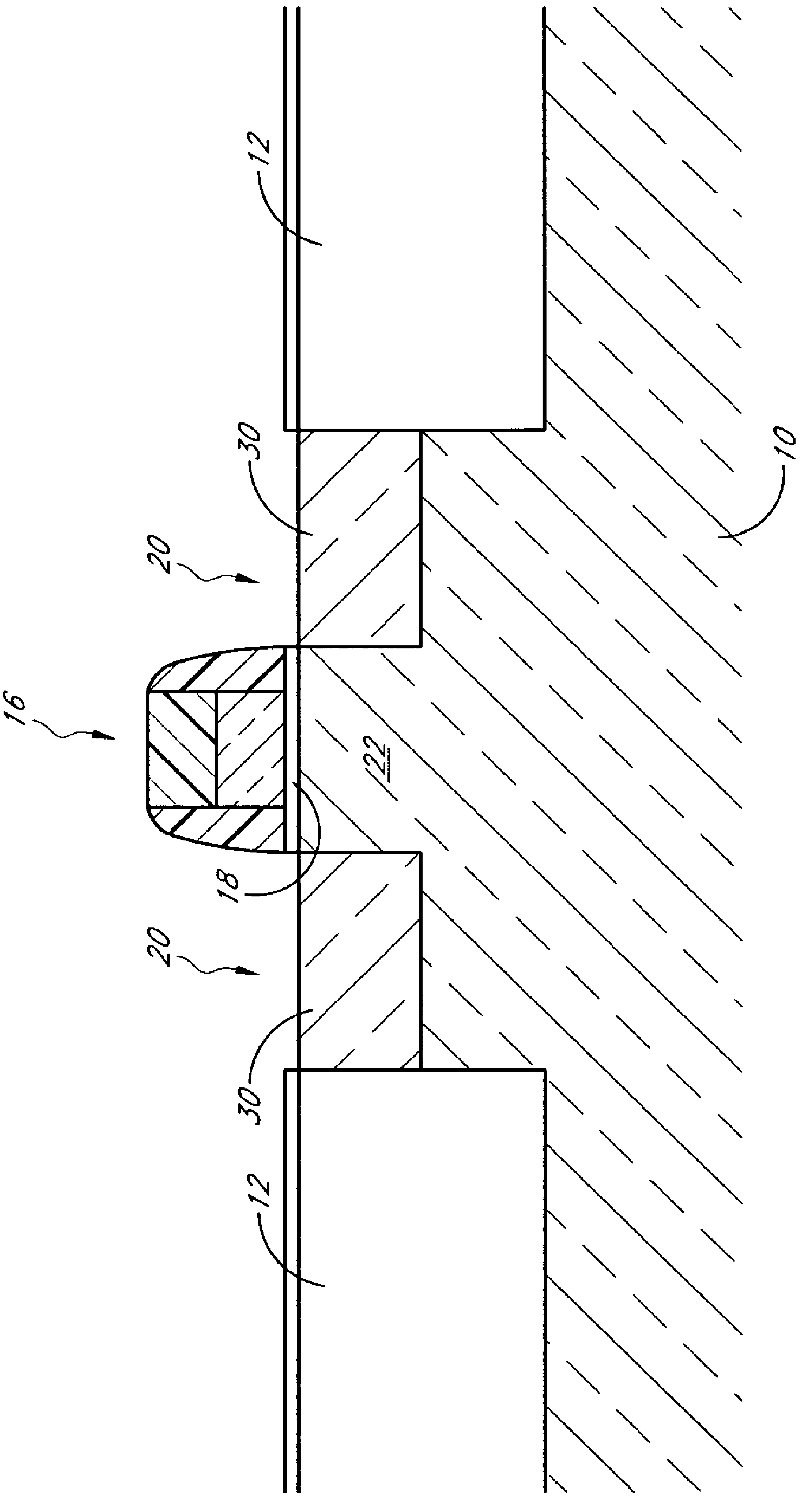

FIG. 4

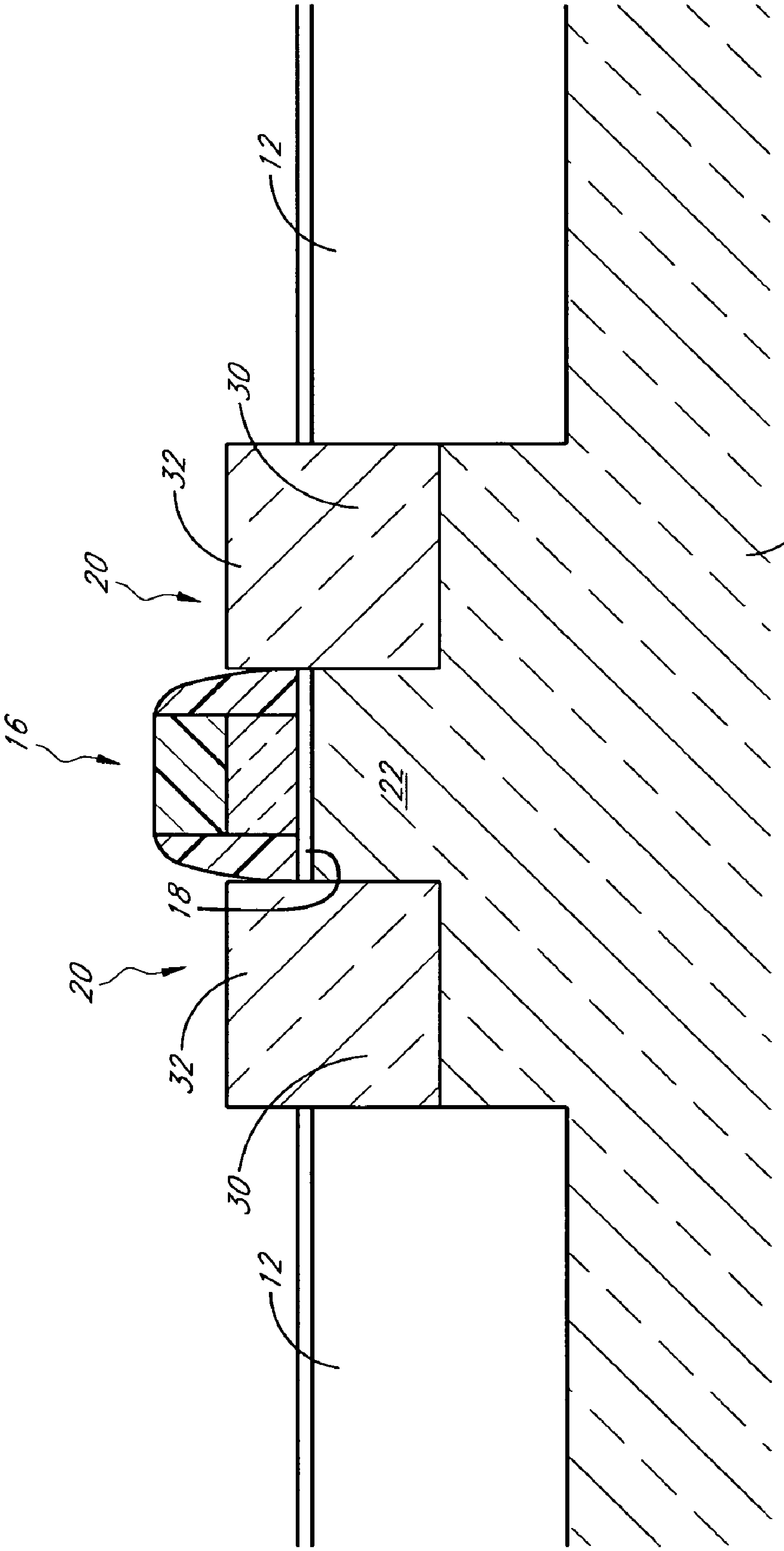

FIG. 5

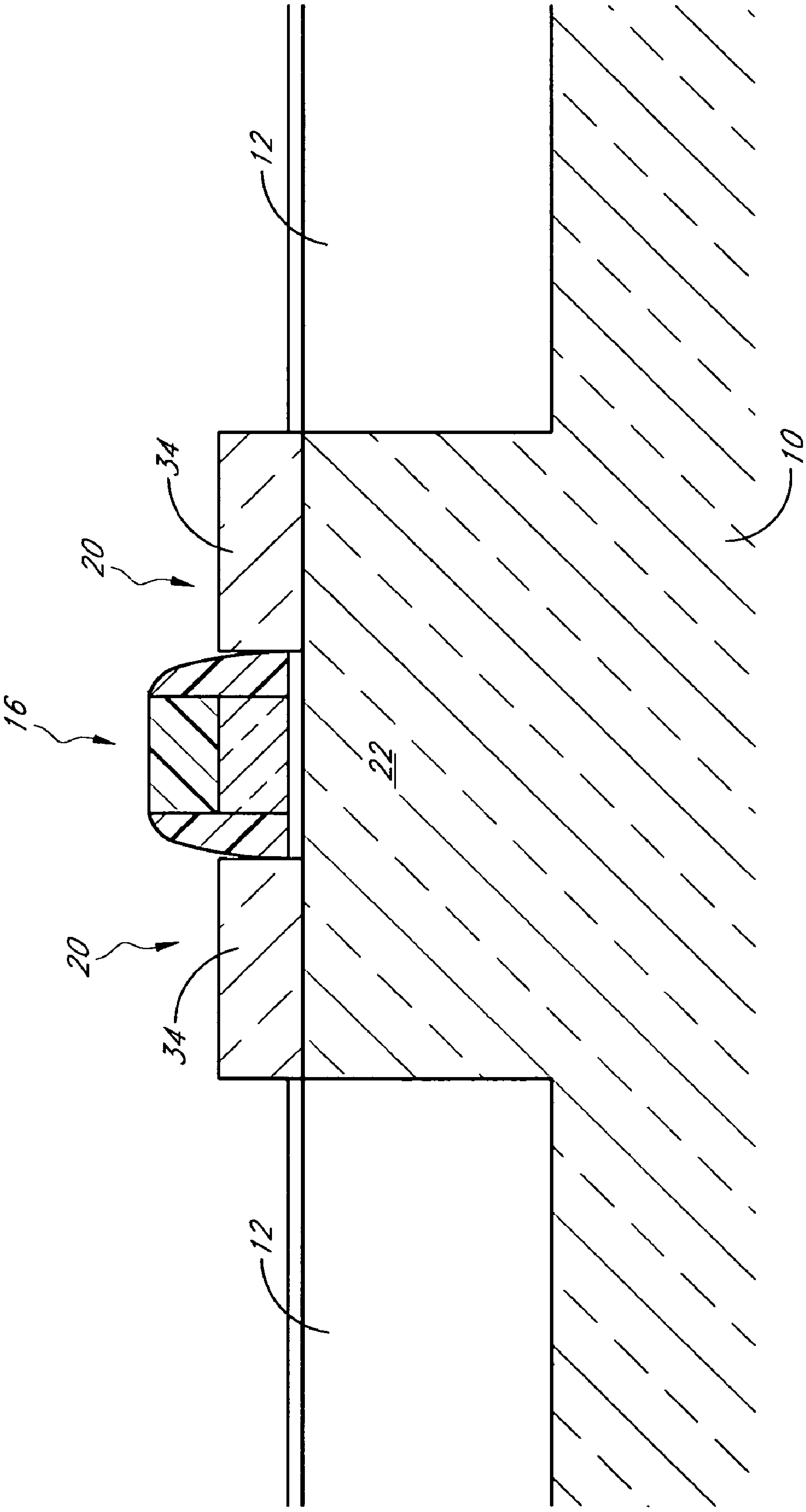

FIG. 6

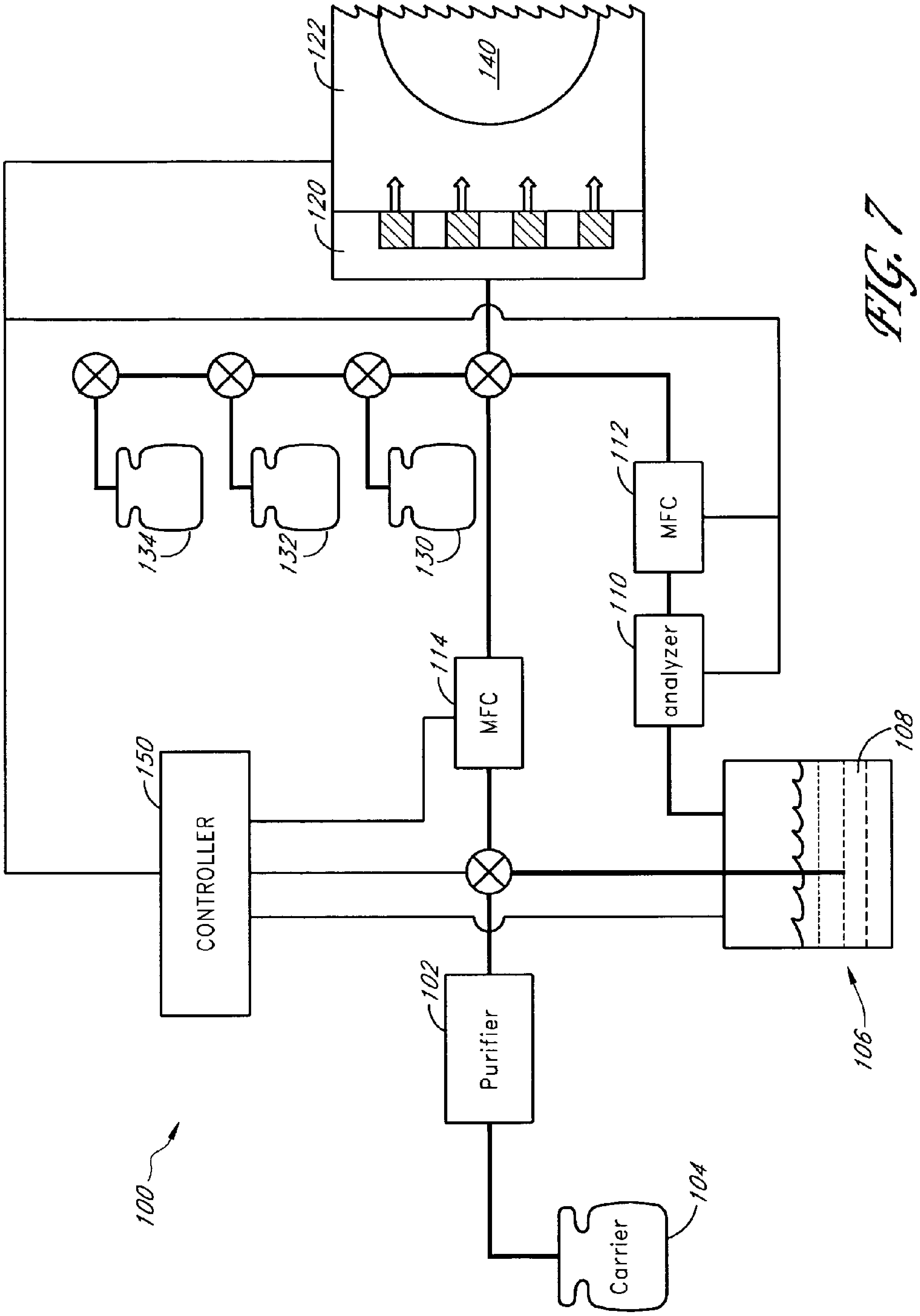
122
140
120
134
132
130
112
MFC
110
analyzer
114
MFC
150
CONTROLLER
108
106
102
Purifier
100
104
Carrier

FIG. 7

EPITAXIAL DEPOSITION OF DOPED SEMICONDUCTOR MATERIALS

PRIORITY APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application 60/754,569 (filed 22 Dec. 2005), the entire disclosure of which is hereby incorporated by reference herein.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. patent application Ser. No. 11/113,829 (filed 25 Apr. 2005;); U.S. patent application Ser. No. 11/343,275 (filed 30 Jan. 2006;); U.S. patent application Ser. No. 11/343,264 (filed 30 Jan. 2006;); and U.S. patent application Ser. No. 11/343,244 (filed 30 Jan. 2006. The entire disclosure of all of these related applications is hereby incorporated by reference herein.

FIELD OF THE INVENTION

The present invention relates generally to epitaxial deposition, and more particularly to in situ selective epitaxial deposition of carbon-doped semiconductor materials.

BACKGROUND OF THE INVENTION

A variety of methods are used in the semiconductor manufacturing industry to deposit materials onto surfaces. For example, one of the most widely used of such methods is chemical vapor deposition ("CVD"), in which atoms or molecules contained in a vapor deposit on a surface and build up to form a film. Deposition of silicon containing materials using conventional silicon sources and deposition methods on certain surfaces, such as insulators, is believed to proceed in several distinct stages. Nucleation, the first stage, occurs as the first few atoms or molecules deposit onto the surface and form nuclei. Nucleation is greatly affected by the nature and quality of the underlying substrate surface. During the second stage, the isolated nuclei form small islands that grow into larger islands. In the third stage, the growing islands begin coalescing into a continuous film. At this point, the film typically has a thickness of a few hundred angstroms and is known as a "transition" film. It generally has chemical and physical properties that are different from the thicker bulk film that begins to grow after the transition film is formed.

In some applications, it is desirable to achieve uniform or "blanket" deposition over both insulating (for example, silicon oxide) and semiconductive (for example, silicon) surfaces. In other applications, it is desirable to deposit selectively on semiconductor windows exposed within fields of different materials, such as field isolation oxide. For example, heterojunction bipolar transistors are often fabricated using selective deposition techniques that epitaxially deposit single crystal semiconductor films only on active areas. Other transistor designs benefit from elevated source/drain structures, which provide additional silicon to be consumed by the source/drain contact process, thus leaving the performance of the resulting shallow junction device unaffected. Selective epitaxy on source/drain regions advantageously allows the number of subsequent patterning and etching steps to be reduced.

Generally, selective deposition takes advantage of differential nucleation during deposition on different materials. Selective deposition generally involves simultaneous etching and deposition of the material being deposited. The precursor of choice generally has a tendency to nucleate and grow more rapidly on one surface and less rapidly on another surface. For example, silane will eventually deposit silicon on both silicon oxide and silicon, but there is a significantly longer nucleation phase on silicon oxide. Thus, at the beginning of a nucleation stage, discontinuous films on oxide have a high exposed surface area relative to merged, continuous films on silicon. Accordingly, an etchant added to the process will have a greater effect upon the poorly nucleating film over oxide as compared to the rapidly nucleating film over silicon. The relative selectivity of a process is thus tunable by adjusting factors that affect the deposition rate (for example, precursor flow rate, temperature, and pressure) and the rate of etching (for example, etchant flow rate, temperature, and pressure). Changes in variables such as these generally result in differential effects upon etch rate and deposition rate. Typically, a selective deposition process is tuned to produce the highest deposition rate feasible on the window of interest while accomplishing little or no deposition in the field regions. Known selective silicon deposition processes include reactants such as silane and hydrochloric acid with a hydrogen carrier gas.

A variety of approaches have been used to make strained single crystalline silicon containing materials that have applications in the semiconductor industry. One approach involves developing the strain at the substrate level before the device (such as a transistor) is fabricated. For example, a thin single crystalline silicon layer can be provided with tensile strain by epitaxially depositing the silicon layer on a strain-relaxed silicon germanium layer. In this example, the epitaxially deposited silicon is strained because its lattice constant follows the larger lattice constant of the underlying silicon germanium. Tensile strained epitaxially deposited silicon typically exhibits increased electron mobility.

Another approach for fabricating strained silicon crystalline silicon containing materials is by substitutional doping, wherein the dopants replace silicon atoms in the lattice structure. For example, substitution of germanium atoms for some of the silicon atoms in the lattice structure of single crystalline silicon produces a compressive strain in the resulting substitutionally doped single crystalline silicon germanium material because the germanium atoms are larger than the replaced silicon atoms. Alternatively, tensile strain is provided in single crystalline silicon by substitutional doping with carbon, because carbon atoms are smaller than the silicon atoms that they replace.

BRIEF SUMMARY OF THE INVENTION

Disadvantageously, the use of etchants causes many selective deposition chemistries to produce slow deposition rates, such that some or all of the throughput gained by omitting patterning and etching steps is lost due to the slower deposition rate. Furthermore, substitutional doping is often complicated by the tendency for the dopant to incorporate interstitially in domains or clusters within the silicon, rather than by substituting for silicon atoms in the lattice structure. Therefore, improved methods for performing selective epitaxial deposition of doped semiconductor materials have been developed.

In one embodiment of the present invention, a method for depositing a carbon doped epitaxial semiconductor layer comprises maintaining a pressure of greater than about 700 torr in a process chamber housing a patterned substrate having exposed single crystal material. The method further comprises providing a flow of a silicon source gas to the process chamber. The silicon source gas comprises dichlorosilane. The method further comprises providing a flow of a carbon precursor to the process chamber. The method further comprises selectively depositing the carbon doped epitaxial semiconductor layer on the exposed single crystal material.

In another embodiment of the present invention, a method comprises positioning a patterned substrate in a process chamber. The patterned substrate has a plurality of exposed fields of semiconductor material defined by a field isolation oxide mask. The method further comprises providing a flow of $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$ to the process chamber, wherein $1 \leqq x \leqq 4$, and $0 \leqq y \leqq 3$, and $(x+y) \leqq 4$, and $0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups. The method further comprises providing a flow of a silicon source gas to the process chamber. The method further comprises selectively depositing a carbon doped epitaxial semiconductor material onto the plurality of exposed fields of semiconductor material. The process chamber is maintained at a pressure greater than about 500 torr during the deposition. The carbon doped epitaxial semiconductor material is deposited onto the plurality of exposed fields of semiconductor material at a rate greater than about 5 nm min^{-1}.

In another embodiment of the present invention, a method of forming a transistor device on a substrate in a reaction chamber comprises defining, on the substrate, a plurality of active areas among a plurality of shallow trench isolation elements. The method further comprises providing a flow of dichlorosilane into the reaction chamber. The method further comprises providing a flow of $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$ into the reaction chamber, wherein $1 \leqq x \leqq 4$, and $0 \leqq y \leqq 3$, and $(x+y) \leqq 4$, and $0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups. The method further comprises depositing a tensile strained Si:C material onto the active areas at a first deposition rate d_1. The first deposition rate d_1 is greater than about 5 nm min^{-1}. The method further comprises depositing a Si:C material onto the trench isolation elements at a second deposition rate d_2, wherein $d_1 \geqq 100\ d_2$.

In another embodiment of the present invention, an apparatus for depositing semiconductor materials comprises a source of dichlorosilane vapor. The apparatus further comprises a source of $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$ vapor, wherein $1 \leqq x \leqq 4$, and $0 \leqq y \leqq 3$, and $(x+y) \leqq 4$, and $0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups. The apparatus further comprises a carrier gas source. The apparatus further comprises a gas distribution network that connects the source of dichlorosilane vapor, the source of $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$ vapor, and the carrier gas source to a single wafer chemical vapor deposition chamber configured for deposition of semiconductor materials under atmospheric pressure. The apparatus further comprises a control system configured to deliver dichlorosilane vapor and $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$ vapor to the gas distribution network under conditions suited to selectively deposit a Si:C material on portions of a substrate within the deposition chamber without depositing on other portions of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the methods and structures disclosed herein are illustrated in the accompanying drawings, which are for illustrative purposes only. The drawings comprise the following figures, in which like numerals indicate like parts.

FIG. **1** is a cross-sectional view of an example silicon wafer substrate having a plurality of field isolation regions.

FIG. **2** is a cross-sectional view of the substrate of FIG. **1** after formation of a gate electrode over one of the active areas.

FIG. **3** is a cross-sectional view of the substrate of FIG. **2** after performing a selective etch step that removes exposed silicon.

FIG. **4** is a cross-sectional view of the substrate of FIG. **3** after refilling the recessed source/drain regions with a heteroepitaxial tensile strained n-doped Si:C film using a selective deposition process.

FIG. **5** is a cross-sectional view of the substrate of FIG. **4** after an optional extension of the selective deposition to form elevated source/drain regions.

FIG. **6** is a cross-sectional view of the substrate of FIG. **2** after selectively depositing a tensile strained n-doped Si:C film.

FIG. **7** is a schematic view of an apparatus employing a silicon source gas source, an etchant source, and a carrier gas source that can be used to deposit Si:C layers in accordance with an example embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Introduction.

Disclosed herein are exemplary embodiments of improved methods for performing selective epitaxial deposition of semiconductor materials, including in situ carbon-doped semiconductor materials. Certain of the CVD techniques disclosed herein produce semiconductor films with improved crystal quality, improved electrical activation of incorporated dopants, and improved growth rate. In certain embodiments, highly n-doped selective deposition is possible under atmospheric conditions using dichlorosilane as a silicon precursor, dopant hydrides, and optionally, HCl to improve selectivity. Carbon precursors, such as methylsilane (CH_3SiH_3), are optionally added to the process gas mixture to form films that include carbon. Deposition at pressures above the low pressure chemical vapor deposition ("LPCVD") and reduced pressure chemical vapor deposition ("RPCVD") pressure regimes, preferably greater than about 500 torr, more preferably greater than about 700 torr, and most preferably at atmospheric pressure, is optionally selective with both high dopant incorporation and high deposition rates.

The processes disclosed herein are useful for, among other things, depositing silicon containing films on a variety of substrates, but certain embodiments are particularly useful for deposition on "mixed substrates". As used herein, the term "mixed substrate" refers, in addition to its ordinary meaning, to a substrate that has two or more different types of surfaces. The surfaces are different from each other in one or more of a variety of different ways. For example, in certain applications the surfaces are made from different silicon containing materials, such as silicon, silicon nitride and silicon dioxide. Even in applications where the surfaces comprise the same element, the surfaces are still considered different if other properties are different, such as the surface electrical properties. For example, in a typical application, silicon containing layers are selectively formed over semiconductor materials while minimizing, and more preferably avoiding, deposition over adjacent dielectrics. Examples of typical dielectric materials include silicon dioxide, silicon nitride, metal oxide and metal silicate.

Mixed substrates include substrates having a first portion with a first surface morphology and a second portion with a second surface morphology. As used herein, "surface morphology" refers, in addition to its ordinary meaning, to the crystalline structure of the substrate surface. For example, a polycrystalline morphology is a crystalline structure that consists of a disorderly arrangement of orderly crystals and thus has an intermediate degree of order. The atoms in a polycrystalline material are ordered within the crystals, but the crystals themselves lack long range order with respect to one another. An amorphous morphology is a non-crystalline structure having a low degree of order because the atoms lack a definite periodic arrangement. Other surface morphologies include microcrystalline and single crystalline. Epitaxial films are characterized by a crystal structure and orientation that is identical to the substrate upon which they are grown, which is typically a single crystal morphology.

The single crystal morphology, which is particularly useful in many semiconductor applications, is a crystalline structure that has a high degree of order. More specifically, as used herein, the morphology descriptions "single crystal" and "single crystalline" refer, in addition to their ordinary meanings, to a predominantly large crystal structure having a tolerable number of faults therein. The crystallinity of a layer generally falls along a continuum from amorphous to polycrystalline to single crystalline; an ordinarily-skilled artisan is able to readily determine whether a crystal structure is considered single crystalline, despite a low density of faults. The atoms in a material with a single crystal morphology are arranged in a lattice-like structure that persists over relatively long distances (on an atomic scale).

Specific examples of mixed substrates include, for example, single crystal and polycrystalline; single crystal and amorphous; epitaxial and polycrystalline; epitaxial and amorphous; single crystal and dielectric; epitaxial and dielectric; conductor and dielectric; and semiconductor and dielectric. The term "mixed substrate" includes substrates having more than two different types of surfaces, and thus certain of the methods described herein for depositing silicon containing films onto mixed substrates having two types of surfaces are also applicable to mixed substrates having three or more different types of surfaces.

As used herein, the term "substrate" refers, in addition to its ordinary meaning, to either the workpiece upon which deposition is desired, or the surface exposed to deposition gases. Examples of substrates include a single crystal silicon wafer; a semiconductor on insulator ("SOI") substrate; or an epitaxial silicon, silicon germanium or III-V material deposited upon an underlying substrate. Substrates are not limited to wafers, and also include glass, plastic, or other substrates employed in semiconductor processing. Semiconductor processing is typically employed for the fabrication of integrated circuits, which entails particularly stringent quality demands, although such processing is also employed in a variety of other fields. For example, semiconductor processing techniques are often used in the fabrication of flat panel displays using a wide variety of technologies, as well as in the fabrication of microelectromechanical systems ("MEMS").

As used herein, "selective" deposition refers, in addition to its ordinary meaning, to a deposition process wherein deposition simultaneously occurs at two significantly different growth rates over two different surfaces. Deposition occurs over a first surface at a rate that is least 10× faster than the deposition rate over a second surface. Preferably, deposition occurs over a first surface at a rate that is least 100× faster than the deposition rate over a second surface. A "completely" selective deposition process typically refers to a process wherein deposition occurs over the first surface while there is no net deposition over the second surface. Other deposition ratios are used in other embodiments of selective deposition.

Deposition is suitably conducted according to various CVD methods, but the greatest benefits are obtained when deposition is conducted according to the CVD methods disclosed herein. The disclosed methods are suitably practiced by employing CVD, including plasma-enhanced chemical vapor deposition ("PECVD"), ultraviolet photo-assisted CVD, or thermal CVD. However, thermal CVD advantageously allows selective deposition to be achieved effectively with reduced risk of damaging substrates and equipment as compared to PECVD.

Typically, delivery of the precursor gases to the substrate surface is accomplished by introducing the gas mixture to a suitable chamber having the substrate disposed therein. In an example embodiment, the chamber is a single-wafer, single pass, laminar horizontal gas flow chamber that is radiantly heated. Suitable reactors of this type include the Epsilon™ series of single wafer reactors, which are commercially available from ASM America, Inc. of Phoenix, Ariz. While the methods disclosed herein are usable with alternative reactor configurations, such as a showerhead arrangement, benefits in increased uniformity and deposition rates have been found particularly effective in the horizontal, single-pass laminar gas flow arrangement of the Epsilon™ chambers, which use a rotating substrate. These advantages are particularly evident in processes that use low process gas residence times. Plasma products are optionally introduced, in situ or downstream of a remote plasma generator, but as noted above, thermal CVD is preferred.

Thermal CVD is conducted at a substrate temperature that is effective to deposit a silicon containing film over the substrate. Preferably, thermal CVD is conducted at a temperature less than 700° C. For example, in a preferred embodiment thermal CVD is conducted in the range of about 350° C. to about 675° C., more preferably between about 500° C. and about 660° C., and most preferably between about 600° C. and about 650° C. For example, in one embodiment thermal CVD is conducted between about 630° C. and about 650° C. These temperature ranges are tunable to account for the realities of actual manufacturing, such as the thermal budget, the deposition rate, the chamber volume (including single wafer and batch reactors), the preferred total and partial pressures, and the like. The substrate is heated using a variety of methods, such as resistive heating and lamp heating.

Incorporation of dopants into selectively-deposited silicon containing films by CVD using dichlorosilane is preferably accomplished by in situ doping using dopant precursors. Preferred precursors for n-type electrical dopants include dopant hydrides, including n-type dopant precursors such as phosphine, arsenic vapor, and arsine. Silylphosphines $[(H_3Si)_{3-x}PR_x]$ and silylarsines $[(H_3Si)_{3-x}AsR_x]$ where $0 \leqq x \leqq 2$ and R=H and/or D are alternative precursors for phosphorous and arsenic dopants. Such dopant precursors are useful for the preparation of preferred films as described below, preferably phosphorous-doped silicon and Si:C films. As used herein, "Si:C" represents materials that comprises silicon, carbon and optionally, other elements such as dopants. "Si:C" is not a stoichiometric chemical formula per se, and thus is not limited to materials that contain particular ratios of the indicated elements. However, in a preferred embodiment the carbon-doped silicon films have a carbon content of less than about 3%.

Example Process Integration.

FIG. **1** illustrates a example silicon wafer substrate **10**. The substrate **10** optionally includes an epitaxial layer formed over a wafer or an SOI substrate. Field isolation regions **12** have been formed by conventional shallow trench isolation ("STI") techniques, defining active areas **14** in windows among the STI elements. Alternatively, other suitable methods are used to define field insulating material, including local oxidation of silicon ("LOCOS") and a number of variations on LOCOS or STI. Typically, several active areas are defined simultaneously by STI across the substrate **10**, and the STI often forms a web separating transistor active areas **14** from one another. In an example embodiment, the substrate is background doped at a level suitable for channel formation.

FIG. **2** illustrates the substrate **10** after formation of a gate electrode **16** over the active area **14**. In the example embodiment illustrated in FIG. **2**, the gate electrode **16** is illustrated as a traditional silicon electrode, surrounded by insulating spacers and cap layers, and separated from the underlying substrate **10** by a gate dielectric layer **18**. However, in other embodiments the transistor gate stack has other configurations. In some process flows, for example, the spacers are omitted. In the illustrated embodiment, the gate electrode **16** defines source/drain regions **20** on either side of the transistor gate electrode **16** within the active area **14**. The gate electrode **16** also defines a channel region **22** under the gate electrode **16** and between the source and drain regions **20**.

FIG. **3** illustrates the result of a selective etch step that removes exposed silicon. In an example embodiment, a reactive ion etch ("RIE") is used to enhance vertical sidewall definition and to reduce damage to exposed oxide and nitride materials, though it will be appreciated that the methods herein are applicable to sloped wall recesses. Preferably the depth of the recesses is less than the critical thickness of the layer to be deposited in the recess, although strain on the channel can also be obtained by depositing to a depth that is greater than the critical thickness. The "critical thickness" is the thickness at which a strained layer spontaneously relaxes under a particular set of conditions. As the etched exposed silicon is essentially the source/drain regions **20** of the active area **14**, this etch is referred to as a source/drain recess. In certain embodiments, a preliminary step of clearing the gate dielectric layer **18** over the source/drain regions **20** is optionally employed.

FIG. **4** shows the result of refilling the recessed source/drain regions **20** using a selective deposition process. For example, in certain embodiments a tensile strained n-doped Si:C film is deposited into the recessed source/drain regions **20** using the techniques disclosed herein. An example feed gas used to obtain such a deposition includes a mixture of dichlorosilane, a dopant hydride such as phosphine, CH_3SiH_3, and HCl. Advantageously, the selectively deposited, heteroepitaxial film **30** fills the source/drain regions **20** and exerts strain on the channel region **22**. In the illustrated embodiment, the heteroepitaxial film **30** is approximately flush with the surface of the channel region **22**. Before deposition, the exposed, recessed semiconductor surfaces are optionally cleaned, such as with an HF vapor or an HF last dip, thereby leaving a clean surface for epitaxy thereover.

FIG. **5** illustrates an optional extension of the selective deposition to form elevated source/drain regions **20** with the extended heteroepitaxial film **32**. As the portion of the heteroepitaxial film **30** below the surface of the channel region **22** exerts lateral stress on the channel region **22**, the extended heteroepitaxial film **32** above the surface of the substrate need not include as much or any lattice deviation from the natural silicon lattice constant. Accordingly, a carbon source gas is optionally tapered or halted for the portion of the selective deposition above the surface of the channel region **22**, while the dichlorosilane flow is continued. In such embodiments, electrical dopant source gases, particularly phosphine, can be continued during deposition of the extended heteroepitaxial film **32**.

The extended heteroepitaxial film **32** of FIG. **5** advantageously provides additional silicon material above the surface of the substrate **10**. In certain embodiments, through subsequent processing, insulating layers are deposited and contacts are made through the insulating film to the source and drain regions **20**. The additional silicon material facilitates formation of silicide contacts, which reduce contact resistance through the formation of ohmic contacts. Accordingly, nickel, cobalt or other metal is deposited into the contact hole and allowed to consume the excess silicon without disturbing electrical properties of shallow junctions for the underlying source/drain regions **20** in such embodiments.

FIG. **6** shows a modified embodiment in which the structure of FIG. **2** is subjected to selective deposition of a tensile strained n-doped Si:C film without the intervening source/drain recess process. In this case, the selective deposition raises the source/drain regions **20**, thereby providing excess silicon **34** to permit consumption by contact silicidation without destroying shallow junctions. Optionally, the dopants are omitted in embodiments wherein the entire excess silicon **34** is to be consumed by contact silicidation.

Advantageously, the selective nature of the tensile strained n-doped Si:C film obviates subsequent pattern and etch steps to remove excess deposition from over field regions. Even imperfect selectivity advantageously allows use of a timed wet etch to remove unwanted deposition over insulating surfaces, rather than requiring an expensive mask step. Furthermore, superior film quality is obtained at relatively high deposition rates despite relatively low temperatures, improving throughput. For example, certain process embodiments are used to form a base structure of a heterobipolar transistor ("HBT"). Other process embodiments are used to form an elevated source/drain ("ESD") structure, a recessed source/drain structure, a contact plug for dynamic random access memory ("DRAM") and/or static random access memory ("SRAM").

Deposition of Tensile Strained, n-Doped Si:C Films.

The lattice constant for single crystal silicon is about 5.431 Å, whereas single crystal carbon in the form of diamond has a lattice constant of about 3.567 Å due to the smaller size of carbon atoms as compared to silicon atoms. Accordingly, it is possible to introduce tensile strain into single crystalline silicon by substitutional doping with carbon. In addition, substitutional incorporation of smaller carbon atoms creates more room for large dopant atoms. For such a process, a small amount of organic silicon precursor, such as monomethyl silane, is added to the process chamber as a source for both silicon and carbon.

Tensile strained Si:C films advantageously exhibit improved electrical carrier mobility, and particularly hole mobility, in semiconductors, thereby improving device efficiency. When the Si:C films are deposited to a thickness that is less than the critical thickness, and a dopant hydride such as phosphine is added to the process flow, the deposited layer remains tensile strained and hole mobility is significantly improved, which is particularly advantageous in n-channel metal oxide semiconductor ("NMOS") applications. This is analogous to boron-doped silicon germanium films that are used in p-channel metal oxide semiconductor ("PMOS") devices.

Furthermore, use of phosphine to dope a Si:C film provides advantages that are not present even when other n-type dopants are used. For example, when a Si:C film is doped with phosphine, the tensile strain in the film is maintained, or is even increased slightly (for example, by about 0.2%). The presence of carbon in the Si:C lattice suppresses phosphorous dopant diffusion, thereby enabling films with sharp dopant profiles to be formed. It is difficult to grow films with sharp dopant profiles when other n-type dopants are used.

However, from a practical standpoint, selective epitaxial growth of low-resistance n-doped Si:C films presents challenges that are not present in the context of selective epitaxial growth of p-doped silicon germanium films. For example, Applicant has determined that substitutional carbon incorporation is enhanced by both lower deposition temperatures and higher growth rates. However, the growth rate for Si:C films decreases with decreasing deposition temperature. Furthermore, use of dichlorosilane as a silicon precursor for selective epitaxial growth of single crystal silicon films typically results in low growth rates, and is enhanced by use of relatively high deposition temperatures (for example, between about 800° C. and about 850° C.). Using conventional deposition techniques, supplying dichlorosilane as a silicon precursor at temperatures less than about 750° C. results in a chlorine-terminated surface, with only negligible desorption.

As disclosed herein, HCl is often used to enhance selectivity, particularly in processes using silicon precursors which do not lend themselves to selective growth, such as silane, Si_2H_6, Si_3H_8 and partially or fully chlorinated disilanes (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n \leqq 6$). Without being limited by theory, it is believed that presence of HCl in the reaction chamber during silicon deposition results in the etch products $SiCl_3H$ and $SiCl_4$. In this case, the etching of a nucleated silicon surface proceeds according to the following net reactions:

$$Si+3HCl \rightarrow SiCl_3H\uparrow+H_2\uparrow$$

$$Si+4HCl \rightarrow SiCl_4\uparrow+2H_2\uparrow$$

Mass changes due to these chemical reactions on the surface of the silicon substrate affect the concentration of the respective species at the substrate surface. Specifically, the concentration of the species at the substrate surface is governed by a balance between these chemical reactions and diffusion fluxes generated by concentration and temperature gradients.

Spectra obtained by residual gas analysis provides additional information on the successive reactions that produce the etch products $SiCl_3H$ and $SiCl_4$. Without being limited by theory, it is believed that these reactions are as follows:

$$Si+HCl \rightarrow {}^*SiCl+\tfrac{1}{2}H_2\uparrow$$

$$^*SiCl+HCl \rightarrow {}^*SiCl_2+\tfrac{1}{2}H_2\uparrow$$

$$^*SiCl_2+HCl \rightarrow SiCl_3H\uparrow$$

The asterisk symbol * indicates chemisorbed states of SiCl and $SiCl_2$ on the surface of the silicon substrate. The resulting $SiCl_3H$ does not remain on the substrate surface because it has a relatively low boiling point (about 32° C.) and a relatively high vapor pressure. Because there is a relatively large concentration of HCl in the gas phase about the silicon substrate, $SiCl_3H$ reacts with HCl to from $SiCl_4$ according to the following reaction:

$$SiCl_3+HCl \rightarrow SiCl_4+\tfrac{1}{2}H_2$$

This reaction occurs in the gas phase.

Both dichlorosilane and $SiHCl_3$ are suitable silicon precursors for epitaxial growth of single crystal silicon, according to the following reactions:

$$SiCl_2H_2 \rightarrow SiCl_2+H_2$$

$$SiCl_2H_2 \rightarrow SiHCl+HCl$$

$$SiHCl_3 \rightarrow SiCl_2+HCl$$

$$^*SiCl_2+H_2 \rightarrow Si(s)+2HCl\uparrow$$

The balance for whether deposition or etch occurs according to the following reaction

$$^*SiCl_2+H_2 \leftrightarrows Si(s)+2HCl,$$

and is determined by the ratio

$$\frac{[HC\ell]^2}{[SiC\ell_2][H_2]}.$$

In an example embodiment, this balance is tuned by holding the flow of dichlorosilane relatively constant while increasing the flow of HCl into the reaction chamber until selective deposition is achieved. In an alternative embodiment, the flow of H_2 is reduced to favor the etch process, or is increased to favor the deposition process. Reducing the flow of H_2 helps to improve precursor consumption by reducing dilution, increasing partial pressures of the etchants, and reducing gas velocity.

Other silicon precursors, such as silane, Si_2H_6, Si_3H_8 and partially or fully chlorinated disilanes (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n < 6$) are also suitable silicon precursors for epitaxial growth of single crystal silicon, especially when used as a component of a silicon precursor gas mixture that also comprises dichlorosilane. It will be appreciated that use of a silicon precursor gas mixture that comprises dichlorosilane advantageously enables the amount of HCl present in the reaction chamber to be reduced, thereby resulting in higher film purity, since commercially available HCl is typically has high contamination levels (for example, moisture) by semiconductor processing standards. The endothermic reaction of dichlorosilane in the absence of HCl turns into an exothermic reaction in the presence of HCl. In embodiments wherein the silicon source gas consists essentially of dichlorosilane, there is relatively little decomposition of the dichlorosilane at the reaction temperatures and pressures disclosed herein, thus resulting in relatively low precursor utilization. Adding one or more supplemental silicon sources to the reaction chamber, such as silane, Si_2H_6, Si_3H_8 and/or partially or fully chlorinated disilanes (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n < 6$), or replacing dichlorosilane with one or more of these supplemental silicon sources, causes the reaction to become more exothermic by tapping the energy stored in the silane, Si_2H_6, Si_3H_8 or partially or fully chlorinated disilane (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n < 6$) molecule. This allows the energetic barrier for precursor decomposition to be overcome more easily, thus resulting in better precursor utilization and higher growth rates.

For example, in certain embodiments, silane is used as a silicon precursor instead of dichlorosilane. In embodiments wherein about 75 sccm to about 100 sccm of silane is provided to the reaction chamber, the HCl flow is increased to between about 80 sccm and about 160 sccm. In such embodiments, the silane flow rate can be adjusted for a given HCl flow rate, or the HCl flow rate can be adjusted for a given silane flow rate. As described herein, in embodiments wherein silane is used as a silicon precursor instead of dichlorosilane, higher precursor utilization can be achieved, and therefore lower precursor flow rates can be used.

In certain embodiments, surface chlorine is removed using a dopant hydride such as PH_3 through the formation of HCl and PCl_3, which is a volatile etch product. Removal of surface chlorine advantageously improves growth rate as compared to intrinsic silicon growth according to the reactions set forth herein. Thus, when PH_3 is supplied to the reaction chamber, a portion of the PH_3 flow does not contribute to doping, but instead contributes to the formation of PCl_3. In such embodiments, PCl_3 is formed according to the following reaction:

$$*3SiCl_2+PH_3 \rightarrow 3Si(s)+PCl_3+3HCl\uparrow$$

As disclosed above, using a supplemental silicon source such as silane, Si_2H_6, Si_3H_8 and partially or fully chlorinated disilanes (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n < 6$) causes the reaction to become more exothermic. In embodiments wherein PH_3 is supplied to the reaction chamber, this enhances the formation of PCl_3, P_2 and P_4.

Without being limited by theory, in certain embodiments wherein a carbon doped film is deposited using a methylsilane such as CH_3SiH_3 as a carbon source, the deposition is believed to proceed according to the following reaction:

$$*3SiCl_2+CH_3SiH_3 \rightarrow 4Si(s)+C(s)+6HCl\uparrow$$

In one embodiment, a low resistivity single crystal silicon film comprises substitutionally doped carbon and an electrically active dopant, such as phosphorous. The carbon is preferably substitutionally doped at between 0.1% and 5%, more preferably between 0.5% and 2%, and most preferably between 0.8% and 1.2%. The level of substitutional doping is optionally determined using x-ray diffraction and the Kelieres/Berti relation. The film preferably has a resistivity of about 1.0 mΩ·cm or less, more preferably 0.7 mΩ·cm or less, and most preferably about 0.5 mΩ·cm or less.

In an example embodiment, a low resistivity single crystal silicon film is deposited at a temperature that is preferably between about 350° C. and about 675° C., more preferably between about 500° C. and about 660° C., and most preferably between about 600° C. and about 650° C. For example, in one embodiment the deposition is conducted between about 630° C. and about 650° C. Despite such low deposition temperatures, the film is preferably grown at greater than about 2 nm min^{-1}, more preferably at greater than about 5 nm min^{-1}, and most preferably at greater than about 8 nm min^{-1}. The thickness of the film is adjusted by controlling the deposition time; preferably the film has a thickness between about 20 nm and about 80 nm, and more preferably between about 25 nm and about 50 nm. The film preferably has a resistivity between about 0.4 mΩ·cm and about 1.1 mΩ·cm, and more preferably between about 0.5 mΩ·cm and about 1.0 mΩ·cm. The partial pressure of dichlorosilane in the reaction chamber is preferably between about 10 torr and about 50 torr, more preferably between about 20 torr and about 40 torr, and most preferably between about 25 torr and about 35 torr. Exemplary flow rates for the various components of the feed gas mixture are provided in Table A.

In this example, the total pressure of the reaction chamber is preferably greater than about 500 torr, more preferably greater than about 700 torr, and most preferably at about atmospheric pressure. While deposition at or near atmospheric pressure is contrary to most selective deposition processes, Applicant has found selective deposition in this pressure regime to be workable and advantageous for certain of the processes disclosed herein. In particular, deposition using certain of the processes disclosed herein advantageously results in a relatively high deposition rate and good levels of carbon incorporation.

TABLE A

gas mixture component	preferred flow rate range	example flow rate
dichlorosilane	200 sccm-500 sccm	300 sccm
H_2	1 slm-10 slm	5 slm
PH_3, 1% in H_2	100 sccm-300 sccm	200 sccm
CH_3SiH_3, 20% in H_2	50 sccm-70 sccm	60 sccm
HCl	10 sccm-40 sccm	12.5 sccm

As noted above, use of a silicon precursor gas mixture that comprises dichlorosilane advantageously enables the amount of HCl present in the reaction chamber to be reduced. Because introducing HCl into the reaction chamber also causes contamination to be introduced into the reaction chamber, reducing the about of HCl in the reaction chamber typically generally results in increased film purity.

Other process components are used in other embodiments. Specifically, depending on the characteristics of the film to be deposited, the process gas mixture comprises one or more precursors selected from the group consisting of silicon source, carbon source, and phosphorous source. Specific examples of such sources include: silane, Si_2H_6, Si_3H_8, partially or fully chlorinated disilanes (that is, $Si_2H_nCl_{6-n}$, wherein $1 \leqq n < 6$), and tetrasilane as silicon sources; carbon sources; monosilylmethane, disilylmethane, trisilylmethane, tetrasilylmethane and particularly methyl silanes such as monomethyl silane, dimethyl silane, trimethyl silane, tetramethylsilane, ethylsilane, diethylsilane, triethylsilane, tetraethylsilane, and methylethylsilane as sources of both carbon and silicon; and various dopant precursors as sources of electrically active n-type dopants such as phosphorous. In some embodiments, a carbon source comprises a chloromethylsilane of the formula $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$, wherein

$1 \leqq x \leqq 4$, and

$0 \leqq y \leqq 3$, and

$(x+y) \leqq 4$, and

$0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups.

In other embodiments, a carbon source comprises $H_3Si—CH_2—SiH_2—CH_3$ (1,3-disilabutane).

Chloromethylsilanes advantageously provide both a carbon source and an etchant source. Without being limited by theory, it is believe that because the carbon atoms in chloromethylsilanes are separated from each other by silicon atoms, chloromethylsilanes promote carbon incorporation on a molecular and atomic level. This reduces the tendency of the carbon atoms to bond together into carbon chains and clusters during deposition. Use of chloromethylsilanes also tend to enhance selectivity and increase film growth rate, while also enabling the carbon concentration in a deposited film to be manipulated without modifying the etchant flow rates. In an example embodiment, chloromethylsilanes are used in conjunction with a separate silicon source and a separate etchant for selective deposition of a Si:C film at atmospheric pressure.

Use of chloromethylsilanes advantageously enhance film uniformity by providing a carbon precursor having a decomposition rate similar to that of the silicon precursors and the etchants disclosed herein. Specifically, given certain processing conditions, such as certain deposition temperatures and pressures, use of precursors and etchants that decompose at similar rates under these conditions promotes film uniformity. The amount of chlorine and thus the weight of a particular chloromethylsilane affects the decomposition rate of that chloromethylsilane.

In a modified embodiment, helium is used instead of, or in addition to, H_2 as a main carrier flow. Such embodiments provide a more efficient decomposition of dichlorosilane into $SiCl_2$ and H_2, as described herein. The H_2 is not required for the silicon etch using HCl. In other embodiments, other inert gases that are used as a main carrier flow instead of H_2 include, but are not limited to, argon, neon, xenon and nitrogen.

Certain of the embodiments disclosed herein advantageously enable selective deposition of a low resistivity single crystal silicon film that comprises substitutionally doped carbon and an electrically active dopant. In certain embodiments, such films are grown at commercially useful rates between about 5 nm min^{-1} and about 14 nm min^{-1}. Use of a dopant hydride (such as PH_3) in combination with dichlorosilane increases the growth rate of the resulting film. Use of a high partial pressure of dichlorosilane advantageously generates enough etchant to obtain selective deposition without requiring a substantial amount of HCl to be added to the process. Certain of the methods disclosed herein are usable to selectively deposit n-doped Si:C films with good crystal quality, low resistivity (sheet resistance), low surface roughness, and low defect density.

Furthermore, micro-loading effects are also reduced when certain of the embodiments disclosed herein are used. In the context of selective deposition on a patterned wafer, micro-loading effects refer to local deposition pattern nonuniformities in growth rate and film composition within the patterned windows on the wafer surface. For example, faceting is a micro-loading effect that causes a thinning of the epitaxial layer around the edges of a selective deposition pattern. Faceting disadvantageously complicates self-aligned salicidation steps that are performed after an epitaxial deposition. In certain embodiments, reducing the deposition pressure and/or reducing the deposition temperature helps to reduce or eliminate micro-loading effects. In one embodiment, within a selected deposition window, less than 20% nonuniformity is present across the deposition window. Few if any loading effects are detectable across the wafer surface when certain of the embodiments disclosed herein are employed. In particular, embodiments using a silicon precursor that includes dichlorosilane, an n-type dopant, and an atmospheric pressure deposition environment have been found to be particularly effective in reducing loading effects. Nonuniformities were found to be about the same from window to window across the wafer surface despite differences in window sizes. Thus, the average nonuniformity for a window of x cm^2 will differ by less than about 5% from the average nonuniformity of a window with about ½xcm^2.

In certain embodiments, the methods disclosed herein are used to selectively deposit tensile strained Si:C films in recessed windows of a (100) silicon substrate. Typically, when a mask is aligned in the <110> direction to etch recessed windows in a (100) silicon substrate, the (111) surface is exposed. In certain configurations, selective deposition of tensile strained semiconductor films on the (111) surface results in an increased defect density in the films. However, by aligning the mask in the <100> direction to etch recessed windows in a (100) silicon substrate, the (111) surface is not exposed. Therefore, when certain of the methods disclosed herein are used to selectively deposit tensile strained Si:C films in recessed windows of a (100) silicon substrate, the mask is optionally rotated 45° such that it is aligned in the <100> direction, thereby preventing exposure of the (111) surface.

Example Reactor System.

FIG. **7** illustrates an example reactor system **100** employing a carrier gas, a silicon precursor, and an etchant gas. In one embodiment, the silicon precursor is dichlorosilane. As shown, a purifier **102** is positioned downstream of the carrier gas source **104**. Some of the inert gas flow is shunted to a vaporizer in the form of a bubbler **106**, from which the carrier gas carries vaporized dichlorosilane **108**. Alternatively, the dichlorosilane is heated to increase the vapor pressure of dichlorosilane in the space above the liquid, and the carrier gas picks up dichlorosilane as it passes through that space. In any case, downstream of the liquid reactant source container **106** is an analyzer **110** that determines, by measuring the speed of sound through the vapor, the reactant concentration of the flowing gas. Based upon that measurement, the setpoint for the software-controlled downstream mass flow controller ("MFC") **112** is altered by the analyzer **110**. Such analyzers are commercially available.

The flow through the MFC **112** merges with the main carrier gas through the main carrier gas MFC **114** and other reactants at the gas panel, upstream of the injection manifold **120** for the deposition chamber **122**. Alternatively, the flow can merge at any point within the reactor system **100** to supply the resulting feed gas to the substrate. An etchant gas source **130**, such as a source of chlorine vapor or hydrochloric acid vapor, is also provided. In the illustrated embodiment, a source for carbon **132** and a source for dopant hydride **134** are also provided.

As illustrated, the reactor system **100** also includes a central controller **150**, electrically connected to the various controllable components of the system **100**. The controller is programmed to provide gas flows, temperatures, pressures, and the like, to practice the deposition processes as described herein upon a substrate **140** housed within the reaction chamber **122**. The controller **150** typically includes a memory and a microprocessor, and may be programmed by software, hardwired or a combination of the two, and the functionality of the controller may be distributed among processors located in different physical locations. Accordingly, the controller **150** can also represent a plurality of controllers distributed through the system **100**.

SCOPE OF THE INVENTION

While the foregoing detailed description discloses several embodiments of the present invention, it should be understood that this disclosure is illustrative only and is not limiting of the present invention. It should be appreciated that the specific configurations and operations disclosed can differ from those described above, and that the methods described herein can be used in contexts other than selective epitaxy of doped semiconductor materials.

I claim:

1. A method for depositing a carbon doped epitaxial semiconductor layer, the method comprising:

maintaining a pressure of greater than about 700 torr in a process chamber housing a patterned substrate having exposed single crystal material and at least a second different exposed material;

providing a flow of a silicon source gas to the process chamber, wherein the silicon source gas comprises dichlorosilane;

providing a flow of a carbon precursor to the process chamber;

selectively depositing the carbon doped epitaxial semiconductor layer on the exposed single crystal material relative to the second exposed material at the pressure of greater than about 700 torr, thereby depositing the carbon doped epitaxial semiconductor layer on the exposed single crystal material at a rate greater than about 5 nm min^{-1}.

2. The method of claim **1**, further comprising providing a flow of an n-dopant hydride to the process chamber.

3. The method of claim **1**, further comprising providing a flow of hydrochloric acid (HCl) to the process chamber.

4. The method of claim **1**, further comprising providing a flow of hydrochloric acid (HCl) to the process chamber at a flow rate that is between about 10 sccm and about 160 sccm.

5. The method of claim **1**:

further comprising providing a flow of hydrochloric acid (HCl) to the process chamber at a flow rate that is between about 80 sccm and about 160 sccm; and

wherein the silicon source gas further comprises silane.

6. The method of claim **1**:

further comprising providing a flow of hydrochloric acid (HCl) to the process chamber at a flow rate that is between about 10 sccm and about 40 sccm; and

wherein the silicon source gas mixture consists essentially of dichlorosilane.

7. The method of claim **1**, further comprising providing a carrier to the process chamber, wherein the carrier is selected from the group consisting of hydrogen and helium.

8. The method of claim **1**, further comprising providing a carrier to the process chamber at a flow rate that is between about 1 slm and about 10 slm.

9. The method of claim **1**, wherein the silicon source gas further comprises silane.

10. The method of claim **1**, wherein the silicon source gas consists essentially of dichlorosilane.

11. The method of claim **1**, wherein the silicon source gas further comprises at least one of silane (SiH_4), trisilane (Si_3H_8), and partially or fully chlorinated disilanes ($Si_2H_nCl_{6-n}$ (wherein $1 \leqq n \leqq 6$)).

12. The method of claim **1**, wherein the silicon source gas has a partial pressure in the process chamber is between about 25 torr and about 35 torr.

13. The method of claim **1**, wherein the silicon source gas is provided to the process chamber at a flow rate that is between about 200 sccm and about 500 sccm.

14. The method of claim **1**, wherein the carbon precursor is provided to the process chamber at a flow rate that is between about 50 sccm and about 70 sccm.

15. The method of claim **1**, wherein the carbon precursor is selected from the group consisting of tetrasilylmethane ($C(SiH_3)_4$), methyl silane (CH_3SiH_3) and 1,3-disilabutane.

16. The method of claim **1**, wherein the carbon precursor comprises $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$, wherein $1 \leqq x \leqq 4$, and $0 \leqq y \leqq 3$, and $(x+y) \leqq 4$, and $0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups.

17. The method of claim **1**, further comprising providing a flow of an n-dopant hydride to the process chamber at a flow rate that is between about 100 sccm and about 500 sccm.

18. The method of claim **1**, further comprising providing a flow of phosphine (PH_3) to the process chamber.

19. The method of claim **1**, wherein the pressure maintained in the process chamber is atmospheric.

20. The method of claim **1**, wherein the carbon doped epitaxial semiconductor layer comprises between about 0.8% and about 1.2% substitutionally doped carbon in single crystal silicon.

21. The method of claim **1**, wherein carbon doped epitaxial semiconductor layer has a resistivity of less than about 0.7 Ω·cm.

22. The method of claim **1**, wherein carbon doped epitaxial semiconductor layer has a resistivity of less than about 0.5 mΩ·cm.

23. The method of claim **1**, wherein the patterned substrate is held at a temperature between about 630° C. and about 650° C. during deposition of the carbon doped epitaxial semiconductor layer.

24. The method of claim **1**, wherein the patterned substrate is held at a temperature between about 600° C. and about 660° C. during deposition of the carbon doped epitaxial semiconductor layer.

25. The method of claim **1**, wherein the patterned substrate is held at a temperature between about 600° C. and about 675° C. during deposition of the carbon doped epitaxial semiconductor layer.

26. The method of claim **1**, wherein the process chamber is a single wafer process chamber.

27. A method for depositing a carbon doped epitaxial semiconductor layer, the method comprising:

maintaining a pressure of greater than about 700 torr in a process chamber housing a patterned substrate having exposed single crystal material and at least a second different exposed material;

providing a flow of a silicon source gas to the process chamber, wherein the silicon source gas comprises dichlorosilane; and

providing a flow of a carbon precursor to the process chamber;

wherein the carbon doped epitaxial semiconductor layer is selectively deposited on the exposed single crystal material relative to the second exposed material at the pressure of greater than about 700 torr, thereby depositing the carbon doped epitaxial semiconductor layer on the exposed single crystal material at a rate greater than about 5 nm min^{-1}, and wherein the carbon doped epitaxial semiconductor layer thus deposited comprises between about 0.8% and about 1.2% substitutionally doped carbon in single crystal silicon.

28. The method of claim **27**, further comprising providing a flow of an n-dopant hydride to the process chamber.

29. The method of claim **27**, further comprising providing a flow of hydrochloric acid (HCl) to the process chamber.

30. The method of claim **27**, wherein the silicon source gas further comprises silane.

31. The method of claim **27**, wherein the silicon source gas consists essentially of dichlorosilane.

32. The method of claim **27**, wherein the silicon source gas further comprises at least one of silane (SiH_4), trisilane (Si_3H_8), and dichlorosilane ($Si_2H_nCl_{6-n}$ (wherein $1 \leqq n \leqq 6$)).

33. The method of claim **27**, wherein the carbon precursor is selected from the group consisting of tetrasilylmethane ($C(SiH_3)_4$), methyl silane (CH_3SIH3), and 1,3-disilabutane.

34. The method of claim **27**, wherein the carbon precursor comprises $(SiH_zCl_{3-z})_xCH_{4-x-y}Cl_y$, wherein $1 \leqq x \leqq 4$, and $0 \leqq y < 3$, and $(x+y) \leqq 4$, and $0 \leqq z \leqq 3$ for each of the SiH_3Cl_{3-z} groups.

35. The method of claim **27**, further comprising providing a flow of an n-dopant hydride to the process chamber at a flow rate that is between about 100 sccm and about 500 sccm.

36. The method of claim **27**, further comprising providing a flow of phosphine (PH_3) to the process chamber.

37. The method of claim **27**, wherein the pressure maintained in the process chamber is atmospheric.

38. The method of claim **27**, wherein carbon doped epitaxial semiconductor layer has a resistivity of less than about 0.7 mΩ·cm.

39. The method of claim **27**, wherein the patterned substrate is held at a temperature between about 630° C. and about 650° C. during deposition of the carbon doped epitaxial semiconductor layer.

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