US007847383B2

(12) **United States Patent**
So et al.

(10) **Patent No.: US 7,847,383 B2**
(45) **Date of Patent: *Dec. 7, 2010**

(54) **MULTI-CHIP PACKAGE FOR REDUCING PARASITIC LOAD OF PIN**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 596 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **11/797,592**

(22) Filed: **May 4, 2007**

(65) **Prior Publication Data**

US 2007/0228546 A1 Oct. 4, 2007

Related U.S. Application Data

(60) Continuation-in-part of application No. 11/589,192, filed on Oct. 30, 2006, now Pat. No. 7,566,958, which is a division of application No. 10/722,159, filed on Nov. 26, 2003, now Pat. No. 7,148,563.

(30) **Foreign Application Priority Data**

Dec. 2, 2002 (KR) 2002-75805

(51) **Int. Cl.**
H01L 23/02 (2006.01)

(52) **U.S. Cl.** **257/685**; 257/723; 257/786; 257/E25.006; 257/E25.027

(58) **Field of Classification Search** 257/685, 257/686, 723, 777, 730, 731, 733, 773, 786, 257/698, 778, 209, E25.006, E25.013, E25.021, 257/E25.027, E21.614, 694, 784, E23.079
See application file for complete search history.

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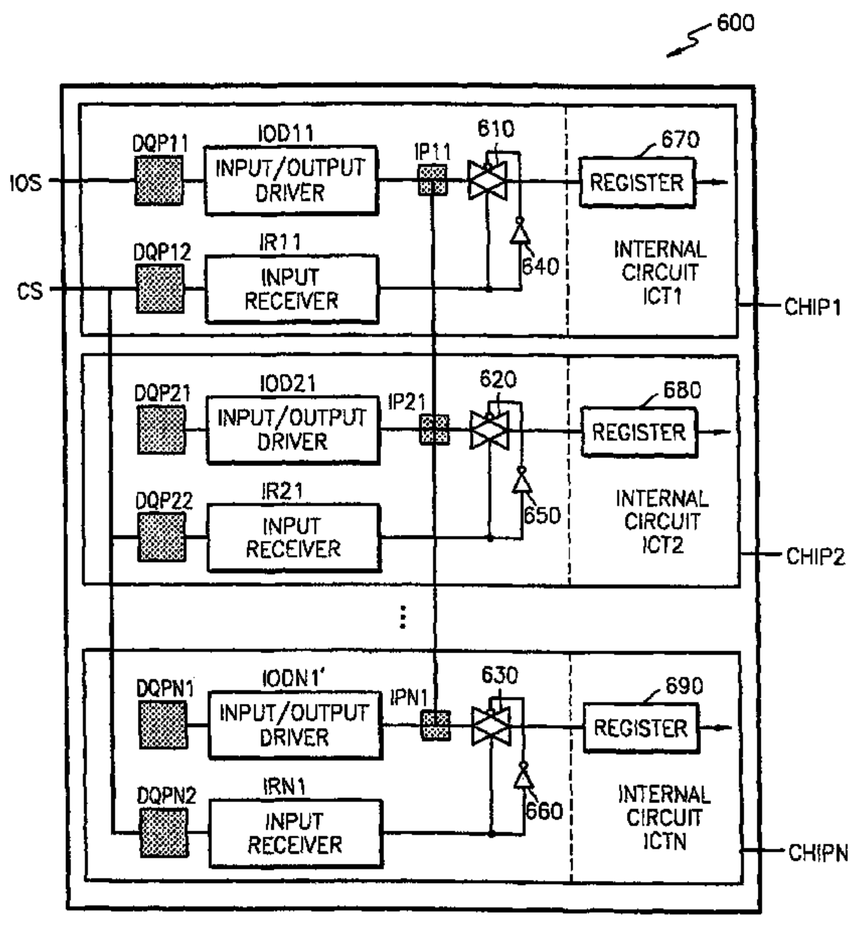
(74) *Attorney, Agent, or Firm*—Volentine & Whitt, PLLC

(57) **ABSTRACT**

A multi-chip package includes first through Nth semiconductor chips, each of which includes an input/output pad, an input/output driver coupled to the input/output pad, and an internal circuit. Each of the first through Nth semiconductor chips includes an internal pad for coupling the internal input/output driver and the internal circuit. The input/output pad of the first semiconductor chip directly receives an input/output signal via a corresponding pin of the multi-chip package. The second through Nth semiconductor chips indirectly receive the input/output signal via the internal pads coupled to each other. The multi-chip package can improve signal compatibility by maintaining a parasitic load of a pin to at least the level of a single chip, when a signal is transmitted to the pin at high speed.

20 Claims, 12 Drawing Sheets



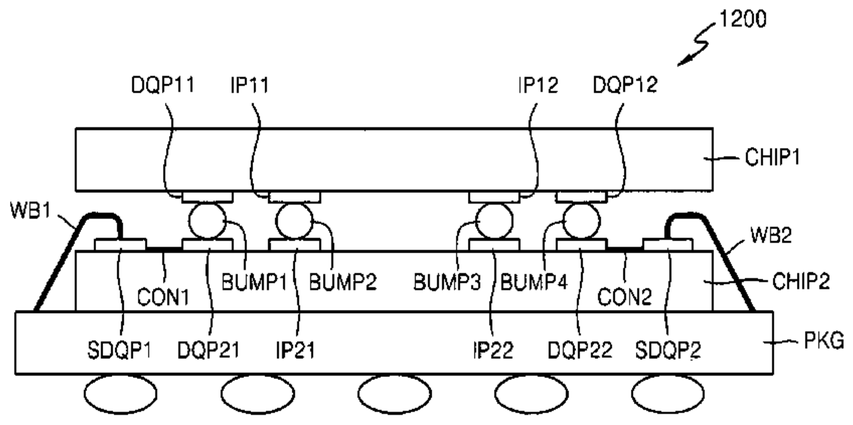


FIG. 1
Prior Art

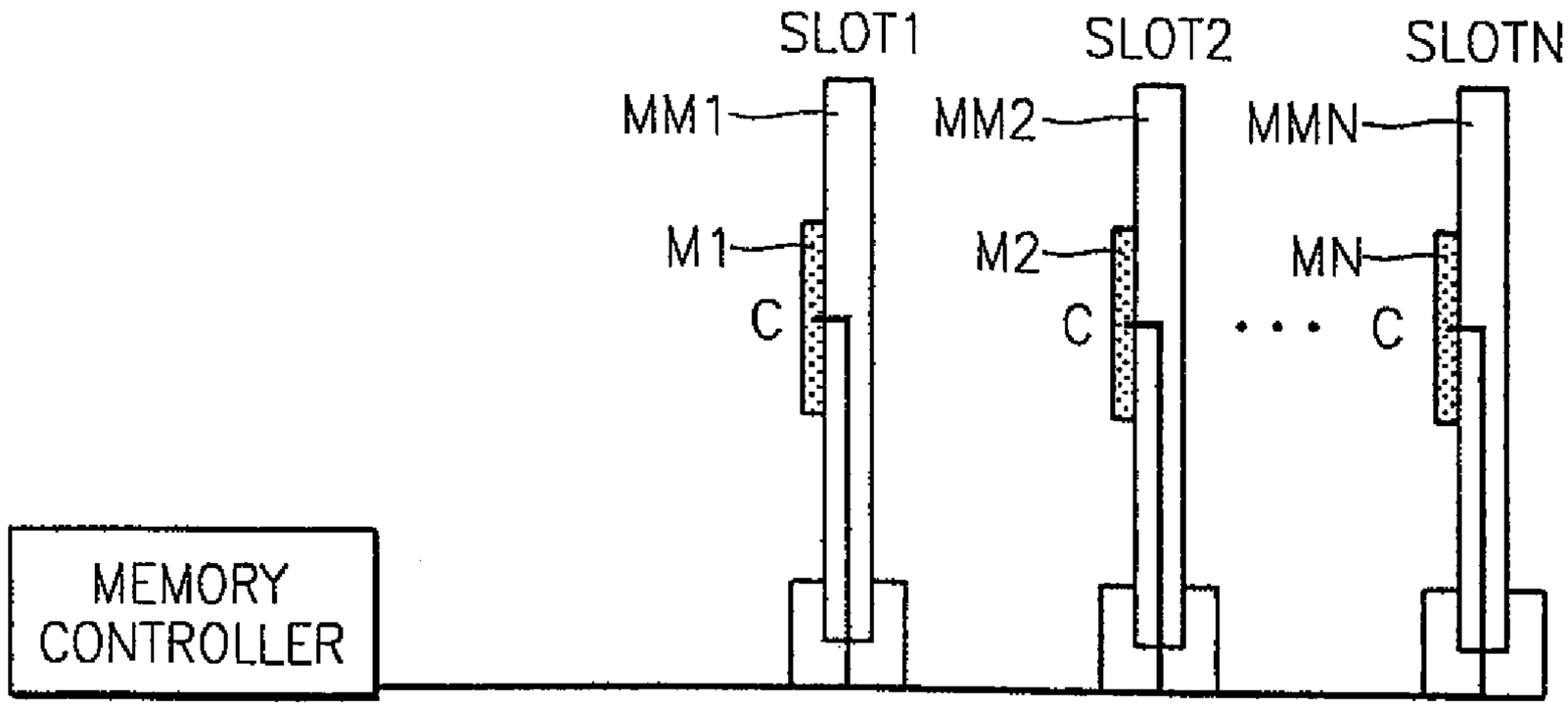


FIG. 2
Prior Art

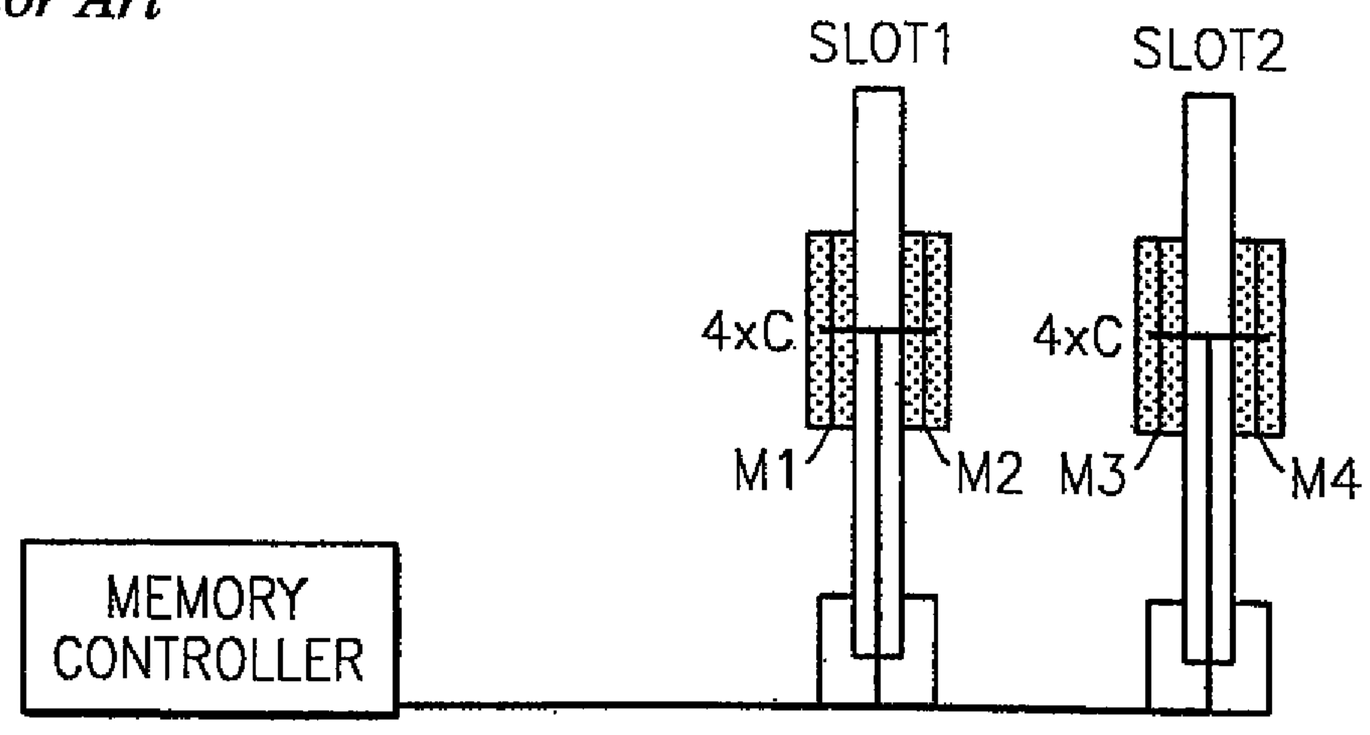


FIG. 3
Prior Art

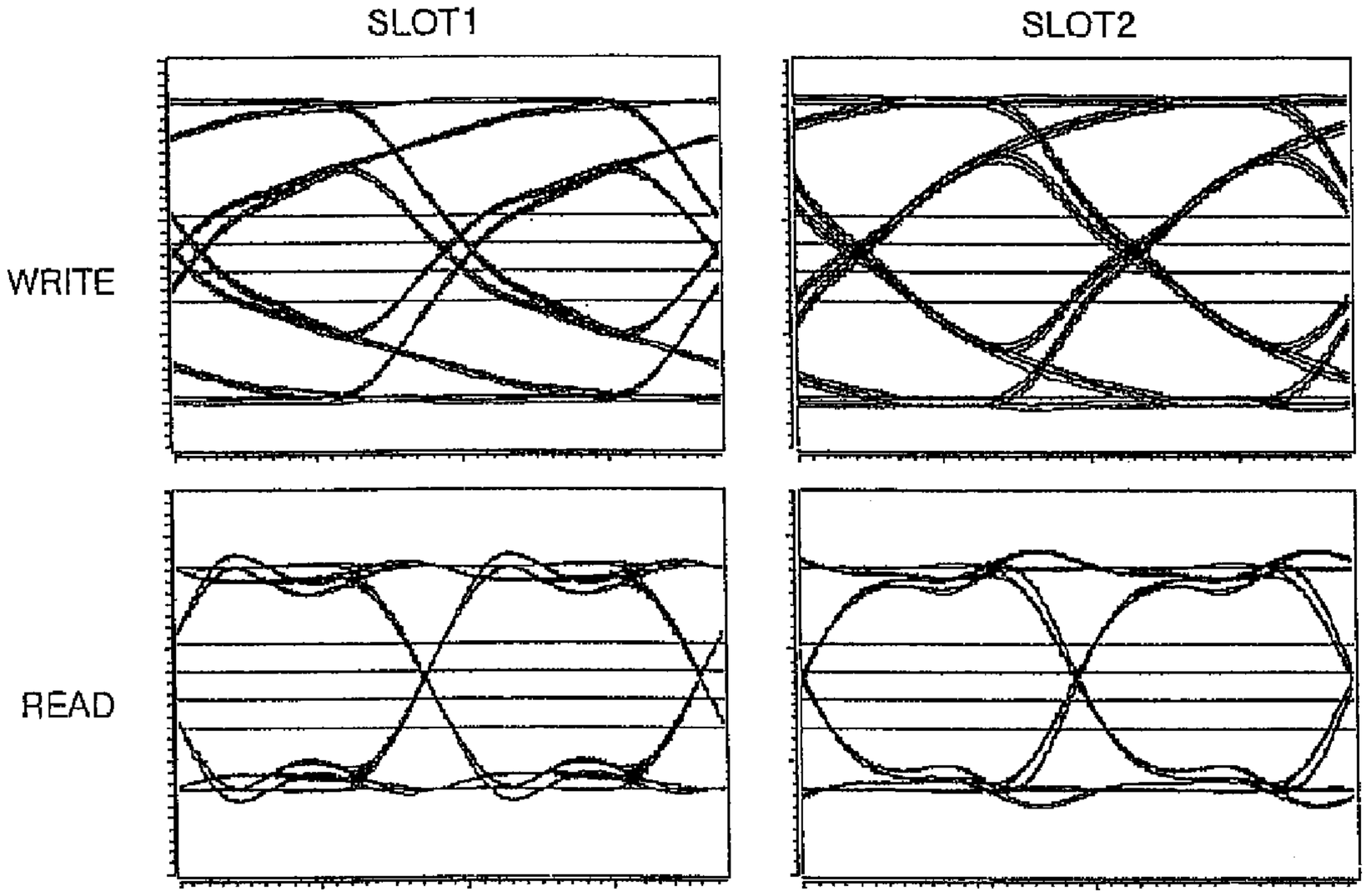


FIG. 4
Prior Art

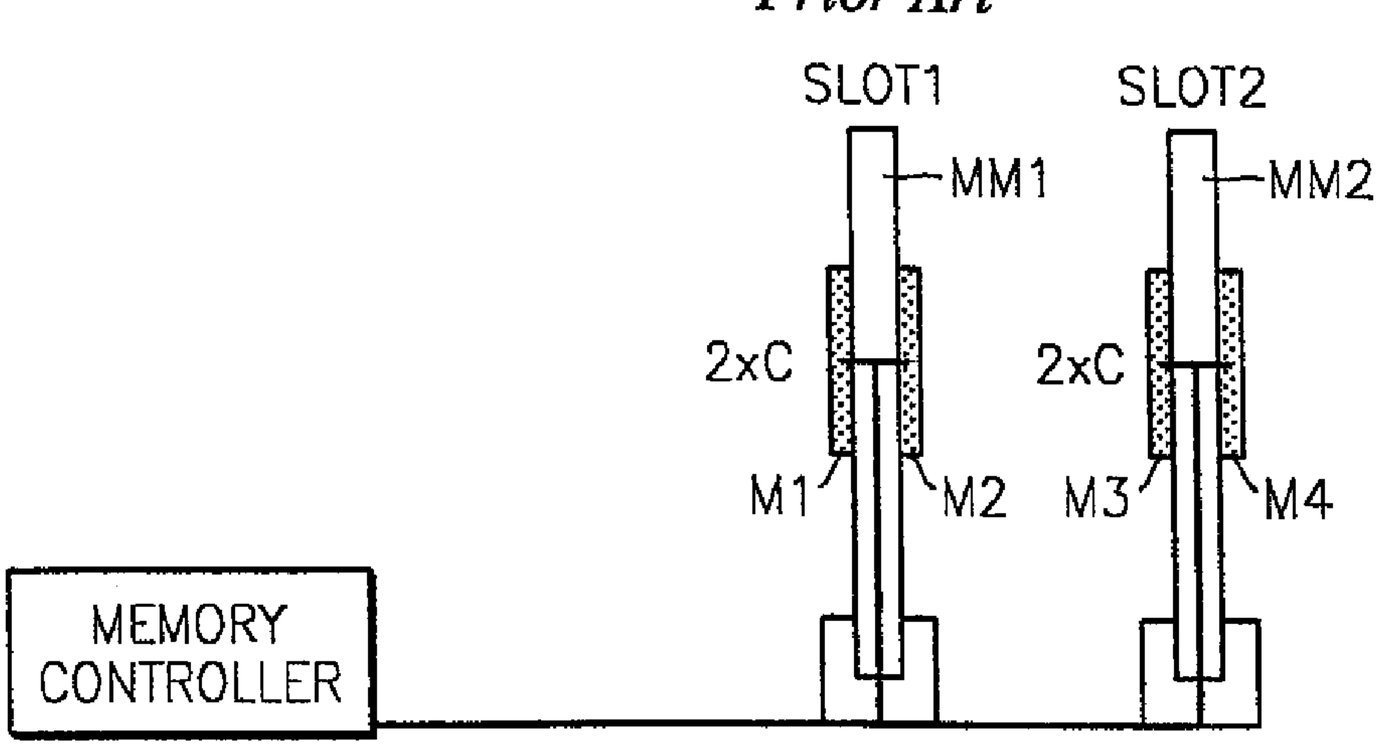


FIG. 5
Prior Art

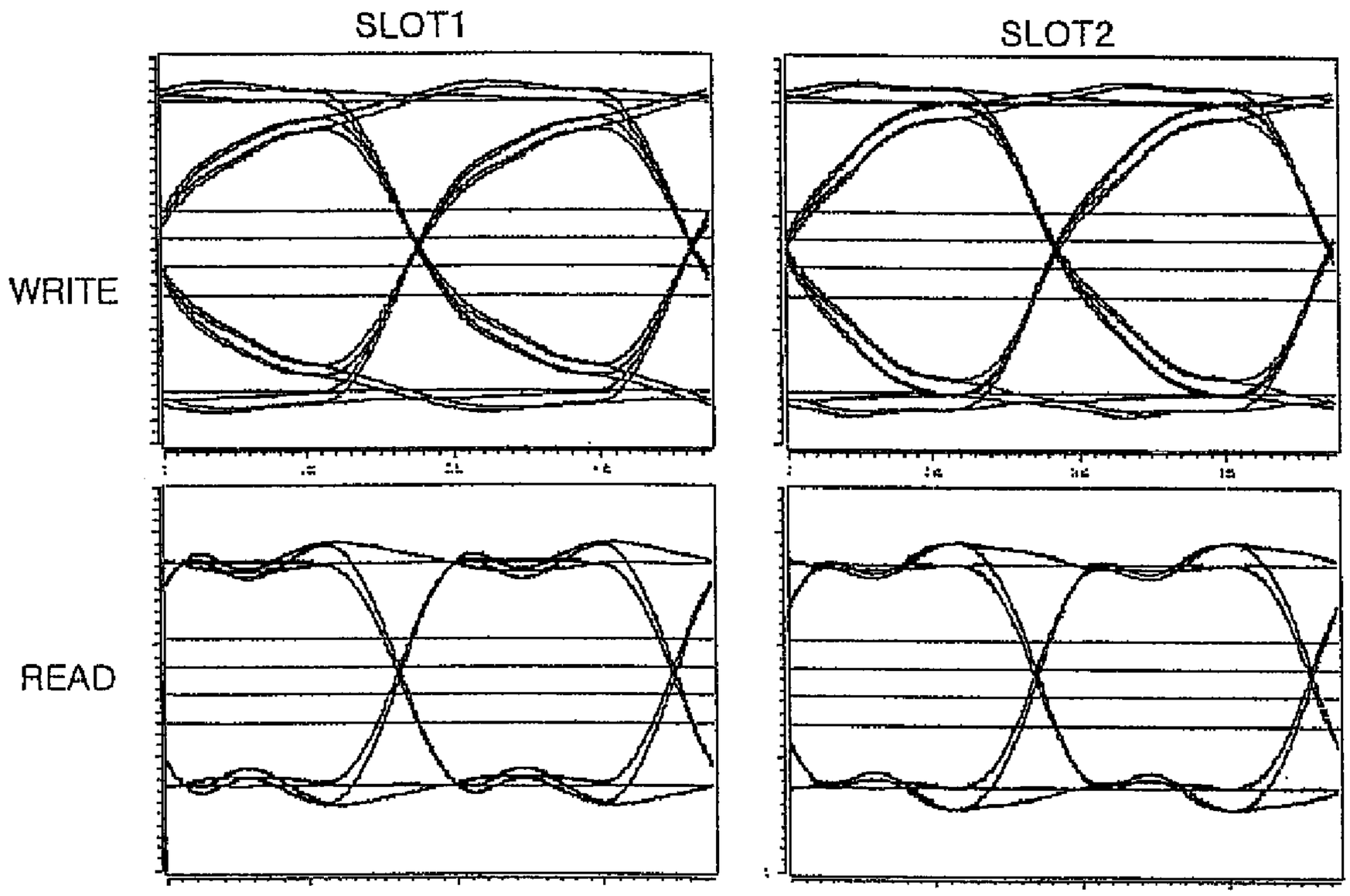


FIG. 6

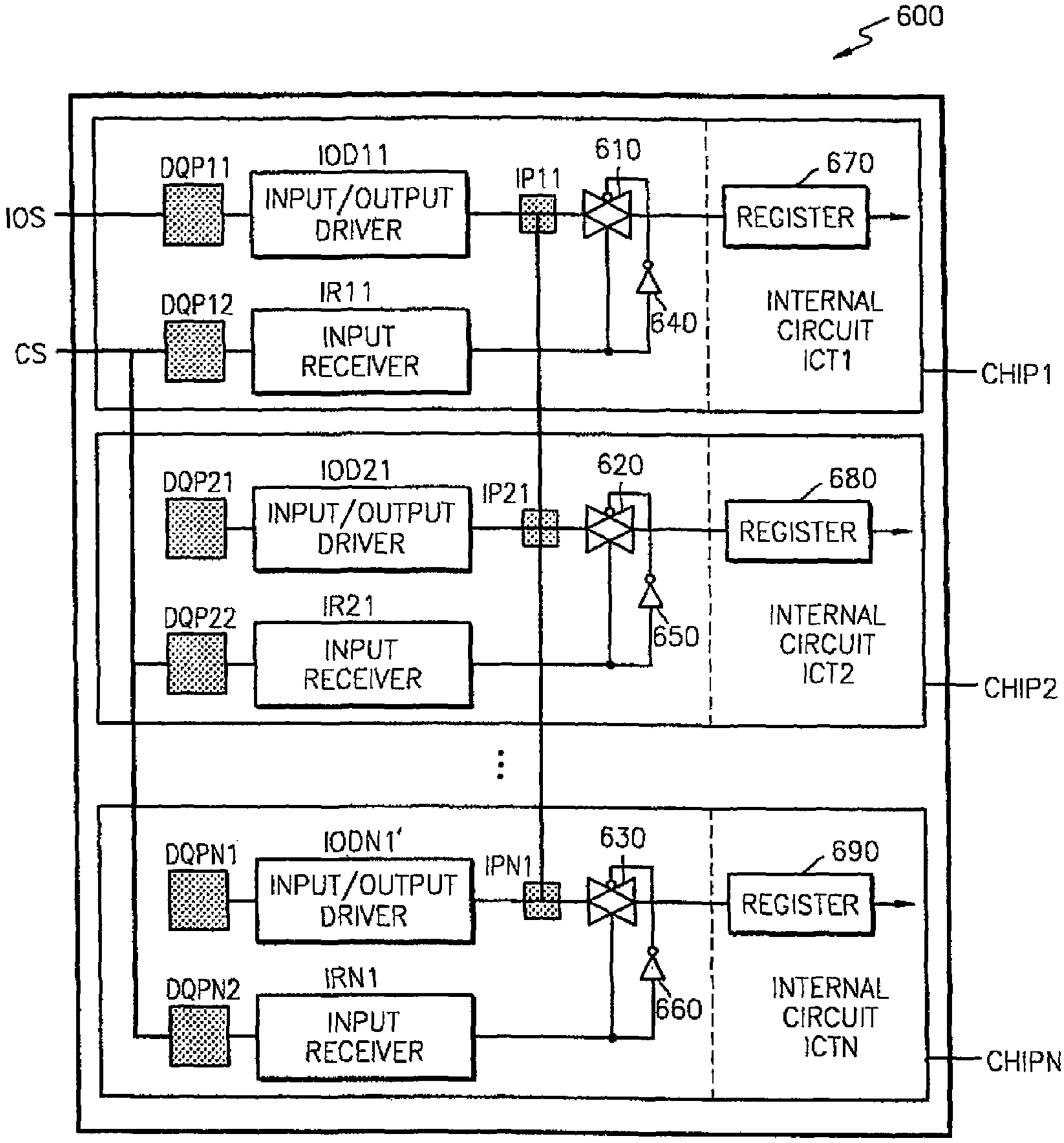

600
IOS
CS
DQP11
IOD11
INPUT/OUTPUT DRIVER
IP11
610
670
REGISTER
DQP12
IR11
INPUT RECEIVER
640
INTERNAL CIRCUIT ICT1
CHIP1
DQP21
IOD21
INPUT/OUTPUT DRIVER
IP21
620
680
REGISTER
DQP22
IR21
INPUT RECEIVER
650
INTERNAL CIRCUIT ICT2
CHIP2
DQPN1
IODN1'
INPUT/OUTPUT DRIVER
IPN1
630
690
REGISTER
DQPN2
IRN1
INPUT RECEIVER
660
INTERNAL CIRCUIT ICTN
CHIPN

FIG. 7

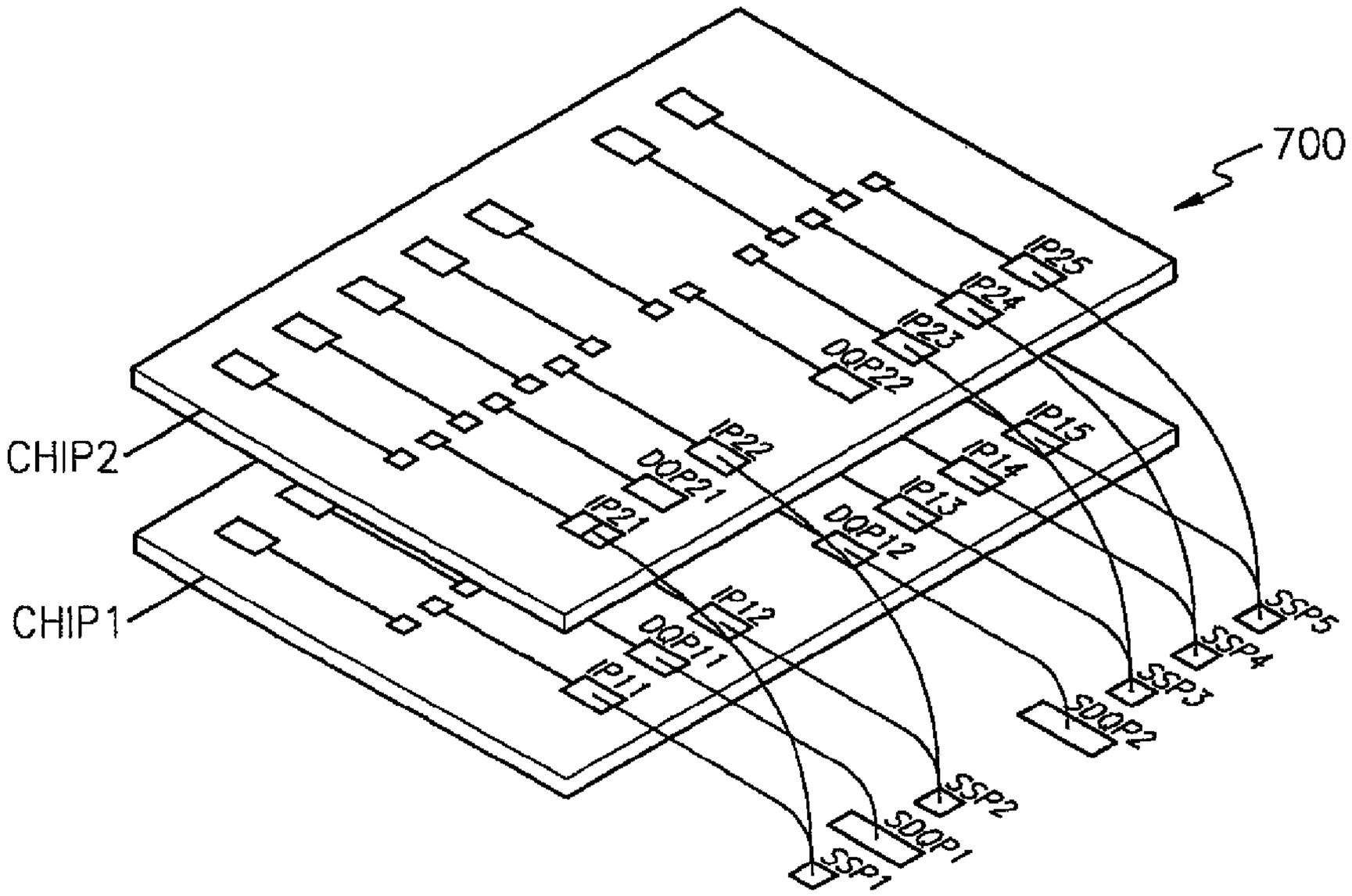

700
CHIP2
CHIP1
IP25
IP24
IP23
DOP22
IP22
DOP21
IP21
IP15
IP14
IP13
DOP12
IP12
DOP11
IP11
SSP5
SSP4
SSP3
SDOP2
SSP2
SDOP1
SSP1

FIG. 8

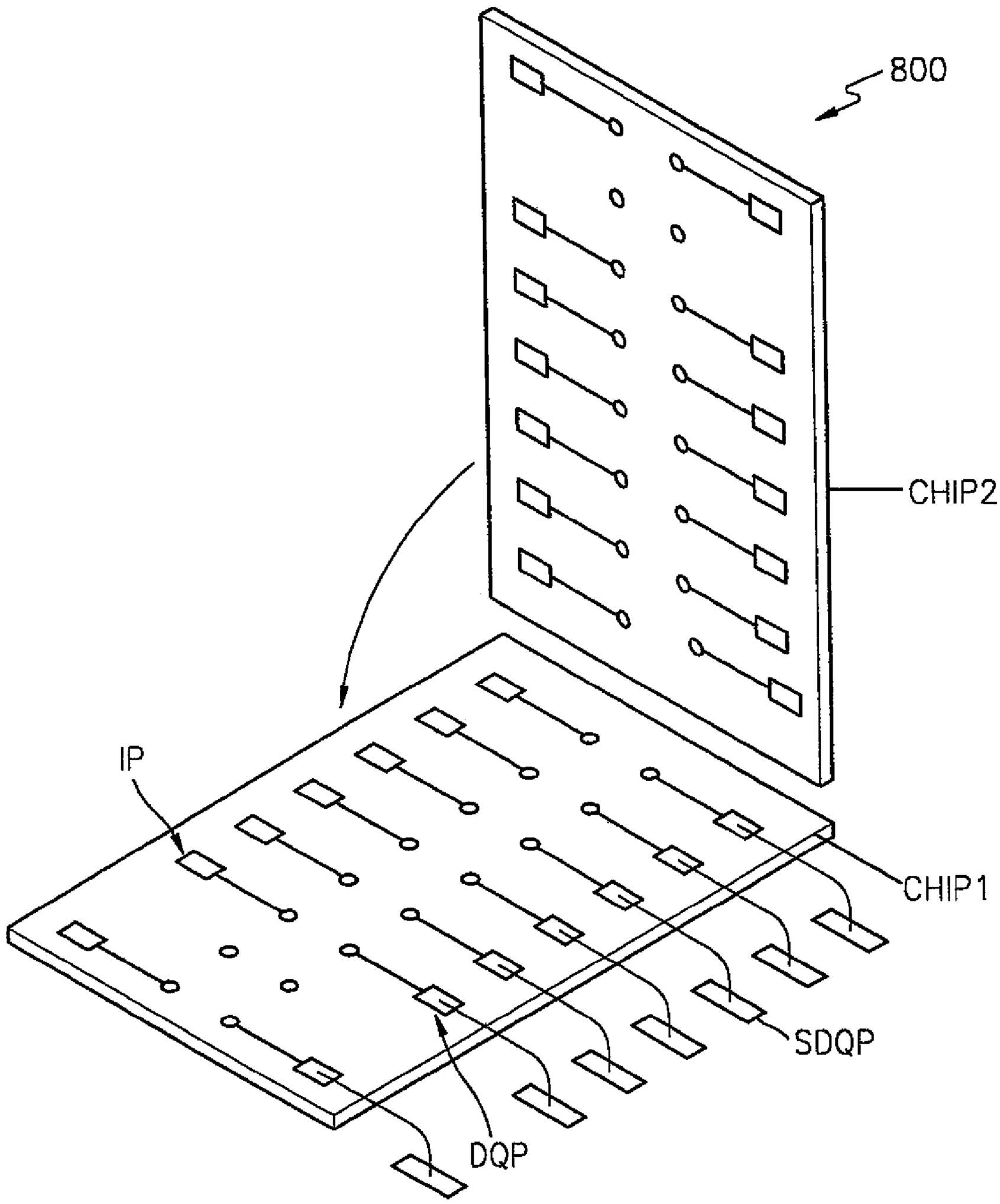


FIG. 9

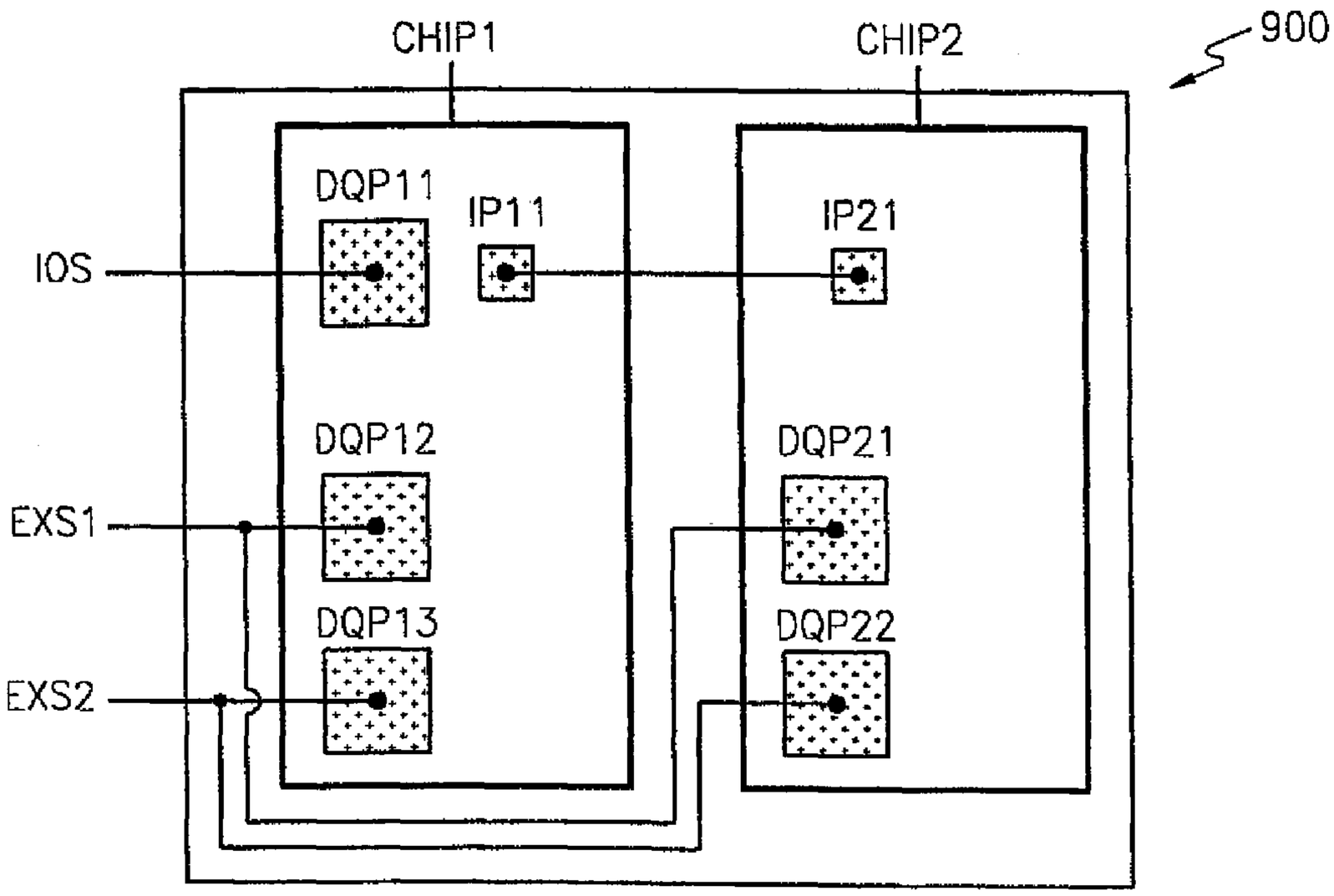

CHIP1
CHIP2
900
DQP11
IP11
IP21
IOS
DQP12
DQP21
EXS1
DQP13
DQP22
EXS2

FIG. 10

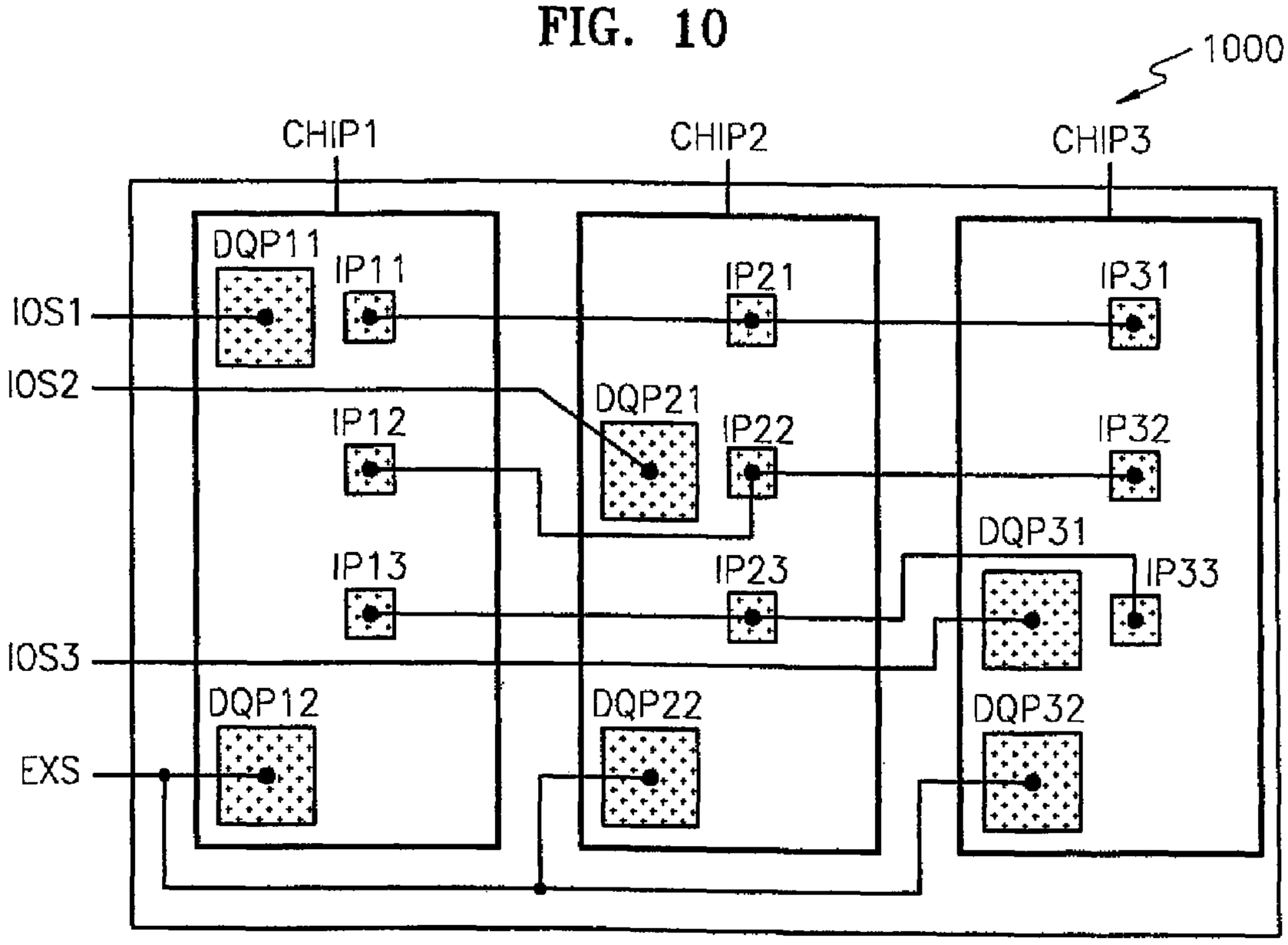

1000
CHIP1
CHIP2
CHIP3
DQP11
IP11
IP21
IP31
IOS1
IOS2
DQP21
IP12
IP22
IP32
DQP31
IP13
IP23
IP33
IOS3
DQP12
DQP22
DQP32
EXS

FIG. 11

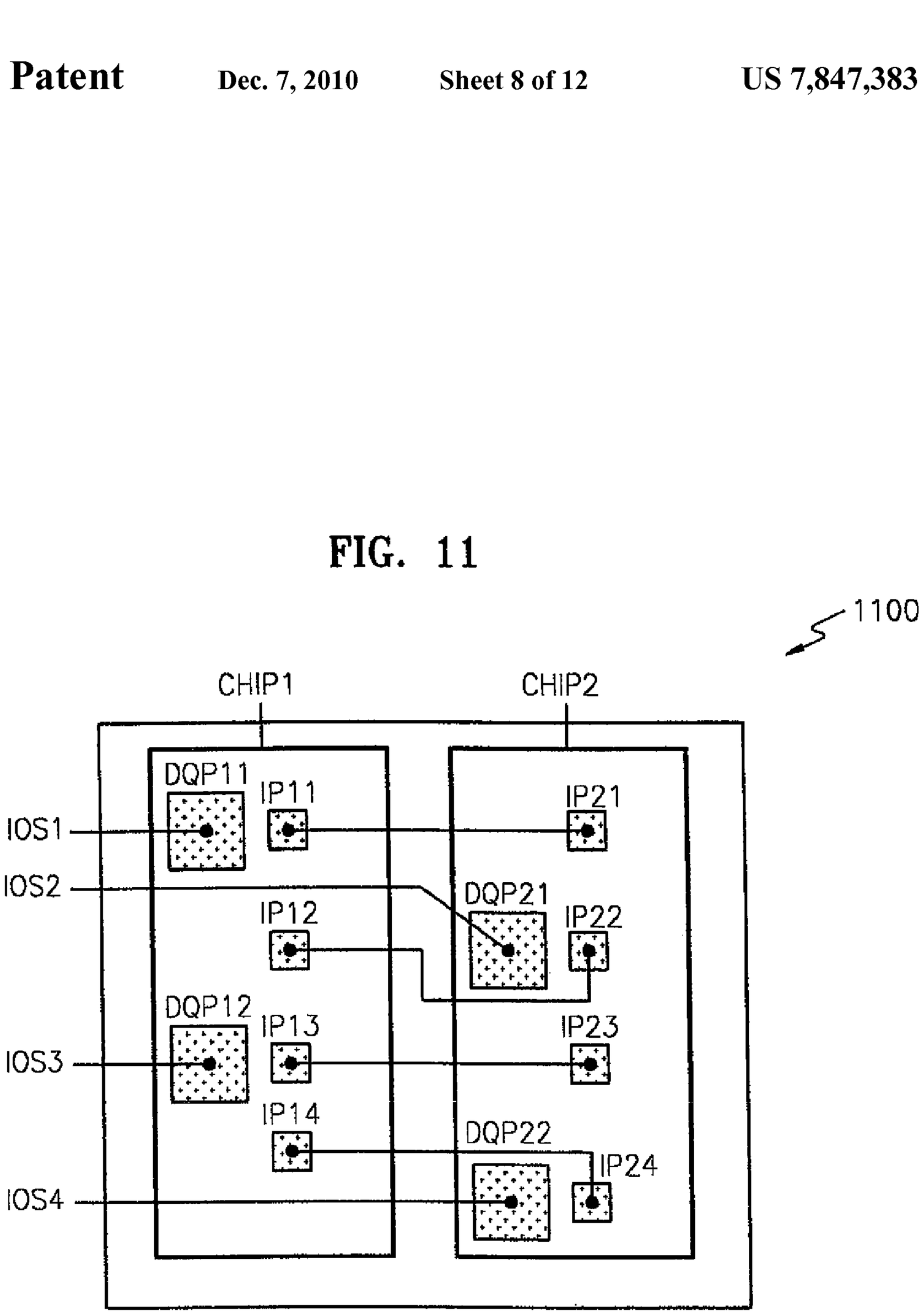

1100
CHIP1
CHIP2
DQP11
IP11
IP21
IOS1
IOS2
DQP21
IP12
IP22
DQP12
IP13
IP23
IOS3
IP14
DQP22
IP24
IOS4

FIG. 12

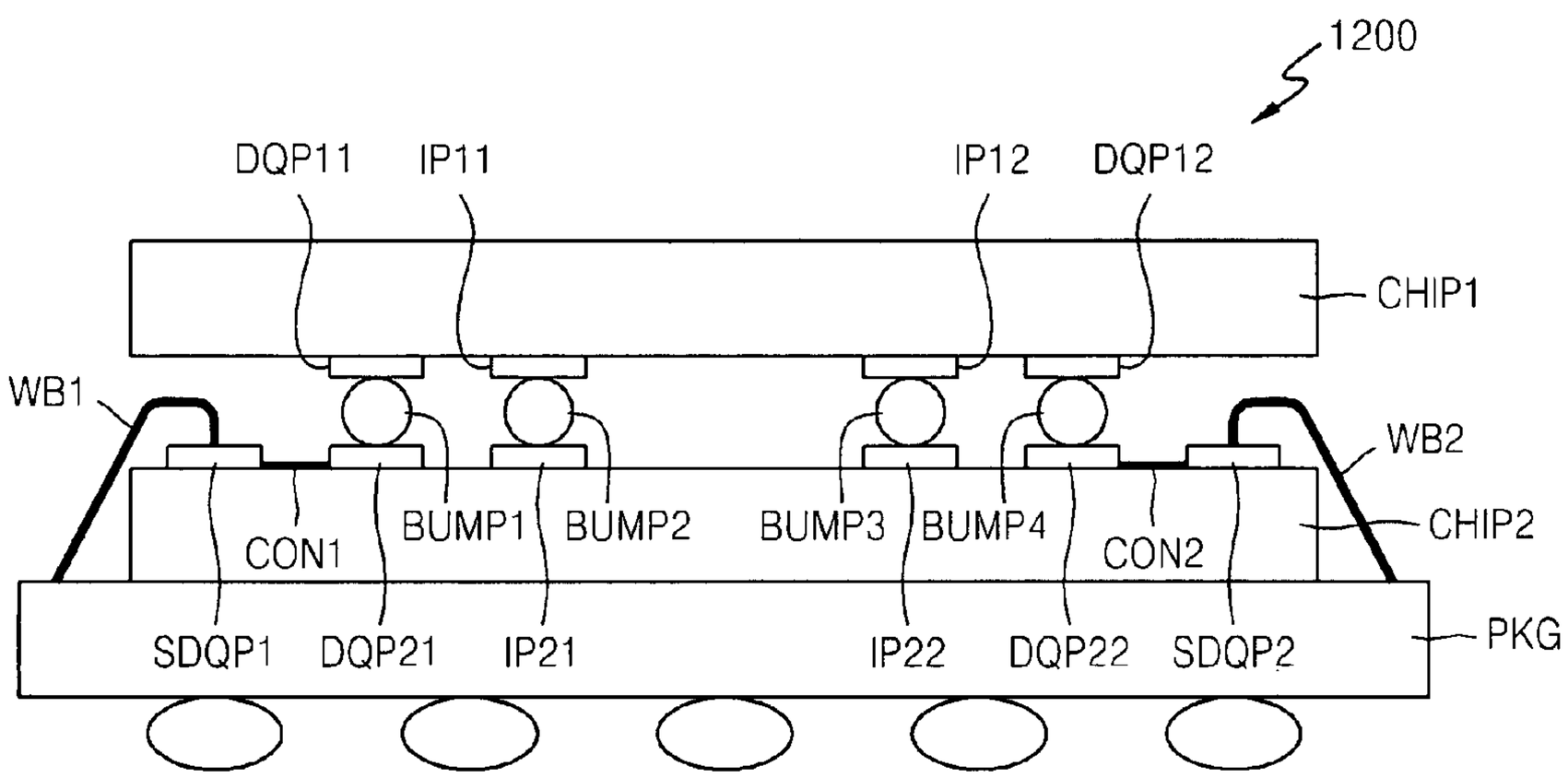

1200
DQP11
IP11
IP12
DQP12
CHIP1
WB1
WB2
CHIP2
CON1
BUMP1
BUMP2
BUMP3
BUMP4
CON2
PKG
SDQP1
DQP21
IP21
IP22
DQP22
SDQP2

FIG. 13

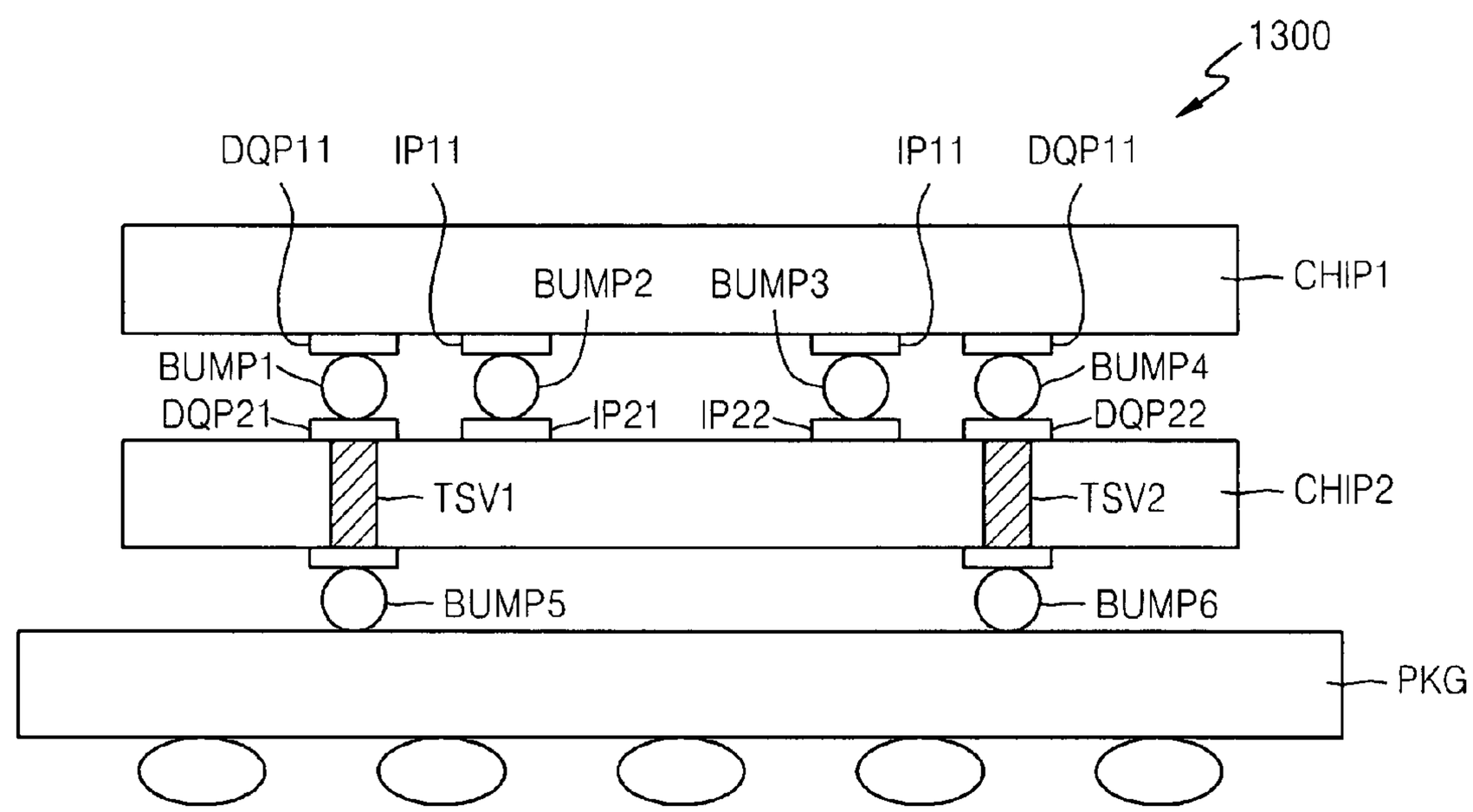

1300
DQP11
IP11
IP11
DQP11
CHIP1
BUMP2
BUMP3
BUMP1
BUMP4
DQP21
IP21
IP22
DQP22
TSV1
TSV2
CHIP2
BUMP5
BUMP6
PKG

FIG. 14

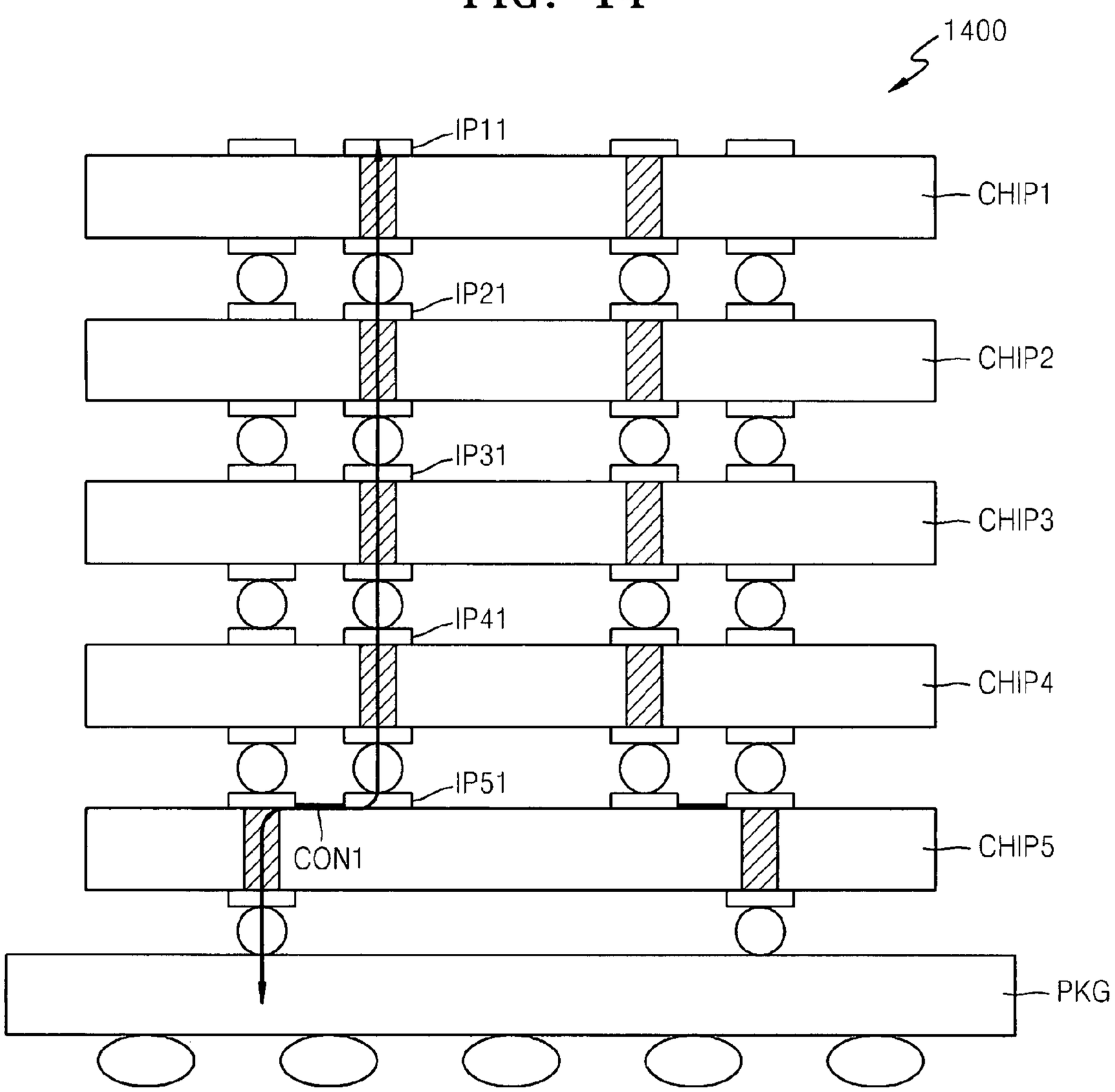

1400
IP11
CHIP1
IP21
CHIP2
IP31
CHIP3
IP41
CHIP4
IP51
CHIP5
CON1
PKG

FIG. 15

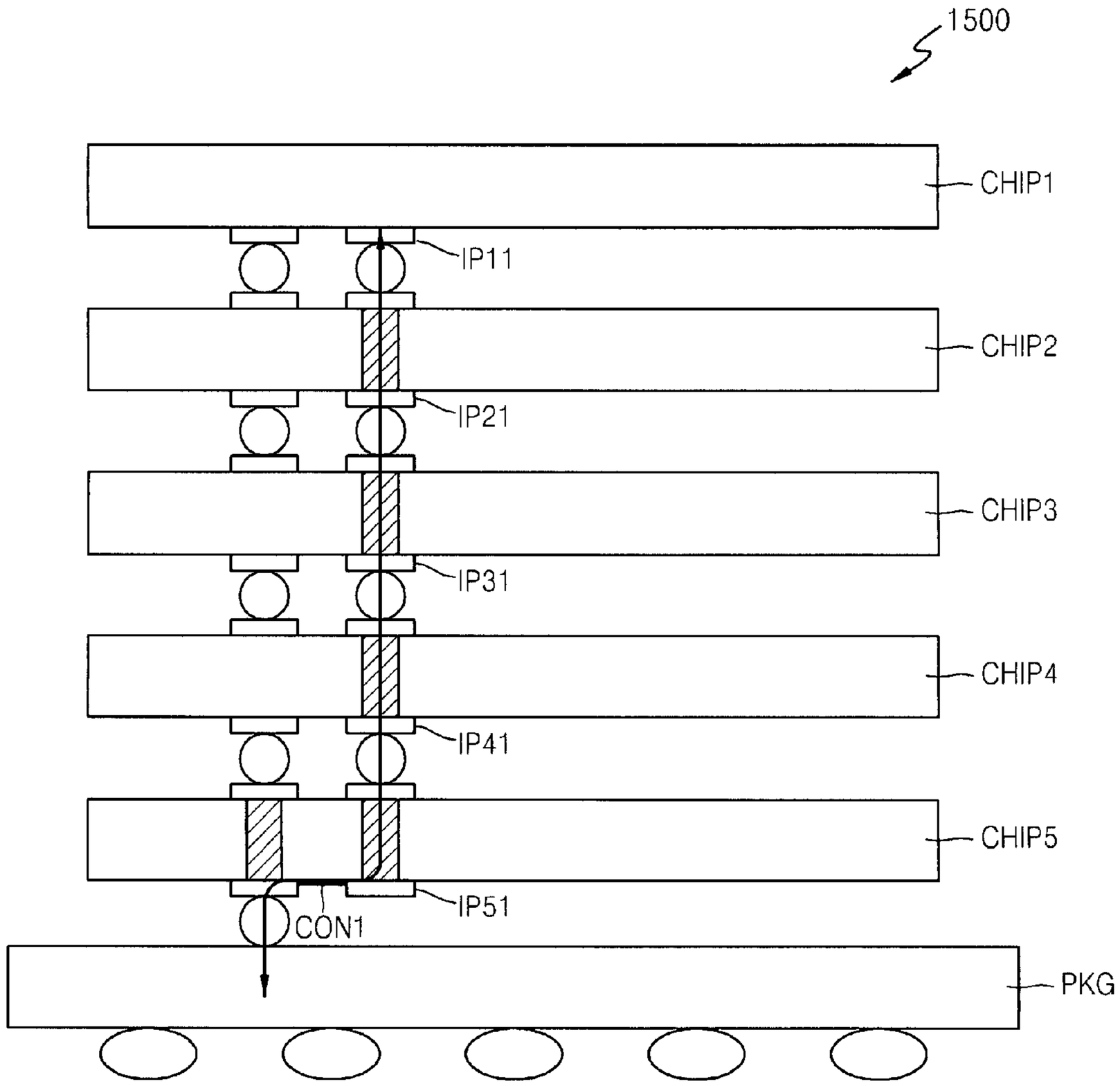
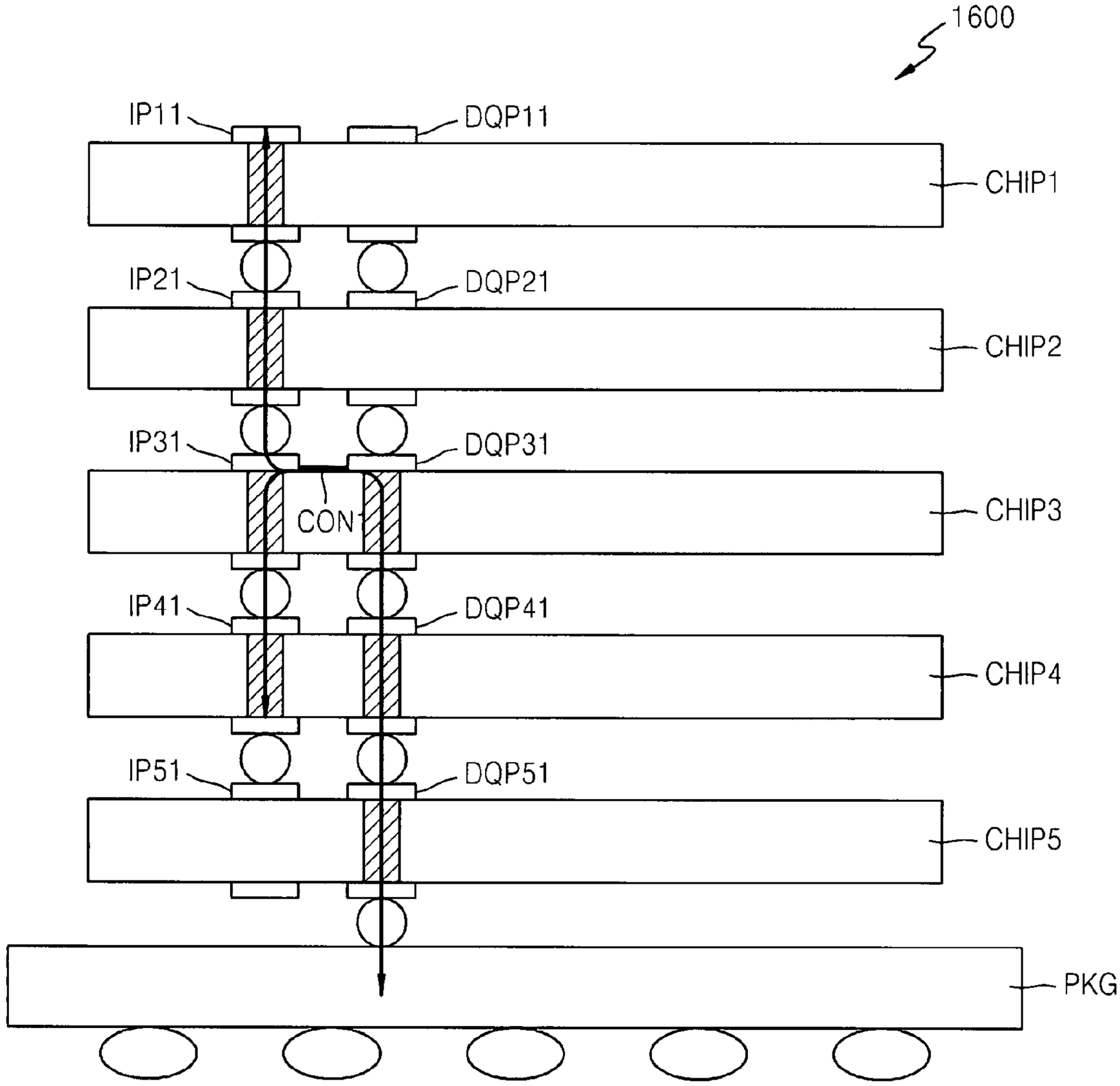

1500
CHIP1
IP11
CHIP2
IP21
CHIP3
IP31
CHIP4
IP41
CHIP5
IP51
CON1
PKG

FIG. 16


1600
IP11
DQP11
CHIP1
IP21
DQP21
CHIP2
IP31
DQP31
CON1
CHIP3
IP41
DQP41
CHIP4
IP51
DQP51
CHIP5
PKG

MULTI-CHIP PACKAGE FOR REDUCING PARASITIC LOAD OF PIN

CROSS REFERENCES TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. patent application Ser. No. 11/589,192, filed on 30 Oct. 2006, and issued on 28 Jul. 2009 as U.S. Pat. No. 7,566,958, which is in turn a divisional of U.S. patent application Ser. No. 10/722,159, filed 26 Nov. 2003 and issued as U.S. Pat. No. 7,148,563, the contents of each of which application are hereby incorporated by reference in their entirety for all purposes as if fully set forth herein, and claims priority under 35 U.S.C. §119 from Korean Patent Application No. 2002-75805, filed on Dec. 2, 2002, the contents of which are hereby incorporated by reference in their entirety as if fully set forth herein.

BACKGROUND AND SUMMARY

1. Technical Field

The present invention relates to multi-chip packages, and more particularly, to a multi-chip package which can minimize the parasitic load of a package pin by adjusting the number of chips coupled to the package pin.

2. Description

In recent years, multi-chip package techniques for incorporating several memory chips into a single package have been widely used to increase memory capacity. However, in typical multi-chip packages, a parasitic load of a package pin is proportional to the number of embedded memory chips. An increased parasitic load impedes high-speed transmission of signals input to the package pin. Accordingly, it is imperative for the multi-chip packages to reduce the parasitic load of the package pin to at least the level of the parasitic load of a single chip.

FIG. **1** is a diagram of a memory bus coupled to N memory modules, each of which includes a memory device.

Referring to FIG. **1**, N memory modules MM**1**, MM**2**, . . . , and MMN are mounted on N memory slots SLOT**1**, SLOT**2**, . . . , SLOTN. Each of the memory modules MM**1**, MM**2**, . . . , and MMN includes a memory device M**1**, M**2**, . . . , and MN, respectively. In FIG. **1**, C represents an input capacitance of each of the memory modules MM**1**, MM**2**, . . . , and MMN.

High-performance memory systems are required to connect more memory per channel and simultaneously transmit signals faster. The amount of memory connected to one channel is limited in order to transmit signals at high speed.

The memory bus of FIG. **1** has an input capacitance of N×C, and the capacitance has the same effect as a load on signal transmission. That is, as N increases, it becomes difficult to transmit signals at high speed. In a typical stub-type memory bus, the number of slots for mounting memory modules is limited to four or less.

In general, while the number of memory slots is limited, to secure maximum memory capacity a memory module is manufactured by stacking several packages, or mounting several chips in a single package.

However, even if a stacked package or a multi-chip package is used, in a case that requires an increased transmission rate of signals, it is still difficult to transmit signals at high speed due to the entire load of signal transmission lines. Also, to secure signal compatibility, packages such as multi-chips may not be used and the number of memory slots is more strictly limited.

FIG. **2** is a diagram of a memory bus, in which the number of memory slots is limited to two.

Referring to FIG. **2**, a first memory module MM**1** includes two multi-chip devices M**1** and M**2**, each of which includes two semiconductor chips. A second memory module MM**2** includes two multi-chip devices M**3** and M**4**, each of which also includes two semiconductor chips. Thus, the memory bus of FIG. **2** has an input capacitance of 8×C.

FIG. **3** is a diagram illustrating signal compatibility in relation to operations of the memory bus of FIG. **2**.

In FIG. **3**, the horizontal axis is the time axis and the vertical axis is the voltage axis.

It can be seen that both the first and second slots SLOT**1** and SLOT**2** exhibit low signal compatibility for write and read operations.

FIG. **4** is a diagram of a memory bus, in which the number of memory chips is reduced when compared to the memory module of FIG. **2**.

FIG. **5** is a diagram illustrating signal compatibility in relation to operations of the memory bus of FIG. **4**.

Referring to FIG. **4**, a first memory module MM**1** includes only two semiconductor chips M**1** and M**2**, and a second memory module MM**2** also includes only two semiconductor chips M**3** and M**4**. Thus, the memory bus of FIG. **4** has an input capacitance of 4×C.

Referring to FIG. **5**, when the input capacitance of the memory bus in FIG. **4** is reduced compared to the input capacitance of the memory bus in FIG. **2**, then the signal compatibility is improved. Therefore, minimizing the parasitic load of a package pin improves the signal compatibility in a memory bus where signals are transmitted at high speed.

The present invention provides a multi-chip package which can minimize the parasitic load of a package pin and improve signal compatibility in a memory bus using memory modules supporting multiple semiconductor chips.

In accordance with one aspect of the present invention, a multi-chip device comprises: a package including a plurality of terminals; N semiconductor chips, each of which includes an input/output pad and an internal pad; and one or more first connectors, each first connector coupling the internal pad of one of the N semiconductor chips to the internal pad of another one of the N semiconductor chips. The input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package, and a remaining (N−1) of the N semiconductor chips indirectly receive the input/output signal via the internal pads.

In accordance with another aspect of the present invention, a multi-chip device comprises: a package including a plurality of terminals; N semiconductor chips, each of which includes an input/output pad and an internal pad; and at least one first connector or second connector, each said connector coupling the internal pad of one of the N semiconductor chips to the internal pad of another one of the N semiconductor chips. The first connector includes a first bump, and the second connector includes a second bump and a Through Silicon Via (TSV). The input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package, and a remaining (N−1) of the N semiconductor chips indirectly receive the input/output signal via the internal pads.

In accordance with still another aspect of the present invention, a multi-chip device comprises: a package including a plurality of terminals; N semiconductor chips, each of which includes an input/output pad and an internal pad; and one or more first connectors, each first connector coupling one of the

internal pad and the input/output pad of one of the N semiconductor chips to one of the internal pad and the input/output pad of another one of the N semiconductor chips. The input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package. The internals pads of another X of the N semiconductor chips indirectly receive the input/output signal, and a remaining (N−X−1) of the N semiconductor chips indirectly receive the input/output signal via the input/output pads.

BRIEF DESCRIPTION OF THE DRAWINGS

The above features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. **1** is a diagram of a memory bus coupled to n memory modules, each of which includes memory;

FIG. **2** is a diagram of a memory bus, in which the number of memory slots is limited to 2;

FIG. **3** is a diagram illustrating signal compatibility in relation to operations of the memory bus of FIG. **2**;

FIG. **4** is a diagram of a memory bus, in which the number of memory chips is reduced as compared to the memory module of FIG. **2**;

FIG. **5** is a diagram illustrating signal compatibility in relation to operations of the memory bus of FIG. **4**;

FIG. **6** is a diagram of a multi-chip package according to a first embodiment;

FIG. **7** is a diagram of an example of a method of connecting semiconductor chips in the multi-chip package of FIG. **6**;

FIG. **8** is a diagram of another example of a method of connecting semiconductor chips in the multi-chip package of FIG. **6**;

FIG. **9** is a diagram of a multi-chip package according to a second embodiment;

FIG. **10** is a diagram of a multi-chip package according to a third embodiment; and

FIG. **11** is a diagram of a multi-chip package according to a fourth embodiment.

FIG. **12** is a diagram of a third example of a method of connecting semiconductor chips in a multi-chip device;

FIG. **13** is a diagram of a fourth example of a method of connecting semiconductor chips in a multi-chip device;

FIG. **14** is a diagram of a fifth example of a method of connecting semiconductor chips in a multi-chip device;

FIG. **15** is a diagram of a sixth example of a method of connecting semiconductor chips in a multi-chip device;

FIG. **16** is a diagram of a seventh example of a method of connecting semiconductor chips in a multi-chip device.

DETAILED DESCRIPTION

The present invention will now be described more fully with reference to the accompanying drawings, in which embodiments of the invention are shown. The same reference numerals in different drawings represent the same element.

FIG. **6** is a diagram of a multi-chip package according to a first embodiment.

The multi-chip package **600** of FIG. **6** includes first through Nth semiconductor chips CHIP**1**, CHIP**2**, . . . , and CHIPN. Here, N is a natural number. The first semiconductor chip CHIP**1** includes input/output pads DQP**11** and DQP**12**, an input/output driver IOD**11** coupled to the input/output pad DQP**11**, and an internal circuit ICT**1**. The first semiconductor chip CHIP**1** includes circuits **610** and **640**, which transmit signals to the internal circuit ICT**1** via the input/output driver IOD**11**. The configuration of each of the second through Nth semiconductor chips CHIP**2**-CHIPN is identical to that of the first semiconductor chip CHIP**1**.

Operations of the first semiconductor chip CHIP**1** will be described hereinafter. An input/output signal IOS is transmitted to the first semiconductor chip CHIP**1** via the input/output pad DQP**11** and the input/output driver IOD**11**. Here, when a chip selection signal CS is set at a high level and transmitted via the input/output pad DQP**12** and an input receiver IR**11**, the chip selection signal CS is sent to a transmission gate **610** directly and via an inverter **640**, and then the transmission gate **610** is turned on. Then, the input/output signal IOS is transmitted to a register **670** of the internal circuit ICT**1**.

Operations of each of the second through Nth semiconductor chips CHIP**2**-CHIPN are the same as those of the first semiconductor chip CHIP**1**. Therefore, a description of those operations will be omitted here for brevity.

Each of the first through Nth semiconductor chips CHIP**1**-CHIPN includes internal pads IP**11**, IP**21**, . . . , and IPN**1**, which couple internal input/output drivers IOD**11**, IOD**21**, . . . , and IODN**1** with internal circuits ICT**1**, ICT**2**, . . . and ICTN. The internal pads IP**11**, IP**21**, . . . , and IPN**1** of the first through Nth semiconductor chips CHIP**1**-CHIPN are coupled to each other via a common pad (not shown) installed at a substrate. The common pad (not shown) will be described later with respect to in FIG. **7**. While the internal pads IP**11**, IP**21**, . . . , and IPN**1** can be coupled by wire bonding, any other method of transmitting signals is also possible.

The input/output pad DQP**11** of the first semiconductor chip CHIP**1** directly receives the input/output signal IOS transmitted via a corresponding pin (not shown) of a multi-chip package **600**. Also, the input/output pad DQP**11** of the first semiconductor chip CHIP**1** is bonded to an external pin (not shown) of the multi-chip package **600**.

The second through Nth semiconductor chips CHIP**2**-CHIPN indirectly receive the input/output signal IOS via the internal pads IP**11**, IP**21**, . . . , and IPN**1**, coupled to each other, without passing through the outside of the multi-chip package **600**.

In the conventional multi-chip package, all of the input/output signals are transmitted via the input/output pads of each semiconductor chip. However, in the multi-chip package **600**, to minimize the parasitic load of a package pin, the input/output signal IOS is transmitted only to one of the semiconductor chips, i.e., the first semiconductor chip CHIP**1**. Because the input/output signal IOS is transmitted only to the input/output pad DQP**11** of the first semiconductor chip CHIP**1**, the parasitic load of the multi-chip package **600** is the same as the parasitic load of a single semiconductor chip.

The chip selection circuit CS is coupled to the input/output pads DQP**12**, DQP**22**, and DQPN**2** in the same manner as that of a typical multi-chip package. The parasitic load of the package pin receiving the chip selection signal CS is affected by all the N semiconductor chips CHIP**1**-CHIPN. Unlike with the input/output signal IOS, the parasitic load increases N-fold and signals can be simultaneously transmitted from the outside to the first through Nth semiconductor chips CHIP**1**-CHIPN.

In general, even if the parasitic load of the pin receiving the chip selection signal CS increases N-fold, as the parasitic load of a pin receiving the chip selection signal CS is less than that of a pin receiving the input/output signal IOS, operations of the multi-chip package **600** are performed without errors.

In the multi-chip package **600** of FIG. **6**, the Nth semiconductor chip CHIPN indirectly receives the input/output signal IOS via the first through (N−1)th semiconductor chips CHIP**1**-CHIP(N−1). Therefore, it may take a longer time for the input/output signal IOS to arrive at the internal circuit ICTN of the Nth semiconductor chip CHIPN than at the internal circuit ICTI of the first semiconductor chip CHIP**1**.

To solve this problem, each of the semiconductor chips CHIP**1**-CHIPN may include a delay circuit (not shown) capable of selectively delaying transmission time of the input/output signal IOS, so that each of the first through (N−1)th semiconductor chips CHIP**1**-CHIP(N−1) receives the input/output signal IOS at the moment the internal circuits ICT**1**-ICTN of the Nth semiconductor chip CHIPN receive the input/output signal IOS.

FIG. **7** is a diagram of an example of a method of coupling semiconductor chips in the multi-chip package of FIG. **6**.

FIG. **7** illustrates only the first and second semiconductor chips CHIP**1** and CHIP**2**. The coupling method will be described using the first and second semiconductor chips CHIP**1** and CHIP**2**.

The first and second semiconductor chips CHIP**1** and CHIP**2** include the internal pads IP**11**, IP**12**, IP**13**, IP**14**, IP**15**, IP**21**, IP**22**, IP**23**, IP**24**, and IP**25**, which can be coupled by bonding for enabling signal transmission. When a pad is installed at an edge of a semiconductor chip, additional re-interconnection processes are not needed. However, when the pad is installed in the center of the semiconductor chip, a pad coupled to the central pad should be disposed again at the edge of the semiconductor chip.

The internal pads IP**11**, IP**12**, IP**13**, IP**14**, IP**15**, IP**21**, IP**22**, IP**23**, IP**24**, and IP**25** are coupled to each other via common pads SSP**1**, SSP**2**, SSP**3**, SSP**4**, and SSP**5** of a substrate. That is, the first internal pad IP**11** of the first semiconductor chip CHIP**1** and the first internal pad IP**21** of the second semiconductor chip CHIP**2** are commonly bonded to the first common pad SSP**1**. In the same manner, the second internal pad IP**12** of the first semiconductor chip CHIP**1** and the second internal pad IP**22** of the second semiconductor chip CHIP**2** are bonded to the second common pad SSP**2**, etc.

The first input/output pad DQP**11** of the first semiconductor chip CHIP**1**, to which the input/output signal IOS is applied, is coupled to a pad SDQP**1** of the substrate, and the pad SDQP**1** is coupled to an external pin or ball of the multi-chip package.

The method of coupling the internal pads of the first and second semiconductor chips using the common pads SSP**1**, SSP**2**, SSP**3**, SSP**4**, and SSP**5** is applicable when the input/output signal IOS is transmitted at a low speed. However, when the input/output signal IOS is transmitted at a high speed, a delay may be caused by the wire. Such a problem can be solved by the method of FIG. **8**.

FIG. **8** is a diagram of another example of a method of coupling semiconductor chips in the multi-chip package of FIG. **6**.

FIG. **8** illustrates a flip chip structure, in which a semiconductor chip is installed on another semiconductor chip. Pads other than the internal pad IP are coupled to a pad SDQP, which may be coupled by wire bonding. The lower semiconductor chip CHIP**1** is coupled to a bonding finger (not shown) of the package by using wire bonding and thereby coupled to a terminal of the package.

Since the internal pad IP is not coupled to the terminal of the package, it is not coupled to the wire-bonded pad SDQP. To embody the same semiconductor chip into the flip chip structure, positions of bumps should be symmetrical.

FIG. **9** is a diagram of a multi-chip package according to a second embodiment.

FIG. **9** illustrates a multi-chip package, in which the input/output signal IOS is directly transmitted to a semiconductor chip CHIP**1** and indirectly transmitted to a semiconductor chip CHIP**2** by using internal pads IP**11** and IP**21**, while other signals are directly input to each of the semiconductor chip CHIP**1** and CHIP**2**.

More specifically, like the multi-chip package **600** of FIG. **6**, the multi-chip package **900** of FIG. **9** includes an input/output pad DQP**11** and internal pads IP**11** and IP**21**. The input/output signal IOS is transmitted to the semiconductor chips CHIP**1** and CHIP**2** via the input/output pad DQP**11** and the internal pads IP**11** and IP**21**. Also, predetermined external signals EXS**1** and EXS**2** are applied to each of the semiconductor chips CHIP**1** and CHIP**2** via direct input/output pads DQP**12**, DQP**13**, DQP**21**, and DQP**22** on the semiconductor chips CHIP**1** and CHIP**2**. The external signals EXS**1** and EXS**2** are input via corresponding pins (not shown) of the multi-chip package **900**.

In the second embodiment, the multi-chip package **900** can select signals transmitted to the semiconductor chips CHIP**1** and CHIP**2** using the internal pads IP**11** and IP**21**.

That is, address signals and commands, which cause a small parasitic load to a package pin or are not restricted by a transmission rate, are transmitted to the semiconductor chips CHIP**1** and CHIP**2** using the direct input/output pads DQP**12**, DQP**13**, DQP**21**, and DQP**22**. By comparison, signals such as the input/output signal IOS, which cause intense parasitic load to a package pin or require high-speed transmission, are applied to the semiconductor chips CHIP**1** and CHIP**2** by using the internal signals IP**11** and IP**21**.

FIG. **10** is a diagram of a multi-chip package according to a third embodiment.

Referring to FIG. **10**, the multi-chip package **1000** according to the third embodiment comprises first through Nth semiconductor chips CHIP**1**, CHIP**2**, and CHIP**3**, each of which includes first through 3rd input/output pads DQP**11**, DQP**21**, and DQP**31**, first through Nth input/output drivers (not shown) coupled to the input/output pads DQP**11**, DQP**21**, and DQP**31**, and an internal circuit (not shown).

Each of the first through 3rd semiconductor chips CHIP**1**, CHIP**2**, and CHIP**3** includes first through 3rd internal pads IP**11**, IP**12**, IP**13**, IP**21**, IP**22**, IP**23**, IP**31**, IP**32**, and IP**33**, which couple the internal input/output drivers (not shown) and the internal circuit (not shown). The first through 3rd internal pads IP**11**, IP**12**, and IP**13** of the first semiconductor chip CHIP**1** are coupled to the second and third internal pads IP**21**, IP**22**, IP**23**, IP**31**, IP**32**, and IP**33** corresponding thereto of the second and third through Nth semiconductor chips CHIP**2** and CHIP**3**.

Predetermined first through 3rd input/output signals IOS**1**, IOS**2**, and IOS**3** are received via corresponding pins of the multi-chip package **1000**. An input/output signal for each semiconductor chip is directly received by the corresponding input/output pad. The first through 3rd semiconductor chips CHIP**1**, CHIP**2**, and CHIP**3** indirectly receive the input/output signals IOS**1**-IOS**3** via the corresponding internal pads IP**11**, IP**12**, IP**13**, IP**21**, IP**22**, IP**23**, IP**31**, IP**32**, and IP**33**, which are coupled to each other.

According to the embodiment of FIG. **10**, the input/output pads, to which the input/output signal is transmitted, are dispersed in several chips in order to minimize the noise caused by the input/output pads of the semiconductor chip.

In the first embodiment of FIG. **6**, a single input/output signal IOS is transmitted to N (e.g. =3) semiconductor chips. By comparison, in the third embodiment shown in FIG. **10**, N

input/output signals IOS1, IOS2, and IOS3 are transmitted to N=3 semiconductor chips CHIP1, CHIP2, and CHIP3. Thus, N=3 input/output pads DQP11, DQP21, and DQP31 are required.

The N=3 input/output pads DQP11, DQP21, and DQP31, to which the input/output signals IOS1, IOS2, and IOS3 are directly transmitted, are dispersed in the N=3 semiconductor chips CHIP1, CHIP2, and CHIP3, thereby enabling minimization of noise. Referring to FIG. 10, the input/output pad DQP11, to which the first input/output signal IOS1 is directly transmitted, is installed on the first semiconductor chip CHIP1. The first input/output signal IOS1 is indirectly transmitted to the second and third semiconductor chips CHIP2, and CHIP3 via internal pads IP11, IP21, and IP31.

The input/output pad DQP21, to which the second input/output signal IOS2 is directly transmitted, is installed on the second semiconductor chip CHIP2. The second input/output signal IOS2 is indirectly transmitted to the first and third semiconductor chips CHIP1 and CHIP3 via internal pads IP12, IP22, and IP32.

The input/output pad DQP31, to which the third input/output signal IOS3 is directly transmitted, is installed on the third semiconductor chip CHIP3. The third input/output signal IOS3 is indirectly transmitted to the first and second semiconductor chips CHIP1 and CHIP2 via internal pads IP13, IP23, and IP33.

The first through 3rd input/output signals IOS1, IOS2, and IOS3 may be identical signals or respectively different signals.

The first through 3rd semiconductor chips CHIP1, CHIP2, and CHIP3 further include direct input/output pads DQP12, DQP22, and DQP32, which directly receive a predetermined external signal EXS input via corresponding pins (not shown) of the multi-chip package 1000. The external signal EXS is transmitted at a lower speed than the input/output signal IOS.

In similarity to the embodiment of FIG. 9, in the multi-chip package 1000 of FIG. 10, the signal may be transmitted to a semiconductor chip depending on a feature of the signal by using internal pads IP11, IP12, IP13, IP21, IP22, IP23, IP31, IP32, and IP33, or directly via direct input/output pads DQP12, DQP22, and DQP32.

The internal pads IP11, IP12, IP13, IP21, IP22, IP23, IP31, IP32, and IP33 can be coupled by using a common pad (not shown) installed at a substrate, in similarity to the first embodiment of FIG. 6. Also, the first through 3rd semiconductor chips CHIP1, CHIP2, and CHIP3 may include delay circuits (not shown) for controlling delay times of the input/output signals IOS1, IOS2, and IOS3, such that the input/output signals IOS1, IOS2, and IOS3 received by the first through 3rd semiconductor chips CHIP1, CHIP2, and CHIP3 are simultaneously input to the respective internal circuits.

FIG. 11 is a diagram of a multi-chip package according to a fourth embodiment.

The multi-chip package 1100 according to the fourth embodiment comprises first and second semiconductor chips CHIP1 and CHIP2, each of which includes a plurality of input/output pads DQP11, DQP12, DPQ21, and DQP22, a plurality of input/output drivers (not shown) coupled to the input/output pads, and an internal circuit (not shown). Each of the first and second semiconductor chips CHIP1 and CHIP2 includes internal pads IP11, IP12, IP13, IP14, IP21, IP22, IP23, and IP24. The total number of internal pads used for coupling the internal input/output drivers (not shown) with the internal circuits (not shown) equals the number of input/output drivers (not shown). The plurality of internal pads IP11, IP12, IP13, and IP14 in the first semiconductor chip CHIP1 are coupled to the plurality of internal pads IP21, IP22, IP23, and IP24 corresponding thereto in the 2nd semiconductor chip.

Among predetermined first through Mth (M>N, M is a natural number) input/output signals IOS1-IOS4 received via pins (not shown) of the multi-chip package 1100, the input/output signals are divided and transmitted directly to the input/output pads of the first and second semiconductor chips CHIP1 and CHIP2. The first and second semiconductor chips CHIP1 and CHIP2 indirectly receive the other input/output signals via the corresponding internal pads IP11, IP12, IP13, IP14, IP21, IP22, IP23, and IP24, which are coupled to each other.

Here, we suppose that N is set to 2 and M is set to 4.

In the third embodiment shown in FIG. 10, if the number of the input/output signals IOS1, IOS2, and IOS3 is equal to that of the semiconductor chips CHIP1, CHIP2, and CHIP3, an individual input/output signal is directly transmitted to only one semiconductor chip, and the other input/output signals are indirectly transmitted to the other semiconductor chips via internal pads.

In the fourth embodiment shown in FIG. 11, in similarity to the third embodiment, multiple input/output pads, to which input/output signals are transmitted, are divided and installed to reduce noise. However, unlike the third embodiment, the number of the input/output signals is more than that of the semiconductor chips. Similarly, if the input/output signals are divided into a proper number and then dispersed appropriately in semiconductor chips, the noise can be minimized.

In FIG. 11, there are 4 input/output signals IOS1, IOS2, IOS3, and IOS4 and 2 semiconductor chips CHIP1 and CHIP2. Thus, if 2 input/output signals are applied to each semiconductor chip, the noise caused by input/output pads, to which the input/output signals are transmitted, can be minimized in each semiconductor chip.

The internal pads IP11, IP12, IP13, IP14, IP21, IP22, IP23, and IP24 can be coupled using a common pad (not shown) installed at a substrate in similarity to the first embodiment shown in FIG. 6. Also, the first and second semiconductor chips CHIP1 and CHIP2 may include delay circuits (not shown) for controlling delay times of the input/output signals IOS1, IOS2, 10S3, and IOS4, such that the input/output signals IOS1, IOS2, IOS3, and IOS4 received by the first and second semiconductor chips CHIP1 and CHIP2 are simultaneously input to the respective internal circuits.

In similarity to the embodiment in FIG. 10, depending on a feature of the signal transmitted to the multi-chip package 1100 of FIG. 11, the signal can be transmitted to a semiconductor chip using the internal pads IP11, IP12, IP13, IP14, IP21, IP22, IP23, and IP24, or directly via direct input/output pads. This can be embodied by installing the direct input/output pads on each semiconductor chip as shown in FIG. 10.

FIG. 12 is a diagram of a third example of a method of connecting semiconductor chips in a multi-chip package 1200.

FIG. 12 illustrates only the first and second semiconductor chips CHIP1 and CHIP2. The coupling method will be described using the first and second semiconductor chips CHIP1 and CHIP2.

In FIG. 12, the first and second semiconductor chips CHIP1 and CHIP2 are arranged face-to-face. In FIG. 12: IP11, IP12, IP21, IP22 are internal pads; DQP11, DQP12, DQP21, DQP22 are input/output pads; BUMP1, BUMP2, BUMP3, BUMP4 are first bumps; SDQP1 and SDQP2 are wire bond pads; and WB1, WB2 are wire-bonds. On CHIP2, wire bond pads SDQP1 and SDQP2 are connected to corresponding input/output pads DQP21 and DQP22 by internal connections CON1 and CON2.

The internal pads IP11 and IP12 of CHIP1 are connected to IP21 and IP22, respectively, of CHIP2 by means of first bumps BUMP2 and BUMP3. Also the input/output pads DQP11 and DQP12 of CHIP1 are connected to DQP21 and DQP22, respectively, of CHIP2 by means of first bumps BUMP1 and BUMP4.

Meanwhile, the input/output pad DQP21 of CHIP2 is connected to a corresponding terminal (e.g., a pin) of the package by the internal connection CON1, wire bond pad SDQP1 and wire bond WB1. Also, the input/output pad DQP22 of CHIP2

is connected to a corresponding terminal (e.g., a pin) of the package by the internal connection CON**2**, wire bond pad SDQP**2** and wire bond WB**2**.

FIG. **13** is a diagram of a fourth example of a method of connecting semiconductor chips in a multi-chip package **1300**.

FIG. **13** illustrates only the first and second semiconductor chips CHIP**1** and CHIP**2**. The coupling method will be described using the first and second semiconductor chips CHIP**1** and CHIP**2**.

In FIG. **13**, the first and second semiconductor chips CHIP**1** and CHIP**2** are arranged face-to-face. In FIG. **13**: IP**11**, IP**12**, IP**21**, IP**22** are internal pads; DQP**11**, DQP**12**, DQP**21**, DQP**22** are input/output pads; BUMP**1**, BUMP**2**, BUMP**3**, BUMP**4** are first bumps; TSV**1** and TSV**2** are through silicon vias; and BUMP **5** and BUMP**6** are second bumps. On CHIP**2**, through silicon vias TSV**1** and TSV**2** connect input/output pads DQP**21** and DQP**22** to corresponding back pads disposed on the back of the semiconductor chip CHIP**2**.

The internal pads IP**11** and IP**12** of CHIP**1** are connected to IP**21** and IP**22**, respectively, of CHIP**2** by means of first bumps BUMP**2** and BUMP**3**. Also the input/output pads DQP**11** and DQP**12** of CHIP**1** are connected to DQP**21** and DQP**22**, respectively, of CHIP**2** by means of first bumps BUMP**1** and BUMP**4**.

Meanwhile, the input/output pad DQP**21** of CHIP**2** is connected to a corresponding terminal (e.g., a pin) of the package by TSV**1** and second bump BUMP**5**, and input/output pad DQP**22** of CHIP**2** is connected to a corresponding terminal (e.g., a pin) of the package by TSV**2** and second bump BUMP**6**.

FIG. **14** is a diagram of a fifth example of a method of connecting semiconductor chips in a multi-chip package **1400**.

In FIG. **14**, the semiconductor chips CHIP**1** through CHIP**5** are all arranged face-up. The internal pad IP**11** of CHIP**1** is connected to the internal pad IP**21** of CHIP**2** by means of a through silicon via (TSV) connecting IP**11** to a back pad on the back of CHIP**1**, and the back pad of CHIP**1** is connected to IP**21** by a bump. IP**31** is connected to IP**21**, IP**41** is connected to IP**31**, and IP**51** is connected to IP**41** each in the same manner.

Meanwhile, IP**51** of CHIP**5** is connected to a corresponding terminal (e.g., a pin) of the package by internal connection CON**1**, a TSV, a back pad, and a bump connecting the back pad of CHIP**5** and the package.

In one example, the method of connecting semiconductor chips illustrated in FIG. **14** may be applied to the multi-chip package **600** of FIG. **6**. In particular, in FIG. **6**, CHIP**1** directly receives the signal IOS through input/output pad DQP**11**. Similarly, in FIG. **14** CHIP**5** directly receives a signal at an input/output pad through a back pad, a bump, and a TSV. Also, in FIG. **6** the signal is provided on CHIP**1** from DQP**11** to internal pad IP**11**, and chips CHIP**2**~CHIPN receive the signal indirectly through a path from IP**11**~IPN**1**. Again, similarly, in FIG. **14** the signal is provided on CHIP **5** from the input/output pad to internal pad IP**51**, and chips CHIP**1**~CHIP**4** all receive the signal indirectly through a path from IP**51**~IP**11**.

FIG. **15** is a diagram of a sixth example of a method of connecting semiconductor chips in a multi-chip package **1500**.

In FIG. **15**, the semiconductor chips CHIP**1** through CHIP**5** are all arranged face-down. Otherwise, the connections of FIG. **15** are similar to those explained above with respect to FIG. **14**, and are further easily understandable from inspecting the drawing, and so a detailed description thereof is omitted. Also in similarity to the method illustrated in FIG. **14**, the method of connecting semiconductor chips illustrated in FIG. **15** may be applied to the multi-chip package **600** of FIG. **6**.

FIG. **16** is a diagram of a seventh example of a method of connecting semiconductor chips in a multi-chip package **1600**.

In FIG. **16**, the semiconductor chips CHIP**1** through CHIP**5** are all arranged face-up. The arrangement of FIG. **16** illustrates how a signal may be provided to any number of chips CHIP**1**~CHIP**5** by any combination of internal pads IP**11**~IP**51**, input/output pads, and internal connections on the chips.

In the specific example of FIG. **16**, the signal is provided from a corresponding terminal (e.g., a pin) of the package to CHIP**5** by a pack pad on the back of CHIP**5** and a TSV from the back pad to input/output DQP**51**. Then, the signal is provided from CHIP**5** to CHIP**4**, and from CHIP**4** to CHIP**3**, by input/output pads DQP**51**, DQP**41**, and DQP**31**, respectively, in combination with bumps, and back pads and TSVs of chips CHIP**3**~CHIP**4**. At CHIP**3**, the signal is provided from input/output pad DQP**31** to internal pad IP**31** by internal connection CON**1**. Then, the signal is provided from CHIP**3** to CHIP**2**, and from CHIP**2** to CHIP**1**, by internal pads on chips CHIP**1**~CHIP**3**, in combination with bumps, and back pads and TSVs of chips CHIP**1** and CHIP **2**.

As described above, the multi-chip package can improve signal compatibility by maintaining the parasitic load of a pin to at least the level of a single chip, when a signal is transmitted to the pin at high speed. Also, when a signal that is not necessarily transmitted at high speed is applied to a pin, semiconductor chips can be packaged according to the conventional method.

While the present invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

What is claimed is:

1. A multi-chip device, comprising:

a package including a plurality of terminals;

N semiconductor chips, each of which includes an input/output pad, an input/output driver coupled to the input/output pad, an internal circuit, and an internal pad disposed in a signal path in between the input/output driver and the internal circuit; and

one or more first connectors, each first connector coupling the internal pad of one of the N semiconductor chips to the internal pad of another one of the N semiconductor chips,

wherein the input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package, and

wherein a remaining (N−1) of the N semiconductor chips indirectly receive the input/output signal via the internal pads.

2. The multi-chip device as claimed in claim **1**, wherein the first connector includes a first bump which couples the internal pads to each other.

3. The multi-chip device as claimed in claim **2**, further comprising one or more second connectors coupling the internal pad of one of the N semiconductor chips to the internal pad of another one of the N semiconductor chips, wherein the second connector includes,

a second bump; and

a Through Silicon Via (TSV) passing through one of the semiconductor chips.

4. The multi-chip device as claimed in claim **3**, wherein the second connector further includes a back pad disposed on the back of the semiconductor chip, wherein the TSV of an i^{th} semiconductor chip couples the internal pad of the i^{th} semiconductor chip with the back pad of the i^{th} semiconductor

chip, and the second bump couples the back pad of the i^{th} semiconductor chip with the internal pad of an $(i+1)^{th}$ semiconductor chip.

5. The multi-chip device as claimed in claim **1**, wherein the input/output pad of the first semiconductor chip is coupled with the corresponding terminal of the package using one of the first connector and a second connector.

6. The multi-chip device as claimed in claim **5**, wherein the first connector includes a first bump which couples the internal pads each other.

7. The multi-chip device as claimed in claim **5**, wherein the second connector includes, a second bump; and a Through Silicon Via (TSV).

8. The multi-chip device as claimed in claim **1**, wherein the N semiconductor chips are stacked on each other, and the first semiconductor chip is located on a bottom of the N semiconductor chips adjacent the package.

9. The multi-chip device as claimed in claim **1**, wherein the N semiconductor chips are stacked on each other, and the first semiconductor chip is separated from the package by at least one other semiconductor chip.

10. A multi-chip device, comprising:

a package including a plurality of terminals;

N semiconductor chips, each of which includes an input/output pad, an input/output driver coupled to the input/output pad, an internal circuit, and an internal pad disposed in a signal path in between the input/output driver and the internal circuit; and

at least one first connector or second connector, each said connector coupling the internal pad of one of the N semiconductor chips to the internal pad of another one of the N semiconductor chips,

wherein the first connector includes a first bump, and the second connector includes a second bump and a Through Silicon Via (TSV),

wherein the input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package, and

wherein a remaining (N−1) of the N semiconductor chips indirectly receive the input/output signal via the internal pads.

11. The multi-chip device as claimed in claim **10**, wherein the internal pads of semiconductor chips which are arranged face to face are coupled to each other using the first connector, and the internal pads of semiconductor chips which are not arranged face to face are coupled to each other using the second connector.

12. The multi-chip device as claimed in claim **10**, wherein the input/output pad of the first semiconductor chip is coupled with the corresponding terminal of the package using one of the first connector and the second connector.

13. The multi-chip device as claimed in claim **12**, wherein the input/output pad of the first semiconductor chip is coupled with the corresponding terminal of the package using the first connector when the first semiconductor chip and the package are arranged face to face.

14. A multi-chip device, comprising:

a package including a plurality of terminals;

N semiconductor chips, each of which includes an input/output pad an input/output driver coupled to the input/output pad, an internal circuit, and an internal pad disposed in a signal path in between the input/output driver and the internal circuit; and

one or more first connectors, each first connector coupling one of the internal pad and the input/output pad of one of the N semiconductor chips to one of the internal pad and the input/output pad of another one of the N semiconductor chips,

wherein the input/output pad of a first one of the N semiconductor chips directly receives an input/output signal transmitted via a corresponding one of the terminals of the package,

wherein the internals pads of another X of the N semiconductor chips indirectly receive the input/output signal; and

wherein a remaining (N−X−1) of the N semiconductor chips indirectly receive the input/output signal via the input/output pads.

15. The multi-chip device as claimed in claim **14**, wherein the first connector includes a first bump which couples the internal pads or the input/output pads to each other.

16. The multi-chip device as claimed in claim **15**, further comprising one or more second connectors coupling one of the internal pad and the input/output pad of one of the N semiconductor chips to one of the internal pad and the input/output pad of another one of the N semiconductor chips, wherein the second connector includes,

a second bump; and

a Through Silicon Via (TSV) passing through one of the semiconductor chips.

17. The multi-chip device as claimed in claim **16**, wherein the second connector further includes a back pad disposed on the back of the semiconductor chip, wherein the TSV of an i^{th} semiconductor chip couples the internal pad or the input/output pad of the i^{th} semiconductor chip with the back pad of the i^{th} semiconductor chip, and the second bump couples the back pad of the i^{th} semiconductor chip with the internal pad or input/output pad of an $(i+1)^{th}$ semiconductor chip.

18. The multi-chip device as claimed in claim **14**, wherein the input/output pad of the first semiconductor chip is coupled with the corresponding terminal of the package using one of the first connector and a second connector.

19. The multi-chip device as claimed in claim **18**, wherein the first connector includes a first bump which couples the internal pads each other.

20. The multi-chip device as claimed in claim **18**, wherein the second connector includes,

a second bump; and

a Through Silicon Via (TSV)

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