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(54) **PRIMARY SIDE CONTROL CIRCUIT AND METHOD FOR ULTRA-LOW IDLE POWER OPERATION**

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See application file for complete search history.

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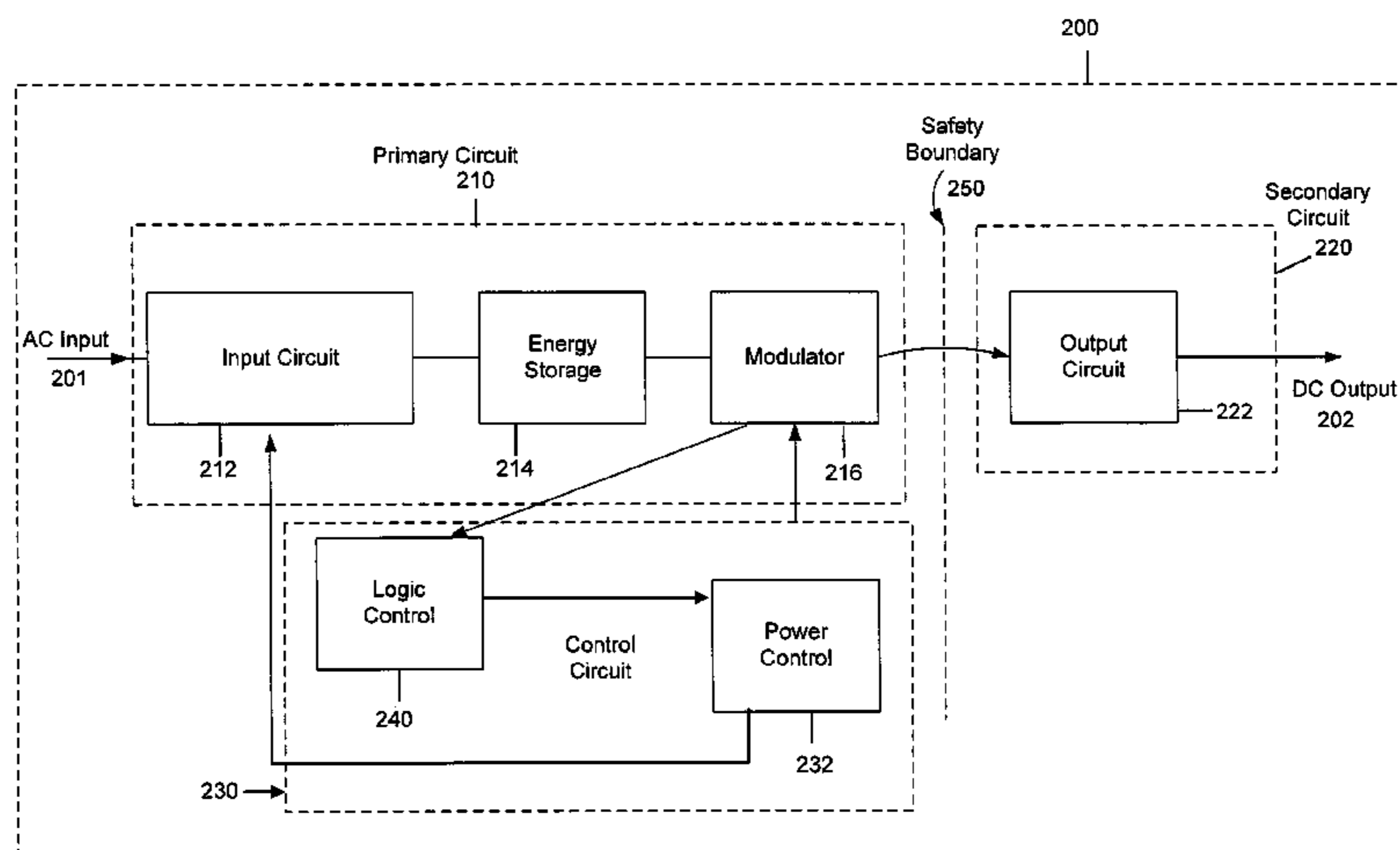
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(57) **ABSTRACT**

A method and circuit for reducing power consumption during idle mode to ultra-low levels, such as about $1/10^{th}$ to $1/1000^{th}$ or less of active power is disclosed. An ultra-low idle power supply comprises a primary circuit, a secondary circuit and a control circuit. The control circuit monitors behavior of the primary circuit and determines whether an idle state or no load condition exists, and if so the primary circuit is disengaged. By disengaging the primary circuit, the power consumption of the ultra-low idle power supply is reduced to ultra-low levels.

18 Claims, 4 Drawing Sheets



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Figure 1

100

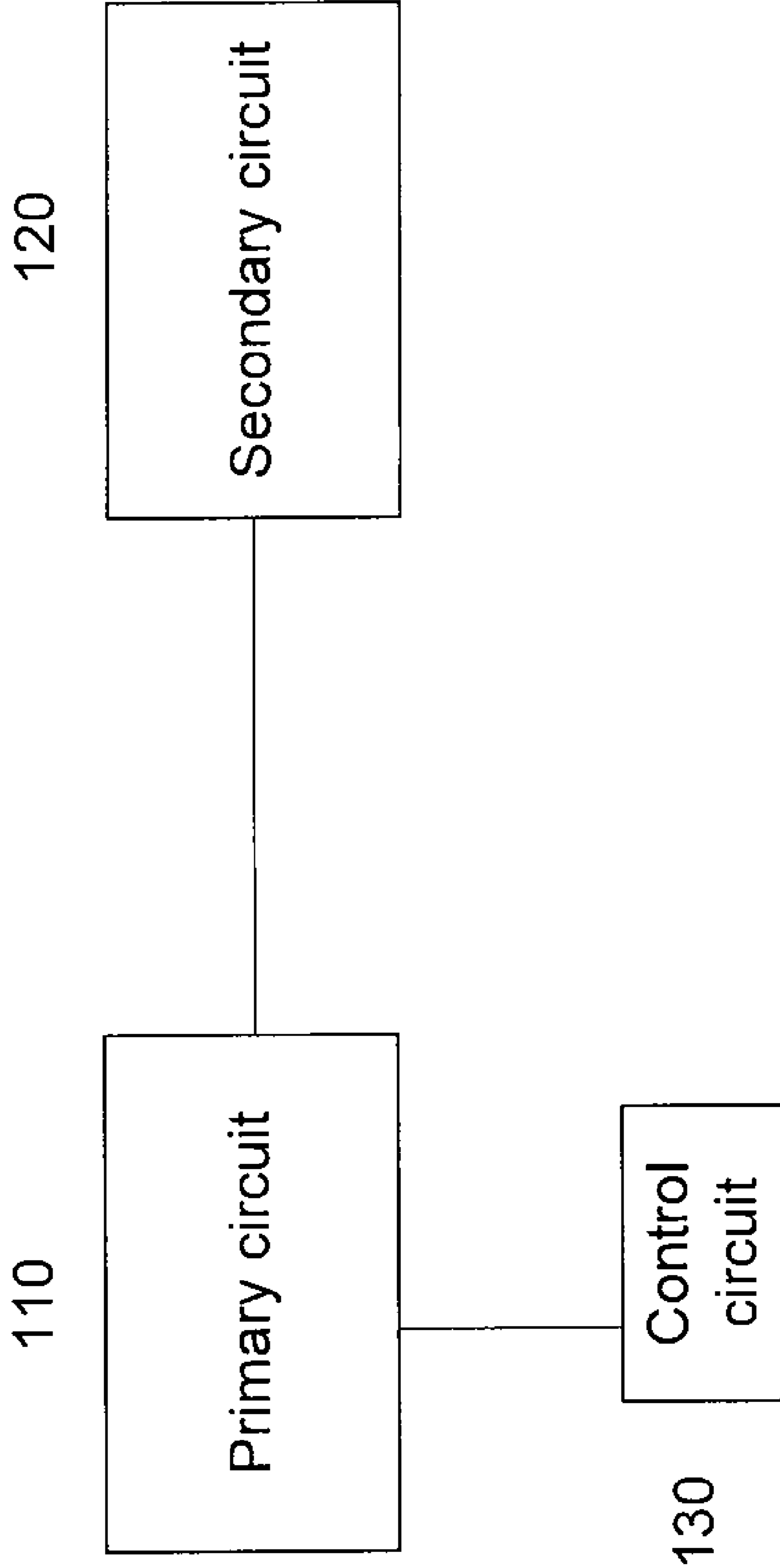
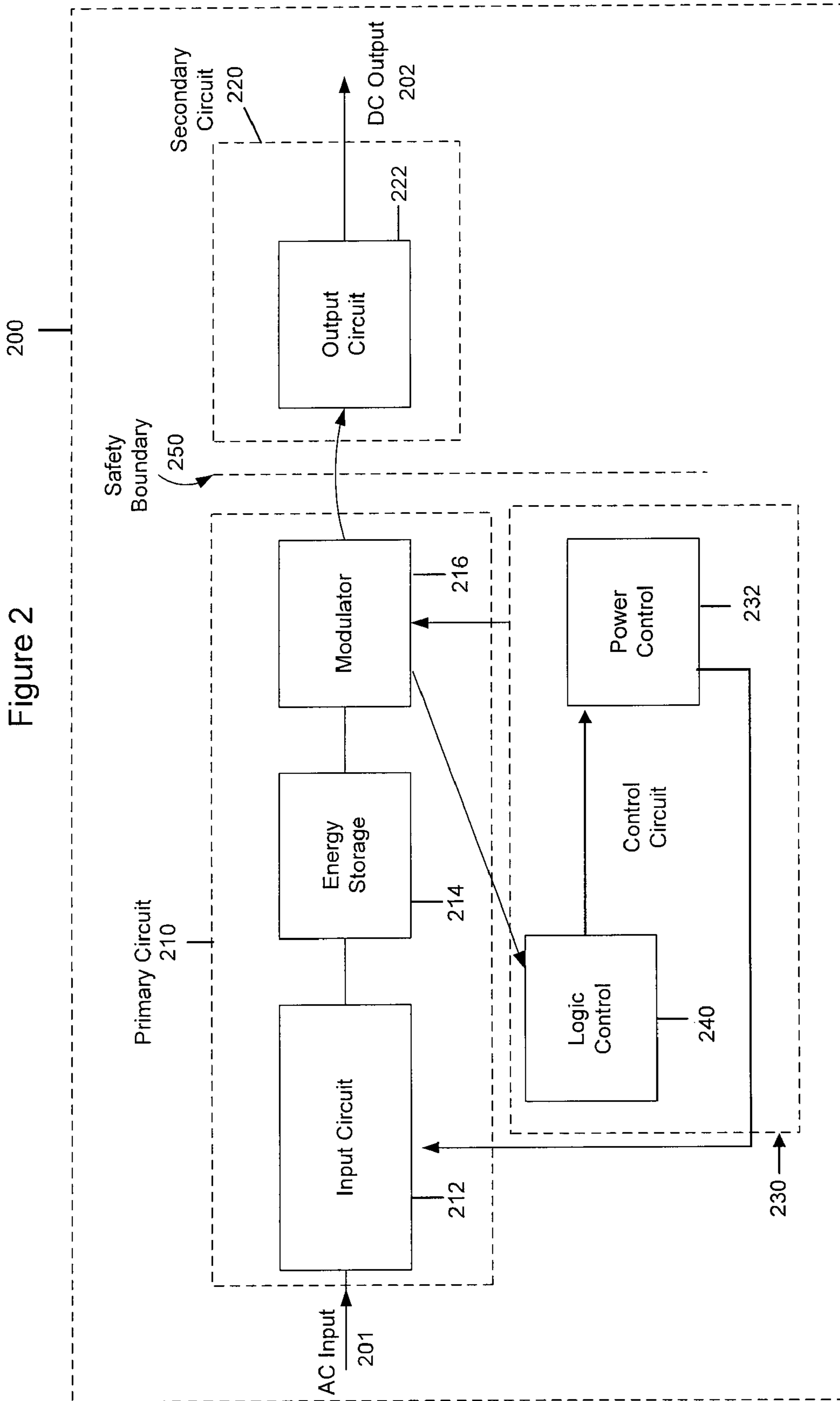


Figure 2



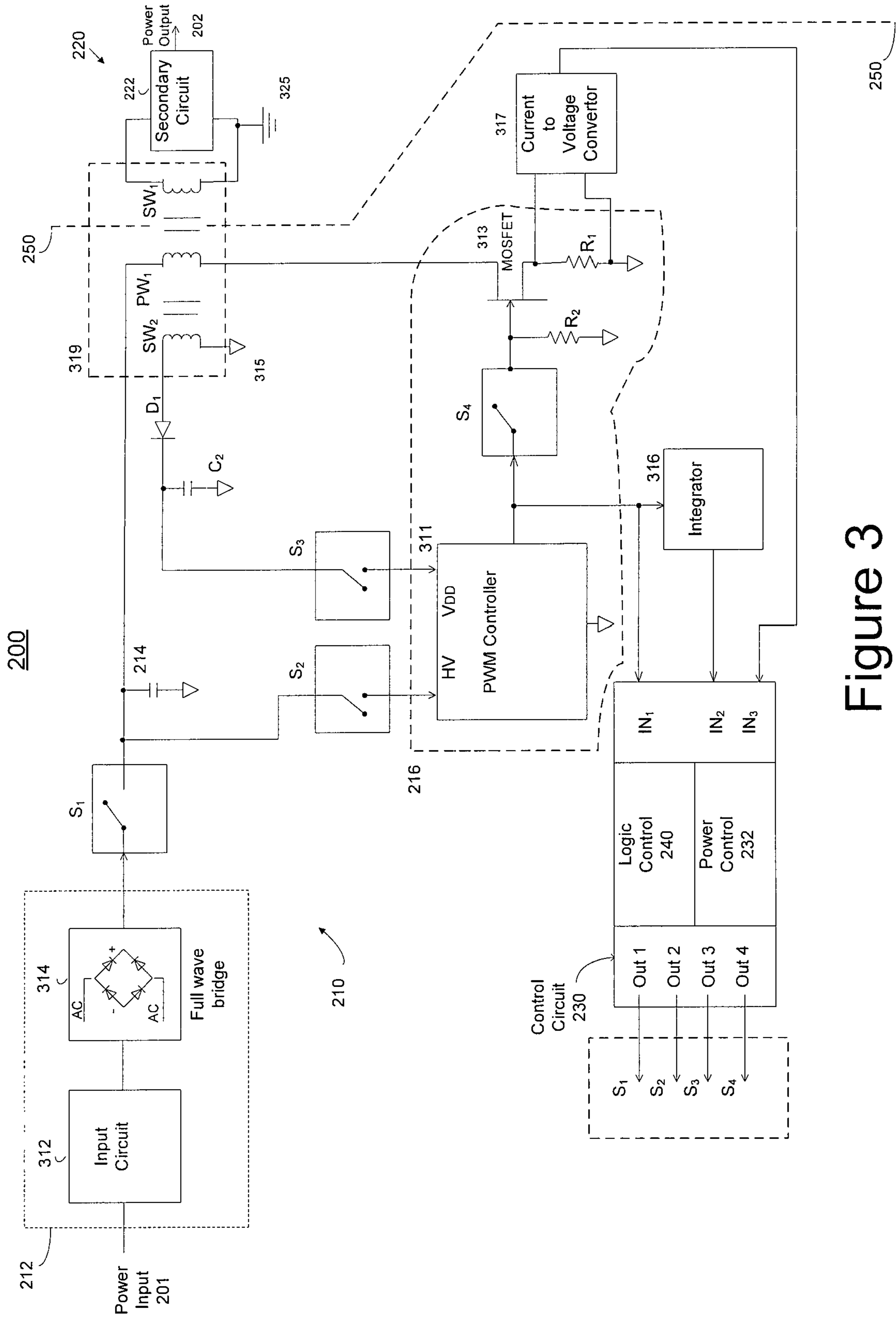


Figure 3

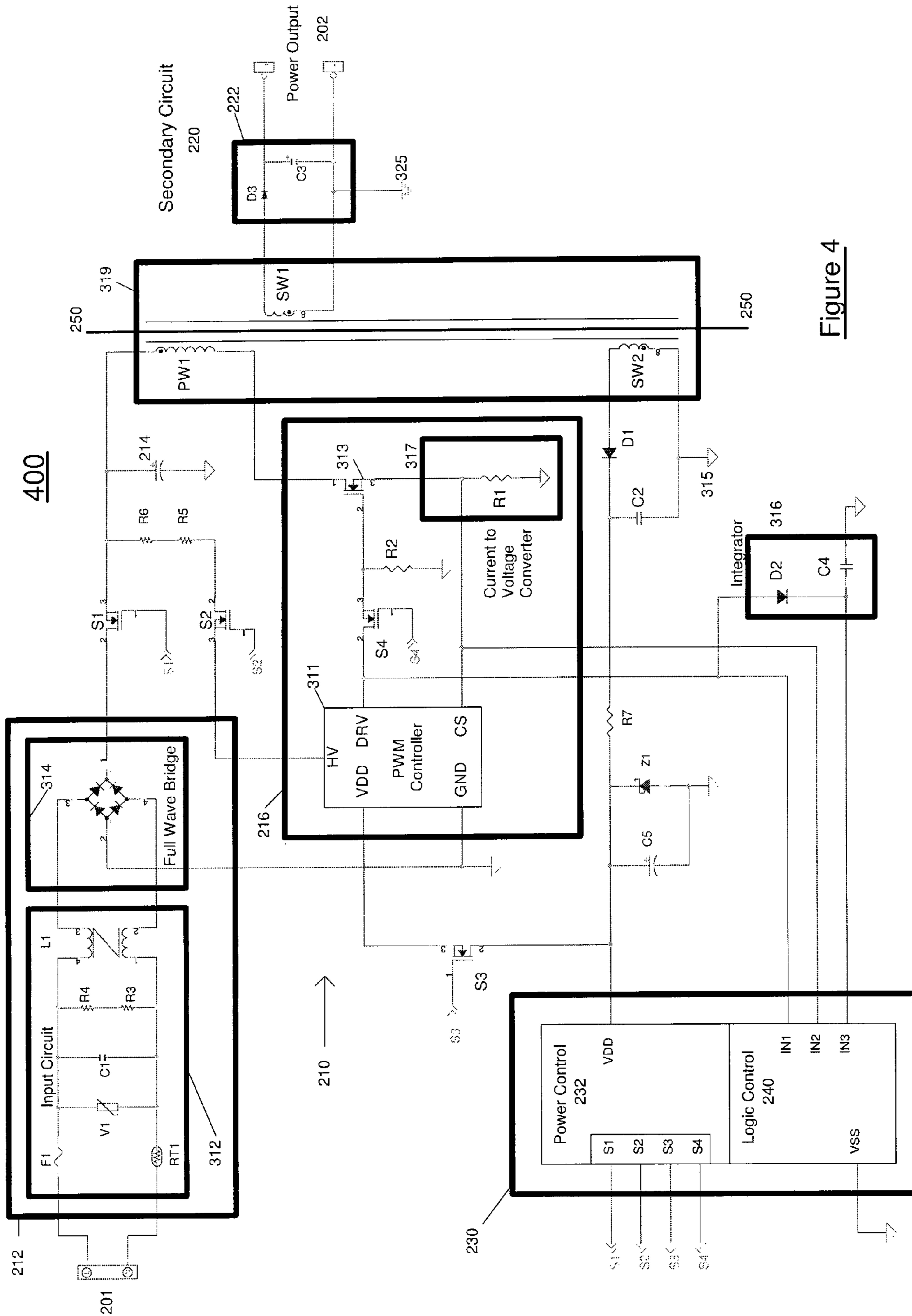


Figure 4

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PRIMARY SIDE CONTROL CIRCUIT AND METHOD FOR ULTRA-LOW IDLE POWER OPERATION

CROSS-REFERENCE TO RELATED APPLICATIONS

This applications claims priority to and benefit of U.S. Provisional Application No. 61/057,157, filed on May 29, 2008, and entitled "PRIMARY SIDE CONTROLLER MONITORING CIRCUIT AND METHOD", and hereby incorporated by reference.

FIELD OF INVENTION

The present invention relates to reducing power consumption in electronic devices. More particularly, the present invention relates to a circuit and method for initiating an ultra-low idle power mode in a power supply or device.

BACKGROUND OF THE INVENTION

The increasing demand for lower power consumption and environmentally friendly consumer devices has resulted in interest in power supply circuits with "green" technology. For example, on average, a notebook power adapter continuously "plugged in" spends 67% of its time in idle mode. Even with a power adapter which conforms to the regulatory requirements of dissipating less than 0.5 watts/hour, this extended idle time adds up to 3000 watt-hours of wasted energy each year per adapter. When calculating the wasted energy of the numerous idle power adapters, the power lost is considerable.

SUMMARY OF THE INVENTION

In accordance with various aspects of the present invention, a method and circuit for reducing power consumption during idle mode of a powered device to ultra-low levels, such as approximately $1/10^{th}$ to $1/1000^{th}$ or less of active power is disclosed. In an exemplary embodiment, an ultra-low idle power supply provides power to an electronic device, such as for example, a notebook computer, mobile phones, Bluetooth headsets, smartphones, MP3 players, and portable GPS systems. An ultra-low idle power supply may include a primary circuit, a secondary circuit, and a control circuit. The secondary circuit is coupled with the primary circuit, such as through an isolation device. The primary circuit receives control signals from the control circuit to suitably control the state of the primary circuit.

In an exemplary embodiment, the control circuit comprises a logic control unit than monitors and assesses whether the powered device is in an idle mode, and if so, will provide a control signal that is configured to control the state of the primary circuit by controlling a switching circuit to alter the primary circuit state. By disengaging and/or disabling the primary circuit, the power consumption of the power supply is substantially reduced to ultra-low levels during idle operation.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the Figures, where like reference numbers refer to similar elements throughout the Figures, and:

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FIG. 1 illustrates a block diagram of an exemplary power supply configured for reducing power consumption during idle mode in accordance with an exemplary embodiment;

FIG. 2 illustrates another block diagram of an exemplary power supply configured with a primary circuit for reducing power consumption during idle mode in accordance with an exemplary embodiment;

FIG. 3 illustrates a circuit diagram of exemplary power supply configured with a primary circuit for reducing power consumption during idle mode in accordance with an exemplary embodiment; and

FIG. 4 illustrates a circuit/schematic diagram of exemplary power supply configured with a primary circuit for reducing power consumption during idle mode in accordance with an exemplary embodiment.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS OF THE INVENTION

The present invention may be described herein in terms of various functional components and various processing steps. It should be appreciated that such functional components may be realized by any number of hardware or structural components configured to perform the specified functions. For example, the present invention may employ various integrated components, such as buffers, current mirrors, and logic devices comprised of various electrical devices, e.g., resistors, transistors, capacitors, diodes and the like, whose values may be suitably configured for various intended purposes. In addition, the present invention may be practiced in any integrated circuit application. However for purposes of illustration only, exemplary embodiments of the present invention will be described herein in connection with a switching power converter for use with power supply circuits. Further, it should be noted that while various components may be suitably coupled or connected to other components within exemplary circuits, such connections and couplings can be realized by direct connection between components, or by connection through other components and devices located thereinbetween.

In accordance with various aspects of the present invention, a power supply configured for reducing power during idle mode to ultra-low levels, such as about $1/10^{th}$ to $1/1000^{th}$ or less of active power is disclosed. In an exemplary embodiment, and with reference to FIG. 1, an ultra-low idle power supply **100** includes a primary circuit **110**, a secondary circuit **120**, and a control circuit **130**. In an exemplary embodiment, ultra-low idle power supply **100** provides power to an electronic device, such as for example, a notebook computer, mobile phones, Bluetooth headsets, smartphones, MP3 players, and portable GPS systems. In addition, the outside power source is either alternating current (AC) or direct current (DC) and connects with primary circuit **110**. Secondary circuit **120** is in communication with primary circuit **110**. Control circuit **130** monitors and controls the state of primary circuit **110**. While control circuit **130** is illustrated in FIG. 1 as a component connected to primary circuit **110**, control circuit **130** can also be integrated within or otherwise considered included within primary circuit **110**, as both components are part of the primary side of power supply **100**, and the embodiment shown is merely for illustration purposes. In an exemplary embodiment, the behavior and/or characteristics of primary circuit **110** are monitored and/or assessed. If the monitored behavior/characteristics of primary circuit **110** indicate that the electronic device is drawing substantially no power from ultra-low idle power supply **100**, control circuit **130** facilitates or controls disengaging or disabling of primary

circuit 110. In one embodiment, substantially no power is intended to convey that the output power is in the range of about 0-1% of a typical maximum output load. In an exemplary embodiment, control circuit 130 is configured to control the state of primary circuit 110 by controlling a switching circuit to alter the primary circuit state and change the operation modes of power supply 100, e.g., to disengage or disable input power from primary circuit 110. In an exemplary embodiment, control circuit 130 controls primary circuit 110 to change the modes of ultra-low idle power supply 100 in accordance with the input power level. However, various other conditions such as rate of operation of the primary circuit with other components, current levels and the like can also be observed and monitored.

By substantially disabling or disengaging primary circuit 110, the power consumption of ultra-low idle power supply 100 is reduced. In one embodiment, substantially disabling the primary circuit is configured such that primary circuit 110 switching circuits are static and drawing quiescent current only. In another embodiment, substantially disabling the primary circuit is configured such that switching circuits are no longer switching and that primary circuit 110 capacitors and secondary circuit capacitors 120 are static and charged with no ripple current. In yet another embodiment, substantially disabling the primary circuit is configured such that power is entirely removed from primary circuit 110.

In an exemplary embodiment, ultra-low idle power supply 100 has three modes: active, normal idle, and ultra-low idle. Active mode is the active functioning of ultra-low idle power supply 100 when powering an electronic device. Normal idle mode is when ultra-low power supply is connected to an input power source but not actively powering an electronic device. In an exemplary embodiment, ultra-low idle power supply 100 verifies that the current state is normal idle mode prior to switching to ultra-low idle mode.

During the ultra-low idle mode, primary circuit 110 is substantially disabled or disengaged, which substantially decreases the rate of power consumption compared to during the normal idle mode. Furthermore, in another embodiment, ultra-low idle power supply 100 can also comprise a low duty cycle "wake up" period to alter the idle time from constant idle to long periods of zero power and short periods of idle power.

In accordance with an exemplary embodiment, and with reference to FIG. 2, an ultra-low idle power supply 200 includes a primary circuit 210, a secondary circuit 220, and a control circuit 230. A safety boundary 250 separates primary circuit 210 and secondary circuit 220. Ultra-low idle power supply 200 receives a power input 201, which can be either AC or DC, and transmits a power output 202, which can also be either AC or DC, to an electronic device.

In an exemplary embodiment, primary circuit 210 includes an input circuit 212, an energy storage unit 214, and a modulator 216. Input circuit 212 is configured for protecting, filtering and/or rectifying input power to primary circuit 210. In one embodiment, input circuit 212 includes input EMI filters and a rectifier, and can comprise any other devices for protection, filtering and/or rectifying. Energy storage unit 214 is configured for smoothing rectified direct current and for storing energy. Energy storage unit 214 can comprise an energy storage capacitor, or any other energy storage device or circuit. Modulator 216 is configured for driving a dielectric isolation device, such as, for example, a transformer. In an exemplary embodiment, modulator 216 can include a PWM controller and/or a MOSFET.

In accordance with an exemplary embodiment, control circuit 230 monitors the behavior of primary circuit 210 and

facilitates control of the mode of ultra-low idle power supply 200 based on at least one of, or a combination of: the power transmitted through primary circuit 210, the rate of operation of primary circuit 210 components, the width of pulses in modulator 216, the ripple current in the storage capacitor contained in energy storage 214, the input current from AC input 201, the temperature of lossy components in primary circuit 210, and/or the current flow through the switch circuits within primary circuit 210. For example, if the output load is at substantially low power for about ten seconds, then control circuit 230 can facilitate changing ultra-low idle power supply 200 to ultra-low idle power mode. In an exemplary embodiment, ultra-low idle power supply 200 mode is changed due to selected criteria, and the criteria can comprise a fixed criterion, a template, and/or a learned criterion.

In accordance with an exemplary embodiment, control circuit 230 comprises a logic control unit 240 and a power control unit 232. Logic control unit 240 is configured to monitor primary circuit 210, e.g., by monitoring operation of modulator 216, and to output a control signal that feeds back information to primary circuit 210. In an exemplary embodiment, logic control unit 240 includes a monitoring and control device. The monitoring and control device may comprise a combinational logic machine, a state machine, and/or a microprocessor. Power control unit 232, which may comprise, for example, a combinational logic machine, a state machine, and/or a microprocessor, controls the operation of primary circuit 210, e.g., by controlling operation of modulator 216. For example, power control unit 232 can receive the control signal from logic control unit 240 and either enables or disables portions of modulator 216, such as by controlling operation of switches S_2 , S_3 , and/or S_4 .

In an exemplary embodiment, and with reference to FIGS. 2 and 3, primary circuit 210 conveys power to secondary circuit 220 through a transformer 319. Furthermore, primary circuit 210 connects to a first ground 315 and secondary circuit 220 connects to a second ground 325, isolated by safety boundary 250. In addition to comprising a full wave bridge circuit 314, an integrator 316, a current-to-voltage converter 317 having a resistor R1 and/or other components, and energy storage unit 214, primary circuit 210 can also be configured with modulator 216 having a Pulse Width Modulator (PWM) controller 311 and a MOSFET 313.

The components within modulator 216, such as PWM controller 311 and MOSFET 313, serve to chop the input DC from input circuit 212 at a high frequency rate to drive transformer 319 and transfer power from the primary (left side) of transformer 319 to the secondary (right side). The rate of chop or duty cycle is directly proportional to the load on output 202.

In an exemplary embodiment, PWM controller 311 may be monitored by logic control unit 240 for behavior that indicates ultra-low idle power supply 200 should change to ultra-low idle mode. PWM controller 311 comprises a discrete component with on/off states and a modulation rate. The on/off states of PWM controller 311 control the power transmitted to secondary circuit 220. For example, in one embodiment, the rate of pulses going from PWM controller 311 to a transistor switch in modulator 216, such as MOSFET 313, substantially affects the output power delivered at power output 202. In another embodiment, PWM controller 311 may use a variable width pulse train with a fixed rate to control power at power output 202. In yet another embodiment, PWM controller 311 may also use a combination of rate and width to control the power transmitted to secondary circuit 220.

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In an exemplary embodiment, when a normal light load condition is detected by PWM controller 311, the rate and pulse width is reduced substantially below normal loaded conditions. In an exemplary embodiment, substantially below normal is defined to be a pulse rate of less than about 1 kilohertz during conditions of loads in the range of about 1-90 watts. In another embodiment, substantially below normal is defined to be a pulse width of microseconds out of a period of milliseconds during idle conditions. Such changes in the output rate of PWM controller 311 can be sampled or detected at input IN1. For example, a DRV output of PWM controller 311 can be sampled by logic control unit 240 and the rate (frequency) of the drive pulses can be measured. At low power levels, PWM controller 311 will be operating in a low pulse rate mode often called "cycle skipping". Cycle skipping usually occurs when the load is below about 20 watts at power output 202, and the pulse rate will vary from a few hundred pulses/second to a few thousand as the load varies from near zero to about 20 watts. Furthermore, this transition to and operating in the lowered PWM rate and reduced width mode can be detected by logic control unit 240 monitoring the rate of pulses from PWM controller 311 observed from the output of integrator 316 at an input IN2 (wherein the pulse rate of a DRV output of PWM controller 311 can be integrated by integrator 316 to provide a DC voltage proportional to the load at 202), and/or current-to-voltage converter 317 at an input IN3 (wherein the current in MOSFET switch 313 is converted to a voltage by resistor R1, and the resulting current varies in proportion to the load current at power output 202). In one embodiment, reduced width may also be described as reduced duty cycle, where the duty cycle refers to the ratio of the time the PWM output pulse is active, or high, or driving a switching element to the rate or period of the PWM signal.

Once detected, logic control unit 240 may further reduce the power by suspending switching in modulator 216 and otherwise within primary circuit 210. In an exemplary embodiment, the switching is suspended by logic control unit 240 sending signals to switches S_2 , S_3 , and/or S_4 to disconnect PWM controller 311 from its power inputs, HV (high voltage input) and V_{DD} (controller operating voltage), and its drive to MOSFET 313.

In accordance with an exemplary embodiment, the power from primary circuit 210 transfers across safety boundary 250, via transformer 319, to secondary circuit 220. Safety boundary 250 creates no direct contact between the primary and secondary circuits to prevent unwanted transfer of electricity. In an exemplary embodiment, safety boundary 250 includes a dielectric isolation component. Dielectric isolation component may comprise a transformer, a capacitive coupling, or an opto-coupler. Furthermore, dielectric isolation component may be any component suitable to meet the criteria of safety requirement Underwriters Laboratory 60950. In accordance with safety regulations, safety boundary 250 is present in embodiments comprising AC into primary circuit 210 and transmitting DC power from the secondary circuit. In additional embodiments, the safety boundary may be present but is not required, or may not be present altogether. For example, there may not be a safety boundary in an embodiment with DC input and DC output.

In an exemplary embodiment, transformer 319 comprises a primary winding PW_1 , a secondary winding SW_1 , and a secondary winding SW_2 . Secondary winding SW_2 provides operating power to PWM controller 311 through switch S_3 , while secondary winding SW_1 provides the output voltage for secondary circuit 220. Diode D_1 and capacitor C_2 within primary circuit 210 serve to rectify and smooth the AC output of secondary winding SW_2 so the input V_{DD} to PWM con-

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troller 311 is direct current (DC). In an exemplary embodiment, PWM controller 311 includes a high-voltage (HV) input in communication with energy storage capacitor 214 and controlled by switch S_2 . The HV input is used to initiate the function of PWM controller 311 at power on, with the V_{DD} input providing normal operating voltage once the PWM controller 311 is driving MOSFET 313 and primary winding PW_1 . In an exemplary embodiment, at power "on" state, switches S_1 - S_4 are normally closed so PWM controller 311 can power up and function normally.

In an exemplary embodiment, secondary circuit 220 further includes an output circuit 222. Output circuit 222 is configured to convert the power from primary circuit 210 into a desired power load at power output 202 for an electronic device. In an exemplary embodiment, output circuit 222 includes a filter capacitor. In another embodiment, where ultra-low idle power supply 200 receives AC power and transmits DC power, output circuit 222 may include at least one rectifier.

Control circuit 230 is configured to control the state of primary circuit 210 by controlling switches S_1 - S_4 to control modulator 216. Switches can comprise FET-type transistor switches, or can comprise relays, such as solid state or Triac or latching type relays, or any other switching device or mechanism suitable for power supplies. In accordance with an exemplary embodiment, control circuit 230 uses power control unit 232 to control the operation of modulator 216 through switches S_2 - S_4 . Power control unit 232 receives the control signal from logic control unit 240 and either enables or disables portions of switch element 216 by controlling switches S_2 , S_3 , and/or S_4 . The enabling or disabling of switch element 216 is dictated by a power control signal communicated from power control unit 232. The power control signal has at least two states; normal idle and ultra-low idle. In addition, in an exemplary embodiment, control circuit 230 retains its present state in memory. In one embodiment, the memory is implemented using a transistor latch. Furthermore, in an exemplary embodiment, the default unprogrammed state of control circuit 230 is normal idle.

In an exemplary embodiment, selection of the current mode is based on the historic rate of PWM controller 311. This historic rate may be determined by logic control unit 240 monitoring input IN_1 from the output of PWM controller 311. A template can be determined based upon the past rate of PWM controller 311 and used to determine which mode the ultra-low idle power supply should be operating. For example, the template can determine that once PWM controller 311 is in idle mode for more than 15 minutes, this usage can indicate the output device will not require an active power supply for a long duration of time and the ultra-low idle power supply should switch to the ultra-low idle mode.

In one embodiment, ultra-low power consumption is less than about 0.5 Watts. In another embodiment, ultra-low power consumption is about $1/10^{th}$ to $1/1000^{th}$ or less of the active state power. In one embodiment, for example, the power supply consumption during normal idle mode is about 300 mW, and the power consumption during ultra-low idle mode is between about 0 mW and about 300 mW.

Such an ultra-low idle power supply circuit can be useful in various applications. For example, an ultra-low idle power supply can decrease wasted power consumption when used to power electronic devices such as a laptop, mobile phones, Bluetooth headsets, smartphones, MP3 players, video game systems, and portable GPS systems. In an exemplary embodiment, ultra-low idle power supply 200 can decrease wasted power consumption on an electronic device using an AC off-line switcher.

Various other features, devices and functions can be included within power supply **200** to facilitate improvement operation and/or to provide feedback information. For example, in an exemplary embodiment, although not illustrated in FIG. **2** or **3**, ultra-low idle power supply **200** can include a physical mechanical standby switch located at either the connection tip or at the body of the power supply. The standby switch may be used to manually change the mode of ultra-low idle power supply **200** from active mode or normal idle mode to the ultra-low idle power mode. In addition, in an exemplary embodiment, ultra-low idle power supply **200** includes at least one illuminated indicator to show the mode of the power supply. In another embodiment, ultra-low idle power supply **200** includes a device to indicate statistics relating to power consumption. For example, the device may be a gauge, a display such as LCD or LED, and the statistics may include watts saved, power levels, efficiency of the power supply, and the like. In another embodiment, logic control unit **240** monitors ambient light conditions and determines whether it is dark. In accordance with an exemplary method of operation, and with reference to FIGS. **2** and **3**, when power supply **200** is first connected to power input **201**, power supply **200** functions normally and responds to load conditions by supplying output power to the electronic output device. Control circuit **230** initiates in the normal idle mode, while logic control unit **240** monitors the behavior of modulator **216** through inputs IN_1 - IN_3 , and determines whether the power output is lightly loaded or not loaded over some period of time.

In an exemplary embodiment, power supply states are changed from normal idle to ultra-low idle when the power output load is below a predetermined threshold. The predetermined threshold may be fixed, dynamic, and/or learned. In one embodiment, a light load is any power output load falling below the predetermined threshold.

If light activity, or no activity, is detected at modulator **216**, logic control unit **240** will send a change/control signal to power control unit **232**. Once the signal is received, power control unit **232** will change states from normal idle to ultra-low idle. Furthermore, power control unit **232** communicates another signal to switches S_2 , S_3 , and S_4 , thereby disabling modulator **216** by opening switches S_2 , S_3 , and S_4 . Once modulator **216** is disabled, the power wasted in the switching elements is eliminated and only very small leakage currents from energy storage unit **214** are lost. As a result, the circuits that consume power are disconnected and power supply **200** goes “dead”, and wherein during the disconnect time the power consumed by components connected to the AC input is greatly minimized.

In an exemplary method of operation, if logic control unit **240** signals power control unit **232** to close switches S_2 , S_3 , and S_4 , logic control unit **240** then monitors the behavior of modulator **216**. If the switching frequency or rate increases within modulator **216**, thereby indicating a demand for load at power output **202**, logic control unit **240** signals power control unit **232** to change states back to normal idle mode. In an exemplary embodiment, ultra-low idle power supply **200** remains in normal idle mode until the load conditions indicate a reduced or “zero” power state. In another exemplary embodiment, logic control unit **240** may include an internal timer to periodically alter the ultra-low idle power supply state back to normal idle, so that the secondary circuit components can maintain power.

In an exemplary embodiment, energy storage unit **214** is connected to power input **201** through switch S_1 periodically even when ultra-low idle power supply **200** is in the ultra-low idle mode. This results in a rapid shift from ultra-low idle

mode to normal idle mode, or active mode, without the delay of recharging energy storage unit **214**. This occurs despite switching elements **216** being disabled during ultra-low idle mode. With reference to FIG. **4**, additional details and operational features can be further disclosed in connection with another exemplary embodiment of a power supply **400**. In accordance with this exemplary embodiment, input circuit **212** comprises an input circuit **312** and a rectifier **314**. Input circuit **312** comprises an RC filtering circuit for AC input power at input terminals **210** and can be structured or rearranged in various manners for providing surge protection and/or filtering functions. Rectifier **314** comprises a full-wave bridge rectifier circuit, but likewise can comprise various other rectifier configurations. In the exemplary embodiment, switches $S1$ - $S4$ comprise FET-type switches, but can also be suitably replaced with various other switching devices and components, such as relays. Switches $S1$ - $S4$ are configured to disconnect power drains from their sources. Integrator **316** comprises diode **D2** and capacitor **C4** for use by logic control unit **240**. To provide conditioned power for PWM controller **311** and power control **232**, primary circuit **210** further comprises a circuit comprising diode **D1**, capacitor **C2**, resistor **R7**, zener-diode **Z1** and capacitor **C5**. Secondary circuit **220** comprises diode **D3** and capacitor **C3** which serve to rectify and filter the pulsating output of secondary winding **SW1** for use by power output **202**.

During start-up of power supply **400**, all FET switches $S1$ - $S4$ are in the “closed” condition, allowing power supply **400** to start up normally. Switches $S1$ - $S4$ may be of the N or P channel variety as required, although N channel is shown. The DC output of input circuit **212** passes through FET switch **S1** and charges energy storage unit **214**. As the voltage is rising on energy storage unit **214**, a small amount of current is “picked off” by resistors **R4** and **R5** through FET switch **S2** and fed to the HV input of PWM controller **311**. This HV (high voltage) input current begins to start up circuits in PWM controller **311**, and on output DRV (Drive) of PWM controller short pulses begin to appear. These pulses travel through FET switch **S4** to the gate of MOSFET **313**. This gate drive to MOSFET **313** causes MOSFET **313** to switch on and off, wherein this switching drives the **PW1** primary winding of transformer **319**. Transformer secondary winding **SW2** receives the driving pulses through the transformer coupling and provides a pulsating output voltage to diode **D1**. Diode **D1** and capacitor **C2** rectify and filter the pulses and produce an unregulated DC voltage to resistor **R7**. Resistor **R7** current limits this DC voltage before it reaches zener diode **Z1** and bulk capacitor **C5**. Capacitor **C5** is a large value capacitor that serves to keep power control **232** powered when the rest of power supply **400** is shut off by control circuit **230**. The voltage on zener diode **Z1** and capacitor **C5** is a regulated and smoothed DC voltage that is used by power control **232** and is also fed to PWM controller **311** through FET switch **S3** to input VDD (main power input) of PWM controller **311**. Once PWM controller **311** senses a stable input on its VDD input, PWM controller **311** will widen the pulse width on the DRV output and increase the frequency of the pulses. This start-up process causes transformer secondary **SW1** to receive the wider high frequency pulses and produce a DC voltage output from **D3** and **C3** at power output **202**. The voltage level at **202** is fed back to PWM controller **311** (feedback path not shown for clarity) by methods known to one in the field. This feedback process completes the regulation loop and at this point the power supply is operating normally.

As to load level detection, during normal operation when power levels are in the about 20 watts to maximum output power range, PWM controller **311** will typically produce

output pulses of varying width up to about a 50% duty cycle and at a fixed frequency of about 60 KHz (60,000 pulses per second). As the load at power output **202** varies over this output range, the feedback in power supply **400** will cause PWM controller **311** to adjust the output pulses at the DRV output to regulate the output voltage at **202**. When the output load is between about 20 watts down to virtually no load, the output pulses of PWM controller **311** will be of shorter duration and less frequent in proportion to the load at power output **202**. Logic control unit **240** will use this pulse information received at inputs IN1-IN3 to determine the approximate load at power output **202**, and will cause power control unit **232** to change the function of modulator **216** based on the load at power output **202**.

When logic control unit **240** has monitored inputs IN1-IN3 and has determined that a low load or zero load condition exists on power output **202**, logic control unit **240** will cause power control unit **232** to send signals to operate switches S1-S4 to selectively disconnect circuits on the primary side to reduce idle power levels. For example, control circuit **230** will first open FET switches S3 and S2, removing all power to PWM controller **311**. Second, FET switch S4 can be opened to remove any residual drive to the gate of MOSFET **313**. This prevents MOSFET **313** from turning on due to leakage currents from the DRV output of PWM controller **311**. Lastly, FET switch S1 is opened to remove the rectified DC coming to energy storage unit **214** from input circuit **212**. At high input voltages, the leakage current required to keep energy storage unit **214** fully charged is significant.

Once modulator **216** and other primary side circuits are isolated by the switches S1-S4, only logic control unit **240** and power control unit **232** are powered by virtue of the charge on bulk capacitor C5. In an exemplary embodiment, capacitor C5 will be of a value large enough to power logic control unit **240** and power control unit **232** for several tens of minutes. During the time the other circuits are dead, i.e., without power, logic control unit **240** and power control unit **232** are in a low power sleep mode that draws only nano-amperes from capacitor C5. Periodically logic control unit **240** can wake up and instruct **232** to close FET switch S1 briefly to keep energy storage unit **214** charged. This pre-charge of **214** will allow the system to start up quickly when operation is restored.

To determine when to turn back on or power up, logic control unit **240** senses the voltage at input VDD of power control unit **232** and will re-energize power supply **400** when either a) the voltage on input VDD of power control unit **232** is reaching a critically low level and must be recharged, or b) after a period of minutes has elapsed. Power control unit **232** will close all four switches S1-S4 simultaneously to re-establish the initial start up conditions of the system at power on. This start up process will be faster than a "cold" power-off start-up because energy storage unit **214** has been kept charged. As power supply **400** starts up, bulk capacitor C5 will be re-charged to continue the supply of voltage to input VDD of power control unit **232**.

Once power supply **400** is up and running as measured by logic control unit **240** from the signals at inputs IN1-IN3, logic control unit **240** will again make measurements and determine power levels. If during the off time the load at power output **202** has increased, then logic control unit **240** will allow power supply **400** to run normally. If the power output **202** load is continuing to be low or near zero, logic control unit **240** will again signal the FET switches S1-S4 with power control unit **232** to set power supply **400** into the low power state.

The present invention has been described above with reference to various exemplary embodiments. However, those skilled in the art will recognize that changes and modifications may be made to the exemplary embodiments without departing from the scope of the present invention. For example, the various exemplary embodiments can be implemented with other types of power supply circuits in addition to the circuits illustrated above. These alternatives can be suitably selected depending upon the particular application or in consideration of any number of factors associated with the operation of the system. Moreover, these and other changes or modifications are intended to be included within the scope of the present invention, as expressed in the following claims.

The invention claimed is:

1. A power supply with a primary side and a secondary side, wherein said power supply is configured with an ultra-low idle power mode, said power supply comprising:

a primary circuit on the primary side, wherein said primary circuit is configured to receive power from an outside power source;

a control circuit on the primary side, wherein said control circuit is configured to monitor said primary circuit and to control said primary circuit such that said primary circuit is substantially disabled in response to detection of an idle power mode;

a secondary circuit on the secondary side, wherein said secondary circuit is coupled to said primary circuit and configured to provide a power output; and

wherein said control circuit monitors at least one of a duty cycle or a switching rate within said primary circuit to determine whether a power level of said power supply is above or below a predetermined threshold.

2. The power supply of claim 1, wherein said control circuit comprises a logic control unit configured for monitoring said primary circuit and a power control unit configured for control of said primary circuit.

3. The power supply of claim 2, wherein said logic control unit and said power control unit comprise at least one of a combinational logic machine, a state machine or a microprocessor.

4. The power supply of claim 2, wherein said primary circuit comprises a modulator circuit configured for driving at least one of a transformer or other dielectric isolation device.

5. The power supply of claim 4, wherein said logic control unit is configured to monitor a signal of said modulator circuit.

6. The power supply of claim 4, wherein said power control unit is configured for control of at least one switch to control said modulator circuit.

7. The power supply of claim 4, wherein said modulator circuit comprises a PWM controller and at least one of a MOSFET or other transistor driver.

8. A primary side circuit configured to facilitate an ultra-low idle power mode in a power supply, said primary side circuit comprising:

an input circuit configured for filtering and rectifying input power;

an energy storage circuit coupled to said input circuit;

a modulator coupled to said energy storage circuit, said modulator configured for modulating the input power at a high frequency rate to drive a transformer and transfer power from a primary side of said transformer to a secondary side of said transformer; and

wherein said primary side circuit is in communication with a control circuit on a primary side of said power supply, and wherein said control circuit is configured to monitor at least one of a duty cycle or a switching rate of said

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modulator and to control said primary side circuit such that said primary side circuit is substantially disabled in response to said control circuit determining that substantially no load exists such that said power supply transitions to an ultra-low idle power mode.

9. The primary side circuit of claim **8**, wherein said control circuit comprises a logic control unit configured for monitoring said modulator and a power control unit configured for control of said primary side circuit.

10. The primary side circuit of claim **8**, wherein said modulator comprises a PWM controller and at least one of a MOS-FET or other transistor driver.

11. The primary side circuit of claim **9**, wherein said logic control unit comprises at least one input coupled to said modulator to monitor said at least one of said duty cycle or said switching rate of said modulator.

12. The primary side circuit of claim **11**, wherein said at least one input coupled to said modulator monitors at least one of an output pulse rate directly from a PWM controller within said modulator, an output from an integrator coupled to said PWM controller within said modulator, and an output from a current-to-voltage converter coupled to said PWM controller within said modulator.

13. The primary side circuit of claim **9**, wherein said primary side circuit comprises at least one switch device coupled between said power control unit and said modulator, whereby said power control unit opens said at least one switch device to disable said modulator.

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14. A method of facilitating a power supply with ultra-low power consumption during idle power operation, said method comprising:

monitoring, using a control circuit in communication with a primary circuit on a primary side of said power supply, at least one of a duty cycle or a switching rate of said primary circuit of said power supply and determining if substantially no load condition exists; and

substantially disabling, using said control circuit, said primary circuit of said power supply in response to said substantially no load condition being detected to result in an ultra-low power mode.

15. The method according to claim **14**, said method further comprising enabling said power supply in response to said control circuit determining a power load exists.

16. The method of claim **14**, wherein said determining if substantially no load condition exists comprises detecting if at least one of a low duty cycle or a switching rate is present within said primary circuit.

17. The method of claim **15**, wherein said enabling said power supply occurs in response to at least one of a duty cycle or a switching rate of said primary circuit increasing above a threshold level.

18. The method of claim **14**, wherein said power supply is substantially disabled for an indeterminate period of time.

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