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(54) **MULTIPLEXER CIRCUIT WITH COMBINED LEVEL SHIFTING AND DELAY CONTROL FUNCTIONS**

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(51) **Int. Cl.**
H03K 7/00 (2006.01)

(52) **U.S. Cl.** **327/407**; 327/287; 327/563

(58) **Field of Classification Search** 327/407–408, 327/158, 359, 280, 287
See application file for complete search history.

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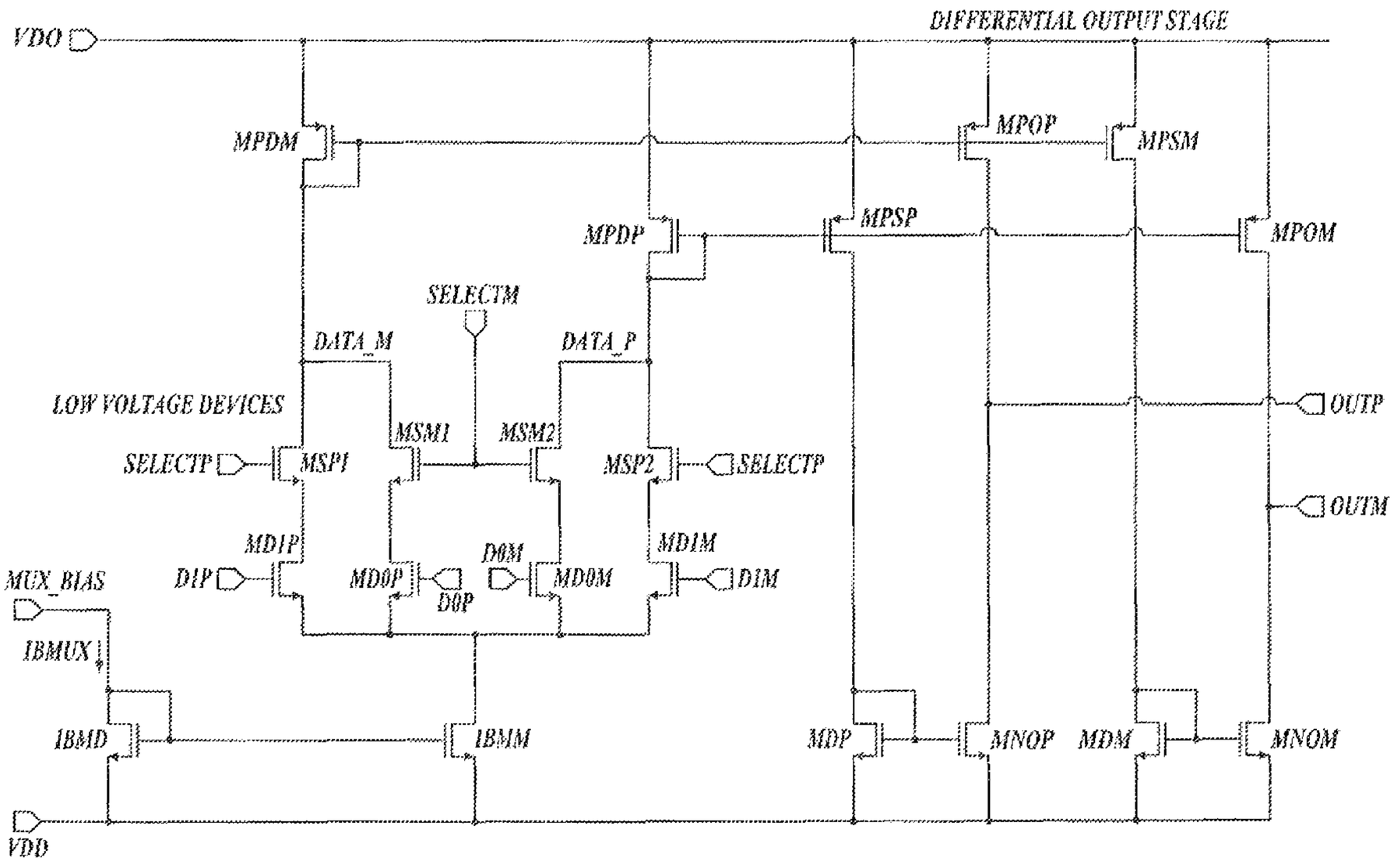
Primary Examiner—Quan Tra

(57) **ABSTRACT**

A digitally controlled circuit is arranged to provide the combined functions of level shifting, multiplexing, and delay control functions. The circuit is compact, and uses lower power and lower overall noise susceptibility over other solutions. A programmable bias current is arranged to adjust the delay through the circuit. The bias current can be provided by a digitally controlled current source, a binary weighted current DAC, or other digitally controlled means. The multiplexing functions are provided by an input stage circuit that is current limited by the programmable bias current. An output stage is arranged to convert signals from the input stage to a desired voltage level.

18 Claims, 6 Drawing Sheets



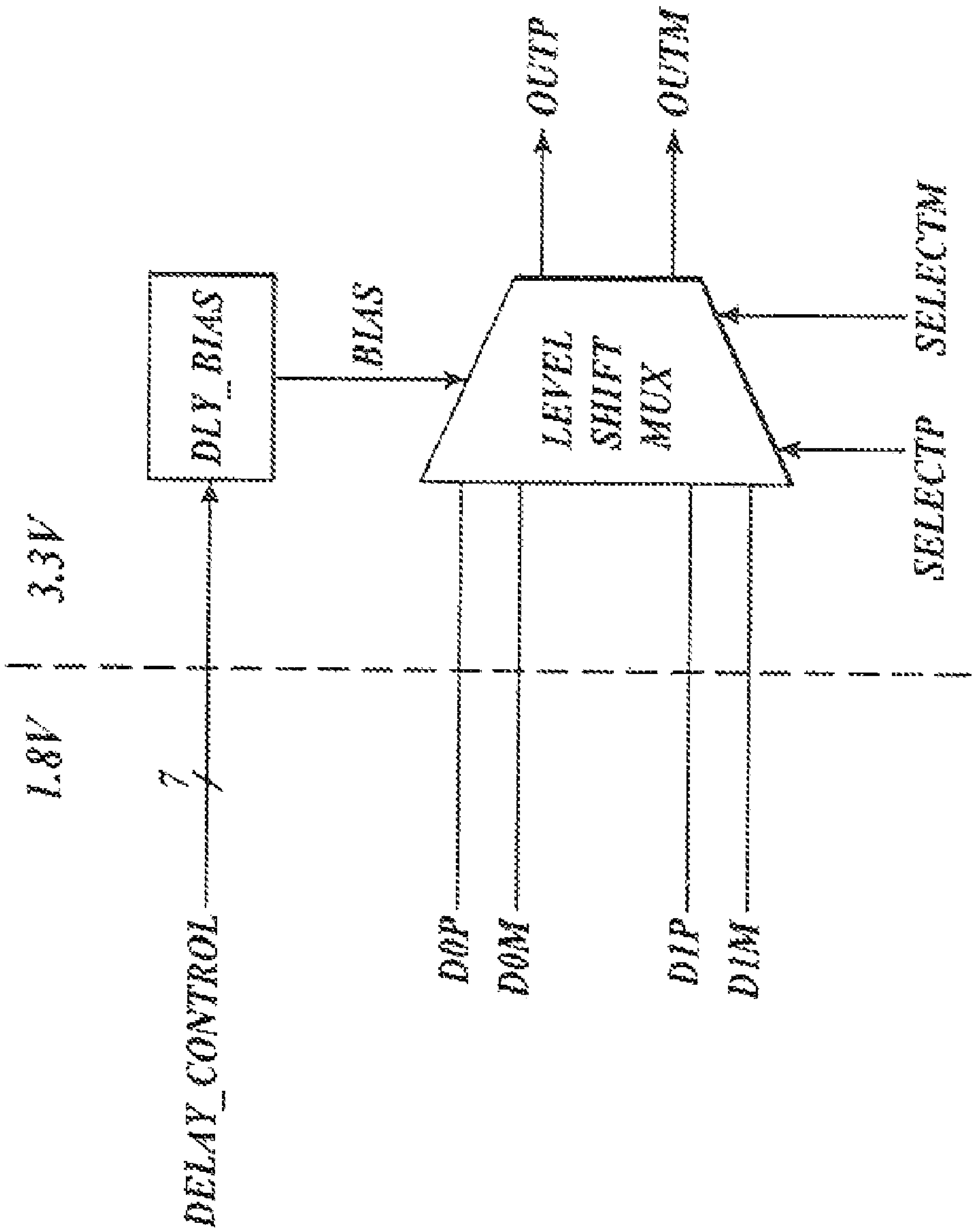

1.8V
3.3V
DELAY_CONTROL
7
DLY_BIAS
BIAS
LEVEL
SHIFT
MUX
OUTP
OUTM
SELECTM
SELECTP
D0P
D0M
D1P
D1M

FIG. 1

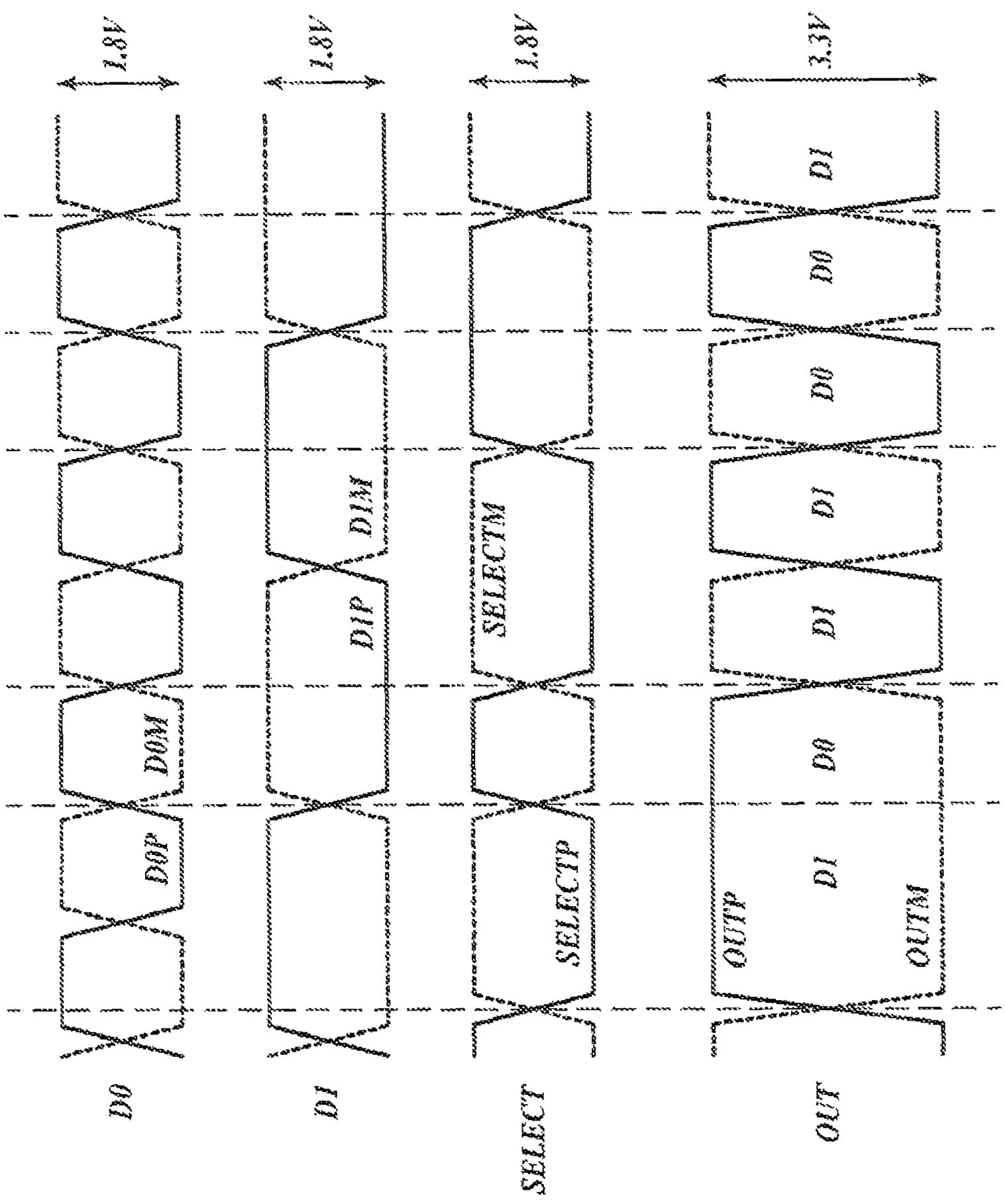

1.8V
1.8V
1.8V
3.3V
D0P
D0M
D1P
D1M
SELECTP
SELECTM
D0
D1
D0
D1
D0
D1
D0
D1
D0
D1
SELECT
OUT
OUTP
OUTM

FIG. 2

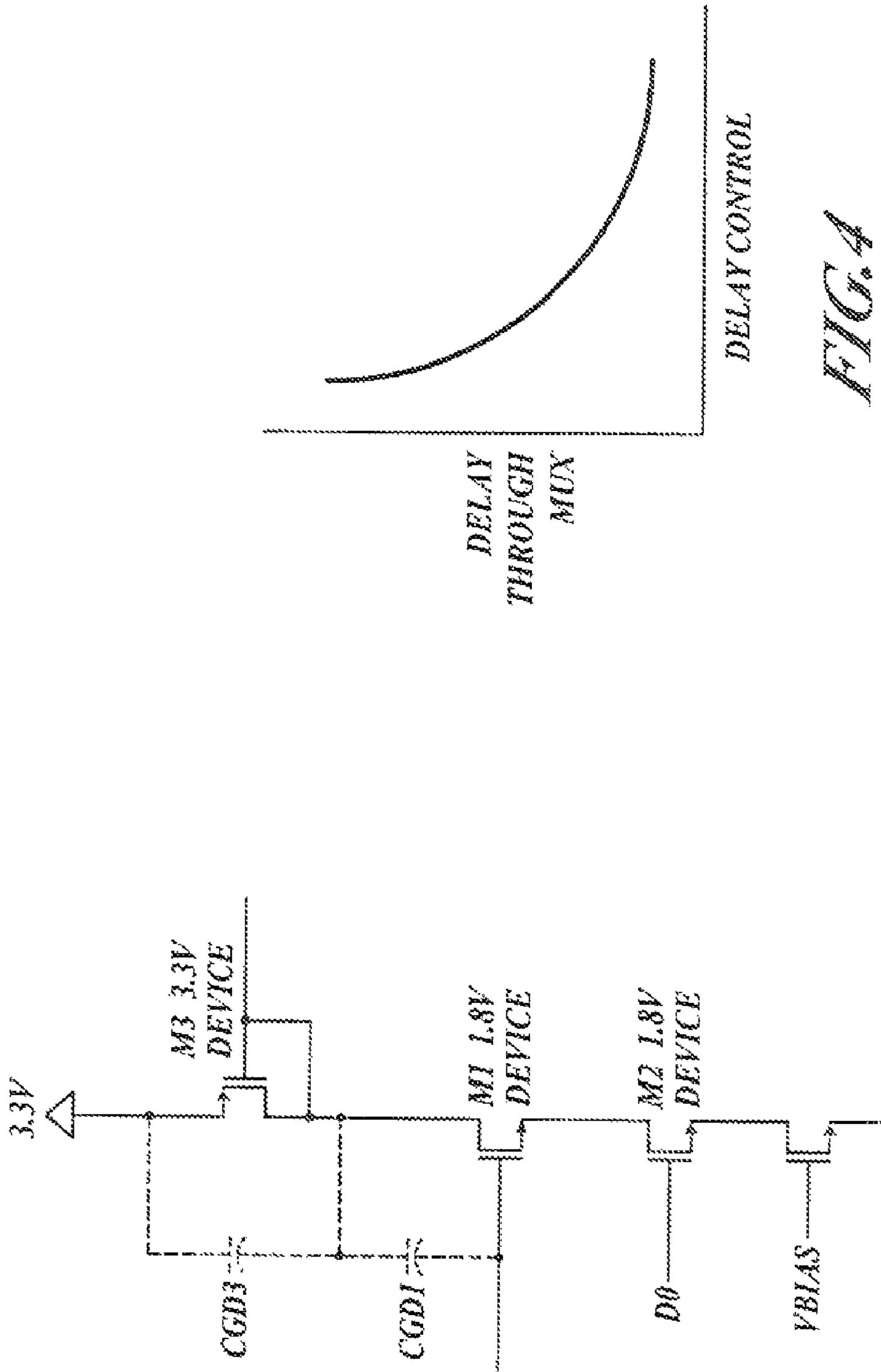

DELAY CONTROL
DELAY THROUGH MUX
M3 3.3V DEVICE
M1 1.8V DEVICE
M2 1.8V DEVICE
3.3V
CGD3
CGD1
SELECT
D0
VBIAS

FIG. 4

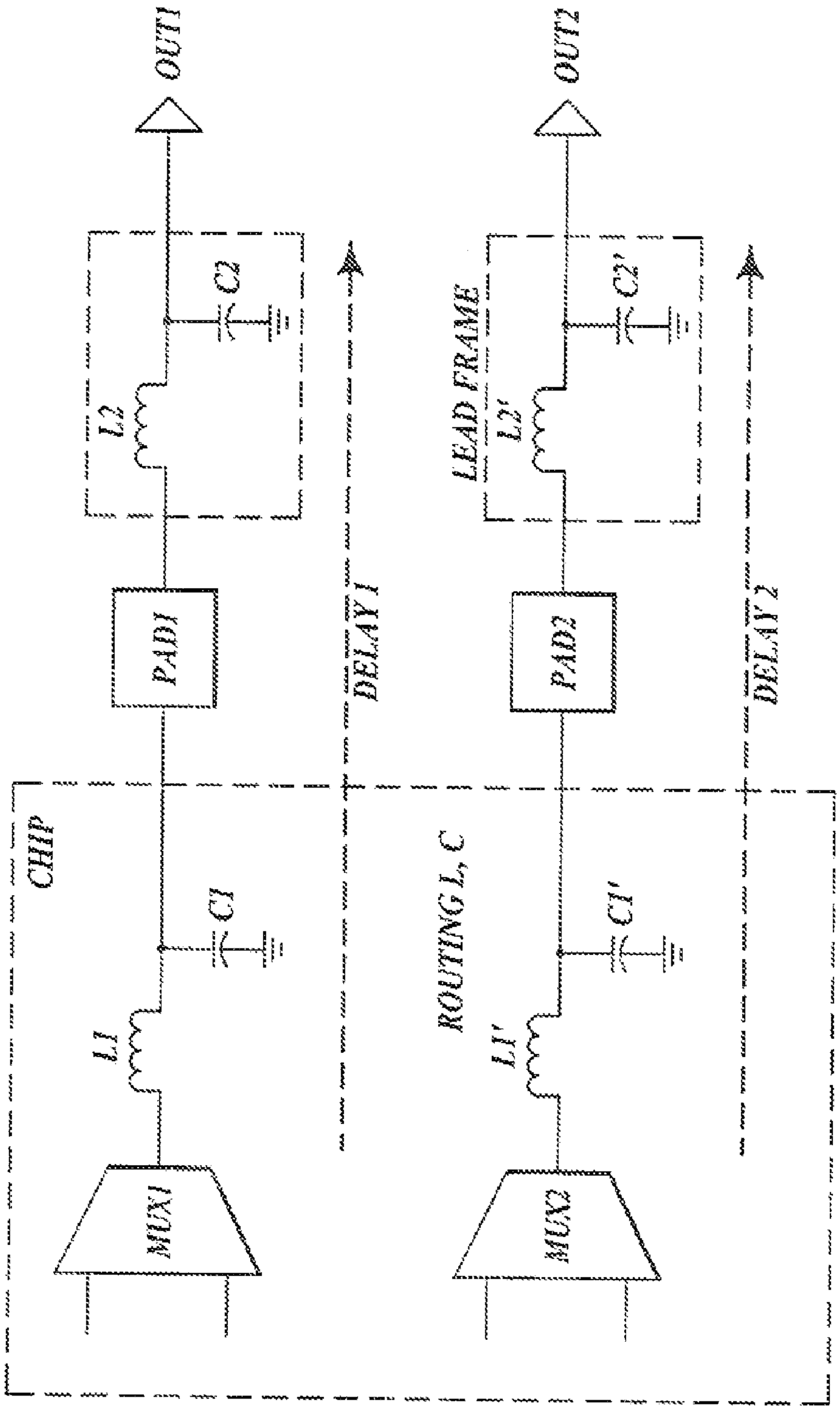

CHIP
OUT1
C2
L2
PAD1
C1
L1
MUX1
DELAY1
ROUTING L, C
OUT2
C2'
LEAD FRAME
L2'
PAD2
C1'
L1'
MUX2
DELAY 2

FIG. 5

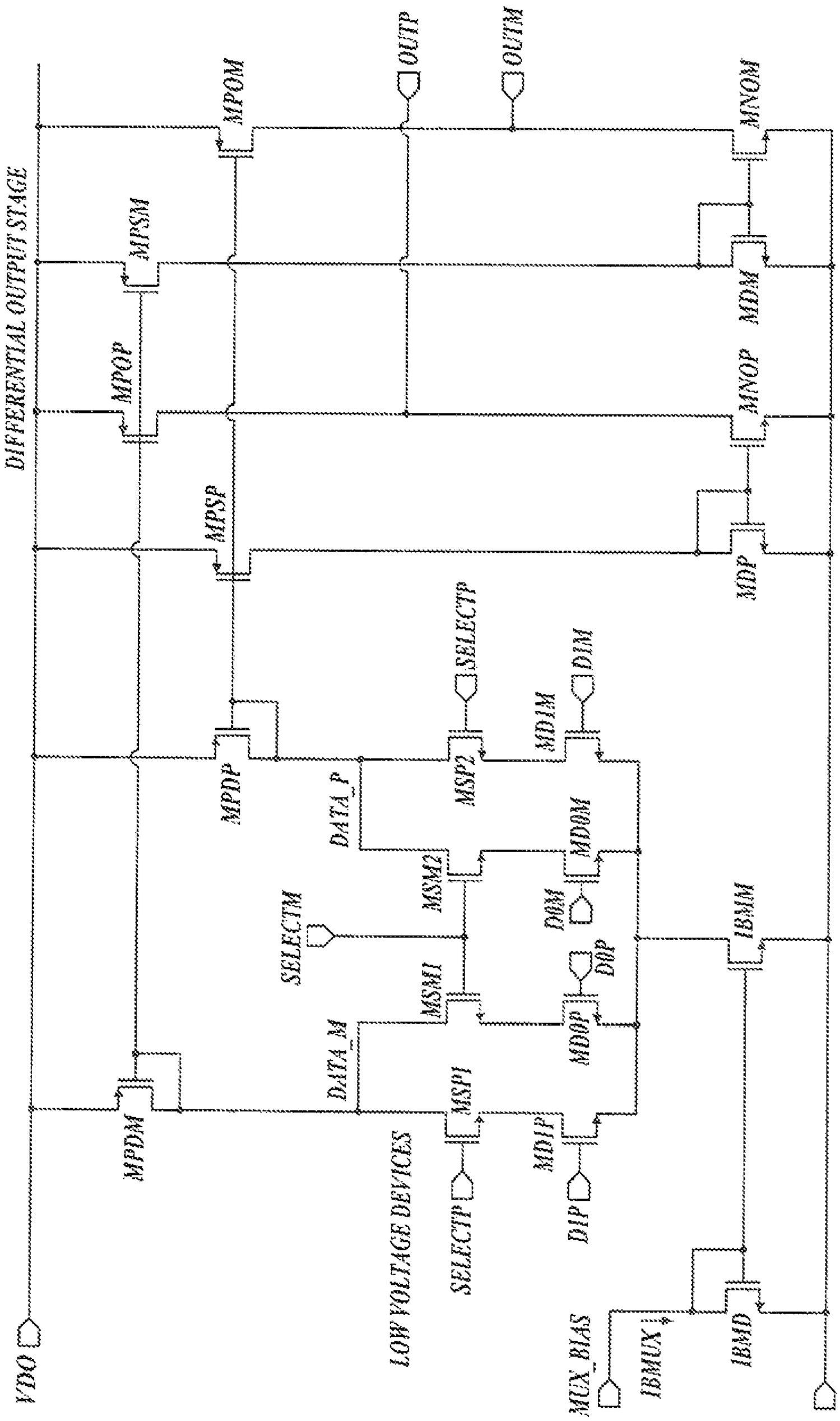

DIFFERENTIAL OUTPUT STAGE
MPOM
OUTP
OUTM
MNOM
MPSM
MDM
MPOP
MNOP
MPSP
MDP
MPDP
SELECTP
DATA_P
MSP2
MD1M
DIM
SELECTM
MSM2
MD0M
D0M
MSM1
D0P
MD0P
DATA_M
IBMM
MPDM
LOW VOLTAGE DEVICES
MSP1
SELECTP
MD1P
DIP
MUX_BIAS
IBMUX
IBMD
VDD
VDD

FIG. 6A

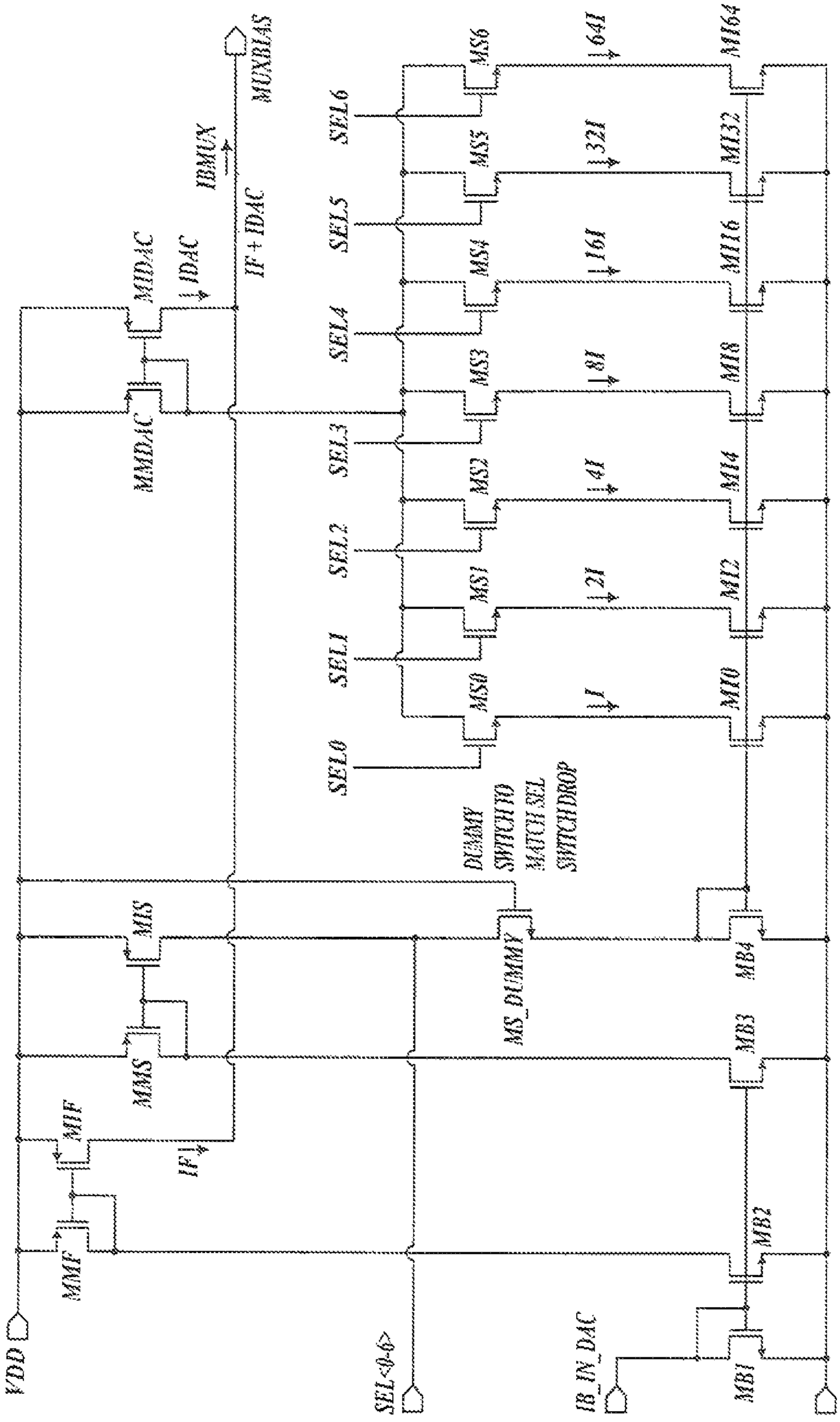

VDD
MMF
MIF
IF1
MMS
MS
MMDAC
MDAC
IDAC
IBMUX
IF+IDAC
MUXBIAS
SEL<0-6>
SEL0
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
DUMMY SWITCH TO MATCH SEL SWITCHDROP
MS0
MS1
MS2
MS3
MS4
MS5
MS6
MS_DUMMY
IB_IN_DAC
MB1
MB2
MB3
MB4
MI0
MI2
MI4
MI8
MI16
MI32
MI64
1I
2I
4I
8I
16I
32I
64I

FIG. 6B

MULTIPLEXER CIRCUIT WITH COMBINED LEVEL SHIFTING AND DELAY CONTROL FUNCTIONS

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of commonly-assigned U.S. patent application Ser. No. 11/303,785, filed Dec. 16, 2005, now U.S. Pat. No. 7,319,356, which is hereby incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

The present invention generally relates to circuits and systems that use multiplexer circuits such as data serializers. More particularly, the present invention is related to a circuit, system, and method for providing a multiplexer with combined level shifting and delay control functions for enhanced performance in applications such as high-speed data serializers.

BACKGROUND

Computer systems and many other electronics systems often store data in a parallel format. The stored data is communicated to other portions within the system with a parallel bus architecture, where each data bit is communicated over a separate communication bus wire. Modern electronics device interfaces have begun to adopt serial communication interfaces as a way of simplifying the interface. Example electronics interfaces that includes serial communication topologies include the Universal Serial Bus (USB) Interface, IEEE 1394 "Firewire" Interface, to name a few.

A data serializer is a device that receives parallel data and converts the parallel data into a serial data stream. Data serializers are useful in many devices such as interfacing a USB device to a computer system, where the computer system has a parallel data bus and the USB device communicates with serial data. A wide variety of applications exist for data serializers such as telecommunications, data communications, backplane/cable interconnect applications, and video interface applications, to name a few. Interface circuits are also becoming available for bi-directional communications that includes both serializing and de-serializing functions.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting and non-exhaustive embodiments are described with reference to the following drawings:

FIG. **1** is a schematic diagram of a level shifting multiplexer that is arranged in accordance with an embodiment of the present disclosure.

FIG. **2** is a timing diagram of waveforms for a level shifting multiplexer circuit that is arranged in accordance with the present disclosure.

FIG. **3** is a schematic diagram of a portion of a level shifting multiplexer circuit that is arranged in accordance with the present disclosure.

FIG. **4** is graph illustrating delay control operation in a level shifting multiplexer circuit that is arranged in accordance with the present disclosure

FIG. **5** is a diagram illustrating skewing effects on an example level shifting multiplexer circuit that is arranged in accordance with the present disclosure.

FIGS. **6**A and **6**B illustrate a detailed example of a level shifting multiplexer circuit that is arranged in accordance with the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, data, or other signal.

Briefly stated, a digitally controlled circuit is arranged to provide the combined functions of level shifting, multiplexing, and delay control functions. The circuit is compact, and uses lower power and lower overall noise susceptibility over other solutions. A programmable bias current is arranged to adjust the delay through the circuit. The bias current can be provided by a digitally controlled current source, a binary weighted current DAC, or other digitally controlled means. The multiplexing functions are provided by an input stage circuit that is current limited by the programmable bias current. An output stage is arranged to convert signals from the input stage to a desired voltage level.

FIG. **1** is a schematic diagram FIG. **1** is a schematic diagram of a multiplexer circuit that is arranged in accordance with an embodiment of the present disclosure. The multiplexer circuit includes a level shifting multiplexer (LEVEL SHIFT MUX) and a delay bias circuit (DLY_BIAS).

The level shifting multiplexer circuit includes a first data input terminal, a second data input terminal, a bias control input terminal, a selection control input terminal, a bias control terminal, and an output terminal. The first data input terminal is arranged to receive a first data input signal (D**0**P, D**0**M). The second data input terminal is arranged to receive a second data input signal (D**1**P, D**1**M). The selection control input terminal is arranged to receive a selection control signal (SELECTP, SELECTM). The bias control terminal is arranged to receive a bias control signal (BIAS), which is provided from an output of the delay bias circuit (DLY_BIAS). The delay bias circuit includes a delay adjustment control terminal that is arranged to receive a delay adjustment control signal (DELAY CONTROL). The D**0**P and D**0**M signals form a complementary input signal (e.g., inverse logic related). Similarly, additional signal pairs are also complementary such as: D**1**P, D**1**M and SELECTP, SELECTM.

The level shifting multiplexer circuit is arranged to provide an output signal (OUTP, OUTM) in response to a selected one of the data input signals (D0P, D0M; D1P, D1M) as determined by the selection control signal (SELECTP, SELECTM). The output signal (OUTP, OUTM) is related to the selected data input signal, but is level shifted from the data input power supply levels and the desired output supply levels. The edge rate for transitions between the logic high and logic low levels in the output signal (OUTP, OUTM) can be adjusted by the bias control signal (BIAS) such the effects of signal delays through each signal path can be equalized for a desired performance.

The input data is illustrated as a pair of signals such as from differential signals (e.g., USB, LVDS, etc). The selection control signal is illustrated as a selection signal (SELECTP) and the complement of the selection signal (SELECTM). The same circuit topology will also work for single-ended signals (control signals and/or data signals) that are referenced to a signal ground. The input signals are illustrated as in a 1.8V power-supply domain, while the output signals are illustrated as in the 3.3V power-supply domain. The delay control signal illustrated as a 7 bit control signal, but any appropriate control mechanism may be used such as a multi-bit digital control signal, and an analog control signal. The output of the circuit provides true and complement form of the multiplexed data.

A truth table for the described multiplexer operation is illustrated below.

SELECT	D1	D0	OUTP	OUTM
L	X	L	L	H
L	X	H	H	L
H	L	X	L	H
H	H	X	H	L

FIG. **2** is a timing diagram of waveforms for a level shifting multiplexer circuit that is arranged in accordance with the present disclosure. As illustrated, the input data signals (D**0**, D**1**) and the section control signal (SELECT) are operated on first power-supply levels (e.g., 1.8V), while the output signal (OUT) is operated at second power supply levels (e.g., 3.3V). The illustrated multiplexing operation includes differential input signals and differential output signals to prevent noise and other problems that may occur. However, in some embodiments single ended signals may be used.

FIG. **3** is a schematic diagram of a portion of a level shifting multiplexer circuit that is arranged in accordance with the present disclosure. The circuit includes a four transistor devices. The first transistor device (M**1**) is responsive to a selection control signal (SELECT). The second transistor device (M**2**) is coupled between the first transistor device (M**1**) and a current source transistor. Transistor M**2** is responsive to changes in the data signal (D**0**). The current source transistor is biased as a current source with a control voltage (VBIAS). An output is from the gate/drain connection of transistor M**3**, which is coupled to a drain of transistor M**1**.

The input data and the select signals are in low voltage domain where as the outputs are in high voltage domain. The low voltage domain has reduced power consumption, such that it is appropriate for signal processing functions. The multiplexer circuit uses both low voltage device (e.g., M**1**, M**2**) and high voltage devices (e.g. M**3**) but due to charge sharing between the cascaded devices, the low voltage devices are safe from potential junction breakdown. For a selection control input (SELECT) corresponding to 0 V, with 3.3 V supply, the voltage at the gate of transistor M**1** is substantially lower due to the voltage division by the parasitic capacitance (Cgd**1** and Cgd**3**) between the gate and drain of transistors M**1** an M**3**, respectively.

The switching between the two multiplexed input signals can be done by cascaded differential pair structures such that equal rise and fall times are ensured. If the Select inputs are 50% duty cycle, the output duty cycle also remains 50%.

The biasing voltage that is applied to the gate of the current source transistor can be increased for faster edge transitions, or decreased to slow down edge transitions as may be desired to conserve power and achieve a desired operating speed. Constant current operation can be applied to the current source operation such that the total current remains relatively constant and no switching noise is injected in the power supply.

The delay through the multiplexer is controlled by a biasing signal that is adjusted in response to at least one of: a resistor, a current source, a programmable current course, a biased transistor, a diode coupled transistor, and an N-bit binary weighted current DAC, or any other reasonable adjustment mechanism. In one example that is illustrated in FIG. **6**B, a 7-bit binary weighted Current DAC can be used to adjust the biasing.

Faster edge transitions can be achieved in the multiplexer circuit by increasing the bias current such that the overall propagation delay through the multiplexer can be controlled. FIG. **4** is graph illustrating delay control operation in a level shifting multiplexer circuit that is arranged in accordance with the present disclosure. As illustrated in FIG. **4**, the delay through the multiplexer circuit is non-linear in nature such that increasing the bias control value (DELAY CONTROL) decreases the delay through the circuit.

FIG. **5** is a diagram illustrating skewing effects on an example level shifting multiplexer circuit that is arranged in accordance with the present disclosure. A chip with more than one multiplexed output may have different delay times between the multiplexer output and any receiving circuit for the output. The skewing that may occur between the various multiplexers can be worse depending on parasitic effects such as parasitic capacitance, inductance and/or resistance from any of the: wires, metallization in an integrated circuit, bonding pads, lead frames, bonding wires, and circuit boards to name a few.

As illustrated in FIG. **5**, a first signal path may have a first delay characteristic (delay **1**) that is the result of various on-chip parasitic inductance (L**1**) and capacitance (C**1**), as well as any bonding pad (PAD**1**) effects, and off-chip parasitic inductance (L**2**) and capacitance (C**2**). A second signal path may have a different delay characteristic (delay **2**) that is the result of different on-chip parasitic inductance (L**1**') and capacitance (C**1**), different bonding pad (PAD**2**) effects, and/or different off-chip parasitic inductance (L**2**) and capacitance (C**2**). The different parasitic effects result in a difference in the delay times that is observed as a skewing between the output signals even when care is taken to make the paths identical. At high frequency operation, the skew control becomes an important factor and the delay control in the presently described multiplexer circuit provides an adjustment mechanism to exactly match the output timings.

FIGS. **6**A and **6**B illustrate a detailed example of a level shifting multiplexer circuit that is arranged in accordance with the present disclosure. FIG. **6**A illustrates a level shifting multiplexer while FIG. **6**B illustrates a delay control circuit for the level shifting multiplexer circuit of FIG. **6**A. The example level shifting multiplexer circuit is a differential circuit that includes a differential input stage and a differential output stage.

The differential input stage includes: four select transistors (MSO**1**, MSM**1**, MSM**2**, and MSP**2**), four switching transistors (MD**0**P, MD**0**M, MD**1**P, and MD**1**M), a current source transistor (IBMM), and a biasing transistor (IBMD). The current source transistor is biased to provide a current to the differential input stage that depends on the current reference IBMUX flowing through the biasing transistor (IBMD). The SELECTP signal is arranged to activate transistors MSP**1** and MPS**2** when asserted, while the SELECTM signal is arranged to activate transistors MSM**1** and MSM**2** when asserted. SELECTP and SELECTM are complementary signals. A differential pair circuit is formed with transistors MD**1**P and MD**1**M when SELECTP is asserted, where the differential pair is responsive to signals D**1**P and D**1**M. Another differential pair circuit is formed with transistors MD**0**P and MD**0**M when SELECTM is asserted, where the differential pair is responsive to signals D**0**P and D**0**M. Each differential pair is arranged to selectively steer current from transistor IBMM between the diode coupled transistors MPDM and MPDP. The diode coupled transistors operate as the output nodes of the differential input stage.

The differential output stage includes at least transistors MPSP, MPOP, MPSM, MPOM, MDP, MNOP, MDM, and MNOM. Transistor MDP will activate transistor MNOP when transistor MPSP is activated in response to a first output of the differential input stage (DATA_P). Transistor MDM will activate transistor MNOM when transistor MPSM is activated in response to a second output of the differential input stage (DATA_M). The activation of transistor MNOP will decrease signal amplitude OUTP, while activation of transistor MPOP will increase the signal amplitude of OUTP. Similarly, the activation of transistor MNOM will decrease signal amplitude OUTM, while activation of transistor MPOM will increase the signal amplitude of OUTM. The rate of the transition between one output polarity and another is dependent on the conduction current in the differential pair.

The delay control circuit from FIG. **6**B is arranged to provide a multiplexer biasing signal (MUX BIAS) that includes a fixed biasing portion (IF) and a variable biasing portion (IDAC).

The fixed biasing portion (IF) is provided by transistors MB**1**, MB**2**, MMF and MIF. Transistor MB**1** can be biased by an externally provided component such as a resistor, a current source, etc. Transistors MB**2** and MB**3** are biased in common with transistor MB**1**. Transistor MMF is configured as a current mirror with transistor MIF, and also biased by transistor MB**2**.

The variable biasing portion (IDAC) is provided by a current DAC, which is illustrated as a 7-bit current DAC. Transistors MB**3**, MMS, MIS, MS_DUMMY, and MB**4** are arranged to provide a biasing signal to transistors MI**0**, MI**2**, MI**4**, MI**8**, MI**16**, MI**32** and MI**64** which are each arranged to operate as a binary power of a unit current source. Transistors MS**0**-MS**6** are switching transistors that are necessary to select each current source in the current DAC. Current from the selected switching transistors are combined by transistor MMDAC, which is arranged in a current mirror configuration with transistor MIDAC. Transistor MIDAC is arranged to provide the variable portion of the multiplexer biasing signal.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.

What is claimed is:

1. A multiplexer comprising:

a multiplexer circuit comprising:

a differential input stage that receives at least two input data signals;

a differential output stage that provides an output data signal and a compliment of the output data signal, the differential output stage comprising:

a first transistor that receives an internal data signal from the differential input stage;

a first current mirror coupled to the first transistor, wherein the first transistor controls the first current mirror in response to the internal data signal;

a second transistor coupled to the first current mirror that receives a compliment of the internal data signal from the differential input stage;

a first output node coupled to the first current mirror and the second transistor that provides the output data signal;

a third transistor that receives the compliment of the internal data signal from the differential input stage;

a second current mirror coupled to the third transistor, wherein the third transistor controls the second current mirror in response to the compliment of the internal data signal;

a fourth transistor coupled to the second current mirror that receives the internal data signal from the differential input stage; and

a second output node coupled to the second current mirror and the fourth transistor that provides the compliment of the output data signal;

wherein the differential output stage maintains a rise time of the output data signal substantially the same as a fall time of the output data signal; and

an adjustable biasing current that controls the rise and fall times of the output data signal; and

a delay bias circuit that analyzes the rise time or the fall time of the output data signal and generates a bias control signal that is varied in response to the analysis;

wherein the bias control signal is provided to the multiplexer circuit to adjust the biasing current.

2. The multiplexer of claim **1**, wherein the multiplexer circuit level shifts a selected input data signal from a first power supply level to a second power supply level.

3. The multiplexer of claim **2**, wherein the first power supply level is approximately 1.8 volts and the second power supply level is approximately 3.3 volts.

4. The multiplexer of claim **1**, wherein the bias control signal comprises a fixed biasing portion and a variable biasing portion.

5. A method of adjusting delay times in a multiplexer circuit, comprising:

receiving a first data input and a second data input;

providing an internal data signal and a compliment of the internal data signal based on a data selection signal and one of the first data input and the second data input;

receiving the internal data signal with a first transistor;

controlling a first current mirror with the first transistor in response to the internal data signal;

receiving the compliment of the internal data signal with a second transistor coupled to the first current mirror;

providing an output data signal with a first output node coupled to the first current mirror and the second transistor;

receiving the compliment of the internal data signal with a third transistor;

controlling a second current mirror with the third transistor in response to the compliment of the internal data signal;

receiving the internal data signal with a fourth transistor coupled to the second current mirror;

providing a compliment of the output data signal with a second output node coupled to the second current mirror and the fourth transistor;

maintaining a rise time of the output data signal substantially the same as a fall time of the output data signal;

analyzing the rise time or the fall time of the output data signal; and

varying a bias control signal to adjust the rise and fall times of the output data signal based on the analysis.

6. The method of claim **5**, wherein the multiplexer circuit level shifts a selected data input from a first power supply level to a second power supply level.

7. The method of claim **6**, wherein the first power supply level is approximately 1.8 volts and the second power supply level is approximately 3.3 volts.

8. The method of claim **5**, wherein the bias control signal comprises a fixed biasing portion and a variable biasing portion.

9. A multiplexer apparatus, comprising:

means for receiving a first data input and a second data input;

means for providing an internal data signal and a compliment of the internal data signal based on a data selection signal and one of the first data input and the second data input;

means for receiving the internal data signal with a first transistor;

means for controlling a first current mirror with the first transistor in response to the internal data signal;

means for receiving the compliment of the internal data signal with a second transistor coupled to the first current mirror;

means for providing an output data signal with a first output node coupled to the first current mirror and the second transistor;

means for receiving the compliment of the internal data signal with a third transistor;

means for controlling a second current mirror with the third transistor in response to the compliment of the internal data signal;

means for receiving the internal data signal with a fourth transistor coupled to the second current mirror;

means for providing a compliment of the output data signal with a second output node coupled to the second current mirror and the fourth transistor;

means for maintaining a rise time of the output data signal substantially the same as a fall time of the output data signal;

means for analyzing the rise time or the fall time of the output data signal; and

means for varying a bias control signal to adjust the rise and fall times of the output data signal based on the analysis.

10. The multiplexer apparatus of claim **9** further comprising level shifting means that level shifts a selected data input from a first power supply level to a second power supply level.

11. The multiplexer apparatus of claim **10**, wherein the first power supply level is approximately 1.8 volts and the second power supply level is approximately 3.3 volts.

12. The multiplexer apparatus of claim **9**, wherein the bias control signal comprises a fixed biasing portion and a variable biasing portion.

13. An multiplexer comprising:

a first multiplexing apparatus that has a first data output, wherein there is a first rise time and a first fall time associated with a logic level transition in the first data output, and wherein the first multiplexing apparatus maintains the first rise time substantially the same as the first fall time;

a second multiplexing apparatus that has a second data output, wherein there is a second rise time and a second fall time associated with a logic level transition in the second data output, and wherein the second multiplexing apparatus maintains the second rise time substantially the same as the second fall time;

wherein each of the first and second multiplexing apparatuses further comprises:

a first transistor that receives an internal data signal from a differential input stage;

a first current mirror coupled to the first transistor, wherein the first transistor controls the first current mirror in response to the internal data signal;

a second transistor coupled to the first current mirror that receives a compliment of the internal data signal from the differential input stage;

a first output node coupled to the first current mirror and the second transistor that provides an output data signal;

a third transistor that receives the compliment of the internal data signal from the differential input stage;

a second current mirror coupled to the third transistor, wherein the third transistor controls the second current mirror in response to the compliment of the internal data signal;

a fourth transistor coupled to the second current mirror that receives the internal data signal from the differential input stage; and

a second output node coupled to the second current mirror and the fourth transistor that provides a compliment of the output data signal; and

a delay bias circuit that analyzes the first and second rise or fall times and that generates a first bias control signal that adjusts the first rise and fall times such that the adjusted first rise and fall times are substantially matched to the second rise and fall times.

14. The multiplexer of claim **13**, wherein the first and second multiplexing apparatus level shift selected input data signals from a first power supply level to a second power supply level.

15. A method of adjusting delay times in a multiplexer circuit comprising:

selecting one of a first data input and a second data input to provide a first data output in a first multiplexer circuit, wherein there is a first rise time and a first fall time associated with a logic level transition in the first data output in response to a corresponding logic level transition in the selected one of the first data input and the second data input;

maintaining the first rise time substantially the same as the first fall time;

selecting one of a third data input and a fourth data input to provide a second data output in a second multiplexer circuit, wherein there is a second rise time and a second fall time associated with a logic level transition in the second data output in response to a corresponding logic level transition in the selected one of the third data input and the fourth data input;

maintaining the second rise time substantially the same as the second fall time; and

adjusting the first rise and fall times such that the adjusted first rise and fall times are substantially matched to the second rise and fall times;

wherein each of the first and second multiplexer circuits comprises:

a first transistor that receives an internal data signal from a differential input stage;

a first current mirror coupled to the first transistor, wherein the first transistor controls the first current mirror in response to the internal data signal;

a second transistor coupled to the first current mirror that receives a compliment of the internal data signal from the differential input stage;

a first output node coupled to the first current mirror and the second transistor that provides an output data signal;

a third transistor that receives the compliment of the internal data signal from the differential input stage;

a second current mirror coupled to the third transistor, wherein the third transistor controls the second current mirror in response to the compliment of the internal data signal;

a fourth transistor coupled to the second current mirror that receives the internal data signal from the differential input stage; and

a second output node coupled to the second current mirror and the fourth transistor that provides a compliment of the output data signal.

16. The method of claim **15**, wherein the first and second multiplexer circuits level shift the selected data inputs from a first power supply level to a second power supply level.

17. A multiplexer apparatus comprising:

means for selecting one of a first data input and a second data input to provide a first data output in a first multiplexing means, wherein there is a first rise time and a first fall time associated with a logic level transition in the first data output in response to a corresponding logic level transition in the selected one of the first data input and the second data input;

means for maintaining the first rise time substantially the same as the first fall time;

means for selecting one of a third data input and a fourth data input to provide a second data output in a second multiplexing means, wherein there is a second rise time and a second fall time associated with a logic level transition in the second data output in response to a corresponding logic level transition in the selected one of the third data input and the fourth data input;

means for maintaining the second rise time substantially the same as the second fall time; and

means for adjusting the first rise and fall times such that the adjusted first rise and fall times are substantially matched to the second rise and fall times;

wherein each of the first and second multiplexing means further comprises:

a first transistor that receives an internal data signal from a differential input stage;

a first current mirror coupled to the first transistor, wherein the first transistor controls the first current mirror in response to the internal data signal;

a second transistor coupled to the first current mirror that receives a compliment of the internal data signal from the differential input stage;

a first output node coupled to the first current mirror and the second transistor that provides an output data signal;

a third transistor that receives the compliment of the internal data signal from the differential input stage;

a second current mirror coupled to the third transistor, wherein the third transistor controls the second current mirror in response to the compliment of the internal data signal;

a fourth transistor coupled to the second current mirror that receives the internal data signal from the differential input stage; and

a second output node coupled to the second current mirror and the fourth transistor that provides a compliment of the output data signal.

18. The multiplexer apparatus of claim **17**, wherein the first and second multiplexing means level shift the selected data inputs from a first power supply level to a second power supply level.

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