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(54) **CAPACITIVE FINGERPRINT SENSOR AND THE PANEL THEREOF**

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G01R 27/28 (2006.01)
G06F 3/041 (2006.01)

(52) **U.S. Cl.** **324/686**; 324/649; 345/173

(58) **Field of Classification Search** 324/662, 324/686; 345/173, 174
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,049,620	A *	4/2000	Dickinson et al.	382/124
6,906,529	B2 *	6/2005	Blanchard	324/662
7,075,316	B2 *	7/2006	Umeda et al.	324/658
7,099,497	B2 *	8/2006	Chou et al.	382/124

OTHER PUBLICATIONS

Hiroyuki Hara, Mikio Sakurai, Mitsutoshi Miyasaka, Simon W.B. Tam, Satoshi Inoue and Tatsuya Shimoda, Low Temperature Polycrystalline Silicone TFT Fingerprint Sensor with Integrated Comparator Circuit, Journal 2004, pp. 403-406, IEEE.*

Hiroyuki Hara, Mikio Sakurai, Mitsutoshi Miyasaka, Simon W.B. Tam, Satoshi Inoue, and Tatsuya Shimoda; Low Temparature Polycrystalline Silicon TFT Fingerprint Sensor with Integrated Comparator Circuit; Journal; 2004; pp. 403-406; IEEE.

H.Hara, M.Miyasaka, C.Iriguchi, S.W.B.Tam, S.Inoue and T. Shimoda; A Capacitive Fingerprint Sensor with Integrated Comparator Based on LTPS TFTs; Journal; 2006; pp. 257-260; IDW.

* cited by examiner

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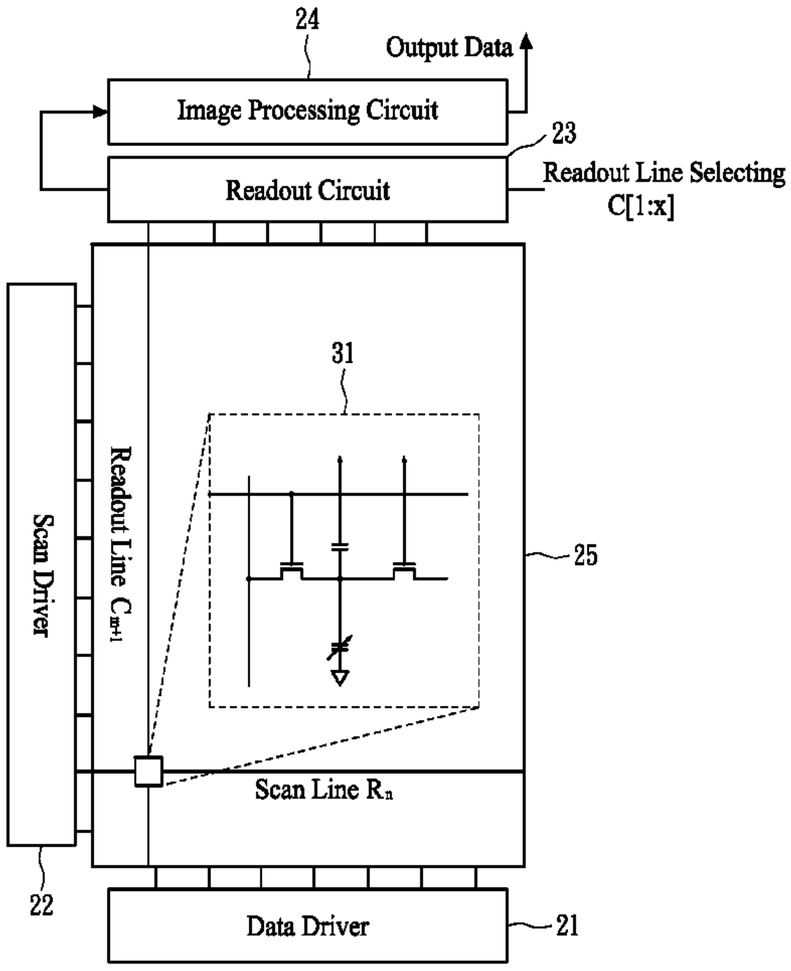
(57) **ABSTRACT**

A capacitive fingerprint sensor comprises a fingerprint capacitor, a reference capacitor, a first transistor and a second transistor. The fingerprint capacitor C_F has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR}. The reference capacitor C_S has a capacitance C_S, and $C_{FV}<C_S<C_{FR}$. The first transistor is configured to precharge the reference capacitor and the fingerprint capacitor during a precharge phase. The second transistor is configured to output the voltage of the reference capacitor during an evaluation phase. The precharge phase is controlled by a first readout select line, the evaluation phase is controlled by a second readout select line, the second readout select line is immediately next to the first readout select line, and the valid time to access the readout line is within an enabling period of the second readout select line.

18 Claims, 6 Drawing Sheets



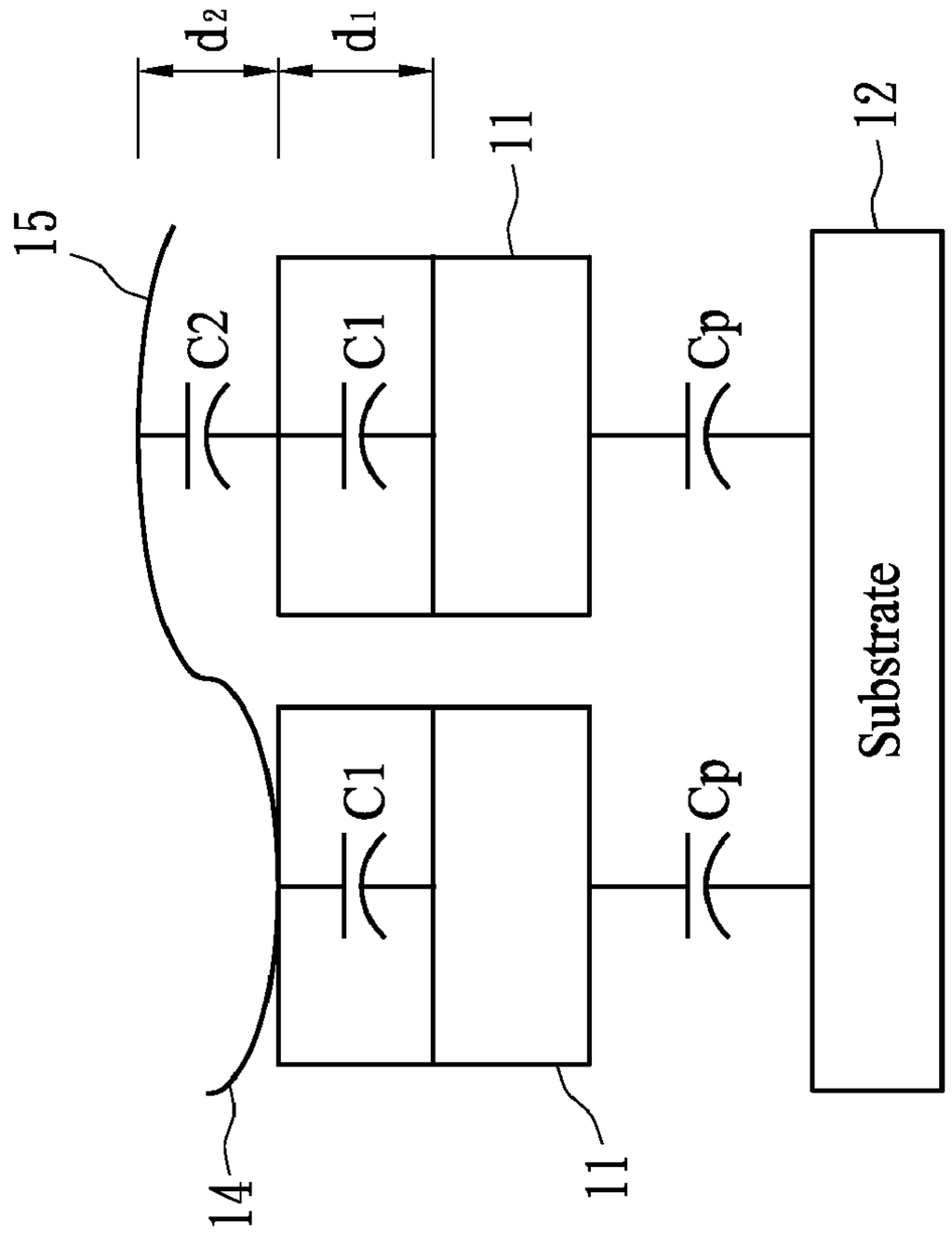


FIG. 1B (PRIOR ART)

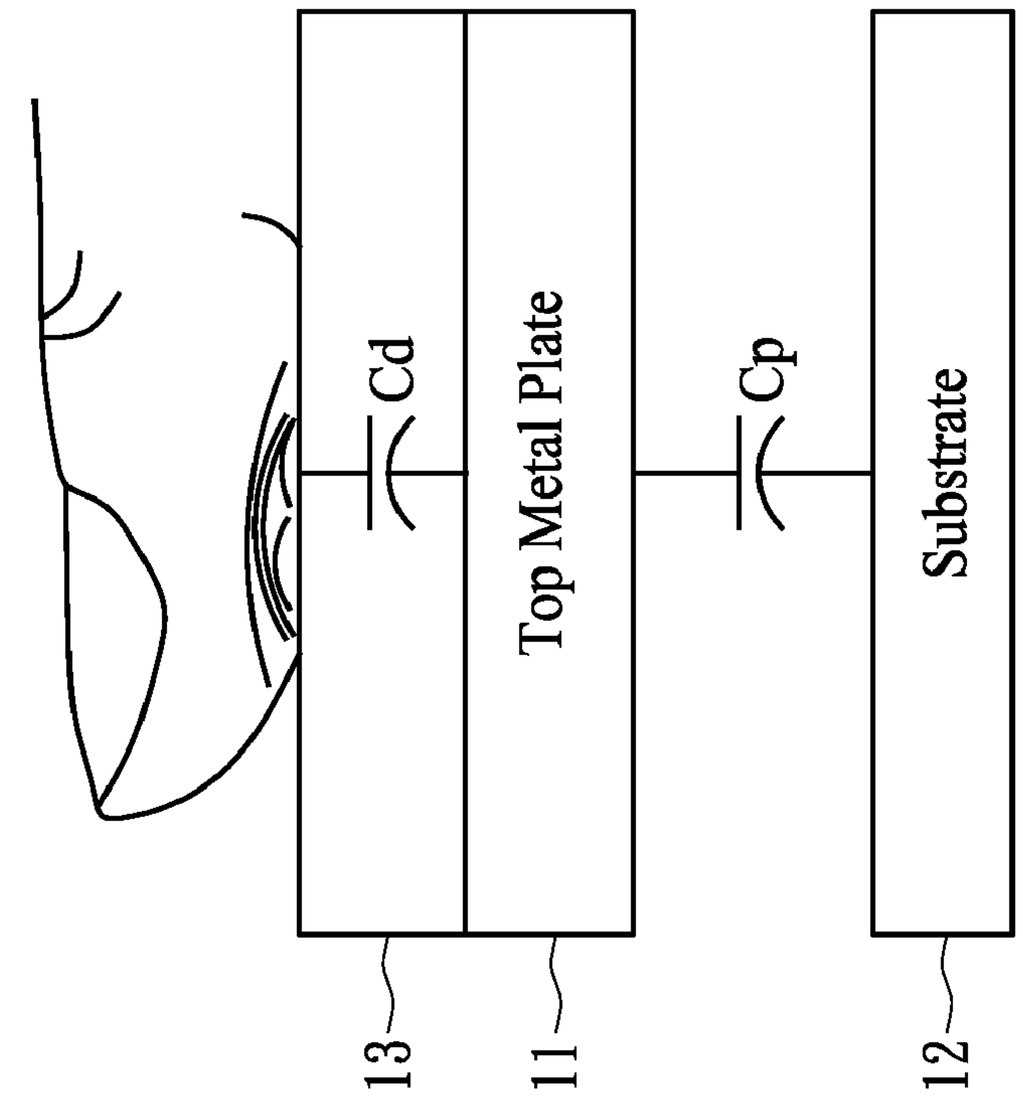


FIG. 1A (PRIOR ART)

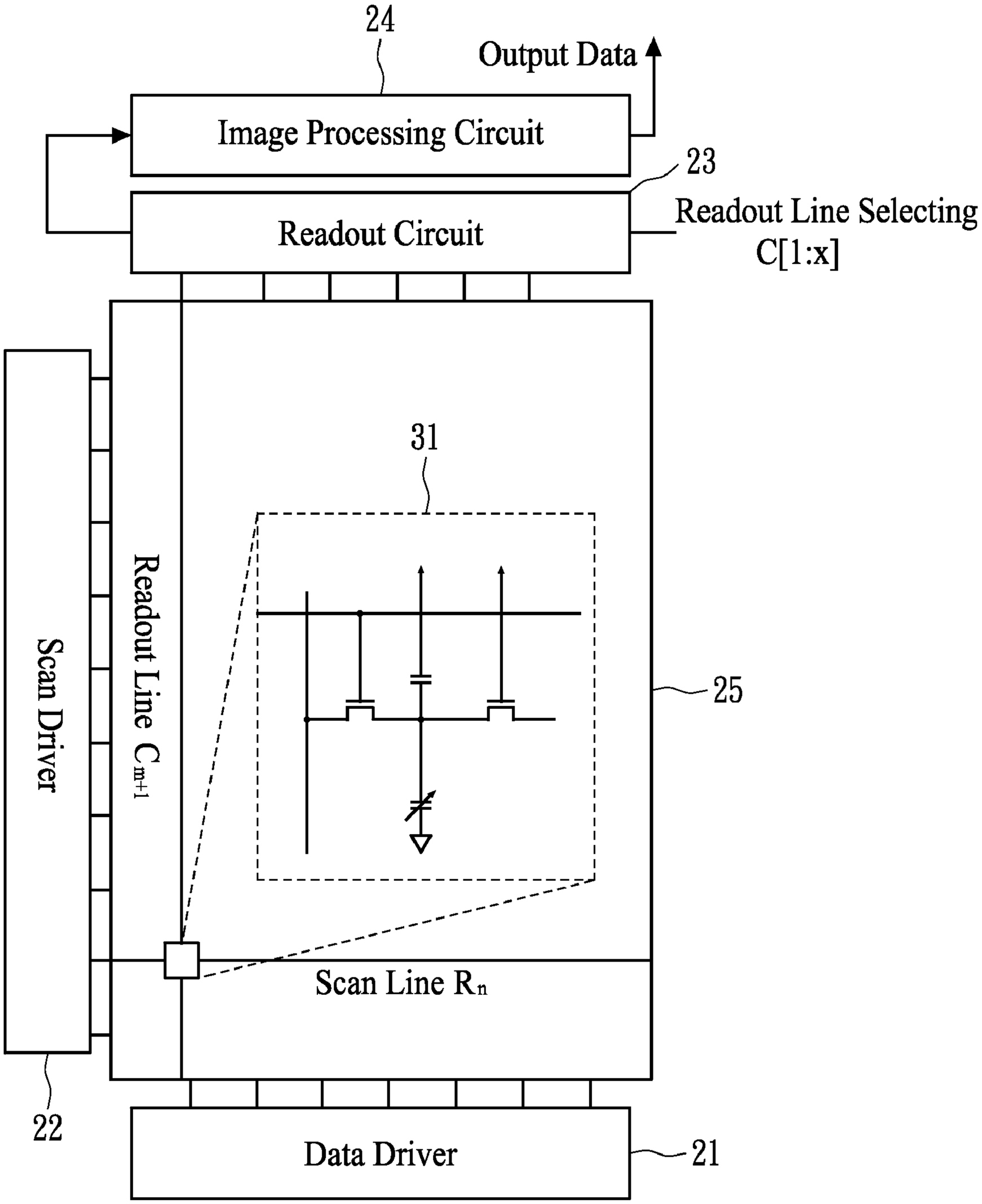

24
Output Data
Image Processing Circuit
23
Readout Line Selecting
C[1:x]
Readout Circuit
31
Scan Driver
Readout Line C_{m+1}
25
Scan Line R_n
22
Data Driver
21

FIG. 2

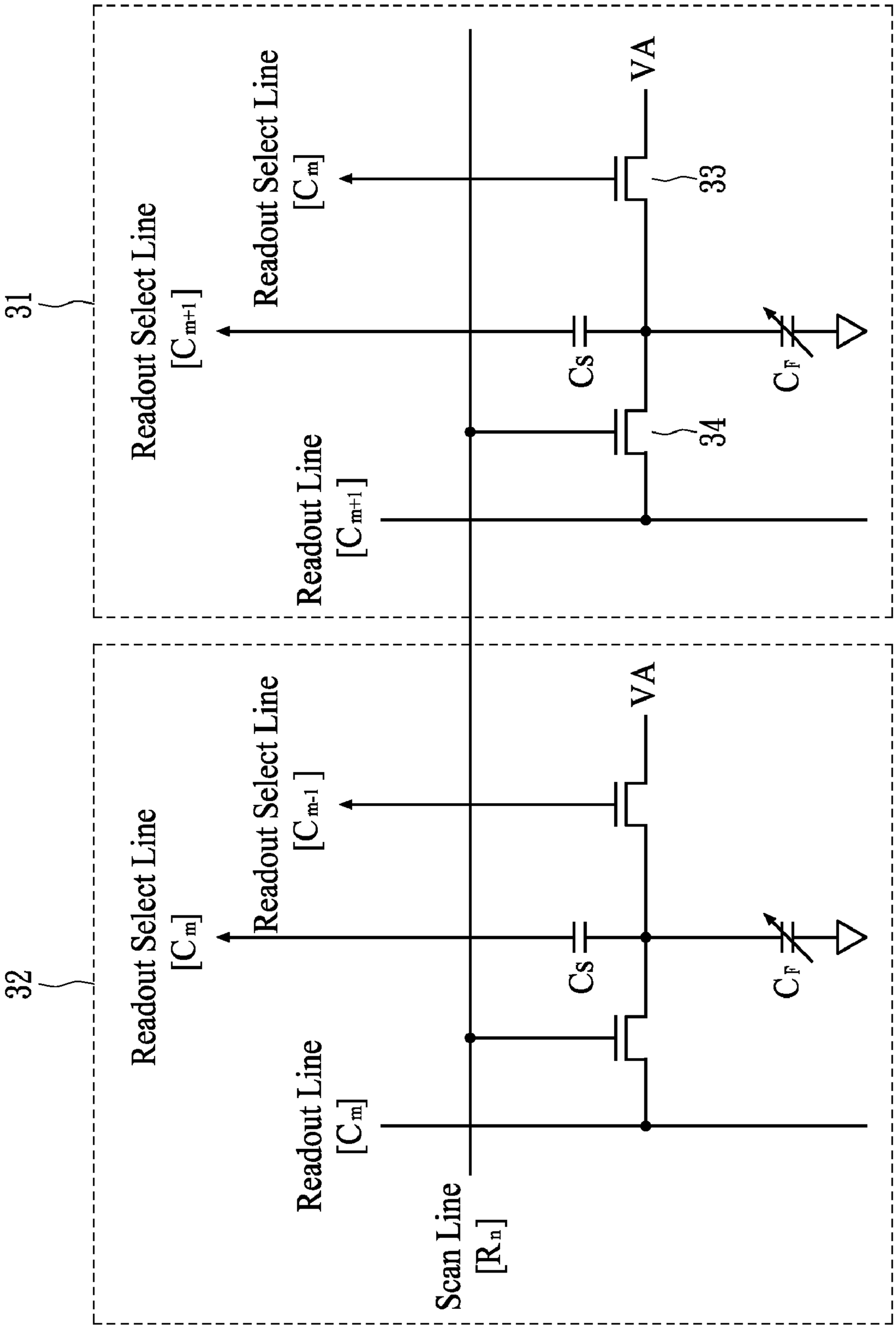

31
Readout Select Line
[Cm+1]
Readout Select Line
[Cm]
VA
33
Cs
CF
34
Readout Line
[Cm+1]
32
Readout Select Line
[Cm-1]
Readout Select Line
[Cm]
VA
Cs
CF
Readout Line
[Cm]
Scan Line
[Rn]

FIG. 3

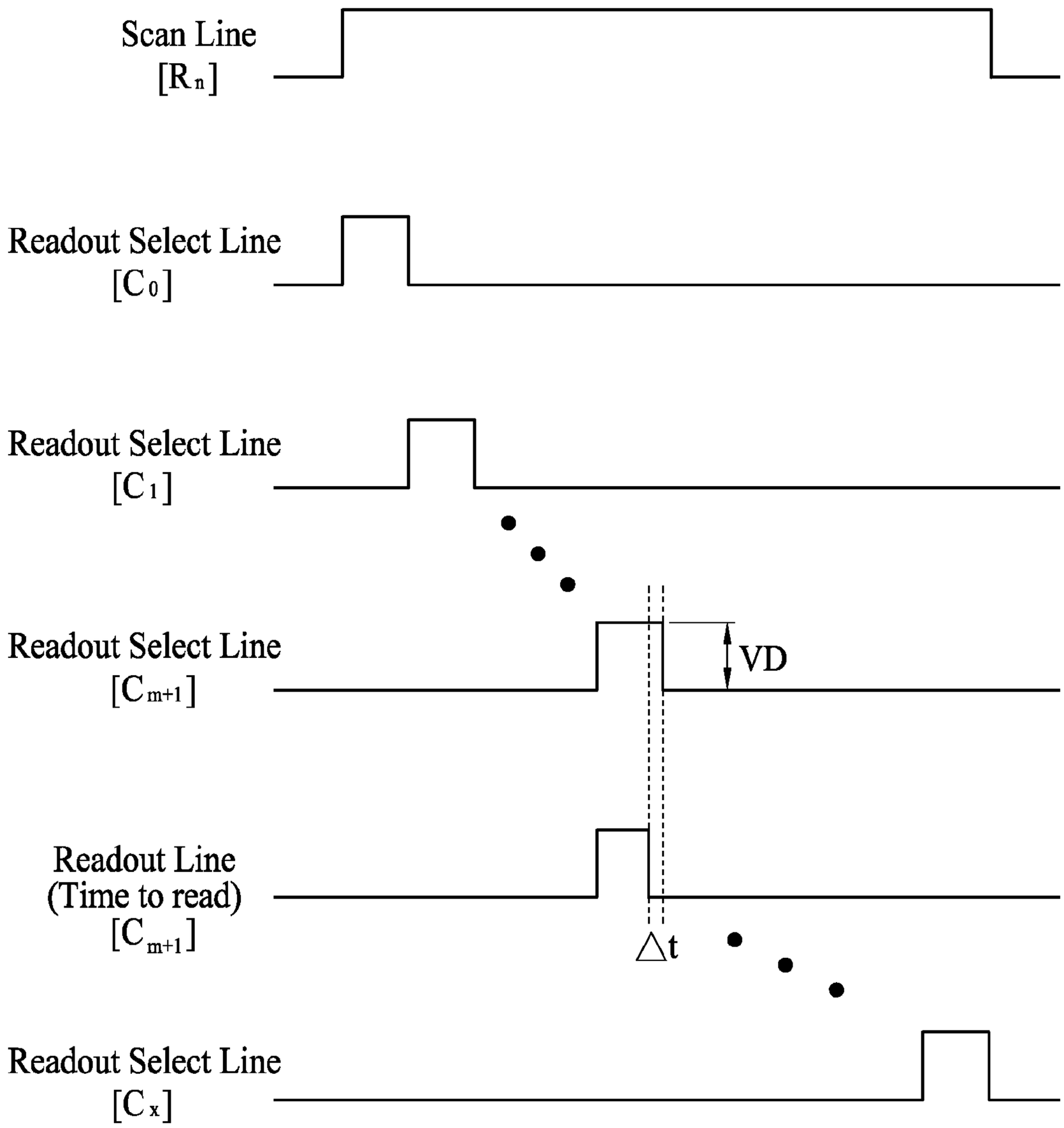

Scan Line
[Rn]
Readout Select Line
[C0]
Readout Select Line
[C1]
Readout Select Line
[Cm+1]
VD
Readout Line
(Time to read)
[Cm+1]
△t
Readout Select Line
[Cx]

FIG. 4

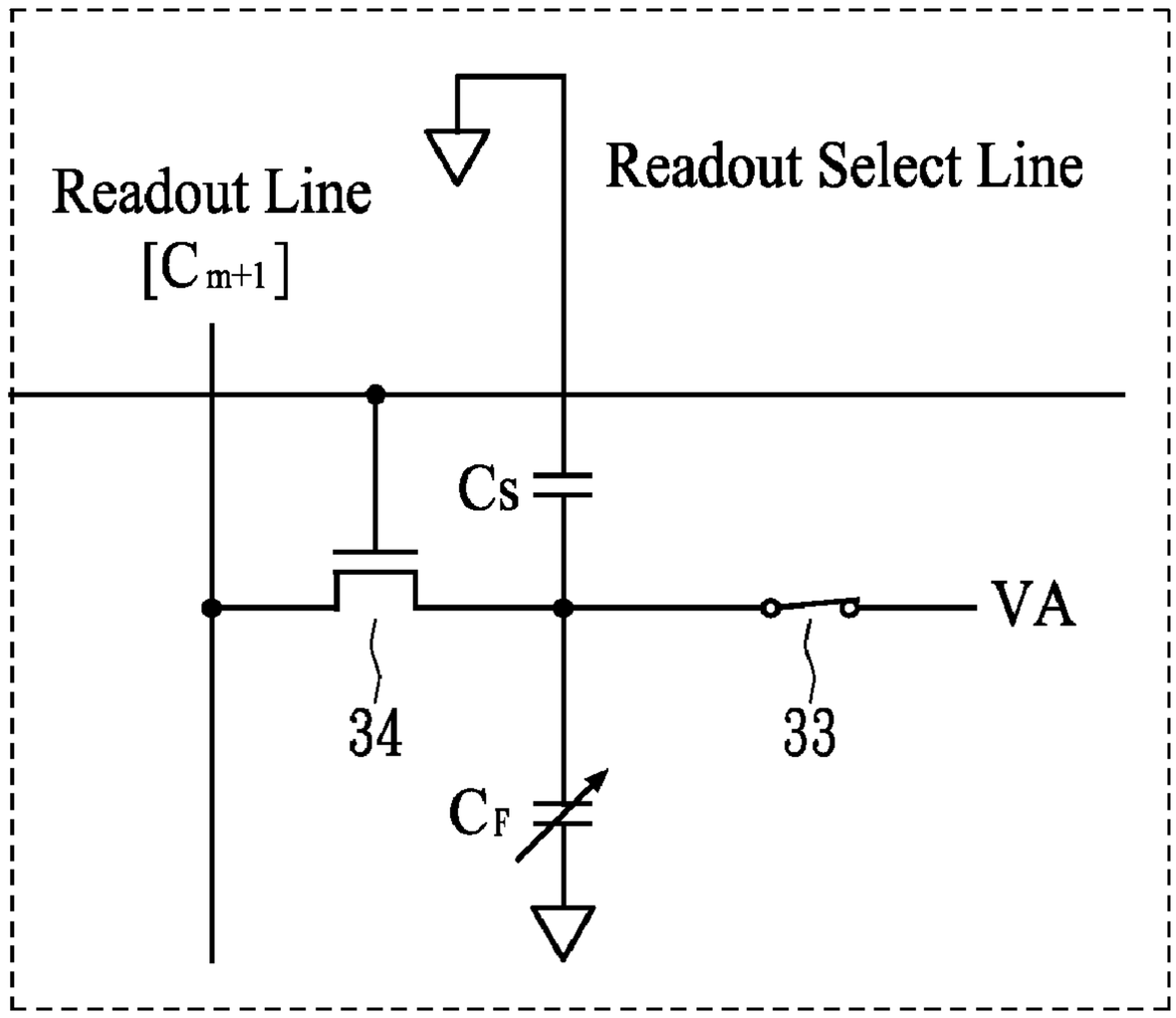

Readout Line
[C m+1]
Readout Select Line
Cs
VA
34
33
C F

FIG. 5A

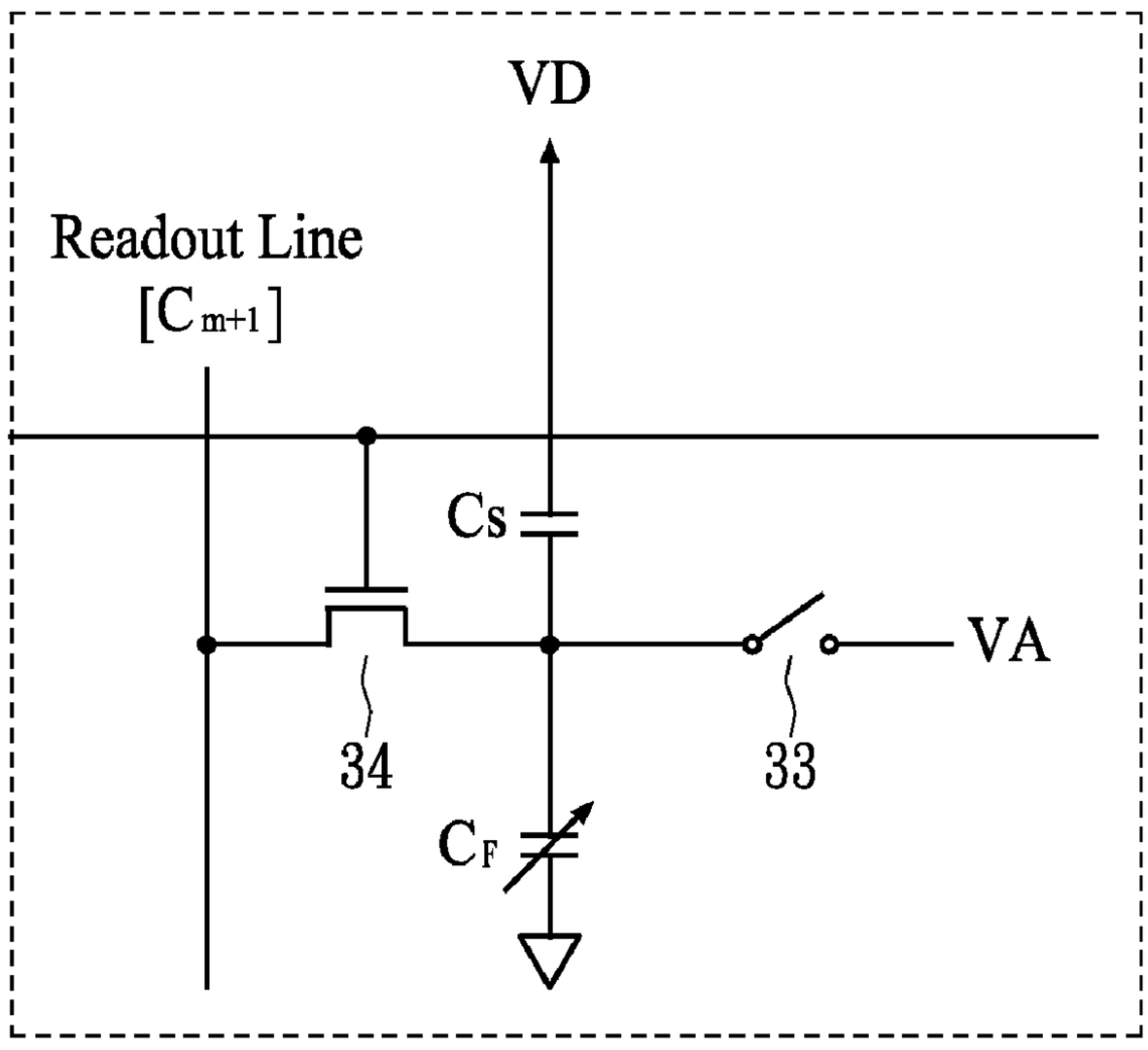

VD
Readout Line
[C m+1]
Cs
VA
34
33
C F

FIG. 5B

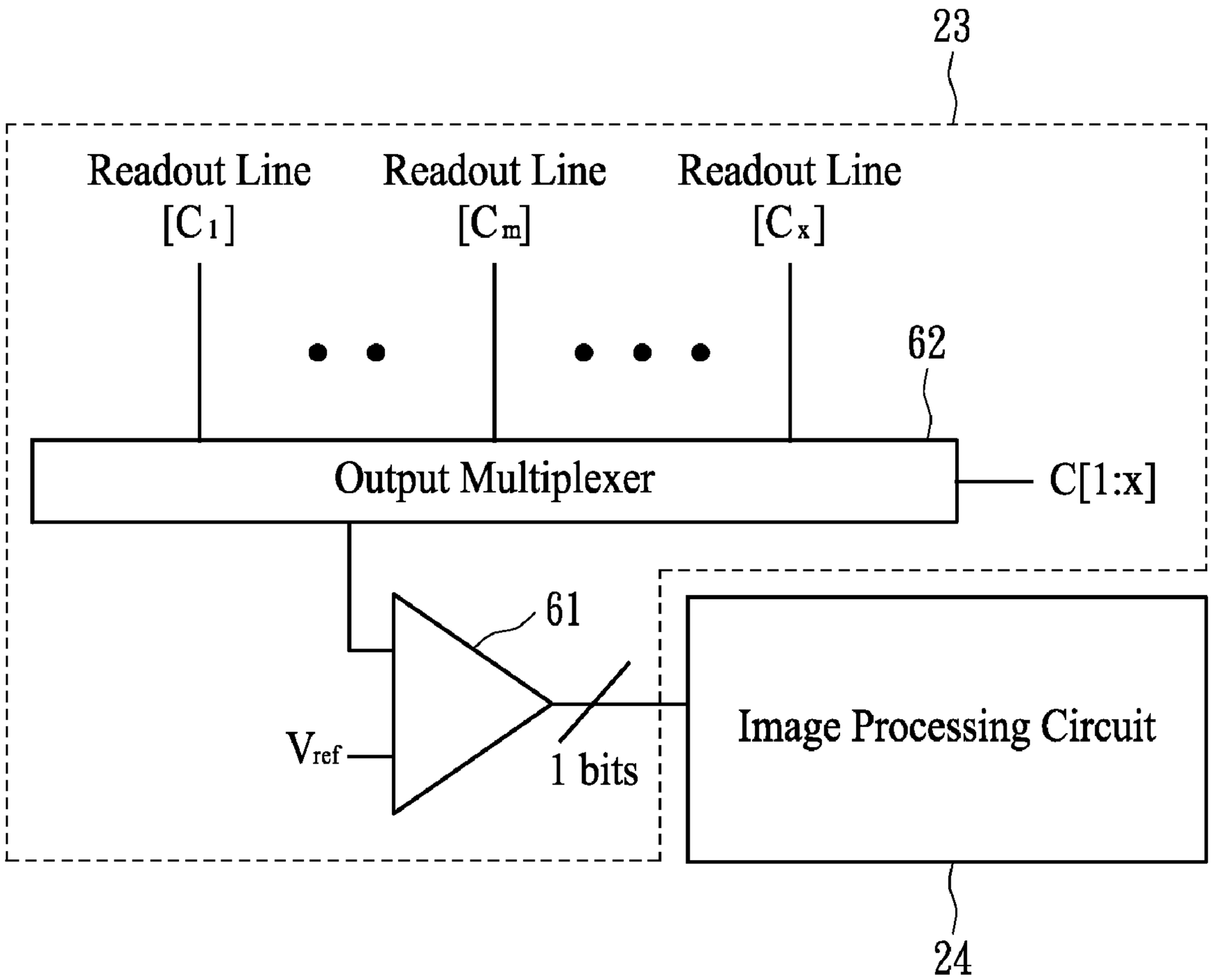

23
Readout Line
[C1]
Readout Line
[Cm]
Readout Line
[Cx]
62
Output Multiplexer
C[1:x]
61
Vref
1 bits
Image Processing Circuit
24

FIG. 6

CAPACITIVE FINGERPRINT SENSOR AND THE PANEL THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a capacitive fingerprint sensor and the panel thereof, and more particularly to a capacitive fingerprint sensor using a plurality of transistors and the panel thereof.

2. Description of the Related Art

A fingerprint sensor is a sensor for recognizing a pattern of a human fingerprint and providing reliable personal identification. The fingerprint sensor is also widely used in portable products such as mobile phones or notebooks in order to achieve security of personal confidential information.

FIGS. **1**A and **1**B show a hint diagram about the relationship between the human finger and a substrate panel and the corresponding equivalent diagram. Generally, the fingerprint sensor could be implemented in a chip or embedded in an image panel. If the fingerprint sensor is implemented in a chip, the number **13** in FIG. **1**A represents a passivation layer, which acts as the dielectric layer of the capacitor C_d. If the fingerprint sensor is embedded in an image panel, the number **11** in FIG. **1**A represents ITO layer, and number **13** represents glass and thin films, such as color filter, polarizer and etc. The following description takes the fingerprint sensor embedded in the image panel as an example. In FIG. **1**A, a glass **13**, a top metal plate **11** and a substrate **12** are combined in series, and the glass **13** is the place where the human finger will touch. Normally, a capacitor C_d exists in the glass **13**, and a capacitor C_p exists between the top metal plate **11** and the substrate **12**. In FIG. **1**B, the surface of the human finger has ridges and valleys, such as the ridge **14** and the valley **15**. The valley **15** has a distance d_2 away from the glass **13** with a thickness d_1. Based on the structure, an additional capacitor C**2** exists between the valley of the human finger and the surface of the glass **13**. The equivalent capacitance of the ridge capacitor C_{FR} is related to C**1**, and the equivalent capacitance of the valley capacitors C_{FV} is related to C**1**//C**2**. The capacitances of C**1** and C**1**//C**2** are listed as follows:

$$C_1 = \frac{\varepsilon_1 A}{d_1},$$

and

$$C_1 // C_2 = \frac{1}{\frac{d_1}{\varepsilon_1 A} + \frac{d_2}{\varepsilon_2 A}}$$

Normally, the ridge capacitor C_{FR} is far greater than the valley capacitors C_{FV}.

For sensing the human fingerprint, a readout circuit should be able to discern the difference between the ridge capacitor and the valley capacitor However, it is not easy to achieve the required accuracy in difference. Some environmental conditions such as noise and cross talk will deteriorate the result.

SUMMARY OF THE INVENTION

The capacitive fingerprint sensor in accordance with one embodiment of the present invention comprises a first transistor, a fingerprint capacitor, a reference capacitor and a second transistor. The first transistor has a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a first readout select line, and the input terminal is connected to a bias voltage VA. The fingerprint capacitor C_F is connected to the output terminal of the first transistor, wherein the fingerprint capacitor has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR}. One end of the reference capacitor is connected to the output terminal of the first transistor, and the other end of the reference capacitor is connected to a second readout select line, wherein the second readout select line is immediately next to the first readout select line, and the reference capacitor has a capacitance C_S, $C_{FV}<C_S<C_{FR}$. The second transistor has a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a scan line, the input terminal is connected to the reference capacitor, and the output terminal is connected to a readout line.

The capacitive fingerprint sensor in accordance with one embodiment of the present invention comprises a fingerprint capacitor, a reference capacitor, a first transistor and a second transistor. The fingerprint capacitor C_F has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR}. The reference capacitor C_S has a capacitance C_S, and $C_{FV}<C_S<C_{FR}$. The first transistor is configured to precharge the reference capacitor and the fingerprint capacitor during a precharge phase. The second transistor is configured to output the voltage of the reference capacitor during an evaluation phase. The precharge phase is controlled by a first readout select line, the evaluation phase is controlled by a second readout select line, the second readout select line is immediately next to the first readout select line, and the valid time to access the readout line is within an enabling period of the second readout select line.

The panel system in accordance with one embodiment of the present invention comprises an active matrix area, a data driver, a scan driver, a readout circuit and an image processing circuit. The active matrix area has the above-mentioned capacitive fingerprint sensors. The data driver is configured to drive data lines to the capacitive fingerprint sensors. The scan driver is configured to control scan lines to the capacitive fingerprint sensors. The readout circuit is configured to receive readout lines of the capacitive fingerprint sensors and to identify the type of the fingerprint capacitor. The image processing circuit is connected to the readout circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described according to the appended drawings in which:

FIGS. **1**A and **1**B show an equivalent circuit of a fingerprint sensor;

FIG. **2** shows the panel in accordance with an embodiment of the present invention;

FIG. **3** shows the fingerprint sensor in accordance with an embodiment of the present invention;

FIG. **4** shows the timing diagram of the circuit in FIG. **3**;

FIGS. **5**A and **5**B show the precharge and evaluation phases of the circuit in FIG. **3**; and

FIG. **6** shows the readout circuit in accordance with an embodiment of the present invention.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION

FIG. **2** shows a panel in accordance with an embodiment of the present invention. The panel system comprises an active matrix area **25**, a data driver **21**, a scan driver **22**, a readout circuit **23** and an image processing circuit **24**. The active matrix area **25** has a plurality of capacitive fingerprint sensors **31**, each of which can selectively coexist with an image pixel

in a pixel unit. The data driver **21** is configured to drive data lines. The scan driver **22** is configured to control scan lines to the capacitive fingerprint sensors **31**. Normally, the scan line is asserted during the operation period of the capacitive fingerprint sensors connected to the scan line. The readout circuit **23** is configured to receive analog signals of readout lines of the capacitive fingerprint sensors **31** and to identify the type of the fingerprint capacitor, which exhibits the features of the ridge capacitor or valley capacitor. The image processing circuit **24** is connected to the readout circuit **23**. The structure in FIG. **2** takes an embedded structure in an image panel as an example. But as known by persons skilled in this art, the structure in FIG. **2** can be easily transformed and applied to be implemented in a chip.

FIG. **3** shows the fingerprint sensor in accordance with an embodiment of the present invention. The capacitive fingerprint sensor **31** comprises a first transistor **33**, a second transistor **34**, a fingerprint capacitor C_F and a reference capacitor C_s. FIG. **3** in fact shows two sets of fingerprint sensors adjacent in the same row with the same scan line. Normally, when the preceding fingerprint sensor **32** is in an evaluation phase, the fingerprint sensor **31** is in a precharge phase. And when the fingerprint sensor **31** is in an evaluation phase, the succeeding fingerprint sensor (not shown) is in a precharge phase. The first transistor **33** has a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a first readout select line C_m, and the input terminal is connected to a bias voltage VA. The second transistor **34** has a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a scan line R_n, the input terminal is connected to the reference capacitor, and the output terminal is connected to a readout line. The fingerprint capacitor C_F is connected to the input terminal of the second transistor **34**, wherein the fingerprint capacitor C_F has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR}. The reference capacitor is connected to the output terminal of the first transistor **33**, wherein the reference capacitor has a capacitance C_S, and $C_{FV}<C_S<C_{FR}$.

FIG. **4** shows the timing diagram of the circuit in FIG. **3**. Normally, the fingerprint sensors in the same row share the same scan line R_n, which is asserted over the entire operation duration of the fingerprint sensors in the same row. The readout select lines C_0 to C_x connecting to each fingerprint sensor are asserted in sequence and do not overlap each other. The readout select lines C_0 to C_x are used to initiate the evaluation phase and precharge phase of each fingerprint sensor, so as to sequentially read out data from the fingerprint sensors of one row corresponding to the asserted scan line. The pulse amplitude of each readout select line is denoted as VD. It should be noted that the readout circuit **23** should read the readout line before unasserting the corresponding readout select line. For example, the time to read the readout line [Cm+1] begins at the asserting readout select line [Cm+1] and ends before unasserting the readout select line [Cm+1].

FIG. **5**A shows the equivalent circuit of the fingerprint sensor **31** in the precharge phase. In the precharge phase for the fingerprint sensor **31**, the readout select line C_m is asserted to turn on the first transistor **33**, and the bias voltages VA precharges the reference capacitor C_S and fingerprint capacitor C_F, respectively.

FIG. **5**B shows the equivalent circuit of the fingerprint sensor **31** in the evaluation phase. In the evaluation for the fingerprint sensor **31**, the readout select line C_{m+1} is asserted as VD, and the electrical charges stored in the reference capacitor C_S and fingerprint capacitor C_F are redistributed. At this moment, the scan line is still asserted, the second transistor **34** is enabled, and the readout line outputs voltage

$$VA + \frac{C_S}{C_S + C_{FR}} \times VD$$

or

$$VA + \frac{C_S}{C_S + C_{FV}} \times VD,$$

depending on which portion of the human fingerprint, i.e., ridge or valley is detected. Apparently, the outputs voltage of the readout line is larger if the valley is detected than if the ridge is detected.

FIG. **6** shows the readout circuit in accordance with an embodiment of the present invention. The readout circuit **23** comprises a multiplexer **62** and a comparator **61**. The input end of the multiplexer **62** is connected to the readout lines, and the output end of the multiplexer **62** is connected to the comparator **61**, which outputs one bit to the image processing circuit **24**. For distinguishing the ridge and valley capacitors, the comparator **61** utilizes a threshold voltage V_{REF}, and

$$VA + \frac{C_S}{C_S + C_{FV}} \times VD > V_{REF} > VA + \frac{C_S}{C_S + C_{FR}} \times VD.$$

Therefore, if the comparator **61** outputs logic high, it means that the data received from the fingerprint sensor implies a valley capacitor. Otherwise, the data implies a ridge capacitor.

The above-described embodiments of the present invention are intended to be illustrative only. Numerous alternative embodiments may be devised by persons skilled in the art without departing from the scope of the following claims.

What is claimed is:

1. A capacitive fingerprint sensor, comprising:

a first transistor having a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a first readout select line, and the input terminal is connected to a bias voltage VA;

a fingerprint capacitor connected to the output terminal of the first transistor, wherein the fingerprint capacitor has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR};

a reference capacitor, wherein one end of the reference capacitor is connected to the output terminal of the first transistor, and the other end of the reference capacitor is connected to a second readout select line, wherein the second readout select line is immediately next to the first readout select line, and the reference capacitor has a capacitance C_S, and $C_{FV}<C_S<C_{FR}$; and

a second transistor having a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a scan line, the input terminal is connected to the reference capacitor, and the output terminal is connected to a readout line.

2. The capacitive fingerprint sensor of claim **1**, wherein in a precharge phase, the first readout select line is asserted.

3. The capacitive fingerprint sensor of claim **2**, wherein in an evaluation phase, the scan line and the second readout select line are asserted such that a readout voltage at the output terminal of the second transistor is outputted to the readout line.

4. The capacitive fingerprint sensor of claim 3, wherein the readout voltage is larger if the fingerprint capacitor has the valley capacitance C_{FV} than if the fingerprint capacitor has the ridge capacitance C_{FR}.

5. The capacitive fingerprint sensor of claim 4, wherein the readout line has a voltage of

$$VA + \frac{C_S}{C_S + C_{FR}} \times VD$$

or

$$VA + \frac{C_S}{C_S + C_{FV}} \times VD$$

during the evaluation phase, and VD represents the enabling voltage of the second readout select line.

6. The capacitive fingerprint sensor of claim 1, wherein the scan line is asserted during the precharge phase and evaluation phase.

7. A capacitive fingerprint sensor, comprising:

a fingerprint capacitor having a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR};

a reference capacitor having a capacitance C_S, and $C_{FV}<C_S<C_{FR}$;

a first transistor precharging the reference capacitor and the fingerprint capacitor during a precharge phase;

a second transistor outputting the voltage of the fingerprint capacitor to a readout line during an evaluation phase;

wherein the precharge phase is controlled by a first readout select line, the evaluation phase is controlled by a second readout select line, the second readout select line is immediately next to the first readout select line, and a valid time to access the readout line is within an enabling period of the second readout select line.

8. The capacitive fingerprint sensor of claim 7, wherein the readout voltage is larger if the fingerprint capacitor has the valley capacitance C_{FV} than if the fingerprint capacitor has the ridge capacitance C_{FR}.

9. The capacitive fingerprint sensor of claim 8, wherein the first transistor is precharging the reference capacitor and the fingerprint capacitor to a bias voltage VA.

10. The capacitive fingerprint sensor of claim 9, wherein the first transistor is used in a precharge phase, the second transistor is used in an evaluation phase, and the precharge phase does not overlap the evaluation phase.

11. The capacitive fingerprint sensor of claim 10, wherein the voltage of the reference capacitor after redistribution has a voltage of

$$VA + \frac{C_S}{C_S + C_{FR}} \times VD$$

or

$$VA + \frac{C_S}{C_S + C_{FV}} \times VD$$

during the evaluation phase, and VD represents an enabling voltage of the second readout select line.

12. A panel system including capacitive fingerprint sensors, comprising:

an active matrix area having capacitive fingerprint sensors and image pixels, the capacitive fingerprint sensor comprising:

a first transistor having a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a first readout select line, and the input terminal is connected to a bias voltage VA;

a fingerprint capacitor connected to the output terminal of the first transistor, wherein the fingerprint capacitor has a capacitance that is either a valley capacitance C_{FV} or a ridge capacitance C_{FR};

a reference capacitor, wherein one end of the reference capacitor is connected to the output terminal of the first transistor, and the other end of the reference capacitor is connected to a second readout select line, wherein the second readout select line is immediately next to the first readout select line, the reference capacitor has a capacitance C_S, and $C_{FV}<C_S<C_{FR}$; and

a second transistor having a gate terminal, an input terminal and an output terminal, wherein the gate terminal is controlled by a scan line, the input terminal is connected to the reference capacitor, and the output terminal is connected to a readout line;

a data driver driving data lines of the image pixels;

a scan driver controlling scan lines to the capacitive fingerprint sensors;

a readout circuit receiving readout lines of the capacitive fingerprint sensors and to identify the type of the fingerprint capacitor; and

an image processing circuit connected to the readout circuit.

13. The panel system of claim 12, wherein the readout circuit comprises a multiplexer and a comparator, the input end of the multiplexer is connected to the readout lines, and the output end of the multiplexer is connected to the comparator.

14. The panel system of claim 13, wherein the comparator outputs to the image processing circuit.

15. The panel system of claim 13, wherein the comparator has a threshold voltage

$$V_{REF},\ VA + \frac{C_S}{C_S + C_{FV}} \times VD > V_{REF} > VA + \frac{C_S}{C_S + C_{FR}} \times VD,$$

and VD represents an enabling voltage of the second readout select line.

16. The panel system of claim 12, wherein the active matrix area further includes image pixels connected to the data lines.

17. The panel system of claim 12, wherein one of the capacitive fingerprint sensors is in a precharge phase when its preceding adjacent one is in an evaluation phase.

18. The panel system of claim 12, wherein one scan line is asserted during the operations of the capacitive fingerprint sensors connected to the scan line.

* * * * *