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Umemoto et al.

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(54) **POWER SUPPLY APPARATUS**

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(73) Assignee: **Rohm Co., Ltd.**, Kyoto (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 95 days.

This patent is subject to a terminal disclaimer.

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(22) Filed: **Nov. 15, 2006**

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(30) **Foreign Application Priority Data**

Apr. 16, 2003 (JP) 2003-111242

(51) **Int. Cl.**
G05F 1/40 (2006.01)

(52) **U.S. Cl.** **323/282**

(58) **Field of Classification Search** 323/282, 323/283, 284, 285, 351
See application file for complete search history.

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(57) **ABSTRACT**

In a power supply apparatus that is so configured as to produce from an input voltage an output voltage Vo within a predetermined permissible variation range, the output voltage Vo is so controlled as to decrease within the permissible variation range as the output current Io increases. This configuration offers an output voltage with an improved transient characteristic against an abrupt variation in the output current and simultaneously permits reduction of the power consumed when the output current increases.

1 Claim, 5 Drawing Sheets

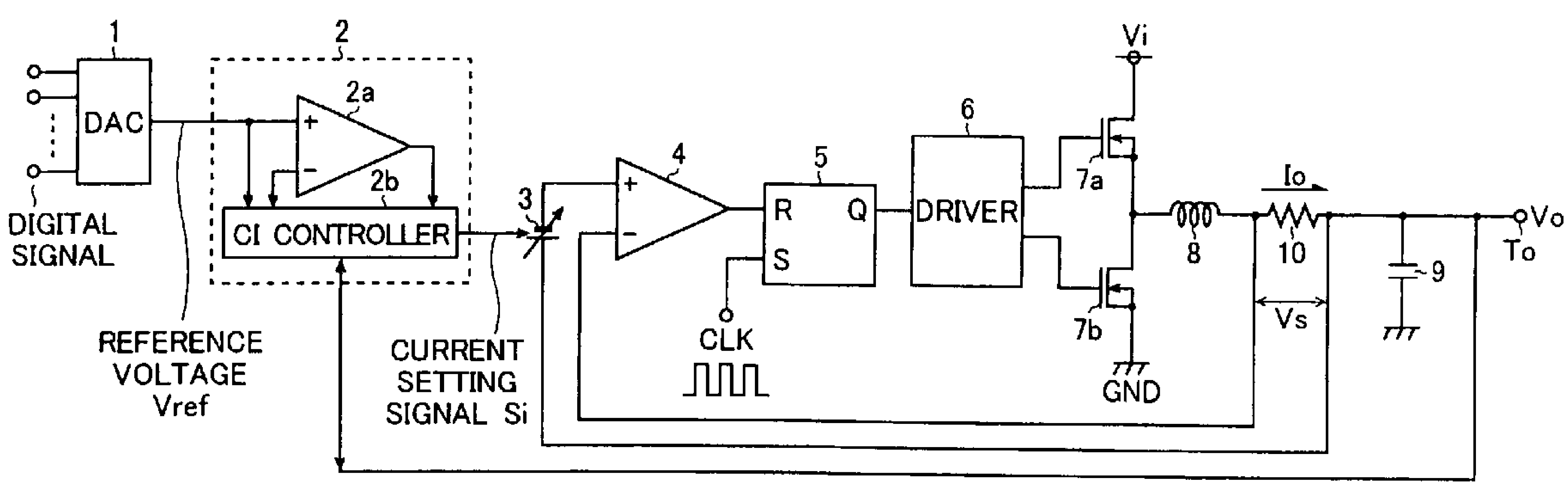
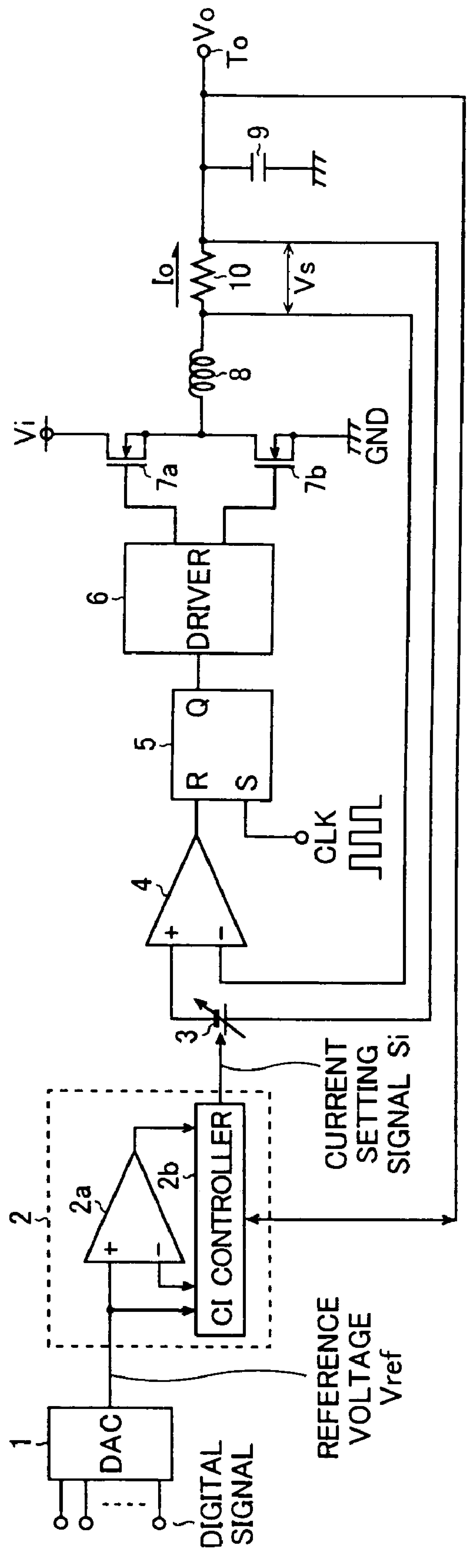
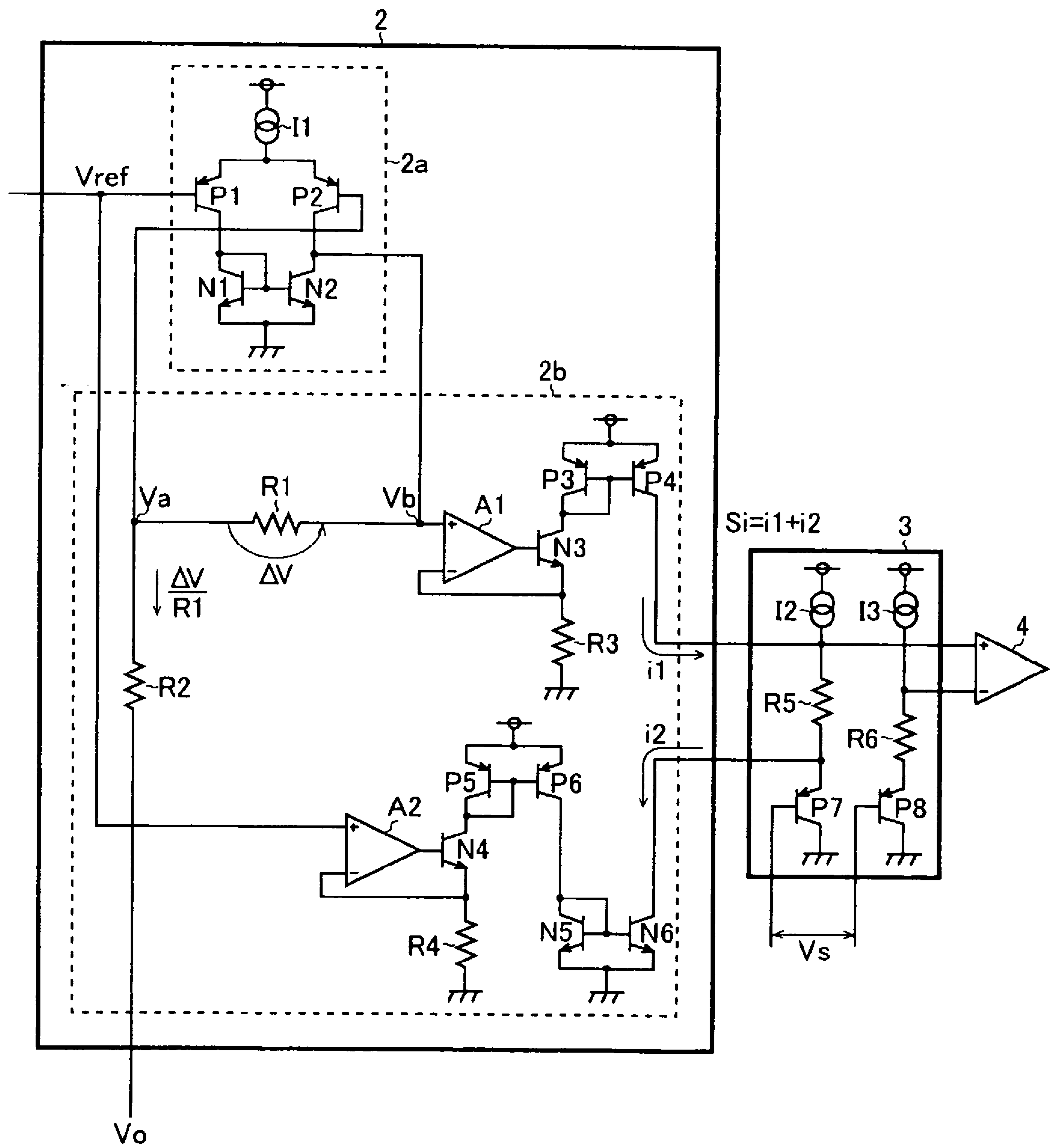


FIG. 1



DIGITAL SIGNAL
1
DAC
REFERENCE VOLTAGE Vref
2
2a
2b
CI CONTROLLER
CURRENT SETTING SIGNAL Si
3
4
5
R
S
Q
CLK
6
DRIVER
Vi
7a
7b
GND
8
Io
10
Vs
9
Vo
To

F I G. 2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Vref
P1
P2
N1
N2
2b
P3
P4
Va
R1
Vb
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N3
ΔV
ΔV/R1
R3
R2
i1
Si=i1+i2
3
I2
I3
4
R5
R6
i2
P5
P6
A2
N4
P7
P8
R4
N5
N6
Vs
Vo

FIG. 3A

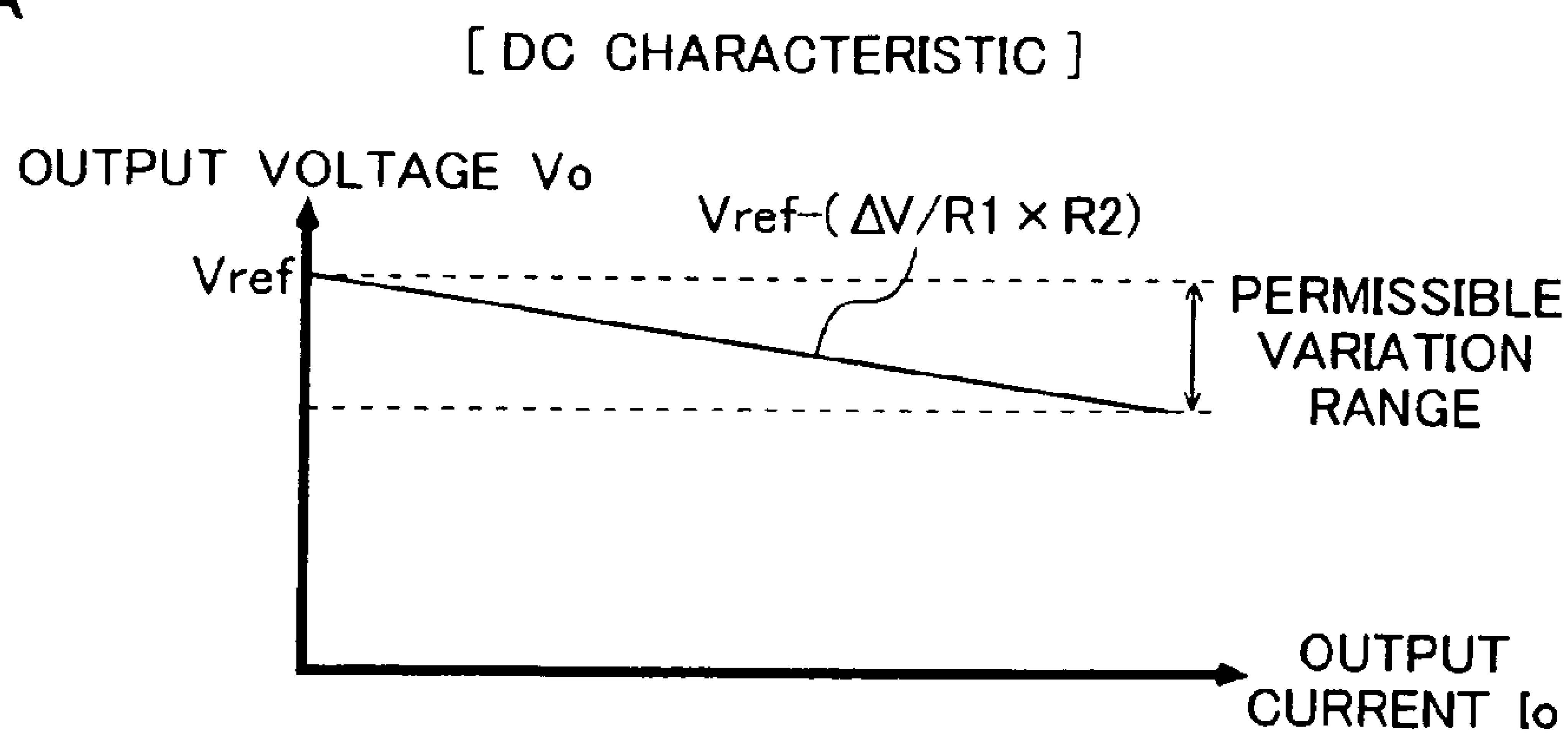


FIG. 3B

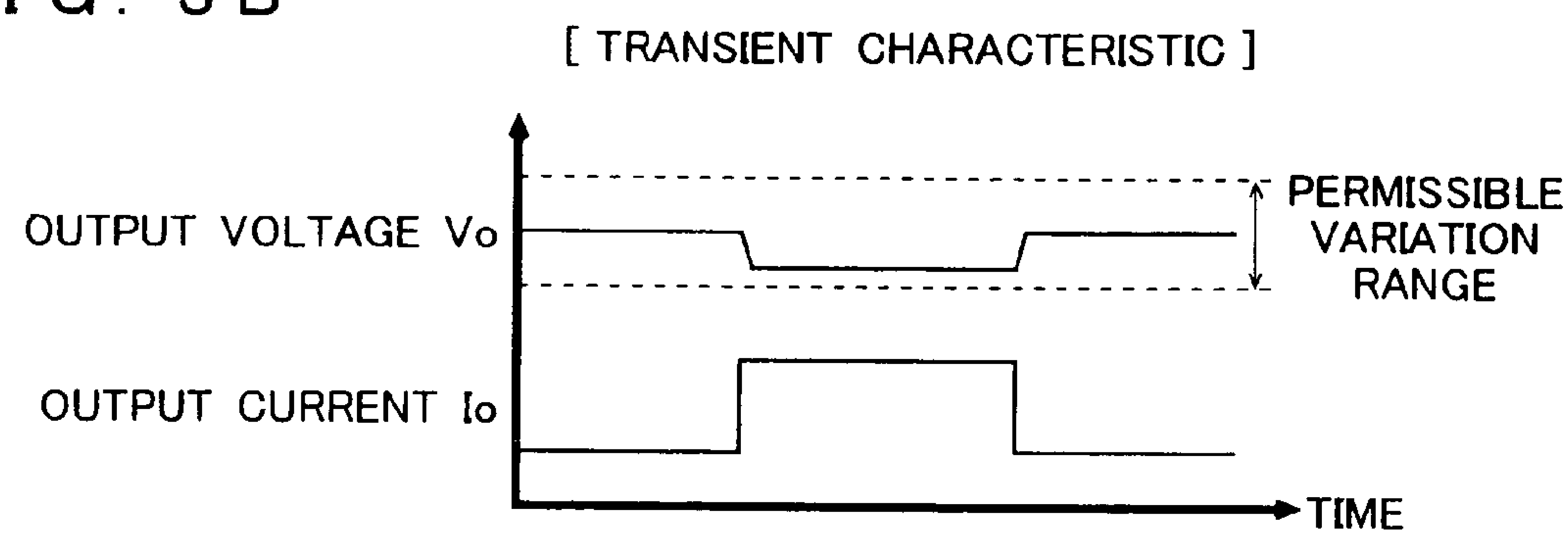
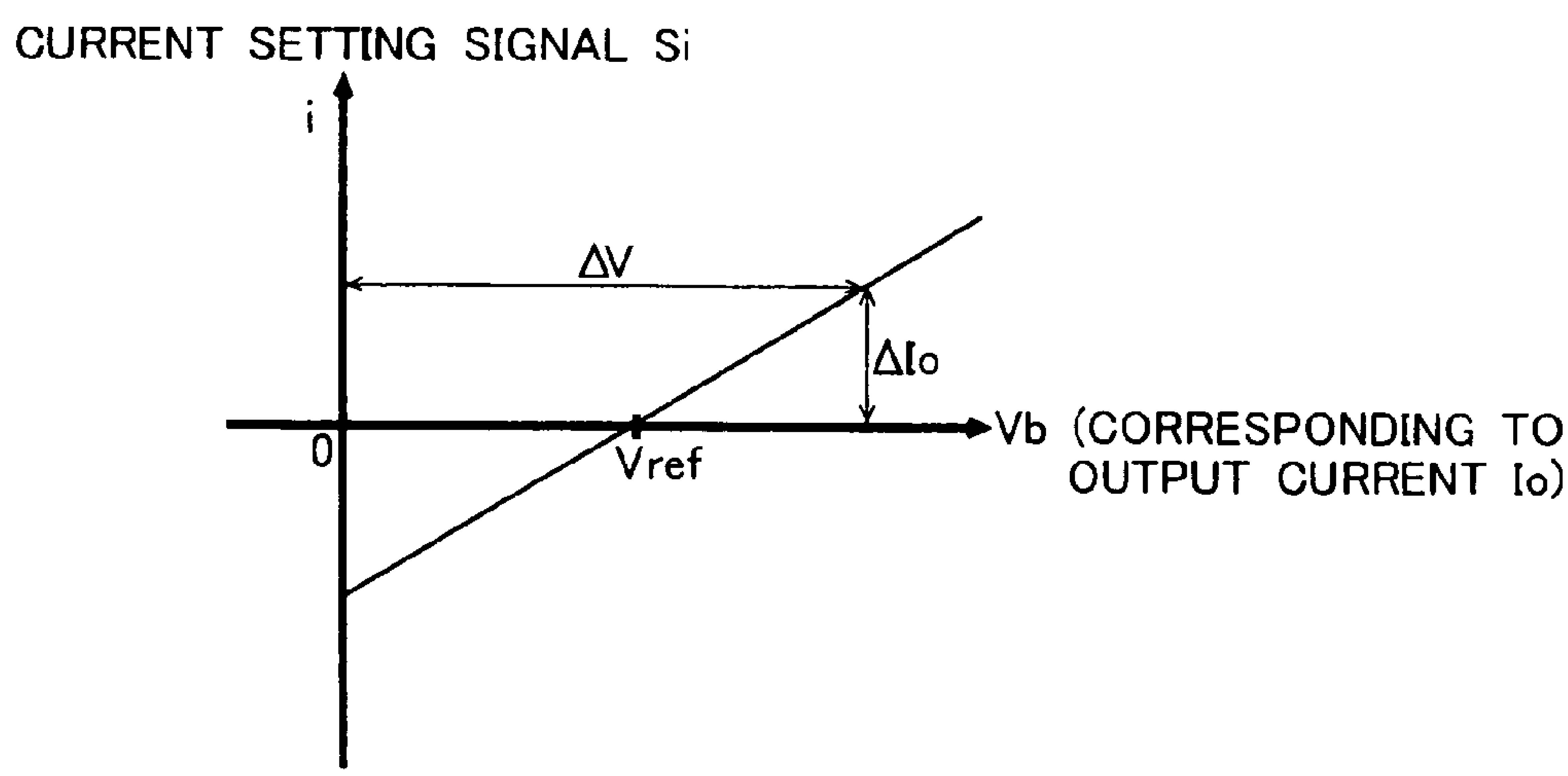
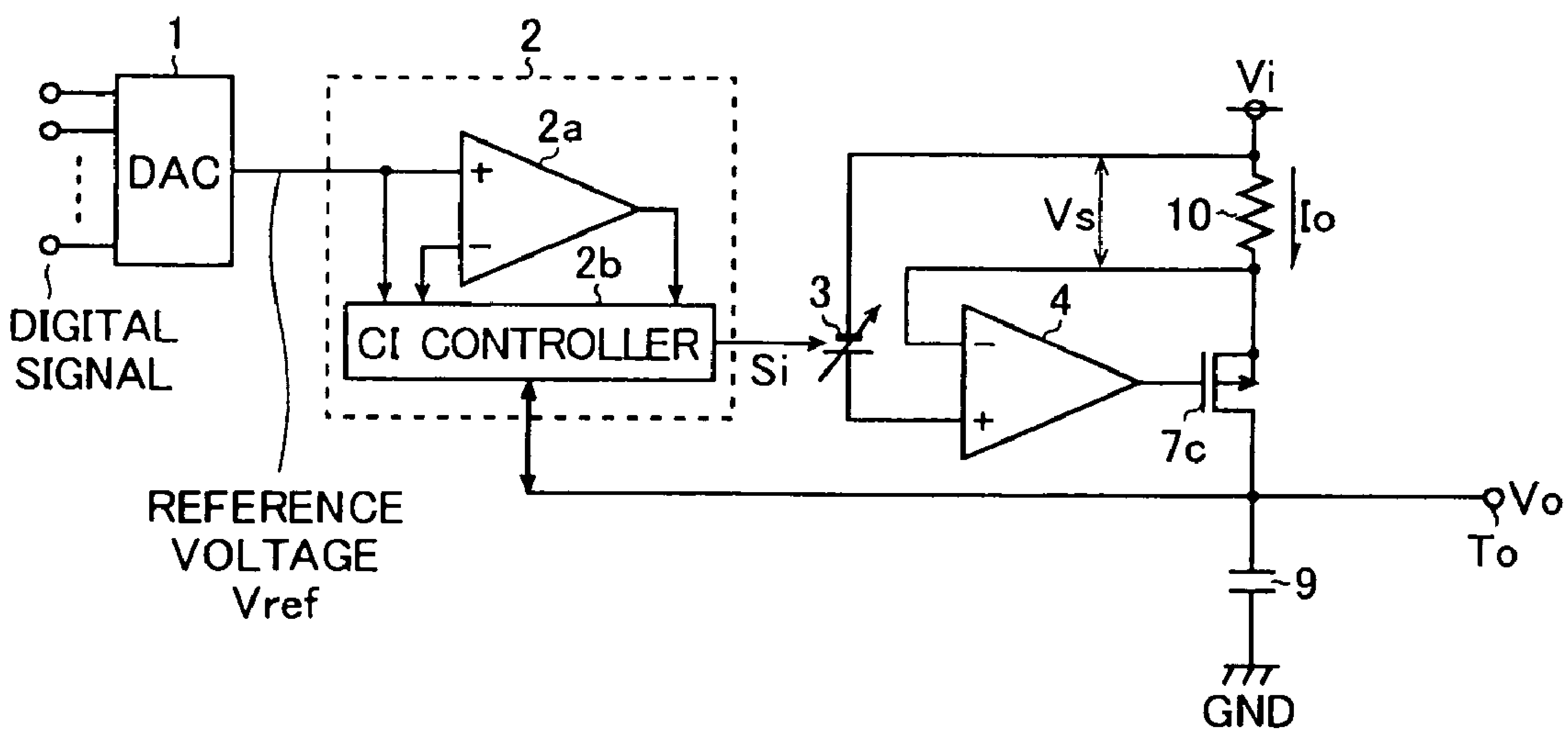


FIG. 4



F I G. 5


1
DAC
DIGITAL
SIGNAL
REFERENCE
VOLTAGE
Vref
2
2a
2b
CI CONTROLLER
Si
3
4
7c
Vi
Vs
10
Io
Vo
To
9
GND

F I G. 6

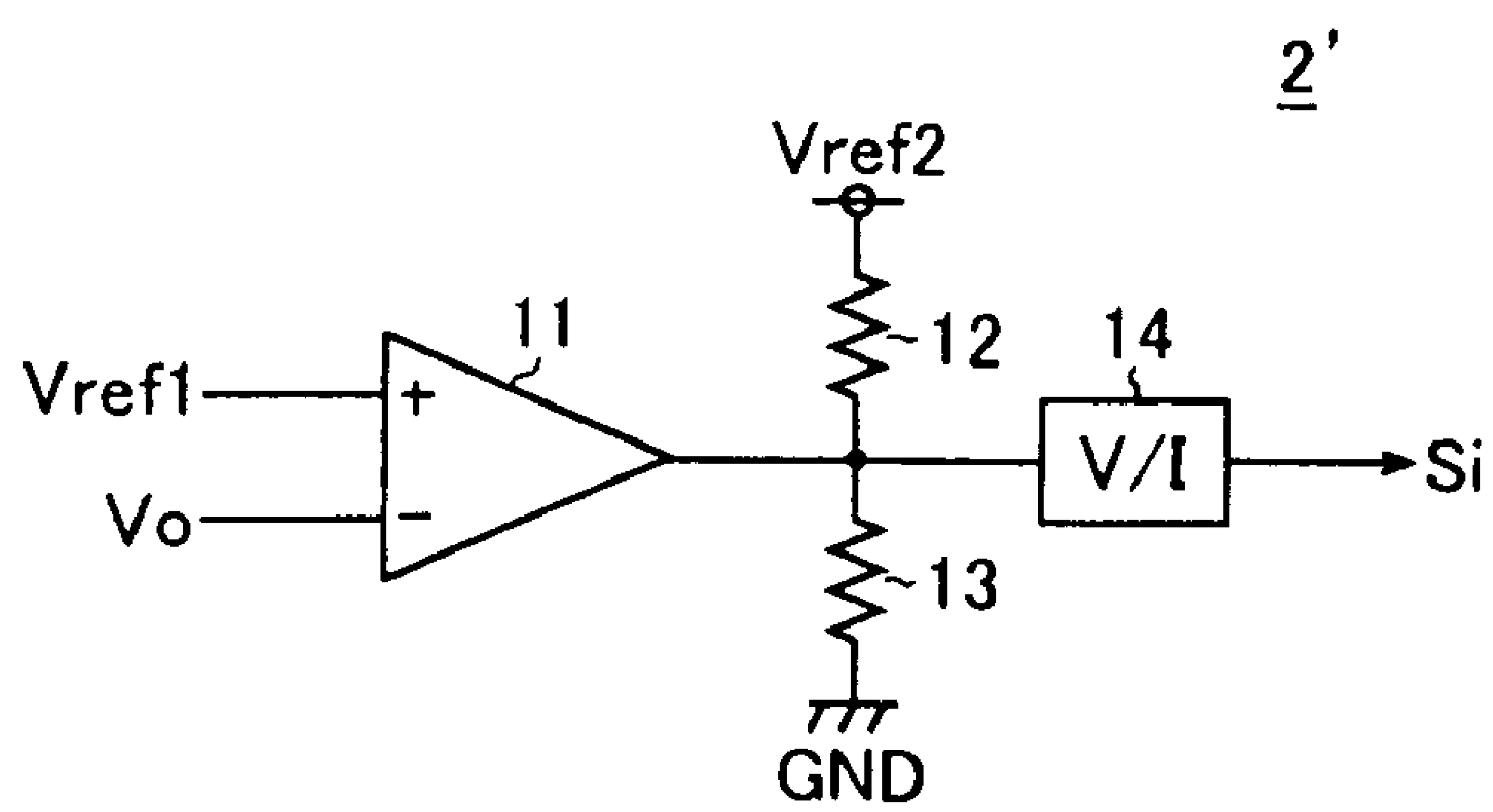

2'
Vref2
Vref1
Vo
11
12
13
14
V/I
Si
GND

FIG. 7A
Prior Art

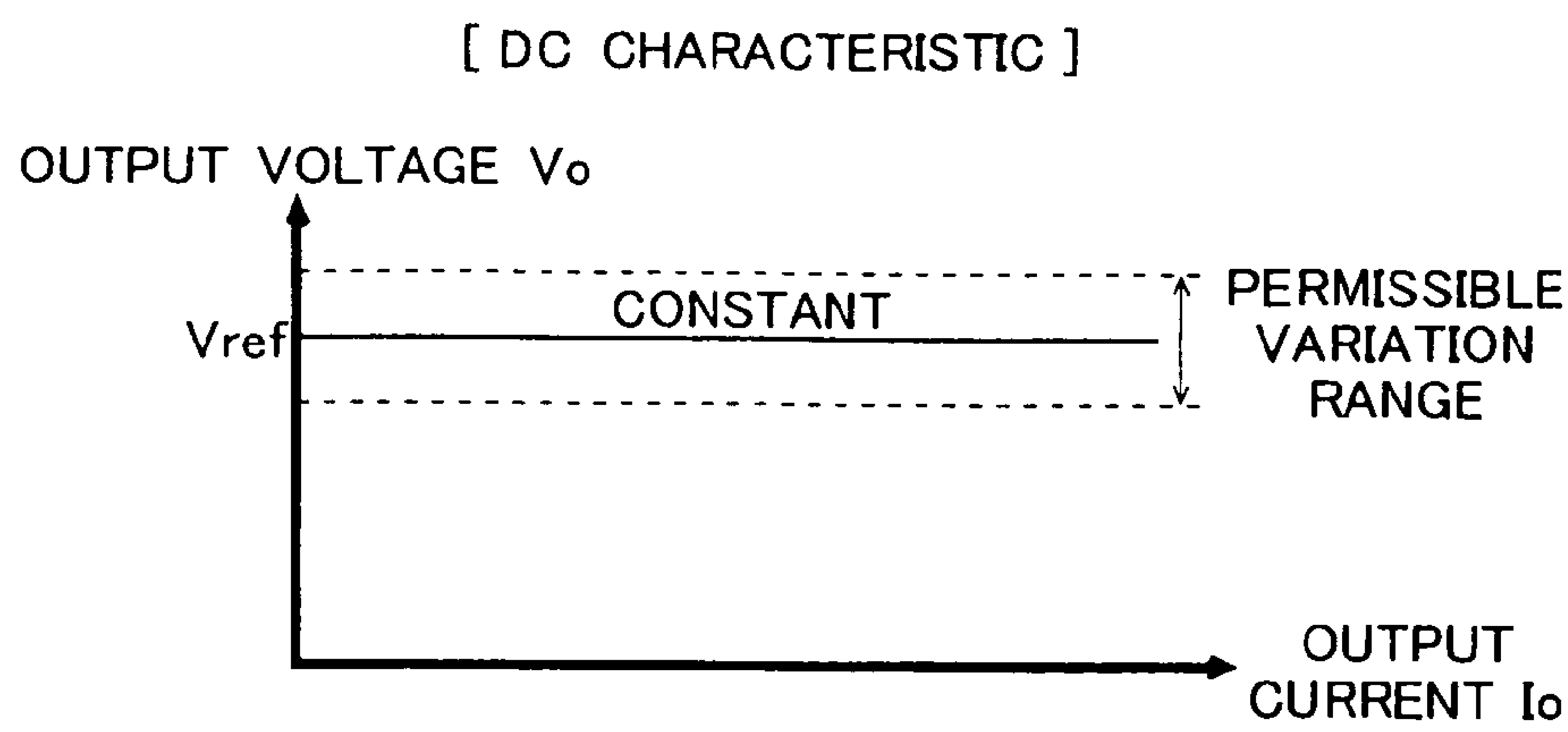
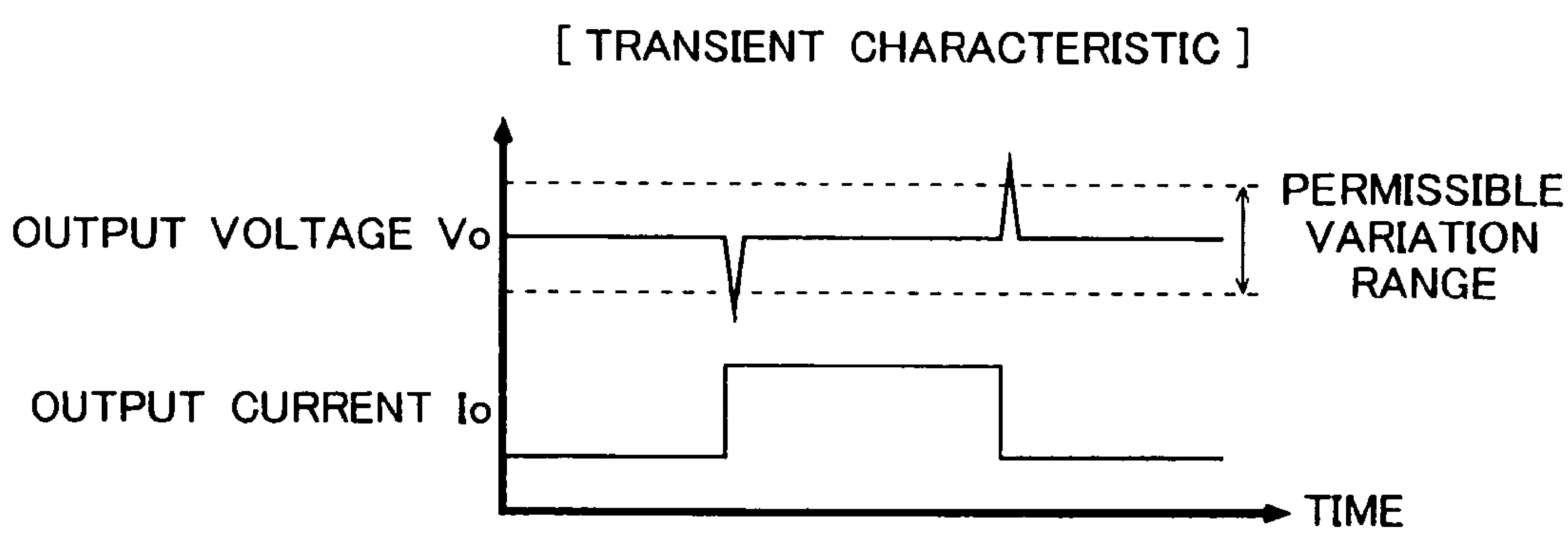


FIG. 7B
Prior Art



POWER SUPPLY APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Divisional Application, which claims the benefit of U.S. patent application Ser. No. 10/822,660, filed Apr. 13, 2004, now U.S. Pat. No. 7,148,667 which claims priority based on Japanese Patent Application No. 2003-111242 filed on Apr. 16, 2003. The disclosure of the prior application is hereby incorporated herein in its entirety by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power supply apparatus that generates from an input voltage an output voltage that is permitted to vary within a predetermined permissible variation range.

2. Description of the Prior Art

Conventionally, in a power supply apparatus that generates from an input voltage Vi an output voltage Vo that is permitted to vary within a predetermined permissible variation range, the output voltage Vo is kept equal to a predetermined reference voltage Vref (a constant level that is not influenced by a increase or decrease in the output current Io) through the feedback control of the output voltage Vo (see FIG. **7**A).

It is true that, with the power supply apparatus that performs the control described above, a load can be supplied with the output voltage Vo of the power. supply apparatus as a voltage of which the variation is within the permissible variation range even when the input voltage Vi or the output current Io varies slightly.

However, in the power supply apparatus that performs the control described above, when the output current Io varies so abruptly as not to be coped with by the feedback loop of the output voltage Vo, a large variation occurs in the output voltage Vo, causing, in the worst case, the output voltage Vo to go out of the permitted variation range (see FIG. **7**B). This is one problem with the conventional power supply apparatus. A solution to this problem has been becoming especially critical in recent years as semiconductor chips (such as CPUs) used as a load for such a power supply apparatus consume increasingly large currents and operates at increasingly high speeds and thus require increasingly stable output voltages Vo even in the event of an abrupt variation in the load. Moreover, in the power supply apparatus configured as described above, the feedback control is so performed that the output voltage Vo is kept equal to the reference voltage Vref that is not influenced by an increase or decrease in the output current Io. This causes the power consumption by the load to increase as the output current Io increases. This is another problem with the conventional power supply apparatus.

Various techniques have conventionally been disclosed and proposed to give a solution to the problems mentioned above (for example, see Japanese Patent Application Laid-Open No. 2002-186254). However, all of those techniques attempt to solve the problems by increasing the response of the feedback loop, and are thus basically no different from the conventional configuration described above in that they perform feedback control so that the output voltage Vo is kept at a constant level that is not influenced by an increase or decrease in the output current Io. As long as such a configuration is used, the transient characteristic of the output voltage Vo cannot be improved beyond a certain limit. That is, in the event of an abrupt variation in the output current Io, there still is a risk, in the worst case, of the output voltage Vo going out of the permitted variation range. Moreover, as the output current Io increases, the power consumption by the load still tends to increase.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a power supply apparatus that offers an output voltage with an improved transient characteristic against an abrupt variation in the output current and that simultaneously permits reduction of the power consumed when the output current increases.

To achieve the above object, according to the present invention, a power supply apparatus is provided with: a circuit that produces from an input voltage an output voltage within a predetermined permissible variation range; and a circuit that, as the output current increases, decreases the target level of the output voltage within the permissible variation range.

BRIEF DESCRIPTION OF THE DRAWINGS

This and other objects and features of the present invention will become clear from the following description, taken in conjunction with the preferred embodiments with reference to the accompanying drawings in which:

FIG. **1** is a circuit diagram showing the power supply apparatus of a first embodiment of the invention;

FIG. **2** is a circuit diagram showing the output voltage comparison circuit **2** and the offset circuit **3**;

FIGS. **3**A and **3**B are diagrams showing the DC and transient characteristics, respectively, of a power supply apparatus embodying the invention;

FIG. **4** is a diagram showing the correlation characteristic of the current setting signal Si with respect to the output current Io;

FIG. **5** is a circuit diagram showing the power supply apparatus of a second embodiment of the invention;

FIG. **6** is a circuit diagram showing the power supply apparatus of a third embodiment of the invention; and

FIGS. **7**A and **7**B are diagrams showing the DC and transient characteristics, respectively, of a conventional power supply apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is a circuit diagram showing the power supply apparatus of a first embodiment of the invention. As shown in this figure, the power supply apparatus of this embodiment is composed of a digital-to-analog converter **1** (hereinafter referred to as the DAC **1**), an output voltage comparison circuit **2**, an offset circuit **3**, an output current comparator **4**, a reset-priority S-R flip-flop **5**, an output transistor driving circuit **6** (hereinafter referred to as the driver **6**), N-channel MOS field-effect transistors **7***a* and **7***b* (hereinafter referred to as the FETs **7***a* and **7***b*), an output coil **8**, an output capacitor **9**, and a sense resistor Io. The power supply apparatus is designed as a DC/DC converter of a synchronous rectification type wherein a desired output voltage Vo obtained from the node between the pair of FETs **7***a* and **7***b* connected in series between two different potentials (between an input potential Vi and the ground potential GND) so as to function as switching devices is passed through an LC filter (composed of the output coil **8** and the output capacitor **9**) and is then fed out via an output terminal To.

The DAC **1** converts a digital signal fed in from outside the apparatus into an analog signal to produce a reference voltage Vref with reference to which the output voltage Vo is determined. It should be noted that, when the output current Io is zero, the reference voltage Vref itself is fed out as the output voltage Vo (see FIG. **4**). The output voltage comparison circuit **2** is composed of an operational amplifier **2***a* and a constant-impedance controller **2***b* (hereinafter referred to as the CI controller **2***b*), and produces, on the basis of the result of comparison between the reference voltage Vref and the output voltage Vo, a setting current signal Si to be fed to the offset circuit **3**. The internal configuration and operation of the output voltage comparison circuit **2** will be described in detail later. On the basis of the setting current signal Si produced by the output voltage comparison circuit **2**, the offset circuit **3** gives a predetermined offset between the two input terminals of the output current comparator **4**.

The output terminal of the output current comparator **4** is connected to the reset input terminal (R) of the S-R flip-flop **5**. The set input terminal (S) of the S-R flip-flop **5** is connected to a clock terminal to which a clock signal CLK (having a frequency of 200 [kHz] to 1 [MHz], for example) is fed, and the output terminal (Q) of the S-R flip-flop **5** is connected to the input terminal of the driver **6**. The driver **6** has two output terminals, which are connected to the gates of the FETs **7***a* and **7***b*, respectively.

The drain of the FET **7***a* is connected to a supply voltage line, and the source of the FET **7***b* is grounded. The source of the FET **7***a* and the drain of the FET **7***b* are connected together, and the node between them is connected through the output coil **8** to one end of the sense resistor **10**. The other end of the sense resistor **10** is connected to the output terminal To, and is also connected through the output capacitor **9** to a reference potential. The one end of the sense resistor **10** (the end thereof closer to the output coil **8**) is connected to the inverting input terminal (−) of the output current comparator **4**, and the other end of the sense resistor **10** (the end thereof closer to the output terminal To) is connected through the offset circuit **3** to the non-inverting input terminal (+) of the output current comparator **4**. Accordingly, the output current comparator **4** changes the output level thereof according to whether or not the voltage Vs (including the offset produced by the offset circuit **3**) across the sense resistor **10**, which varies with the output current Io, is higher than a predetermined threshold level.

When the reset signal to the S-R flip-flop **5** is low and the set signal thereto is high, the driver **6** turns the FET **7***a* on and the FET **7***b* off. On the other hand, when the reset signal to the S-R flip-flop **5** is low and the set signal thereto is low, the driver **6** turns the FET **7***a* off and the FET **7***b* on. Incidentally, when the reset signal is high, the driver **6** turns the FET **7***a* off irrespective of the state of the set signal (the state of the FET **7***b* is indeterminate). In the configuration described above, when the voltage Vs across the sense resistor **10** reaches the predetermined threshold level, the reset signal to the S-R flip-flop **5** turns high, and thus the switching of the FET **7***a* is stopped.

Next, with reference to FIG. **2**, the internal configuration of the output voltage comparison circuit **2** and the offset circuit **3** will be described in detail. As described earlier, in this embodiment, the output voltage comparison circuit **2** is composed of an operational amplifier **2***a* and a CI controller **2***b*. The operational amplifier **2***a* is composed of pnp-type bipolar transistors P**1** and P**2**, npn-type bipolar transistors N**1** and N**2**, and a constant current source I**1**. The CI controller **2***b* is composed of pnp-type bipolar transistors P_3 to P**6**, npn-type bipolar transistors N_3 to N**6**, amplifiers A**1** and A**2**, and resistors R**1** to R_4. The offset circuit **3** is composed of pnp-type bipolar transistors P_7 and P**8**, constant current sources I**2** and I_3, and resistors R_5 and R**6**.

The emitters of the transistors P**1** and P**2** are connected together, and the node between them is connected through the constant current source I**1** to the supply voltage line. The collectors of the transistors P**1** and P**2** are connected to the collectors of the transistors N**1** and N**2**, respectively. The base of the transistor P_1, which serves as the non-inverting input terminal (+) of the operational amplifier **2***a*, is connected to the output terminal of the DAC **1** (not illustrated) so that the reference voltage Vref is applied thereto. The base of the transistor P**2**, which serves as the inverting input terminal (−) of the operational amplifier **2***a*, is connected through the resistor R**1** to the non-inverting input terminal (+) of the amplifier A**1**, and is also connected through the resistor R**2** to the output terminal To (not illustrated) of the power supply apparatus. The node between the collectors of the transistors P**2** and N**2**, which serves as the output terminal of the operational amplifier **2***a*, is connected to the non-inverting input terminal (+) of the amplifier A**1**. The emitters of the transistors N**1** and N**2** are connected together, and the node between them is grounded. The bases of the transistors N**1** and N**2** are connected together, and the node between them is connected to the collector of the transistor N**1**.

The output terminal of the amplifier A**1** is connected to the base of the transistor N_3. The emitter of the transistor N_3 is consented to the inverting input terminal (−) of the amplifier A**1**, and is also grounded through the resistor R_3. The collector of the transistor N_3 is connected to the collector of the transistor P_3. The emitters of the transistors P_3 and P_4 are connected together, and the node between them is connected to the supply voltage line. The bases of the transistors P_3 and P_4 are connected together, and the node between them is connected to the collector of the transistor P_3. The collector of the transistor P_4 is connected through the resistor R_5 to the collector of the transistor N**6**.

The emitters of the transistors N_5 and N**6** are connected together, and the node between them is grounded. The collector of the transistor N_5 is connected to the collector of the transistor P**6**. The bases of the transistors N_5 and N**6** are connected together, and the node between them is connected to the collector of the transistor N_5. The emitters of the transistors P_5 and P**6** are connected together, and the node between them is connected to the supply voltage line. The collector of the transistor P_5 is connected to the collector of the transistor N_4. The bases of the transistors P_5 and P**6** are connected together, and the node between them is connected to the collector of the transistor P_5. The emitter of the transistor N_4 is connected to the inverting input terminal (−) of the amplifier A**2**, and is also grounded through the resistor R_4. The base of the transistor N_4 is connected to the output terminal of the amplifier A**2**. The non-inverting input terminal (+) of the amplifier A**2** is connected to the output terminal of the DAC **1** (see FIG. **1**) so that the reference voltage Vref is applied thereto.

The two ends of the sense resistor **10** (see FIG. **1**) are connected to the bases of the transistors P_7 and P**8**, respectively. The collectors of the transistors P_7 and P**8** are both grounded. The emitter of the transistor P_7 is connected through the resistor R_5 and the constant current source I**2** to the supply voltage line. The node between the constant current source I**2** and the resistor R_5 is connected to the collector of the transistor P_4, and is also connected to the non-inverting input terminal (+) of the output current comparator **4**. The node between the resistor R_5 and the emitter of the transistor P_7 is connected to the collector of the transistor N**6**. The emitter of the transistor P8 is connected through the resistor R6 and the constant current source I_3 to the supply voltage line. The node between the constant current source I_3 and the resistor R6 is connected to the inverting input terminal (−) of the output current comparator **4**.

In the output voltage comparison circuit **2** configured as described above, as the output current lo increases and accordingly the collector current i**1** of the transistor P_4 increases, the inverting input voltage to the amplifier A**1** provided in the CI controller **2***b* increases, and accordingly the non-inverting input voltage to the amplifier A**1** (i.e., the output voltage Vb of the operational amplifier **2***a*) increases. Thus, a voltage difference ΔV commensurate with an increase or decrease in the output current Io appears across the resistor R**1** between the inverting input voltage Va to the operational amplifier **2***a* and the output voltage Vb.

At this time, the operational amplifier **2***a* so operates as to make the inverting input voltage Va and the non-inverting input voltage (i.e., the reference voltage Vref) equal. This causes the current that flows from the resistor R**1** to the resistor R**2** to increase, and thus makes the output voltage Vo lower than the reference voltage Vref by a predetermined level (ΔV/R**1**×R**2**) (see FIG. **3**A). That is, in the power supply apparatus of this embodiment, even in the event of an abrupt change in the output current Io, the output voltage Vo shifts to a voltage commensurate with the output current Io and is then kept at that voltage (see FIG. **3**B). This eliminates the likeliness of a large variation appearing in the output voltage Vo, and thus helps enhance the transient characteristic of the output voltage Vo against an abrupt variation in the output current Io. Moreover, in the power supply apparatus of this embodiment, the output voltage Vo is reduced according to the increase in the output current Io. This helps reduce the power consumed when the output current Io increases.

Configured as described above, the power supply apparatus of this embodiment so operates that, as the output current Io increases, the output voltage Vo is reduced within a predetermined permissible variation range, and this can be achieved without requiring any offset to be produced in the input voltages themselves to the operational amplifier **2***a*. This permits the difference between the input voltages to the operational amplifier **2***a* to be set small. In other words, it is possible to use as the operational amplifier **2***a* one close to an ideal operational amplifier that receives equal potentials as the input voltages thereto. This configuration helps obtain a high gain in the operational amplifier **2***a*, and thus helps increase the response of the feedback loop and thereby enhance the transient characteristic of the output voltage Vo against an abrupt variation in the output current Io.

In the power supply apparatus of this embodiment, the DC characteristic (see FIG. **3**A) of the output voltage Vo with respect to the output current Io can be set simply by appropriately setting the ratio between the resistances of the resistors R**1** and R**2**, and does not depend on the gain characteristic of the operational amplifier **2***a*. Thus, there are very few factors that cause the output voltage Vo to vary. Accordingly, with the power supply apparatus of this embodiment, even when the permissible variation range of the output voltage Vo is narrow (for example, ±50 [mV]), the output voltage Vo can be controlled accurately to vary within the permissible variation range.

Moreover, in the power supply apparatus of this embodiment, used as the current setting reference voltage (corresponding to the output voltage Vb of the operational amplifier **2***a* as obtained when the collector currents i**1** and i**2** of the transistors P_4 and N6 are equal and a current setting signal Si is zero; see FIG. **4**) that determines the correlation between the output voltage Vb of the operational amplifier **2***a* (i.e., the output current Io) and the current setting signal Si (=i**1**+i**2**) is the reference voltage Vref (or a voltage produced from the reference voltage Vref), which determines the output voltage Vo. With this configuration, even if a variation occurs in the reference voltage Vref, it has no influence whatsoever on the correlation characteristic of the current setting signal Si with respect to the output current Io. This configuration is particularly suitable for a power supply apparatus, like that of this embodiment, where the reference voltage Vref is controlled to vary.

The embodiment described above deals with a case where the present invention is applied to a switching regulator. It should be understood, however, that the present invention can be applied to any other configuration, for example, a series regulator having an FET **7***c* connected in series between an input and an output terminal as shown in FIG. **5**.

Instead of the output voltage comparison circuit **2** described above, an output voltage comparison circuit **2'** as shown in FIG. **6** may be used. This output voltage comparison circuit **2'** is composed of an output voltage comparison amplifier **11** that amplifies the differential voltage between a first reference voltage Vref**1** and the output voltage Vo, resistors **12** and **13** that are connected in series between a previously set second reference voltage Vref**2** and the ground potential GND so as to bias the voltage amplified by the output voltage comparison amplifier **11**, and a voltage-to-current conversion circuit **14** that converts the amplified and then biased voltage into a current to produce a current setting signal Si. Here, by lowering the output gain of the output voltage comparison amplifier **11** according to the second reference voltage Vref**2** and the resistances of the bias resistors **12** and **13**, a difference commensurate with a variation in the current setting signal Si is produced between the first reference voltage Vref**1** and the output voltage Vo. With this configuration, it is possible to obtain almost the same advantages as those achieved in the first and second embodiments described earlier.

It should be noted here that the power supply apparatus configured as described above, while having the advantage that it can be realized with a simpler configuration than in the first and second embodiments, has the following disadvantages: (a) a wide voltage range needs to be secured for the inputs to the output voltage comparison amplifier **11**; (b) the resistances of the resistors R**1** and R**2** need to be set with consideration given both to their ratio (the mid-point voltage) and to their absolute values, and thus variations in those resistances have a great influence; (c) variations in the gain characteristic of the output voltage comparison amplifier **11** have a great influence, and the output voltage comparison amplifier **11** has a poor temperature characteristic; and (d) the gain of the output voltage comparison amplifier **11** needs to be set low, and thus the output voltage comparison amplifier **11** shows a poor high-speed response. Accordingly, due caution needs to be exercised when this configuration is adopted. For example, in a case where power is supplied to a load that permits the input voltage thereto to vary only within a narrow variation range, the power supply apparatus of the first or second embodiment is more suitable than the power supply apparatus of this embodiment.

The descriptions above deal only with cases where the output current of the output voltage comparison circuit **2** is converted into a voltage by the offset circuit **3**. It is, however, possible to adopt any other configuration. For example, it is possible to use a digital signal as the current setting signal Si.

As described above, according to the present invention, in a power supply apparatus, to produce from an input voltage an output voltage within a predetermined permitted variation range, the target voltage of the output voltage is so controlled as to be reduced within the permissible variation range as the out current increases. More specifically, according to the present invention, a power supply apparatus is provided with: an output current detector that produces a monitoring voltage commensurate with the output current; a comparator that changes the output level thereof according to whether or not the monitoring voltage is higher than a predetermined threshold level; an output controller that controls the output voltage based on the output signal from the comparator; an offsetter that gives the monitoring voltage an offset; and an output voltage comparator that controls the magnitude of the offset according to the result of comparison between the output voltage and a predetermined reference voltage. Here, the output voltage comparator, in producing from the input voltage the output voltage within a predetermined permissible variation range, controls the magnitude of the offset in such a way that, as the output current increases, the output voltage decreases within the permissible variation range. This configuration helps enhance the transient characteristic of the output voltage against an abrupt variation in the output current and simultaneously reduce the power consumed when the output current increases.

In the power supply apparatus configured as described above, advisably, the output voltage comparator includes: an operational amplifier that operates so as to make the output voltage and the reference voltage equal; and a constant-impedance controller that controls the magnitude of the offset according to the output terminal voltage of the operational amplifier and that produces a signal by which the target level of the output voltage is reduced within the permissible variation range as the output current increases. With this configuration, the power supply apparatus so operates that, as the output current increases, the output voltage is reduced within the predetermined permissible variation range, and this can be achieved without requiring any offset to be produced in the input voltages themselves to the operational amplifier. This permits the difference between the input voltages to the operational amplifier to be set small. Thus, it is possible to use as the operational amplifier one close to an ideal operational amplifier that receives equal potentials as the input voltages thereto. This helps obtain a high gain in the operational amplifier, and thus helps increase the response of the feedback loop and thereby enhance the transient characteristic of the output voltage against an abrupt variation in the output current.

In the power supply apparatus configured as described above, advisably, the constant-impedance controller includes: a first resistor connected between one input terminal of the operational amplifier to which the output voltage is applied and the output terminal of the operational amplifier; and a second resistor connected between the one input terminal of the operational amplifier to which the output voltage is applied and the terminal to which the output voltage is applied. Here, by producing a voltage difference commensurate with an increase or decrease in the output current across the first resistor between the voltage at the one input terminal of the operational amplifier and the voltage at the output terminal thereof, the current that flows from the first resistor to the second resistor is varied. With this configuration, the DC characteristic of the output voltage with respect to the output current can be set simply by appropriately setting the ratio between the resistances of the first and second resistors, and does not depend on the gain characteristic of the operational amplifier. Thus, there are very few factors that cause the output voltage to vary. Thus, even when the permissible variation range of the output voltage is narrow, the output voltage can be controlled accurately to vary within the permissible variation range.

In the power supply apparatus configured as described above, advisably, the constant-impedance controller uses the reference voltages as a current setting reference voltage with reference to which the constant-impedance controller determines the correlation between the voltage at the output terminal of the operational amplifier and the magnitude of the offset. With this configuration, even if a variation occurs in the reference voltage, it has no influence whatsoever on the correlation characteristic of the magnitude of the offset with respect to the output current.

Alternatively, in the power supply apparatus configured as described above, advisably, the output voltage comparator includes: an amplifier that amplifies the differential voltage between the output voltage and a first reference voltage; a pair of resistors that are serially connected between two different potentials so as to bias the voltage amplified by the amplifier; and a voltage-to-current converter that converts the amplified and then biased voltage into a current to produce a setting signal by which the magnitude of the offset is set. With this configuration, it is possible, with a simpler configuration, to obtain almost the same advantages as those achieved by the differently configured power supply apparatuses described above. The power supply apparatus of this configuration, however, also has many disadvantages as compared with the differently configured power supply apparatuses, and therefore due caution needs to be exercised when this configuration is adopted.

What is claimed is:

1. A power supply apparatus comprising:

an output current detector that produces a monitoring signal commensurate with an output current;

a comparator that changes an output level thereof according to whether or not the monitoring signal is higher than a predetermined threshold level;

an output controller that controls an output voltage based on an output signal from the comparator;

an offsetter that gives the monitoring signal an offset; and

an output voltage comparator that receives the output current and controls the offsetter such that, as the output current increases, the offset given by the offsetter increases and, as the output current decreases, the offset given by the offsetter decreases.

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