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Kreps

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(54) **METHOD FOR MAKING SEMICONDUCTOR DEVICE COMPRISING A SUPERLATTICE WITH UPPER PORTIONS EXTENDING ABOVE ADJACENT UPPER PORTIONS OF SOURCE AND DRAIN REGIONS**

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Related U.S. Application Data

(63) Continuation-in-part of application No. 10/647,069, filed on Aug. 22, 2003, now Pat. No. 6,897,472, which is a continuation-in-part of application No. 10/603,696, filed on Jun. 26, 2003, now abandoned, which is a continuation-in-part of application No. 10/603,621, filed on Jun. 26, 2003, now abandoned.

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/285**; 438/197

(58) **Field of Classification Search** 438/197, 438/285

See application file for complete search history.

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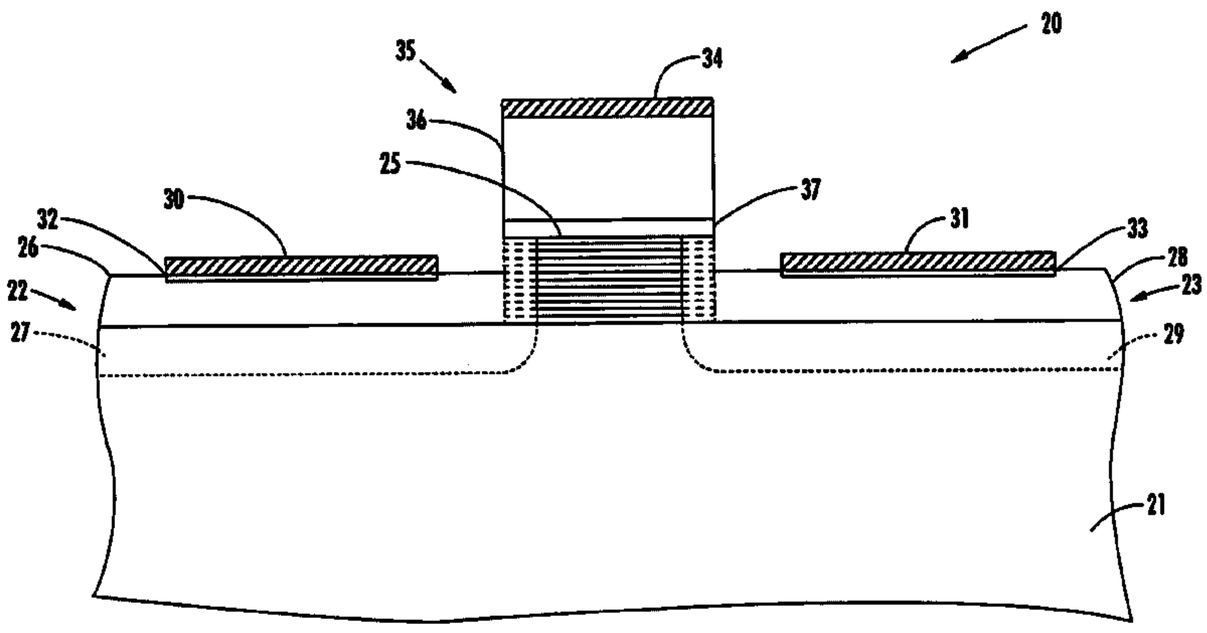
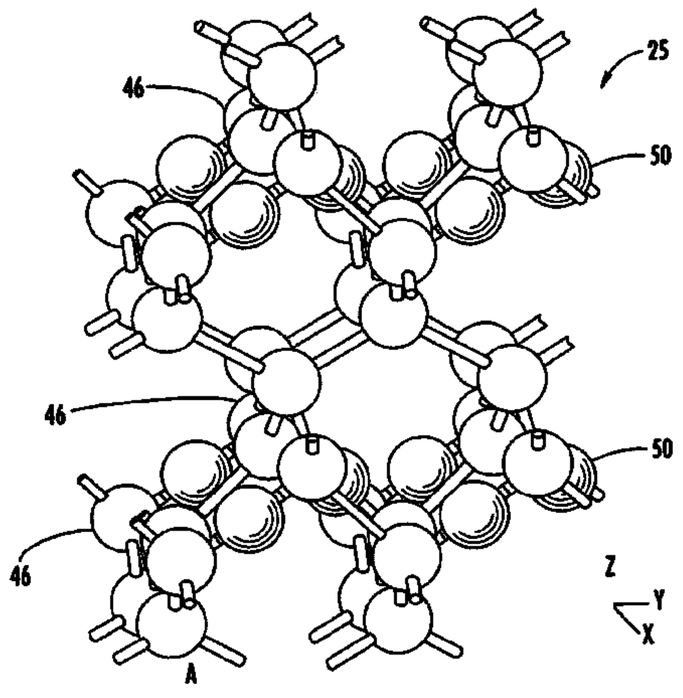
(57) **ABSTRACT**

A method for making a semiconductor device may include providing a semiconductor substrate and forming at least one MOSFET by forming spaced apart source and drain regions and a superlattice on the substrate so that the superlattice is between the source and drain regions. The superlattice may include a plurality of stacked groups of layers. The superlattice may have upper portions extending above adjacent upper portions of the source and drain regions, and lower portions contacting the source and drain regions so that a channel is defined in lower portions of the superlattice. Each group of layers of the superlattice may include a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. The energy-band modifying layer may include at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor. The method may further include forming a gate overlying the superlattice.

46 Claims, 14 Drawing Sheets





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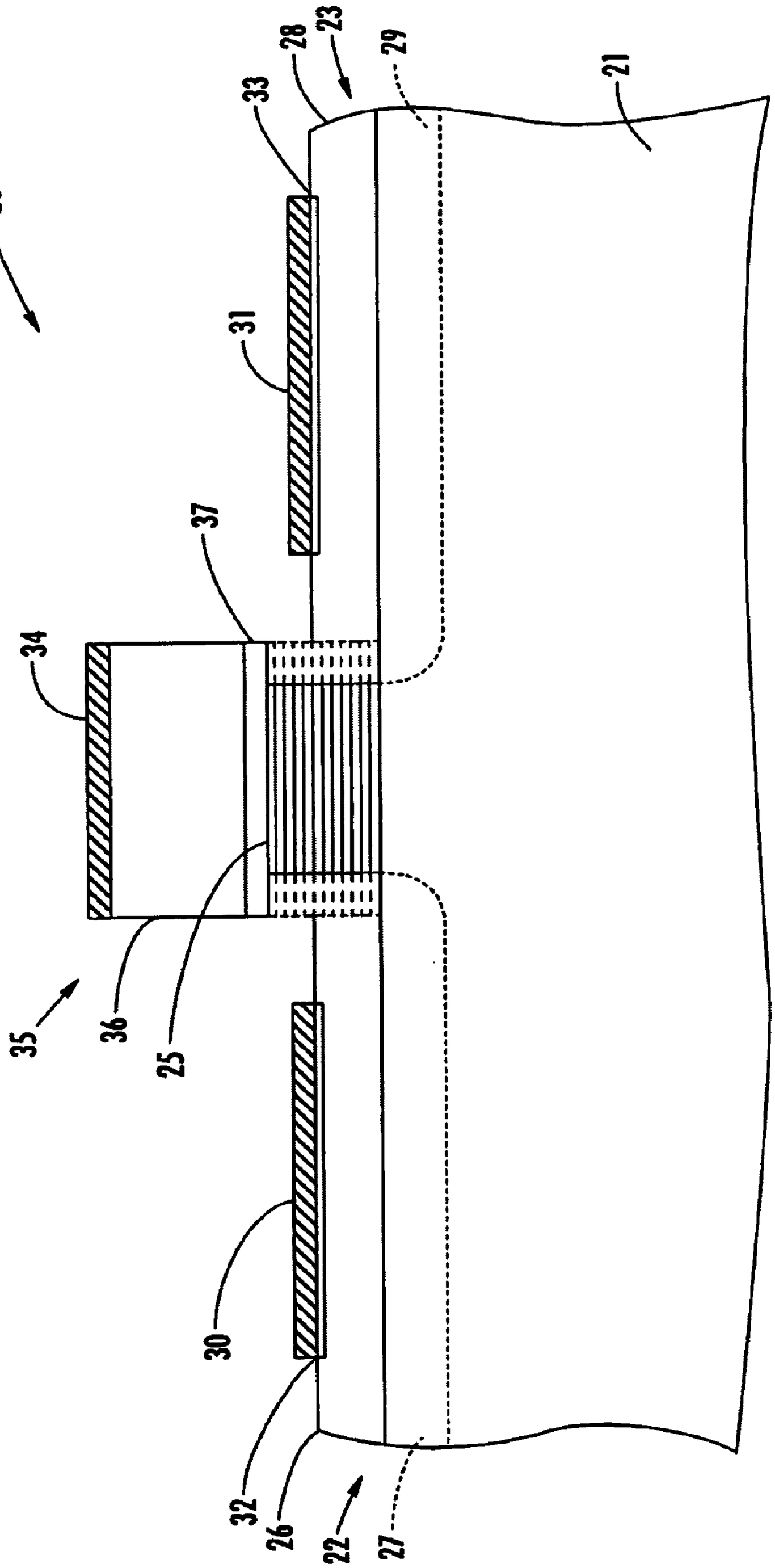

FIG. 1

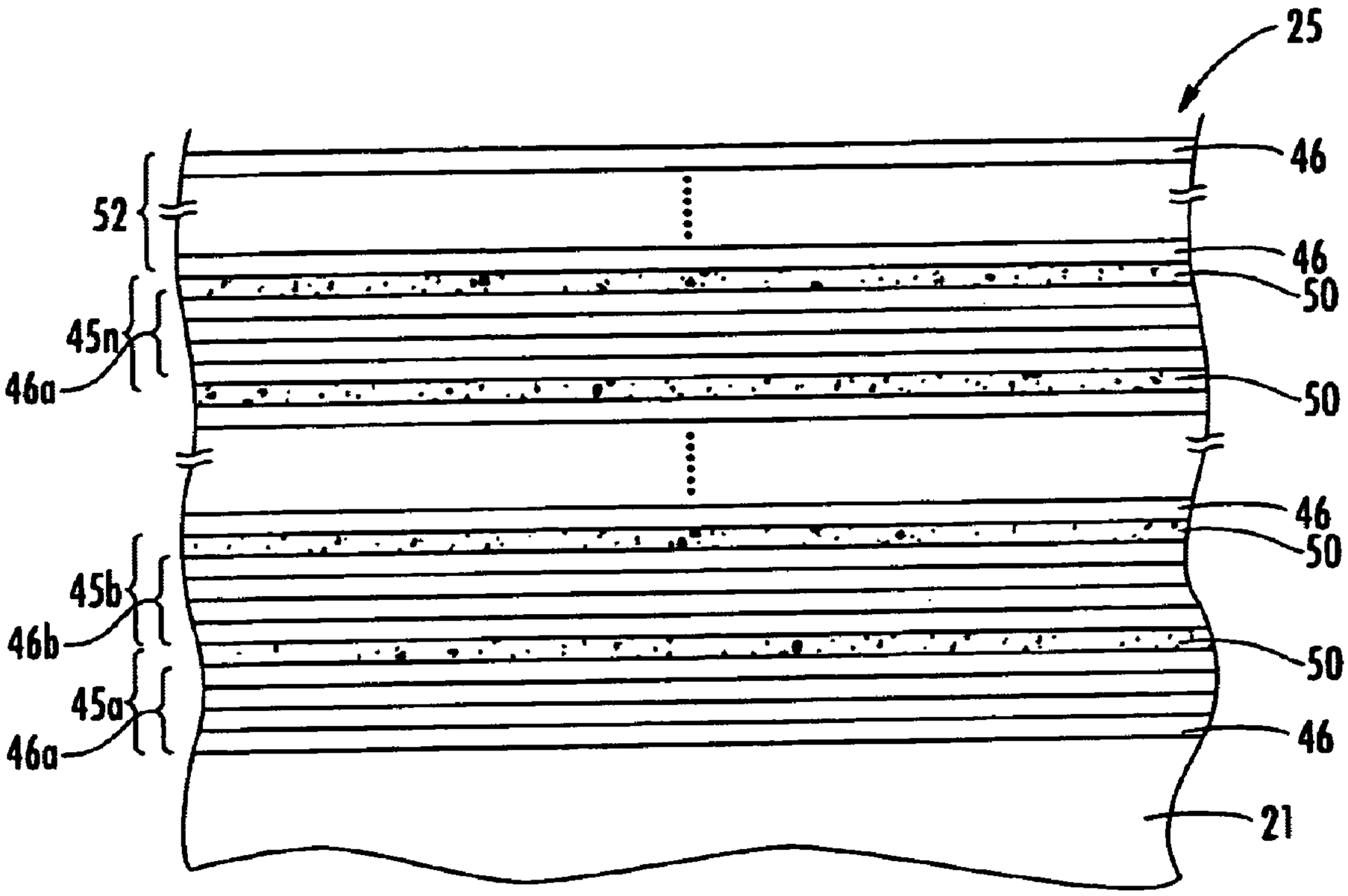

FIG. 2

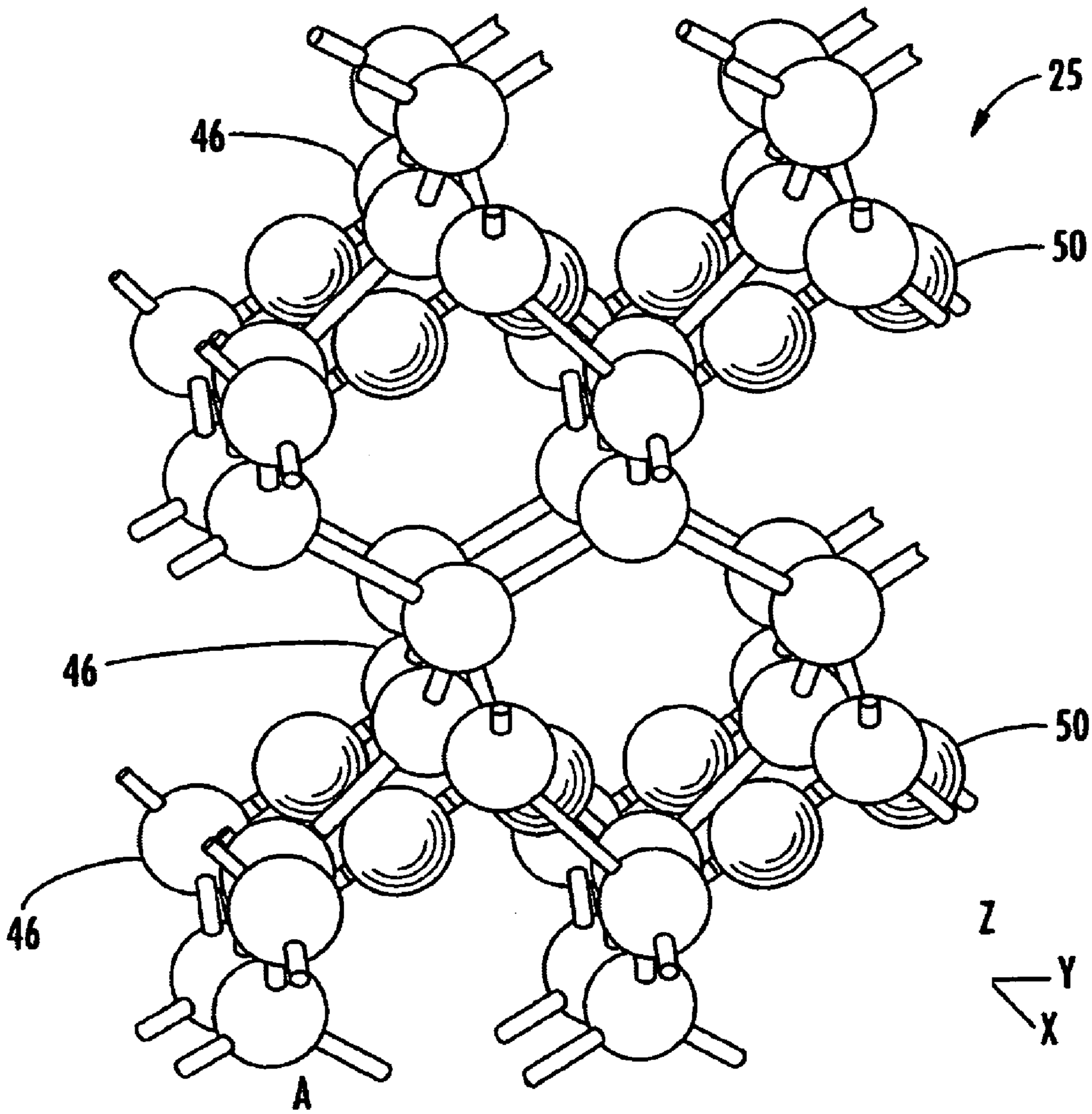

FIG. 3

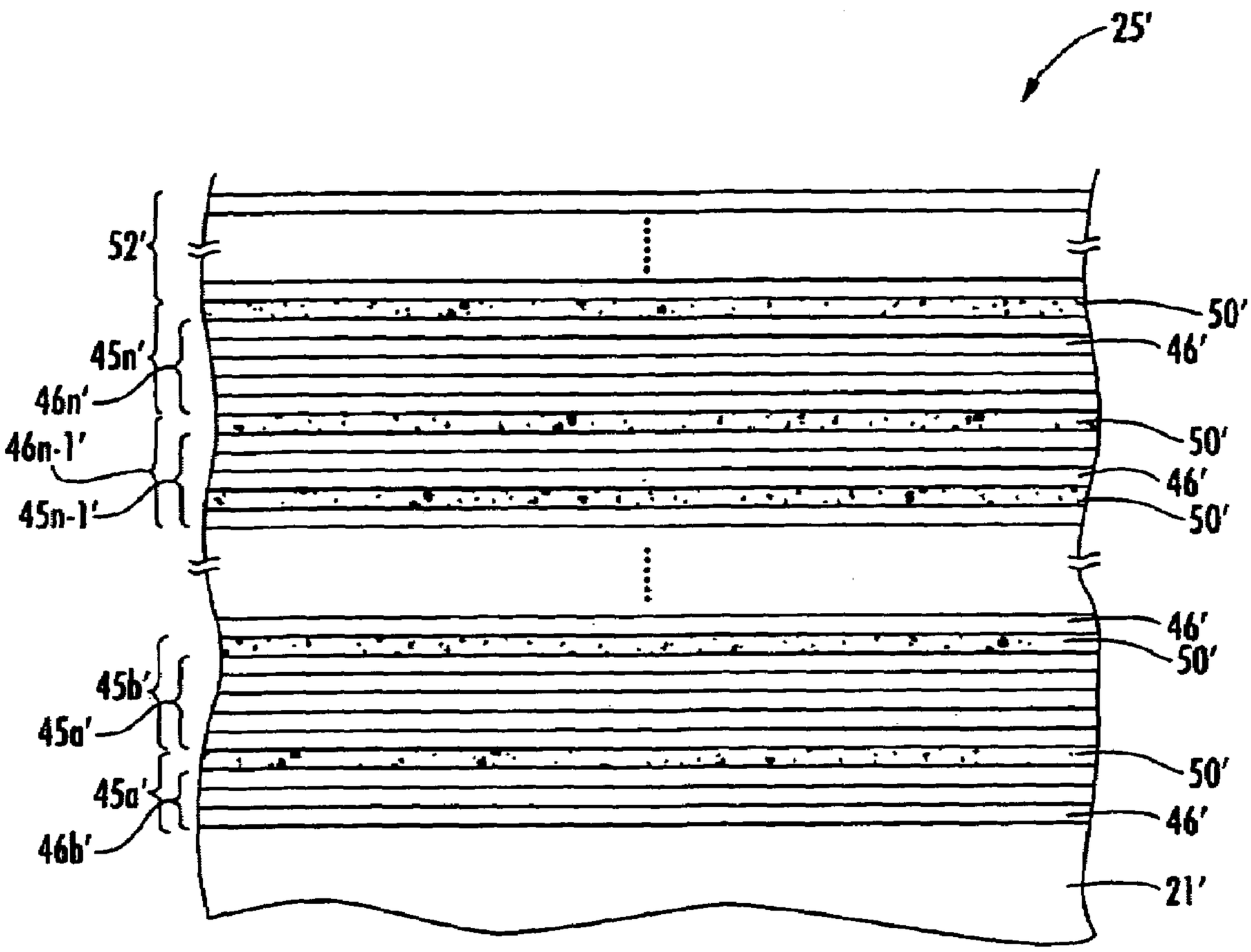
25'
52'
45n'
46n'
46n-1'
45n-1'
45b'
45a'
45a'
46b'
50'
46'
50'
50'
46'
50'
46'
50'
50'
46'
21'

FIG. 4

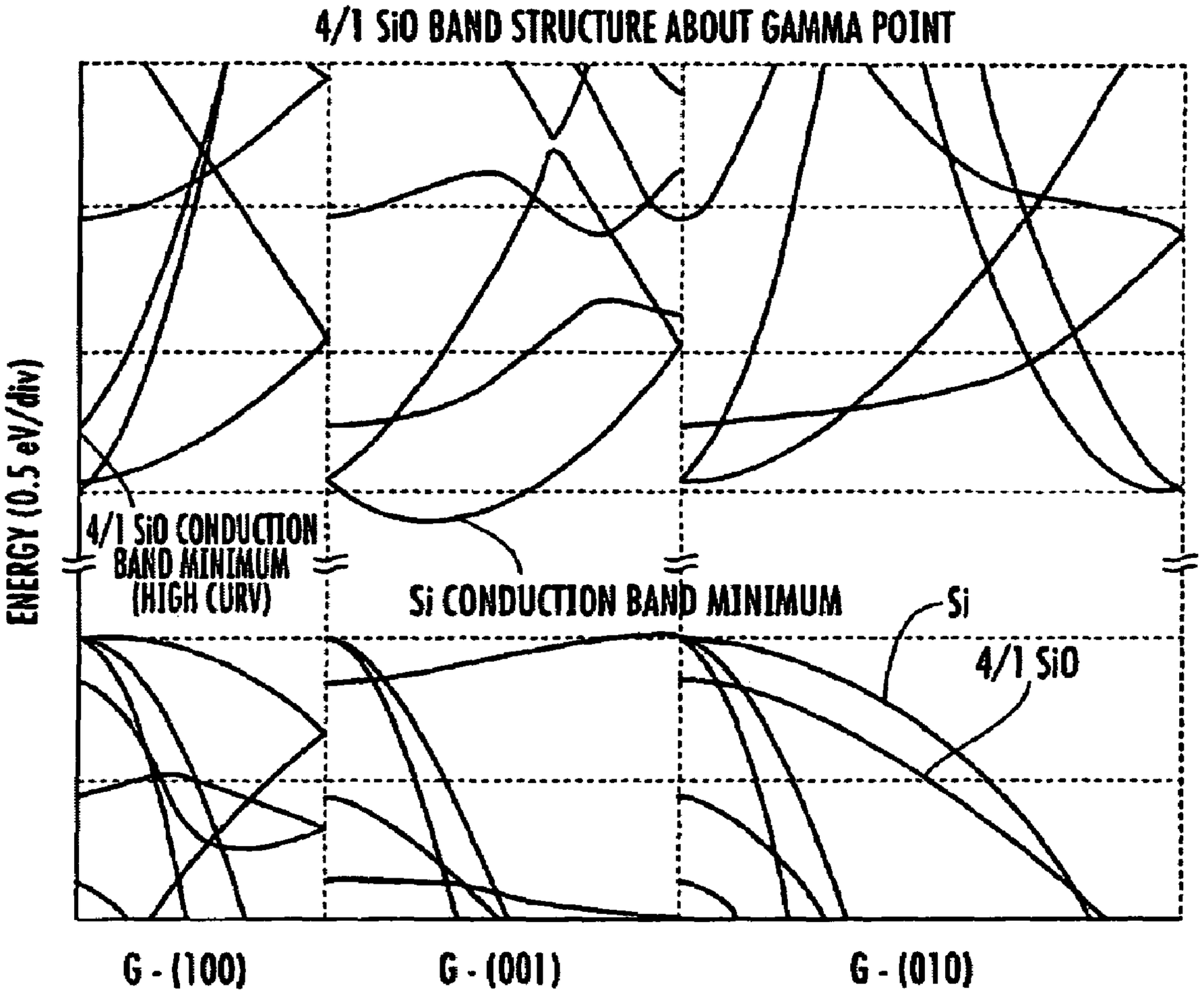
4/1 SiO BAND STRUCTURE ABOUT GAMMA POINT
ENERGY (0.5 eV/div)
4/1 SiO CONDUCTION BAND MINIMUM (HIGH CURV)
Si CONDUCTION BAND MINIMUM
Si
4/1 SiO
G - (100)
G - (001)
G - (010)

FIG. 5A

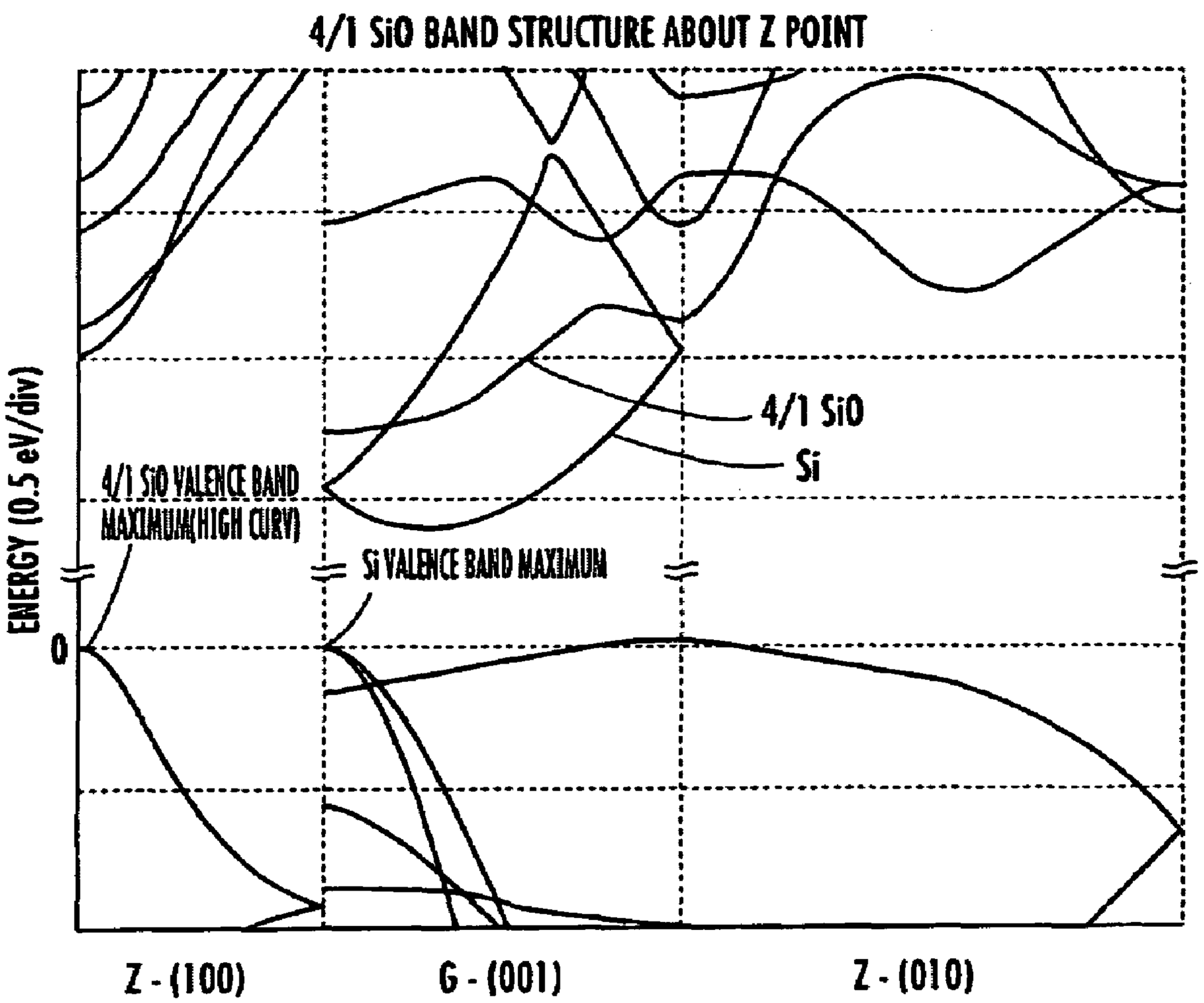
4/1 SiO BAND STRUCTURE ABOUT Z POINT
ENERGY (0.5 eV/div)
0
4/1 SiO
Si
4/1 SiO VALENCE BAND MAXIMUM(HIGH CURV)
Si VALENCE BAND MAXIMUM
Z - (100)
G - (001)
Z - (010)

FIG. 5B

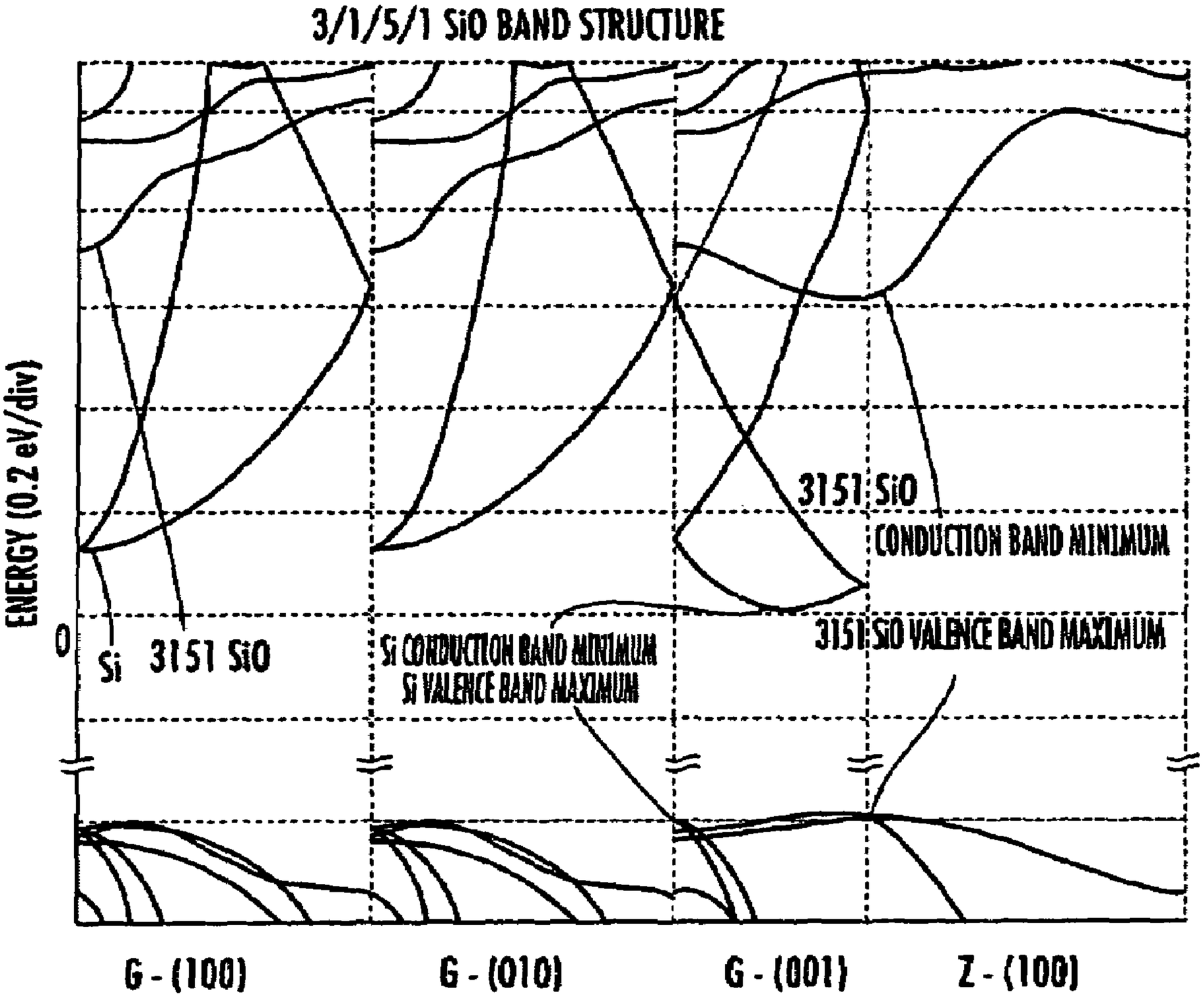
3/1/5/1 SiO BAND STRUCTURE
ENERGY (0.2 eV/div)
0
Si
3151 SiO
Si CONDUCTION BAND MINIMUM
Si VALENCE BAND MAXIMUM
3151 SiO
CONDUCTION BAND MINIMUM
3151 SiO VALENCE BAND MAXIMUM
G - (100)
G - (010)
G - (001)
Z - (100)

FIG. 5C

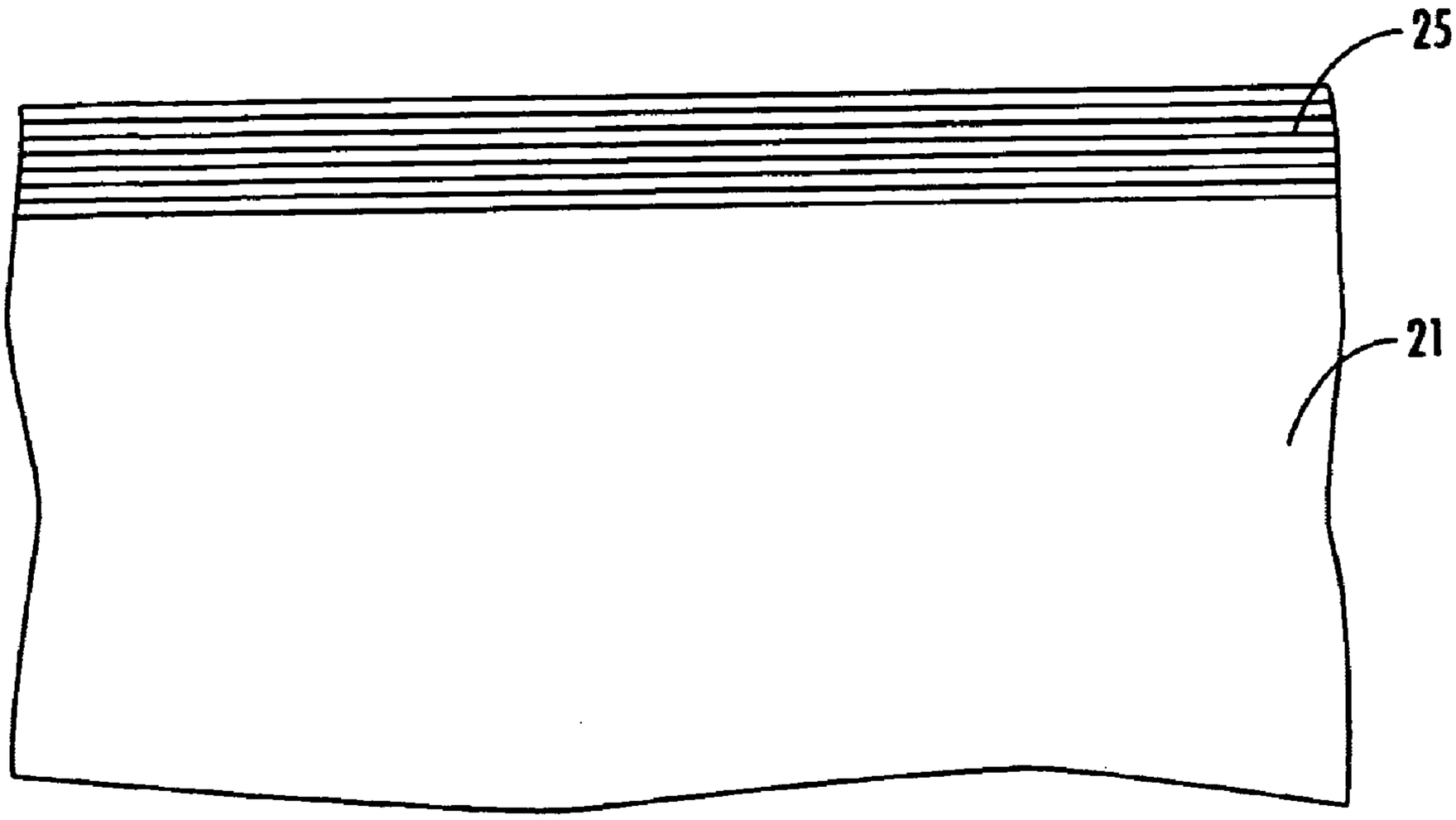

FIG. 6A

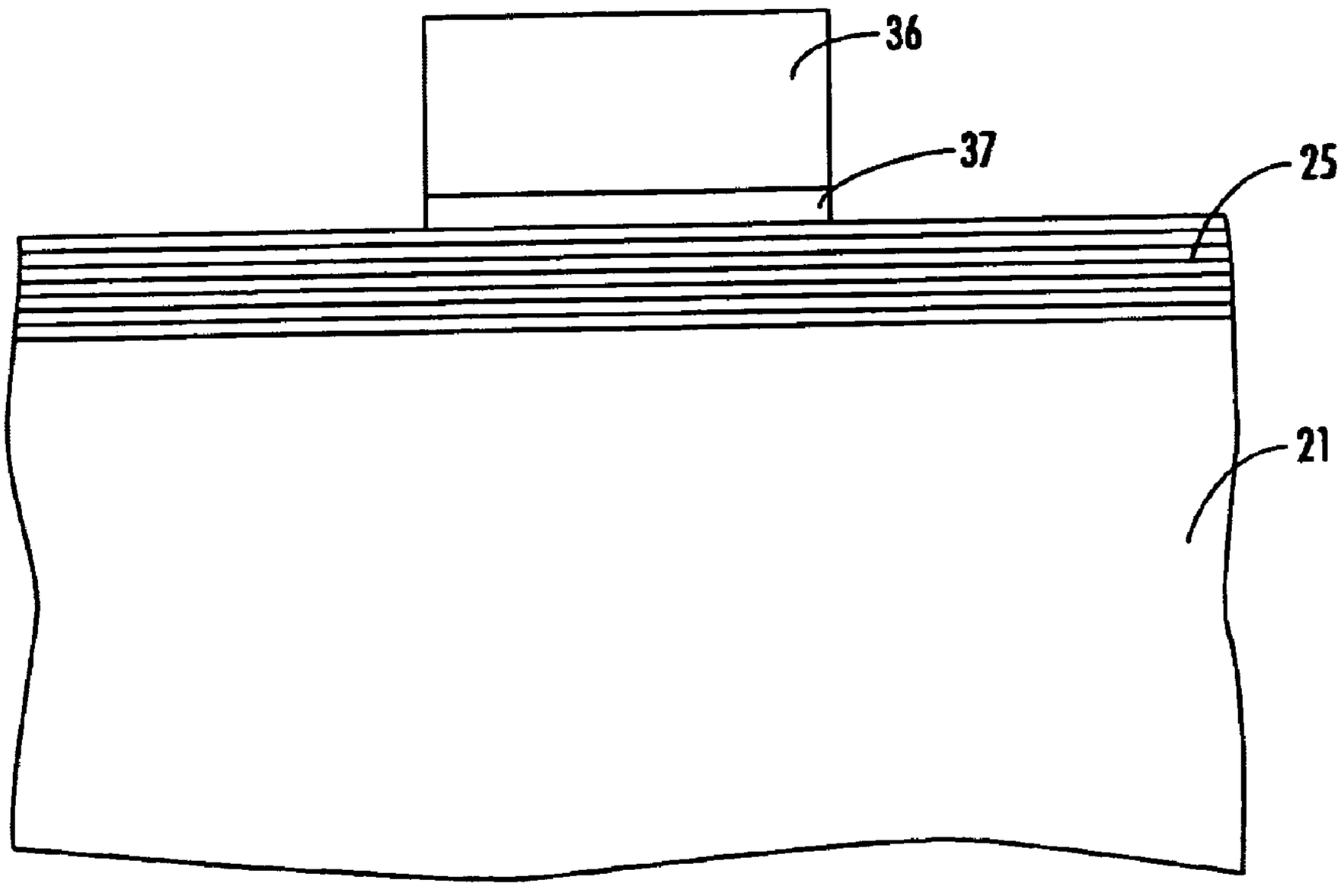

FIG. 6B

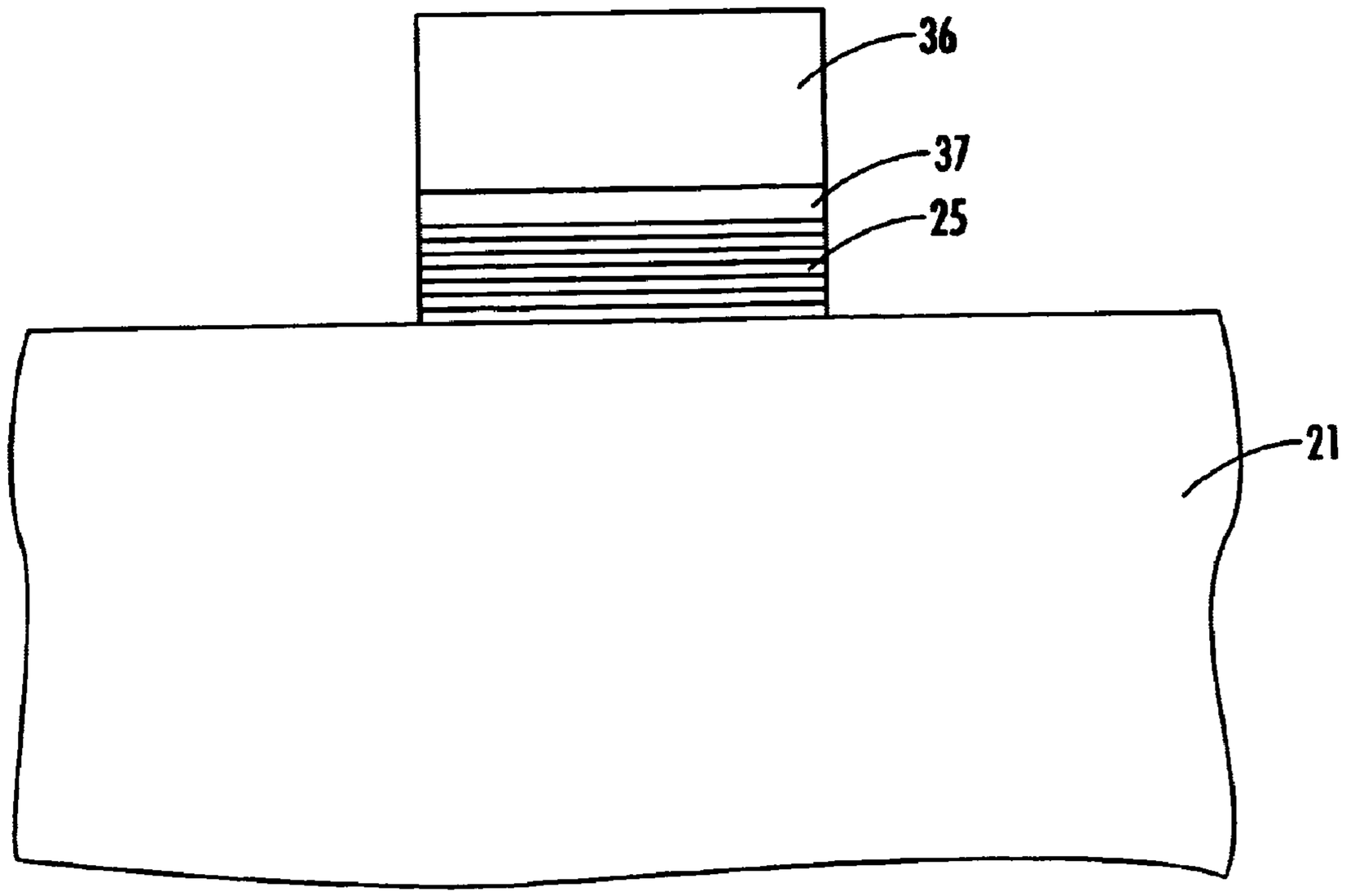

FIG. 6C

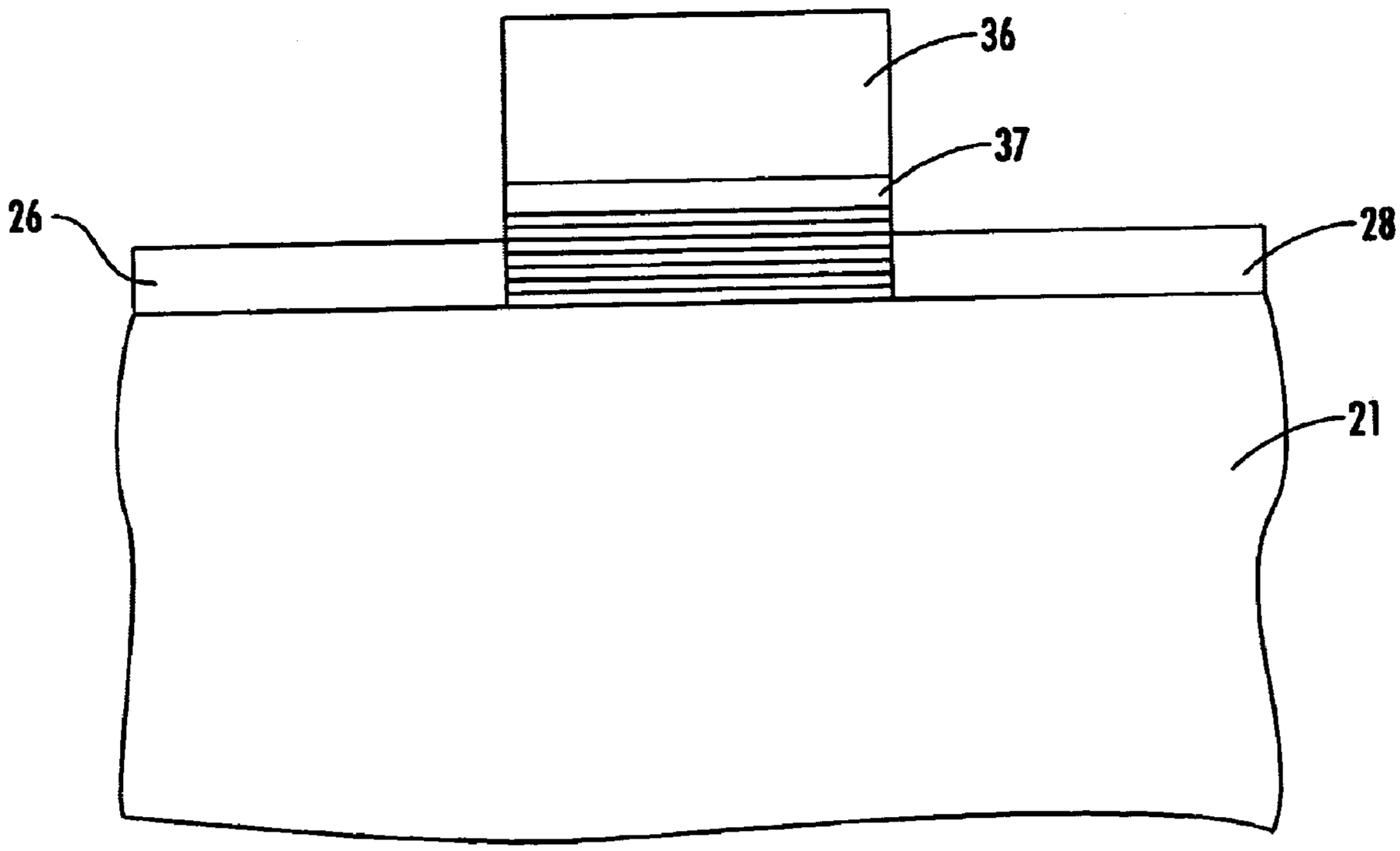

FIG. 6D

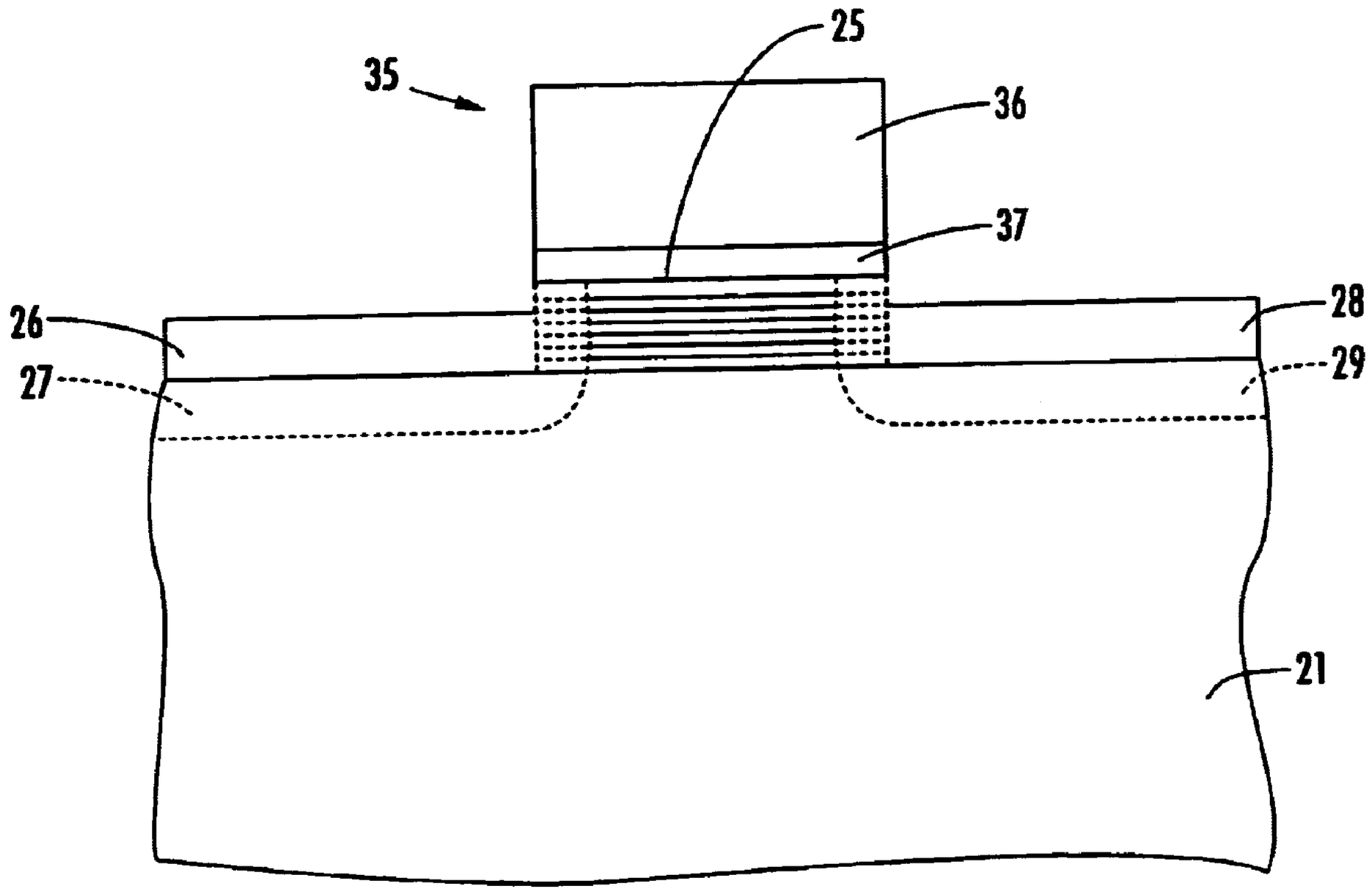

FIG. 6E

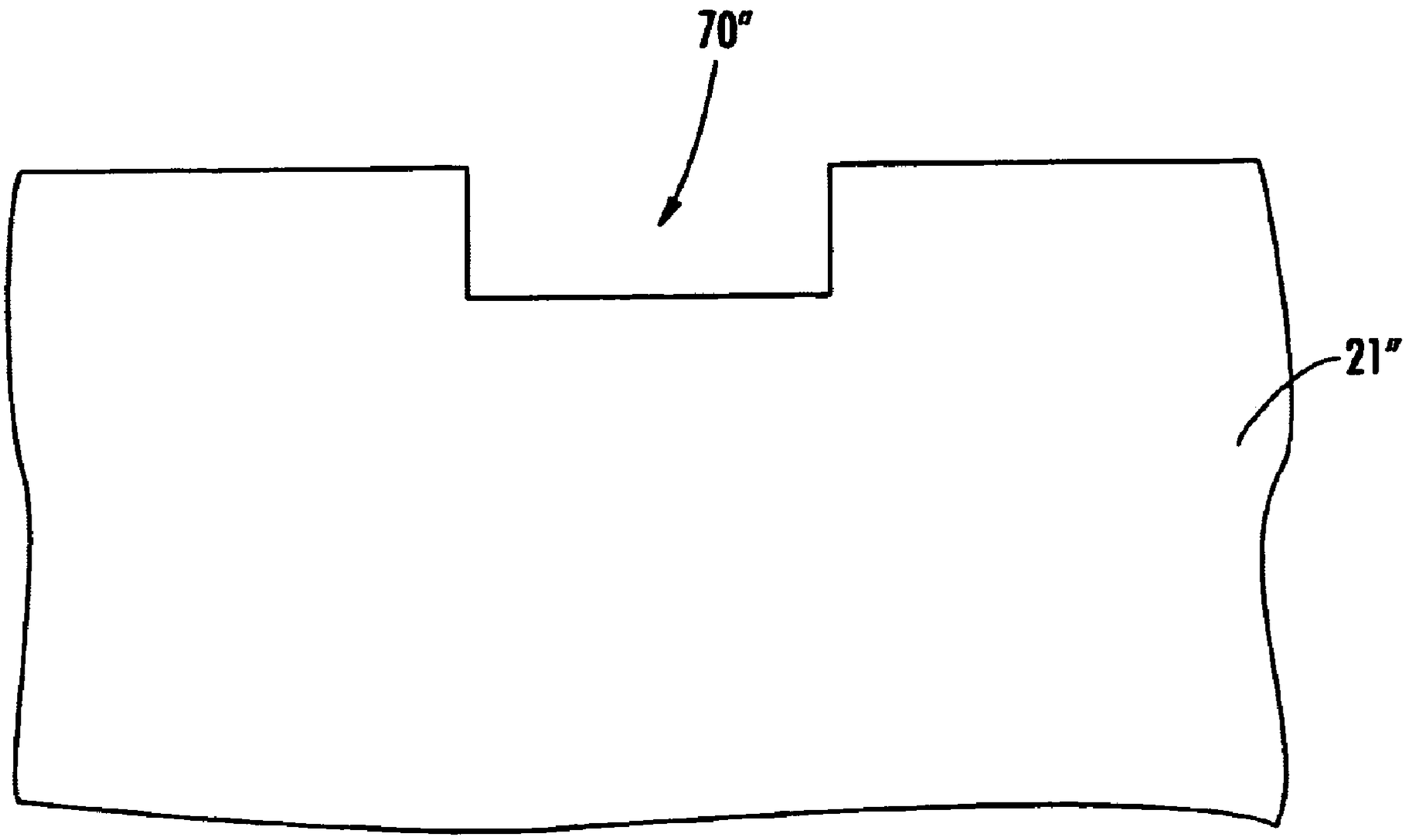

FIG. 7A

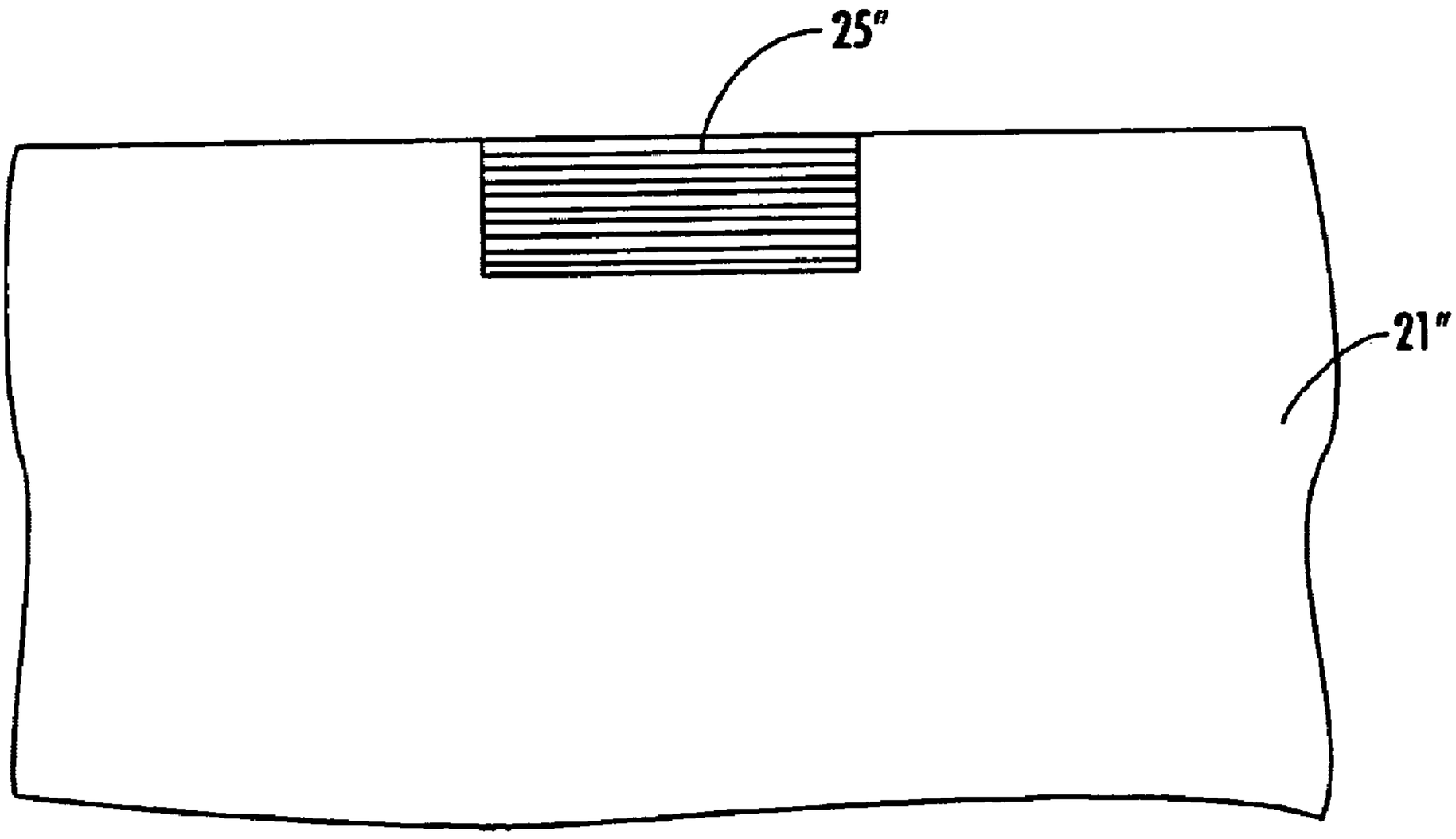

FIG. 7B

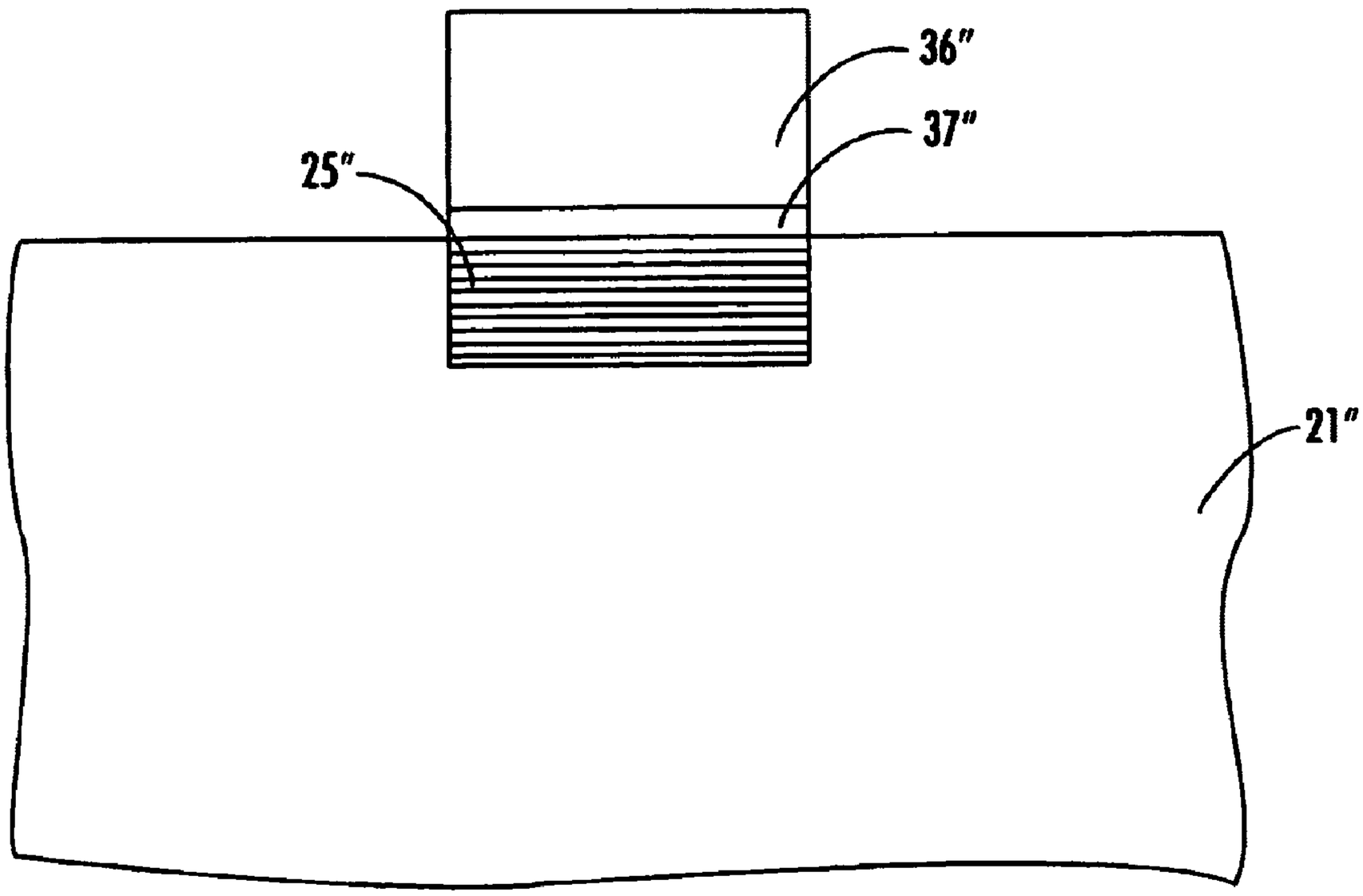

FIG. 7C

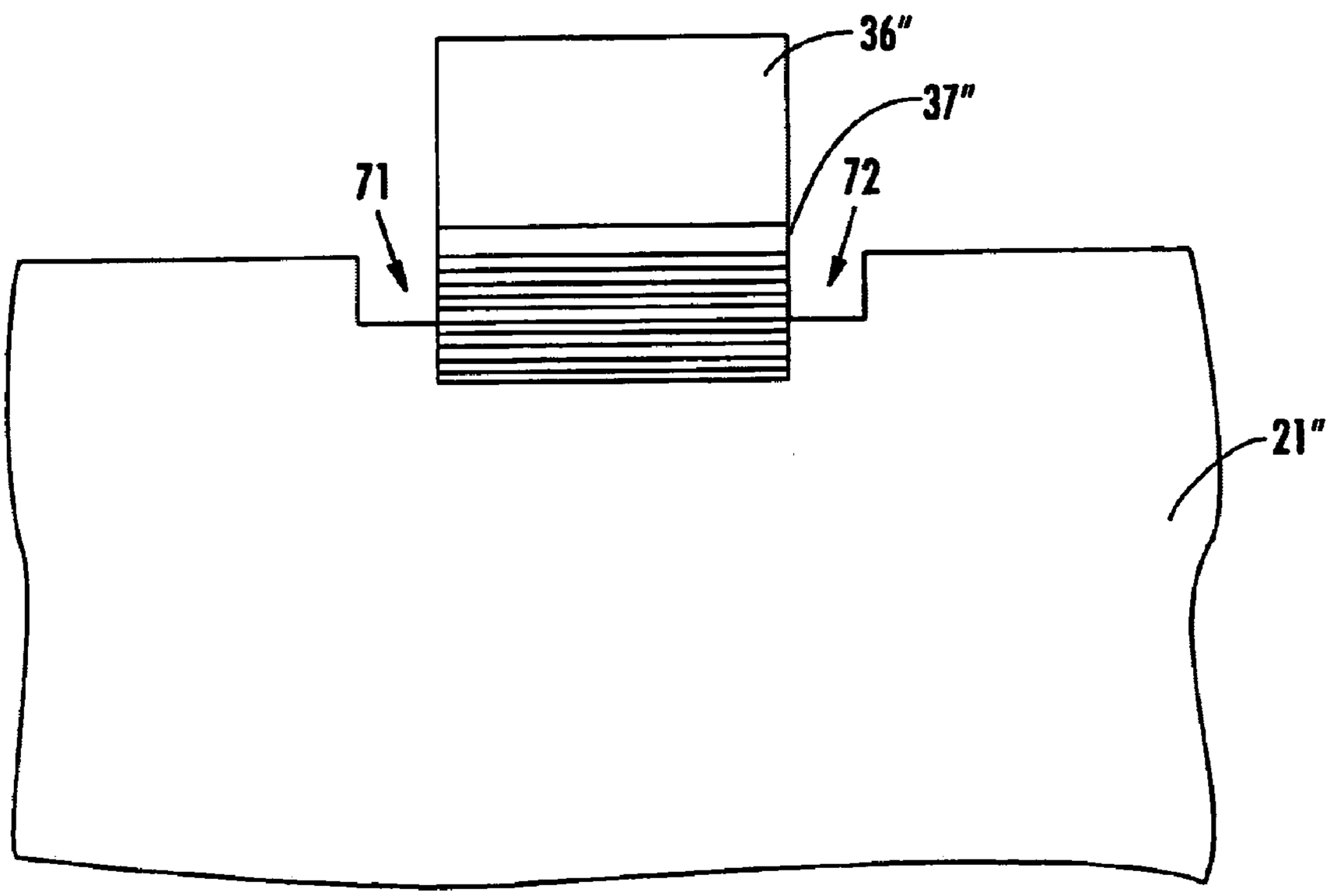

FIG. 7D

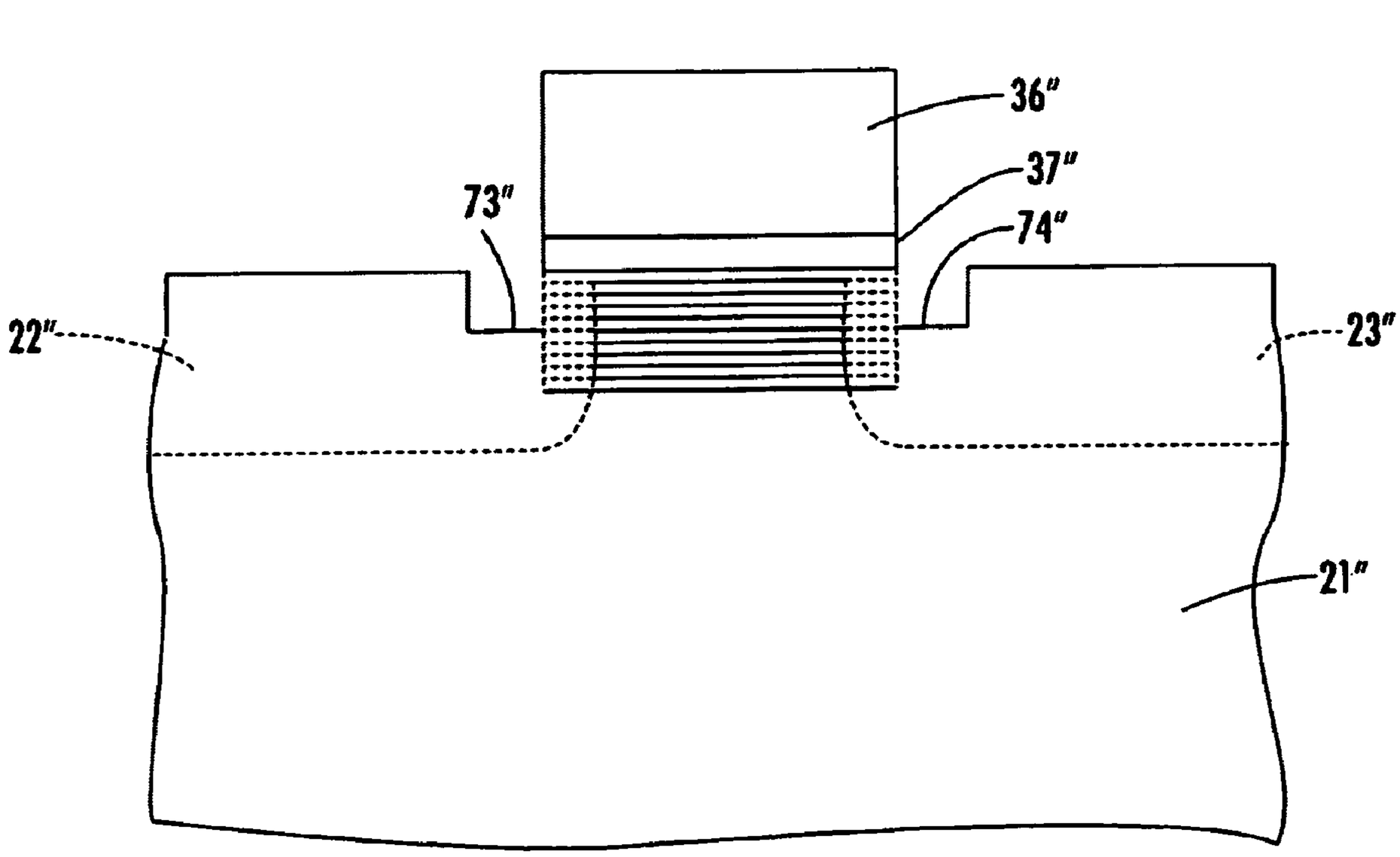

FIG. 7E

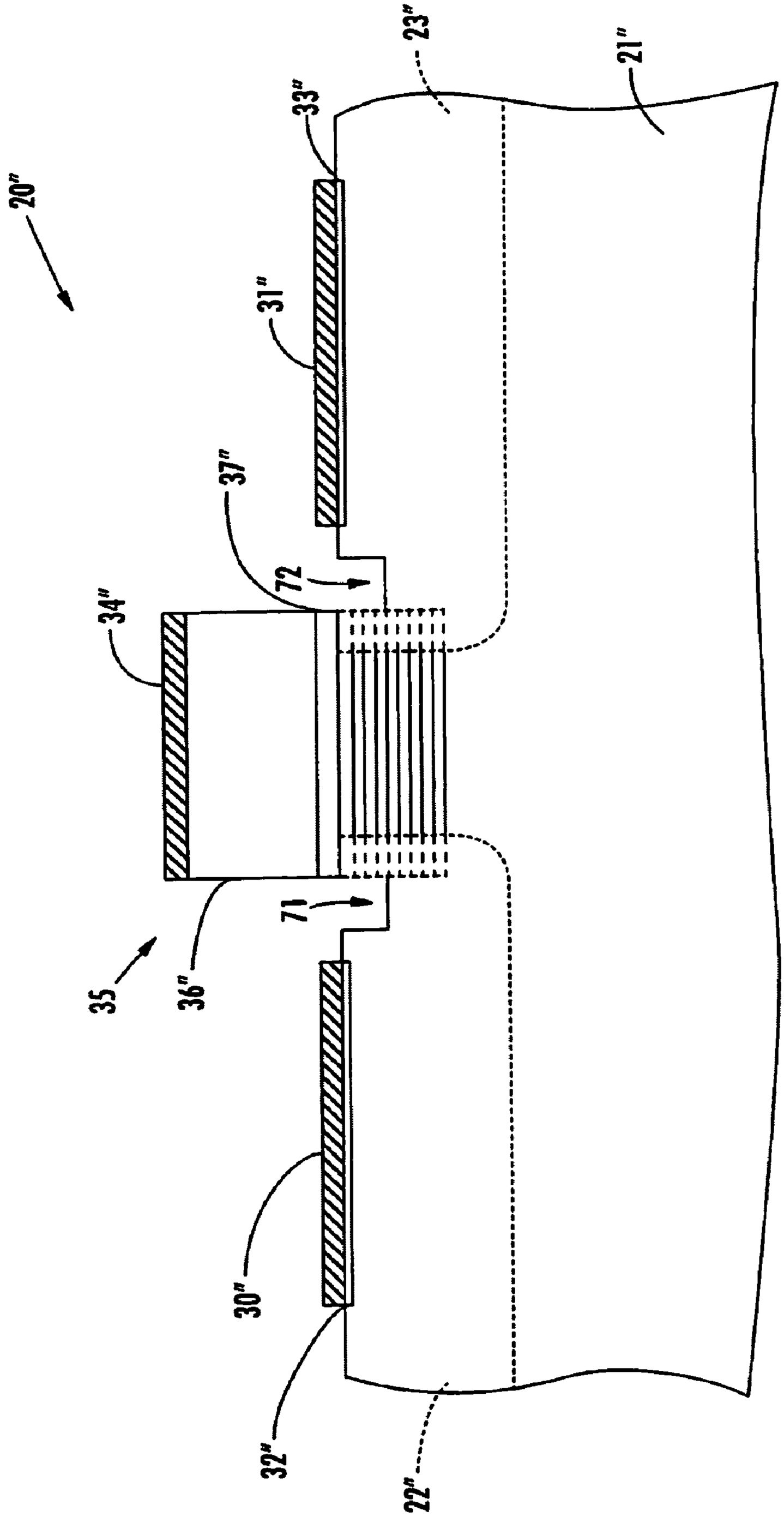

FIG. 8

METHOD FOR MAKING SEMICONDUCTOR DEVICE COMPRISING A SUPERLATTICE WITH UPPER PORTIONS EXTENDING ABOVE ADJACENT UPPER PORTIONS OF SOURCE AND DRAIN REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. patent application Ser. No. 10/647,069 filed Aug. 22, 2003, now U.S. Pat. No. 6,897,472 which in turn is a continuation-in-part of U.S. patent application Ser. Nos. 10/603,696 now abandoned and 10/603,621, now abandoned both filed on Jun. 26, 2003, the entire disclosures of which are hereby incorporated by reference herein.

FIELD OF THE INVENTION

The present invention relates to the field of semiconductors, and, more particularly, to semiconductors having enhanced properties based upon energy band engineering and associated methods.

BACKGROUND OF THE INVENTION

Structures and techniques have been proposed to enhance the performance of semiconductor devices, such as by enhancing the mobility of the charge carriers. For example, U.S. Patent Application No. 2003/0057416 to Currie et al. discloses strained material layers of silicon, silicon-germanium, and relaxed silicon and also including impurity-free zones that would otherwise cause performance degradation. The resulting biaxial strain in the upper silicon layer alters the carrier mobilities enabling higher speed and/or lower power devices. Published U.S. Patent Application No. 2003/0034529 to Fitzgerald et al. discloses a CMOS inverter also based upon similar strained silicon technology.

U.S. Pat. No. 6,472,685 B2 to Takagi discloses a semiconductor device including a silicon and carbon layer sandwiched between silicon layers so that the conduction band and valence band of the second silicon layer receive a tensile strain. Electrons having a smaller effective mass, and which have been induced by an electric field applied to the gate electrode, are confined in the second silicon layer, thus, an n-channel MOSFET is asserted to have a higher mobility.

U.S. Pat. No. 4,937,204 to Ishibashi et al. discloses a superlattice in which a plurality of layers, less than eight monolayers, and containing a fraction or a binary compound semiconductor layers, are alternately and epitaxially grown. The direction of main current flow is perpendicular to the layers of the superlattice.

U.S. Pat. No. 5,357,119 to Wang et al. discloses a Si—Ge short period superlattice with higher mobility achieved by reducing alloy scattering in the superlattice. Along these lines, U.S. Pat. No. 5,683,934 to Candelaria discloses an enhanced mobility MOSFET including a channel layer comprising an alloy of silicon and a second material substitutionally present in the silicon lattice at a percentage that places the channel layer under tensile stress.

U.S. Pat. No. 5,216,262 to Tsu discloses a quantum well structure comprising two barrier regions and a thin epitaxially grown semiconductor layer sandwiched between the barriers. Each barrier region consists of alternate layers of SiO_2/Si with a thickness generally in a range of two to six monolayers. A much thicker section of silicon is sandwiched between the barriers.

An article entitled "Phenomena in silicon nanostructure devices" also to Tsu and published online Sep. 6, 2000 by Applied Physics and Materials Science & Processing, pp. 391-402 discloses a semiconductor-atomic superlattice (SAS) of silicon and oxygen. The Si/O superlattice is disclosed as useful in a silicon quantum and light-emitting devices. In particular, a green electroluminescence diode structure was constructed and tested. Current flow in the diode structure is vertical, that is, perpendicular to the layers of the SAS. The disclosed SAS may include semiconductor layers separated by adsorbed species such as oxygen atoms, and CO molecules. The silicon growth beyond the adsorbed monolayer of oxygen is described as epitaxial with a fairly low defect density. One SAS structure included a 1.1 nm thick silicon portion that is about eight atomic layers of silicon, and another structure had twice this thickness of silicon. An article to Luo et al. entitled "Chemical Design of Direct-Gap Light-Emitting Silicon" published in Physical Review Letters, Vol. 89, No. 7 (Aug. 12, 2002) further discusses the light emitting SAS structures of Tsu.

Another example of an optical device incorporating a superlattice is disclosed in U.S. Pat. No. 6,566,679 to Nikonov et al. This patent discloses an integrated semiconductor optical modulator which includes a semiconductor substrate and associated integrated circuit element. The integrated circuit element includes a superlattice having alternating layers of the semiconductor material and an insulator. The semiconductor layers and insulator layers are configured to cause direct bandgap absorption of radiation energy in the semiconductor layers to modulate a radiation beam that passes through the superlattice structure.

Published International Application WO 02/103,767 A1 to Wang, Tsu and Lofgren, discloses a barrier building block of thin silicon and oxygen, carbon, nitrogen, phosphorous, antimony, arsenic or hydrogen to thereby reduce current flowing vertically through the lattice more than four orders of magnitude. The insulating layer/barrier layer allows for low defect epitaxial silicon to be deposited next to the insulating layer.

Published Great Britain Patent Application 2,347,520 to Mears et al. discloses that principles of Aperiodic Photonic Band-Gap (APBG) structures may be adapted for electronic bandgap engineering. In particular, the application discloses that material parameters, for example, the location of band minima, effective mass, etc, can be tailored to yield new aperiodic materials with desirable band-structure characteristics. Other parameters, such as electrical conductivity, thermal conductivity and dielectric permittivity or magnetic permeability are disclosed as also possible to be designed into the material.

Despite considerable efforts at materials engineering to increase the mobility of charge carriers in semiconductor devices, there is still a need for greater improvements. Greater mobility may increase device speed and/or reduce device power consumption. With greater mobility, device performance can also be maintained despite the continued shift to smaller device features.

SUMMARY OF THE INVENTION

In view of the foregoing background, it is therefore an object of the present invention to provide a method for making a semiconductor device including one or more MOSFETS having relatively high charge carrier mobility and related methods.

This and other objects, features, and advantages in accordance with the present invention are provided by a method

for making a semiconductor device which may include providing a semiconductor substrate and forming at least one metal oxide semiconductor field-effect transistor (MOSFET). More particularly, the MOSFET may be formed by forming spaced apart source and drain regions and a superlattice on the semiconductor substrate so that the superlattice is between the source and drain regions. The superlattice may include a plurality of stacked groups of layers. Further, the superlattice may have upper portions extending above adjacent upper portions of the source and drain regions, and lower portions contacting the source and drain regions so that a channel is defined in lower portions of the superlattice. Also, each group of layers of the superlattice may include a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon. The energy-band modifying layer may include at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor. The method may further include forming a gate overlying the superlattice.

More specifically, the source and drain regions may each include a respective epitaxial silicon layer, and the superlattice may have a greater thickness than the epitaxial silicon layers. Also, the source and drain regions may each have a respective trench therein adjacent the superlattice, and the upper portions of the superlattice may extend above bottom portions of the trenches. The gate may include an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer. Further, a contact layer may be on the source regions and/or the drain region.

Furthermore, the superlattice channel may have a common energy band structure therein, and it may also have a higher charge carrier mobility than would otherwise be present. Each base semiconductor portion may comprise silicon or germanium, for example, and each energy band-modifying layer may comprise oxygen. Further, each energy band-modifying layer may be a single monolayer thick, and each base semiconductor portion may be less than eight monolayers thick.

The superlattice may further have a substantially direct energy bandgap, and it may also include a base semiconductor cap layer on an uppermost group of layers. In one embodiment, all of the base semiconductor portions may be a same number of monolayers thick. In accordance with an alternate embodiment, at least some of the base semiconductor portions may be a different number of monolayers thick. In addition, each energy band-modifying layer may include a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is schematic cross-sectional view of a semiconductor device in accordance with the present invention.

FIG. **2** is a greatly enlarged schematic cross-sectional view of the superlattice as shown in FIG. **1**.

FIG. **3** is a perspective schematic atomic diagram of a portion of the superlattice shown in FIG. **1**.

FIG. **4** is a greatly enlarged schematic cross-sectional view of another embodiment of a superlattice that may be used in the device of FIG. **1**.

FIG. **5**A is a graph of the calculated band structure from the gamma point (G) for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. **1-3**.

FIG. **5**B is a graph of the calculated band structure from the Z point for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. **1-3**.

FIG. **5**C is a graph of the calculated band structure from both the gamma and Z points for both bulk silicon as in the prior art, and for the 5/1/3/1 Si/O superlattice as shown in FIG. **4**.

FIGS. **6**A-**6**E are a series of schematic cross-sectional diagrams illustrating a method for making the semiconductor device of FIG. **1**.

FIGS. **7**A-**7**E are a series of schematic cross-sectional diagrams illustrating a method for making an alternate embodiment of the semiconductor device of FIG. **1**.

FIG. **8** is a schematic cross-sectional diagram illustrating a completed semiconductor device formed using the method steps illustrated in FIGS. **7**A-**7**E.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout, and prime and multiple prime notation are used to indicate similar elements in alternate embodiments.

The present invention relates to controlling the properties of semiconductor materials at the atomic or molecular level to achieve improved performance within semiconductor devices. Further, the invention relates to the identification, creation, and use of improved materials for use in the conduction paths of semiconductor devices.

Applicants theorize, without wishing to be bound thereto, that certain superlattices as described herein reduce the effective mass of charge carriers and that this thereby leads to higher charge carrier mobility. Effective mass is described with various definitions in the literature. As a measure of the improvement in effective mass Applicants use a "conductivity reciprocal effective mass tensor", M_e^{-1} and M_h^{-1} for electrons and holes respectively, defined as:

$$M_{e,ij}^{-1}(E_F,T)=\frac{\sum_{E>E_F}\int_{B.Z.}(\nabla_k E(k,n))_i(\nabla_k E(k,n))_j\frac{\partial f(E(k,n),E_F,T)}{\partial E}d^3k}{\sum_{E>E_F}\int_{B.Z.}f(E(k,n),E_F,T)d^3k}$$

for electrons and:

$$M_{h,ij}^{-1}(E_F,T)=\frac{-\sum_{E<E_F}\int_{B.Z.}(\nabla_k E(k,n))_i(\nabla_k E(k,n))_j\frac{\partial f(E(k,n),E_F,T)}{\partial E}d^3k}{\sum_{E<E_F}\int_{B.Z.}(1-f(E(k,n),E_F,T)d^3k}$$

for holes, where f is the Fermi-Dirac distribution, E_F is the Fermi energy, T is the temperature, E(k,n) is the energy of

an electron in the state corresponding to wave vector k and the n^{th} energy band, the indices i and j refer to Cartesian coordinates x, y and z, the integrals are taken over the Brillouin zone (B.Z.), and the summations are taken over bands with energies above and below the Fermi energy for electrons and holes respectively.

Applicants' definition of the conductivity reciprocal effective mass tensor is such that a tensorial component of the conductivity of the material is greater for greater values of the corresponding component of the conductivity reciprocal effective mass tensor. Again Applicants theorize without wishing to be bound thereto that the superlattices described herein set the values of the conductivity reciprocal effective mass tensor so as to enhance the conductive properties of the material, such as typically for a preferred direction of charge carrier transport. The inverse of the appropriate tensor element is referred to as the conductivity effective mass. In other words, to characterize semiconductor material structures, the conductivity effective mass for electrons/holes as described above and calculated in the direction of intended carrier transport is used to distinguish improved materials.

Using the above-described measures, one can select materials having improved band structures for specific purposes. One such example would be a superlattice **25** material for a channel region in a semiconductor device. A planar MOSFET **20** including the superlattice **25** in accordance with the invention is now first described with reference to FIG. **1**. One skilled in the art, however, will appreciate that the materials identified herein could be used in many different types of semiconductor devices, such as discrete devices and/or integrated circuits.

The illustrated MOSFET **20** includes a substrate **21**, source and drain regions **22**, **23**, and the superlattice **25** is positioned between the source and drain regions. In the illustrated example, the source and drain regions **22**, **23** are raised source and drain regions in that they include respective epitaxial silicon layers **26**, **28** formed on the substrate **21** which are doped to the desired concentration. Moreover, the dopant may permeate portions **27**, **29** of the substrate **21** so that the source and drain regions **22**, **23** extend beneath the epitaxial layers **26**, **28**, respectively, and under the superlattice **25**, as shown.

The MOSFET **20** also illustratively includes a gate **35** comprising a gate insulating (e.g., oxide) layer **37** on the superlattice **25** and a gate electrode layer **36** on the gate insulating layer. Source/drain silicide layers **30**, **31** and source/drain contacts **32**, **33** overlie the source/drain regions, as will be appreciated by those skilled in the art.

In the illustrated embodiment, upper portions of the superlattice **25** extend above adjacent upper portions of the source and drain regions **22**, **23**, and, more particularly, the epitaxial layers **26**, **28**. Stated alternately, the superlattice **25** has a greater thickness than the epitaxial layers **26**, **28**, and thus upper sidewall portions of the superlattice do not contact the epitaxial layers. Yet, lower sidewall portions of the superlattice **25** do contact the source and drain regions **22**, **23** as shown so that a channel is defined in lower portions of the superlattice.

Accordingly, it will be appreciated by those skilled in the art that the channel only occupies the lower portion of the superlattice **25**, and thus current flow is reduced in the upper portions of the superlattice near the gate insulating layer **37**. This advantageously reduces hot carrier injection, for example, which may otherwise result in premature oxide breakdown and failure, as will be appreciated by those skilled in the art.

Applicants have identified improved materials or structures for the superlattice **25** of the MOSFET **20**. More specifically, the Applicants have identified materials or structures having energy band structures for which the appropriate conductivity effective masses for electrons and/or holes are substantially less than the corresponding values for silicon.

Referring now additionally to FIGS. **2** and **3**, the materials or structures are in the form of a superlattice **25** whose structure is controlled at the atomic or molecular level and may be formed using known techniques of atomic or molecular layer deposition. The superlattice **25** includes a plurality of layer groups **45***a*-**45***n* arranged in stacked relation, as perhaps best understood with specific reference to the schematic cross-sectional view of FIG. **2**.

Each group of layers **45***a*-**45***n* of the superlattice **25** illustratively includes a plurality of stacked base semiconductor monolayers **46** defining a respective base semiconductor portion **46***a*-**46***n* and an energy band-modifying layer **50** thereon. The energy band-modifying layers **50** are indicated by stippling in FIG. **2** for clarity of illustration.

The energy-band modifying layer **50** illustratively includes one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. In other embodiments, more than one such monolayer may be possible. It should be noted that reference herein to a non-semiconductor or semiconductor monolayer means that the material used for the monolayer would be a non-semiconductor or semiconductor if formed in bulk. That is, a single monolayer of a material, such as semiconductor, may not necessarily exhibit the same properties that it would if formed in bulk or in a relatively thick layer, as will be appreciated by those skilled in the art.

Applicants theorize without wishing to be bound thereto that the energy band-modifying layers **50** and adjacent base semiconductor portions **46***a*-**46***n* cause the superlattice **25** to have a lower appropriate conductivity effective mass for the charge carriers in the parallel layer direction than would otherwise be present. Considered another way, this parallel direction is orthogonal to the stacking direction. The band modifying layers **50** may also cause the superlattice **25** to have a common energy band structure.

It is also theorized that the semiconductor device, such as the illustrated MOSFET **20**, enjoys a higher charge carrier mobility based upon the lower conductivity effective mass than would otherwise be present. In some embodiments, and as a result of the band engineering achieved by the present invention, the superlattice **25** may further have a substantially direct energy bandgap that may be particularly advantageous for opto-electronic devices, for example, as described in further detail below.

As will be appreciated by those skilled in the art, the source/drain regions **22**, **23** and gate **35** of the MOSFET **20** may be considered as regions for causing the transport of charge carriers through the superlattice in a parallel direction relative to the layers of the stacked groups **45***a*-**45***n*. Other such regions are also contemplated by the present invention.

The superlattice **25** also illustratively includes a cap layer **52** on an upper layer group **45***n*. The cap layer **52** may comprise a plurality of base semiconductor monolayers **46**. The cap layer **52** may have between 2 to 100 monolayers of the base semiconductor, and, more preferably between 10 to 50 monolayers.

Each base semiconductor portion **46***a*-**46***n* may comprise a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors. Of course, the term Group IV

semiconductors also includes Group IV-IV semiconductors, as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example.

Each energy band-modifying layer **50** may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen, for example. The non-semiconductor is also desirably thermally stable through deposition of a next layer to thereby facilitate manufacturing. In other embodiments, the non-semiconductor may be another inorganic or organic element or compound that is compatible with the given semiconductor processing, as will be appreciated by those skilled in the art.

It should be noted that the term monolayer is meant to include a single atomic layer and also a single molecular layer. It is also noted that the energy band-modifying layer **50** provided by a single monolayer is also meant to include a monolayer wherein not all of the possible sites are occupied. For example, with particular reference to the atomic diagram of FIG. **3**, a 4/1 repeating structure is illustrated for silicon as the base semiconductor material, and oxygen as the energy band-modifying material. Only half of the possible sites for oxygen are occupied.

In other embodiments and/or with different materials this one half occupation would not necessarily be the case as will be appreciated by those skilled in the art. Indeed, it can be seen even in this schematic diagram, that individual atoms of oxygen in a given monolayer are not precisely aligned along a flat plane as will also be appreciated by those of skill in the art of atomic deposition. By way of example, a preferred occupation range is from about one-eighth to one-half of the possible oxygen sites being full, although other numbers may be used in certain embodiments.

Silicon and oxygen are currently widely used in conventional semiconductor processing, and, hence, manufacturers will be readily able to use these materials as described herein. Atomic or monolayer deposition is also now widely used. Accordingly, semiconductor devices incorporating the superlattice **25** in accordance with the invention may be readily adopted and implemented, as will be appreciated by those skilled in the art.

It is theorized without Applicants wishing to be bound thereto that for a superlattice, such as the Si/O superlattice, for example, that the number of silicon monolayers should desirably be seven or less so that the energy band of the superlattice is common or relatively uniform throughout to achieve the desired advantages. The 4/1 repeating structure shown in FIGS. **2** and **3** for Si/O has been modeled to indicate an enhanced mobility for electrons and holes in the X direction. For example, the calculated conductivity effective mass for electrons (isotropic for bulk silicon) is 0.26 and for the 4/1 SiO superlattice in the X direction it is 0.12, resulting in a ratio of 0.46. Similarly, the calculation for holes yields values of 0.36 for bulk silicon and 0.16 for the 4/1 Si/O superlattice resulting in a ratio of 0.44.

While such a directionally preferential feature may be desired in certain semiconductor devices, other devices may benefit from a more uniform increase in mobility in any direction parallel to the groups of layers. It may also be beneficial to have an increased mobility for both electrons and holes, or just one of these types of charge carriers, as will be appreciated by those skilled in the art.

The lower conductivity effective mass for the 4/1 Si/O embodiment of the superlattice **25** may be less than two-thirds the conductivity effective mass than would otherwise occur, and this applies for both electrons and holes. Of course, the superlattice **25** may further comprise at least one type of conductivity dopant therein as will also be appreciated by those skilled in the art.

Indeed, referring now additionally to FIG. **4**, another embodiment of a superlattice **25'** in accordance with the invention having different properties is now described. In this embodiment, a repeating pattern of 3/1/5/1 is illustrated. More particularly, the lowest base semiconductor portion **46***a'* has three monolayers, and the second lowest base semiconductor portion **46***b'* has five monolayers. This pattern repeats throughout the superlattice **25'**. The energy band-modifying layers **50'** may each include a single monolayer. For such a superlattice **25'** including Si/O, the enhancement of charge carrier mobility is independent of orientation in the plane of the layers. Those other elements of FIG. **4** not specifically mentioned are similar to those discussed above with reference to FIG. **2** and need no further discussion herein.

In some device embodiments, all of the base semiconductor portions of a superlattice may be a same number of monolayers thick. In other embodiments, at least some of the base semiconductor portions may be a different number of monolayers thick. In still other embodiments, all of the base semiconductor portions may be a different number of monolayers thick.

In FIGS. **5**A-**5**C band structures calculated using Density Functional Theory (DFT) are presented. It is well known in the art that DFT underestimates the absolute value of the bandgap. Hence all bands above the gap may be shifted by an appropriate "scissors correction." However the shape of the band is known to be much more reliable. The vertical energy axes should be interpreted in this light.

FIG. **5**A shows the calculated band structure from the gamma point (G) for both bulk silicon (represented by continuous lines) and for the 4/1 Si/O superlattice **25** as shown in FIGS. **1-3** (represented by dotted lines). The directions refer to the unit cell of the 4/1 Si/O structure and not to the conventional unit cell of Si, although the (001) direction in the figure does correspond to the (001) direction of the conventional unit cell of Si, and, hence, shows the expected location of the Si conduction band minimum. The (100) and (010) directions in the figure correspond to the (110) and (−110) directions of the conventional Si unit cell. Those skilled in the art will appreciate that the bands of Si on the figure are folded to represent them on the appropriate reciprocal lattice directions for the 4/1 Si/O structure.

It can be seen that the conduction band minimum for the 4/1 Si/O structure is located at the gamma point in contrast to bulk silicon (Si), whereas the valence band minimum occurs at the edge of the Brillouin zone in the (001) direction which we refer to as the Z point. One may also note the greater curvature of the conduction band minimum for the 4/1 Si/O structure compared to the curvature of the conduction band minimum for Si owing to the band splitting due to the perturbation introduced by the additional oxygen layer.

FIG. **5**B shows the calculated band structure from the Z point for both bulk silicon (continuous lines) and for the 4/1 Si/O superlattice **25** (dotted lines). This figure illustrates the enhanced curvature of the valence band in the (100) direction.

FIG. **5**C shows the calculated band structure from both the gamma and Z point for both bulk silicon (continuous lines) and for the 5/1/3/1 Si/O structure of the superlattice **25'** of FIG. **4** (dotted lines). Due to the symmetry of the 5/1/3/1 Si/O structure, the calculated band structures in the (100) and (010) directions are equivalent. Thus the conductivity effective mass and mobility are expected to be isotropic in the plane parallel to the layers, i.e., perpendicular to the

(001) stacking direction. Note that in the 5/1/3/1 Si/O example the conduction band minimum and the valence band maximum are both at or close to the Z point.

Although increased curvature is an indication of reduced effective mass, the appropriate comparison and discrimination may be made via the conductivity reciprocal effective mass tensor calculation. This leads Applicants to further theorize that the 5/1/3/1 superlattice **25'** should be substantially direct bandgap. As will be understood by those skilled in the art, the appropriate matrix element for optical transition is another indicator of the distinction between direct and indirect bandgap behavior.

Referring now additionally to FIGS. **6**A-**6**E, a method for making the MOSFET **20** will now be described. The method begins with providing the silicon substrate **21**. By way of example, the substrate may be an eight-inch wafer **21** of lightly doped P-type or N-type single crystal silicon with <100> orientation, although other suitable substrates may also be used. In accordance with the present example, a layer of the superlattice **25** material is then formed across the upper surface of the substrate **21**.

More particularly, the superlattice **25** material is deposited across the surface of the substrate **21** using atomic layer deposition and the epitaxial silicon cap layer **52** is formed, as discussed previously above, and the surface is planarized to arrive at the structure of FIG. **6**A. It should be noted that in some embodiments the superlattice **25** material may be selectively deposited in those regions where channels are to be formed, rather than across the entire substrate **21**, as will be appreciated by those skilled in the art. Moreover, planarization may not be required in all embodiments.

The epitaxial silicon cap layer **52** may have a preferred thickness to prevent superlattice consumption during gate oxide growth, or any other subsequent oxidations, while at the same time reducing or minimizing the thickness of the silicon cap layer to reduce any parallel path of conduction with the superlattice. According to the well-known relationship of consuming approximately 45% of the underlying silicon for a given oxide grown, the silicon cap layer may be greater than 45% of the grown gate oxide thickness plus a small incremental amount to account for manufacturing tolerances known to those skilled in the art. For the present example, and assuming growth of a 25 angstrom gate, one may use approximately 13-15 angstroms of silicon cap thickness.

FIG. **6**B depicts the MOSFET **20** after the gate oxide **37** and the gate electrode **36** are formed. More particularly, a thin gate oxide is deposited, and steps of poly deposition, patterning, and etching are performed, as will be appreciated by those skilled in the art. Poly deposition refers to low pressure chemical vapor deposition (LPCVD) of silicon onto an oxide (hence it forms a polycrystalline material). The step includes doping with P+ or As− to make it conducting, and the layer may be around 250 nm thick, for example.

In addition, the pattern step may include performing a spinning photoresist, baking, exposure to light (i.e., a photolithography step), and developing the resist. Usually, the pattern is then transferred to another layer (oxide or nitride) which acts as an etch mask during the etch step. The etch step typically is a plasma etch (anisotropic, dry etch) that is material selective (e.g., etches silicon ten times faster than oxide) and transfers the lithography pattern into the material of interest.

Referring to FIG. **6**C, once the gate **35** is formed, the gate may then be used as an etch mask to remove the superlattice **25** material in the regions where the source and drain **22**, **23** are to be formed, as will be appreciated by those skilled in the art. The superlattice **25** material may be etched in a similar fashion to that described above for the gate **35**. However, it should be noted that with the non-semiconductor present in the superlattice **25**, e.g., oxygen, the superlattice may be more easily etched using an etchant formulated for oxides rather than silicon. Of course, the appropriate etch for a given implementation will vary based upon the structure and materials used for the superlattice **25** and substrate **21**, as will be appreciated by those of skill in the art.

In FIG. **6**D, the epitaxial source and drain layers **26**, **28** are formed, which may be done using known epitaxial deposition methods. Referring to FIG. **6**E, the source and drain regions **22**, **23** are doped using the appropriate n-type or p-type implantation. An anneal and/or clean step may be used after the implantation, but depending on the specific process, they may be omitted. Self-aligned silicide formation may then be performed to form the silicide layers **30**, **31**, and **34**, and the source/drain contacts **32**, **33**, are formed to provide the final semiconductor device **20** illustrated in FIG. **1**. The silicide formation is also known as salicidation. The salicidation process includes metal deposition (e.g. Ti), nitrogen annealing, metal etching, and a second annealing.

The foregoing is, of course, but one example of a process and device in which the present invention may be used, and those of skill in the art will understand its application and use in many other processes and devices. In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer. Additionally, the use of an atomic layer deposition tool may also not be needed for forming the superlattice **25** in some embodiments. For example, the monolayers may be formed using a CVD tool with process conditions compatible with control of monolayers, as will be appreciated by those skilled in the art.

An alternate embodiment of the semiconductor device **20"** and method form making the same will now be described with reference to FIGS. **7**A-**7**E and **8**. First, a trench **70"** is formed in the substrate **21"** using known semiconductor techniques (FIG. **7**A). Next, the superlattice **25"** is formed within the trench **70"** (FIG. **7**B), as described above. The gate insulating layer **37"** and gate electrode layer **36"** are then formed and patterned, as necessary, as seen in FIG. **7**C. Trenches **71"**, **72"** are then formed next to the gate in the substrate **21"** in the areas where the source and drain regions **23"**, **24"** are to be formed (FIG. **7**D).

Thus, it may be seen that the upper portions of the superlattice **25"** extend above bottom portions **73"**, **74"** of the trenches **71"**, **72"**. Again, this creates a channel region which occupies only the lower portions of the superlattice **25"**, thus advantageously reducing current flow near the gate insulation layer **37"**. Source and drain implantation is next performed, as described above, to form the source and drain regions **22"**, **23"** (FIG. **7**E). Furthermore, silicide formation may then be performed to form the silicide layers **30"**, **31"**, and **34"**, and the source/drain contacts **32"**, **33"** are formed to provide the final semiconductor device **20"** illustrated in FIG. **8**.

It should be noted that certain of the above-noted steps may be performed in different orders in different embodiments. For example, the trenches **71"**, **72"** may be formed after implantation of the source and drain regions **22"**, **23"**. Moreover, in an alternate embodiment, the trenches **71"**, **72"** may be formed in the superlattice **25"** at the outer edges thereof to provide the desired separation between the upper portions of the superlattice and the source and drain regions **22"**, **23"**, as will be appreciated by those skilled in the art.

While only a single MOSFET **20"** has been illustrated in the drawings and described above for clarity of explanation and illustration, it will be appreciated that multiple MOSFETs may be formed in the substrate **21"**, such as NMOS and PMOS transistors to provide a CMOS device. More particularly, shallow trench isolation (STI) regions (not shown) may be formed between adjacent MOSFETS, as will be appreciated by those skilled in the art. In accordance with one embodiment, the STI regions may be formed prior to depositing the superlattice **25"**, so that the STI regions thus provide boundaries for selective deposition of the superlattice.

More particularly, the wafer is patterned and trenches are etched (e.g., 0.3-0.8 um) in the desired STI regions. A thin oxide is then grown, and the trenches are filled with SiO_2 to provide the STI regions, and the upper surfaces thereof may be planarized, if desired. The STI regions may also be used as an etch stop in performing certain of the above-noted steps, as will be appreciated by those skilled in the art. The superlattice **25"** structure may also be formed prior to formation of the STI regions to thereby eliminate a masking step, if desired. Further details regarding fabrication of the semiconductor devices in accordance with the present invention may be found in the above-noted U.S. application Ser. No. 10/467,069.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

That which is claimed is:

1. A method for making a semiconductor device comprising:

providing a semiconductor substrate; and

forming at least one metal oxide semiconductor field-effect transistor (MOSFET) by

forming spaced apart source and drain regions and a superlattice on the semiconductor substrate so that the superlattice is between the source and drain regions, the superlattice comprising a plurality of stacked groups of layers and having upper portions extending above adjacent upper portions of the source and drain regions and lower portions contacting the source and drain regions so that a channel is defined in lower portions of the superlattice,

each group of layers of the superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

the energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions, and at least some semiconductor atoms from opposing semiconductor portions being chemically bound together through the at least one non-semiconductor monolayer therebetween, and

forming a gate overlying the superlattice.

2. The method of claim **1** wherein each of the source and drain regions comprises a respective epitaxial silicon layer.

3. The method of claim **2** wherein the superlattice has a greater thickness than the epitaxial silicon layers.

4. The method of claim **1** wherein the source and drain regions each have a respective trench therein adjacent the superlattice; and wherein the upper portions of the superlattice extend above bottom portions of the trenches.

5. The method of claim **1** wherein forming the gate comprises forming an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer.

6. The method of claim **1** further comprising forming a contact layer on at least one of the source and drain regions.

7. The method of claim **1** wherein the superlattice has a common energy band structure therein.

8. The method of claim **1**. wherein the superlattice has a higher charge carrier mobility than would otherwise be present without the non-semiconductor layer.

9. The method of claim **1** wherein each base semiconductor portion comprises silicon.

10. The method of claim **1** wherein each base semiconductor portion comprises germanium.

11. The method of claim **1** wherein each energy band-modifying layer comprises oxygen.

12. The method of claim **1** wherein each energy band-modifying layer is a single monolayer thick.

13. The method of claim **1** wherein each base semiconductor portion is less than eight monolayers thick.

14. The method of claim **1** wherein the superlattice further has a substantially direct energy bandgap.

15. The method of claim **1** wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

16. The method of claim **1** wherein all of the base semiconductor portions are a same number of monolayers thick.

17. The method of claim **1** wherein at least some of the base semiconductor portions are a different number of monolayers thick.

18. The method of claim **1** wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

19. A method for making a semiconductor device comprising:

providing a semiconductor substrate; and

forming at least one metal oxide semiconductor field-effect transistor (MOSFET) by

forming spaced apart source and drain regions and a superlattice on the semiconductor substrate so that the superlattice is between the source and drain regions, the source and drain regions each having a respective trench therein adjacent the superlattice, and the superlattice having upper portions extending above bottom portions of the trenches and lower portions contacting the source and drain regions so that a channel is defined in lower portions of the superlattice,

each group of layers of the superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

the energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor, and at least some semiconductor atoms from opposing semiconductor portions being chemically bound together through the at least one non-semiconductor monolayer therebetween, and

forming a gate overlying the superlattice by forming an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer.

20. The method of claim 19 further comprising forming a contact layer on at least one of the source and drain regions.

21. The method of claim 19 wherein the superlattice has a common energy band structure therein.

22. The method of claim 19 wherein the superlattice has a higher charge carrier mobility than would otherwise be present without the non-semiconductor layer.

23. The method of claim 19 wherein each base semiconductor portion comprises silicon.

24. The method of claim 19 wherein each base semiconductor portion comprises germanium.

25. The method of claim 19 wherein each energy band-modifying layer comprises oxygen.

26. The method of claim 19 wherein each energy band-modifying layer is a single monolayer thick.

27. The method of claim 19 wherein each base semiconductor portion is less than eight monolayers thick.

28. The method of claim 19 wherein the superlattice further has a substantially direct energy bandgap.

29. The method of claim 19 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

30. The method of claim 19 wherein all of the base semiconductor portions are a same number of monolayers thick.

31. The method of claim 19 wherein at least some of the base semiconductor portions are a different number of monolayers thick.

32. The method of claim 19 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

33. A method for making a semiconductor device comprising:

providing a semiconductor substrate; and

forming at least one metal oxide semiconductor field-effect transistor (MOSFET) by

forming spaced apart source and drain regions and a superlattice on the semiconductor substrate so that the superlattice is between the source and drain regions, the source and drain regions each comprising a respective epitaxial silicon layer, and the superlattice comprising a plurality of stacked groups of layers,

the superlattice having a greater thickness than the epitaxial silicon layers, and lower portions of the superlattice being in contact with the epitaxial silicon layers so that a channel is defined in lower portions of the superlattice,

each group of layers of the superlattice comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion and an energy band-modifying layer thereon,

the energy-band modifying layer comprising at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions, and at least some semiconductor atoms from opposing semiconductor portions being chemically bound together through the at least one non-semiconductor monolayer therebetween, and

forming a gate overlying the superlattice by forming an oxide layer overlying the superlattice channel and a gate electrode overlying the oxide layer.

34. The method of claim 33 further comprising forming a contact layer on at least one of the source and drain regions.

35. The method of claim 33 wherein the superlattice has a common energy band structure therein.

36. The method of claim 33 wherein the superlattice has a higher charge carrier mobility than would otherwise be present without the non-semiconductor layer.

37. The method of claim 33 wherein each base semiconductor portion comprises silicon.

38. The method of claim 33 wherein each base semiconductor portion comprises germanium.

39. The method of claim 33 wherein each energy band-modifying layer comprises oxygen.

40. The method of claim 33 wherein each energy band-modifying layer is a single monolayer thick.

41. The method of claim 33 wherein each base semiconductor portion is less than eight monolayers thick.

42. The method of claim 33 wherein the superlattice further has a substantially direct energy bandgap.

43. The method of claim 33 wherein the superlattice further comprises a base semiconductor cap layer on an uppermost group of layers.

44. The method of claim 33 wherein all of the base semiconductor portions are a same number of monolayers thick.

45. The method of claim 33 wherein at least some of the base semiconductor portions are a different number of monolayers thick.

46. The method of claim 33 wherein each energy band-modifying layer comprises a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, and carbon-oxygen.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,288,457 B2
APPLICATION NO. : 10/940594
DATED : October 30, 2007
INVENTOR(S) : Kreps

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3, Line 55 — Delete: "is schematic"
Insert: -- is a schematic --

Column 4, Line 63 — Delete: " $\sum_{E<E_F} \int_{B.Z.} (1 - f(E(\mathbf{k},n), E_F, T)\, d^3\mathbf{k}$ "

Insert: -- $\sum_{E<E_F} \int_{B.Z.} (1 - f(E(\mathbf{k},n), E_F, T))\, d^3\mathbf{k}$ --

Column 10, Line 36 — Delete: "form"
Insert: -- for --

Column 12, Line 10 — Delete: "claim 1. wherein"
Insert: -- claim 1 wherein --

Signed and Sealed this

Twenty-ninth Day of July, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office