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(54) **MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE**

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(51) **Int. Cl.**
H01L 51/40 (2006.01)

(52) **U.S. Cl.** **438/99**; 438/102

(58) **Field of Classification Search** 438/3, 438/102–103, 99
See application file for complete search history.

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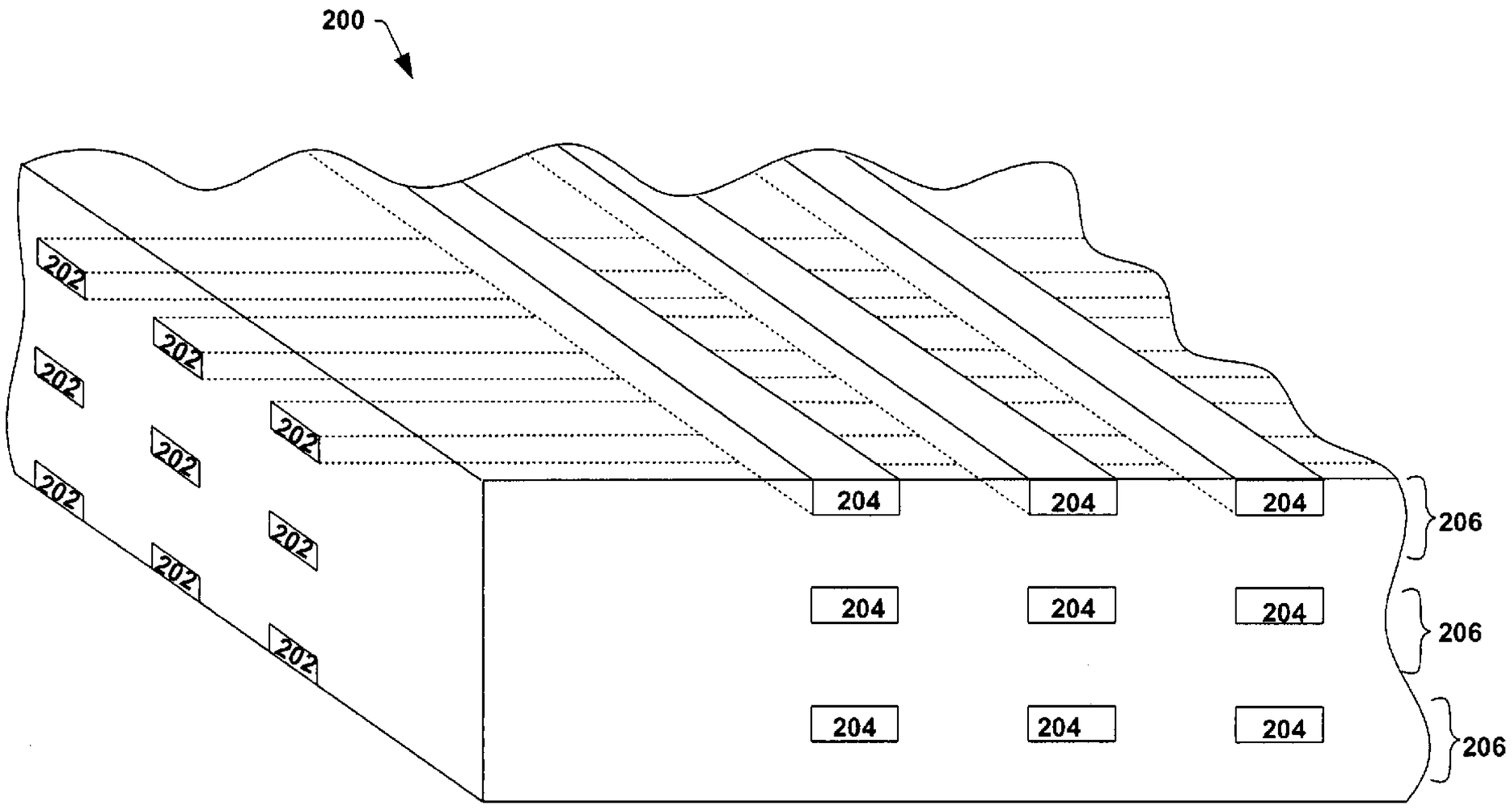
(57) **ABSTRACT**

A memory cell made of two electrodes with a controllably conductive media between the two electrodes is disclosed. The controllably conductive media contains an active low conductive layer and passive layer. The controllably conductive media changes its impedance when an external stimuli such as an applied electric field is imposed thereon. Methods of making the memory devices/cells, methods of using the memory devices/cells, and devices such as computers containing the memory devices/cells are also disclosed.

19 Claims, 2 Drawing Sheets



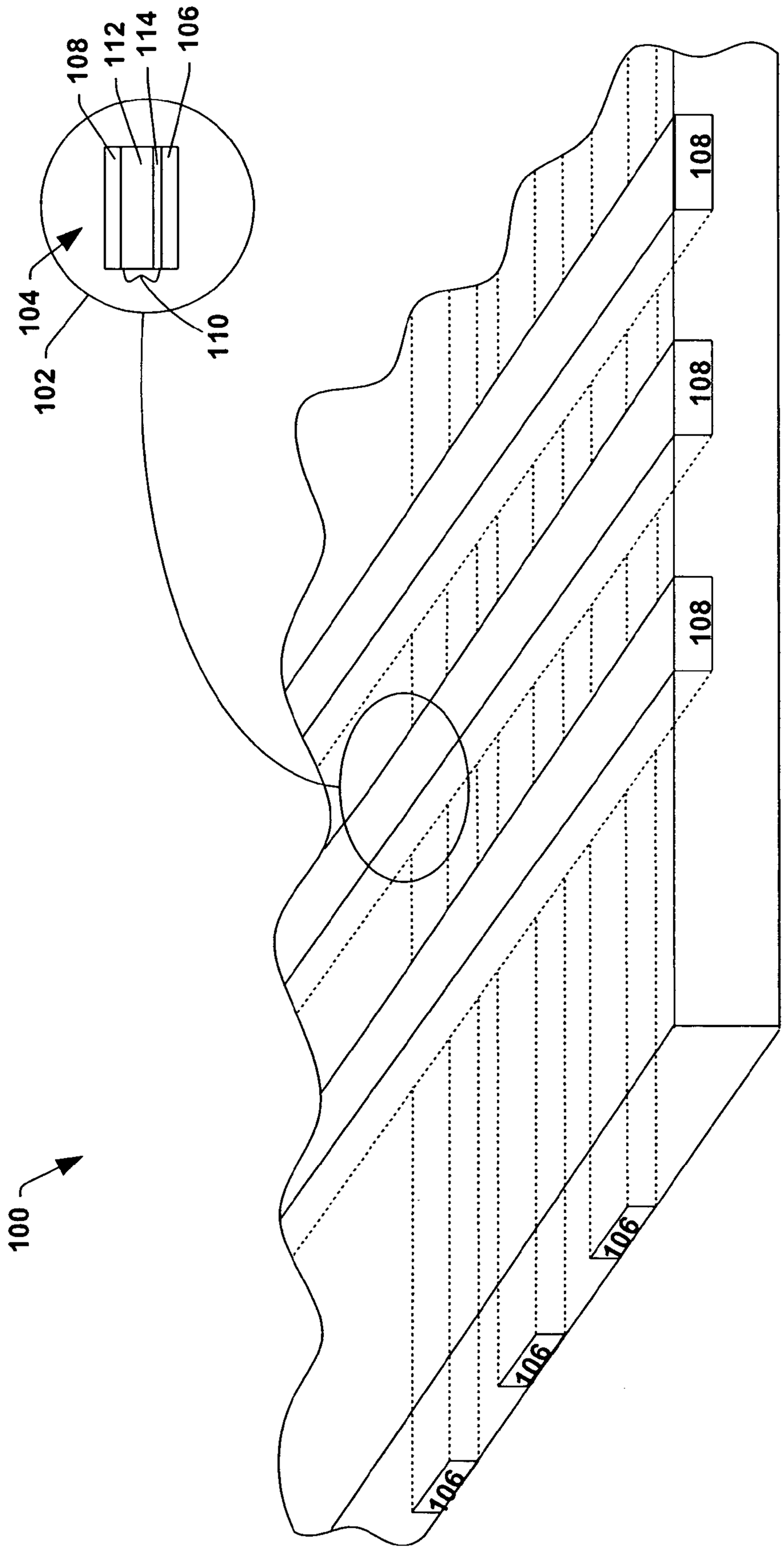


FIG. 1

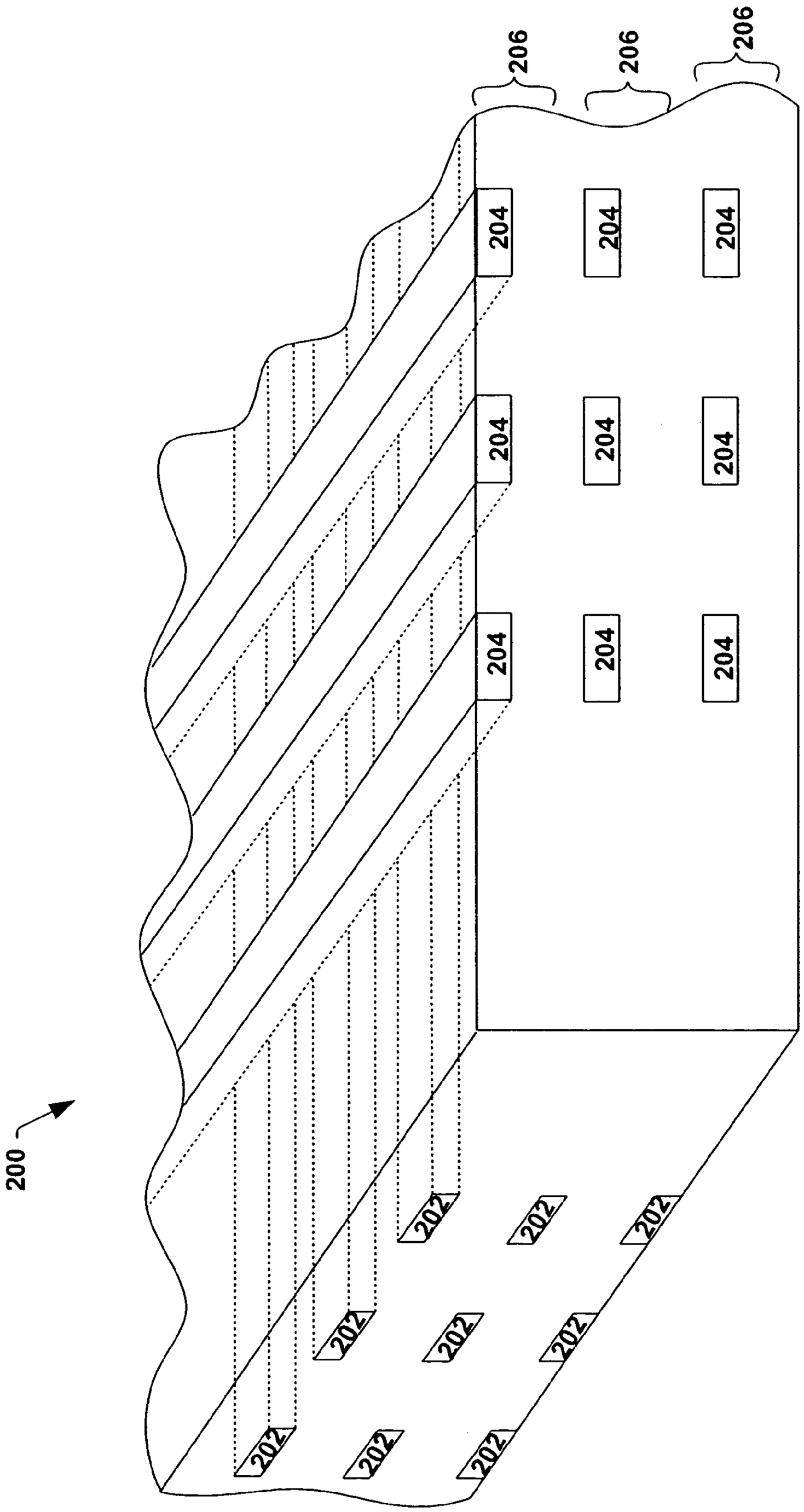

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FIG. 2

MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE

TECHNICAL FIELD

The present invention generally relates to memory devices and methods of making and using the memory devices. In particular, the present invention relates to memory devices containing controllably conductive layer(s).

BACKGROUND ART

The basic functions of a computer and memory devices include information processing and storage. In typical computer systems, these arithmetic, logic, and memory operations are performed by devices that are capable of reversibly switching between two states often referred to as "0" and "1." Such switching devices are fabricated from semiconducting devices that perform these various functions and are capable of switching between two states at high speed.

Electronic addressing or logic devices, for instance for storage or processing of data, are made with inorganic solid state technology, and particularly crystalline silicon devices. The metal oxide semiconductor field effect transistor (MOSFET) is one the main workhorses.

Much of the progress in making computers and memory devices faster, smaller and cheaper involves integration, squeezing ever more transistors and other electronic structures onto a postage-stamp-sized piece of silicon. A postage-stamp-sized piece of silicon may contain tens of millions of transistors, each transistor as small as a few hundred nanometers. However, silicon-based devices are approaching their fundamental physical size limits.

Inorganic solid state devices are generally encumbered with a complex architecture which leads to high cost and a loss of data storage density. The circuitry of volatile semiconductor memories based on inorganic semiconductor material must constantly be supplied with electric current with a resulting heating and high electric power consumption in order to maintain stored information. Non-volatile semiconductor devices have a reduced data rate and relatively high power consumption and large degree of complexity.

Moreover, as inorganic solid state device sizes decrease and integration increases, sensitivity to alignment tolerances increases making fabrication markedly more difficult. Formation of features at small minimum sizes does not imply that the minimum size can be used for fabrication of working circuits. It is necessary to have alignment tolerances which are much smaller than the small minimum size, for example, one quarter the minimum size.

Scaling inorganic solid state devices raises issues with dopant diffusion lengths. As dimensions are reduced, the dopant diffusion lengths in silicon are posing difficulties in process design. In this connection, many accommodations are made to reduce dopant mobility and to reduce time at high temperatures. However, it is not clear that such accommodations can be continued indefinitely.

Applying a voltage across a semiconductor junction (in the reverse-bias direction) creates a depletion region around the junction. The width of the depletion region depends on the doping levels of the semiconductor. If the depletion region spreads to contact another depletion region, punch-through or uncontrolled current flow, may occur.

Higher doping levels tend to minimize the separations required to prevent punch-through. However, if the voltage change per unit distance is large, further difficulties are created in that a large voltage change per unit distance implies that the magnitude of the electric field is large. An electron traversing such a sharp gradient may be accelerated to an energy level significantly higher than the minimum conduction band energy. Such an electron is known as a hot electron, and may be sufficiently energetic to pass through an insulator, leading to irreversibly degradation of a semiconductor device.

Scaling and integration makes isolation in a monolithic semiconductor substrate more challenging. In particular, lateral isolation of devices from each other is difficult in some situations. Another difficulty is leakage current scaling. Yet another difficulty is presented by the diffusion of carriers within the substrate; that is free carriers can diffuse over many tens of microns and neutralize a stored charge.

SUMMARY OF THE INVENTION

The following is a summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not intended to identify key/critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later.

The present invention provides new memory devices that possess one or more of the following: small size compared to conventional memory devices, capability to store multiple bits of information, short resistance/impedance switch time, low operating voltages, low cost, high reliability, long life (thousands/millions of cycles), capable of three dimensional packing, associated low temperature (or high temperature) processing, light weight, high density/integration, and extended memory retention.

One aspect of the present invention relates to a memory device containing at least one memory cell made of two electrodes with a controllably conductive media between the two electrodes, the controllably conductive media containing a low conductive layer and passive layer, wherein the passive layer has a Fermi level close to the valence band of the low conductive layer. Other aspects of the present invention relate to making the memory devices/cells, using (such as programming) the memory devices/cells, and to devices such as computers containing the memory devices/cells.

To the accomplishment of the foregoing and related ends, the invention comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative aspects and implementations of the invention. These are indicative, however, of but a few of the various ways in which the principles of the invention may be employed. Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** illustrates a perspective view of a two dimensional microelectronic device containing a plurality of memory cells in accordance with one aspect of the invention.

FIG. **2** illustrates a perspective view of a three dimensional microelectronic device containing a plurality of memory cells in accordance with another aspect of the invention.

DISCLOSURE OF INVENTION

The present invention involves memory cells made of two electrodes with a controllably conductive media between the two electrodes. The controllably conductive media contains a low conductive layer and passive layer. This media can be organic, inorganic, or organic mixed with inorganic material(s). The memory cells may optionally contain additional layers, such as additional electrodes, charge retention layers, and/or chemically active layers. The impedance of the controllably conductive media changes when an external stimuli such as an applied electric field is imposed. A plurality of the memory cells, which may be referred to as an array, form a new memory device. In this connection, memory cells may form new memory devices and function in a manner analogous to metal oxide semiconductor field effect transistors (MOSFETs) in conventional semiconductor memory devices. However, there are advantages to using the new memory cells instead of conventional MOSFETs in memory devices.

Referring to FIG. **1**, a brief description of a microelectronic memory device **100** containing a plurality of memory cells in accordance with one aspect of the invention is shown, as well as an exploded view **102** of an exemplary memory cell **104**. The microelectronic memory device **100** contains a desired number of memory cells, as determined by the number of rows, columns, and layers (three dimensional orientation described later) present. The first electrodes **106** and the second electrodes **108** are shown in substantially perpendicular orientation, although other orientations are possible to achieve the structure of the exploded view **102**. Each memory cell **104** contains a first electrode **106** and a second electrode **108** with a controllably conductive media **110** therebetween. The controllably conductive media **110** contains a low conductive layer **112** and passive layer **114**. Peripheral circuitry and devices are not shown for brevity.

The memory cells contain at least two electrodes, as one or more electrodes may be disposed between the two electrodes that sandwich the controllably conductive media. The electrodes are made of conductive material, such as conductive metal, conductive metal alloys, conductive metal oxides, conductive polymer films, semiconductive materials, and the like.

Examples of electrodes include one or more of aluminum, chromium, copper, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, and alloys thereof; indium-tin oxide (ITO); polysilicon; doped amorphous silicon; metal silicides; and the like. Alloy electrodes specifically include Hastelloy®, Kovar®, Invar, Monel®, Inconel®, brass, stainless steel, magnesium-silver alloy, and various other alloys.

In one embodiment, the thickness of each electrode is independently about 0.01 μm or more and about 10 μm or less. In another embodiment, the thickness of each electrode is independently about 0.05 μm or more and about 5 μm or less. In yet another embodiment, the thickness of each electrode is independently about 0.1 μm or more and about 1 μm or less.

The controllably conductive media, disposed between the two electrodes, can be rendered conductive, semiconductive, or nonconductive in a controllable manner using an external stimuli. Generally, in the absence of an external stimuli, the controllably conductive media is nonconductive or has a high impedance. Further, in some embodiments, multiple degrees of conductivity/resistivity may be established for the controllably conductive media in a controllable manner. For example, the multiple degrees of conductivity/resistivity for the controllably conductive media may include a nonconductive state, a highly conductive state, and a semiconductive state.

The controllably conductive media can be rendered conductive, non-conductive or any state therebetween (degree of conductivity) in a controllable manner by an external stimulus (external meaning originating from outside the controllably conductive media). For example, under an external electric field, radiation, and the like, a given non-conductive controllably conductive media is converted to a conductive controllably conductive media.

The controllably conductive media contains one or more low conductive layers and one or more passive layers. In one embodiment, the controllably conductive media contains at least one organic semiconductor layer that is adjacent a passive layer (without any intermediary layers between the organic semiconductor layer and passive layer). In another embodiment, the controllably conductive media contains at least one inorganic low conductive layer that is adjacent a passive layer (without any intermediary layers between the inorganic layer and passive layer). In yet another embodiment, the controllably conductive media contains a mixture of organic and inorganic materials as the low conductive layer that is adjacent a passive layer (without any intermediary layers between the low conductive layer and passive layer).

The organic semiconductor layer contains at least one of an organic polymer (such as a conjugated organic polymer), an organometallic compound (such as a conjugated organometallic compound), an organometallic polymer (such as a conjugated organometallic polymer), a buckyball, a carbon nanotube (such as a C6-C60 carbon nanotubes), and the like. Organic semiconductors thus have a carbon based structure, often a carbon-hydrogen based structure, which is different from conventional MOSFETs. The organic semiconductor materials are typically characterized in that they have overlapping p orbitals, and/or in that they have at least two stable oxidation states. The organic semiconductor materials are also characterized in that they may assume two or more resonant structures. The overlapping p orbitals contribute to the controllably conductive properties of the controllably conductive media. The amount of charge injected into the organic semiconductor layer also influences the degree of conductivity of the organic semiconductor layer.

A carbon nanotube is typically a hexagonal network of carbon atoms (from about 6 to about 60 carbon atoms, typically) that is rolled up into a seamless cylinder. Each end may be capped with half of a fullerene molecule. Carbon nanotubes may be prepared by the laser vaporization of a carbon target (a cobalt-nickel catalyst may facilitate growth) or a carbon-arc method to grow similar arrays of single-wall nanotubes. A buckyball is more specifically a Buckminsterfullerene, a soccerball-shaped 60-atom cluster of pure carbon.

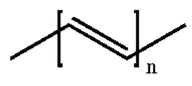
The organic polymer typically contains a conjugated organic polymer. The polymer backbone of the conjugated organic polymer extends lengthwise between the electrodes (generally substantially perpendicular to the inner, facing surfaces of the electrodes). The conjugated organic polymer may be linear or branched, so long as the polymer retains its conjugated nature. Conjugated polymers are characterized in that they have overlapping p orbitals. Conjugated polymers are also characterized in that they may assume two or more resonant structures. The conjugated nature of the conjugated organic polymer contributes to the controllably conductive properties of the controllably conductive media.

In this connection, the low conductive layer or organic semiconductor layer, such as the conjugated organic polymer, has the ability to donate and accept charges. Generally, the organic semiconductor or an atom/moiety in the polymer has at least two relatively stable oxidation states. The two relatively stable oxidation states permit the organic semiconductor to donate and accept charges and electrically interact with the conductivity facilitating compound. The ability of the organic semiconductor layer to donate and accept charges and electrically interact with the passive layer also depends on the identity of the conductivity facilitating compound. The injected charges from the passive layer can be trapped in the organic semiconductor layer and the interface adjacent to the passive layer. This changes the conductivity of the low conductive layer and results in memory effect.

The organic polymers (or the organic monomers constituting the organic polymers) may be cyclic or acyclic. During formation or deposition, the organic polymer self assembles between the electrodes. Examples of conjugated organic polymers include one or more of polyacetylene; polyphenylacetylene; polydiphenylacetylene; polyaniline; poly(p-phenylene vinylene); polythiophene; polyporphyrins; porphyrinic macrocycles, thiol derivatized polyporphyrins; polymetallocenes such as polyferrocenes, polyphthalocyanines; polyvinylenes; polystiroles; poly(t-butyl) diphenylacetylene; poly(trifluoromethyl)diphenylacetylene; polybis(trifluoromethyl)acetylene; polybis(t-butyldiphenyl) acetylene; poly(trimethylsilyl) diphenylacetylene; poly(carbazole)diphenylacetylene; polydiacetylene; polypyridineacetylene; polymethoxyphenylacetylene; polymethylphenylacetylene; poly(t-butyl)phenylacetylene; polynitro-phenylacetylene; poly(trifluoromethyl) phenylacetylene; poly(trimethylsilyl)pheylacetylene; polydipyrrylmethane; polyindoqiunone; polydihydroxyindole; polytrihydroxyindole; furane-polydihydroxyindole; polyindoqiunone-2-carboxyl; polyindoqiunone; polybenzobisthiazole; poly(p-phenylene sulfide); polypyrrole; polystyrene; polyfuran; polyindole; polyazulene; polyphenylene; polypyridine; polybipyridine; polysexithiofene; poly(siliconoxohemiporphyrazine); poly(germaniumoxohemiporphyrazine); poly(ethylenedioxythiophene); polypyridine metal complexes; and the like.

Chemical structures of examples of repeating units/moieties that make up the conjugated organic polymers and conjugated organometallic polymers include one or more of Formulae (I) to (XIII):

(I)



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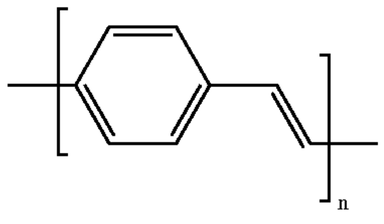

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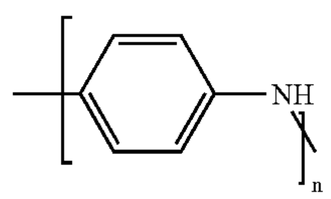

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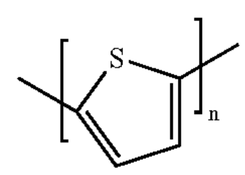

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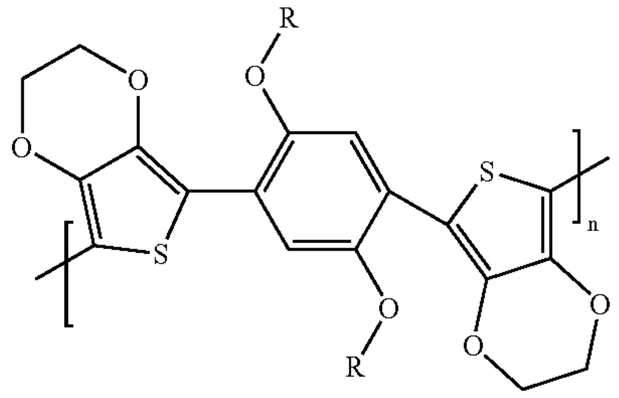

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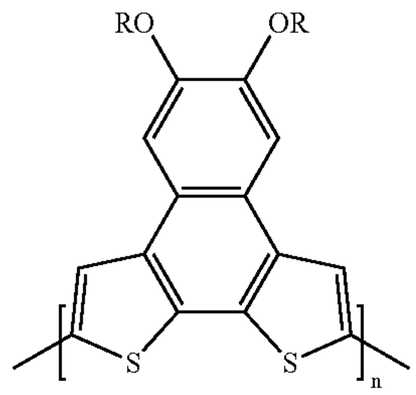

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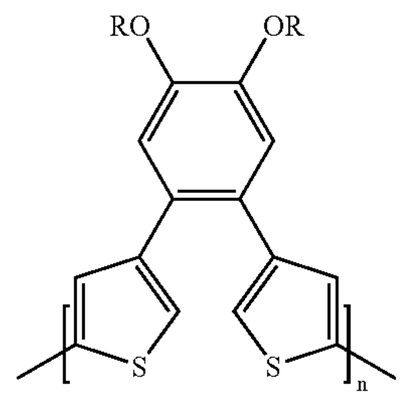

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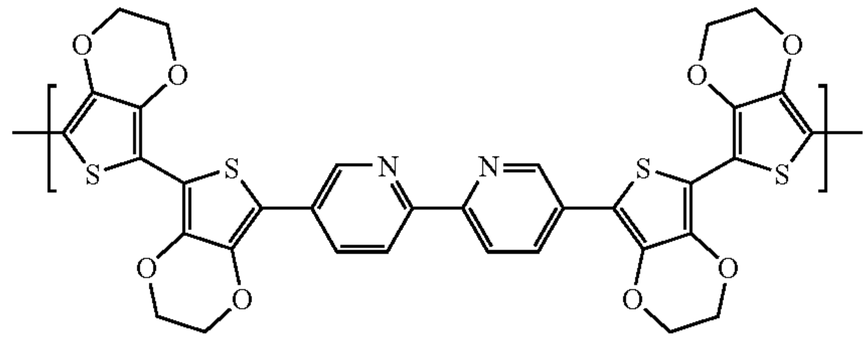

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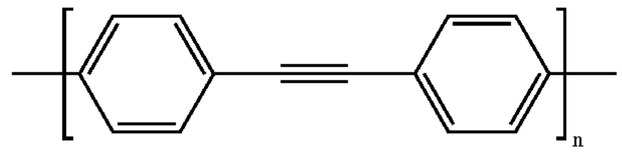

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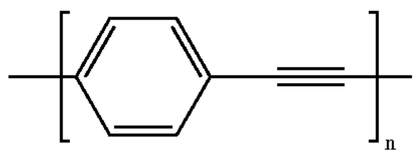

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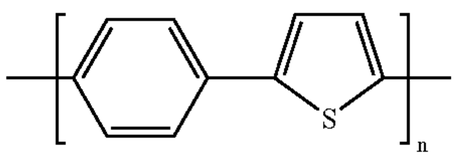

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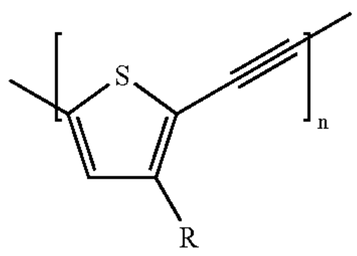

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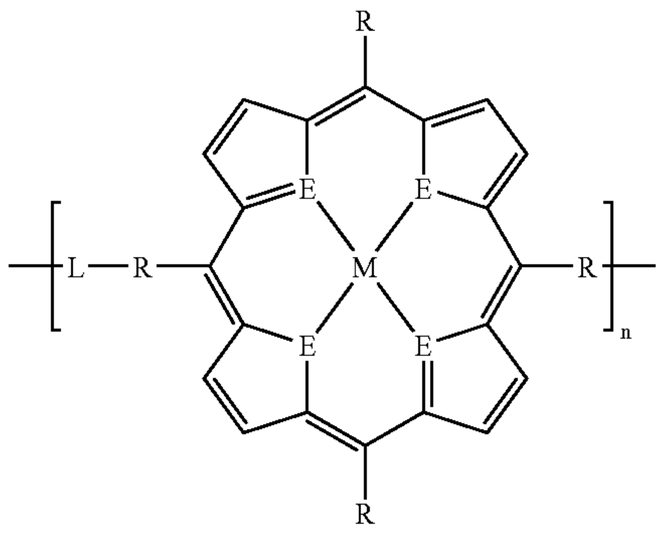


wherein each R is independently hydrogen or hydrocarbyl; each M is independently a metal; each E is independently O, N, S, Se, Te, or CH; each L is independently a group containing or continuing conjugation (unsaturation); and each n is independently about 1 or more and about 25,000 or less. In another embodiment, each n is independently about 2 or more and about 10,000 or less. In yet another embodiment, each n is independently about 20 or more and about 5,000 or less. Examples of metals include Ag, Al, Au, B, Cd, Co, Cu, Fe, Ga, Hg, Ir, Mg, Mn, Ni, Pb, Pd, Pt, Rh, Sn, and Zn. Examples of L groups include hydrocarbyl groups possessing conjugation or the ability to form resonance structures, such as phenyl groups, substituted phenyl groups, acetylene groups, and the like.

Any of the formulae may have one or more pendent substituent groups, not shown in the formulae. For example, a phenyl group may appear on the polythiophene structure, such as on the 3 position of each thiophene moiety. As another example, alkyl, alkoxy, cyano, amino, and/or hydroxy substituent groups may be present on the phenyl rings in any of the polyphenylacetylene, polydiphenylacetylene, and poly(p-phenylene vinylene) conjugated polymers.

The term "hydrocarbyl" includes hydrocarbon as well as substantially hydrocarbon groups. Hydrocarbyl groups contain 1 or more carbon atom and typically about 60 or less carbon atoms. In another embodiment, hydrocarbyl groups contain 2 or more carbon atoms and about 30 or less carbon atoms. Substantially hydrocarbon describes groups which contain heteroatom substituents or heteroatoms which do not alter the predominantly organic character of the polymer, and do not impede the ability of the organic polymer to form a conjugated structure. Examples of hydrocarbyl groups include the following:

(1) hydrocarbon substituents, i.e., aliphatic (e.g., alkyl or alkenyl), alicyclic (e.g., cycloalkyl, cycloalkenyl) substituents, acyl, phenyl, aromatic-, aliphatic- and alicyclic-substituted aromatic substituents and the like as well as cyclic substituents wherein the ring is completed through another portion of the molecule (that is, for example, any two indicated substituents may together form an alicyclic radical);

(2) substituted hydrocarbon substituents, i.e., those substituents containing nonhydrocarbon groups which, in the context of this invention, do not alter the predominantly organic nature of the substituent; those skilled in the art will be aware of such groups (e.g., halo (especially chloro and fluoro, such as perfluoroalkyl, perfluoroaryl), cyano, thiocyanato, amino, alkylamino, sulfonyl, hydroxy, mercapto, nitro, nitroso, sulfoxy, etc.);

(3) heteroatom substituents, i.e., substituents which, while having a predominantly organic character within the context of this invention, contain an atom other than carbon present in a ring or chain otherwise composed of carbon atoms (e.g., alkoxy, alkylthio). Suitable heteroatoms will be apparent to those of ordinary skill in the art and include, for example, sulfur, oxygen, nitrogen, fluorine, chlorine, and such substituents as, e.g., pyridyl, furyl, thienyl, imidazolyl, imido, amido, carbamoyl, etc.

In addition to or as an alternative to the organic material, the active low conductive layer may contain an inorganic material. Inorganic materials include, low conductive chalcogenides and transition metal oxides. The oxide of a transition metal, represented by the general formula M_xO_y where M is a transition metal, and x and y are independently from about 0.25 to about 5, usually has low conductivity. Analogous transition metal sulfides may also be used. The transition metal in the oxide allows multi oxidation states that lead to conductivity changes under an external field. Examples include copper oxide (CuO, Cu_2O), iron oxide (FeO, Fe_3O_4), manganese oxide (MnO_2, Mn_2O_3, etc), titanium oxide (TiO_2). This material can be formed by thermal evaporation, CVD, or plasma. One advantage to using an inorganic material is that it has more flexibility with high temperature manufacture processes that in turn makes it possible to combine its use with conventional technology to deposit top layer(s) such as electrode. Another advantage is that inorganic materials have high heat diffusion capabilities. This allows high current operation of the resultant device with high reliability.

The active low conductive layer can be mixture of organic and inorganic materials. The inorganic material (transition metal oxide/sulfide) is usually embedded in an organic semiconductor material. Examples include polyphenylacetylene mixed with Cu_2S, polyphenylacetylene mixed with Cu_2O, and the like. This layer can be formed by economical methods. For example, one can spin on polyphenylacetylene dissolved with a Cu^+ salt such as copper styrene 4-sulfonate. The substrate can be a passive layer or facilitation layer. A CVD method then is used to introduce a reactive gas such as H_2S to react with Cu^+ to produce uniformly embedded Cu_2S. This type of organic-inorganic mixture material can have controlled initial conductivity by adjusting the copper ion concentration. Another advantage over pure organic materials is that organic-inorganic mixture materials can in some instances have good heat diffusion capabilities due to the presence of the inorganic material. Therefore, it can allow high current operation of the resultant device with good reliability.

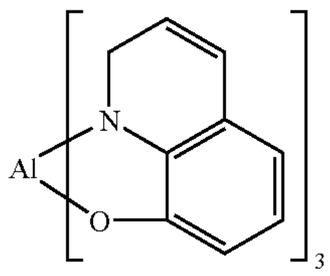
In one embodiment, the new memory cells contain both inorganic Cu_2O and an organic semiconductor material as

the active low conductive layer. In this embodiment, the Cu_2O is just above the passive layer and has a thickness from about 1 nm to about 3 nm. The organic semiconductor material is above the Cu_2O and has a thickness of about 0.001 μm or more and about 1 μm or less.

In one embodiment, the low conductive layer contains a thin layer designed to improve or lengthen charge retention time. The thin layer may be disposed anywhere within the low conductive layer, but typically near the middle of the layer. The thin layer contains any of the electrode materials or the compounds of the below-described heterocyclic/aromatic compound layer. In one embodiment, the thin layer has a thickness of about 50 Å or more and about 0.1 μm or less. In another embodiment, the thin layer has a thickness of about 100 Å or more and about 0.05 μm or less. For example, a memory cell may contain a first electrode of copper, a passive layer of copper sulfide, a low conductive layer of poly(phenylene vinylene), and a second electrode of aluminum, wherein the poly(phenylene vinylene) low conductor layer contains a 250 Å thick layer of copper therein.

In one embodiment, the organic semiconductor material does not contain an organometallic compound. In another embodiment, the organic semiconductor material contains an organic polymer doped with an organometallic compound. In yet another embodiment, the memory cells optionally contain an organometallic compound layer. In still yet another embodiment, the low conductive layer contains an organometallic compound. Examples of the chemical structures of various organometallic compounds include Formulae (XIV) to (XVII):

(XIV)



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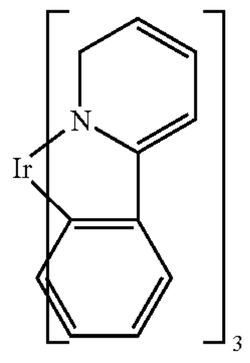

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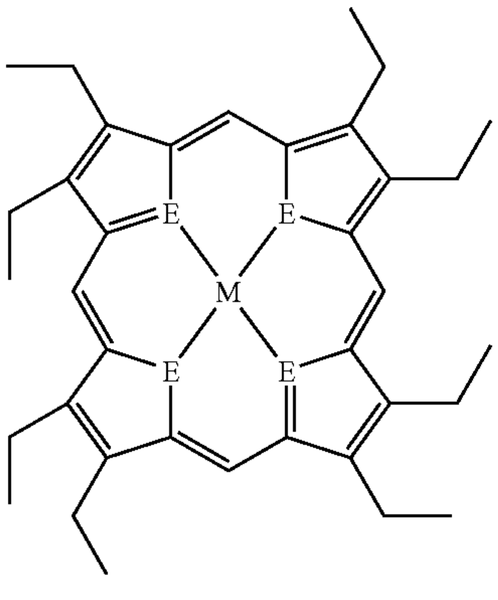

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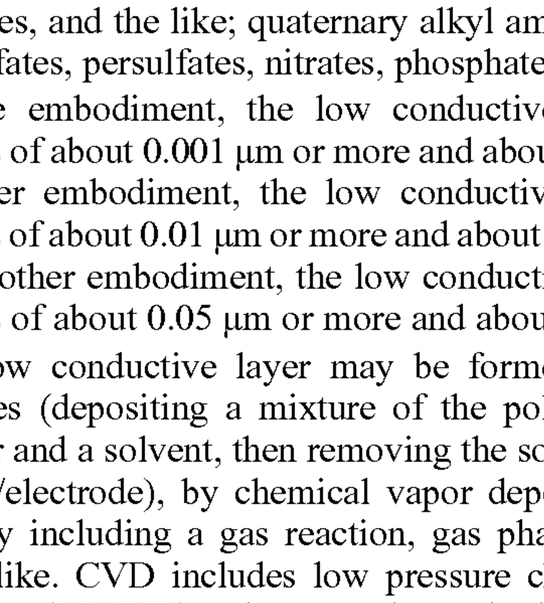

wherein M and E are as defined above.

In one embodiment, the low conductive layer is not doped with a salt. In another embodiment, the low conductive layer is doped with a salt. A salt is an ionic compound having an anion and cation. General examples of salts that can be employed to dope the low conductive layer include alkaline earth metal halogens, sulfates, persulfates, nitrates, phosphates, and the like; alkali metal halogens, sulfates, persulfates, nitrates, phosphates, and the like; transition metal halogens, sulfates, persulfates, nitrates, phosphates, and the like; ammonium halogens, sulfates, persulfates, nitrates, phosphates, and the like; quaternary alkyl ammonium halogens, sulfates, persulfates, nitrates, phosphates, and the like.

In one embodiment, the low conductive layer has a thickness of about 0.001 μm or more and about 5 μm or less. In another embodiment, the low conductive layer has a thickness of about 0.01 μm or more and about 2.5 μm or less. In yet another embodiment, the low conductive layer has a thickness of about 0.05 μm or more and about 1 μm or less.

The low conductive layer may be formed by spin-on techniques (depositing a mixture of the polymer/polymer precursor and a solvent, then removing the solvent from the substrate/electrode), by chemical vapor deposition (CVD) optionally including a gas reaction, gas phase deposition, and the like. CVD includes low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), and high density chemical vapor deposition (HDCVD). During formation or deposition, the low conductor material may self assemble between the electrodes. It is not typically necessary to functionalize one or more ends of an organic polymer in order to attach it to an electrode/passive layer.

A covalent bond may be formed between the low conductive material and the passive layer. Alternatively, close contact is required to provide good charge carrier/electron exchange between the low conductive layer and the passive layer. The low conductive layer and the passive layer are electrically coupled in that charge carrier/electron exchange occurs between the two layers.

A passive layer contains at least one conductivity facilitating compound that contributes to the controllably conductive properties of the controllably conductive media. The conductivity facilitating compound has the ability to donate and accept charges (holes and/or electrons). The passive layer thus may transport between an electrode and the low conductive layer/passive layer interface, facilitate charge/carrier injection into the low conductive layer, and/or increase the concentration of a charge carrier in the low conductive layer. In some instances, the passive layer may store opposite charges thereby providing a balance of

charges in the memory device as a whole. Storing charges/charge carriers is facilitated by the existence of two relatively stable oxidation states for the conductivity facilitating compound.

In other instances, the passive layer has ferroelectric behavior such as ionic displacement under external field. This often occurs at the junction with the active layer. The "ferroelectric" property results in the polarity effected by external field that significantly modifies the interface states and then changes conductivity of the memory cell. The memory cell made from this type of passive layer material has ionic-electronic conductive mechanism, and its data retention time is usually relatively longer because of the displacement of the metal ion at the interface. However, it is disadvantageous in some instances because it sometimes requires a longer time to switch the memory cell from one state to the other.

Generally, the conductivity facilitating compound or an atom in the conductivity facilitating compound has at least two relatively stable oxidation states. The two relatively stable oxidation states permit the conductivity facilitating compound to donate and accept charges and electrically interact with the low conductive layer. The particular conductivity facilitating compound employed in a given memory cell is selected so that the two relatively stable oxidation states match with the two relatively stable oxidation states of the low conductive material. Matching the energy bands of two relatively stable oxidation states of the low conductive material and the conductivity facilitating compound facilitate charge carrier retention in the low conductive layer.

Matching energy bands means that the Fermi level of the passive layer is close to the valence band of the active low conductive layer. Consequently, the injected charge carrier (into the active layer) may recombine with the charge at the passive layer if the energy band of the charged low conductive layer does not substantially change. Matching energy bands involves compromising between ease of charge injection and length of charge (data) retention time.

In one embodiment, when matching energy bands, the Fermi level of the passive layer is within about 0.7 eV of the valence band of the low conductive layer. In another embodiment, the Fermi level of the passive layer is within about 0.5 eV of the valence band of the low conductive layer. In yet another embodiment, the Fermi level of the passive layer is within about 0.3 eV of the valence band of the low conductive layer. In still yet another embodiment, the Fermi level of the passive layer is within about 0.15 eV of the valence band of the low conductive layer. The valence band, in some instances, is the highest occupied molecular orbital (HOMO) of the material.

The applied external field can reduce the energy barrier between passive layer and low conductive layer depending on the field direction. Therefore, enhanced charge injection in the forward direction field in programming operation and also enhanced charge recombination in reversed field in erase operation can be obtained.

The passive layer may in some instances act as a catalyst when forming the low conductive layer, particularly when the low conductive layer contains a conjugated organic polymer. In this connection, the polymer backbone of the conjugated organic polymer may initially form adjacent the passive layer, and grow or assemble away and substantially perpendicular to the passive layer surface. As a result, the polymer backbones of the conjugated organic polymers are self aligned in a direction that traverses the two electrodes.

Examples of conductivity facilitating compounds that may make up the passive layer include one or more of copper sulfide (Cu_xS, where x is from about 0.5 to about 3), silver sulfide (Ag_2S, AgS), gold sulfide (Au_2S, AuS), and the like. Among these materials, Cu_2S and Ag_2S may have ferroelectric properties, meaning metal ions have displacement under an external operation field. The passive layer may contain two or more sub-passive layers, each sub-layer containing the same, different, or multiple conductivity facilitating compounds.

The passive layer is grown using oxidation techniques, formed via gas phase reactions, or deposited between the electrodes. In some instances, to promote long charge retention times (in the low conductive layer), the passive layer may be treated with a plasma after it is formed. The plasma treatment modifies the energy barrier of the passive layer.

In one embodiment, the passive layer containing the conductivity facilitating compound has a thickness of about 2 Å or more and about 0.1 μm or less. In another embodiment, the passive layer has a thickness of about 10 Å or more and about 0.01 μm or less. In yet another embodiment, the passive layer has a thickness of about 50 Å or more and about 0.005 μm or less.

In order to facilitate manufacture and operation of the new memory cells, the active low conductive layer is thicker than the passive layer. In one embodiment, the thickness of the low conductive layer is from about 10 to about 500 times greater than the thickness of the passive layer. In another embodiment, the thickness of the low conductive layer is from about 25 to about 250 times greater than the thickness of the passive layer.

In one embodiment, the new memory cells optionally contain a heterocyclic/aromatic compound layer. In another embodiment, the low conductive layer is doped with a heterocyclic/aromatic compound. If present, the heterocyclic/aromatic compound layer has a thickness of about 0.001 μm or more and about 1 μm or less. Examples of the chemical structures of various heterocyclic/aromatic compounds specifically including nitrogen containing heterocycles, include Formulae (XVIII) to (XXIII):

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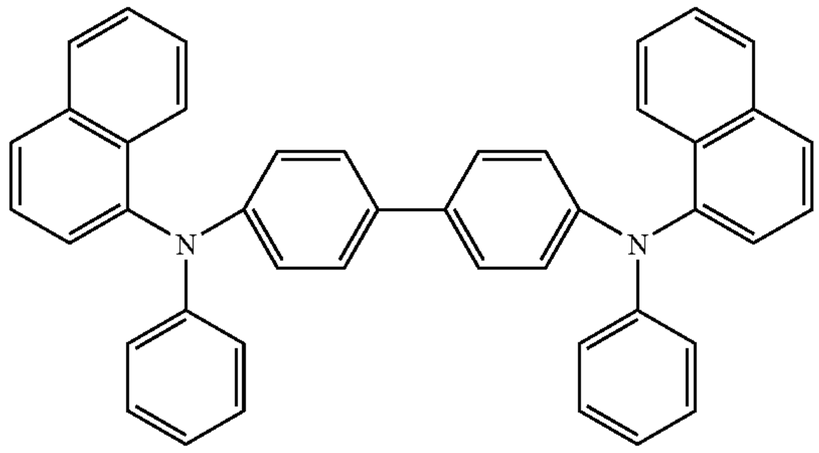

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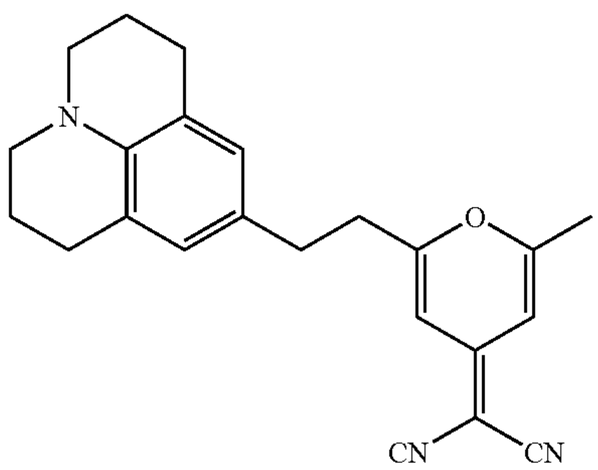

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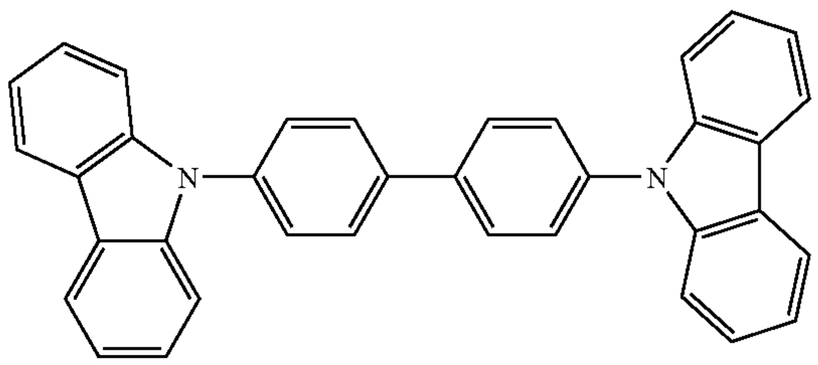

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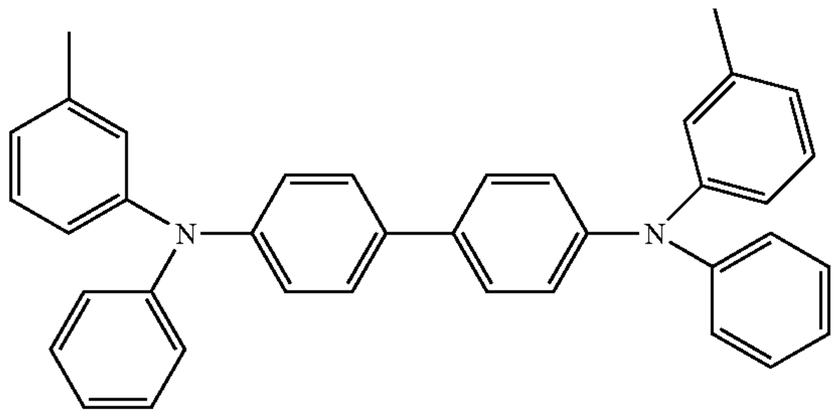

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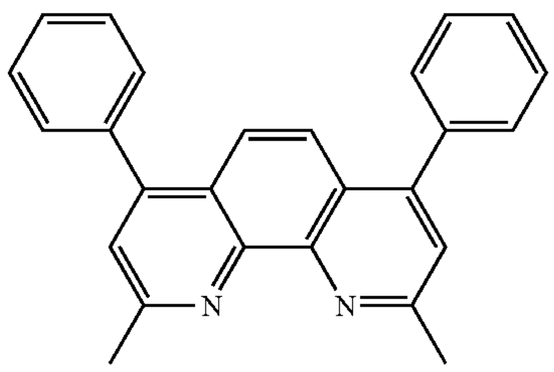

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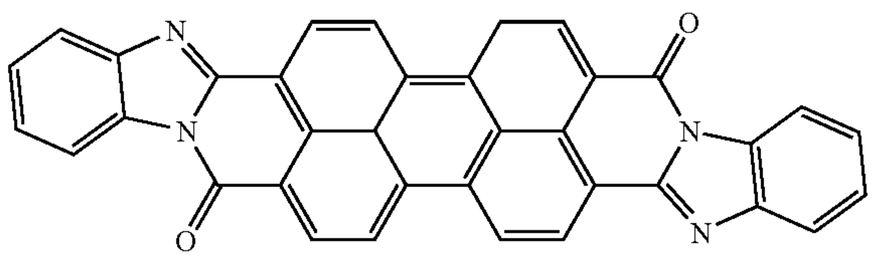

The area size of the individual memory cells (as measured by the surface area of the two electrodes directly overlapping each other) can be small compared to conventional silicon based memory cells such as MOSFETs. In one embodiment, the area size of the memory cells of the present invention is about 0.0001 μm^2 or more and about 4 μm^2 or less. In another embodiment, the area size of the memory cells is about 0.001 μm^2 or more and about 1 μm^2 or less.

Operation of the new memory devices/cells is facilitated using an external stimuli to achieve a switching effect. The external stimuli include an external electric field and/or light radiation. Under various conditions, the memory cell is either conductive (low impedance or "on" state) or non-conductive (high impedance or "off" state).

The memory cell may further have more than one conductive or low impedance state, such as a very highly conductive state (very low impedance state), a highly conductive state (low impedance state), a conductive state (medium level impedance state), and a non-conductive state (high impedance state) thereby enabling the storage of multiple bits of information in a single memory cell, such as 2 or more bits of information or 4 or more bits of information.

Switching the memory cell to the "on" state from the "off" state occurs when an external stimuli such as an applied electric field exceeds a threshold value. Switching the memory cell to the "off" state from the "on" state occurs when an external stimuli does not exceed a threshold value or does not exist. The threshold value varies depending upon a number of factors including the identity of the materials that constitute the memory cell, the low conductive layer, and the passive layer, the thickness of the various layers, and the like.

Generally speaking, the presence of an external stimuli such as an applied electric field that exceeds a threshold value ("on" state) permits an applied voltage to write or erase information into/from the memory cell and the presence of an external stimuli such as an applied electric field that is less than a threshold value permits an applied voltage to read information from the memory cell; whereas the absence of the external stimuli that exceeds a threshold value ("off" state) prevents an applied voltage to write or erase information into/from the memory cell.

To write information into the memory cell, a voltage or pulse signal that exceeds the threshold is applied. To read information written into the memory cell, a voltage or electric field of any polarity is applied. Measuring the impedance determines whether the memory cell is in a low impedance state or a high impedance state (and thus whether it is "on" or "off"). To erase information written into the memory cell, a negative voltage or a polarity opposite the polarity of the writing signal that exceeds a threshold value is applied.

The memory devices described herein can be employed to form logic devices such as central processing units (CPUs); volatile memory devices such as DRAM devices, SRAM devices, and the like; input/output devices (I/O chips); and non-volatile memory devices such as EEPROMs, EPROMs, PROMs, and the like. The memory devices may be fabricated in planar orientation (two dimensional) or three dimensional orientation containing at least two planar arrays of the memory cells.

Referring to FIG. **2**, a three dimensional microelectronic memory device **200** containing a plurality of memory cells in accordance with an aspect of the invention is shown. The three dimensional microelectronic memory device **200** contains a plurality of first electrodes **202**, a plurality of second electrodes **204**, and a plurality of memory cell layers **206**. Between the respective first and second electrodes are the controllably conductive media (not shown). The plurality of first electrodes **202** and the plurality of second electrodes **204** are shown in substantially perpendicular orientation, although other orientations are possible. The three dimensional microelectronic memory device is capable of containing an extremely high number of memory cells thereby improving device density. Peripheral circuitry and devices are not shown for brevity.

The Memory cells/devices are useful in any device requiring memory. For example, the memory devices are useful in computers, appliances, industrial equipment, hand-held devices, telecommunications equipment, medical equipment, research and development equipment, transportation vehicles, radar/satellite devices, and the like. Hand-held devices, and particularly hand-held electronic devices, achieve improvements in portability due to the small size and light weight of the new memory devices. Examples of hand-held devices include cell phones and other two way communication devices, personal data assistants, palm pilots, pagers, notebook computers, remote controls, recorders (video and audio), radios, small televisions and web viewers, cameras, and the like.

The following examples illustrate the present invention. Unless otherwise indicated in the following examples and elsewhere in the specification and claims, all parts and percentages are by weight, all temperatures are in degrees Centigrade, and pressure is at or near atmospheric pressure.

EXAMPLE 1

Memory cells are formed using an upper electrode of ITO having a thickness of 2,000 Å and a lower electrode of silver having a thickness of 1,000 Å. A passive layer of silver sulfide having a thickness of 50 Å is provided over the lower electrode. An organic semiconductor layer containing polyphenylacetylene and having a thickness of 800 Å is formed over the passive layer using CVD techniques. The upper electrode is then affixed over the polymer layer.

EXAMPLE 2

Memory cells are formed using an upper electrode of copper having a thickness of 1,000 Å and a lower electrode of copper having a thickness of 1,000 Å. A passive layer of copper sulfide having a thickness of 70 Å is provided over the lower electrode. A Cu_2O as a first active layer having a thickness of 2 nm is formed over the copper sulfide using a thermal heating technique. An organic polymer layer containing polyacetylene and having a thickness of 900 Å as a second active layer is formed over the Cu_2O first active layer using CVD techniques. The upper electrode is then affixed over the polymer layer.

EXAMPLE 3

Memory cells are formed using an upper electrode of aluminum having a thickness of 1,500 Å and a lower electrode of copper having a thickness of 1,000 Å. A passive layer of copper sulfide having a thickness of 65 Å is provided over the lower electrode. An organic semiconductor layer containing polyphenylacetylene and having a thickness of 700 Å is formed over the passive layer using CVD techniques. The upper electrode is then affixed over the polymer layer.

EXAMPLE 4

Memory cells are formed using an upper electrode of copper having a thickness of 1,500 Å and a lower electrode of copper having a thickness of 1,000 Å. A passive layer of copper sulfide having a thickness of 25 Å is provided over the lower electrode. An organic semiconductor layer containing polythiophene with Cu_2S nanoparticles embedded therein and having a thickness of 700 Å is formed over the passive layer using spin-on and CVD techniques. The upper electrode is then affixed over the polymer layer.

Although the invention has been shown and described with respect to a certain preferred embodiment or embodiments, it is obvious that equivalent alterations and modifications will occur to others skilled in the art upon the reading and understanding of this specification and the annexed drawings. In particular regard to the various functions performed by the above described components (assemblies, devices, circuits, etc.), the terms (including any reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (i.e., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary embodiments of the invention. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several embodiments, such feature may be combined with one or more other features of the other embodiments as may be desired and advantageous for any given or particular application.

What is claimed is:

1. A method of making a memory cell comprising:

providing a first electrode;

forming a passive layer comprising a conductivity facilitating compound over the first electrode, the passive layer having an ability to donate and accept at least one of holes and electrons;

forming a low conductive layer comprising a conjugated organic polymer over the passive layer, wherein the conductivity facilitating compound of the passive layer is selected, the low conductive layer having an ability to donate and accept at least one of holes and electrons, the low conductive layer selected so that the passive layer has a Fermi level within about 0.7 eV of a valence band of the low conductive layer, the conjugated organic polymer is formed by chemical vapor deposition and a catalytic action of the passive layer; and

providing a second electrode over the low conductive layer.

2. The method of claim **1**, wherein the conductivity facilitating compound comprises at least one selected from the group consisting of copper sulfide, silver sulfide, and gold sulfide.

3. The method of claim **1**, wherein the passive layer has a thickness from about 2 Å to about 0.1 μm.

4. The method of claim **1**, wherein the low conductive layer has a thickness from about 0.001 μm to about 5 μm.

5. The method of claim **1**, wherein the passive layer acts as a catalyst when forming the low conductive layer.

6. The method of claim **1**, wherein the low conductive layer comprises a conjugated organic polymer.

7. The method of claim **1**, wherein the passive layer has a Fermi level within about 0.5 eV of a valence band of the low conductive layer.

8. The method of claim **1**, wherein the memory cell has a size area of about 0.0001 μm^2 or more and about 4 μm^2 or less.

9. The method of claim **1**, wherein the passive layer has a Fermi level within about 0.3 eV of a valence band of the low conductive layer.

10. The method of claim **1**, wherein the conductivity facilitating compound comprises copper sulfide.

11. The method of claim **1**, wherein the low conductive layer comprises a polyacetylene.

12. The method of claim **1**, wherein the low conductive layer comprises a polyphenylacetylene.

13. The method of claim **1**, wherein the low conductive layer comprises a polydiphenylacetylene.

14. The method of claim **1**, wherein the low conductive layer comprises a polyaniline.

15. The method of claim **1**, wherein the low conductive layer comprises a poly(p-phenylene vinylene).

16. The method of claim **1**, wherein the low conductive layer comprises a polythiophene.

17. The method of claim **1**, wherein the low conductive layer comprises a polyporphyrin.

18. The method of claim **1**, wherein the low conductive layer comprises a polyvinylene.

19. The method of claim **1**, wherein the low conductive layer comprises a polystirole.

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