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Logothetis

(10) **Patent No.: US 7,250,827 B2**
(45) **Date of Patent: Jul. 31, 2007**

(54) **CIRCUITRY MODULE**

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(73) Assignee: **Merrimac Industries, Inc.**, West Caldwell, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 2 days.

(21) Appl. No.: **11/077,935**

(22) Filed: **Mar. 11, 2005**

(65) **Prior Publication Data**

US 2005/0219009 A1 Oct. 6, 2005

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/659,542, filed on Sep. 10, 2003, now Pat. No. 7,042,307.

(51) **Int. Cl.**
H01P 5/12 (2006.01)
H03H 7/00 (2006.01)
H03H 7/38 (2006.01)

(52) **U.S. Cl.** **333/26**; 333/32

(58) **Field of Classification Search** 333/26, 333/32, 116, 117, 124, 125
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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* cited by examiner

Primary Examiner—Dean Takaoka
(74) *Attorney, Agent, or Firm*—Drew Wintringham, Esq.; Clifford Chance US LLP

(57) **ABSTRACT**

A circuit assembly includes multiple substrate with a regions of embedded signal processing circuitry can be connected to a region of adjustable signal processing circuitry and a cavity formed through an area of the substrate layers to expose signal connection terminals. These signal connection terminals are connected to the embedded signal processing circuitry and/or to the customizable circuitry and enables the addition of a circuit element to the assembly after the bonding of the substrate layers and enables the connection of that added element to the signal processing circuitry and to the adjustable processing circuitry.

18 Claims, 29 Drawing Sheets

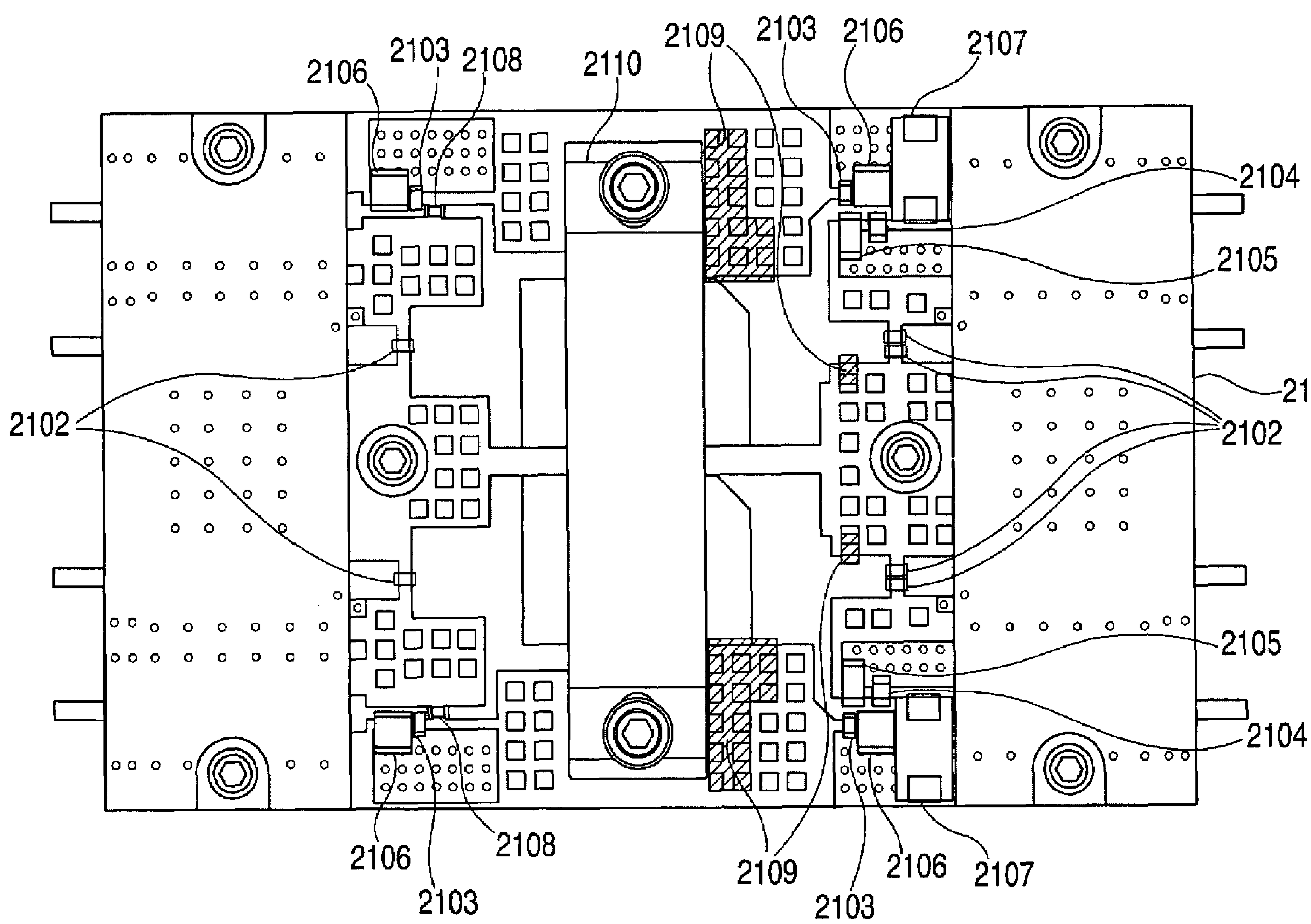
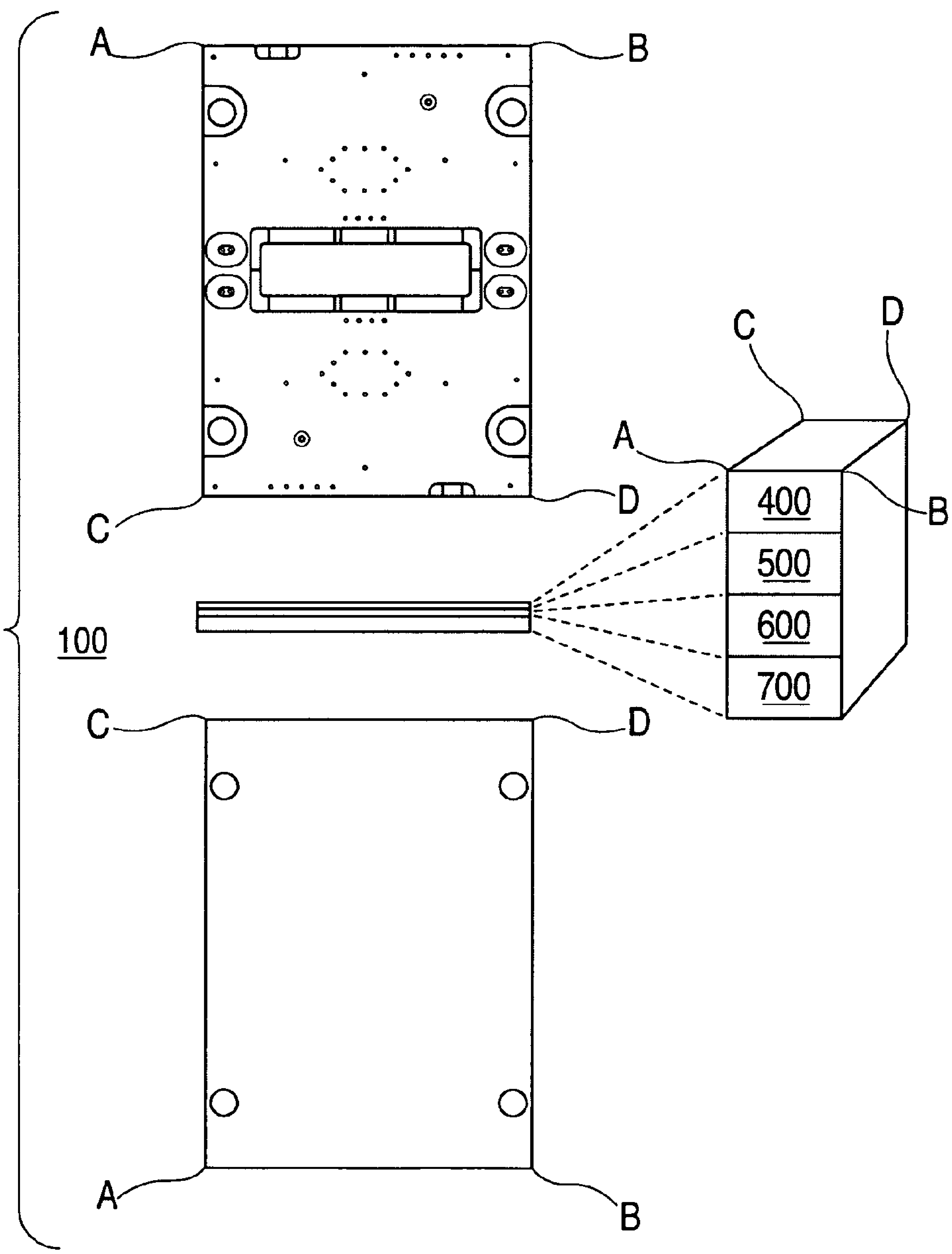
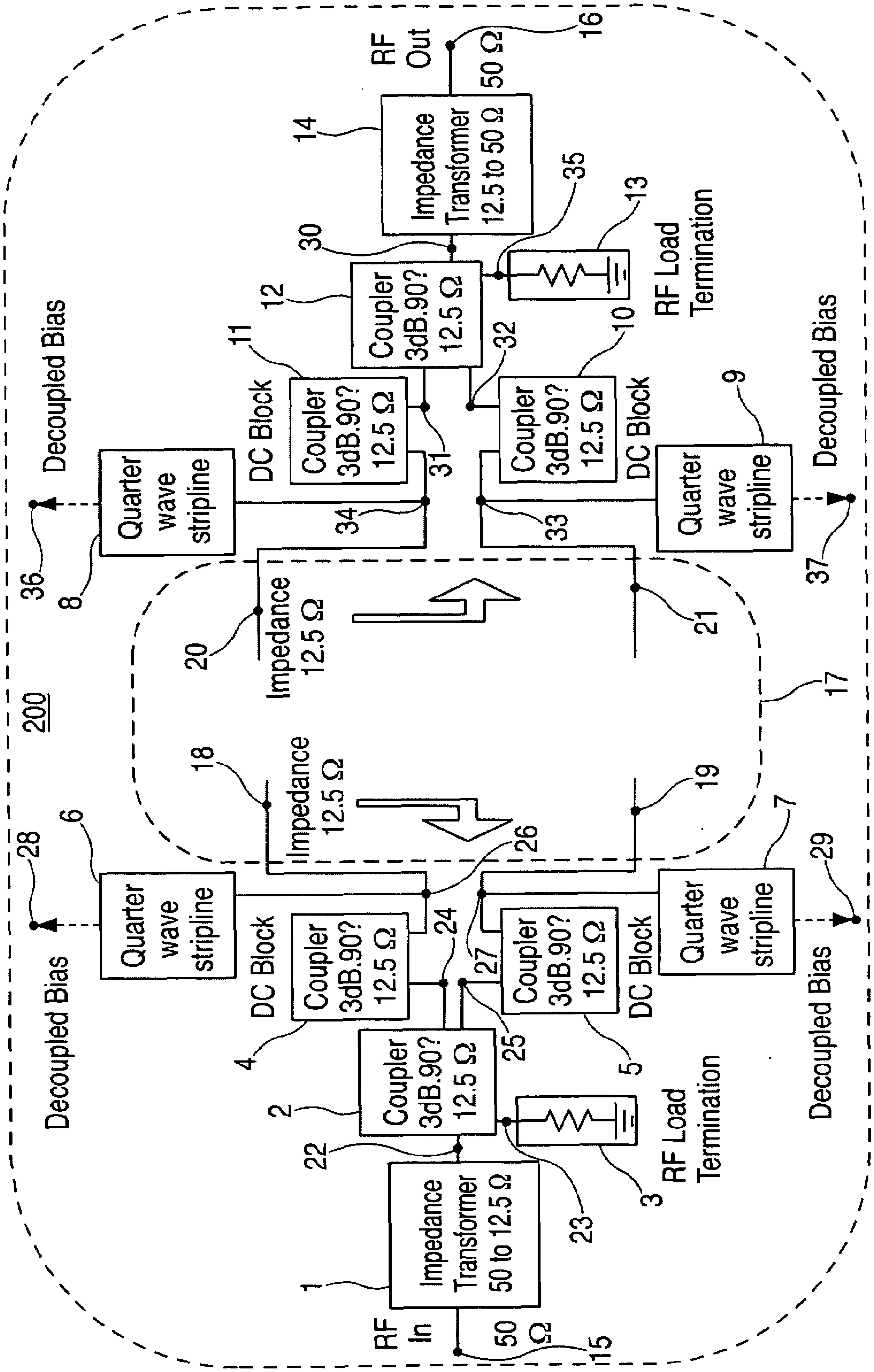


FIG. 1




200
RF In
50 Ω
15
1
Impedance Transformer 50 to 12.5 Ω
22
2
Coupler 3dB.90? 12.5 Ω
23
3
RF Load Termination
4
Coupler 3dB.90? 12.5 Ω
DC Block
5
Coupler 3dB.90? 12.5 Ω
DC Block
24
25
26
27
6
Quarter wave stripline
28
Decoupled Bias
7
Quarter wave stripline
29
Decoupled Bias
18
Impedance 12.5 Ω
19
20
Impedance 12.5 Ω
21
17
8
Quarter wave stripline
36
Decoupled Bias
9
Quarter wave stripline
37
Decoupled Bias
34
33
31
32
11
Coupler 3dB.90? 12.5 Ω
DC Block
10
Coupler 3dB.90? 12.5 Ω
DC Block
12
Coupler 3dB.90? 12.5 Ω
30
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13
RF Load Termination
14
Impedance Transformer 12.5 to 50 Ω
RF Out
50 Ω
16

FIG. 2

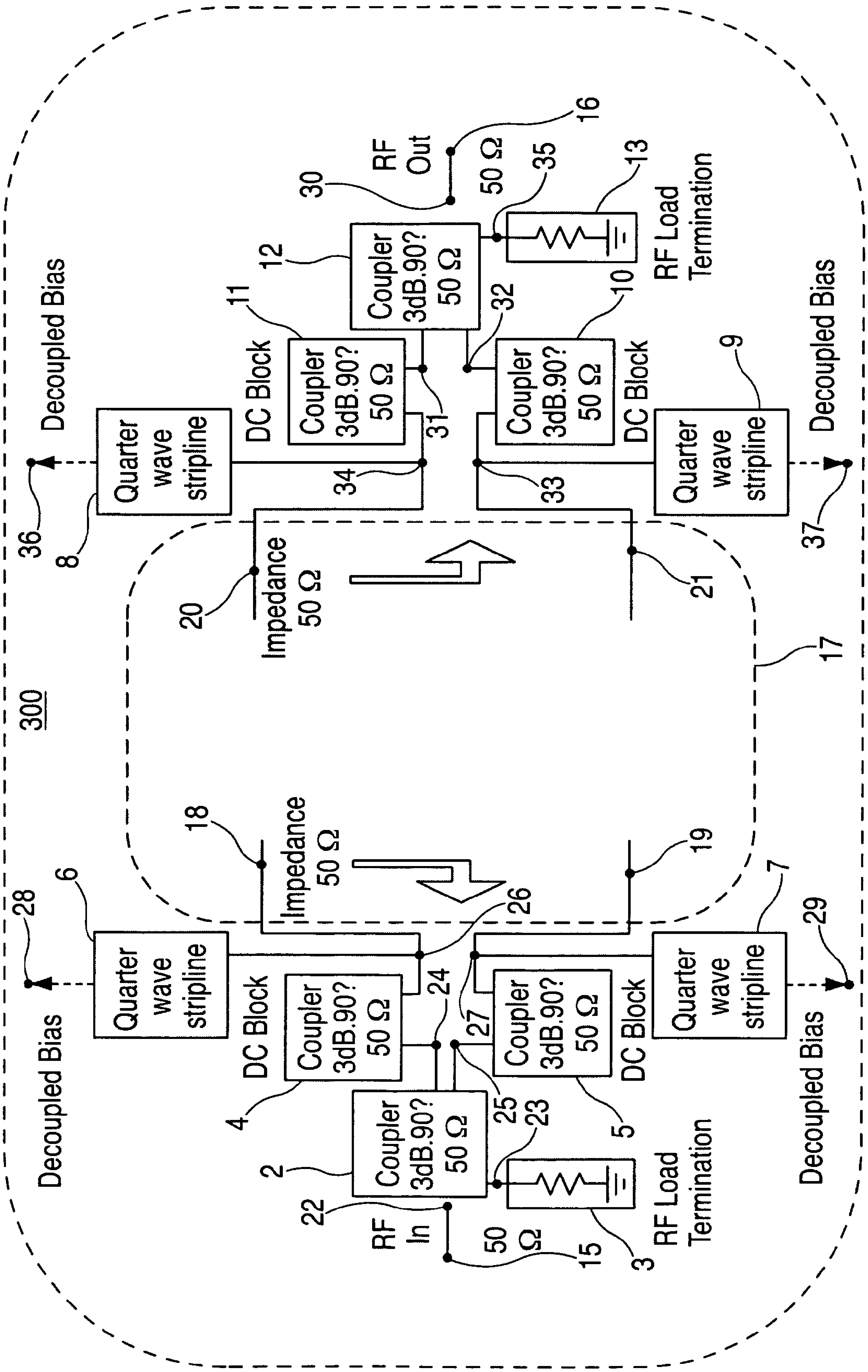
300
RF In
50 Ω
Coupler 3dB.90? 50 Ω
RF Load Termination
DC Block
Quarter wave stripline
Decoupled Bias
Impedance 50 Ω
RF Out
2
3
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FIG. 3

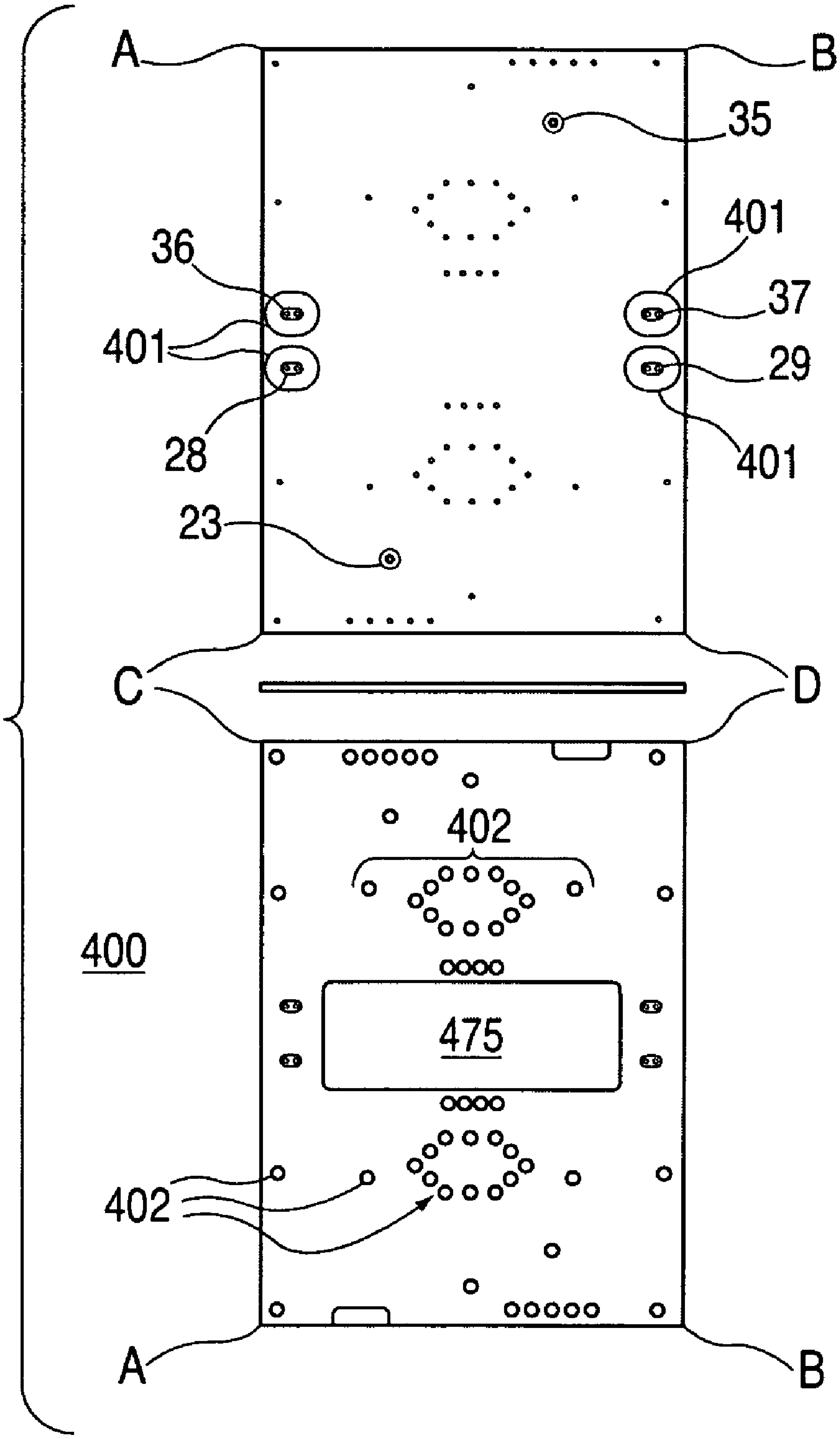
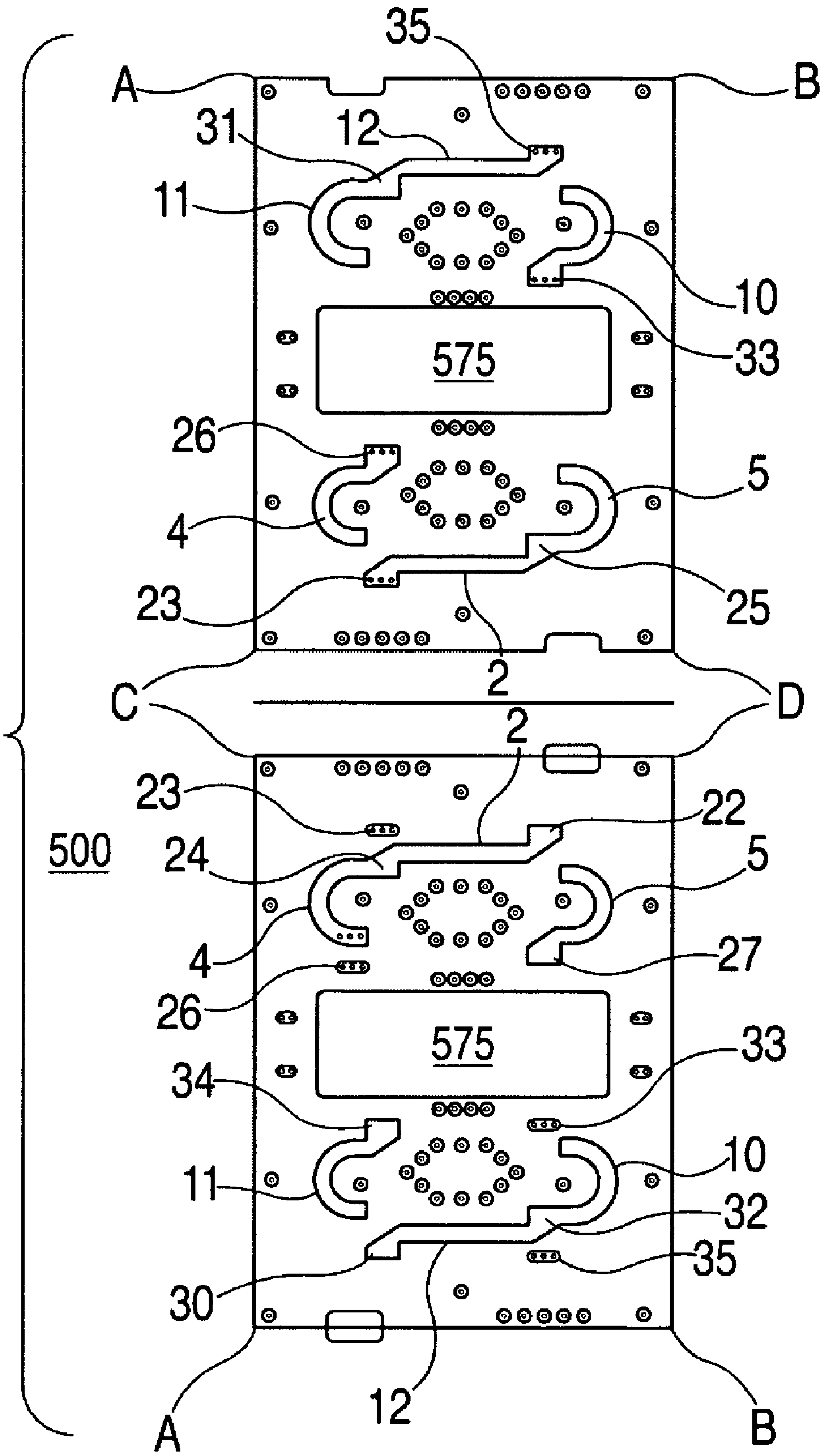


FIG. 4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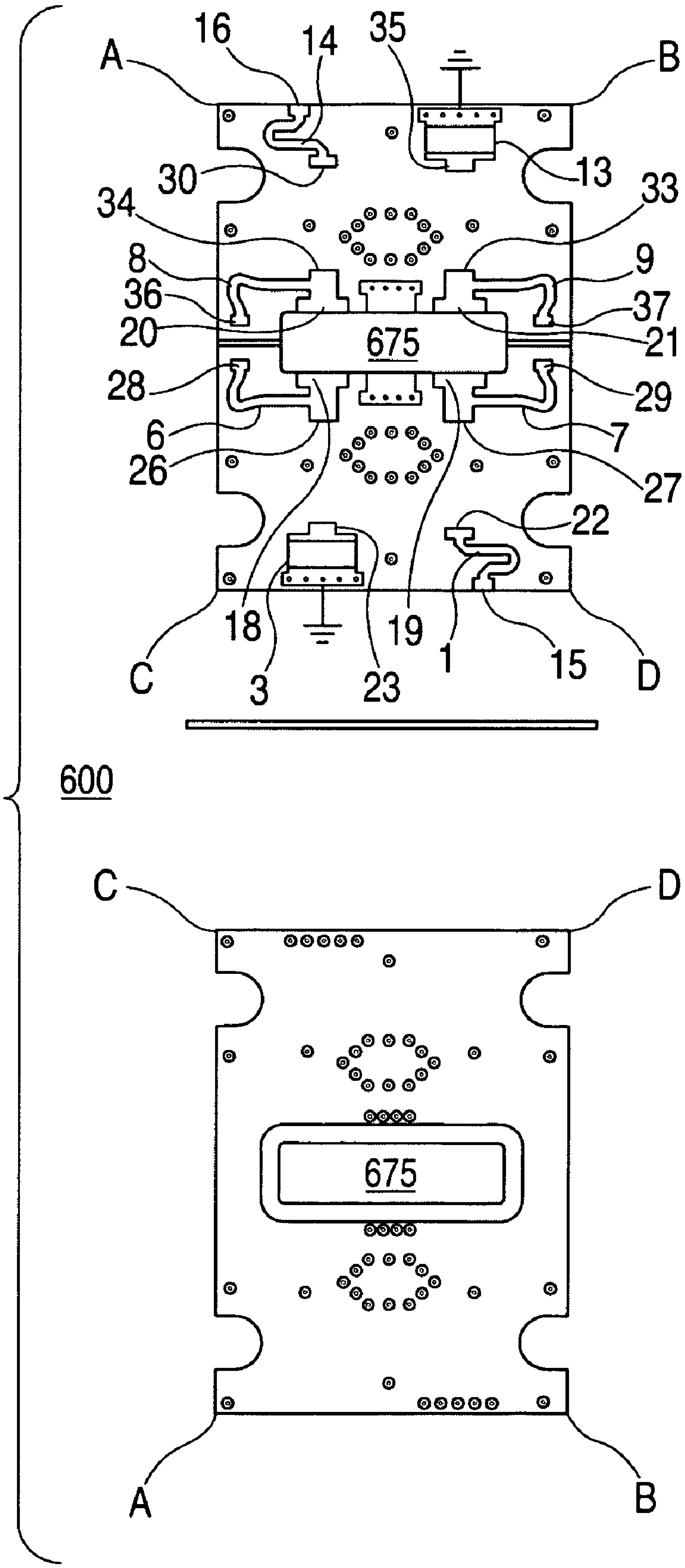
A
B
31
12
11
10
33
575
26
5
4
23
25
2
C
D
2
23
22
500
24
5
4
27
26
575
33
34
10
11
32
35
30
A
12
B

FIG. 5


A
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B
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9
36
37
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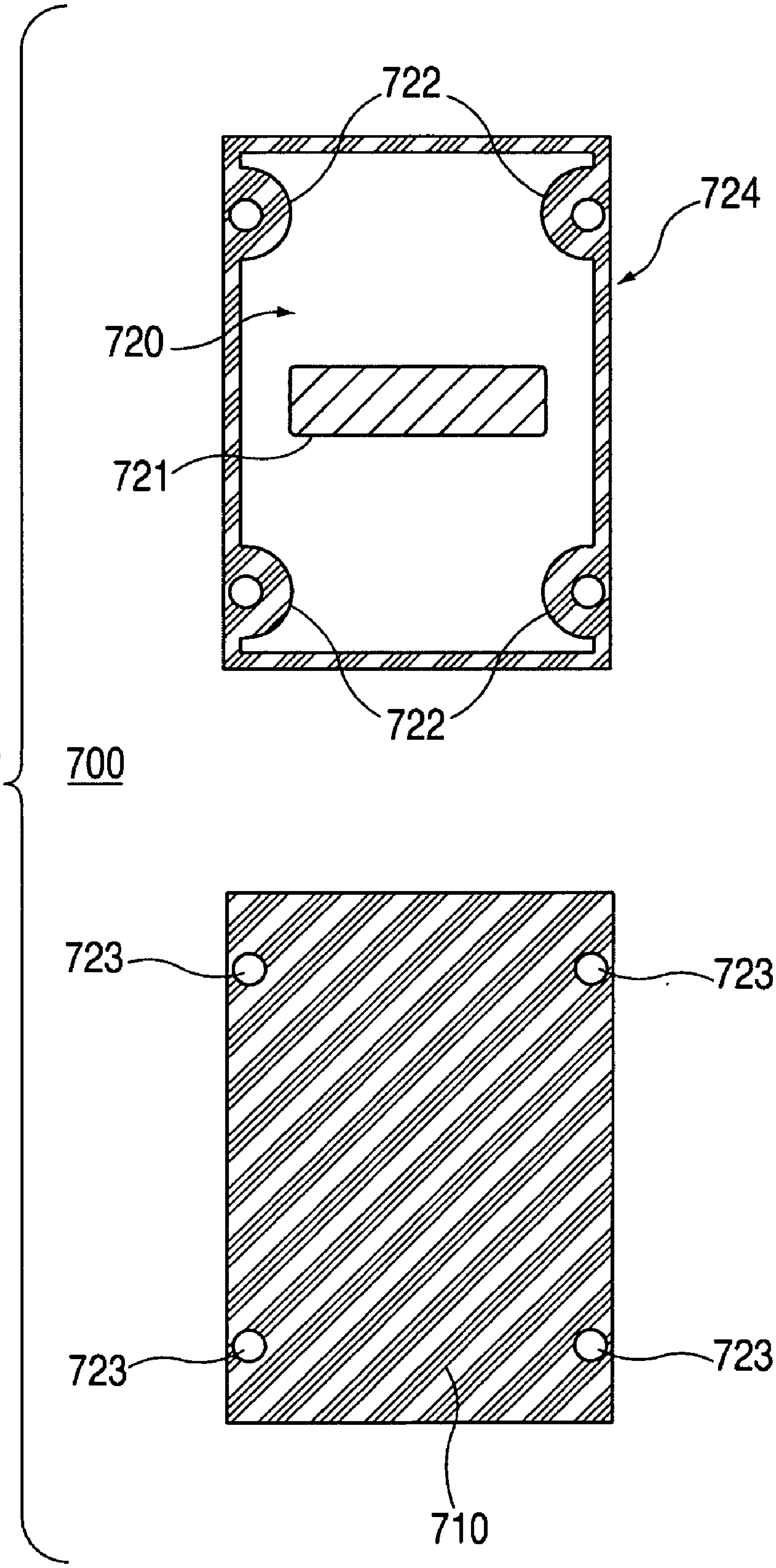
7
26
27
22
18
19
C
3
23
1
15
D
600
C
D
675
A
B

FIG. 6

FIG. 7



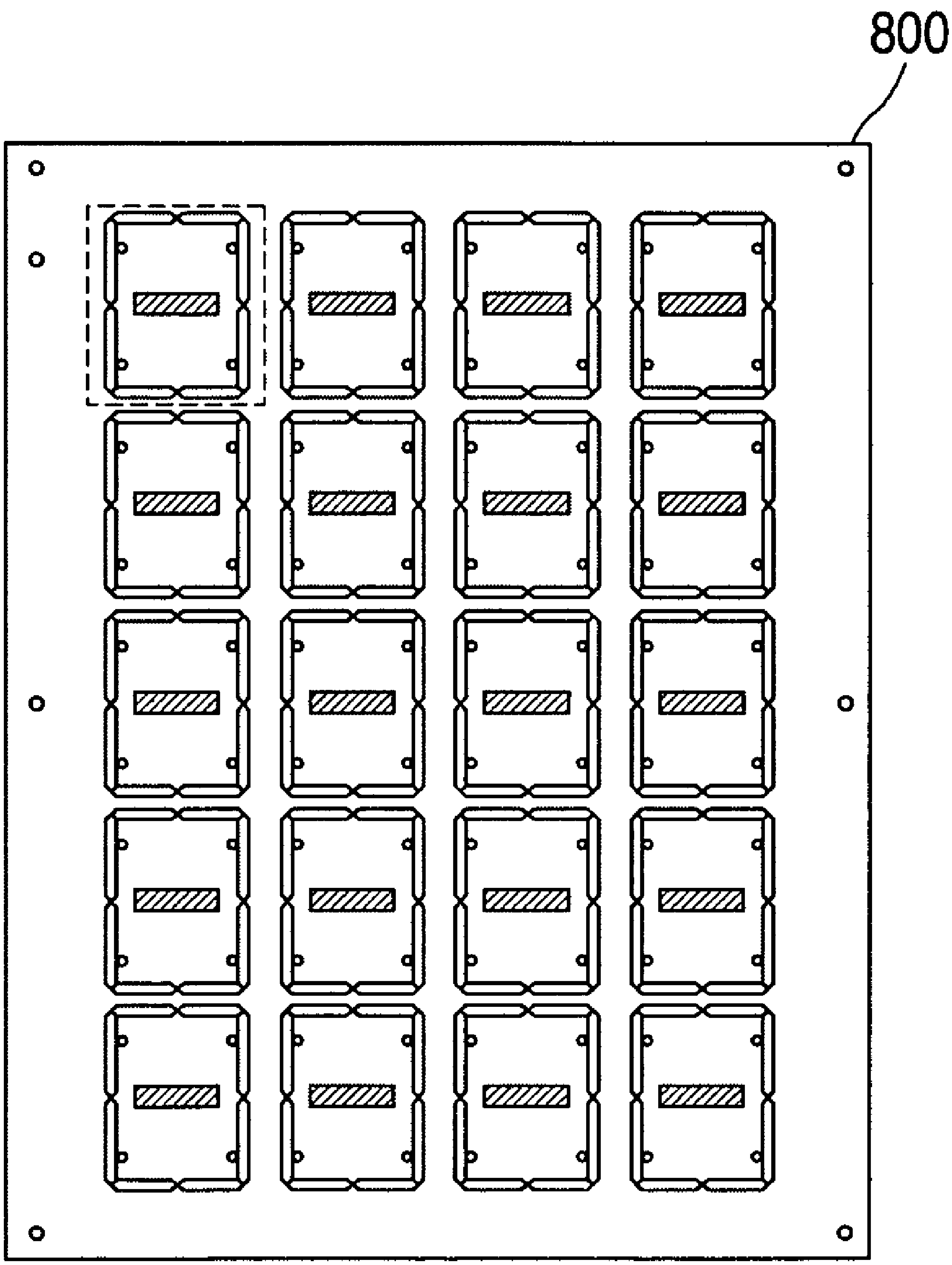


FIG. 8

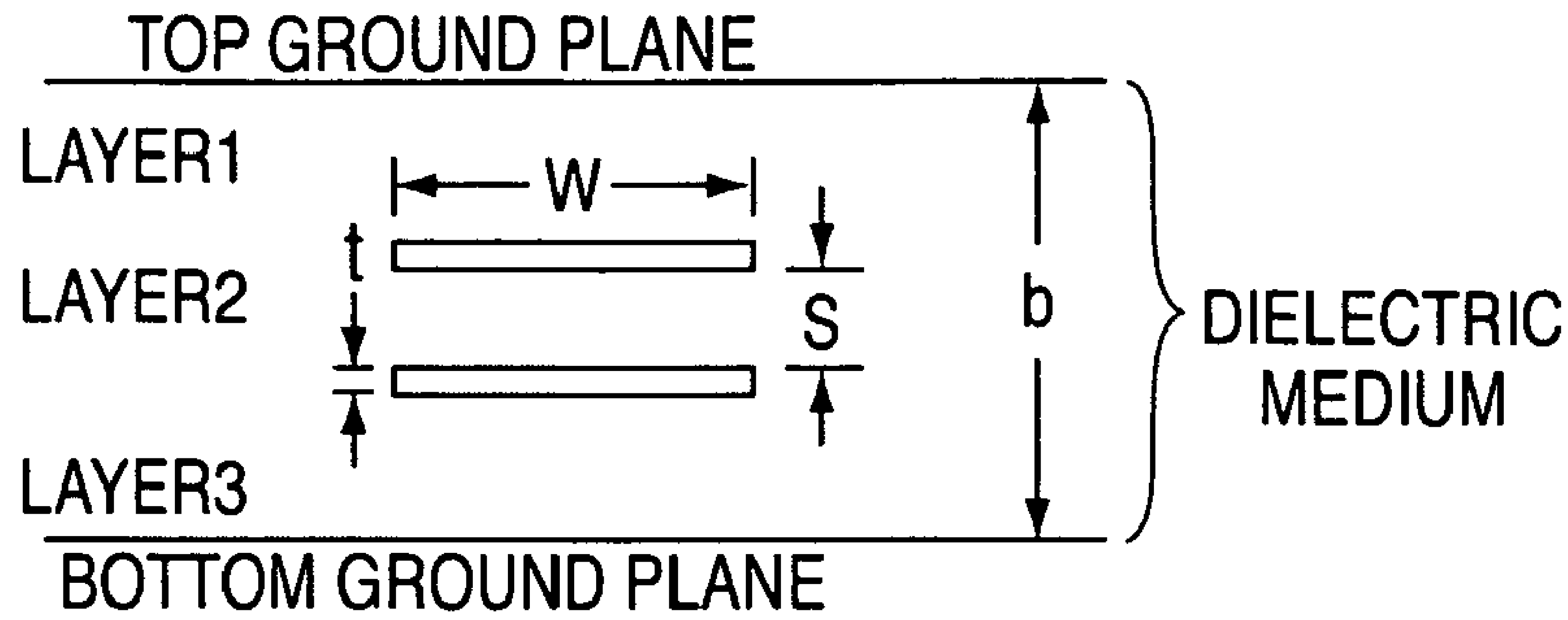


FIG. 9

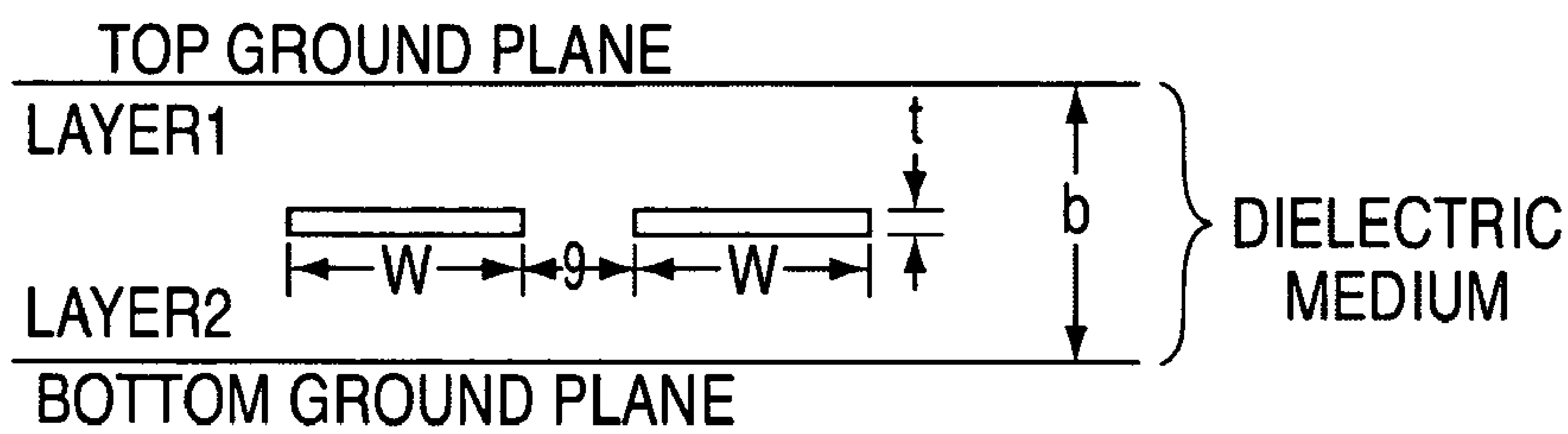


FIG. 10

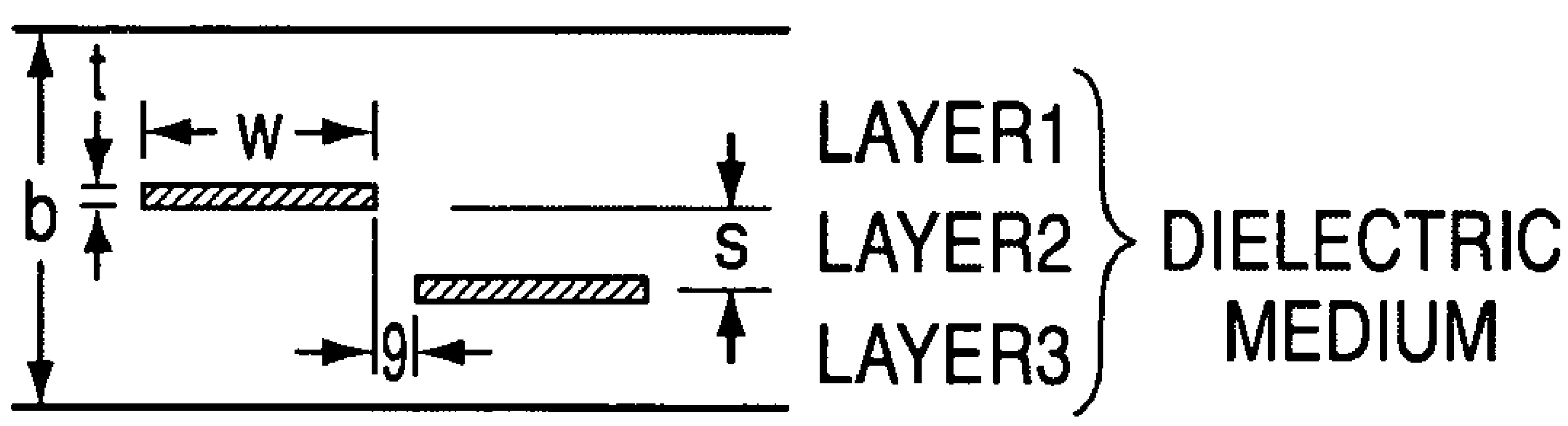


FIG. 11

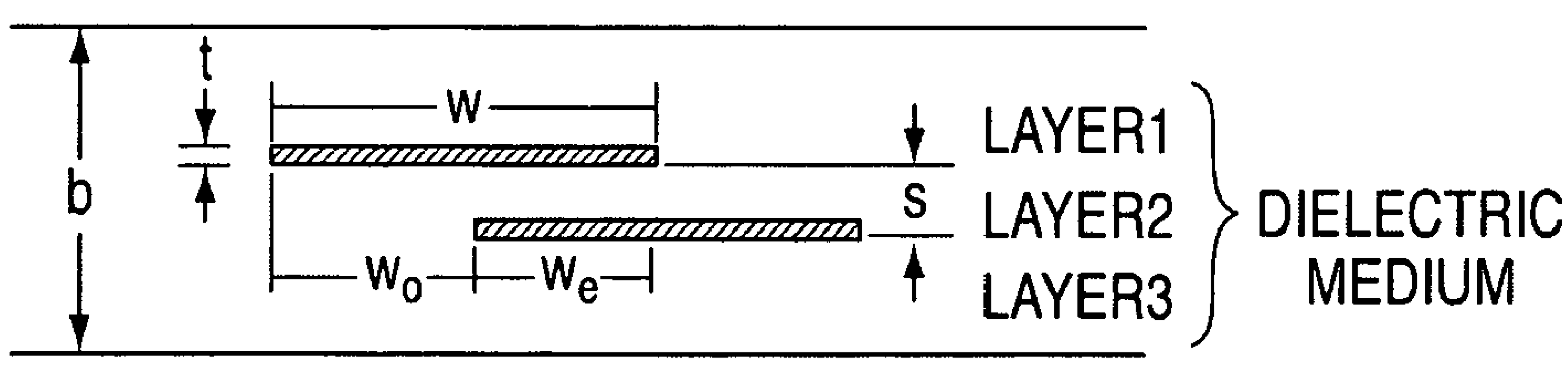


FIG. 12

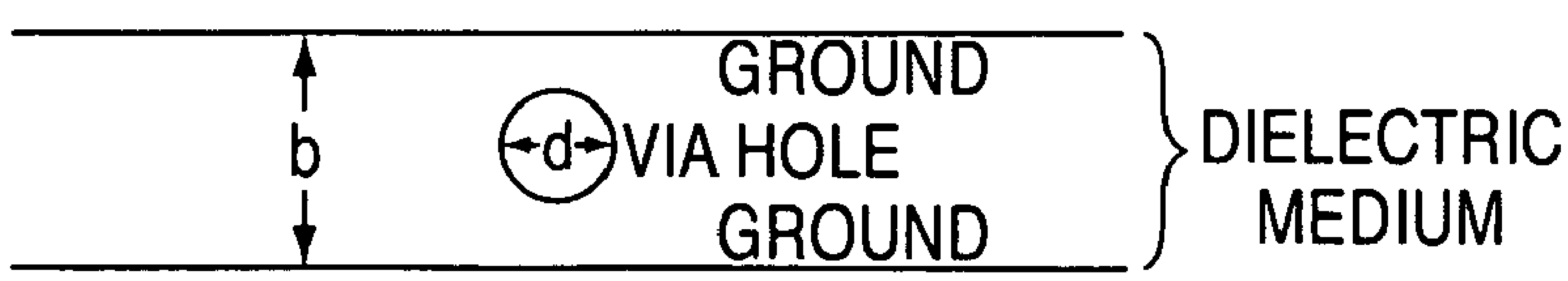
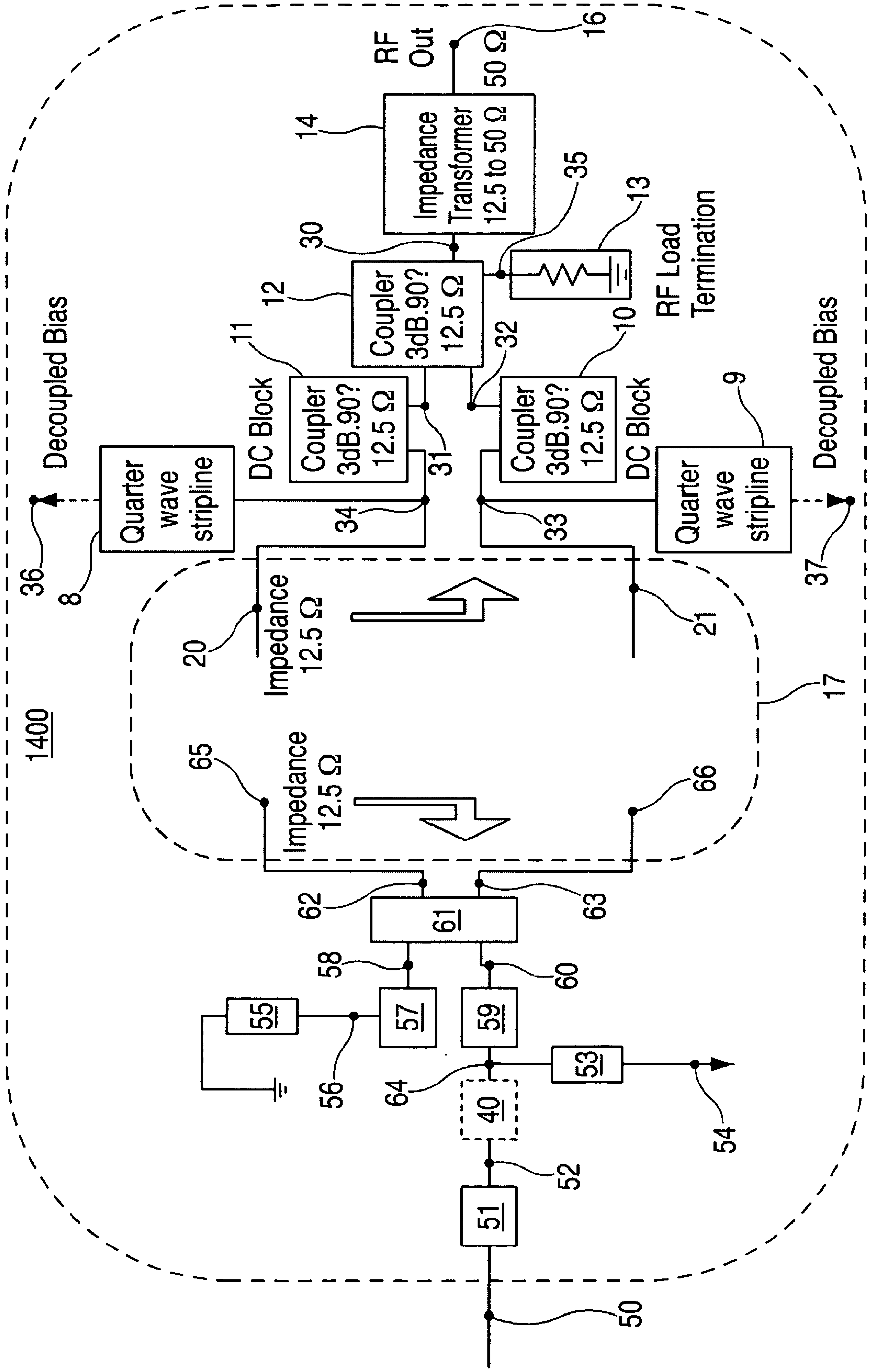


FIG. 13



RF Out
16
50 Ω
14
Impedance Transformer 12.5 to 50 Ω
35
13
30
RF Load Termination
12
Coupler 3dB.90? 12.5 Ω
11
32
10
Decoupled Bias
DC Block
Coupler 3dB.90? 12.5 Ω
Coupler 3dB.90? 12.5 Ω
DC Block
9
Decoupled Bias
31
Quarter wave stripline
Quarter wave stripline
34
33
36
8
37
20
Impedance 12.5 Ω
21
1400
17
65
Impedance 12.5 Ω
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FIG. 14

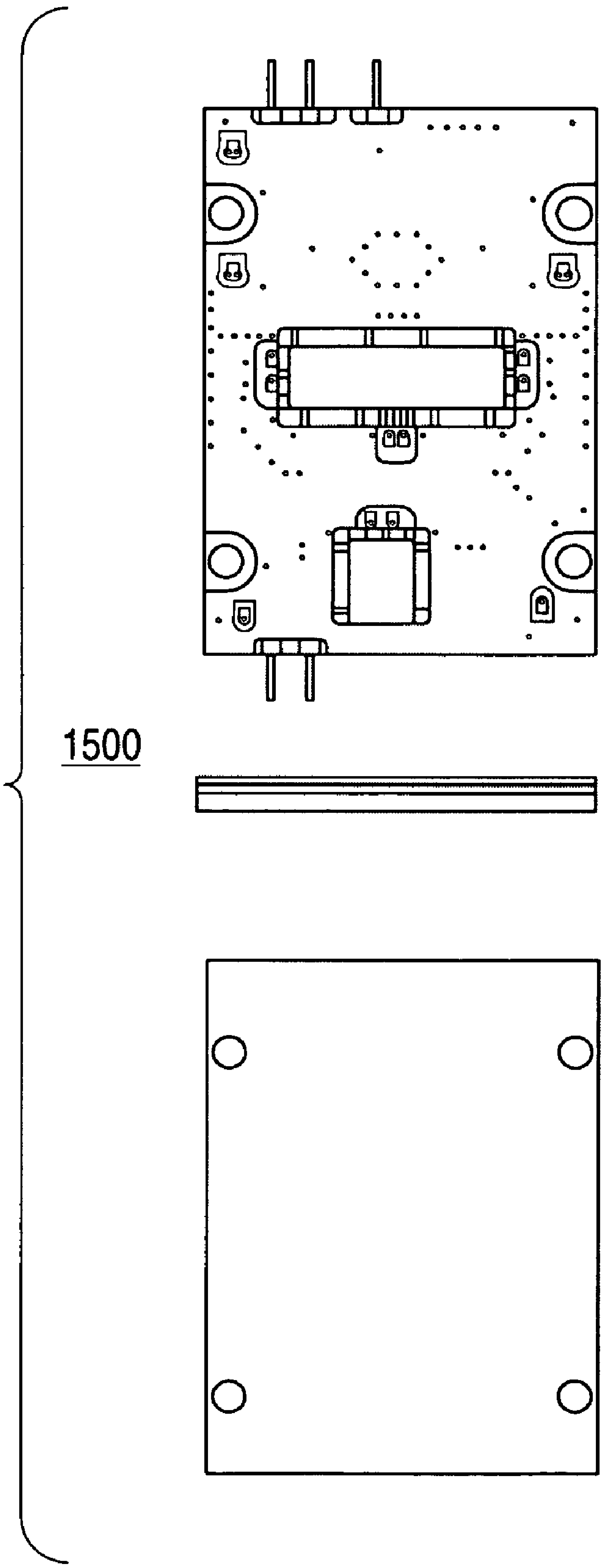


FIG. 15

FIG. 16

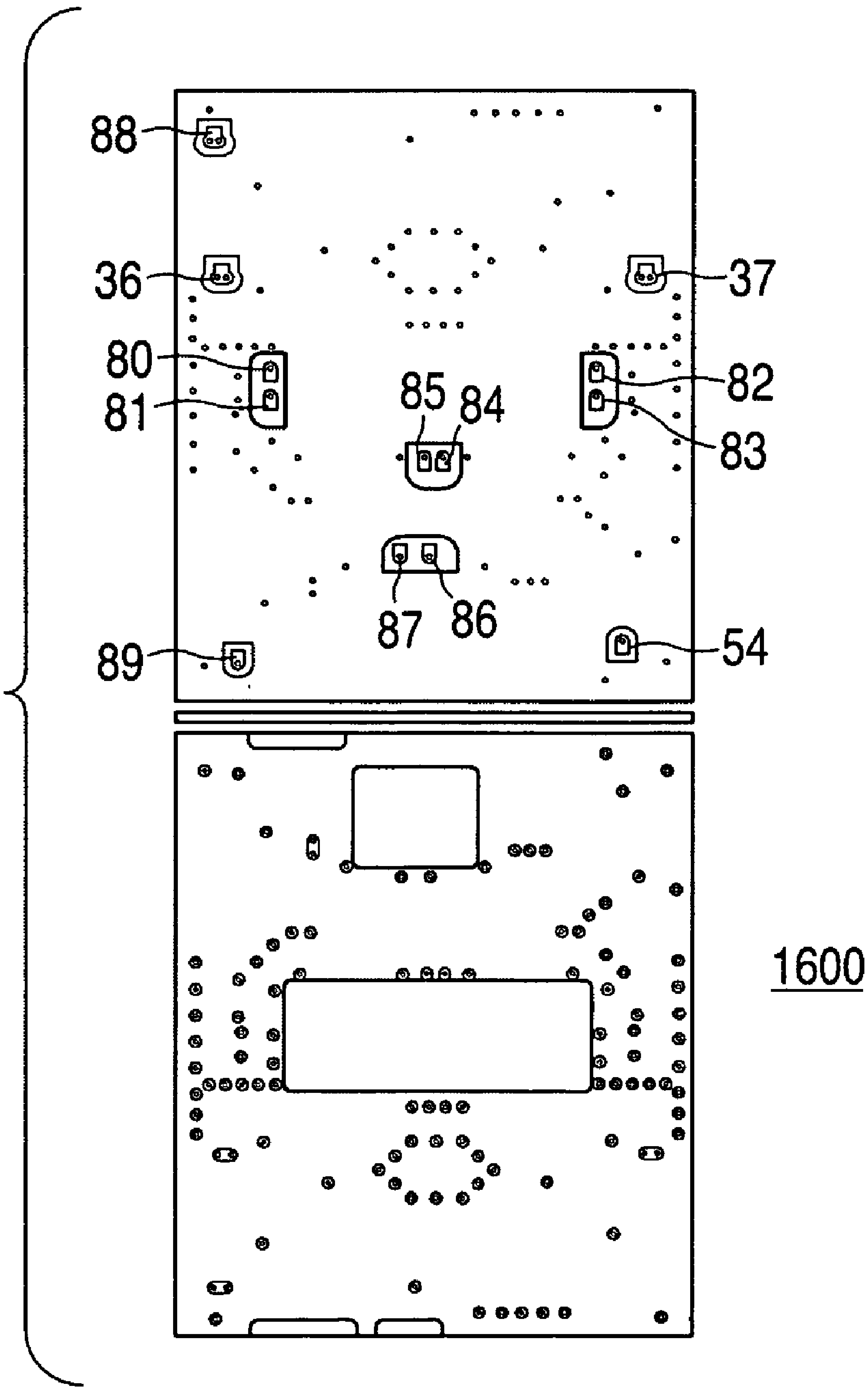
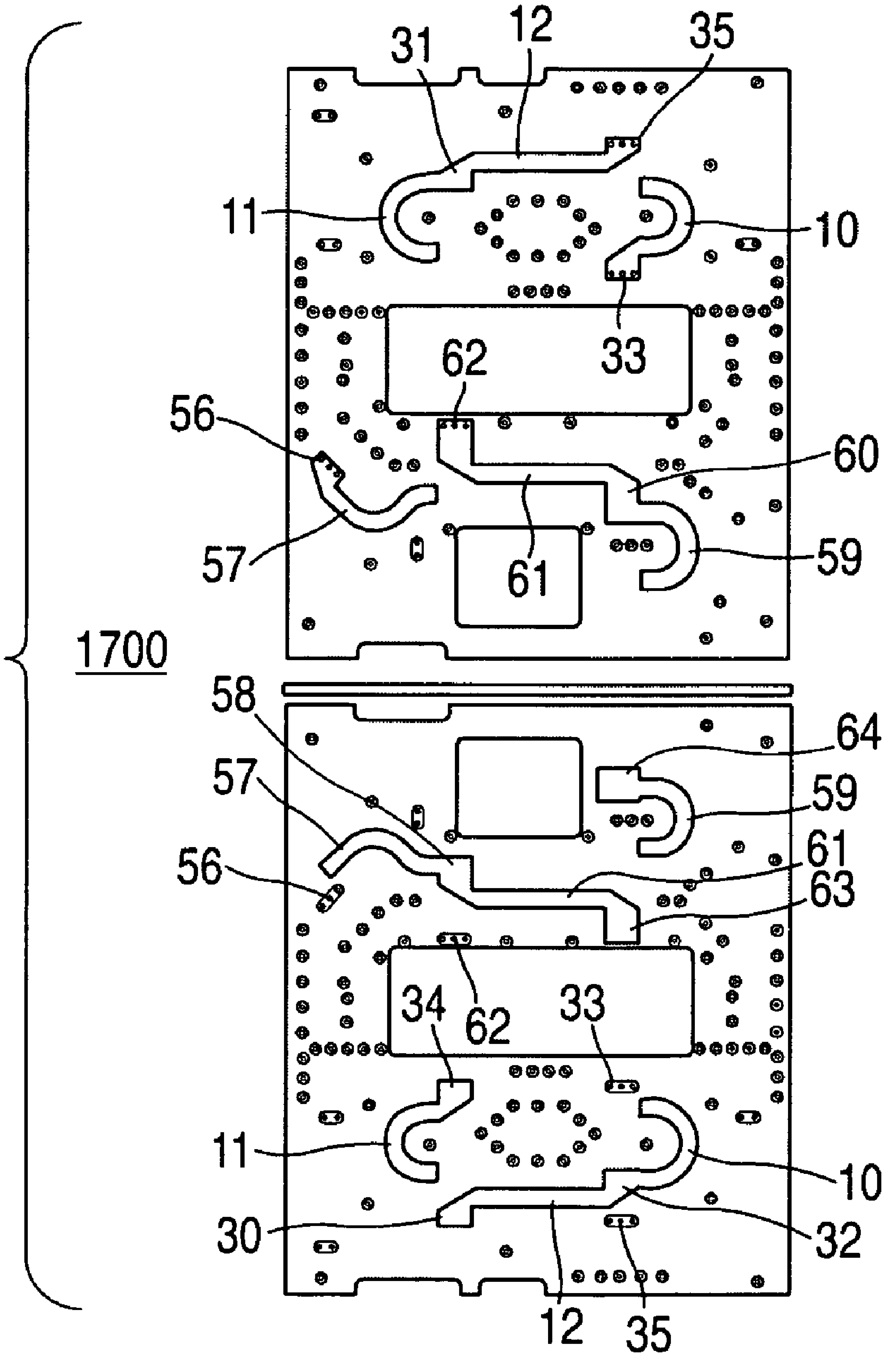


FIG. 17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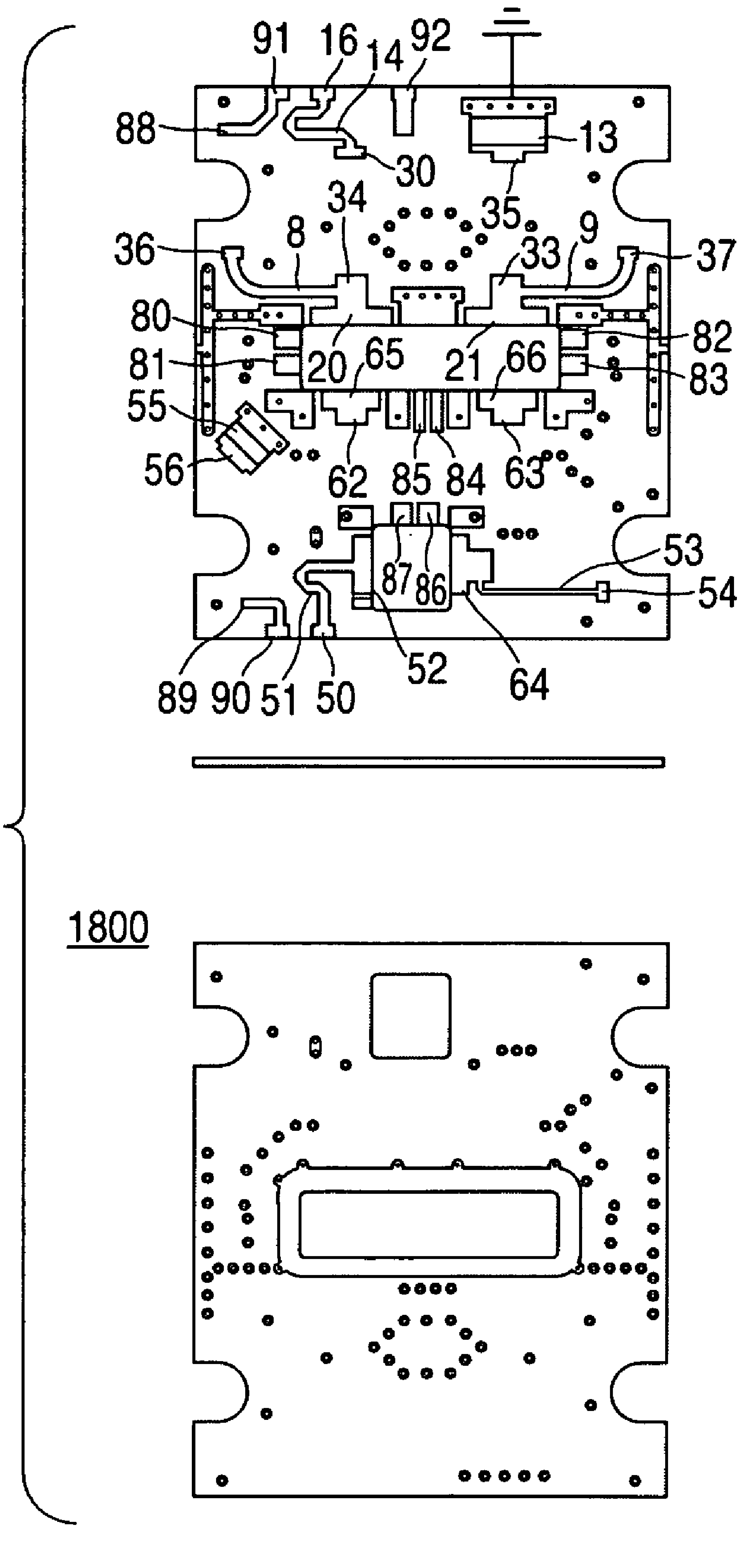
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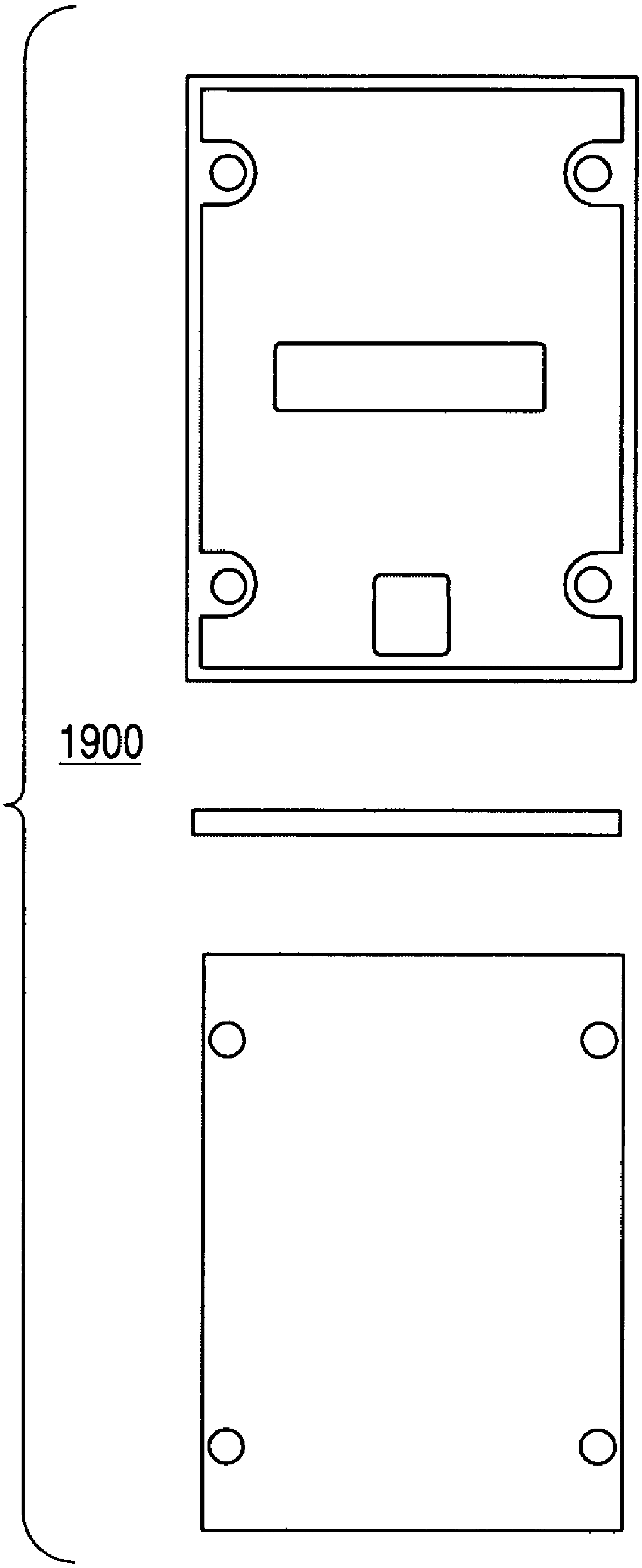
90
51
50
1800

FIG. 18



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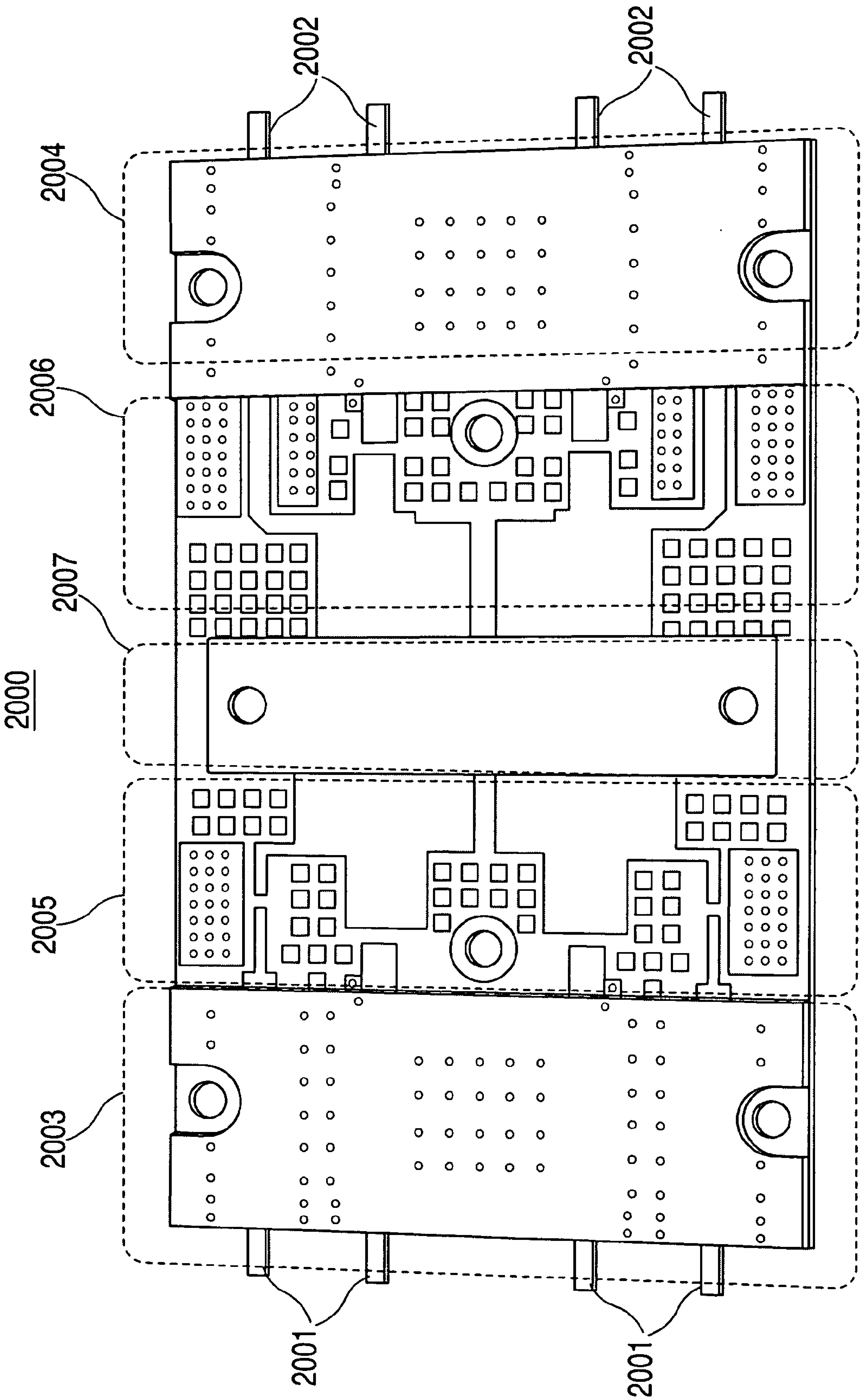


FIG. 20

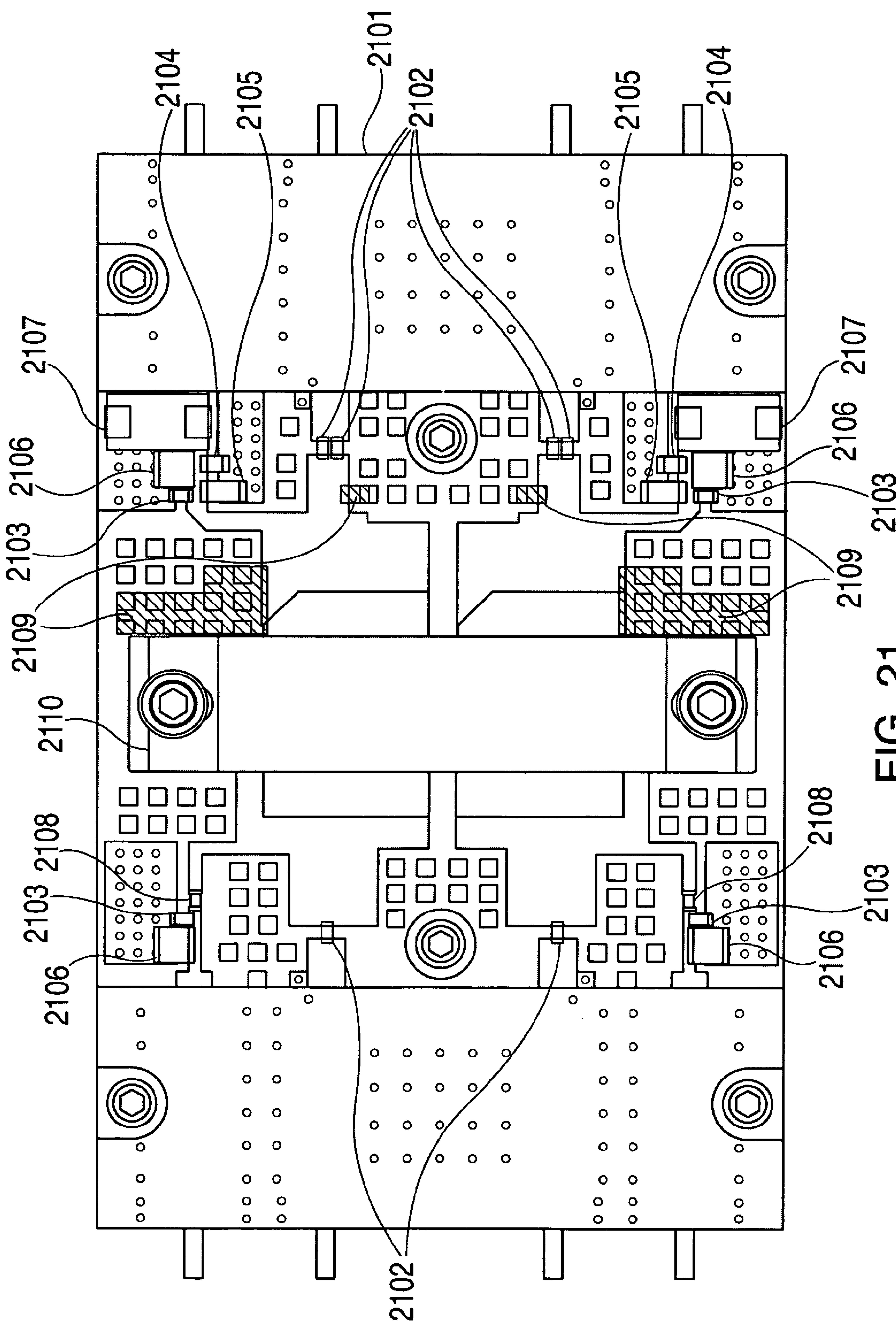


FIG. 21

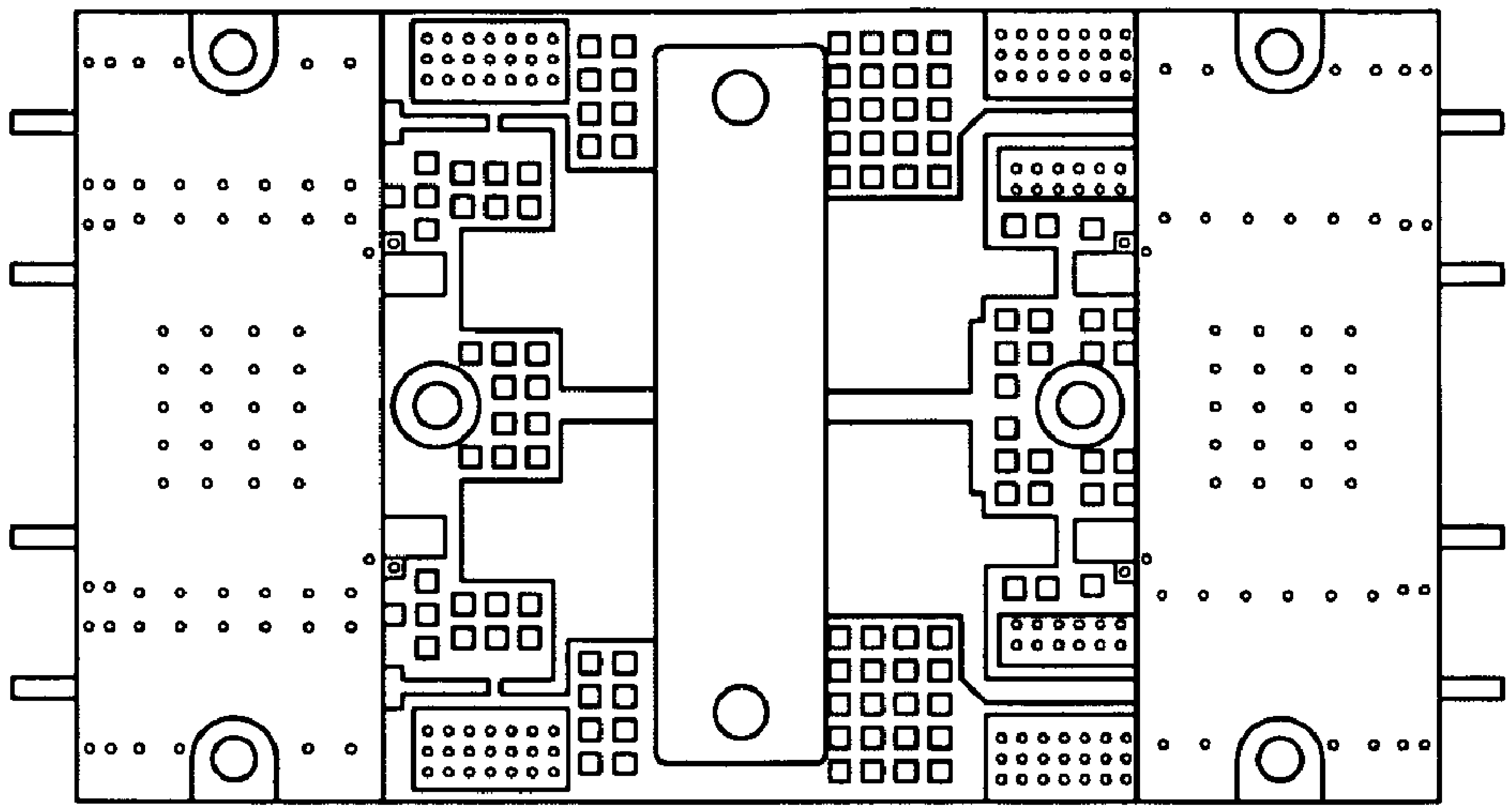


FIG. 22A

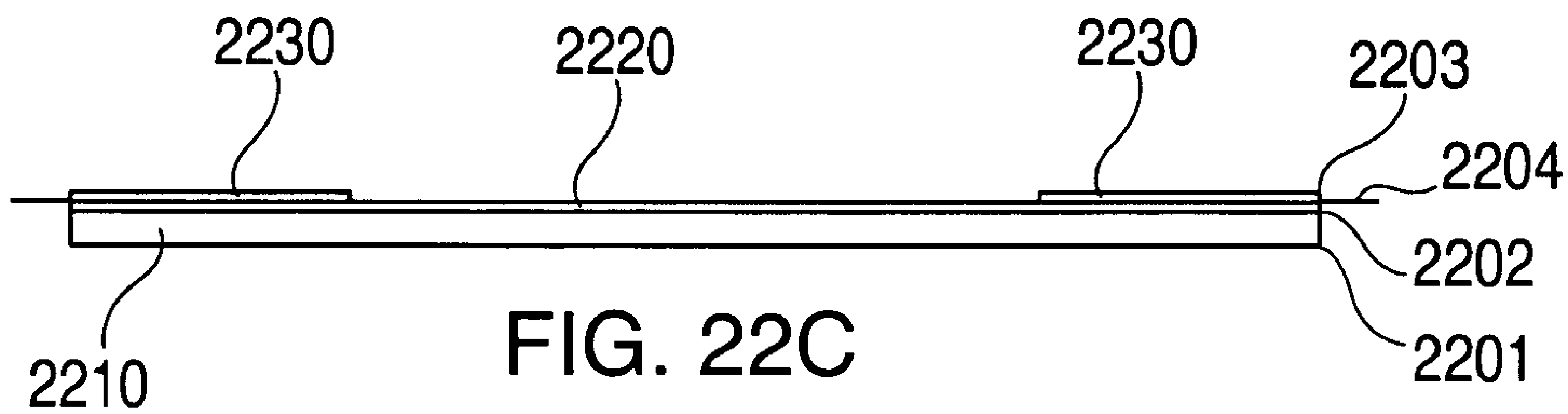


FIG. 22C

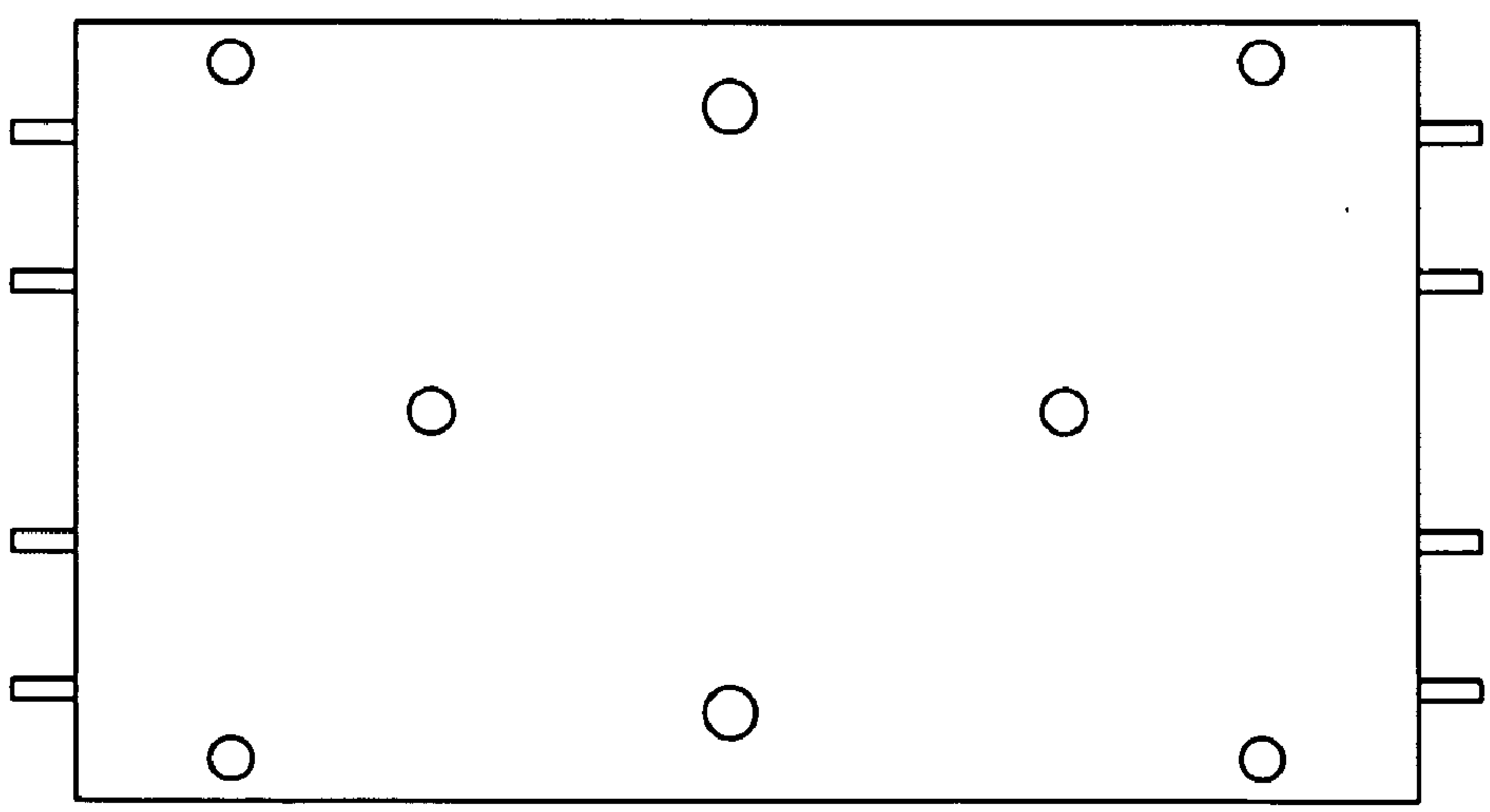
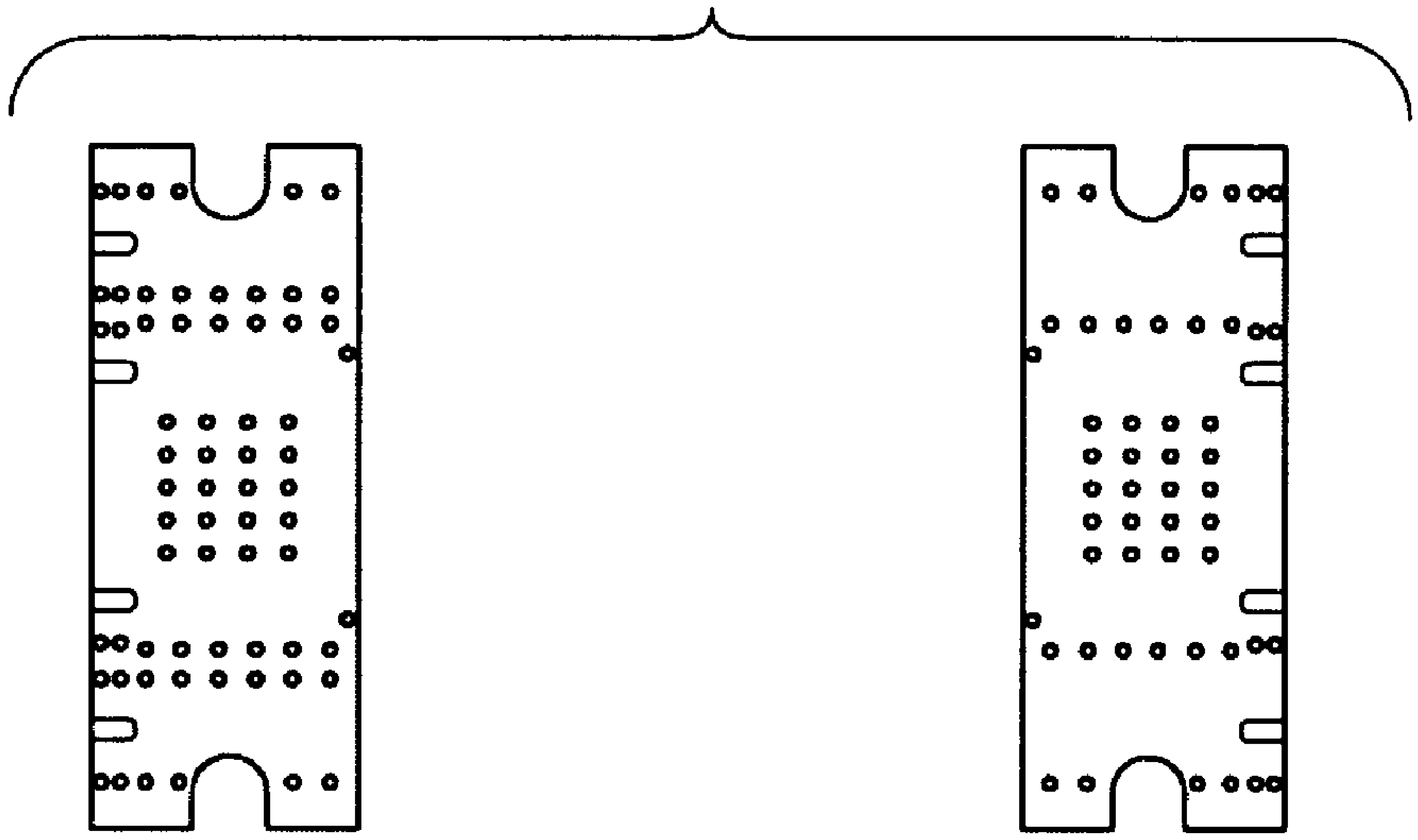


FIG. 22B

FIG. 23B



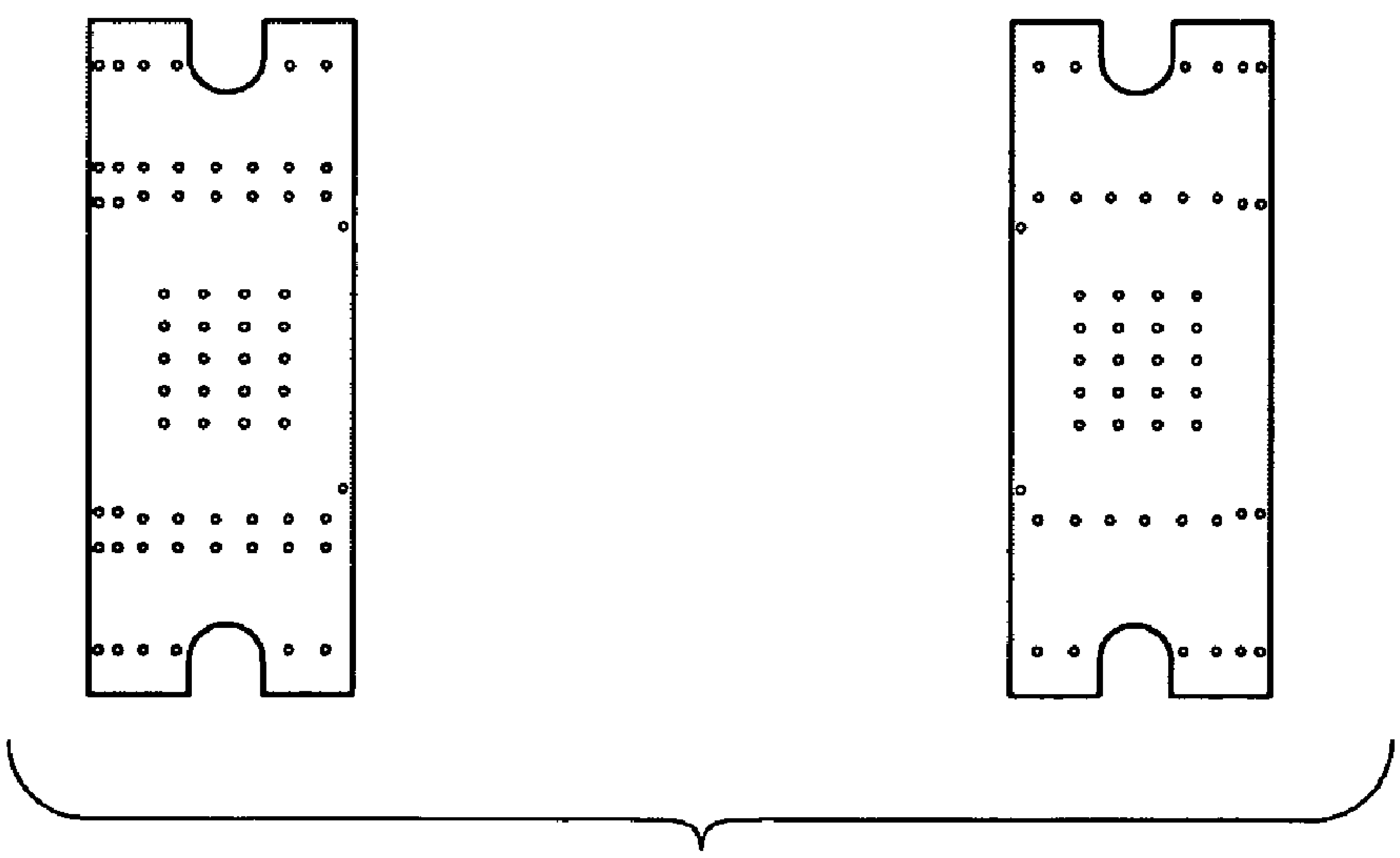


FIG. 23A

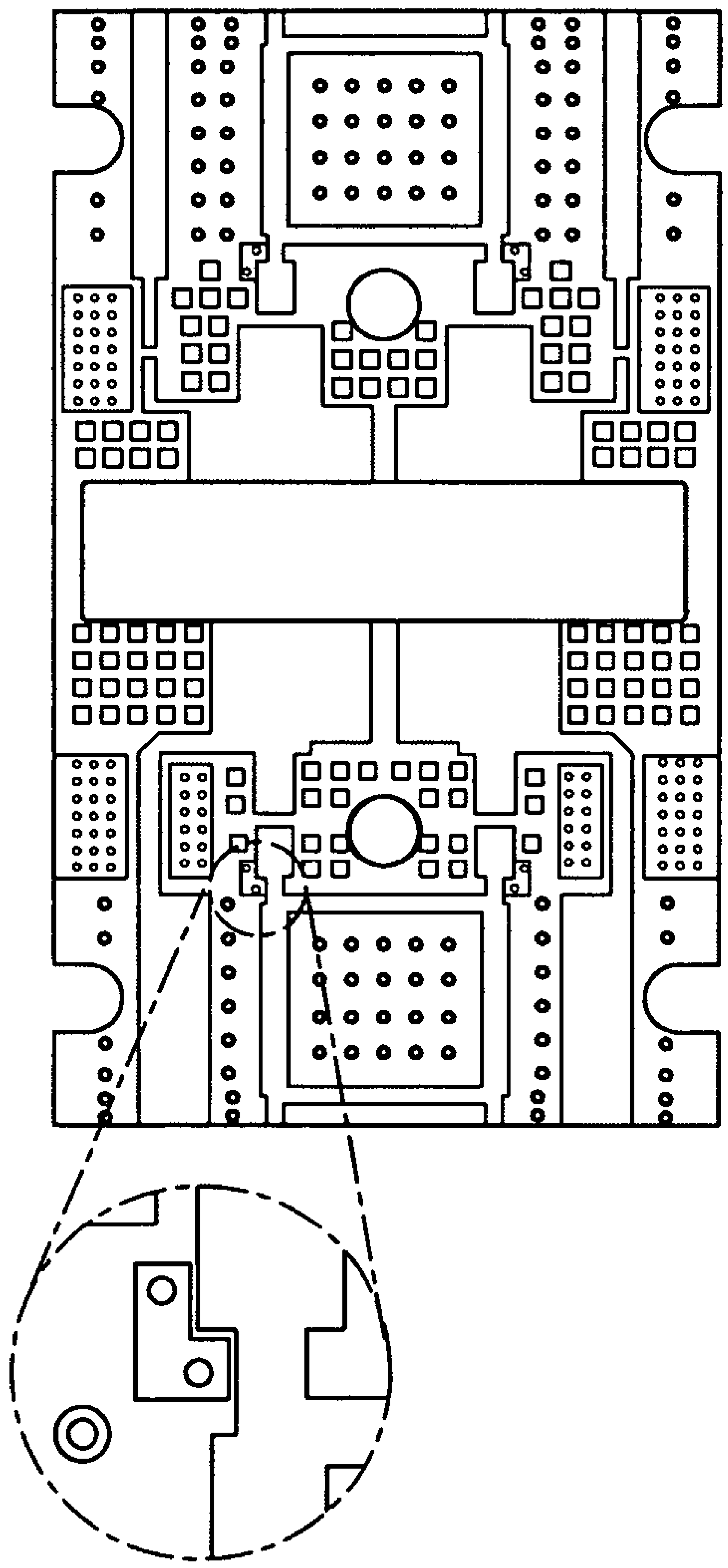


FIG. 24A

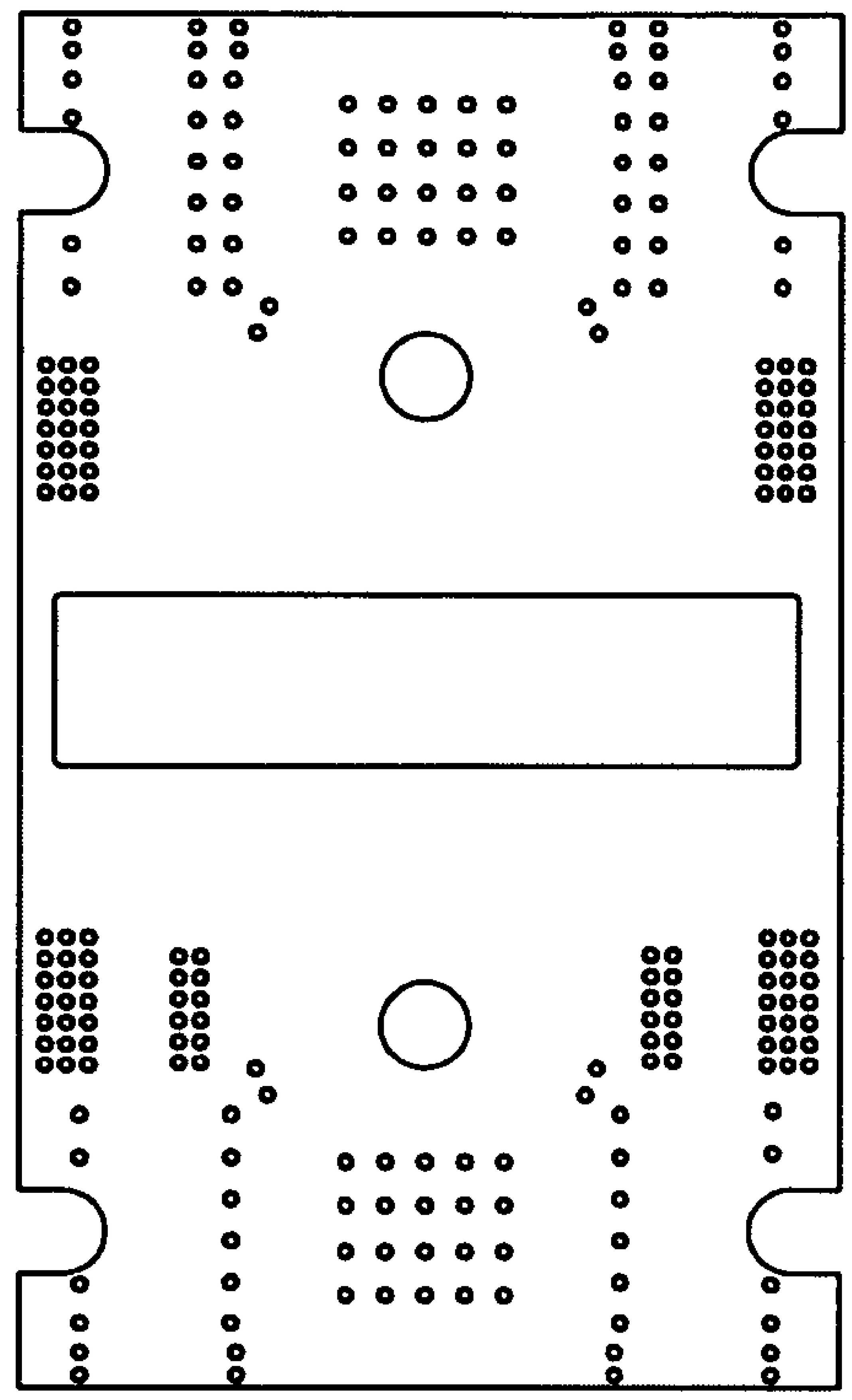


FIG. 24B

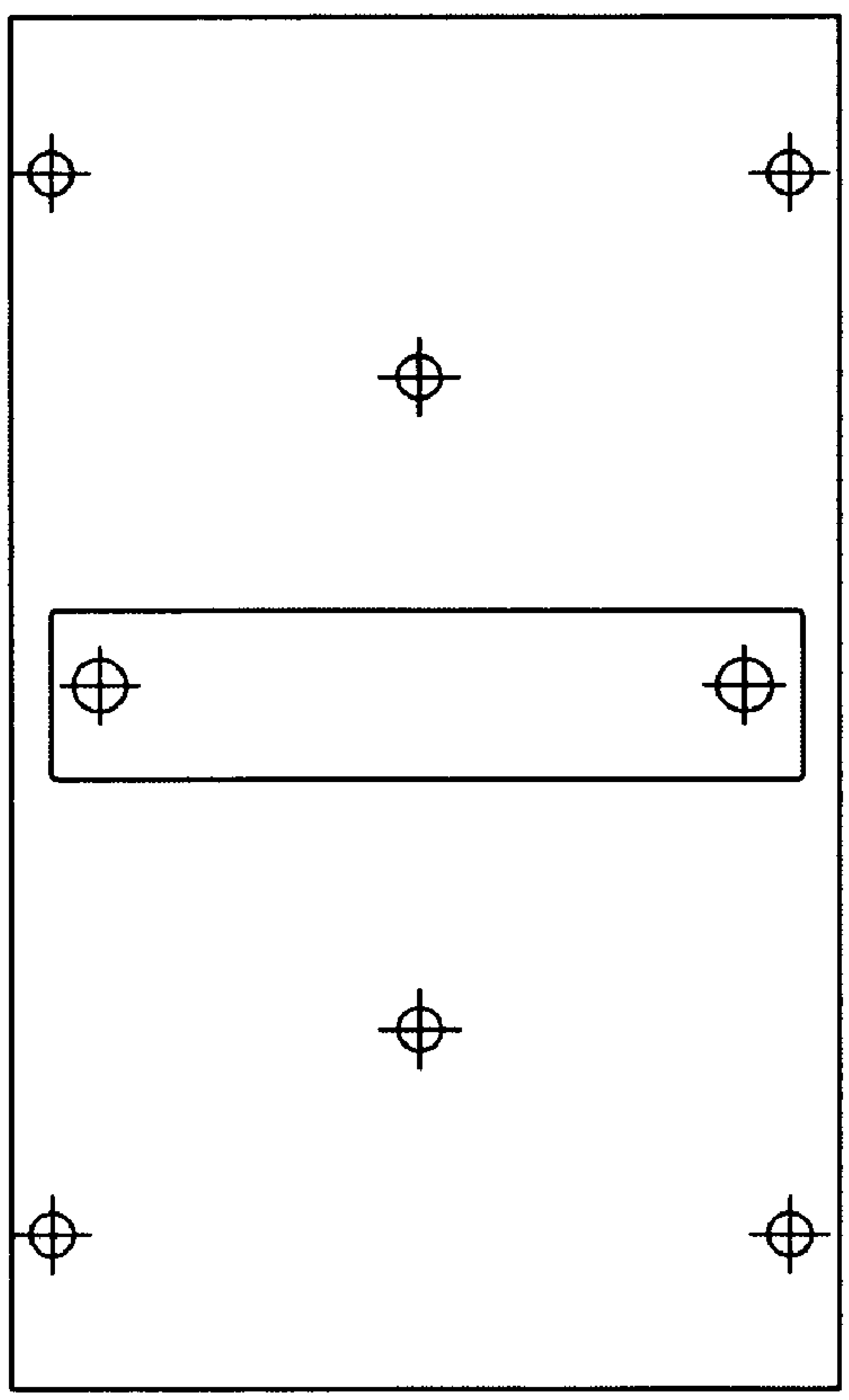


FIG. 25A

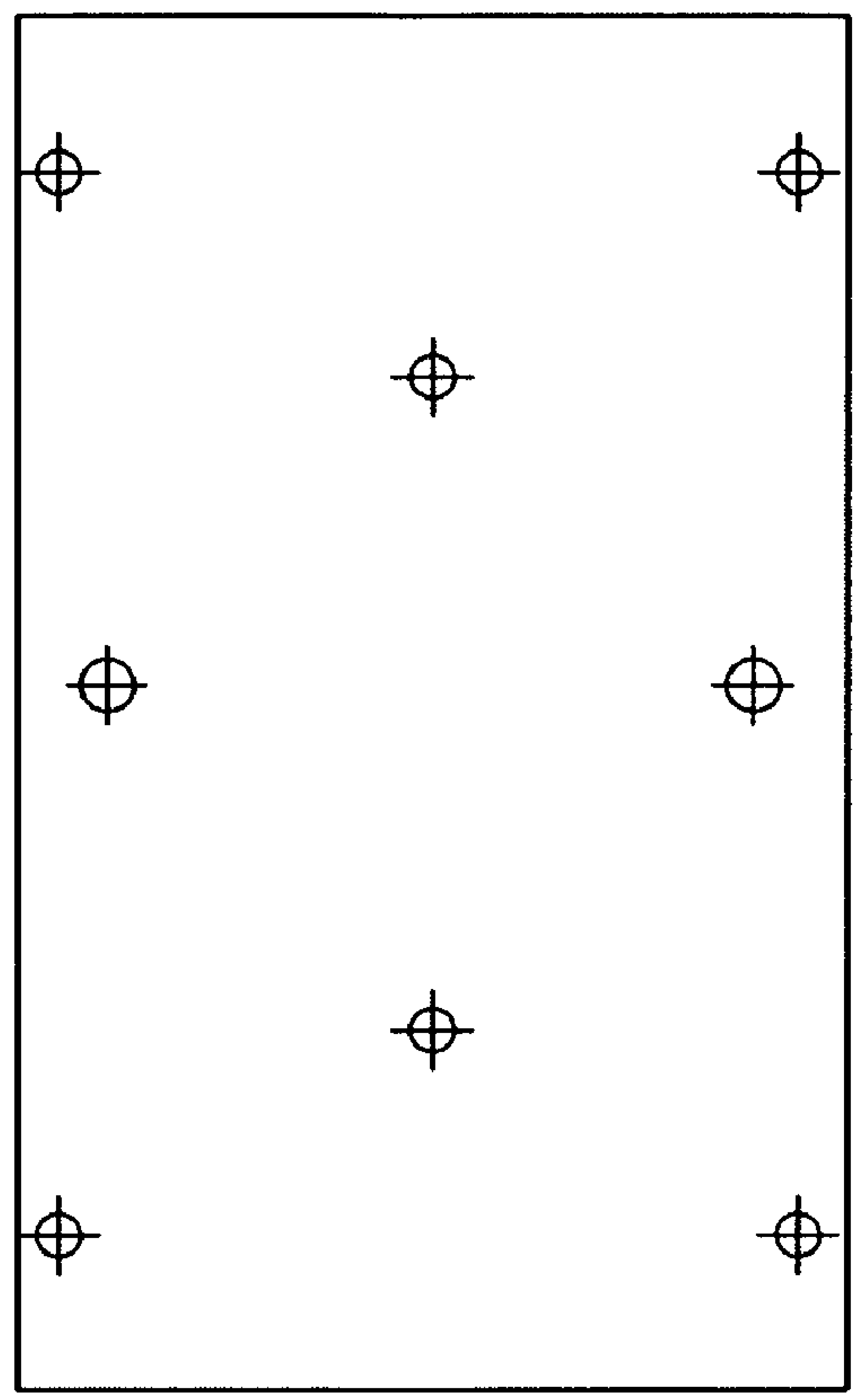


FIG. 25B

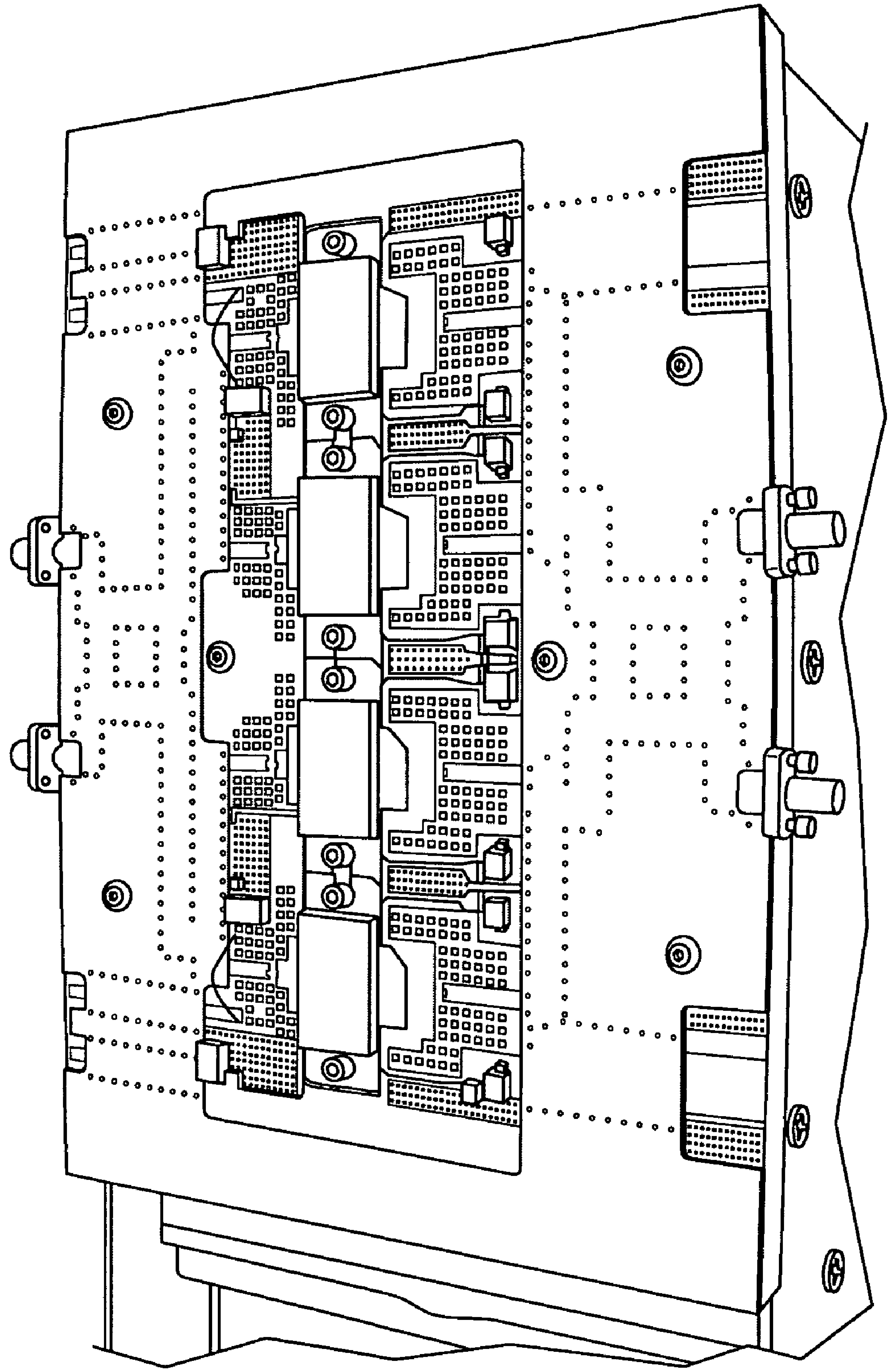


FIG. 26A

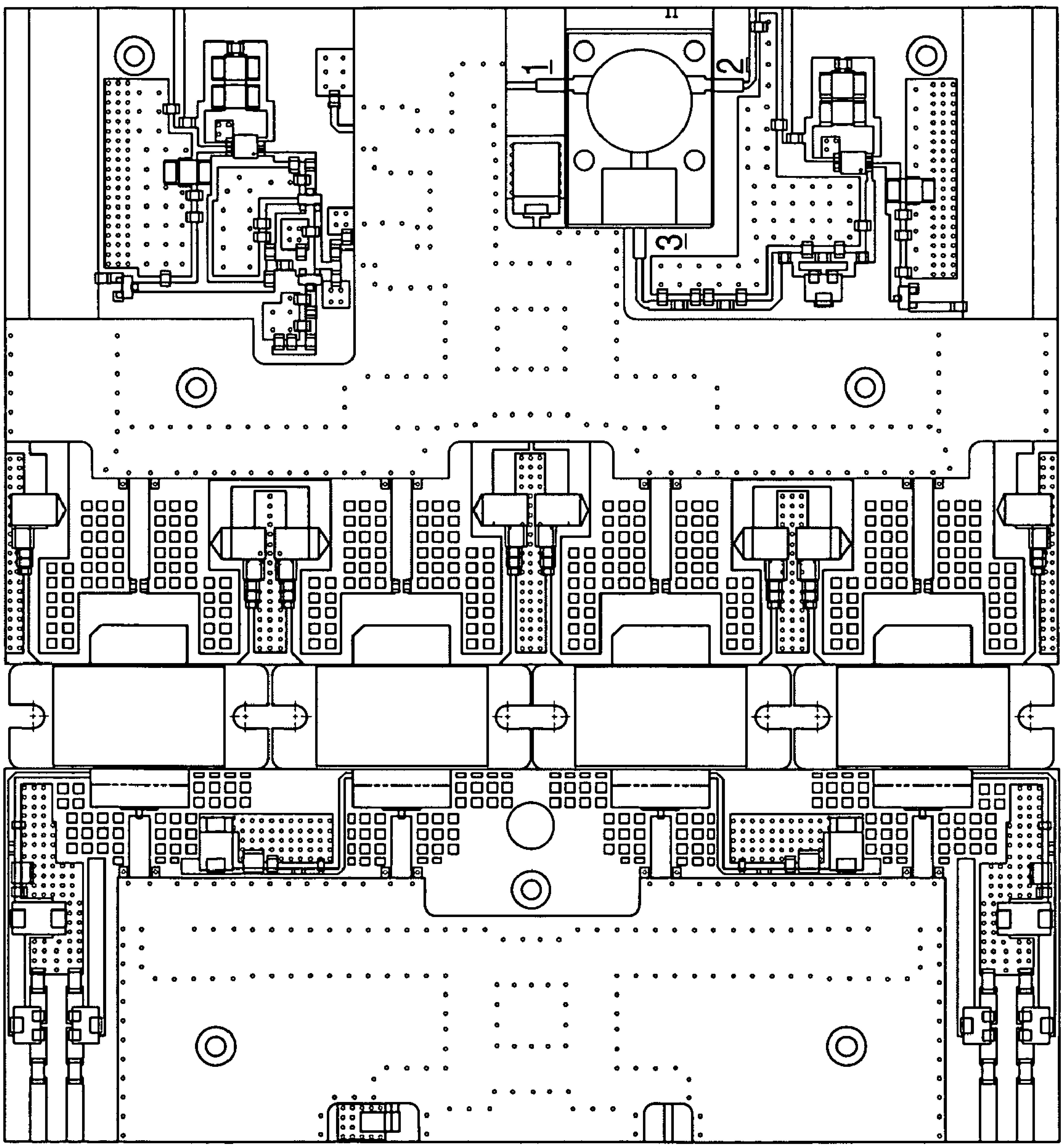


FIG. 26B

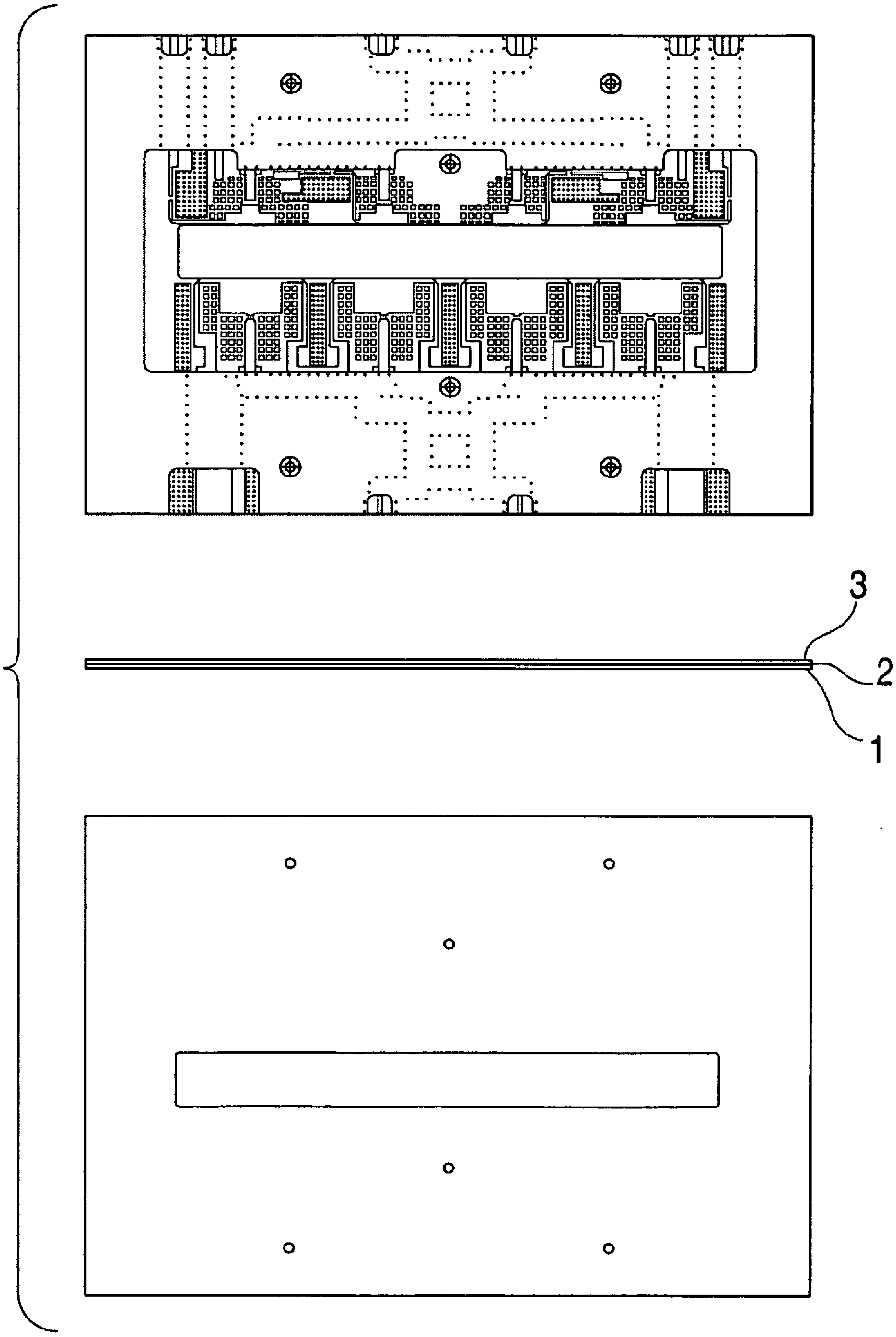


FIG. 27

FIG. 28

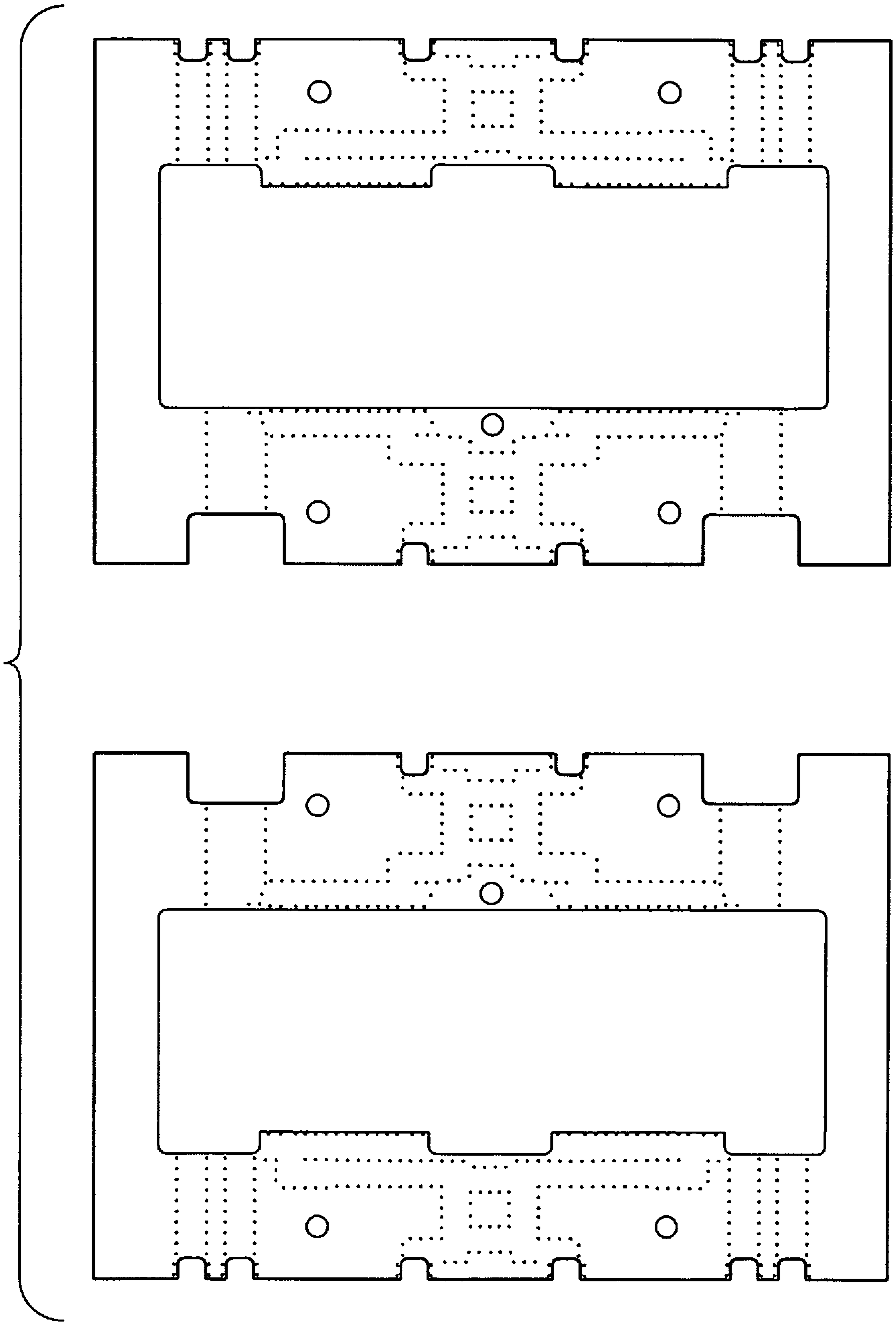


FIG. 29

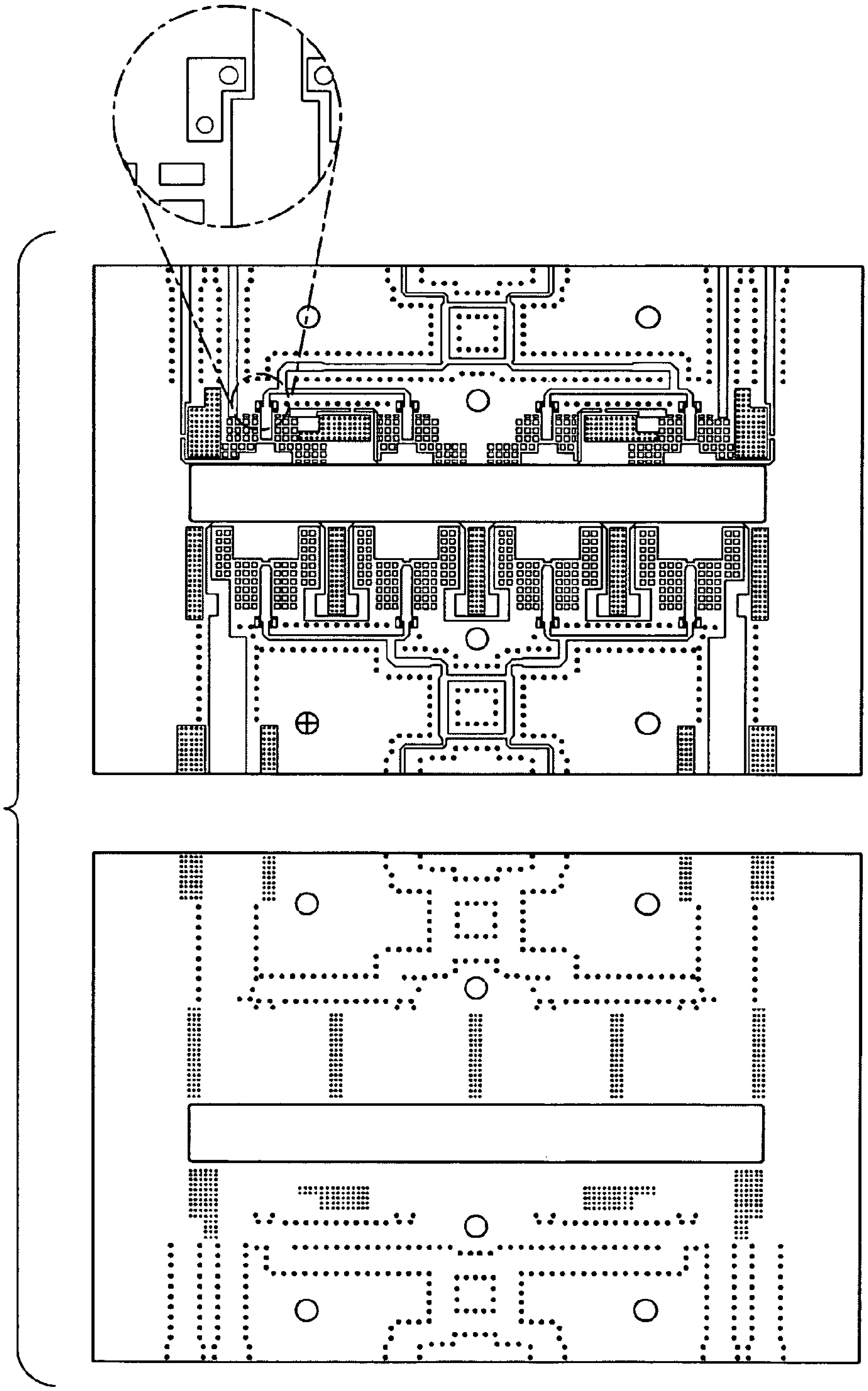
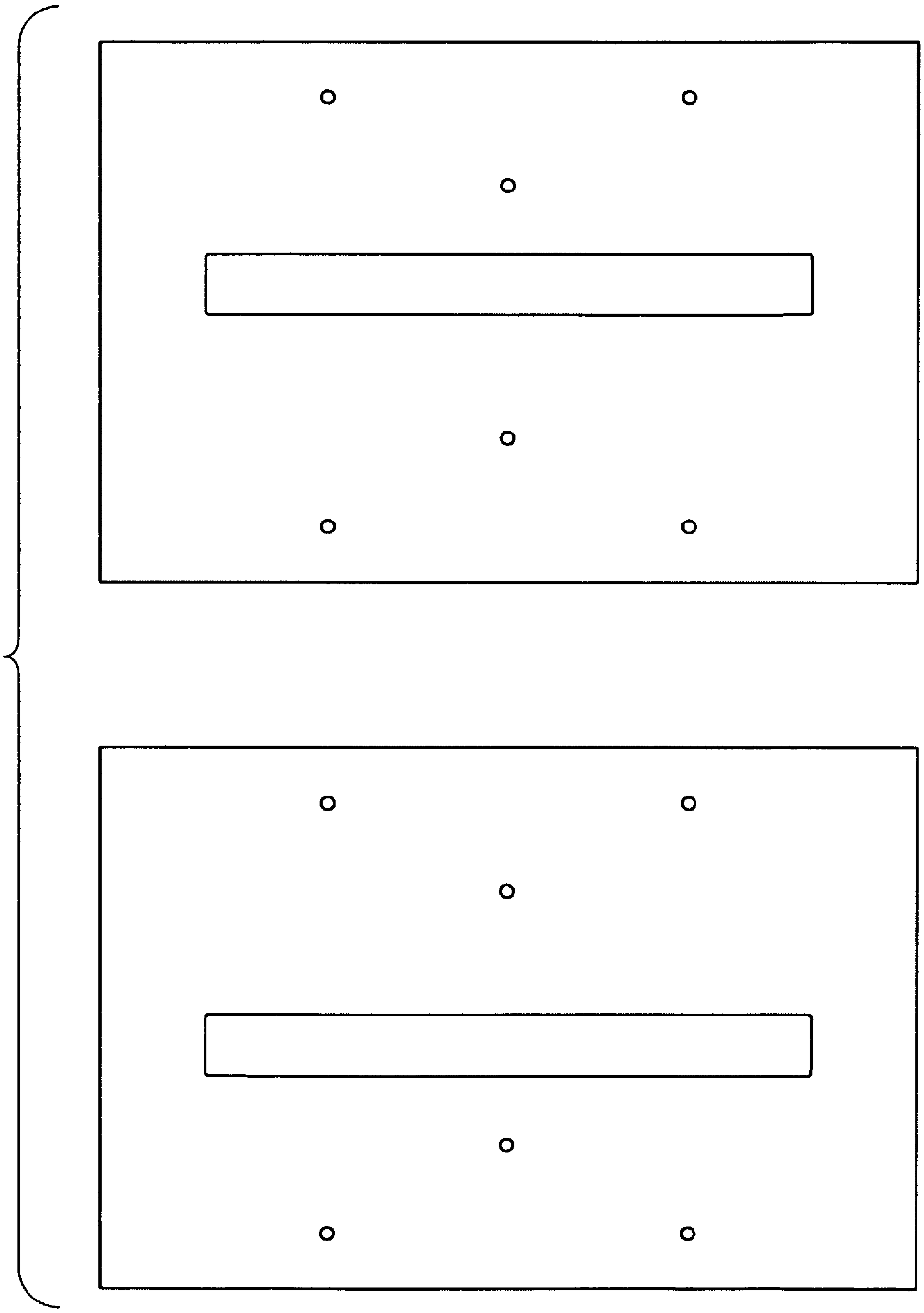


FIG. 30



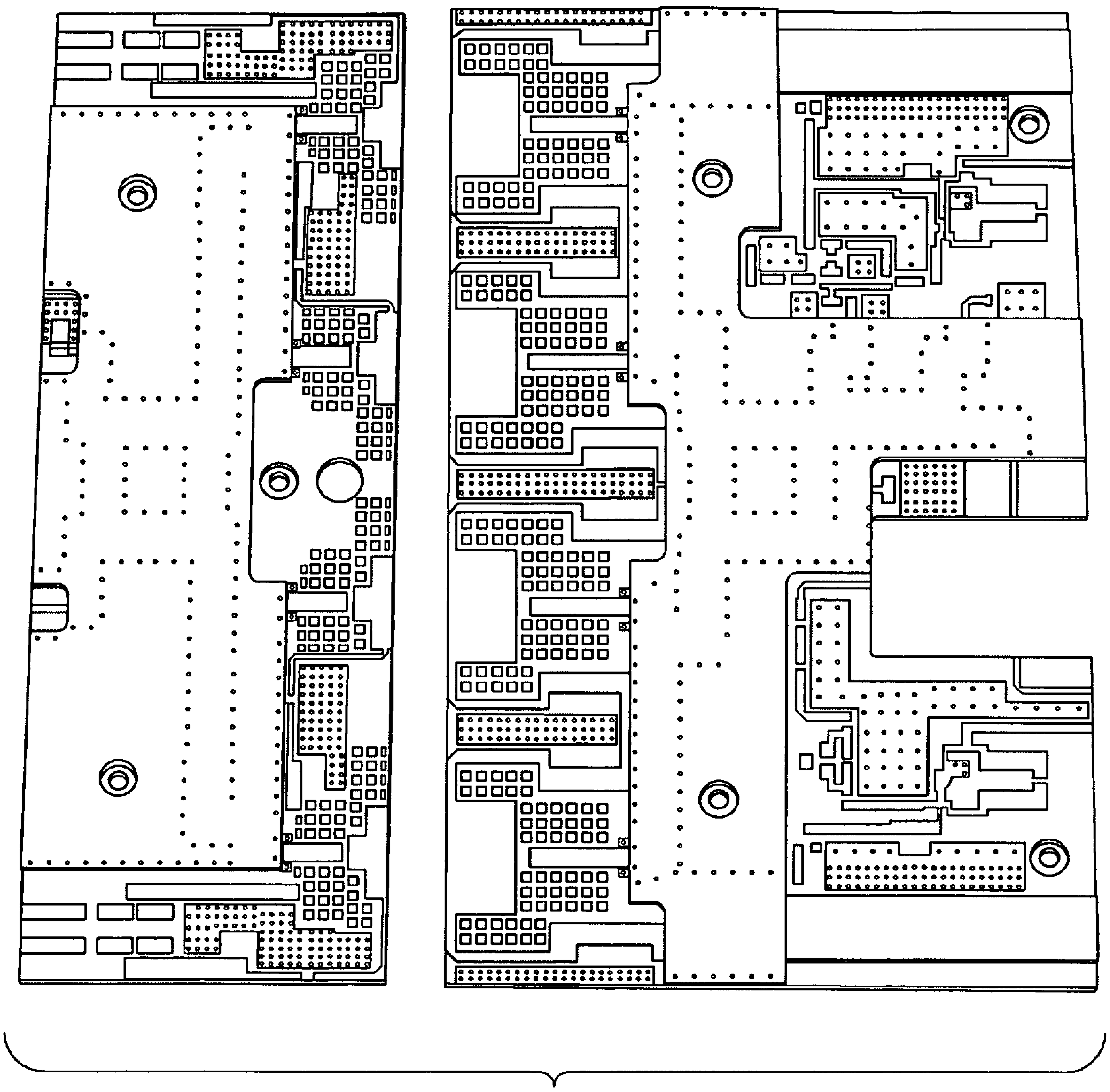


FIG. 31

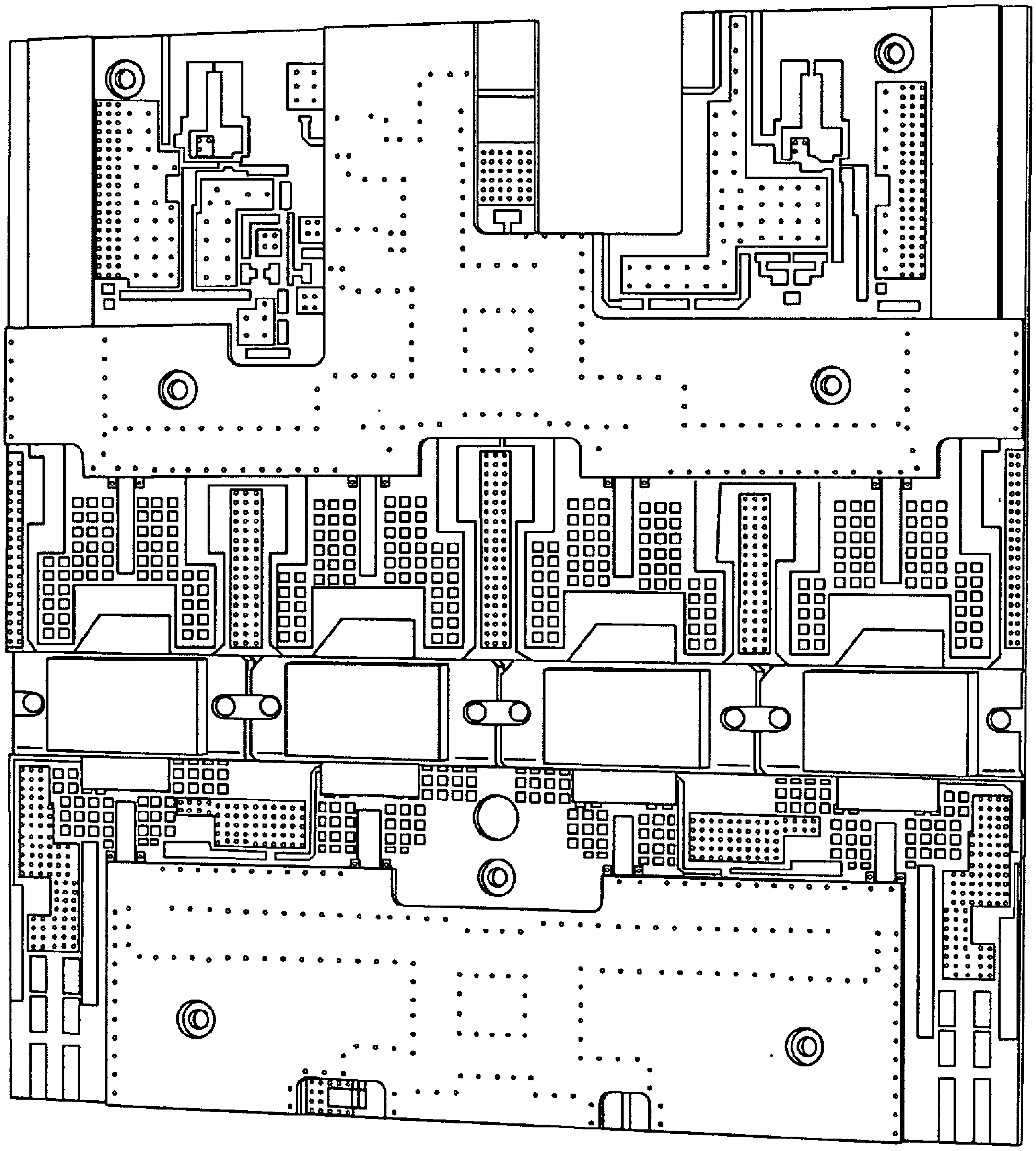


FIG. 32

CIRCUITRY MODULE

This application is a continuation-in-part of U.S. application Ser. No. 10/659,542 filed on Sep. 10, 2003, now U.S. Pat. No. 7,042,307 and entitled "COUPLER RESOURCE MODULE."

BACKGROUND OF THE INVENTION

The development of planar transmission media in the early 1950's had a major impact on microwave circuit and component packaging technology. The engineering of the microwave printed circuit and the supporting analytical theories for stripline and microstrip occurred at a rapid pace. The early years of stripline circuit design were devoted almost entirely to the design of passive circuits such as directional couplers, power dividers, filters, and antenna feed networks. Early implementations were housed in bulky metal housings and connected by coaxial connectors.

To reduce size and weight, case-less and connector-less couplers were developed. These later implementations were sometimes referred to as "filmbrids" and included laminated stripline assemblies bonded together by fusion, or with thermoplastic or thermoset films. Further refinements continued in areas such as the dielectric materials used in these devices and the microwave-circuit fabrication process itself. A historical perspective on the development and applications of microwave integrated circuits, can be found in "Microwave Integrated Circuits—An Historical Perspective", H. Howe, Jr., IEEE Trans. MTT-S, Vol. MTT-32, pp. 991-996; September 1984; and "Microwave Printed Circuits—The Early Years", R. M. Barrett, IEEE Trans. MTT-S, Vol. MTT-32, pp. 983-990; September 1984.

Stripline and microstrip components have been integrated for various applications in housings and packages, as well as monolithically on a common substrate. Methods of integration and packaging affect the system interface and installation, as well as the module's ability to handle post-processing temperatures (i.e., post-manufacture of the stripline or microstrip component), and the module's operating thermal management ability (i.e., its heat transfer ability). Common techniques for integrating components call for bonding them together using, e.g., epoxies, adhesives and solder. In some cases, a module that uses epoxies, adhesives, solder and/or other bonding agents will be subject to subsequent processing steps exposing the module to high temperatures or other processing conditions. These subsequent processing steps must be compatible with the bonding agent and material used in forming the modules. For example, when a module is formed using conventional epoxies, adhesives, and solders, high temperature post-processing may need to be avoided as it may cause deterioration in module bonding.

Planar signal coupling and processing modules that can be subject to, and retain their integrity under, a wider range of manufacturing processes are desired. Accordingly, there exists a need to integrate coupler circuitry, DC blocking structures, impedance matching networks, bias decoupling structures and RF load terminations into a modular planar structure that will be able to withstand, e.g., high temperature processing or other processing steps that the module may be subject to after its manufacture. Such processing may occur, e.g., when the microwave module is integrated with other components in a circuit assembly. Furthermore, there exist a need to have coupling circuitry that can be easily customized by the addition of components post-manufacture of the coupling assembly.

SUMMARY OF THE INVENTION

A coupling module that can be used, e.g., for the integration of microwave couplers, DC blocking structures, impedance matching networks, bias decoupling structures, RF load terminations, and amplification circuitry is disclosed. The module, also referred to herein as a "resource module", has a multi-layer module architecture that can include multiple circuit layers bonded together and, in some implementations, to a metal flange. The metal flange can be used for device attachment and thermal management, and as a package interface and for installation. The resource module can include a device attachment area (also referred to as a "resource well" or a "cavity" through the substrate layers). The resource well allows the addition of devices to the module, and coupling of those devices to circuitry in the resource module, after the module itself has been formed. That is, additional devices can be added into the resource well after the layers of the resource module have been bonded. In some implementations, the resource well includes attachment points within the well whereby an added device can be signal-connected to coupler circuitry formed in the resource module's dielectric layers, and can be coupled to the module's metal flange. This module may be used to provide a common platform for various microwave circuit applications, and a method of system interface and installation which offers a significant degree of freedom by allowing, e.g., high temperature device attachment processing, as well as optimal operating thermal management. This common platform can be customized by adding a wide variety of circuits and circuit elements to the resource module and by the addition of circuits to exposed contacts on a surface layer. These circuit elements can include microwave circuits, transistors, varactor diodes, PIN diodes, and Shottky diodes.

In one implementation, the coupling assembly includes multiple composite substrate layers and an (optional) flange layer fusion bonded together in a stacked arrangement. The substrate layers are positioned on top of the flange layer and include fixed embedded signal processing circuitry (e.g., stripline impedance matching circuitry) connected to a signal input and a signal output. A second "tunable" or "adjustable" region of circuitry, e.g., microstrip impedance matching circuitry is coupled between the fixed embedded signal processing circuitry and a cavity formed through an area of the substrate layers. The cavity exposes signal connection terminals coupled to the adjustable embedded circuitry. These signal connection terminals are coupled to the adjustable embedded circuitry and they enable the addition of a circuit element to the assembly after the bonding of substrate layers. The adjustable embedded circuitry is further coupled to the fixed embedded circuitry and enables the addition of circuit elements (e.g., resistors and capacitors) at contact regions on the substrate surface in order to customize the adjustable circuitry. In one implementation, the assembly is configured such that the fixed embedded circuitry presents a predetermined impedance at the assembly's signal input and signal output terminals and also presents predetermined impedance characteristics at the adjustable embedded circuitry. The adjustable embedded circuitry may then be "tuned" by, e.g., the addition of capacitive and resistive elements to provide for impedance matching between the fixed embedded circuitry and any circuit elements coupled within the resource well. Such an implementation thereby provides for a module that may be easily customized for the addition of elements with different impedances within the cavity while providing for an assembly that presents a standardized impedance to external devices.

Implementation may include one or more of the following features. The embedded signal processing circuitry (which may include, e.g., microwave coupler circuitry, impedance matching circuitry, DC blocking circuitry, bias decoupling circuitry, and/or RF load terminations) can include first signal processing circuitry coupled to the signal input and to a first signal connection terminal exposed within the cavity and second signal processing circuitry coupled to the signal output and to a second signal connection terminal exposed within the cavity. The cavity can be configured to receive added circuit element such as a microwave circuit, a transistor, a varactor diode, a PIN diode, a Shottky diode, or other circuit elements. There may also be conductive terminals exposed within the cavity and coupled to conductive terminals on an exterior surface of the assembly to provide for signal connections between a circuit element added to the cavity and external signal sources.

Implementations may also include one or more of the following features. The cavity may expose a top surface of the flange layer enabling coupling (e.g., either electrical or thermal coupling) of the added circuit element to the flange layer. The flange layer can be formed of a substantially homogeneous metal core. Plated metals (e.g., nickel, gold, or other metal inhibiting oxidation of the metal core) may be added to the surfaces of the flange layer. Interconnections can be made between substrate layers using plated via holes.

Manufacture of the coupling assembly includes drilling the substrate layers to create a plurality of vias and forming cutouts in the substrate layers. The cutouts are positioned such that when the substrate layers are fused in a stacked arrangement, the cutouts form a cavity through the substrate layers exposing a top surface of a lower layer (e.g., the flange layer). In some implementations, the top-most layer may cover the cavity during bonding and then be drilled or milled to "open" the cavity and/or to expose regions of lower substrate layers, while in other implementations, the top-most layer may already have cavity and or other lower-layer exposing regions pre-milled to create an open cavity and exposed lower-layer surfaces upon bonding.

Prior to bonding, the surfaces of the substrate layers are metalicized to form both the fixed and variable embedded signal processing circuitry elements, signal input and output terminals, signal connection terminal exposed within the cavity, and conductive vias interconnecting the foregoing structures when the plurality of composite substrate layers are positioned in a stacked arrangement.

The details of one or more implementations of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF THE DRAWINGS

FIG. **1** show a top, side, and bottom view of an assembled resource module.

FIG. **2** is a block diagram showing signal processing circuit components that may be included in an implementation of the resource module of FIG. **1**.

FIG. **3** is a block diagram showing signal processing circuit components that may be included in an alternative implementation of the resource module of FIG. **1**.

FIG. **4-6** show top and bottom metal layers of three dielectric substrates implementing the signal processing circuit of FIG. **2**

FIG. **7** shows top and bottom views of a metal flange layer.

FIG. **8** shows a panel array.

FIGS. **9-12** show different types of striplines.

FIG. **13** shows a slab line transmission line.

FIG. **14** shows an alternative embodiment of a coupler resource module.

FIG. **15** shows top, side, and bottom views of the coupler resource module of FIG. **14**.

FIGS. **16-18** show top and bottom metal layers of three dielectric substrates implementing the signal processing circuit of FIG. **14**.

FIG. **19** shows top and bottom views of a metal flange layer.

FIG. **20** shows a completed circuitry assembly including a resource well, both fixed and adjustable embedded signal processing circuitry, and signal connection points that enable addition of components to the assembly so as to adjust electrical characteristics of the adjustable embedded signal processing circuitry.

FIG. **21** shows the completed circuitry assembly of FIG. **20** with components **2102-2110** added to signal connection points.

FIGS. **22**A, **22**B, **22**C show a top, bottom, and side view of the module of FIG. **20**

FIGS. **23**A, **23**B, **24**A, **24**B, **25**A and **25**B show top and bottom views of layers of the module of FIG. **20**.

FIG. **26**A shows another implementation of a coupler module configured such that multiple power amplifiers may be added within the module's resource well. FIG. **26**B shows the module of FIG. **26**A with circuit elements added to microstrip circuitry formed on the module.

FIGS. **27-30** show the layers of the module of FIGS. **26**A and **26**B.

FIG. **31** shows an implementation in which the module is constructed in a split fashion.

FIG. **32** shows the module of FIG. **31** with amplifier circuitry added.

DETAILED DESCRIPTION OF THE INVENTION

A "resource module" structure is disclosed herein. Top, side, and bottom views of the module are shown in FIG. **1**. As shown in side view, and in more detail in FIGS. **4-7**, the resource module **100** may be fashioned from a stack of bonded substrate layers and a metal flange layer. The substrate layers are preferably formed of polytetrafluoroethylene (PTFE), glass, and ceramic. Each substrate layer may include circuitry on one or both sides. The circuitry can include, e.g., microwave directional couplers, and 3 dB quadrature couplers, impedance matching networks, DC blocks, bias decoupling, and RF load terminations. The flange layer provides for mounting of the resource and for improved thermal properties.

FIGS. **2** and **3** are block diagram for different implementation of the resource module. The block diagram of FIG. **2** shows circuitry **200** that is formed in the substrate layers of FIGS. **4-6**. An example of how this circuit operates will given for the case of 12.5 ohms, although similar operation occurs for circuits of other impedance values. The example shown is for the case of 3 dB couplers, however other networks can be composed using couplers with other coupling values. In figures used throughout this disclosure, like-numbered elements reference the same structure (whether in, e.g., the block diagram form of FIGS. **2** and **3** or in the flange and dielectric layer forms of FIGS. **4-7**). The circuitry shown in the block diagram of FIG. **2** may be used where the impedance at input **15** and output **16** is different from the impedance of devices added to the resource well **17**. In particular, the circuitry **200** is for an implementation in which inputs and outputs are at 50 ohms and the module enables attachment of 12.5 ohm devices in the resource well **17**. The circuitry in the block diagram of FIG. **3** is for an implementation in which input, output, and attached resource impedances are the same. The circuit elements shown in FIG. **3** are substantially identical to those of FIG. **2** except that the block diagram of FIG. **3** lacks transformer elements **1**, **14** of FIG. **2**. Substrate layers to implement **300** follow from those for the circuit **200** of FIG. **2**.

The circuit **200** receives a RF input signal at terminal **15**. The input signal is transformed from 50 ohms to 12.5 ohms by transformer **1** and the output signal **22** is then divided by a first coupler **2**. The resulting two signals at **24**, **25** are then fed through individual couplers **4**, **5**, respectively. The couplers **4**, **5** perform DC blocking functions. Two RF signals **26**, **27** are now available at resource well terminals **18**, **19**, respectively. The signals at terminals **18**, **19** can be connected to devices such as transistors, varactor diodes, PIN diodes, and Shottky diodes that may be added to the resource well **17** after formation of the module **100**. Additional signal terminals may be present in the well **17** for, e.g., ground connections or connections to external signal sources. In addition, other lumped components such as resistors, capacitors and inductors may be placed in the resource well **17**. After the RF signals are processed by the devices in the well **17**, they are output to terminals **20**, **21** and processed by circuitry **8-14**. Circuits **8-14** perform a complementary function to that of circuitry **1-7**. That is, signals on terminals **20-21** are provided at input points **33**, **34** to couplers **10**, **11** and to quarter wave striplines **8**, **9**. The couplers **10**, **11** serve to block DC bias from input signals **33**, **34**. The coupler output signals **31**, **32** are then recombined by an output coupler **14** and the output **30** from the coupler **12** is provided to impedance transformer **14** which transforms the input signal **30** from 12.5 ohms impedance to a 50 ohms output impedance at signal point **16**.

The devices used in the resource module **17** may require a DC bias for operation. This DC bias is contained in the device area **17** by the DC blocks **4**, **5**, **10**, **11**. The DC bias **28-29**, **36-37** is connected to the device area **17** through bias decoupling lines (i.e., quarter wave striplines **6-9**) which appear as an open circuit to the RF signal in the device area **17**. The RF load terminations **3**, **13** are connected to the couplers **2** and **12** at signal points **23**, **35**, respectively, and provide matched impedance to isolated ports of the couplers. The impedance of the terminations **3**, **13** matches the coupler impedance.

Basic principles for design of the design of the microwave directional couplers and 3 dB quadrature couplers circuitry is well known to those skilled in the art, and described in such papers as "Shielded Coupled-Strip Transmission Line", S. B. Cohn, IEEE Trans. MTT-S, Vol. MTT-3, No. 5, pp. 29-38; October, 1955; "Characteristic Impedances of Broadside-Coupled Strip Transmission Lines", S. B. Cohn, IRE Trans. MTT-S, Vol. MTT-8, No. 6, pp. 633-637; November, 1960; and "Impedances of Offset Parallel-Coupled Strip Transmission Lines", J. P. Shelton, Jr., IEEE Trans. MTT-S, Vol. MTT-14, No. 1, pp. 7-15; January, 1966. Directional couplers are usually implemented as edge-coupled striplines (FIG. **10**) or offset-coupled striplines (FIG. **11**, **12**), whereas quadrature couplers are typically configured as offset-coupled striplines (FIG. **12**) or broadside-coupled striplines (FIG. **9**). The teaching of this disclosure demonstrates that stripline couplers synthesized from these theories may be integrated in a resource module with integrated flange.

The resource module, including the circuitry of FIG. **2**, may be implemented using three dielectric substrate layers bonded together with a thick metal flange. The substrate layers can be formed of modem composite dielectric materials (containing PTFE, glass and ceramic). These materials have electrical and mechanical properties that are stable over wide temperature ranges, and have low loss properties that enhance performance at microwave frequencies. Coefficient of thermal expansion values close to copper allow the formation of reliable plated-through holes and slots. These plated-through features are used to connect conducting layers into stacked stripline structures as well as to form separated groundplanes. Ground slots can be formed in mathematical proximity to signal holes through the dielectric layers to form slab transmission lines maintaining a controlled impedance for propagation in the Z direction (i.e., from top to bottom through the layers of the stacked dielectric layer structure).

FIGS. **4-6** show top, side, and bottom views for three substrate layers **400**, **500**, **600** forming the module **100**. The top-side view can be matched to the bottom-side view by folding the page one the horizontal rectangle formed by the side view. The substrates **400**, **500**, **600** can be formed from composites of polytetrafluoroethylene, glass, and ceramic, having a range of relative dielectric constants (Er) from 2.1 to 20.0, and a range of thickness (h) from 0.001 to 0.060 inches. The substrates, are metalized with copper foil (typically 0.0007 inches thick, but may range from 0.0001 to 0.003 inches), and are etched to form circuits. Via holes and slots (i.e., elongated holes and openings), plated with copper, connect one substrate layer to another. Examples of slots include slots **401**; examples of via holes include holes **402** (other slots and holes are shown in the drawings and are left unnumbered). Details of each layer of the assembly are shown in FIGS. **4** through **7**. The modules are fabricated in array panels as shown in FIG. **8**.

The resource modules described in this disclosure can be fabricated following the processes disclosed in U.S. Pat. No. 6,099,677 (the '677 patent) and U.S. Pat. No. 6,395,374 (the '374 patent), incorporated herein by reference. The layers **400**, **500**, **600** and a thick metal flange **700** (FIG. **7**) are bonded together, directly, by a fusion process, which utilizes a specific profile of temperature and pressure to change the material's state, and form a homogeneous dielectric, while also permanently attaching the dielectric to the thick metal flange. Fusion bonding of a thick metal flange directly to the dielectric layers provides a mechanical mounting interface for system installation. The multilayer resource module may be bolted directly into a system assembly by means of mounting holes **701** in the flange. Since the fusion bonding process occurs at temperatures between 350° C. to 400° C., the resource module can easily withstand the elevated post process assembly temperatures used for device attachment within the resource well **17**. These post-process assembly temperatures can include temperatures arising from attachment of devices using solders (Sn63, Sn96, Au/Si eutectic), epoxies (silver-filled epoxy, insulating epoxy), and adhesives (silver-filled glass, silver-filled cyanate ester).

Fusion bonding of a thick metal flange **700** directly to the dielectric layers (in particular, to the bottom layer **600**) provides an integrated heat sink for thermal management of dissipated RF and DC power. Cutout areas **475**, **575**, **675** in layers **400**, **500**, **600** allow for device mounting directly to the flange or on a dielectric layer surface with thermal vias conducting heat to the flange. In some implementations, the cutout areas **475**, **575**, **675** may be progressively smaller (from top surface to bottom surface) to expose different attachment areas on different dielectric layers. Etched metal-film resistors and printed thick film resistors may be included in the circuit layers, while resistor components may also be attached in the resource well **17**. All of these resistors, typically configured as RF load terminations, can benefit from attachment to the heat sink flange, enabling them to operate at higher power levels.

The following steps summarize construction of the resource module **100** in accordance with the process disclosed in the '677 patent and the '374 patent. It should be understood that each substrate **400-600** and flange **700** is manufactured as part of a panel (e.g., panel **800**) that, in general, will include a number of identical substrate elements (though, in some cases, such as where only a few devices need to be manufactured, panels could be manufactured with a number of different substrates to form differently configured resource modules).

Construction of one implementation of the resource module will now be described. The flange plate layer and each of the substrate layers can be manufactured as follows.

Manufacture of the Flange Plate

1. Each flange plate **700** is formed by selectively plating a copper panel with nickel and gold.
2. Attachment holes **723**, as well as slots and alignment pin holes, may then be drilled through the flange plate **700**. The attachment holes **723** are included when, e.g., the completed module is to be screw-mounted to another surface.
3. The entire bottom surface **710** may be nickel/gold plated while the top surface **720** may be nickel/gold plated over the entire top surface or, in some implementations, nickel/gold plating may be limited to the area around the perimeter **724** of the surface **720** and in the area **722** surrounding attachment holes **723** and slots.
4. Selective gold plating may be used in the resource well area **721**. The selective gold plating **721** provides for improved corrosion resistance in the area **721** and helps to ensure a good electrical connection between the flange plate **720** and devices added in the resource well **17**. A photoresist process can be used to define the area for selective gold plating.

Manufacture of Substrate Layers

1. Drill slots and via holes through the substrates layers (**400**, **500**, **600**). Alternatively, slots and via holes through the substrate layers may be formed by drilling and then plasma etching of the exposed substrate layers within the hole and slots, before plating with copper.
2. The substrate layers (in particular, the hole and slots) are then plated with copper, first using an electroless copper seed layer, followed by an electrolytic copper plate, preferably to a thickness of 0.0005 to 0.0010 inches.
3. The substrate layers are then laminated with photoresist on both sides of each layer. The photoresist is exposed using photographic masks, and then developed to reveal selected areas of the substrate layers. After exposing and developing the photoresist, the photoresist remains to protect the copper layer used to form structures **1-14** and interconnections (e.g., **15-37**). The plated copper is then etched from areas of the substrate layers that are not shielded by photoresist.
4. Resistors **3** and **13** are then formed by further etching the copper in the areas of the resistors **3**, **13**, exposing a thin film of nickel phosphate below the copper layer. To do so, photoresist is again applied to the substrate layers. Using a photographic mask, the photoresist is exposed and developed such that the copper in areas **3**, **13** is exposed, while copper in other areas remain shielded by the photoresist. The exposed copper in areas **3**, **13** is then etched to define resistors. The photoresist is then stripped away.
5. Selective gold plating is then done for input and output contact connections, and resource well contact connections, and top surface connections. To do so, photoresist is again applied to both sides of all substrate layers, exposed using photographic mask, and developed. The substrates are then plated with nickel and gold. After the plating, the remaining photoresist is stripped.
6. Slots are then milled through all of the substrates. After milling, the plates are cleaned by rinsing in alcohol, and then in hot (70° F.) distilled water and vacuum baked for 1 hour at 149° C.
7. The final assembly step includes bonding of the dielectric layers using the fusion process described in the '374 and '677 patents. This bonding may be done at a pressure of 250 PSI and a temperature of 375° C. Slots may then be milled in the module assembly, opening the formed cavities (i.e., cavity **17**). That is, the cavity opening **475** in the top layer **400** may be formed after fusion bonding. The individual modules can be de-paneled by machining.

Via holes used in forming interconnections between substrate layers and between sides of a substrate may present a degradation in performance if they are not compensated for by means of electromagnetic modeling and analysis. Generally speaking, these via holes may be modeled as vertical slabline transmission lines (FIG. **13**). To provide controlled impedance interconnections in the Z-plane, the teachings of "Microwave Transmission Line Impedance Data", M. A. R. Gunston., pp 63-82; Van Nostrand Reinhold Company, 1971 may be followed. The example coupler assembly disclosed herein includes, among other things, wide bandwidth directional couplers and wide bandwidth quadrature couplers. Wide bandwidth directional couplers are usually synthesized from the formulas given by, e.g., "General Synthesis Of Asymetric Multi-Element Coupled-Transmission-Line Directional Couplers", R. Levy, IEEE Trans. MTT-S, Vol. MTT-11, No. 4, pp226-237; July 1963; and "Tables For Asymetric Multi-Element Coupled-Transmission-Line Directional Couplers", R. Levy, IEEE Trans. MTT-S, Vol. MTT-12, No. 3, pp. 275-279; May 1964. Wide bandwidth quadrature couplers, on the other hand, can be synthesized from the tables given in, e.g., "Theory And Tables Of Optimum Symetrical TEM-Mode Coupled-Transmission-Line Directional Couplers", E. G. Cristal and L. Young, IEEE Trans. MTT-S, Vol. MTT-13, No. 5, pp544-558; September 1965. Another choice is to follow the teaching set forth in "Four Port Networks Synthesized From Interconnection Of Coupled And Uncoupled Sections Of Line Lengths", Joseph D. Cappucci., U.S. Pat. No. 3,761,843; Sep. 25, 1973. The U.S. Pat. No. 3,761,843 patent discloses how to synthesize wide bandwidth couplers from a series of coupled and uncoupled striplines. In this case, a series of uncoupled interconnections are combined with a series of coupled sections to form a broad bandwidth quadrature coupler. Additionally, the non-uniform, coupled structures defined in "The Design And Construction Of Broadband, High Directivity, 90-Degree Couplers Using Nonuniform Line Techniques", C. P. Tresselt., IEEE Trans. MTT-S, Vol. MTT-14, No. 12, pp. 647-656; December 1966; and "The Design And Computed Performance Of Three Classes Of Equal-Ripple Nonuniform Line Couplers", C. P. Tresselt, IEEE Trans. MTT-S, Vol. MTT-17, No. 4, pp. 218-230; April 1969, may be stacked and connected in tandem, vertically, to provide very wide band performance, characterized by a high pass frequency response.

A number of embodiments of the present invention have been described.

Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Another embodiment is shown in FIGS. **14-19**. These figures include a circuit block diagram (FIG. **14**), top, side, and bottom views of a completed module (FIG. **15**), top and bottom metallizations for three substrate layers (FIGS. **16-18**), and a flange layer **19** of an alternative embodiment. The alternative embodiment of FIG. **14** includes a second resource well **40** located at the input side of the circuit **1400**.

The circuitry shown in FIG. **14** includes circuit elements and connections **9-14**, **16**, **17**, **20-21**, **30-37** substantially identical to those of FIG. **2**. The embodiment **1400** also includes a modified input stage **50-66** and a second resource well **40**. The input stage receives a RF signal at input **50**. The signal is transformed from 50 ohms to 12.5 ohms by transformer **51** and the output signal is provided to a contact **52** at resource well **40**. Additional devices (e.g., a diode, resistor, transistor, or simple bridging connection) may be coupled between terminals **52** and **64** of the resource well **40**. The signal **52**, as transformed by any device in resource well **40**, is provided to the terminal **64** and, from there, to DC block coupler **59** and then to signal coupler **61**. The outputs **62-63** of the signal coupler **61** are provided to contacts **65-66** in the resource well **17**. DC bias may be provided through top surface contact points **36-37**, **54**, **80-87**. Similarly, a DC bias may be provided at input **54** connected to quarter wave stripline **53**, and input **36** connected to quarter wave stripline **8** and input **37** connected to quarter wave stripline **9**. Substrate layers **1600**, **1700**, **1800** and flange plate **1900** may be manufactured and bonded in accordance with the process described for the implementation of FIG. **2**. Other features of the substrate layers **1600**, **1700**, **1800**, and flange plate **1900** follow from descriptions given with respect to layers **400**, **500**, **600**, and flange plate **700**.

Circuit Module With Adjustable Microstrip Circuitry

FIG. **20** shows an embodiment of a circuit module assembly **2000** suitable for use in power amplification applications and in which the embedded signal processing circuitry includes both fixed stripline circuitry and adjustable microstrip signal processing circuitry. The microstrip circuitry is formed by printing (i.e., depositing and etching metal) on one side of a substrate layers. In module **2000**, that microstrip circuitry remains exposed to the air following bonding of the assembly and a ground plane is on an opposing side of the substrate layer containing that circuitry. The fixed signal processing circuitry includes stripline circuitry which is between two substrate layers the two substrate layers are further positioned between ground planes.

Signal processing characteristics of the adjustable signal processing circuitry may be altered by the connection of circuitry components to signal contacts on an exposed surface of a substrate layer. More particularly, the assembly **2000** includes inputs **2001** and outputs **2002** that are coupled to fixed signal processing circuitry embedded in substrate regions **2003** and **2004**. Signals from the fixed signal processing circuitry are coupled to adjustable signal processing circuitry formed in regions **2005** and **2006** from metal deposited and etched on a surface of a substrate layer and from a ground plane embedded on an opposing surface. Signals from that adjustable circuitry are, in turn, coupled to signal connections adjacent the resource well **2007**. A power amplifier or other circuitry may be added in the resource well **2007** post-bonding of the assembly **2000**. The circuitry added in the resource well **2007** may be thermally coupled to a metallic flange layer exposed within the resource well **2007** and to electrical signal contacts at edges of the resource well. The electrical contacts at the edge of the well **2007** provide for coupling of the circuitry added in the well **2007** to the adjustable signal processing circuitry formed in regions **2005** and **2006**. By the addition of circuit components to signal contacts exposed on the surface of regions **2005**, **2006**, the electrical characteristics of the adjustable circuitry in the regions **2005**, **2006** may be changed.

FIG. **21** shows the assembly of FIG. **20** with circuit components added. For example, FIG. **21** shows the assembly **2000** with a power transistor **2110** placed within the resource well **2007**, chip capacitors **2102-2107**, resistors **2108** and interconnecting copper foil **2109** added to in the surface regions **2005**, **2006**. The added circuitry **2102-2109** may perform the function of impedance matching between the transistor **2110** and fixed embedded circuitry fashioned in regions **2003**, **2004**.

FIGS. **22**A, **22**B, and **22**C are top, bottom and side views of the structure **2000**. As seen in FIG. **22**C, the assembly **2000** is formed from three layers, a metal flange layer **2210**, an intermediate composite substrate layer **2220**, and a top composite substrate layer **2230**. FIGS. **23**A, **23**B, **24**A, **24**B, **25**A and **25**B show top and bottom views of layers **2210**, **2220** and **2230**. The process used for construction of the layers **2210**, **2220** and **2230** can be the same as for construction of, e.g., the layers **400**, **500** and **700** of FIG. **1**. Furthermore, although the embodiment **2000** includes only a single intermediate layer **2220**, implementations may have multiple intermediate layers, each including embedded circuitry, and including conductive which may be connected to each other by interconnecting vias.

FIG. **26**A shows another implementation of a coupler module configured such that multiple power amplifiers may be added within the module's resource well. FIG. **26**B shows the module of FIG. **26**A with circuit elements added to microstrip circuitry formed on the module. FIGS. **27-30** show the construction of layers of the module of FIGS. **26**A and **26**B.

It is further noted that although fluoropolymer composite substrate layers have been disclosed as one embodiment, implementations may use other types of substrate layers, e.g., ceramic substrate layers. Similarly, while fusion bonding is preferable for fluoropolymer composite substrate layers, in some implementations, other bonding methods may be used (e.g., adhesive bonding films). Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A dielectric assembly comprising:

a plurality of substrate layers bonded together in a stacked arrangement wherein said substrate layers comprising embedded signal processing circuitry, said embedded signal processing circuitry comprising fixed signal processing circuitry and adjustable signal processing circuitry;

a signal input and a signal output each connected to the embedded signal processing circuitry; and

a cavity formed through the plurality of substrate layers, said cavity being configured to receive a circuit element added to the assembly after the bonding of the substrate layers and said cavity exposing signal connection terminals connected to the embedded signal processing circuitry to enable connection of the added circuit element to said embedded signal processing circuitry; and

wherein,

the fixed signal processing circuitry operates to alter electrical characteristics of signals coupled to that circuitry and where the altering characteristics of said fixed circuitry are predetermined at the time of bonding of the substrate layers, and

the adjustable signal processing circuitry operates to alter electrical characteristics of signals coupled to that circuitry and where the altering characteristics of said adjustable circuitry can be changed post-bonding of the substrate layers by the connection of circuit elements to signal path connections on exposed substrate surface regions

the fixed signal processing circuitry comprises at least first and second fixed impedance matching circuitry;

the adjustable signal processing circuitry comprises at least first and second adjustable impedance matching circuitry;

the first fixed impedance matching circuitry is connected between the signal input and the first adjustable impedance matching circuitry;

the second fixed impedance matching circuitry is connected between the signal output and the second adjustable impedance matching circuitry;

the first adjustable impedance matching circuitry is further connected to signal connection terminals in the cavity; and

the second adjustable impedance matching circuitry is further connected to signal connection terminals in the cavity.

2. The assembly of claim **1** wherein:

the adjustable signal processing circuitry comprises microstrip circuitry comprising printed circuitry formed on a side of a first one of the substrate layers, said side of the first substrate layer remaining exposed to air following the bonding of the substrate layers, and said microstrip also being positioned between said exposed air on one side and a ground plane on another side; and

the fixed signal processing circuitry comprising stripline circuitry comprising printed circuitry sandwiched between two substrate layers where said two substrate layers are further positioned between ground planes.

3. The assembly of claim **2** wherein said ground planes are formed by metallizing sides of substrate layers.

4. The assembly of claim **1** wherein said plated metals added to the surface comprises a metal inhibiting oxidation of said metal core.

5. The assembly of claim **1**, wherein signal paths on different substrate surfaces are connected by plated via holes.

6. The assembly of claim **1** wherein the embedded signal processing circuitry further comprises microwave coupler circuitry.

7. The assembly of claim **1** wherein:

the assembly is configured such that the fixed and adjustable signal processing circuitry enables impedance matching between the signal input and signal connection terminals in the cavity and between the signal output and signal connection terminals in the cavity; and

the impedance matching characteristics of the adjustable signal processing circuitry are alterable by the addition of discrete circuit elements to the signal path connections on said exposed substrate surface regions such that, by addition of said discrete circuit elements, a user-configured impedance level is presented to the fixed circuitry at a connection point between the fixed and adjustable circuitry.

8. The assembly of claim **1** wherein said embedded signal processing circuitry further comprises circuitry selected from the group consisting of DC blocking circuitry, DC biasing circuitry, and a RF load termination.

9. The assembly of claim **8** wherein the assembly is configured for addition of an added circuit element to the cavity, said circuit element being selected from the group consisting of a microwave circuit, a transistor, a varactor diode, a PIN diode, and a Shottky diode.

10. The assembly of claim **1** wherein:

the assembly further comprises a flange layer and the cavity exposes a top surface of the flange layer enabling coupling of the circuit element added in the cavity to the flange layer.

11. The assembly of claim **10** wherein said flange layer comprises a substantially homogeneous metal core and said composite substrate layers comprise fluoropolymer composite material.

12. The assembly of claim **1** wherein the substrate layers comprise ceramic substrate layers that are adhesively bonded.

13. The assembly of claim **11** wherein coupling of the added circuit element to the flange layer comprises thermal coupling between said circuit element and the flange layer.

14. The assembly of claim **13** wherein said flange layer consist of said metal core and plated metals added to surfaces of said metal core.

15. A assembly manufactured by a process comprising the steps of:

manufacturing a plurality of substrate layers comprising a top and one or more intermediate layers;

forming a cutout in the intermediate layers such that when the intermediate layers are positioned in a stacked arrangement on top of a bottom layer said cutouts form a cavity through the intermediate layers;

selectively metallizing surfaces of said intermediate layers to form embedded signal processing circuitry comprising fixed signal processing circuitry and adjustable signal processing circuitry, a signal input terminal, a signal output terminal, a first and a second signal connection terminal exposed within said formed cavity, and device connection terminals enabling connection of circuit elements to the adjustable signal processing circuitry;

positioning said intermediate layers in a stacked arrangement between the top and bottom layers and bonding said stacked arrangement of layers

selectively removing regions of the top layer following said bonding to expose the cavity and to expose said device connection terminals; whereby

said cavity enables the addition of a circuit element to the assembly after the bonding of the substrate layers and enables connection of the added circuit element to the embedded signal processing circuitry, and

said device connection terminals enable connection of discrete circuit devices to the adjustable signal processing circuitry.

16. The manufacturing process of claim **15** where said metalicizing of surfaces further comprises forming conductive vias interconnecting said embedded signal processing circuitry elements, signal input terminal, signal output terminal, first and second signal connection terminal and device connection terminals when the plurality of intermediate layers are positioned in a stacked arrangement between said top and bottom layers.

17. The manufacturing process of claim **15** where said bottom layer comprises a flange layer.

18. The manufacturing process of claim **15** where said bottom layer comprises a selectively metallizing substrate layer.

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