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(54) **MEMORY ELEMENT AND ITS METHOD OF FORMATION**

(75) Inventors: **John T. Moore**, Boise, ID (US); **Kristy A. Campbell**, Boise, ID (US); **Terry L. Gilton**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

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See application file for complete search history.

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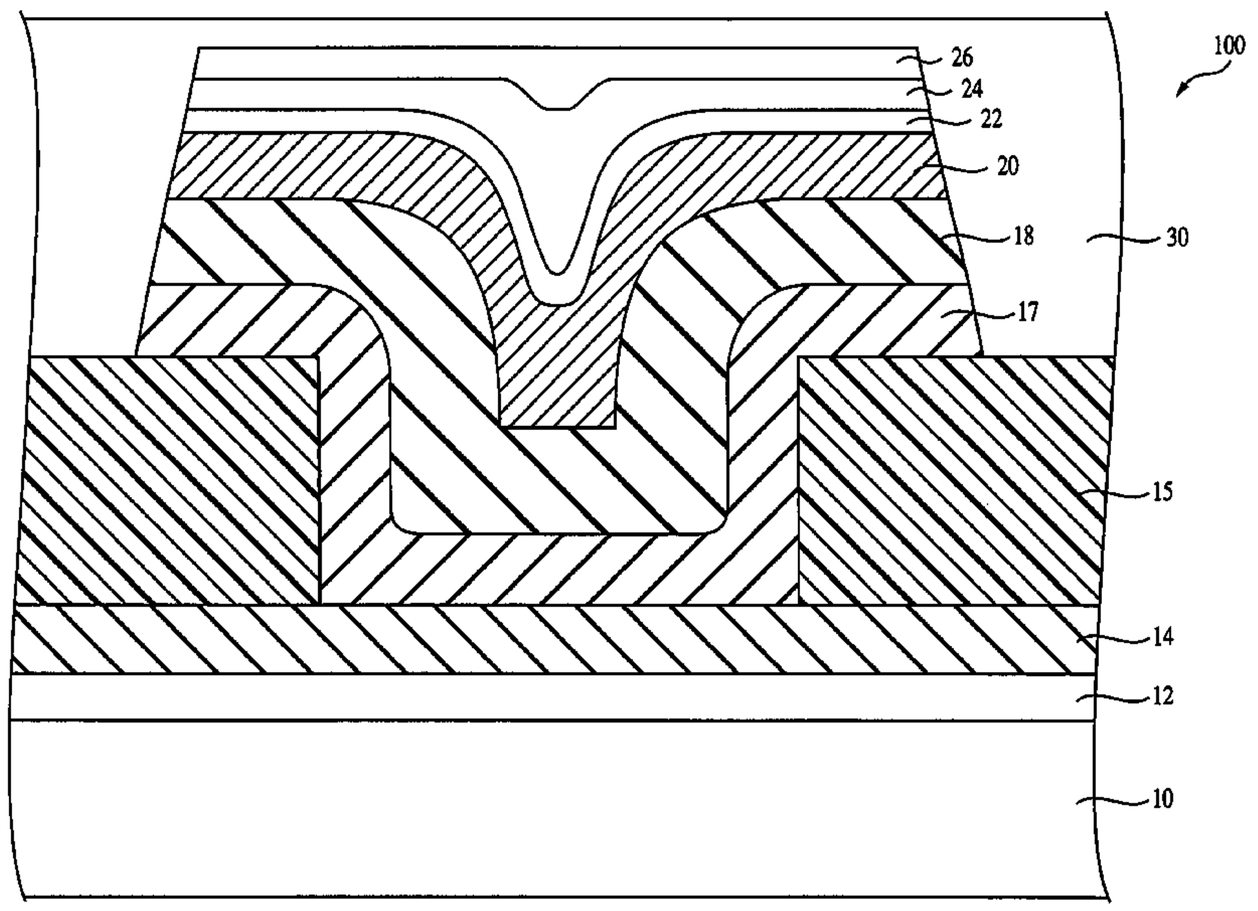
Primary Examiner—Walter Lindsay, Jr.
Assistant Examiner—Thu-Huong Dinh
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro LLP

(57) **ABSTRACT**

A method for controlling silver doping of a chalcogenide glass in a resistance variable memory element is disclosed herein. The method includes forming a thin metal containing layer having a thickness of less than about 250 Angstroms over a second chalcogenide glass layer, formed over a first metal containing layer, formed over a first chalcogenide glass layer. The thin metal containing layer preferably is a silver layer. An electrode may be formed over the thin silver layer. The electrode preferably does not contain silver.

18 Claims, 9 Drawing Sheets



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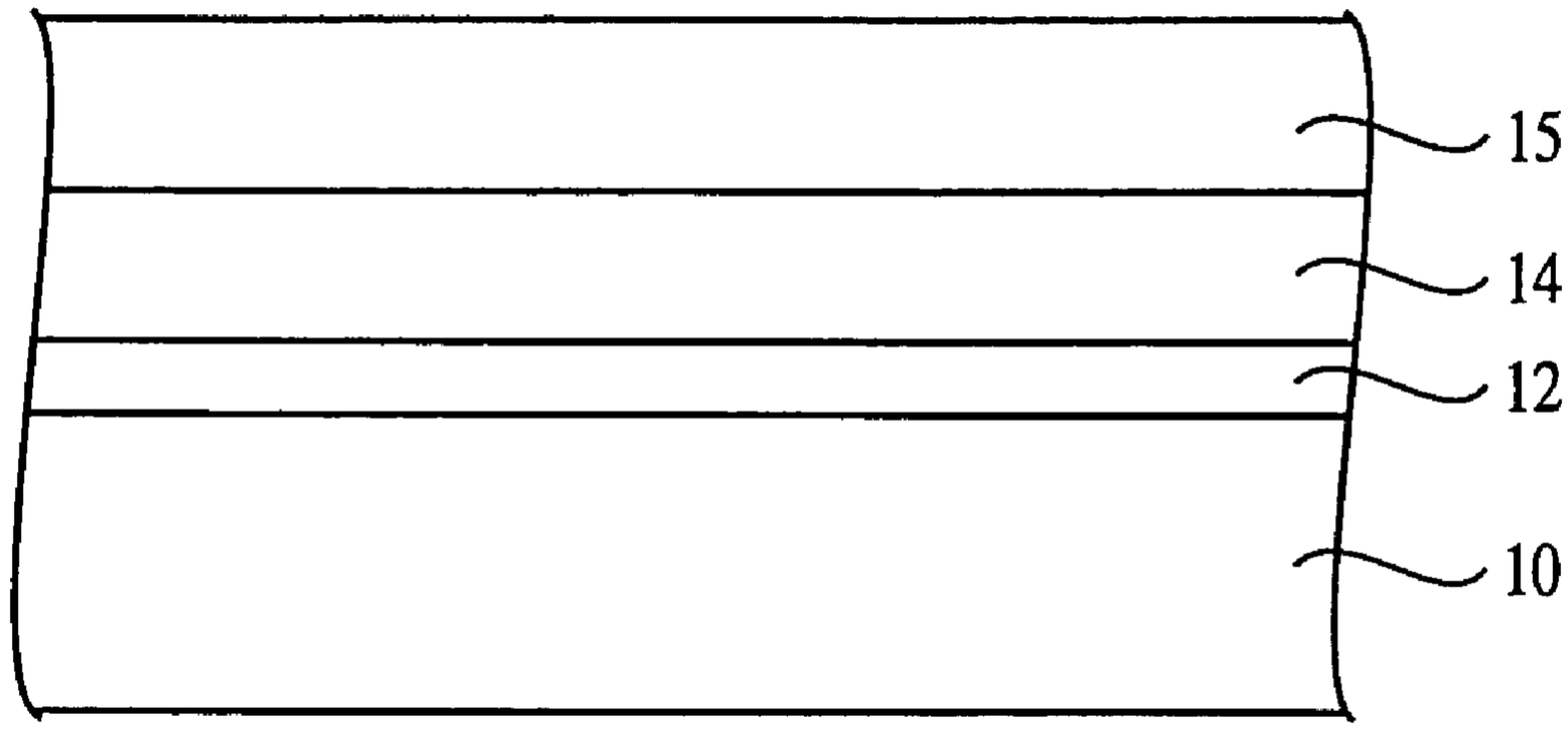


FIG. 1

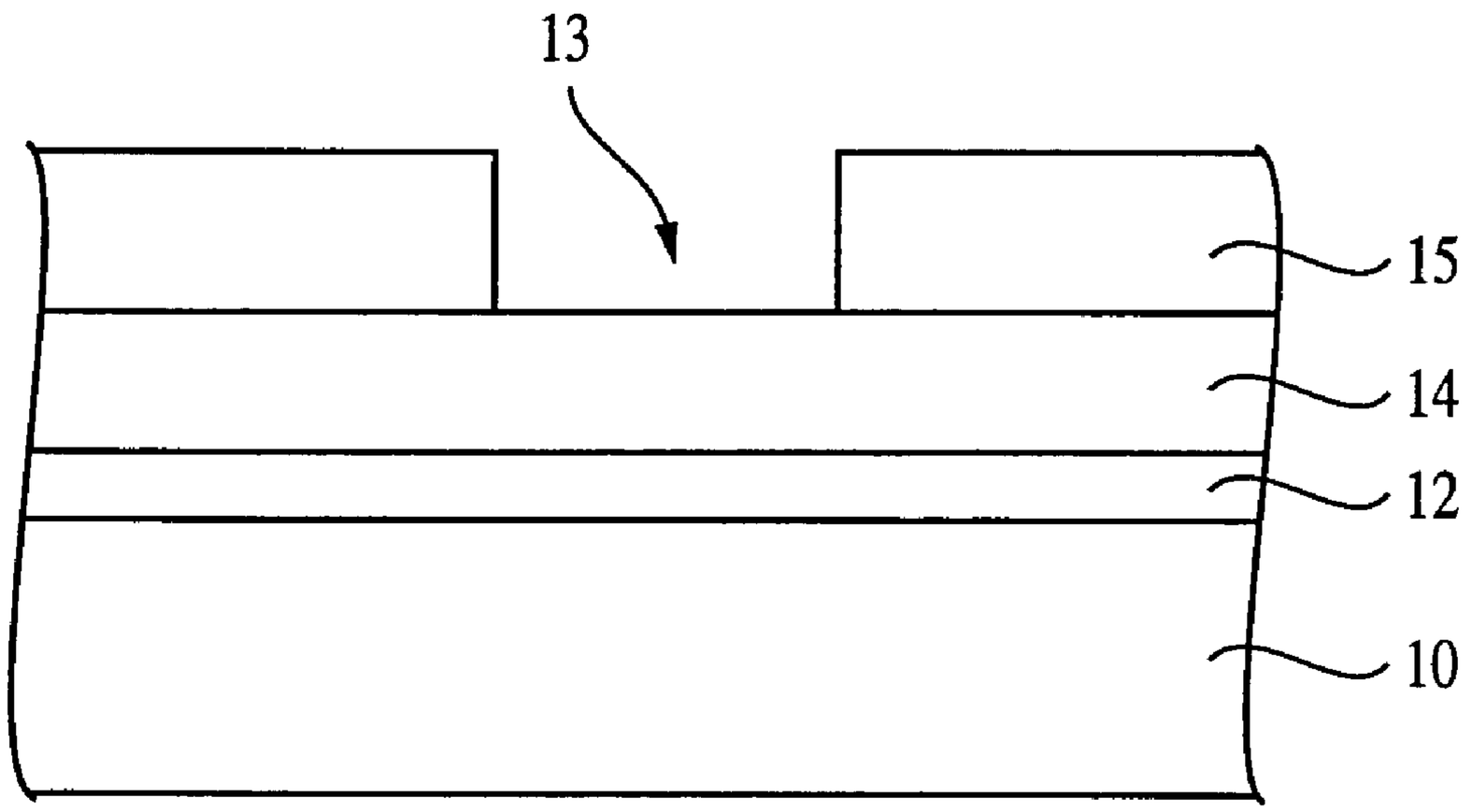


FIG. 2

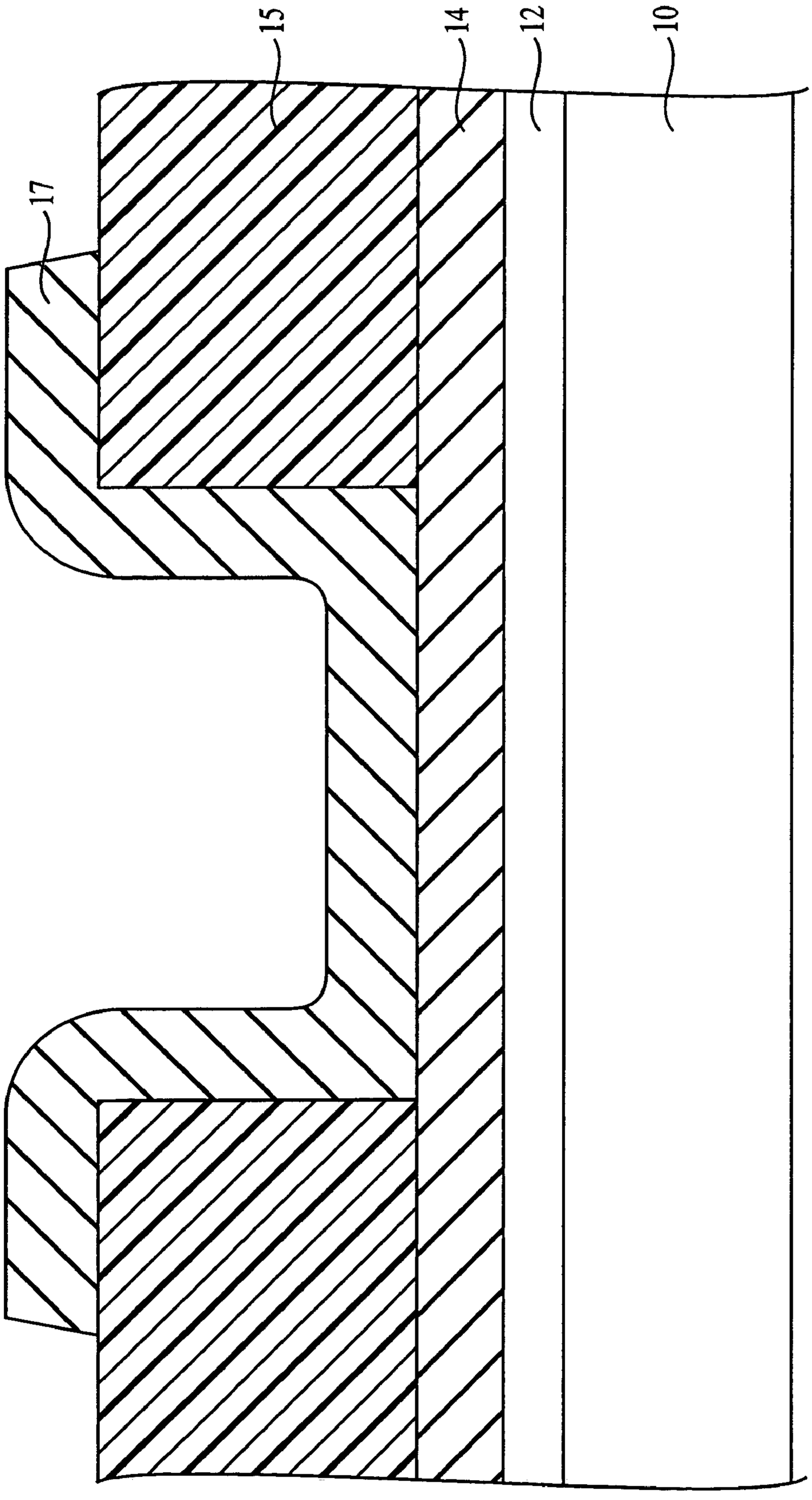


FIG. 3

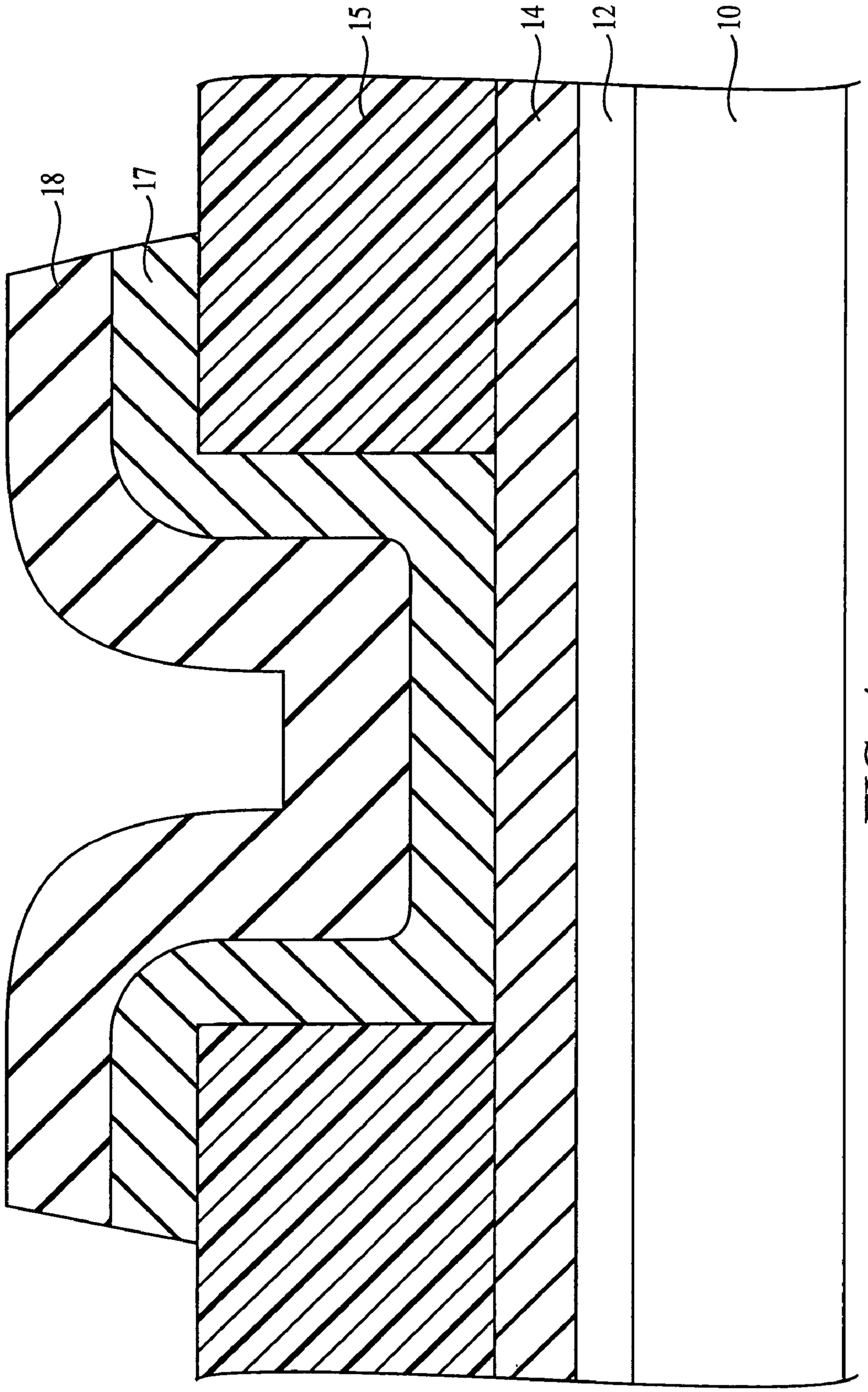


FIG. 4

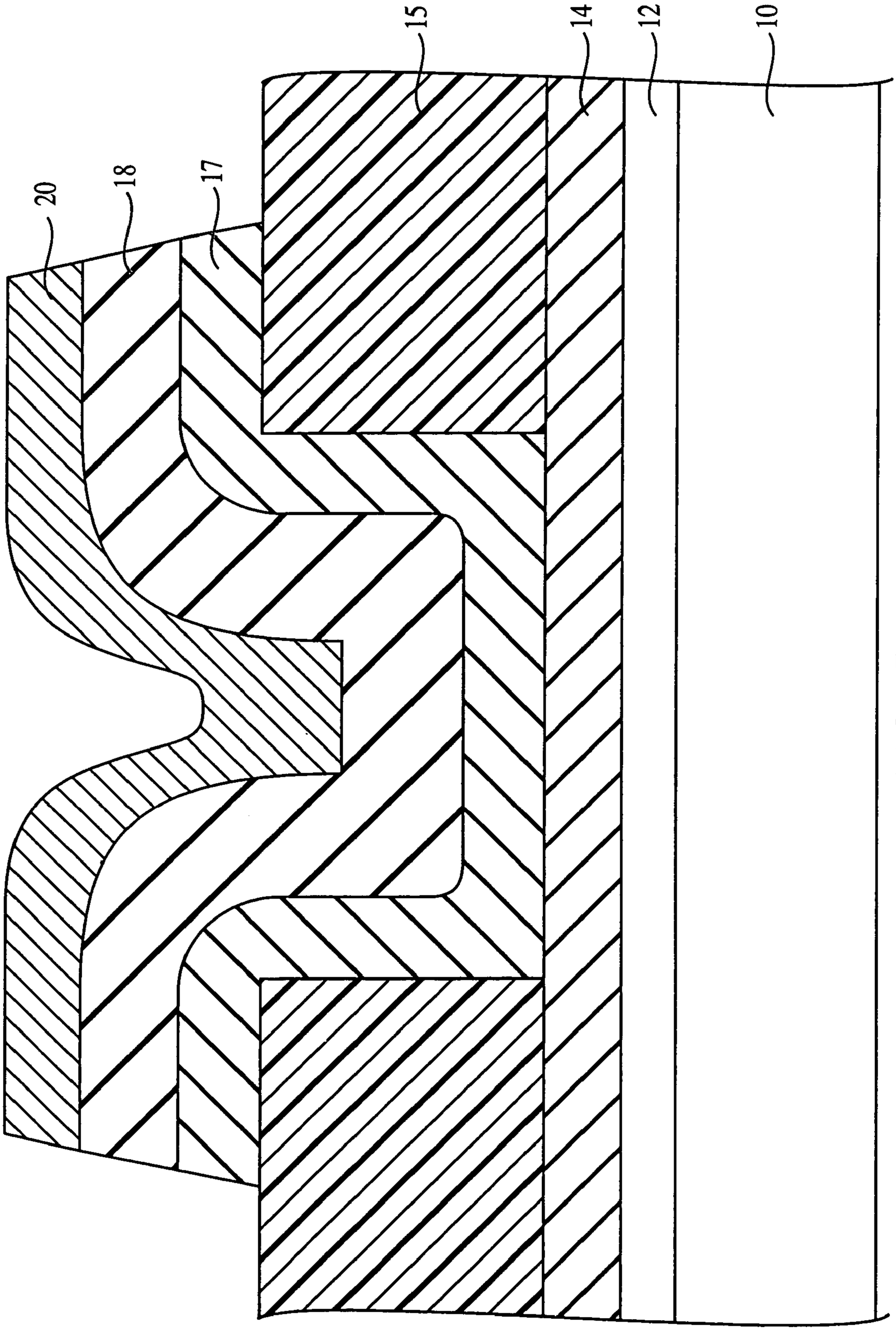


FIG. 5

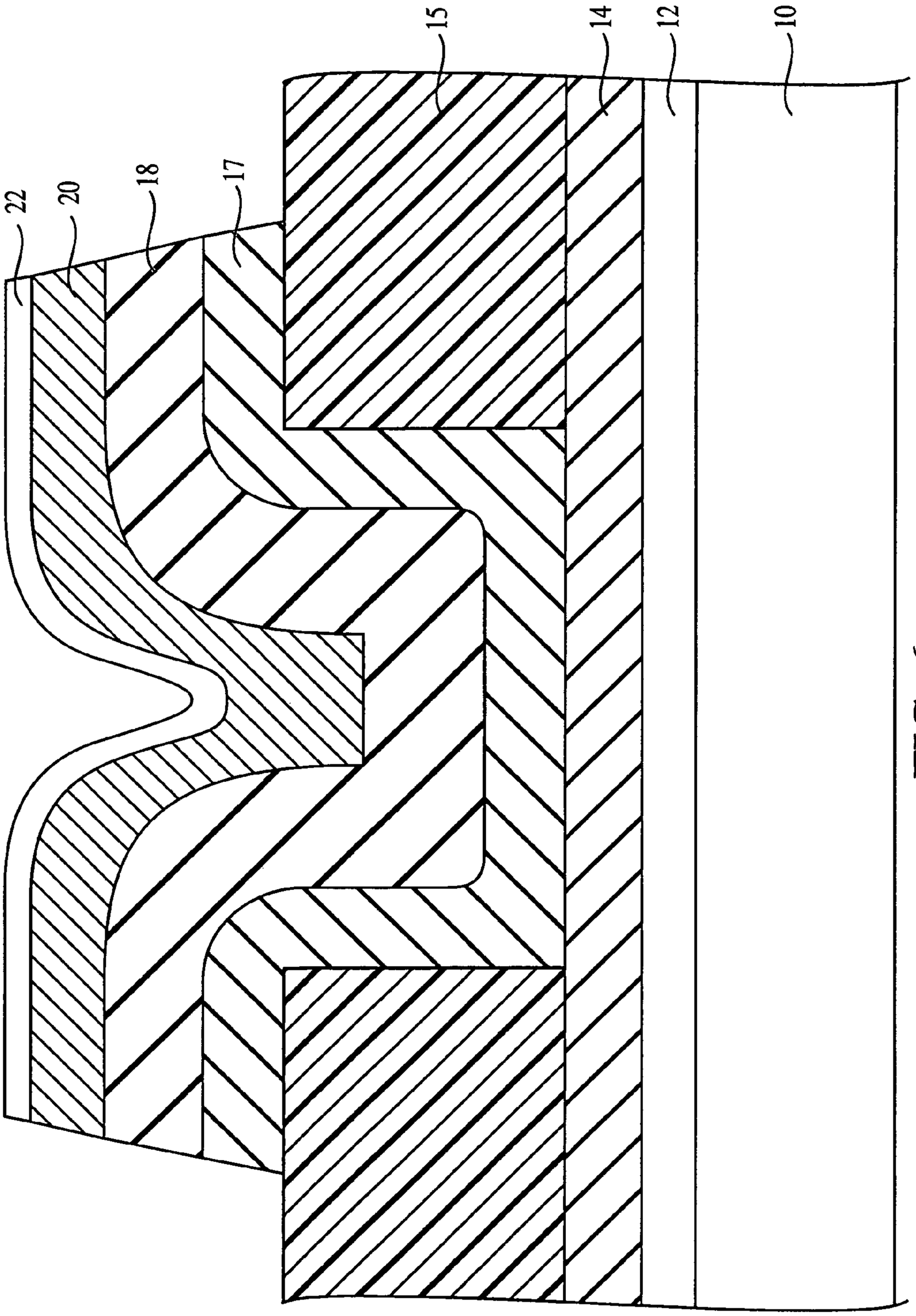


FIG. 6

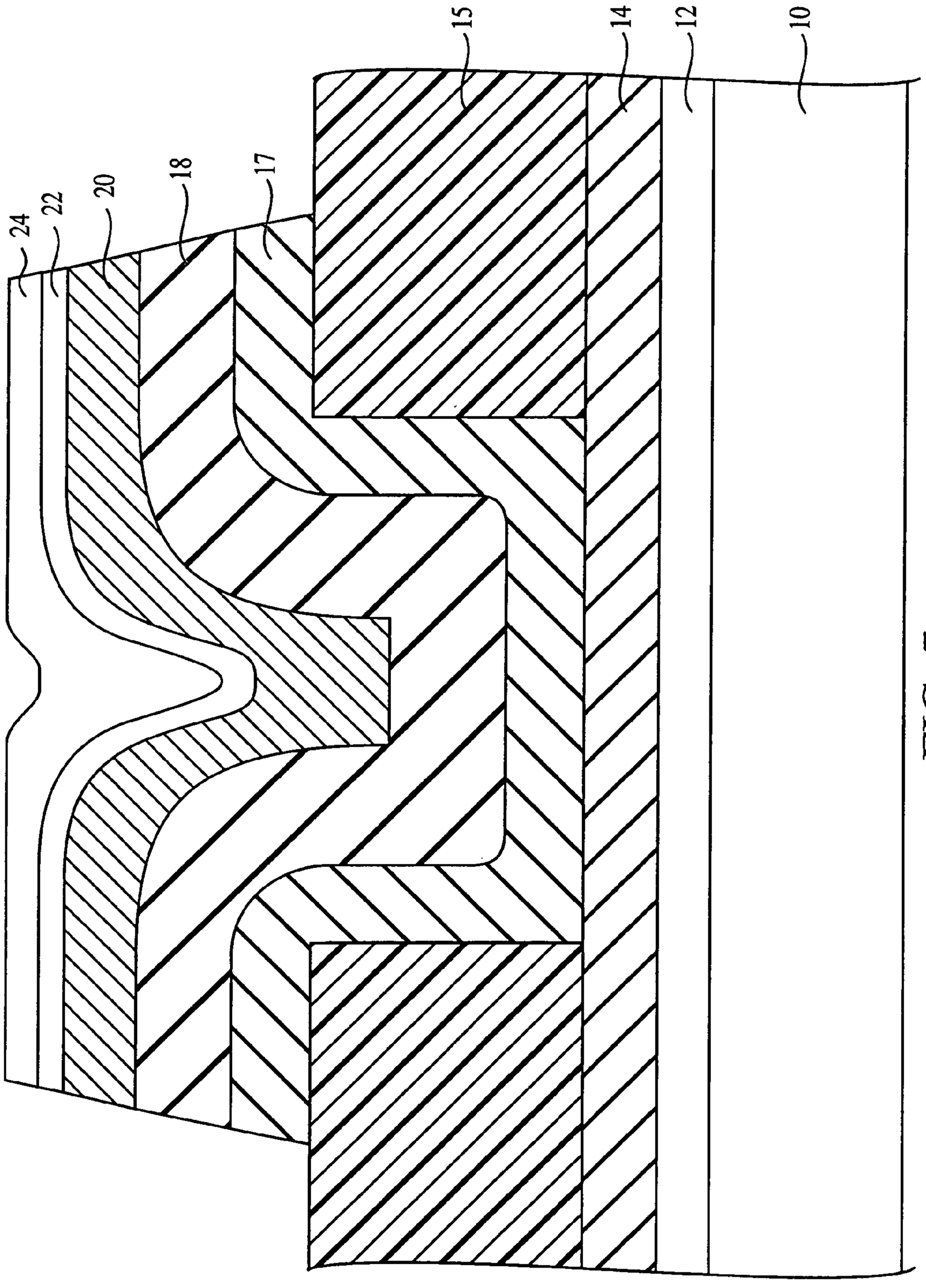


FIG. 7

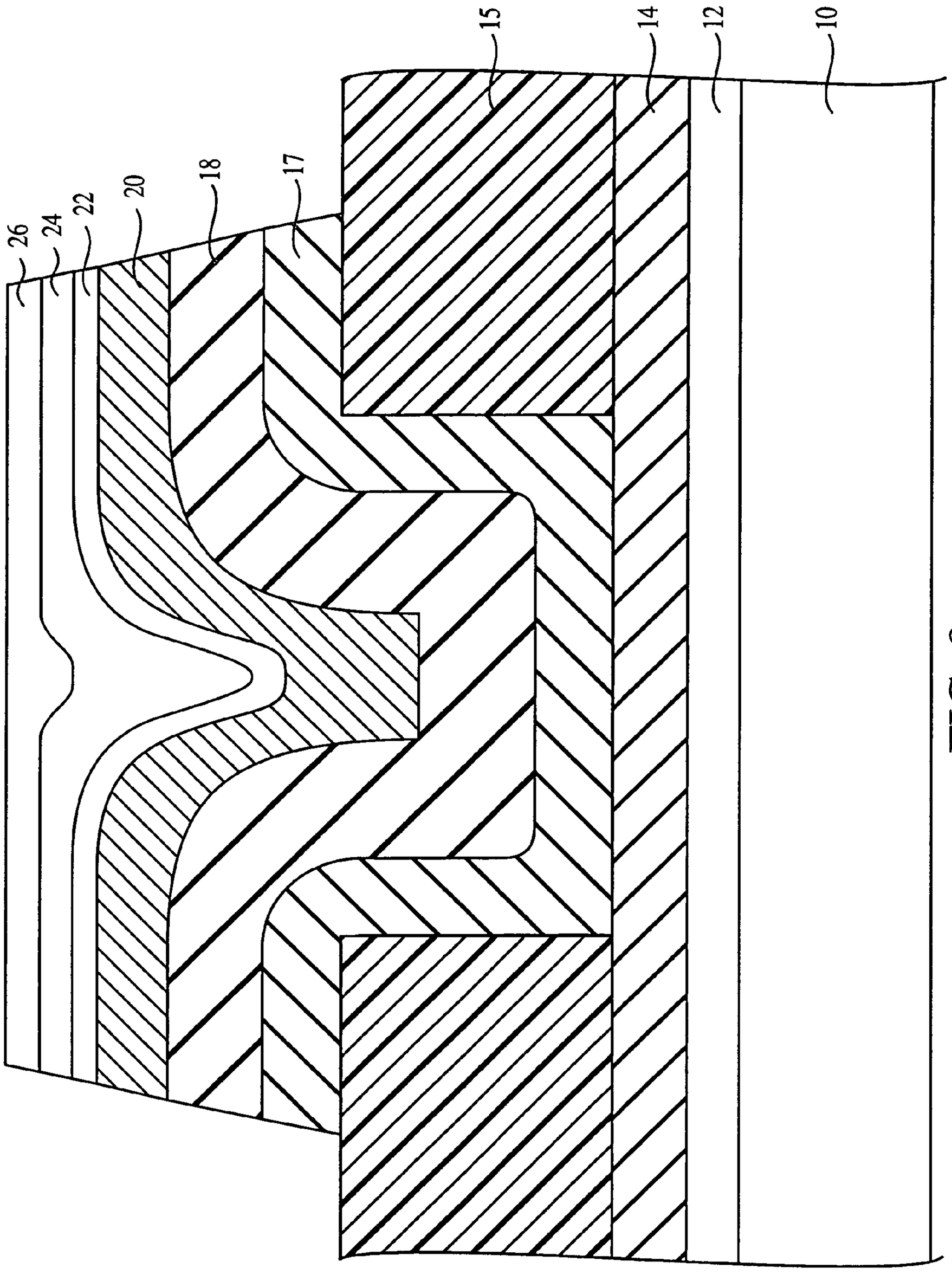


FIG. 8

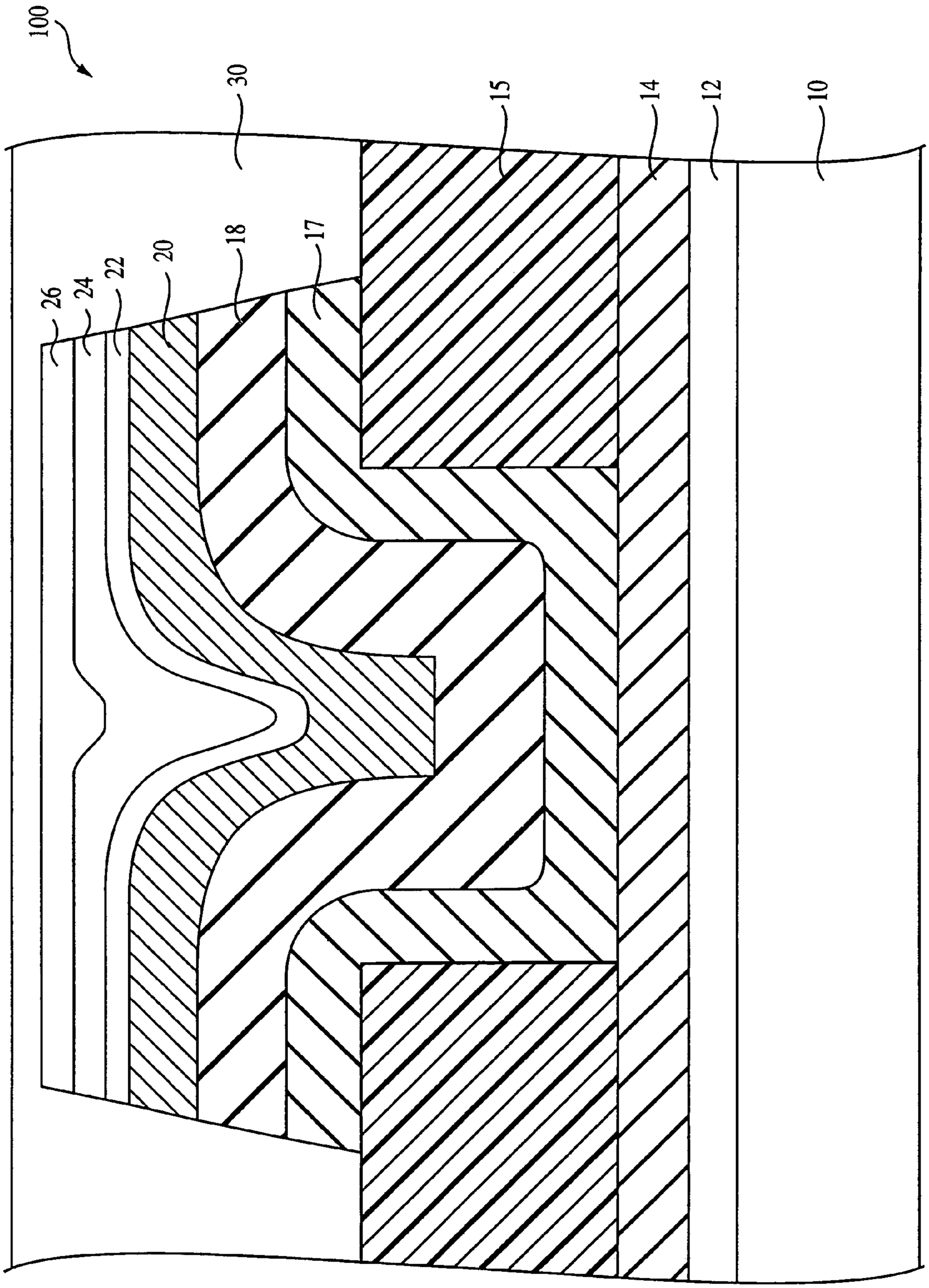
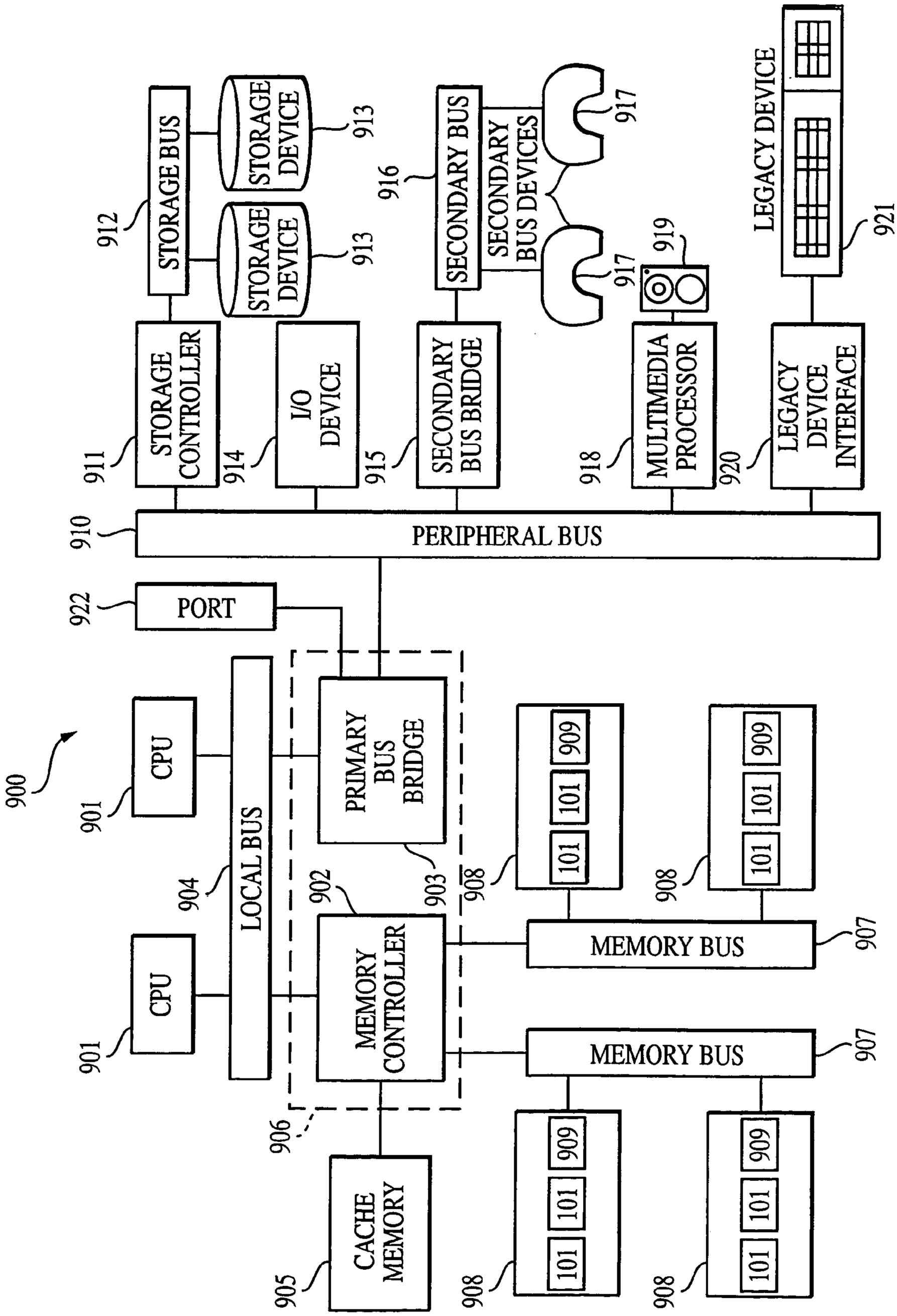


FIG. 9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LOCAL BUS
903
PRIMARY BUS BRIDGE
904
MEMORY CONTROLLER
905
CACHE MEMORY
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MEMORY BUS
908
909
101
910
PERIPHERAL BUS
911
STORAGE CONTROLLER
912
STORAGE BUS
913
STORAGE DEVICE
914
I/O DEVICE
915
SECONDARY BUS BRIDGE
916
SECONDARY BUS
917
SECONDARY BUS DEVICES
918
MULTIMEDIA PROCESSOR
919
920
LEGACY DEVICE INTERFACE
921
LEGACY DEVICE
922
PORT

FIG. 10

MEMORY ELEMENT AND ITS METHOD OF FORMATION

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. patent application Ser. No.: 10/230,212, filed on Aug. 29, 2002 now U.S. Pat. No. 6,864,521, the subject matter of which is incorporated in its entirety by reference herein.

FIELD OF THE INVENTION

The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to controlling silver incorporation into a resistance variable memory element formed using chalcogenide glass.

BACKGROUND OF THE INVENTION

A well-known semiconductor memory component is random access memory (RAM). RAM permits repeated read and write operations on memory elements. Typically, RAM devices are volatile, in that stored data is lost once the power source is disconnected or removed. Non-limiting examples of RAM devices include dynamic random access memory (DRAM), synchronized dynamic random access memory (SDRAM) and static random access memory (SRAM). In addition, DRAMS and SDRAMS also typically store data in capacitors, which require periodic refreshing to maintain the stored data.

Recently resistance variable memory elements have been investigated for suitability as semi-volatile and non-volatile random access memory elements. In a resistance variable memory element, a conductive material, such as silver, is incorporated into a dielectric material. The resistance of the conductive material containing dielectric material can be changed between high resistance and low resistance states. The resistance variable memory element is normally in a high resistance state when at rest. A write operation to a low resistance state is performed by applying a voltage potential across the two electrodes.

One preferred resistance variable material comprises a chalcogenide glass. A specific example is germanium-selenide (Ge_xSe_{100-x}) containing a silver (Ag) component. One method of providing silver to the germanium-selenide composition is to initially form a germanium-selenide glass and then deposit a thin layer of silver upon the glass, for example by sputtering, physical vapor deposition, or other known techniques in the art. The layer of silver is irradiated, preferably with electromagnetic energy at a wavelength less than 600 nanometers, so that the energy passes through the silver and to the silver/glass interface, to break a chalcogenide bond of the chalcogenide material such that the glass is doped with silver. Another method for providing silver to the glass is to provide a layer of silver-selenide on a germanium-selenide glass. A top electrode comprising silver is then formed over the silver-germanium-selenium glass or in the case where a silver selenide layer is provided over a germanium-selenide glass, the top electrode is formed over the silver-selenide layer.

It has been found that over time devices fabricated via the above described methods fail if excess silver from a top silver containing electrode continues to diffuse into the silver germanium-selenium glass or into the silver-selenide layer and eventually into the germanium-selenide glass layer (the primary switching area) below the silver-selenide layer.

Furthermore, during semiconductor processing and/or packaging of a fabricated structure, which incorporates the memory element, the structure undergoes thermal cycling or heat processing. The memory element is also subject to heat during operation of the memory device containing the memory element. Heat processing can result in substantial amounts of silver migrating into the memory element uncontrollably. Too much silver incorporated into the memory element may result in faster degradation, i.e., a short life, and eventually device failure.

Control of the amount of available silver that enters the glass would be highly desirable to prevent premature memory cell failure.

BRIEF SUMMARY OF THE INVENTION

An exemplary embodiment of the present invention includes a method of fabricating a resistance variable memory element and the resulting device wherein silver doping of a chalcogenide glass is controlled. The method includes forming a first chalcogenide glass layer; forming a first silver-selenide layer in contact with the first chalcogenide glass layer; forming a second chalcogenide glass layer in contact with the first silver-selenide layer; and forming a thin silver layer in contact with the second chalcogenide glass layer.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the invention will be better understood from the following detailed description, which is provided in connection with the accompanying drawings.

FIG. **1** illustrates a cross-sectional view of a memory element fabricated in accordance with a first embodiment of the invention and at an initial stage of processing.

FIG. **2** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **1**.

FIG. **3** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **2**.

FIG. **4** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **3**.

FIG. **5** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **4**.

FIG. **6** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **5**.

FIG. **7** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **6**.

FIG. **8** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **7**.

FIG. **9** illustrates a cross-sectional view of the memory element of FIG. **1** at a stage of processing subsequent to that shown in FIG. **8**.

FIG. **10** illustrates a processor-based system having a memory element formed according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

The term "substrate" used in the following description may include any supporting structure including, but not limited to, a plastic or a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor material structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged.

The term "silver-selenide" is intended to include various species of silver-selenide, including some species, which have a slight excess or deficit of silver, for instance, Ag_2Se, $Ag_{2+x}Se$, and $Ag_{2-x}Se$.

The term "chalcogenide glass" is intended to include glasses that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O).

The invention will now be explained with reference to FIGS. **1**–**10**, which illustrate exemplary embodiments of a resistance variable memory element **100** fabricated in accordance with the invention. FIG. **1** depicts a portion of an insulating layer **12** formed over a semiconductor substrate **10**, for example, a silicon substrate. As noted earlier, it should be understood that the resistance variable memory element can be formed on a variety of substrate materials and not just semiconductor substrates. The insulating layer **12** may be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The insulating layer **12** may be formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4), or a low dielectric constant material, among many others.

A first electrode layer **14** is next formed over the insulating layer **12**, as also illustrated in FIG. **1**. The first electrode layer **14** may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, or platinum, among many others. A first dielectric layer **15** is next formed over the first electrode **14**. The first dielectric layer **15** may comprise the same or different materials as those described above with reference to the insulating layer **12**.

Referring now to FIG. **2**, an opening **13** extending to the first electrode layer **14** is formed in the first dielectric layer **15**. The opening **13** may be formed by known methods in the art, for example, by a conventional patterning and etching process. A first chalcogenide glass layer **17** is next formed over the first dielectric layer **15**, to fill in the opening **13**, as shown in FIG. **3**.

According to a first embodiment of the invention, the first chalcogenide glass layer **17** is a germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. The preferred stoichiometric range is between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$. The first chalcogenide glass layer **17** preferably has a thickness from about 100 Å to about 1000 Å and is more preferably about 150 Å.

The use of a metal containing layer, such as a silver-selenide layer, in contact with the chalcogenide glass layer **17** makes it unnecessary to photodope the glass with silver. However, it is possible to also metal (e.g., silver) dope the chalcogenide glass layer, which is in contact with the silver-selenide layer, as an optional variant.

The formation of the first chalcogenide glass layer **17**, having a stoichiometric composition in accordance with the invention may be accomplished by any suitable method. For instance, evaporation, co-sputtering germanium and selenium in the appropriate ratios, sputtering using a germanium-selenide target having the desired stoichiometry, or chemical vapor deposition with stoichiometric amounts of GeH_4 and SeH_2 gases (or various compositions of these gases), which result in a germanium-selenide film of the desired stoichiometry are examples of methods which may be used to form the first chalcogenide glass layer **17**.

Referring now to FIG. **4**, a first metal containing layer **18**, preferably silver-selenide, is deposited over the first chalcogenide glass layer **17**. Any suitable metal containing layer may be used. For instance, other suitable metal containing layers include silver-chalcogenide layers. Silver sulfide, silver oxide, and silver telluride may be suitable silver-chalcogenides for use in combination with any suitable chalcogenide glass layer **17**. For purposes of simplified discussion, metal containing layer **18** will be further described herein as a silver selenide layer. However, it should be understood that other metal containing layers, including those just identified could also be used. A variety of processes can be used to form the silver-selenide layer **18**. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation or depositing a layer of selenium above a layer of silver to form silver-selenide can also be used.

The layers **17** and **18** may be any suitable thickness depending upon the mechanism for switching. Preferably, the thickness of the layers is such that the silver-selenide layer **18** is thicker than the first chalcogenide glass layer **17**. The silver-selenide layer **18** is also thicker than a second chalcogenide glass layer, described below. More preferably, the thickness of the layers are such that a ratio of the silver-selenide layer thickness to the first chalcogenide glass layer thickness is between about 5:1 and about 1:1. In other words, the thickness of the silver-selenide layer **18** is between about 1 to about 5 times greater than the thickness of the first chalcogenide glass layer. Even more preferably, the ratio is between about 3.1:1 and about 2:1 silver-selenide layer thickness to first chalcogenide glass layer thickness.

Referring now to FIG. **5** a second chalcogenide glass layer **20** is formed over the silver-selenide layer **18**. The second glass layer **20** allows deposition of silver above the silver-selenide layer **18**, since silver cannot be directly sputtered on silver-selenide.

The second chalcogenide glass layer **20** is preferably a germamum-selenide glass having a Ge_xSe_{100-x} stoichiometry. The second chalcogenide glass layer **20** may, but need

not, have the same stoichiometric composition as the first chalcogenide glass layer. However, the preferred stoichiometric range is the same as the first glass layer and thus is between about $Ge_{18}Se_{82}$ to about $Ge_{43}Se_{57}$ and is more preferably about $Ge_{40}Se_{60}$.

The thickness of the layers are such that the silver-selenide layer **18** thickness is greater than the thickness of the second chalcogenide glass layer **20**. Preferably, a ratio of the silver-selenide layer **18** thickness to the second chalcogenide glass layer **20** thickness is between about 5:1 and about 1:1. More preferably, the ratio of the silver-selenide layer **18** thickness to the thickness of the second chalcogenide glass layer **20** is between about 3.3:1 and about 2:1 silver-selenide layer **18** thickness to second chalcogenide glass layer **20** thickness. The second chalcogenide glass layer **20** preferably has a thickness between about 100 Å to about 1000 Å and is more preferably 150 Å.

The formation of the second chalcogenide glass layer **20** may be accomplished by any suitable method. For instance, chemical vapor deposition, evaporation, co-sputtering, or sputtering using a target having the desired stoichiometry, may be used.

Referring now to FIG. **6**, silver layer **22** is formed over the second glass layer **20**. The silver layer is preferably between about 50 Å to about 250 Å thick and is more preferably 200 Å thick. The thickness of the second chalcogenide glass layer **20** and the silver layer **22** are preferably such that sufficient silver is available to ensure the resistance between the silver selenide layer **18** and a top electrode (to be described later) is sufficiently low. The use of too much silver, for example, a silver layer having a thickness of greater than about 250 Å limits the functionality of the device at high temperature processing, for example, of about 200° C. Devices having a thin layer of silver (for example, 50 Å) last substantially longer in high temperatures (for example, 200° C.). The silver layer may be deposited by any suitable mechanism, for instance, physical vapor deposition (PVD) or evaporation, however, sputter deposition is preferred.

Referring now to FIG. **7**, a second conductive electrode material **24** is formed over the silver layer **22**. The second conductive electrode material **24** may comprise any electrically conductive material, for example, tungsten, tantalum or titanium, among many others, but does not contain silver.

Referring now to FIG. **8**, an optional tungsten nitride layer **26** may be formed over the second electrode material **24**.

Referring now to FIG. **9**, one or more additional dielectric layers **30** may be formed over the second electrode **24** or alternatively over the tungsten nitride layer **26** and the first dielectric layer **15** (as shown) to isolate the resistance variable memory element **100** from other structures fabricated over the substrate. Conventional processing steps can then be carried out to electrically couple the second electrode **24** to various circuits of memory arrays.

Devices constructed according to the invention, particularly those incorporating a thin layer of silver, having a thickness of between about 50 Å to about 250 Å, underlying an uppermost electrode, shows improved functionality at higher processing temperatures, thereby allowing devices in accordance with the invention to be processed at higher temperatures. Devices according to the invention also show improved functionality at high operating temperatures thus devices according to the invention are more durable. Accordingly, a device in accordance with the invention shows improved durability over conventional resistance variable memory devices.

Although the embodiments described above refer to the formation of only one resistance variable memory element **100**, it must be understood that the invention contemplates the formation of any number of such resistance variable memory elements, which can be fabricated in a memory array and operated with memory element access circuits.

FIG. **10** illustrates an exemplary processing system **900**, which utilizes a resistance variable memory element constructed as described above in a memory device **101**. The processing system **900** includes one or more processors **901** coupled to a local bus **904**. A memory controller **902** and a primary bus bridge **903** are also coupled the local bus **904**. The processing system **900** may include multiple memory controllers **902** and/or multiple primary bus bridges **903**. The memory controller **902** and the primary bus bridge **903** may be integrated as a single device **906**.

The memory controller **902** is also coupled to one or more memory buses **907**. Each memory bus accepts memory components **908**, which include at least one memory device **101** of the invention. Alternatively, in a simplified system, the memory controller **902** may be omitted and the memory components directly coupled to one or more processors **901**. The memory components **908** may be a memory card or a memory module. The memory components **908** may include one or more additional devices **909**. For example, the additional device **909** might be a configuration memory. The memory controller **902** may also be coupled to a cache memory **905**. The cache memory **905** may be the only cache memory in the processing system. Alternatively, other devices, for example, processors **901** may also include cache memories, which may form a cache hierarchy with cache memory **905**. If the processing system **900** include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller **902** may implement a cache coherency protocol. If the memory controller **902** is coupled to a plurality of memory buses **907**, each memory bus **907** may be operated in parallel, or different address ranges may be mapped to different memory buses **907**.

The primary bus bridge **903** is coupled to at least one peripheral bus **910**. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus **910**. These devices may include a storage controller **911**, a miscellaneous I/O device **914**, a secondary bus bridge **915**, a multimedia processor **918**, and a legacy device interface **920**. The primary bus bridge **903** may also coupled to one or more special purpose high speed ports **922**. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system **900**.

The storage controller **911** couples one or more storage devices **913**, via a storage bus **912**, to the peripheral bus **910**. For example, the storage controller **911** may be a SCSI controller and storage devices **913** may be SCSI discs. The I/O device **914** may be any sort of peripheral. For example, the I/O device **914** may be a local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices **917** via to the processing system **900**. The multimedia processor **918** may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers **919**. The legacy device interface **920** is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system **900**.

The processing system **900** illustrated in FIG. **10** is only an exemplary processing system with which the invention may be used. While FIG. **10** illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system **900** to become more suitable for use in a variety of applications. For example, many electronic devices, which require processing may be implemented using a simpler architecture that relies on a CPU **901**, coupled to memory components **908** and/or memory elements **101**. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

The invention is not limited to the details of the illustrated embodiment. Accordingly, the above description and drawings are only to be considered illustrative of exemplary embodiments which achieve the features and advantages of the invention. Modifications and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States:

1. A method of forming a memory element comprising:
forming a first electrode layer over a semiconductor substrate;
forming a dielectric layer over at least a portion of said first electrode layer;
forming a first chalcogenide glass layer over said dielectric layer;
forming a metal-selenide layer over at least a portion of said first chalcogenide glass layer;
forming a second chalcogenide glass layer over at least a portion of said metal-selenide layer;
forming a metal-containing layer over at least a portion of said second chalcogenide glass layer; and
forming a second electrode layer over at least a portion of said metal-containing layer, wherein said first and second electrode layers are in electrical communication with each other.

2. The method of claim **1**, wherein said metal-containing layer is formed having a thickness of between about 50 Å to about 250 Å.

3. The method of claim **1**, wherein said metal-selenide layer is about 1 to about 5 times thicker than said first chalcogenide glass layer.

4. The method of claim **1**, wherein said metal-containing layer comprises silver.

5. The method of claim **1**, wherein said metal-containing layer is a metal-selenide layer.

6. The method of claim **1**, wherein said metal-selenide layer is about 1 to about 5 times thicker than said second chalcogenide glass layer.

7. A method of forming a memory element between two conductive electrodes, said method comprising:
forming a first glass layer comprising a chalcogen;
forming a metal-selenide layer over said first glass layer;
forming a second glass layer comprising a chalcogen over said metal-selenide layer; and
forming a metal-containing layer over said second glass layer.

8. The method of claim **7**, wherein said second metal-containing layer is formed to be about 50 Å to about 250 Å thick.

9. The method of claim **7**, wherein said metal-selenide layer is formed to be about 1 to about 5 times thicker than said first chalcogenide glass layer.

10. The method of claim **7**, wherein said metal-containing layer comprises silver.

11. The method of claim **7**, wherein said metal-containing layer comprises a metal-selenide.

12. A method of forming a memory element between two electrodes comprising:
forming a first and second glass layer, wherein at least one glass layer is in electrical communication with at least one electrode;
forming a metal-selenide layer between said first and second glass layers, wherein said second glass layer is formed over at least a portion of said metal-selenide layer; and
forming a metal-containing layer on one side of said second glass layer, wherein said metal-selenide layer is formed on the opposite side of said second glass layer.

13. The method of claim **12**, wherein said first and second glass layers are chalcogenide glass layers.

14. The method of claim **13**, wherein said metal-selenide layer is about 1 to about 5 times thicker than said second glass layer.

15. The method of claim **12**, wherein said metal-containing layer is formed having a thickness of between about 50 Å to about 250 Å.

16. The method of claim **12**, wherein said metal-selenide layer is about 1 to about 5 times thicker than said first glass layer.

17. The method of claim **12**, wherein said metal-containing layer comprises silver.

18. The method of claim **12**, wherein said metal-containing layer is a metal-selenide layer.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,223,627 B2
APPLICATION NO. : 10/988836
DATED : May 29, 2007
INVENTOR(S) : John T. Moore et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6:

Line 12, “coupled the” should read --coupled to the--;

Line 32, “include” should read --includes--;

Line 46, “also coupled” should read --also be coupled--;

Line 60, “an universal” should read --a universal--;

Line 61, “via to the” should read --via the--; and

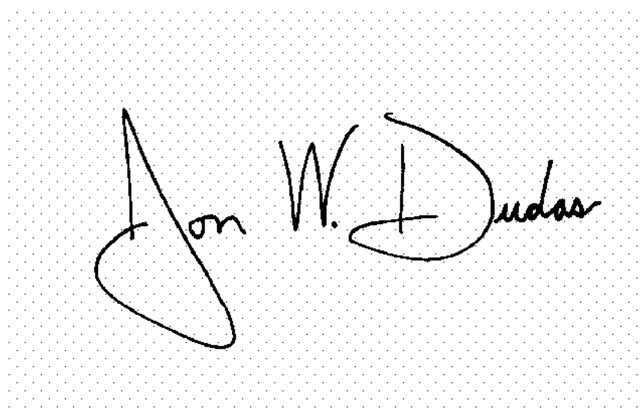
Line 64, “to one additional” should read --to additional--.

Column 7:

Line 15, “system” should read --system--.

Signed and Sealed this

Seventh Day of August, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office