US007179717B2

(12) **United States Patent**
Sandhu et al.

(10) **Patent No.: US 7,179,717 B2**
(45) **Date of Patent: Feb. 20, 2007**

(54) **METHODS OF FORMING INTEGRATED CIRCUIT DEVICES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 86 days.

(21) Appl. No.: **11/136,823**

(22) Filed: **May 25, 2005**

(65) **Prior Publication Data**

US 2006/0270181 A1 Nov. 30, 2006

(51) **Int. Cl.**
H01L 21/76 (2006.01)

(52) **U.S. Cl.** **438/424**; 438/426; 438/427

(58) **Field of Classification Search** 438/424, 438/426, 427
See application file for complete search history.

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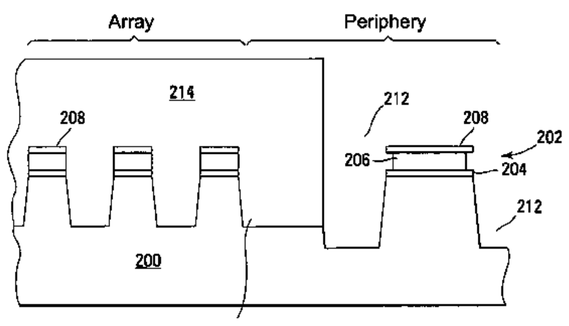
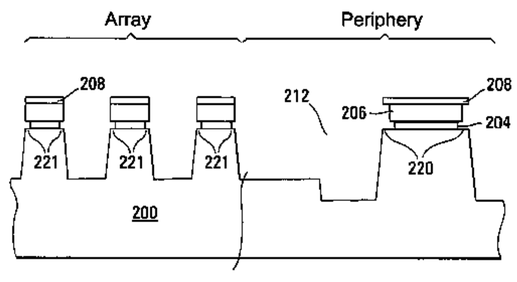
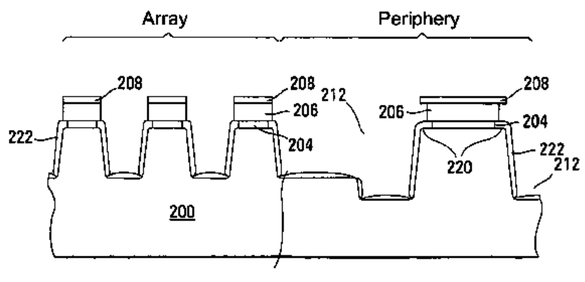
(57) **ABSTRACT**

Forming an integrated circuit device includes forming a hard mask layer overlying a semiconductor substrate. The hard mask layer is patterned to expose portions of the substrate and edges of the hard mask layer. Exposed portions of the substrate are removed. A first portion of the substrate is covered with a photoresist layer while leaving a second portion exposed. The exposed edges of the hard mask are recessed to expose a third portion of the substrate. Recessing the exposed edges of the hard mask includes using at least a dry-etch chemistry. The exposed second and third portions of the substrate are oxidized.

48 Claims, 6 Drawing Sheets







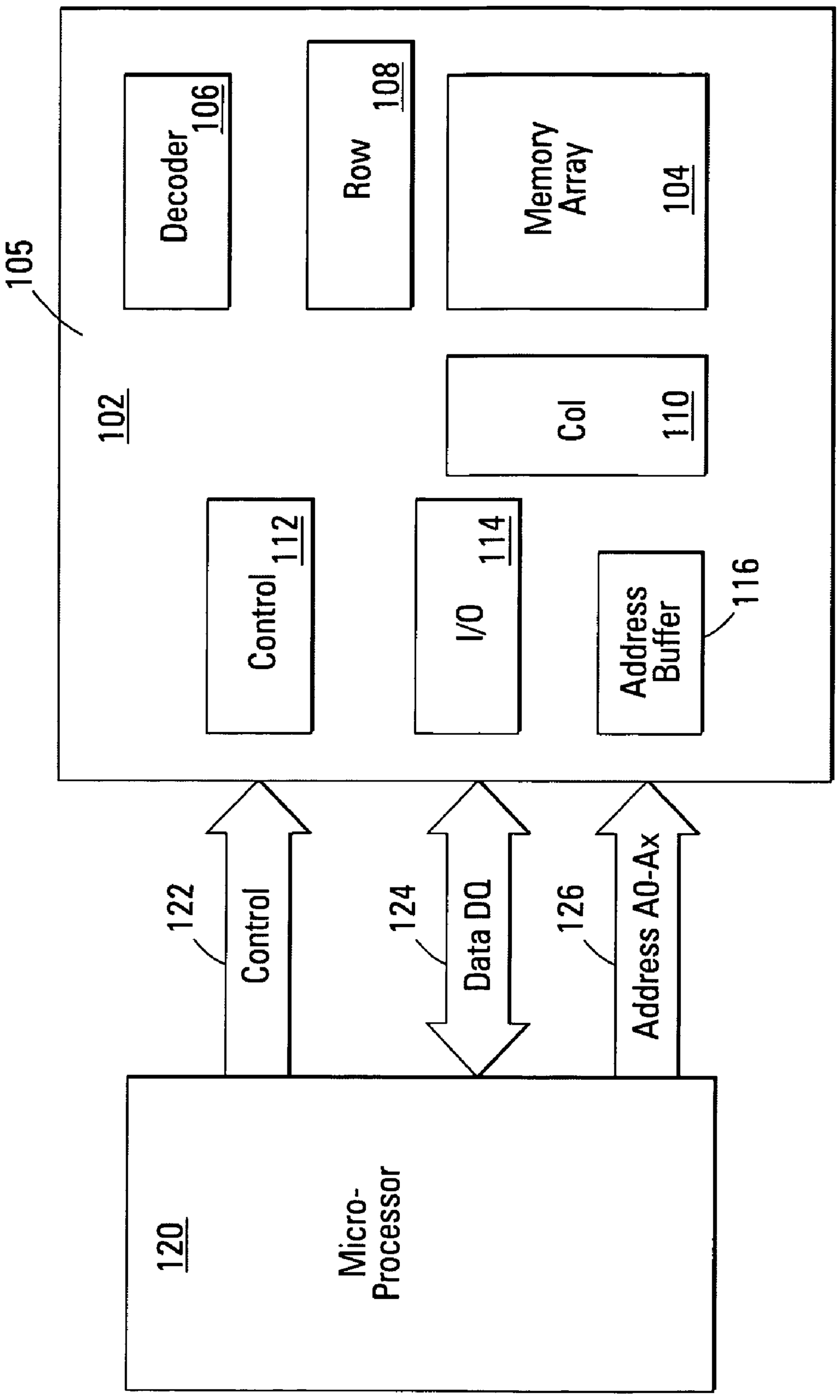

105
102
Decoder 106
Row 108
Memory Array 104
Col 110
Control 112
I/O 114
Address Buffer 116
122
Control
124
Data DQ
126
Address A0-Ax
120
Micro-Processor

FIG. 1

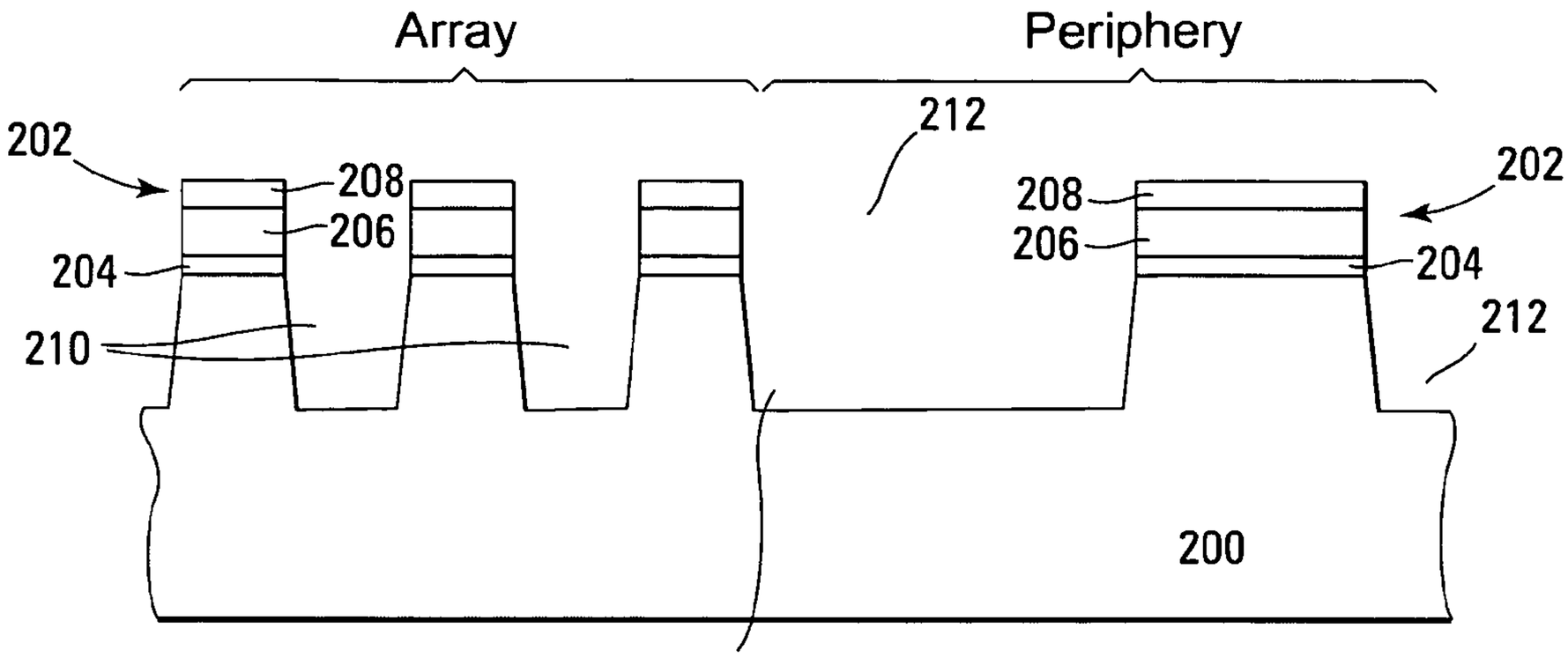
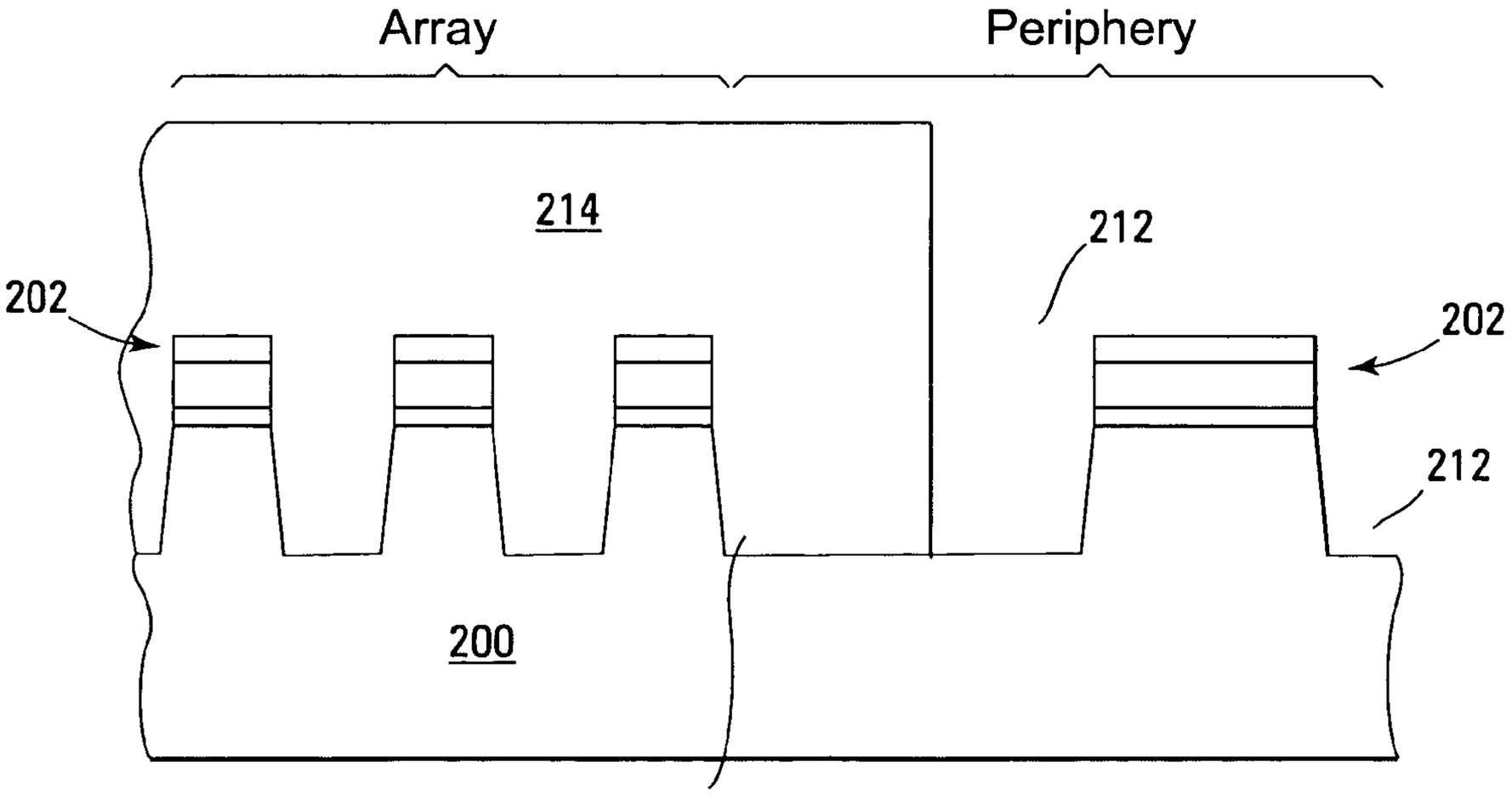

Array
Periphery
202
208
206
204
210
212
202
208
206
204
212
200

FIG. 2A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Periphery
214
212
202
202
212
200

FIG. 2B

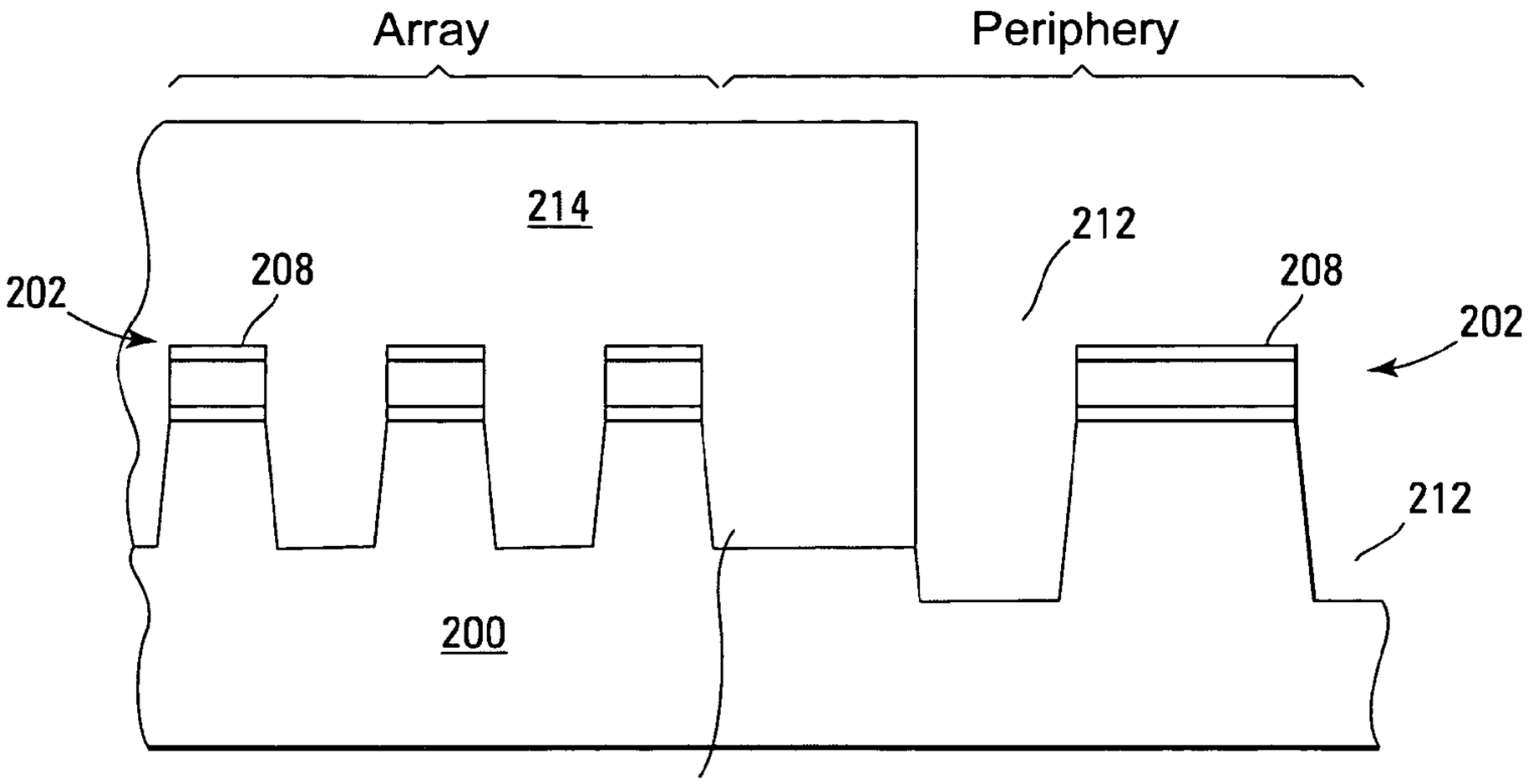
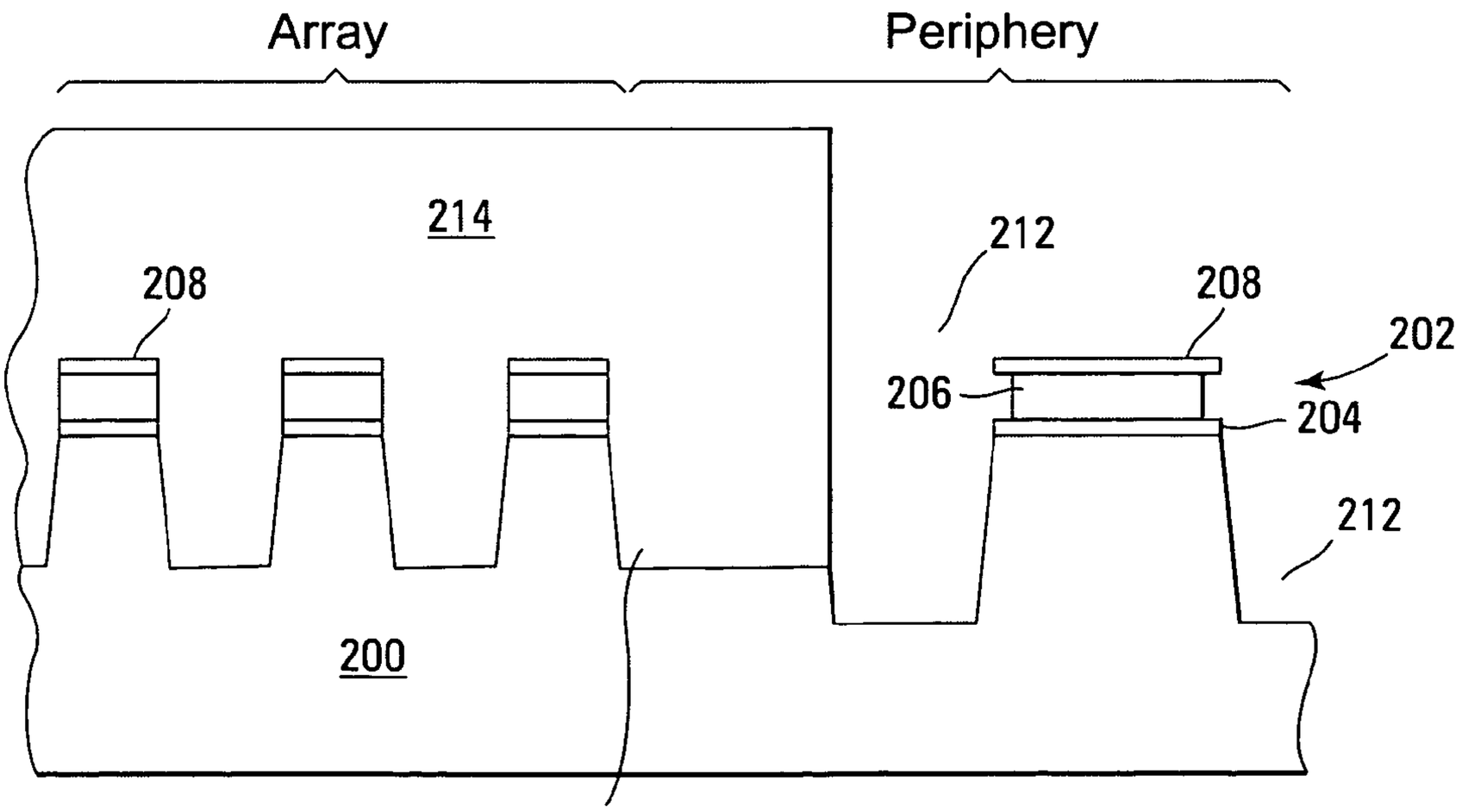

Array
Periphery
214
212
208
208
202
202
212
200

FIG. 2C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Periphery
214
212
208
208
202
206
204
212
200

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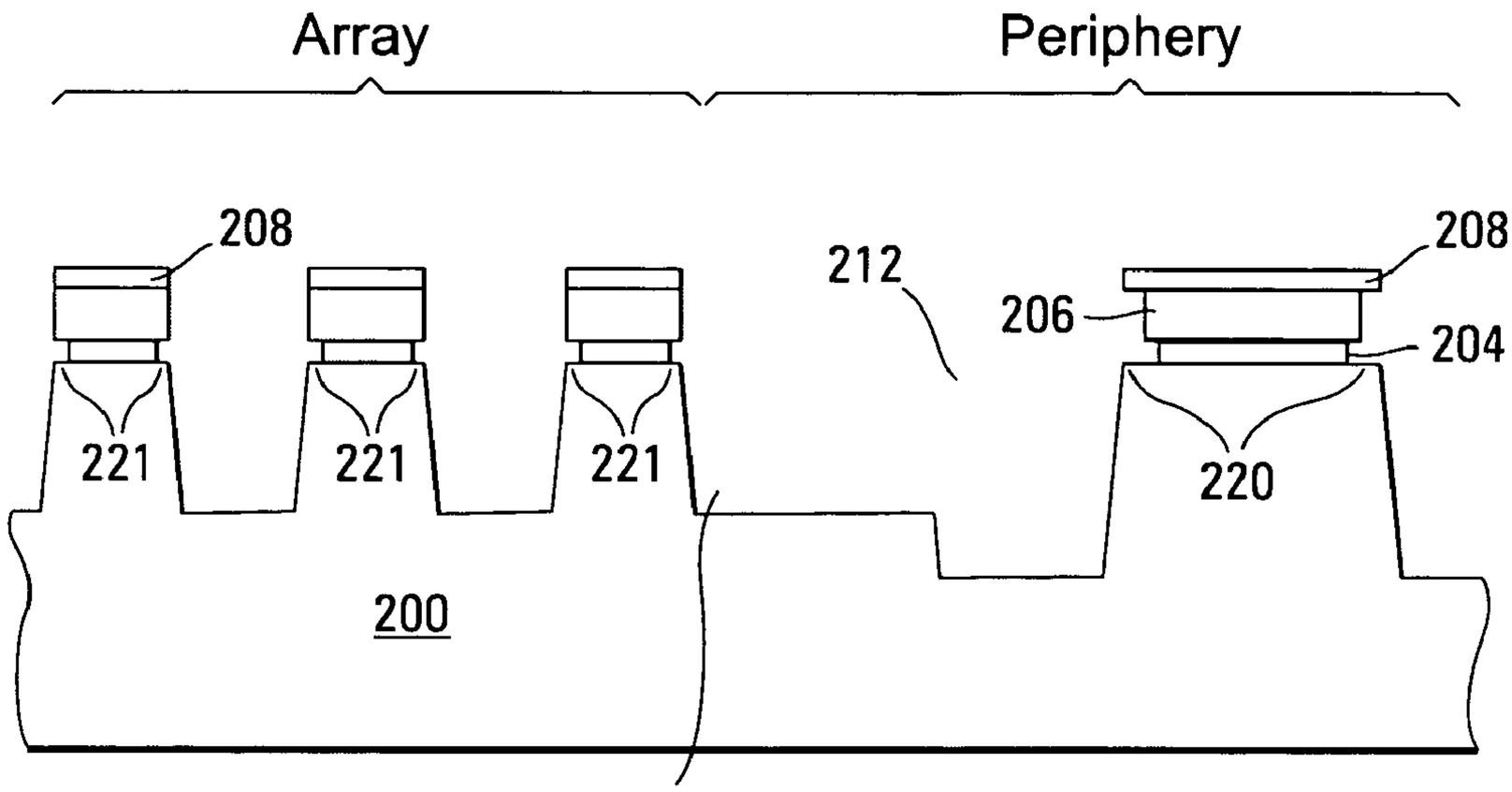

Array
Periphery
208
212
208
206
204
221
221
221
220
200

FIG. 2E

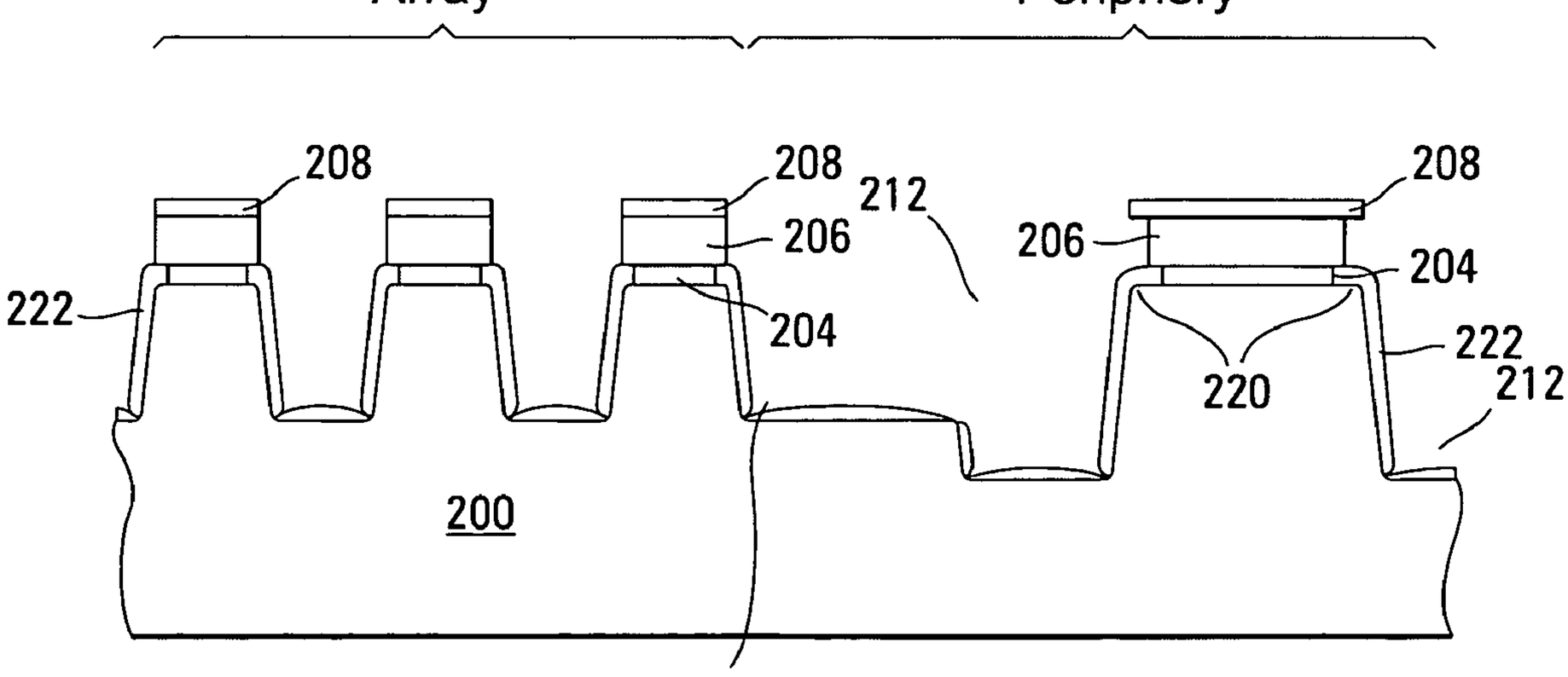
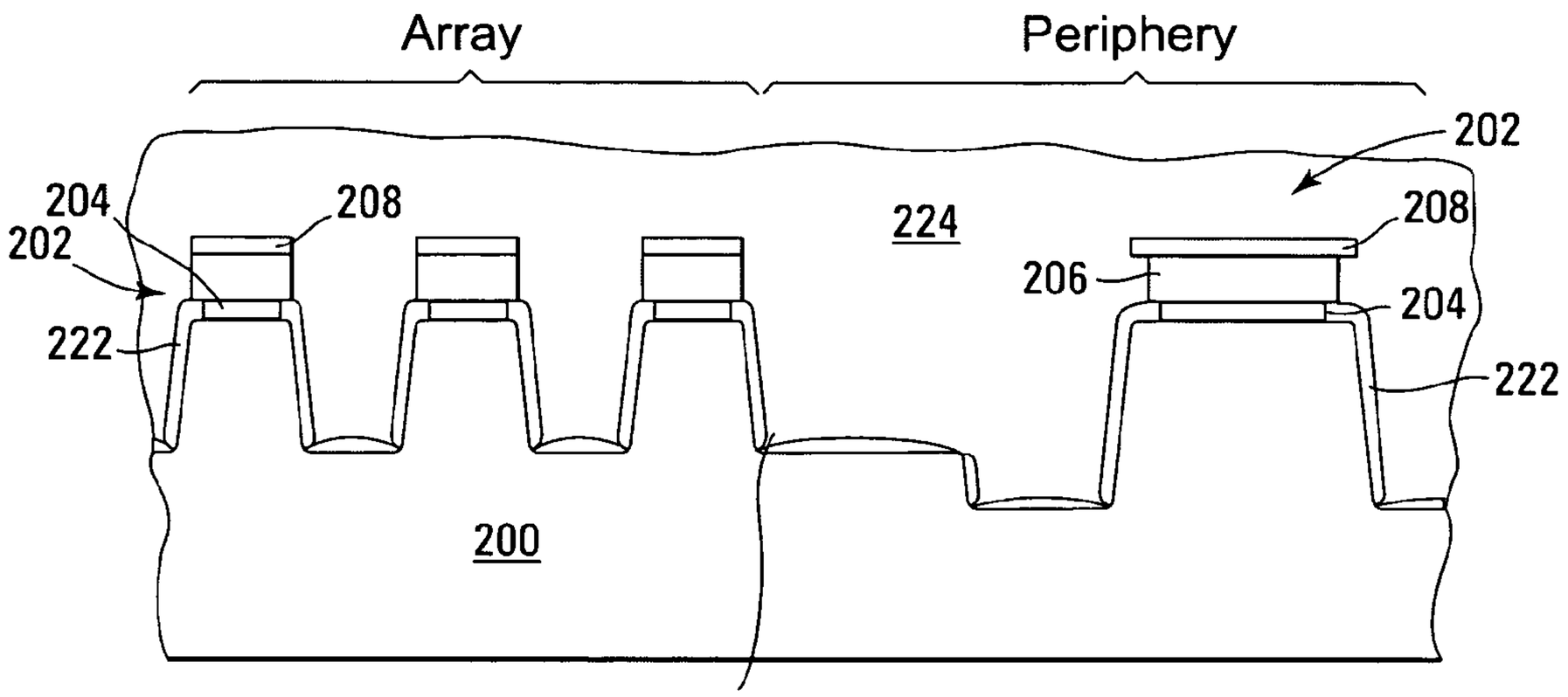

Array
Periphery
208
208
212
208
206
206
204
222
204
222
220
212
200

FIG. 2F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Periphery
202
204
208
202
224
208
206
204
222
222
200

FIG. 2G

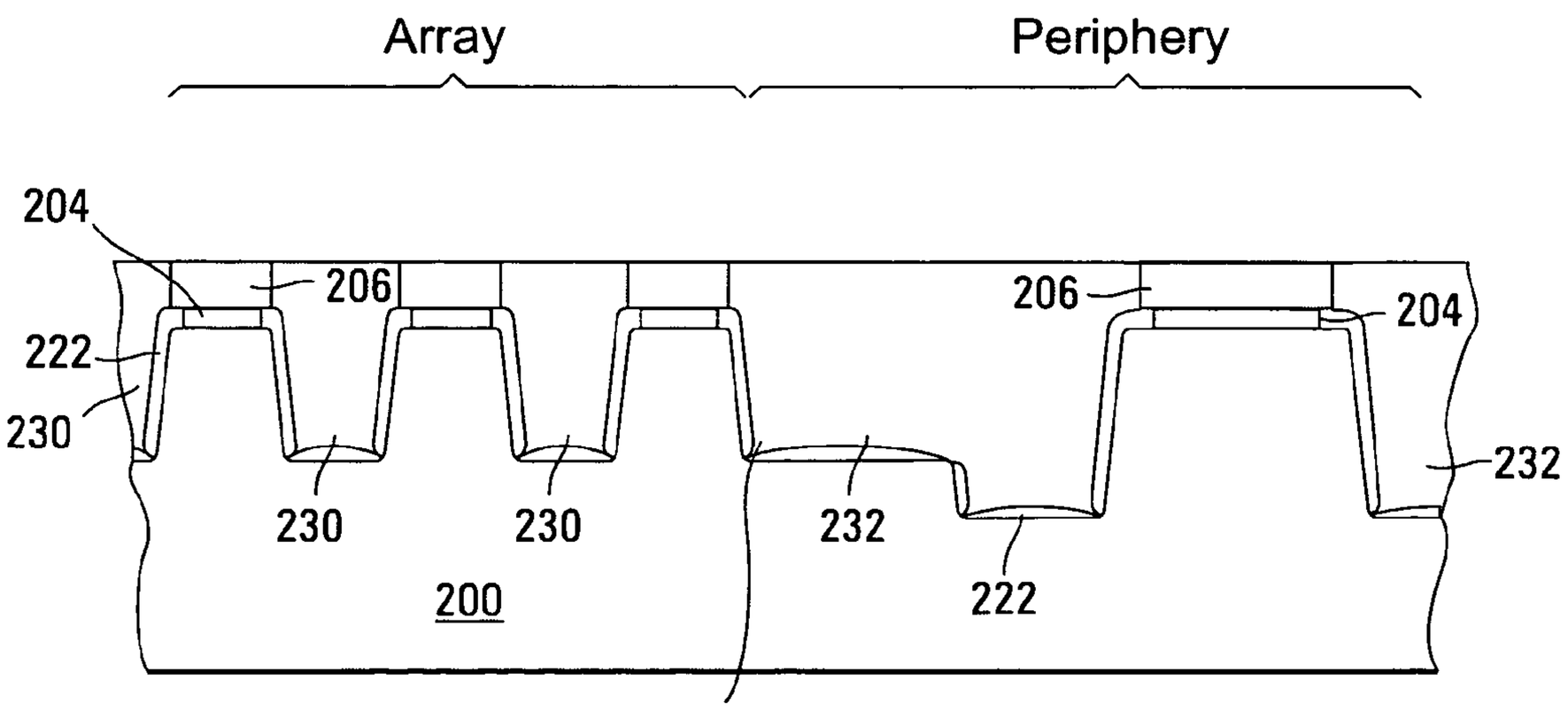
Array
Periphery
204
206
206
204
222
230
232
230
230
232
222
200

FIG. 2H

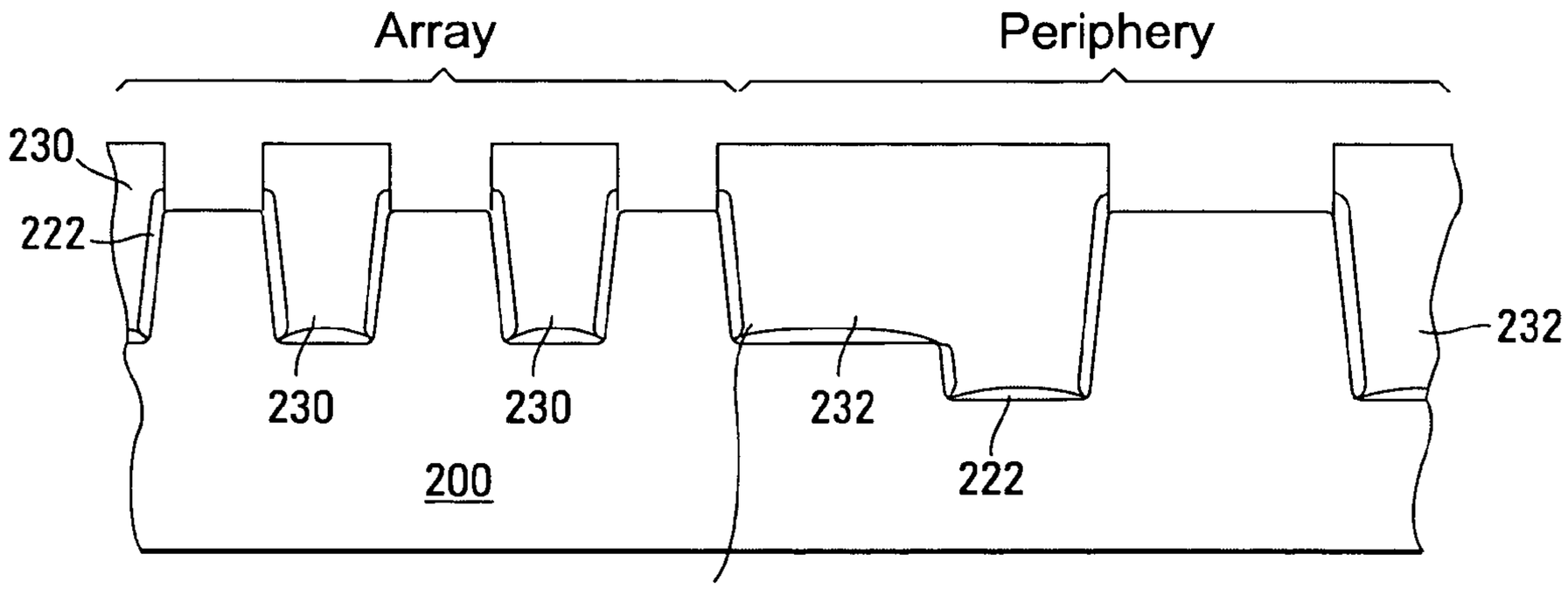
Array
Periphery
230
222
230
230
232
232
200
222

FIG. 2I

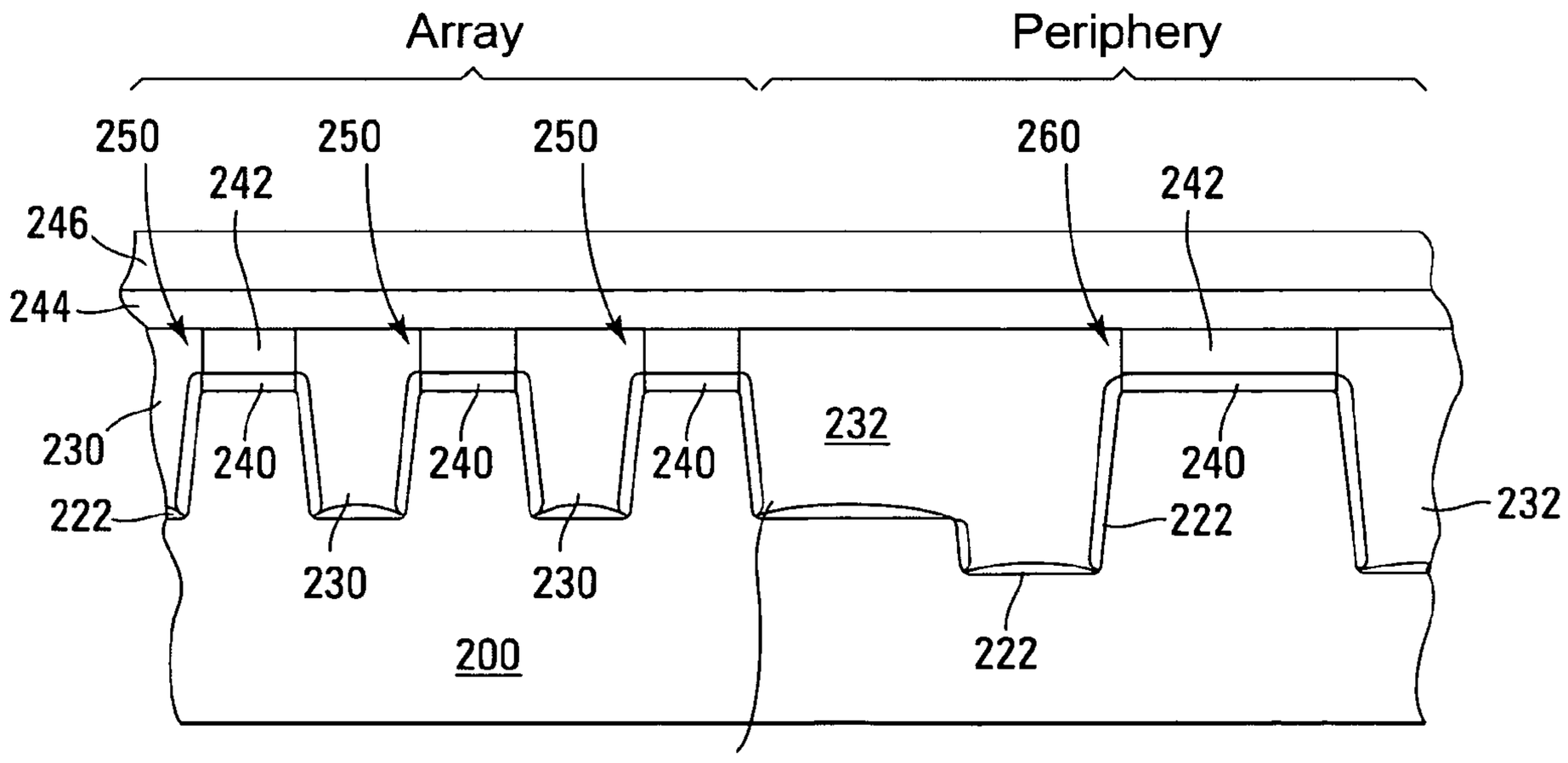
Array
Periphery
250
250
250
260
242
242
246
244
230
240
240
240
232
240
222
222
232
230
230
200
222

FIG. 2J

METHODS OF FORMING INTEGRATED CIRCUIT DEVICES

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuit devices and in particular the present invention relates to methods of forming integrated circuit devices.

BACKGROUND OF THE INVENTION

Memory devices are typically provided as internal storage areas in computers. The term memory identifies data storage that comes in the form of integrated circuit chips. In general, memory devices contain an array of memory cells for storing data, and row and column decoder circuits coupled to the array of memory cells for accessing the array of memory cells in response to an external address.

One type of memory is a non-volatile memory known as flash memory. A flash memory is a type of EEPROM (electrically-erasable programmable read-only memory) that can be erased and reprogrammed in blocks. Many modern personal computers (PCs) have their BIOS stored on a flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a flash BIOS. Flash memory is also popular in wireless electronic devices because it enables the manufacturer to support new communication protocols as they become standardized and to provide the ability to remotely upgrade the device for enhanced features.

A typical flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating-gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed on an individual basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge on the floating gate.

Memory devices are typically formed on semiconductor substrates using semiconductor fabrication methods. The array of memory cells is disposed on the substrate. Isolation regions formed in the substrate within the array, e.g., shallow trench isolation, provide voltage isolation on the memory array by acting to prevent extraneous current flow through the substrate between the memory cells. Various memory devices include passive elements, such as capacitors, and/or active elements, such as transistors, that are formed in the periphery, such as for accessing, programming, and erasing the memory cells, e.g., select circuitry having high voltage pumps, etc. Isolation regions formed in the substrate at the periphery provide isolation at the periphery by acting to prevent extraneous current from flowing through the substrate between the passive and/or active elements and the memory array.

Isolation regions are normally formed by forming a hard mask layer over the substrate, patterning the hard mask to define regions of the substrate for removal, removing the substrate material to form trenches in the substrate, and filling the trenches with isolation material to form the isolation regions. One problem with the fabrication of the trenches is the formation of sharp corners in the substrate near an upper surface of the semiconductor substrate adjacent the trenches. These sharp corners may carry stronger electric fields that may cause problems when later forming active regions on either side of the trench. For example,

when forming a transistor adjacent to the trench, a gate insulating oxide layer may be grown over the substrate and over the trench, because of the sharp corners, the gate oxide layer cannot be grown with a uniform thickness because it becomes too thin over the sharp corners. The thin gate oxide layer may break down if subjected to a high electric field.

Sharp top corners also cause a problem when filling the trench with an isolation material, e.g., using a high-density-plasma (HDP) chemical-vapor-deposition (CVD) process. HDP CVD processes subject the structure to plasma that also induces an electric field around the sharp corners that causes a non-uniform deposition process and that may create gaps or voids in the isolation material. Therefore, the sharp corners are often rounded.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternatives for rounding the sharp corners that form adjacent isolation trenches.

SUMMARY

The above-mentioned problems with wet etching and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

For one embodiment, the invention provides a method of forming an integrated circuit device that includes forming a hard mask layer overlying a semiconductor substrate, patterning the hard mask layer to expose portions of the substrate and edges of the hard mask layer, and removing exposed portions of the substrate. The method includes covering a first portion of the substrate with a photoresist layer while leaving a second portion exposed. Recessing the exposed edges of the hard mask to expose a third portion of the substrate, where recessing the exposed edges of the hard mask comprises using at least a dry-etch chemistry, is also included in the method, as is oxidizing the exposed second and third portions of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustration of an integrated circuit device, according to an embodiment of the invention.

FIGS. **2A–2J** are cross-sectional views of a portion of an integrated circuit device at various stages of fabrication in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The term wafer or substrate used in the following description includes any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well

as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

FIG. **1** is a block diagram illustration of an integrated circuit device, such as a processor, a memory device **102**, etc., according to an embodiment of the invention. The memory device **102** may be fabricated as semiconductor device on a semiconductor substrate. Examples of memory devices include NAND or NOR flash memory devices, dynamic random access memory devices (DRAMs), static random access memory devices (SRAMs), or the like.

For one embodiment, memory device **102** includes an array of flash memory cells **104** and a region **105** peripheral to memory array **104** that includes an address decoder **106**, row access circuitry **108**, column access circuitry **110**, control circuitry **112**, Input/Output (I/O) circuitry **114**, and an address buffer **116**. The row access circuitry **108** and column access circuitry **110** may include high-voltage circuitry, such as high-voltage pumps. The device of FIG. **1** includes isolation regions formed in accordance with an embodiment of the invention, e.g., between region **105** and memory **104** as well as within memory array **104**. It will be appreciated by those skilled in the art that various integrated circuit devices include passive elements, such as capacitors, and active elements, such as transistors, and that for some embodiments such active and passive elements are formed in the periphery.

Memory device **100** may be coupled an external microprocessor **120**, or memory controller, for memory accessing as part of an electronic system. The memory device **102** receives control signals from the processor **120** over a control link **122**. The memory cells are used to store data that are accessed via a data (DQ) link **124**. Address signals are received via an address link **126** that are decoded at address decoder **106** to access the memory array **104**. Address buffer circuit **116** latches the address signals. The memory cells are accessed in response to the control signals and the address signals. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of FIG. **1** has been simplified to help focus on the invention.

The memory array **104** includes memory cells arranged in row and column fashion. For one embodiment, each of the memory cells includes a floating-gate field-effect transistor capable of holding a charge. The cells may be grouped into blocks. Each of the cells within a block can be electrically programmed on an individual basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation.

For one embodiment, memory array **104** is a NOR flash memory array. A control gate of each memory cell of a row of the array is connected to a word line, and a drain region of each memory cell of a column of the array is connected to a bit line. The memory array for NOR flash memory devices is accessed by row access circuitry, such as the row access circuitry **108** of memory device **102**, activating a row of floating-gate memory cells by selecting the word line connected to their control gates. The row of selected memory cells then place their data values on the column bit lines by flowing a differing current, depending upon their programmed states, from a connected source line to the connected column bit lines.

For another embodiment, memory array **104** is a NAND flash memory array also arranged such that the control gate of each memory cell of a row of the array is connected to a word line. However, each memory cell is not directly connected to a column bit line by its drain region. Instead, the memory cells of the array are arranged together in strings (often termed NAND strings), e.g., of 32 each, with the memory cells connected together in series, source to drain, between a source line and a column bit line. The memory array for NAND flash memory devices is then accessed by row access circuitry, such as the row access circuitry **108** of memory device **102**, activating a row of memory cells by selecting the word line connected to a control gate of a memory cell. In addition, the word lines connected to the control gates of unselected memory cells of each string are driven to operate the unselected memory cells of each string as pass transistors, so that they pass current in a manner that is unrestricted by their stored data values. Current then flows from the source line to the column bit line through each series connected string, restricted only by the selected memory cells of each string. This places the current-encoded data values of the row of selected memory cells on the column bit lines.

FIGS. **2**A–**2**J are cross-sectional views of a portion of an integrated circuit device, such as memory device **102** of FIG. **1**, at various stages of fabrication in accordance with one embodiment of the invention. FIG. **2**A depicts a portion of the memory device after several processing steps have occurred. The structure of FIG. **2**A includes an array portion where an array of memory cells, such as of memory array **104** of memory device **102**, will be formed. The structure of FIG. **2**A further includes a periphery, such as the region **105** of memory device **102**, where various integrated circuit elements, including passive elements, such as capacitors, and active elements, such as transistors, e.g., of row access circuitry **108** and column access circuitry **110** of memory **102** of FIG. **1**, will be formed. For one embodiment, the active elements include field-effect transistors.

Formation of the type of structure depicted in FIG. **2**A is well known and will not be detailed herein. In general, the array and the periphery are formed concurrently on a semiconductor substrate **200**, such as a silicon-containing substrate, e.g., a monocrystalline silicon substrate, a P-type monocrystalline silicon substrate, etc. A hard mask **202** is formed overlying portions of substrate **200** in the array portion and the periphery. For one embodiment, hard mask **202** includes a sacrificial pad oxide layer **204**, such as a thermal oxide or deposited silicon dioxide (SiO_2), formed overlying substrate **200**. A nitride layer **206** of hard mask **202**, such as a layer of silicon nitride, or a layer of another suitable material having a high selectivity to silicon, is formed overlying pad oxide layer **204**. A cap layer **208**, e.g., of tetraethylorthosilicate (TEOS), is formed overlying nitride layer **206**. Trenches **210** are formed in the array portion and trenches **212** are formed in the periphery by patterning the hard mask layer **202** and removing portions of the substrate **200** exposed by the patterned hard mask **202**. Trenches **210** and **212** will be filled with a dielectric material, as described below, to form isolation regions, such as shallow trench isolation (STI) regions.

A photoresist mask layer **214** is subsequently formed overlying the array portion in FIG. **2**B, while leaving at least a portion the periphery exposed, including at least a portion of one of trenches **212** and the portion of hard mask layer

202 in the periphery. Photoresist mask layer 214 protects the array while additional material of substrate 200 is removed from trenches 212 in FIG. 2C to increase the extent or depth of of trenches 212 in substrate 200, e.g., using an anisotropic etch. The exposed portion of hard mask layer 202 in the periphery protects the underlying substrate during the removal of the additional substrate material from trenches 212 for the future formation of a circuit element there. Note that the removal of the additional substrate material removes material from cap layer 208 in the periphery causing cap layer 208 to be thinner in the periphery than in the array, as shown in FIG. 2C.

In FIG. 2D, a dry isotropic etch is performed to etch back (or recess) nitride layer 206 relative to pad oxide layer 204 and cap layer 208 of the exposed portion of hard mask layer 202 in the periphery in a direction generally parallel to an upper surface of substrate 200. This exposes portions of pad oxide layer 204, as shown in FIG. 2D. It should be noted that wet etch methods that can remove nitrides, such as phosphoric acid dips or the like, are not suitable for recessing nitride layer 206 because they act to lift photoresist mask layer 214 off the array portion.

For one embodiment, the isotropic dry etch is performed using a plasma containing an oxygen source, a hydrogen source, and a fluorine source. More specifically, for another embodiment, the isotropic dry etch is performed using a forming gas of nitrogen (N_2) with 3.8% hydrogen (H_2) by volume at a flow rate of about 700 to about 1600 standard cubic centimeters per minute (sccm), tetrafluoromethane (CF_4) at a flow rate from about 30 to about 200 sccm, and an oxygen (O_2) at a flow rate from about 40 to about 1000 sccm, at a pressure of about 0.5 to about 2.5 torr., a temperature of about 20 to about 120° C., and a microwave power of about 500 to about 3000 Watts. Nitric Oxide (N_2O) and H_2 or water (H_2O) and N_2 may be substituted for N_2, H_2, and O_2, for another embodiment, and trifluoromethane (CHF_3) or nitrogen trifluoride (NF_3) may be substituted for CF_4 for yet another embodiment.

Photoresist mask layer 214 is removed, e.g., using a stripping operation, and the exposed portions of pad oxide layer 204 are subsequently removed in FIG. 2E to expose portions of substrate 200 adjacent corners 220 that are respectively adjacent trenches 212 in the periphery and adjacent corners 221 that are respectively adjacent trenches 210 in the periphery. For one embodiment, a wet etch, such as an etch using diluted hydrofluoric acid (HF) may be used to remove the exposed portions of pad oxide layer 204. An oxide liner 222 is formed on the exposed surfaces of substrate 200 by rapid thermal oxidation, for one embodiment, or with in-situ generated steam, for another embodiment, in FIG. 2F. The oxidation acts to round corners 220 and 221, as shown in FIG. 2F. Note, however, that the rounding of corners 221 is less pronounced than the rounding of corners 220, owing to the recessing of both pad oxide layer 204 and nitride layer 206 in the periphery. Rounding of corners 220 acts to reduce oxide stresses that may form in the vicinity of corners 220.

A layer of dielectric material 224 is deposited in trenches 210 and 212 and overlying protective cap layer 202 in the array portion and periphery, such as by blanket deposition, in FIG. 2G. For other embodiments, a spin-on process may be used to deposit dielectric material in trenches 210 and 212. Suitable dielectric materials may include oxides, e.g., thermal oxides and/or high-density-plasma (HDP) oxides, spin-on dielectric materials, e.g., hydrogen silsesquioxane (HSQ), hexamethyldisiloxane, octamethyltrisiloxane, etc. For some embodiments, a nitride liner is formed on oxide liner 222, before filling trenches 210 and 212 with the dielectric material.

Subsequently, for one embodiment, a portion of the dielectric material 224 and cap layer 208 of hard mask 202 are removed, e.g., by chemical mechanical planerization (CMP), using the nitride layer 206 as a stopping layer, to expose an upper surface of nitride layer 206 of hard mask 202 and to respectively form isolation regions 230 and 232 in trenches 210 of the array portion and trenches 212 of the periphery in FIG. 2H.

In FIG. 2I, nitride layer 206 and pad oxide layer 204 of hard mask 202 are removed, exposing portions of substrate 200 to define active regions between isolation regions 230 in the array portion over which memory cells will be formed, and active regions between isolation regions 232 in the periphery over which a circuit element, such as a field effect transistor, will be formed. Note that for the embodiment where the cap layer 208 is left after removal of the portion of the dielectric material 224, this step involves removing the entire hard mask 202.

Upon exposing future active regions of substrate 200, formation of circuit elements can proceed in a manner suitable for the desired integrated circuit device. FIG. 2J provides one example for forming a memory device. Note that for various embodiments, the substrate will contain active areas having rounded corners prior to forming circuit elements thereon, with the rounding being more pronounced in the periphery.

In FIG. 2J, a first dielectric layer 240, e.g., an oxide layer, is formed on the exposed portions of substrate in the array portion and the periphery. For one embodiment, forming the first dielectric layer on the exposed portions of the substrate includes blanket depositing or thermally growing the dielectric layer. A first conductive layer 242 is subsequently formed on first dielectric layer 240. For one embodiment, first conductive layer 242 is a silicon-containing layer, preferably a polysilicon (polycrystalline silicon) layer, but could also include other forms of doped or undoped silicon materials, such as monocrystalline silicon, nanocrystalline silicon, and amorphous silicon.

A second dielectric layer 244 is formed overlying first conductive layer 242 and the isolation regions 230 and 232. Second dielectric layer 244 may be one or more layers of dielectric material. For example, the second dielectric layer 244 could be of a multi-layer dielectric material commonly referred to as ONO (oxide-nitride-oxide). Other dielectric materials may be substituted for the ONO, such as tantalum oxide, barium strontium titanate, silicon nitride, and other materials providing dielectric properties.

A second conductive layer 246 is formed overlying second dielectric layer 244. Second conductive layer 246 is generally one or more layers of conductive material. For one embodiment, the second conductive layer 246 contains a conductively-doped polysilicon. For a further embodiment, the second conductive layer 246 includes a metal-containing layer overlying a polysilicon layer, e.g., a refractory metal silicide layer formed on a conductively-doped polysilicon layer. The metals of chromium (Cr), cobalt (Co), hafnium (Hf), molybdenum (Mo), niobium (Nb), tantalum (Ta), titanium (Ti), tungsten (W), vanadium (V) and zirconium (Zr) are generally recognized as refractory metals. For another embodiment, second conductive layer 246 contains multiple metal-containing layers, e.g., a titanium nitride (TiN) barrier layer overlying the second dielectric layer 244, a titanium (Ti) adhesion layer overlying the barrier layer, and a tungsten (W) layer overlying the adhesion layer. An

insulative cap layer (not shown) is often formed overlying the second conductive layer **246** to protect and isolate the second conductive layer **246** from further processing.

The first conductive layer **242**, the second dielectric layer **244**, and the second conductive layer **246** form gate stacks. In the array portion of the memory device, the gate stacks form a part of floating gate memory cells **250**, where the first dielectric layer **240** is a tunnel dielectric layer, the first conductive layer **242** is a floating gate, the second dielectric layer **244** is an intergate dielectric layer, and the second conductive layer **246** is a control gate of the memory cells **250**. The second conductive layer **246** (or control gate) of the array portion is subsequently patterned to define the word lines of the memory device (not shown in FIG. **2**J). Note that an isolation region **230** of the memory array portion isolates the tunnel dielectric layers and the floating gates of adjacent memory cells **250**.

In the periphery, for one embodiment, the gate stacks form a part of a circuit element **260**, e.g., field-effect transistor. For example, the field-effect transistor can be part of row access circuitry **108** and/or column access circuitry **110** of the memory device **102** of FIG. **1** for accessing rows and columns of the memory array **104**. The first dielectric layer **240** is a gate dielectric layer, and the first conductive layer **242** and the second conductive layer **246** are portions of a control gate of the element **260**, for one embodiment. For some embodiments, the first conductive layer **242** and the second conductive layer **246** may be strapped (or shorted) together so that the shorted together first conductive layer **242** and second conductive layer **246** form the control gate of the element **260**. For another embodiment, the first conductive layer **242** and the second conductive layer **246** are not shorted together, and first conductive layer **242** forms the control gate of the element **260**.

It is noted that FIGS. **2**A–**2**J depict a portion of a row of memory cells running parallel to a face plane of the drawings. Columns of memory cells, separated by the isolation regions **230**, run perpendicular to the drawings, with source and drain regions formed at opposing ends of the tunnel dielectric layer **240**, one above the face plane of the figures and one below the face plane of the figures. It is noted that FIGS. **2**A–**2**J can depict either a NOR-type memory device or a NAND-type memory device, with the differences occurring in the column direction in manners that are well understood in the art of memory fabrication.

CONCLUSION

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A method of forming an integrated circuit device, comprising:

forming and patterning a hard mask layer overlying a semiconductor substrate, the patterned hard mask layer exposing two or more areas of the substrate for future isolation regions of the integrated circuit device;

removing portions of the substrate in the areas for future isolation regions, thereby forming two or more trenches;

forming a second mask layer overlying a first portion of the hard mask layer and at least one first trench, leaving a second portion of the hard mask layer and at least a portion of at least one second trench uncovered;

removing additional substrate material from the uncovered portion of the at least one second trench so that the uncovered portion of the at least one second trench is deeper than the at least one first trench; and

recessing a portion of the second portion of the hard mask layer in a direction generally parallel to an upper surface of the substrate using an isotropic dry etch while the second mask layer overlies the first portion of the hard mask layer and the at least one first trench.

2. The method of claim **1**, wherein recessing the portion of the second portion of the hard mask layer, comprises recessing a nitride layer of the hard mask layer.

3. The method of claim **2** further comprises removing the second mask layer and recessing an oxide layer of the hard mask layer interposed between the semiconductor substrate and nitride layer in a direction generally parallel to the upper surface of the substrate, wherein the oxide layer is recessed in both the first and second portions of the hard mask layer.

4. The method of claim **3**, wherein recessing the oxide layer comprises a wet-etch process.

5. The method of claim **3** further comprises oxidizing a portion of the semiconductor substrate exposed by recessing the nitride and oxide layers of the second portion of the hard mask layer, oxidizing a portion of the semiconductor substrate exposed by recessing the oxide layer of the first portion of the hard mask layer, and oxidizing exposed semiconductor substrate material within the at least one first trench and the at least one second trench.

6. The method of claim **1**, wherein forming the hard mask layer comprises:

forming an oxide layer overlying the semiconductor substrate;

forming a nitride layer overlying the oxide layer; and

forming a cap layer overlying the nitride layer.

7. The method of claim **1**, wherein the second mask layer is a layer of photoresist.

8. A method of forming an integrated circuit device, comprising:

forming a hard mask layer overlying a semiconductor substrate;

patterning the hard mask layer to expose portions of the substrate and edges of the hard mask layer;

removing exposed portions of the substrate;

covering a first portion of the substrate with a photoresist layer while leaving a second portion exposed;

recessing the exposed edges of the hard mask to expose a third portion of the substrate, wherein recessing the exposed edges of the hard mask comprises using at least a dry-etch chemistry; and

oxidizing the exposed second and third portions of the substrate.

9. The method of claim **8** further comprises removing the photoresist layer before oxidizing the exposed second and third portions of the substrate.

10. The method of claim **9** further comprises oxidizing exposed portions of the first portion of the substrate after removing the photoresist layer.

11. The method of claim **8**, wherein forming the hard mask layer comprises:

forming an oxide layer overlying the semiconductor substrate;

forming a nitride layer overlying the oxide layer; and

forming a cap layer overlying the nitride layer.

12. The method of claim **11**, wherein the dry-etch chemistry recesses exposed edges of the nitride layer.

13. The method of claim **8**, wherein recessing the exposed edges of the hard mask further comprises using a wet-etch chemistry.

14. The method of claim **8**, wherein the dry-etch chemistry isotropically etches the exposed edges of the hard mask.

15. A method of forming an integrated circuit device, comprising:

forming a sacrificial oxide layer overlying a substrate;

forming a nitride layer overlying the sacrificial oxide layer;

forming a cap layer overlying the nitride layer;

patterning the sacrificial oxide layer, the nitride layer and the cap layer to expose first portions of the substrate and edges of the sacrificial oxide, the nitride, and the cap layers;

removing exposed portions of the substrate;

exposing the substrate to a dry etch chemistry to recess the exposed edges of the nitride layer and to expose portions of the sacrificial oxide layer, wherein at least a portion of the substrate is covered by a photoresist layer;

removing the exposed portions of the sacrificial oxide layer; and

oxidizing exposed portions of the substrate.

16. The method of claim **15**, wherein the dry etch chemistry isotropically etches the exposed edges of the nitride layer.

17. The method of claim **15**, wherein the dry-etch chemistry comprises nitrogen and hydrogen, oxygen, and tetrafluoromethane.

18. The method of claim **17**, wherein the dry-etch is performed at temperature of about 20 to about 120° C. and a pressure of about 0.5 to about 2.5 torr.

19. The method of claim **18**, wherein the nitrogen and hydrogen flow at a rate from about 30 to about 200 standard cubic centimeters per minute, the oxygen flows at a rate from about 40 to about 1000 standard cubic centimeters per minute, and the tetrafluoromethane flows at a rate from about 30 to about 200 standard cubic centimeters per minute.

20. The method of claim **19**, wherein a microwave power of about 500 to about 3000 Watts is supplied to the dry-etch chemistry.

21. The method of claim **15**, wherein removing the exposed portions of the sacrificial oxide layer comprises using a wet-etch chemistry.

22. The method of claim **21**, wherein the wet-etch chemistry comprises diluted hydrofluoric acid.

23. The method of claim **15**, wherein the cap layer is of TEOS.

24. A method of forming a memory device, comprising:

forming a hard mask layer by

forming a sacrificial oxide layer overlying a substrate;

forming a nitride layer overlying the sacrificial oxide layer; and

forming a cap layer overlying the nitride layer;

patterning the hard mask layer to expose two or more areas of the substrate for future isolation regions of the memory device and edges of the hard mask layer;

removing portions of the substrate in the areas for future isolation regions, thereby forming two or more trenches;

forming a second mask layer overlying a first portion of the hard mask layer and at least one first trench, leaving a second portion of the hard mask layer and at least a portion of at least one second trench uncovered;

removing additional substrate material from the uncovered portion of the at least one second trench so that the uncovered portion of the at least one second trench is deeper than the at least one first trench;

exposing the uncovered portion of the at least one second trench and the second portion of the hard mask layer to a dry-etch chemistry to recess exposed edges of the nitride layer, thereby exposing portions of the sacrificial oxide layer;

removing the second mask layer;

removing the exposed portions of the sacrificial oxide layer; and

oxidizing exposed portions of the substrate;

filling the two or more trenches with isolation material to form two or more isolation regions;

removing the hard mask to expose regions of the substrate between the two or more isolation regions;

forming a first dielectric layer on each of the exposed regions of the substrate;

forming a first conductive layer on the first dielectric layer;

forming a second dielectric layer overlying the first conductive layer and the two or more isolation regions; and

forming a second conductive layer overlying the second dielectric layer.

25. The method of claim **24**, wherein the dry-etch chemistry isotropically etches the exposed edges of the nitride layer.

26. The method of claim **24**, wherein removing the exposed portions of the sacrificial oxide layer comprises a wet-chemistry etch.

27. The method of claim **24** wherein the isolation material is a dielectric material selected from the group consisting of oxides and spin-on-dielectric materials.

28. The method of claim **24**, wherein the second mask layer is a photoresist mask layer.

29. The method of claim **24**, wherein forming the first dielectric layer comprises blanket depositing or thermally growing the first dielectric layer.

30. The method of claim **24**, wherein the first dielectric layer is an oxide layer.

31. The method of claim **24**, wherein the second dielectric layer is selected from the group consisting of one or more layers of dielectric material, an oxide-nitride-oxide dielectric material, tantalum oxide, barium strontium titanate, and silicon nitride.

32. The method of claim **24**, wherein the second conductive layer is selected from the group consisting of a layer containing a conductively-doped polysilicon, a metal-containing layer overlying a polysilicon layer, a refractory metal silicide layer formed on a conductively-doped polysilicon layer, multiple metal-containing layers, and a layer including a barrier layer overlying the second dielectric layer, an adhesion layer overlying the barrier layer, and a metal layer overlying the adhesion layer.

33. The method of claim **24**, wherein the first conductive layer is selected from the group consisting of a polysilicon layer, doped or undoped silicon materials, monocrystalline silicon, nanocrystalline silicon, and amorphous silicon.

34. The method of claim 24, wherein the dry-etch chemistry comprises tetrafluoromethane, trifluoromethane, or nitrogen trifluoride.

35. The method of claim 34, wherein the dry-etch chemistry further comprises nitrogen hydrogen, and oxygen or nitric oxide and hydrogen or water and nitrogen.

36. The method of claim 34, wherein the dry-etch is performed at temperature of about 20 to about 120° C. and a pressure of about 0.5 to about 2.5 torr.

37. The method of claim 35, wherein the nitrogen and hydrogen flow at a rate from about 30 to about 200 standard cubic centimeters per minute, the oxygen flows at a rate from about 40 to about 1000 standard cubic centimeters per minute, and the tetrafluoromethane flows at a rate from about 30 to about 200 standard cubic centimeters per minute.

38. The method of claim 24, wherein a microwave power of about 500 to about 3000 Watts is supplied to the dry-etch chemistry.

39. A method of forming a memory device, comprising:

forming a hard mask layer by

forming a sacrificial oxide layer overlying a substrate;

forming a nitride layer overlying the sacrificial oxide layer; and

forming a TEOS layer overlying the nitride layer;

patterning the hard mask layer to expose two or more areas of the substrate for future isolation regions of the memory device and edges of the hard mask layer;

removing portions of the substrate in the areas for future isolation regions, thereby forming two or more trenches;

forming a photoresist mask layer overlying a first portion of the hard mask layer and at least one first trench in a memory array portion of the memory device, leaving a second portion of the hard mask layer and at least a portion of at least one second trench uncovered in a periphery of the memory device;

removing additional substrate material from the uncovered portion of the at least one second trench so that the uncovered portion of the at least one second trench is deeper than the at least one first trench;

exposing the uncovered portion of the at least one second trench and the second portion of the hard mask layer to a dry-etch chemistry to recess exposed edges of the nitride layer, thereby exposing portions of the sacrificial oxide layer;

removing the photoresist mask layer;

removing the exposed portions of the sacrificial oxide layer; and

oxidizing exposed portions of the substrate;

filling the at least one first trench and the at least one second trench with a dielectric material to respectively form at least one first isolation region in the memory array portion and at least one second isolation region in the periphery;

removing the hard mask to expose at least one first region of the substrate in the array portion adjacent at least one first isolation region and to expose at least one second region of the substrate in the periphery adjacent the at least one second isolation region;

forming a first dielectric layer on each of the exposed regions of the substrate;

forming a first conductive layer on the first dielectric layer;

forming a second dielectric layer overlying the first conductive layer and the two or more isolation regions; and

forming a second conductive layer overlying the second dielectric layer.

40. The method of claim 39, wherein the dry-etch chemistry isotropically etches the exposed edges of the nitride layer.

41. The method of claim 39, wherein removing the exposed portions of the sacrificial oxide layer comprises a wet-chemistry etch.

42. The method of claim 39, wherein the dry-etch chemistry comprises tetrafluoromethane, trifluoromethane, or nitrogen trifluoride.

43. The method of claim 42, wherein the dry-etch chemistry further comprises nitrogen hydrogen, and oxygen or nitric oxide and hydrogen or water and nitrogen.

44. The method of claim 42, wherein the dry-etch is performed at temperature of about 20 to about 120° C. and a pressure of about 0.5 to about 2.5 torr.

45. The method of claim 43, wherein the nitrogen and hydrogen flow at a rate from about 30 to about 200 standard cubic centimeters per minute, the oxygen flows at a rate from about 40 to about 1000 standard cubic centimeters per minute, and the tetrafluoromethane flows at a rate from about 30 to about 200 standard cubic centimeters per minute.

46. The method of claim 39, wherein a microwave power of about 500 to about 3000 Watts is supplied to the dry-etch chemistry.

47. The method of claim 39, wherein the first dielectric layer, the first conductive layer, the second dielectric layer, and the second conductive layer in the memory array portion respectively form a tunnel dielectric layer, a floating gate, an intergate dielectric layer, and a control gate of one or more floating-gate memory cells adjacent the at least one first isolation region.

48. The method of claim 39, wherein the first dielectric layer, the first conductive layer, the second dielectric layer, and the second conductive layer in the periphery form at least one circuit element of the memory device adjacent the at least one second isolation region.

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