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**Crispin**

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(54) **APPARATUS AND METHOD FOR REDUCING SEQUENTIAL BIT CORRELATION IN A RANDOM NUMBER GENERATOR**

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(65) **Prior Publication Data**

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Primary Examiner—D. H. Malzahn

(52) **U.S. Cl.** ..... **708/250**

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(58) **Field of Classification Search** ..... 708/250–256  
See application file for complete search history.

(57) **ABSTRACT**

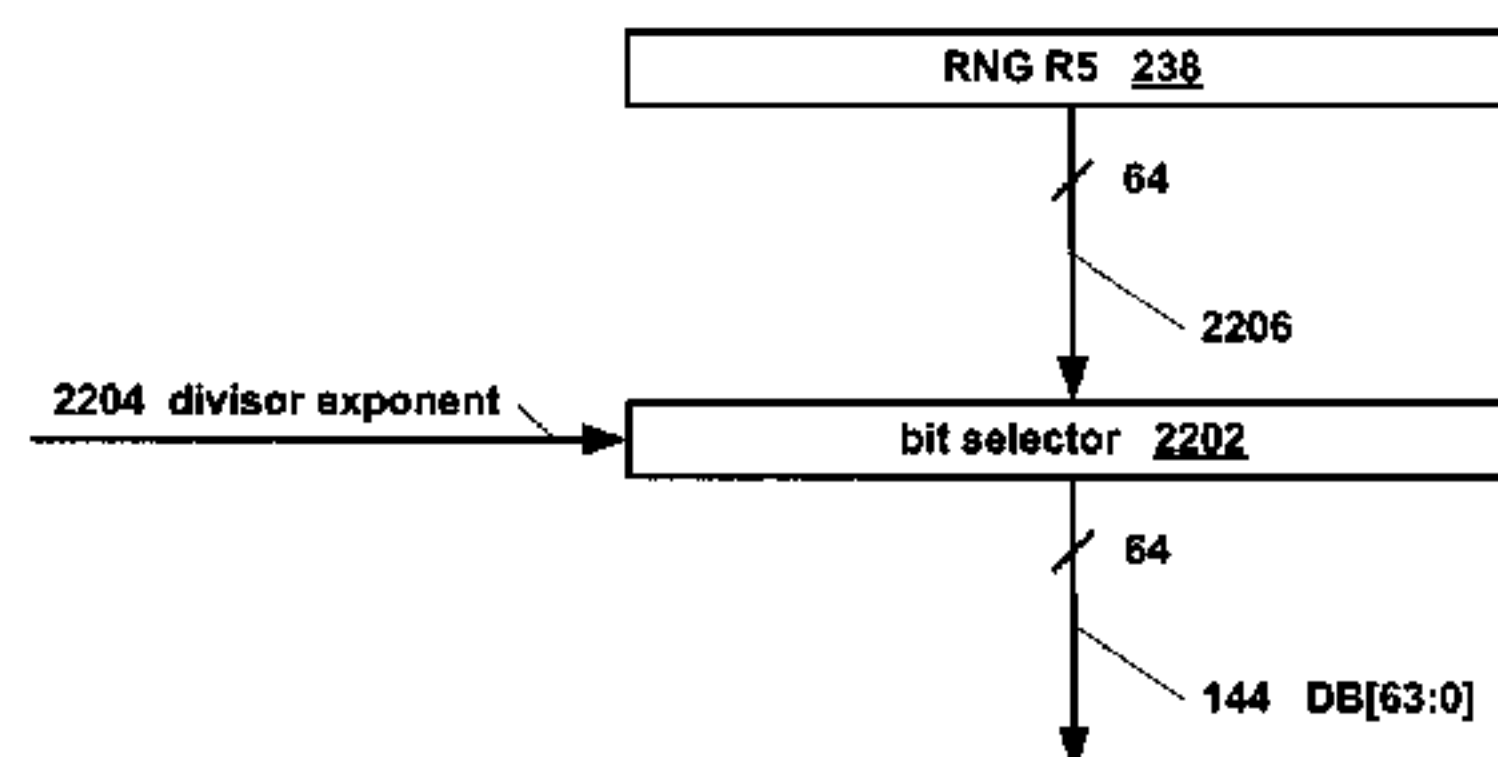
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An apparatus and method for reducing sequential bit correlation in a random number generator. The method includes generating a stream of random bits and selecting every Nth bit from the stream for accumulation and delivery to the requesting software application rather than delivering all the bits in the stream, where N is a programmable value. In one embodiment, the apparatus for carrying out the method includes a microprocessor that includes elements such as an arithmetic and logic unit, store unit, branching circuitry, and registers that execute instructions specified in microcode stored in a microcode memory. In another embodiment, the apparatus includes a plurality of multiplexers that select every Nth bit. In one embodiment, N is specified as an input parameter to a microprocessor instruction that stores the random bits selected.

**19 Claims, 23 Drawing Sheets**



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FIG. 1

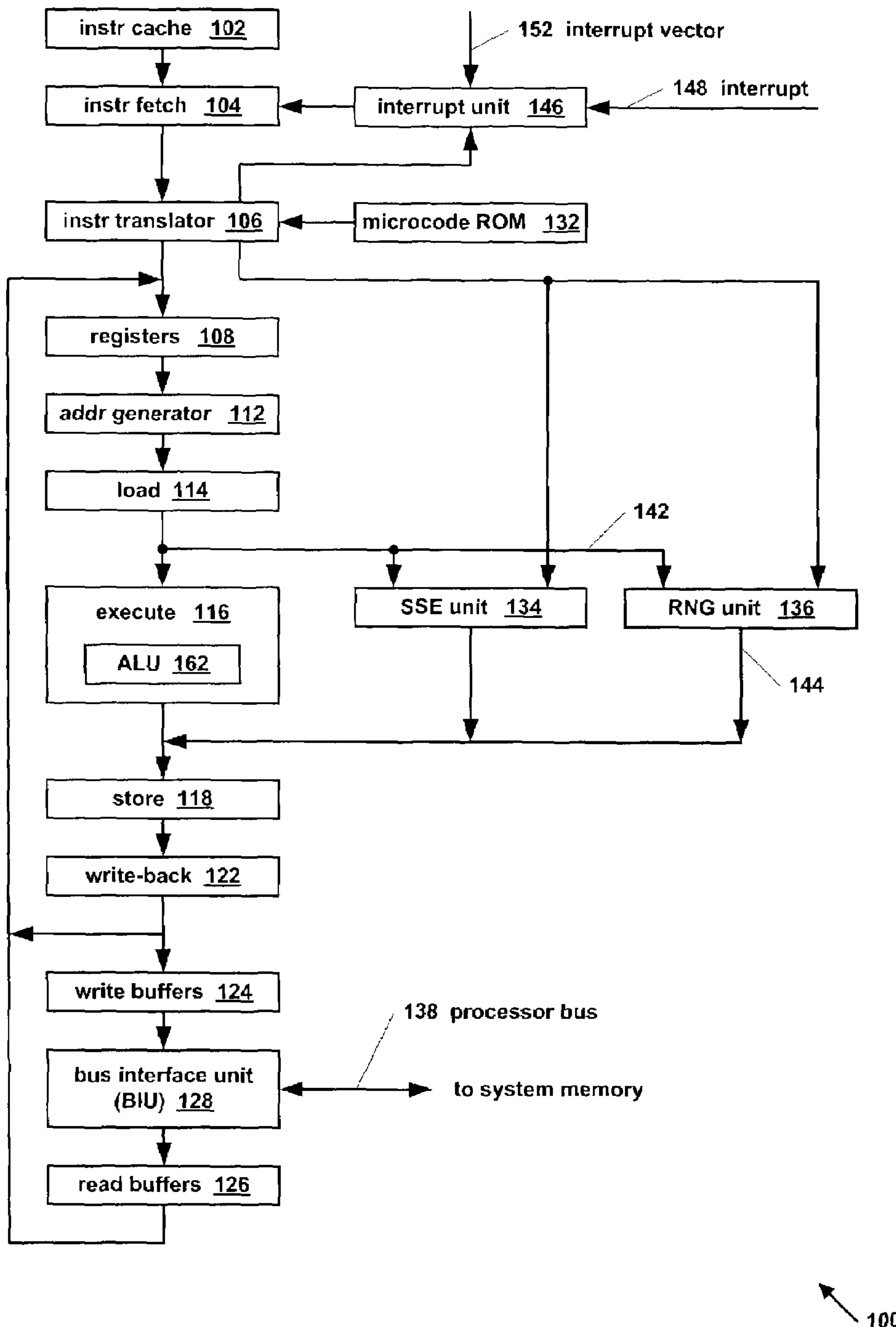


FIG. 2

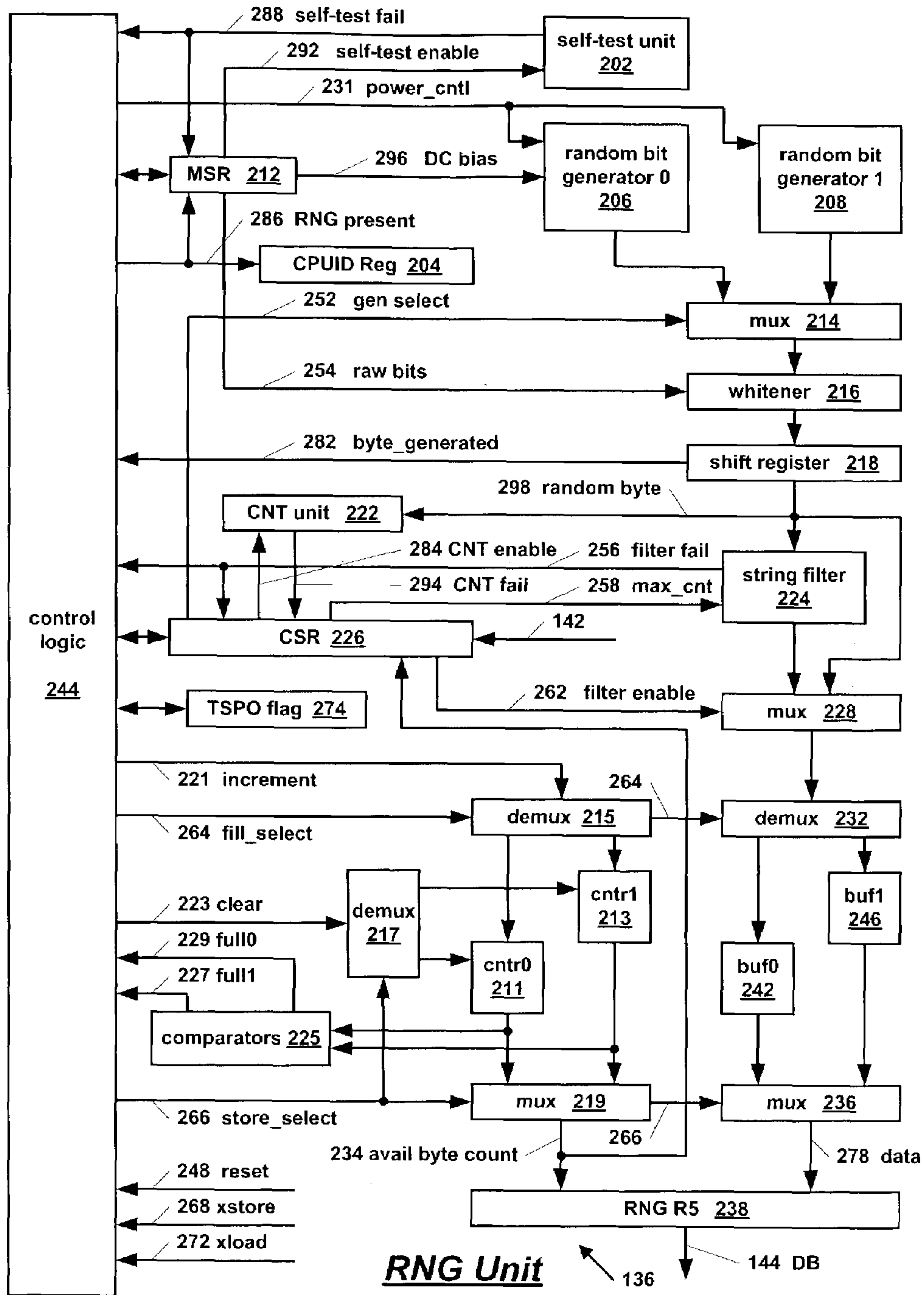


FIG. 3

	RNG present	
	<u>302</u>	

204 CPUID Register

	raw bits	DC bias	self-test failed	self-test enabled	RNG present	RNG enable
	<u>324</u>	<u>322</u>	<u>318</u>	<u>316</u>	<u>314</u>	<u>312</u>

212 MSR

	string filter max_cnt	CNT failed	CNT enable	string filter fail	gen select	string filter enable	avail byte count
	<u>346</u>	<u>344</u>	<u>342</u>	<u>338</u>	<u>336</u>	<u>334</u>	<u>332</u>

226 CSR

XMM0 <u>372</u>
XMM1
XMM2
XMM3 <u>376</u>
XMM4
XMM5 <u>374</u>
XMM6
XMM7

352 SSE Registers

RNG CSR 226

RNG R5 238

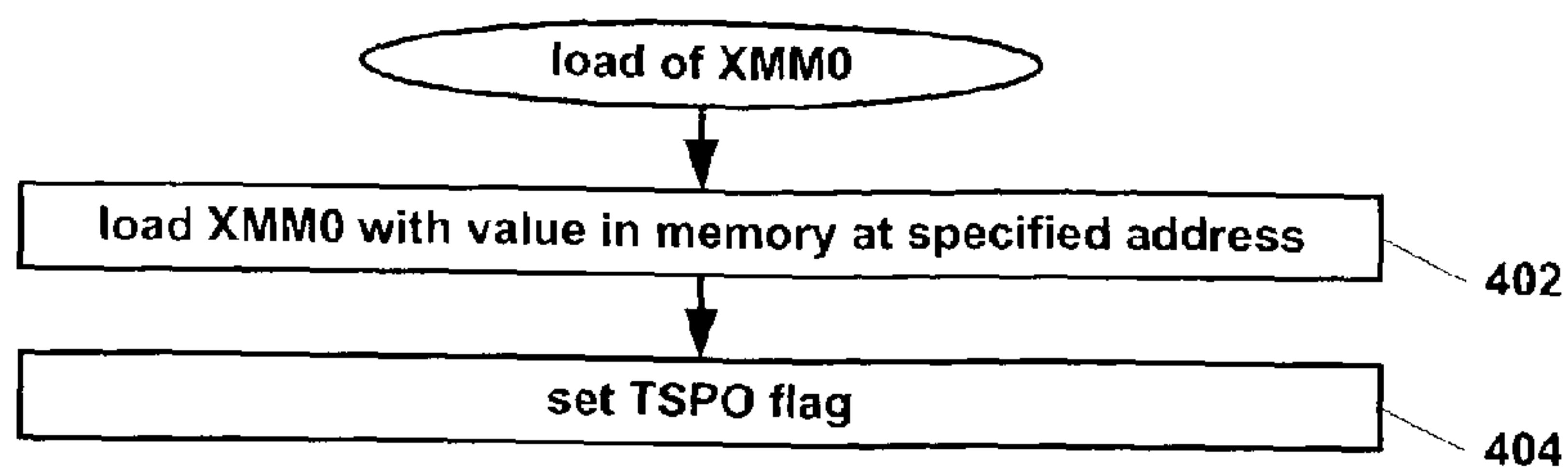
up to 15 random data bytes <u>364</u>	avail byte count <u>362</u>
--	--------------------------------

valid random data bytes are right-adjusted next to the available byte count

**RNG-Related Registers**

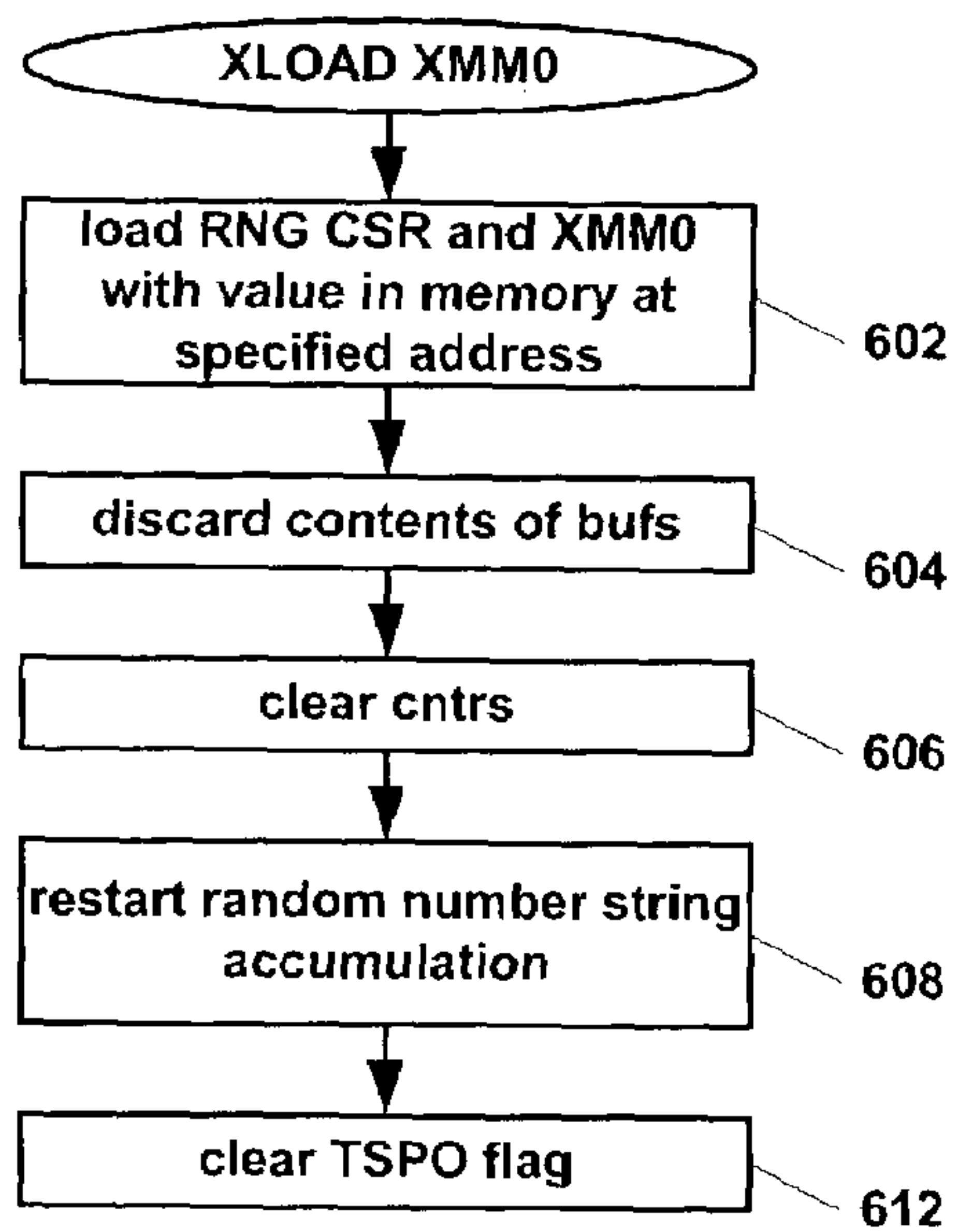


FIG. 4



RNG Unit Operation (load of XMM0)

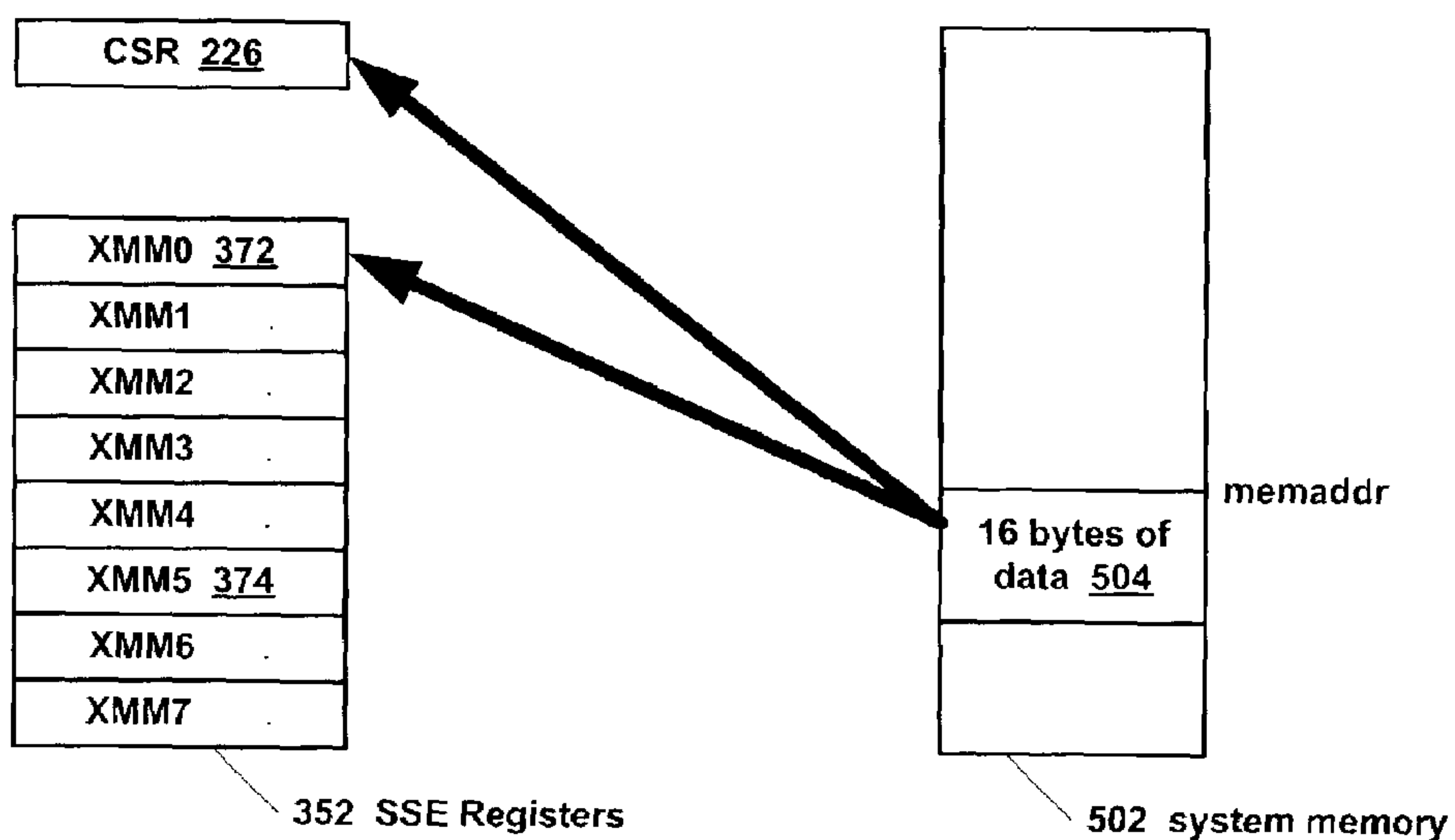
FIG. 6



RNG Unit Operation (XLOAD XMM0 instruction)

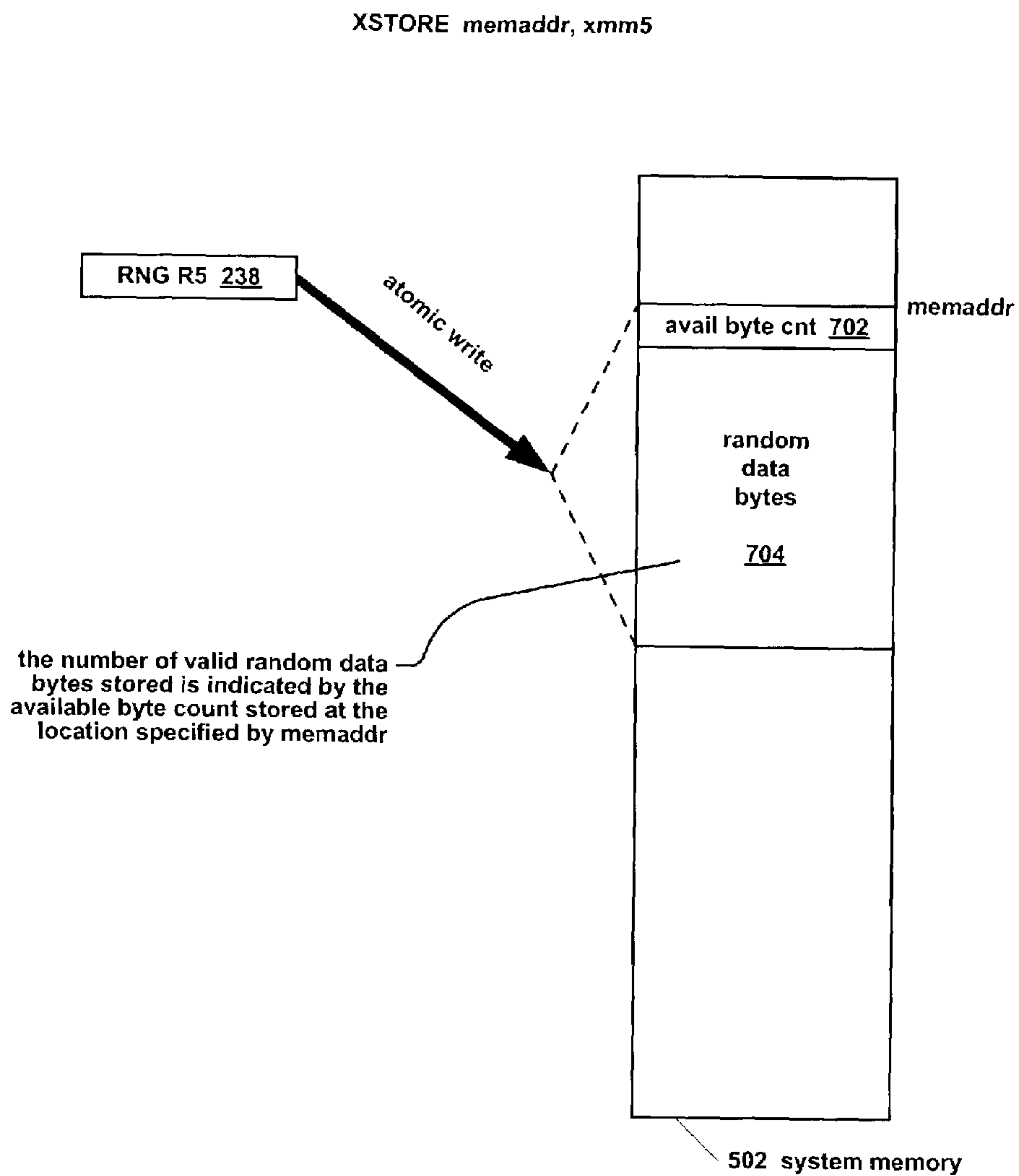
FIG. 5

XLOAD xmm0, memaddr



XLOAD instruction

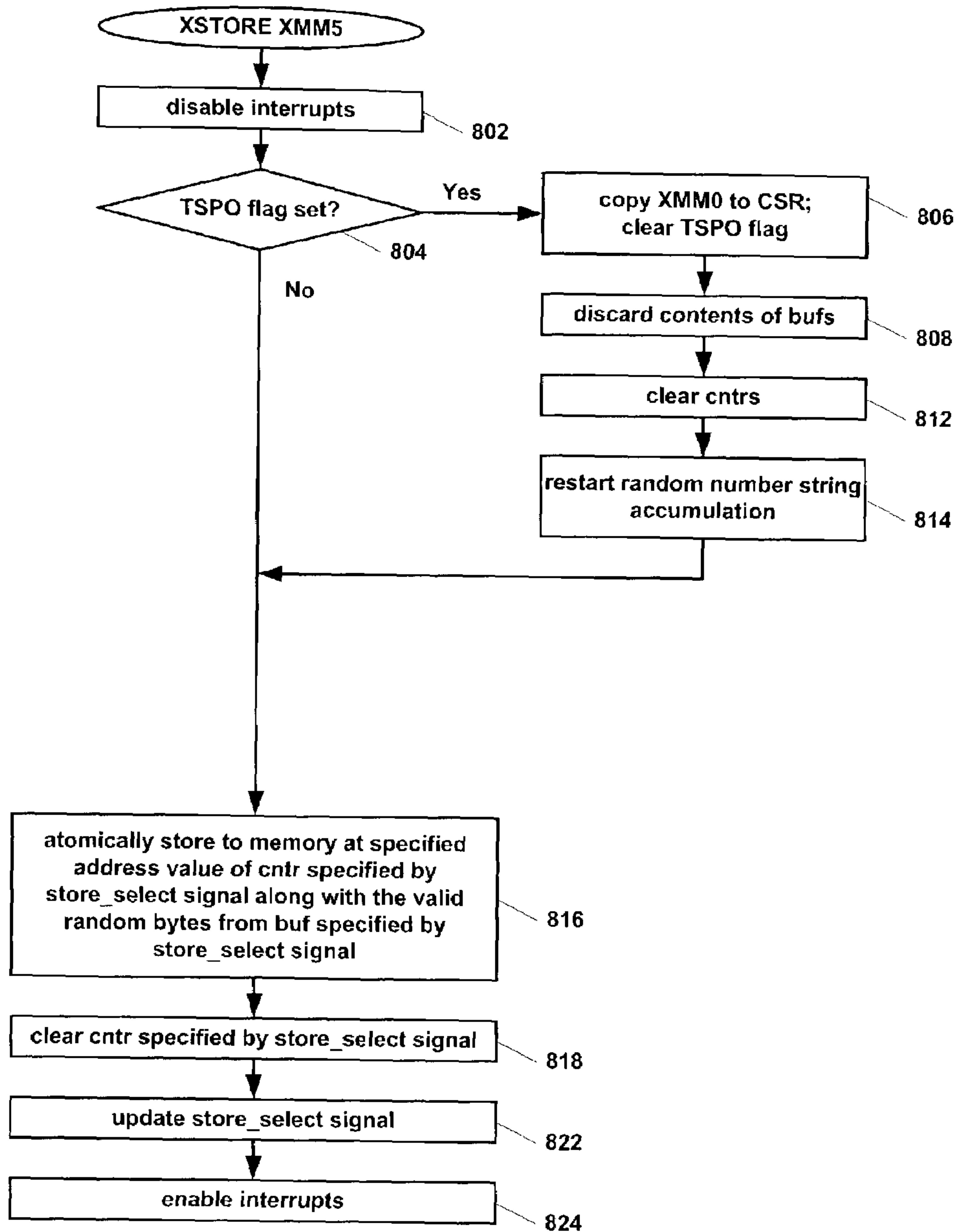
FIG. 7



XSTORE instruction

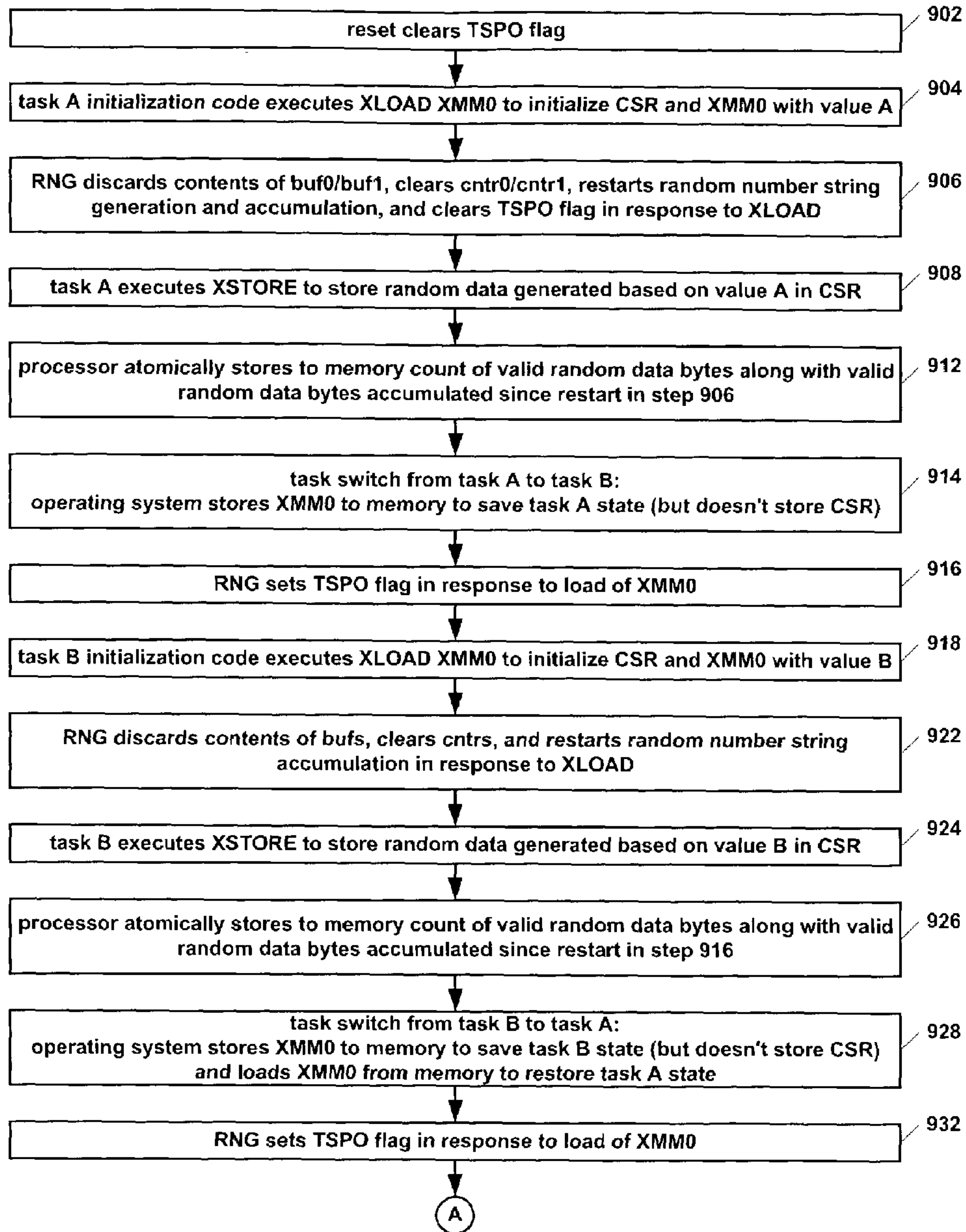


FIG. 8



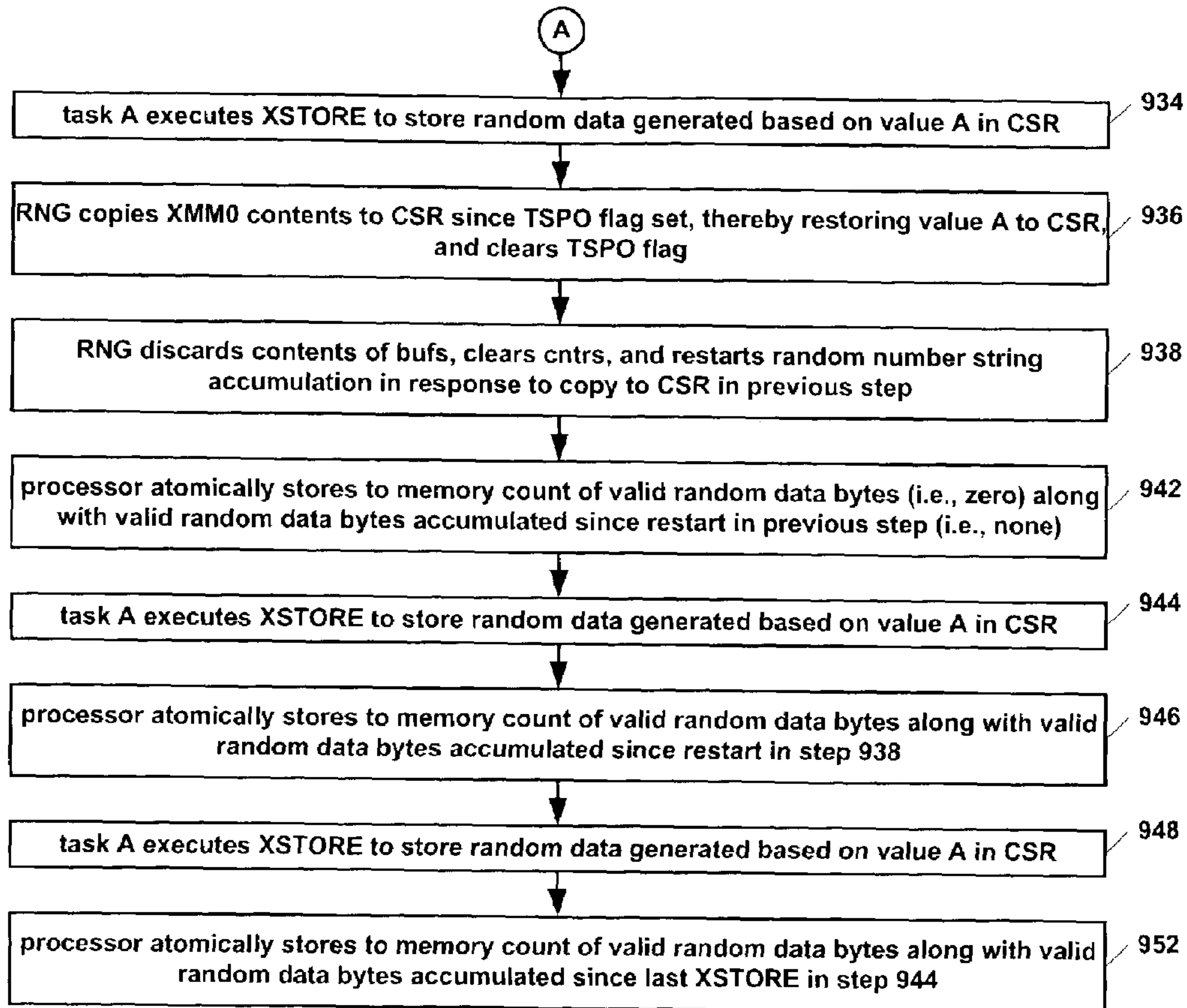
RNG Unit Operation (XSTORE XMM5 instruction)

FIG. 9A



**Multitasking Operation**

FIG. 9B



Multitasking Operation

FIG. 10

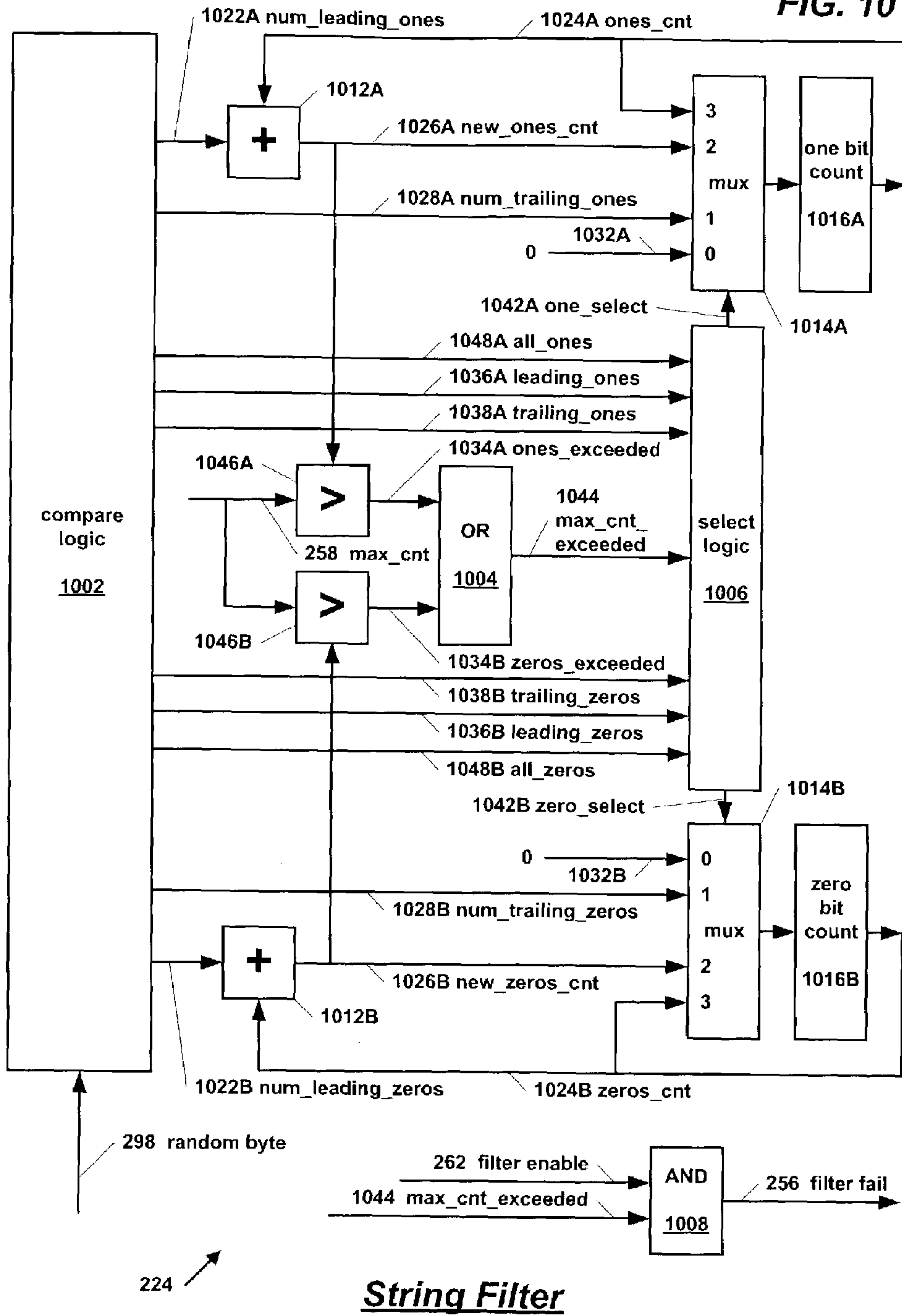
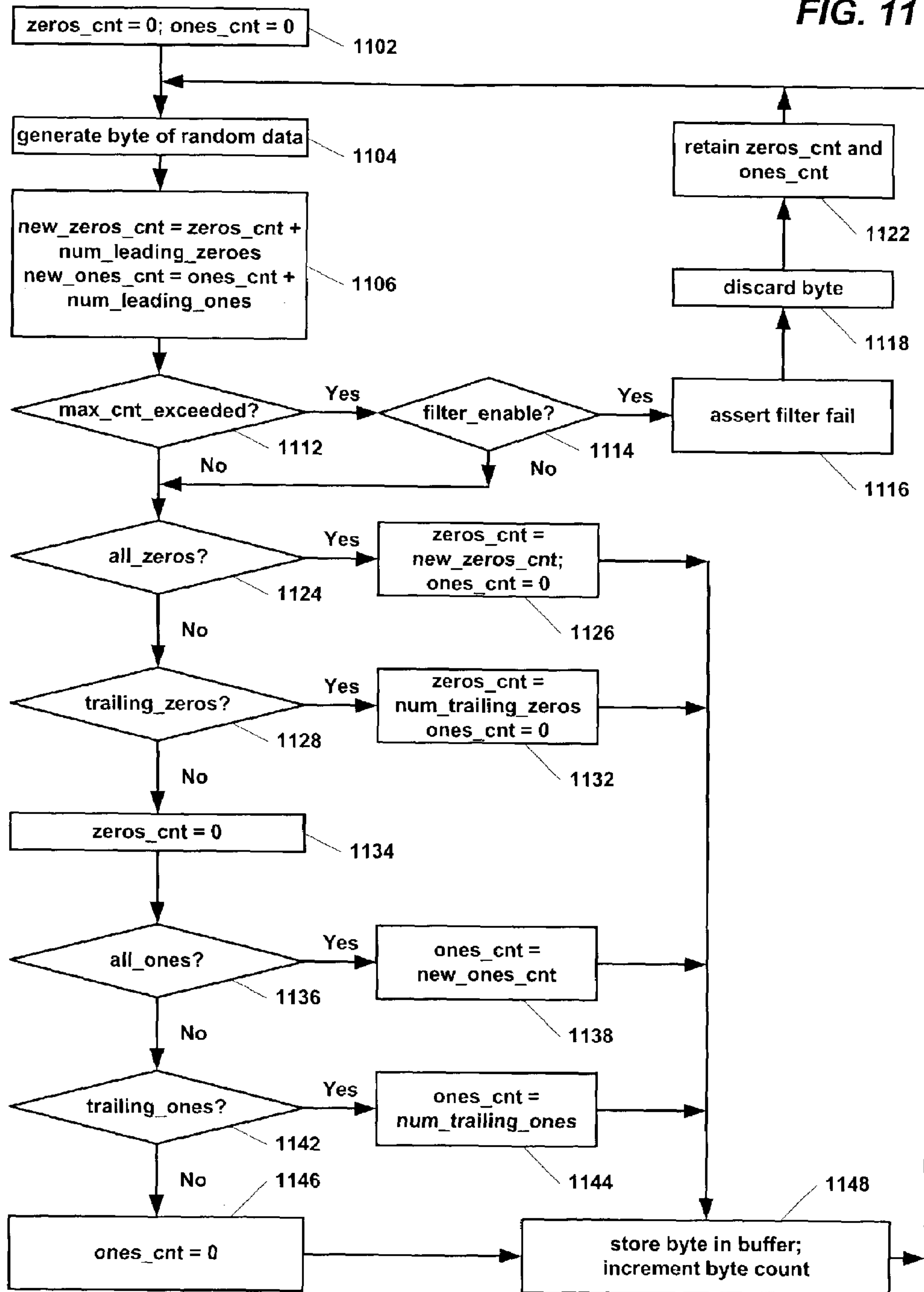
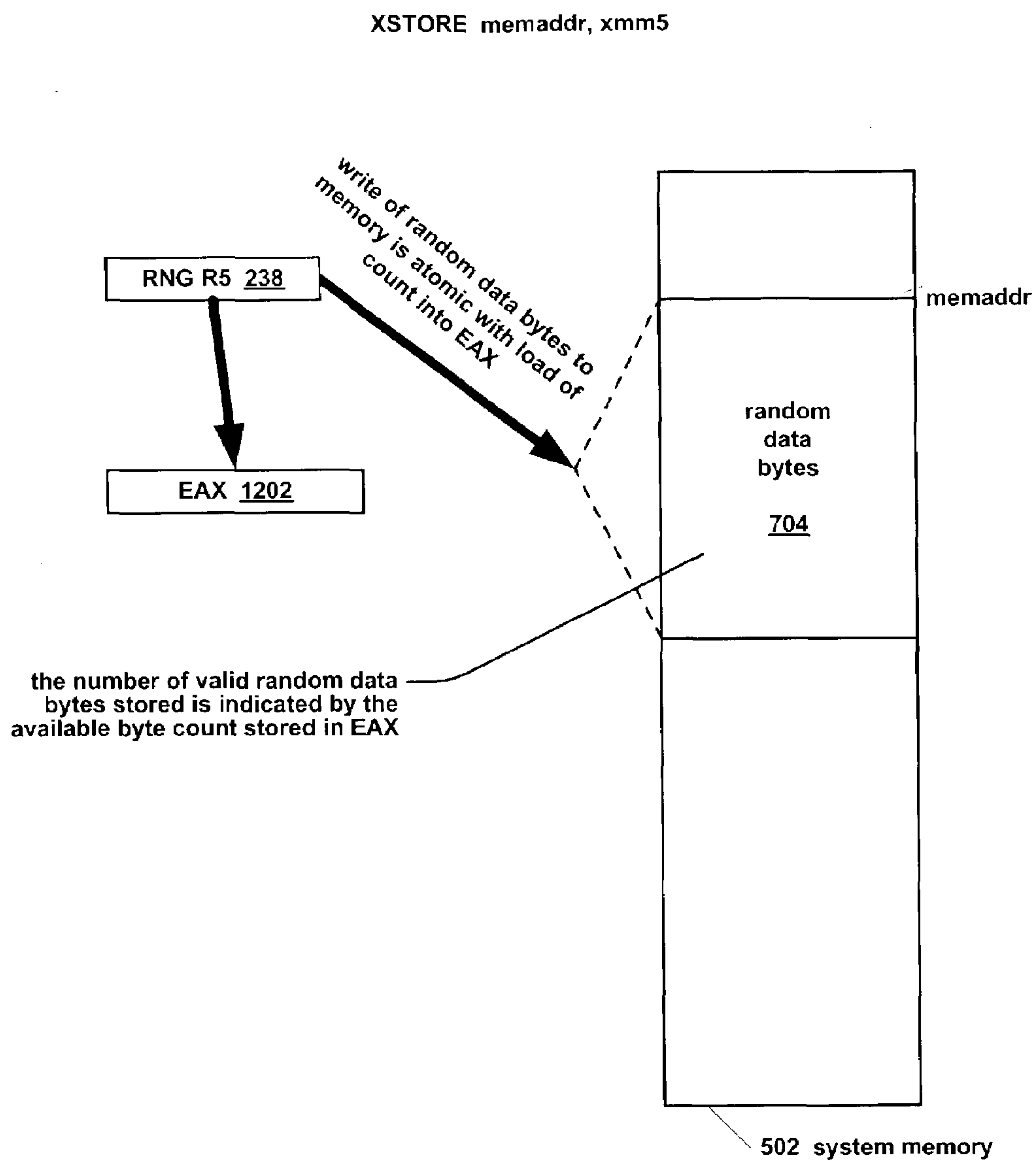


FIG. 11



String Filter Operation

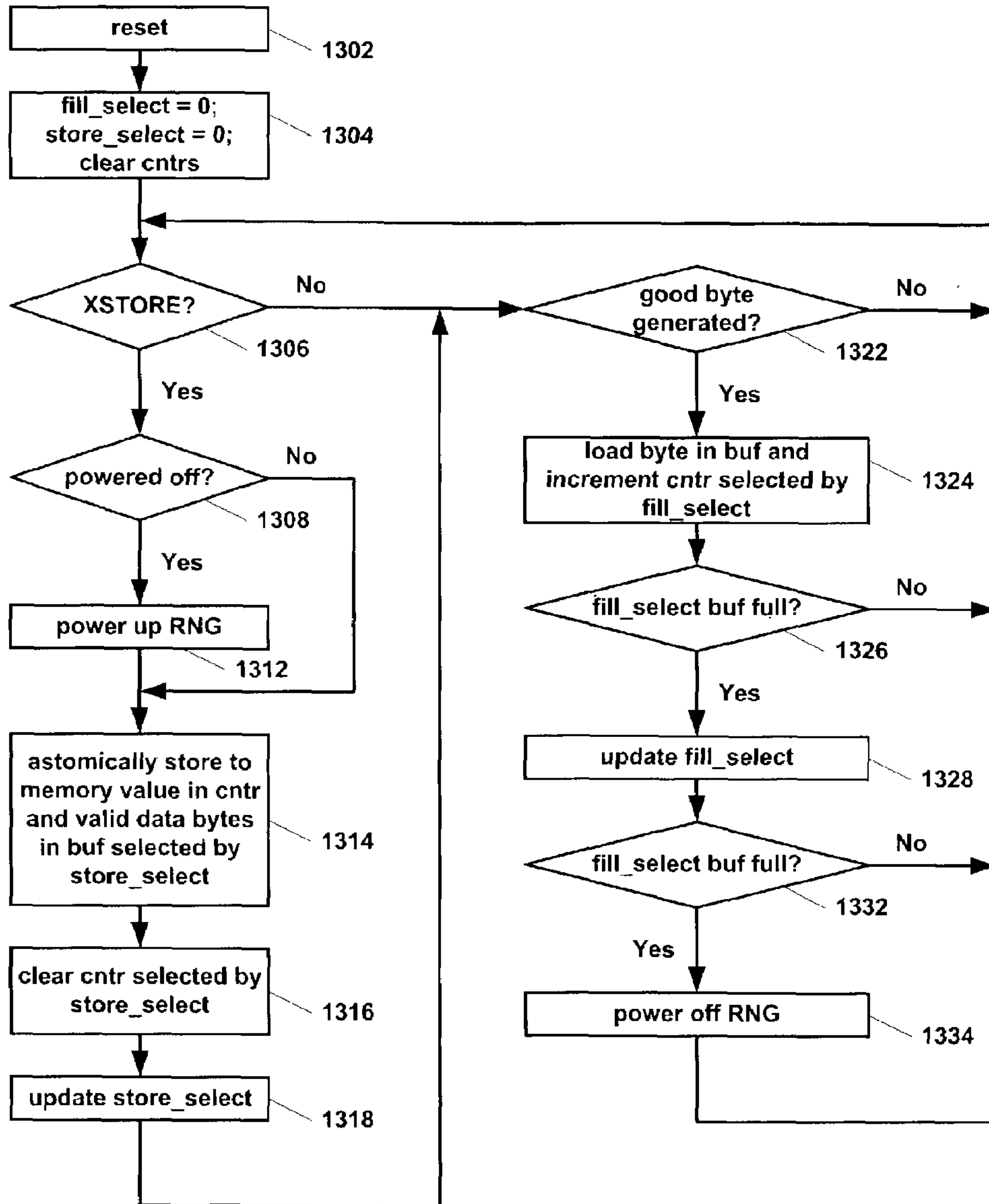
FIG. 12



**XSTORE instruction (Alternate Embodiment)**

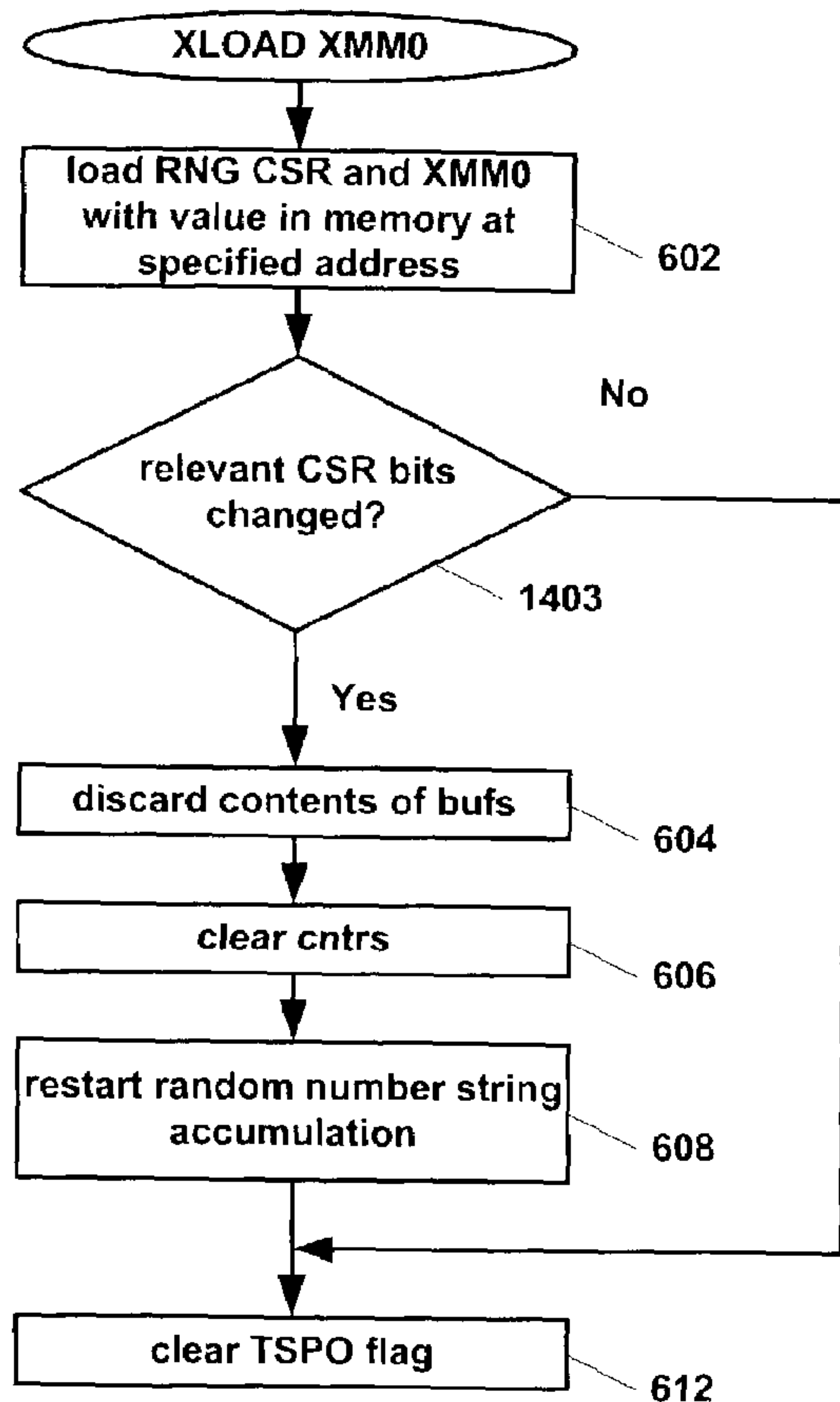


FIG. 13



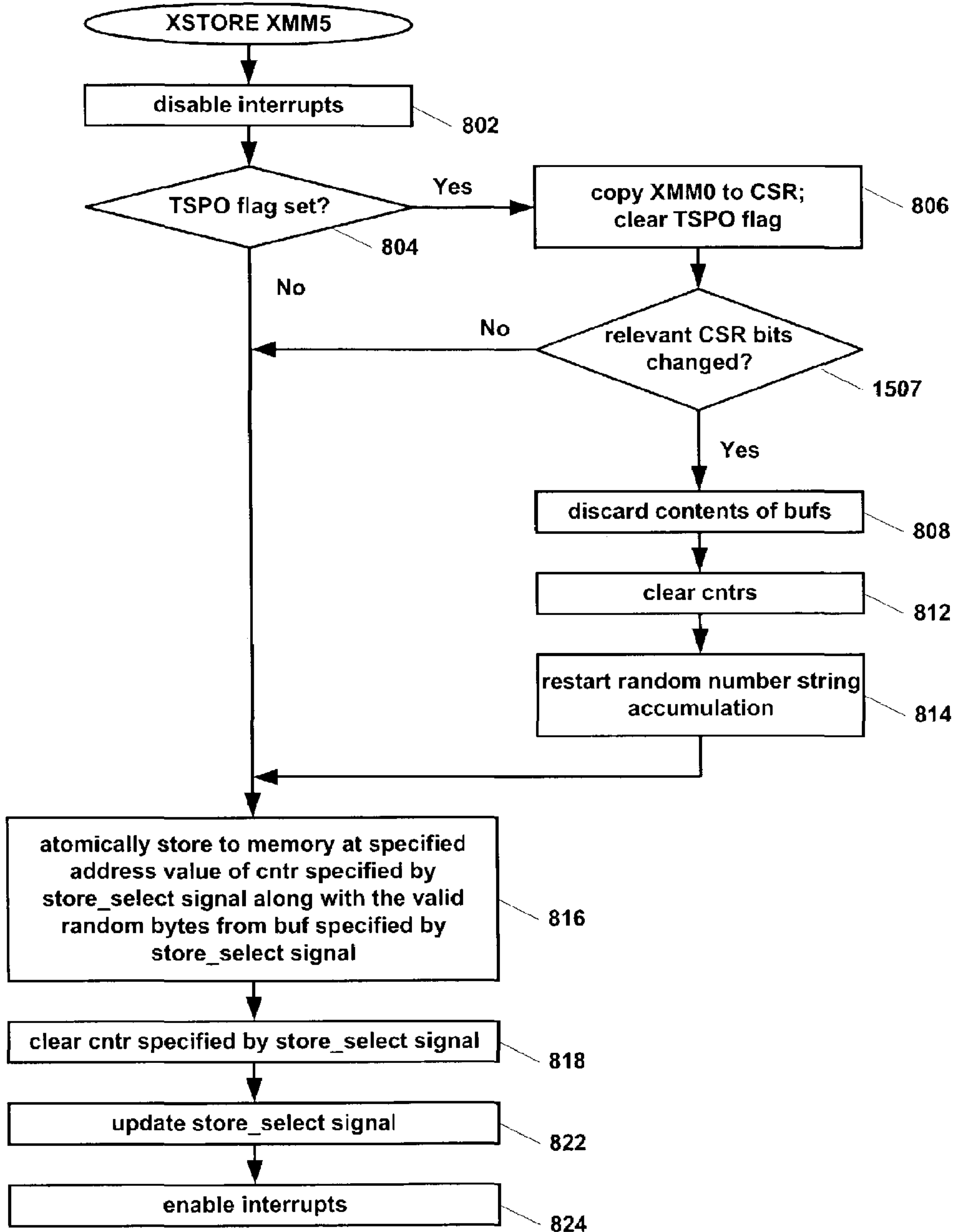
Multi-Buffering Operation

FIG. 14



**RNG Unit Operation (XLOAD XMM0 instruction)**  
**Alternate Embodiment**

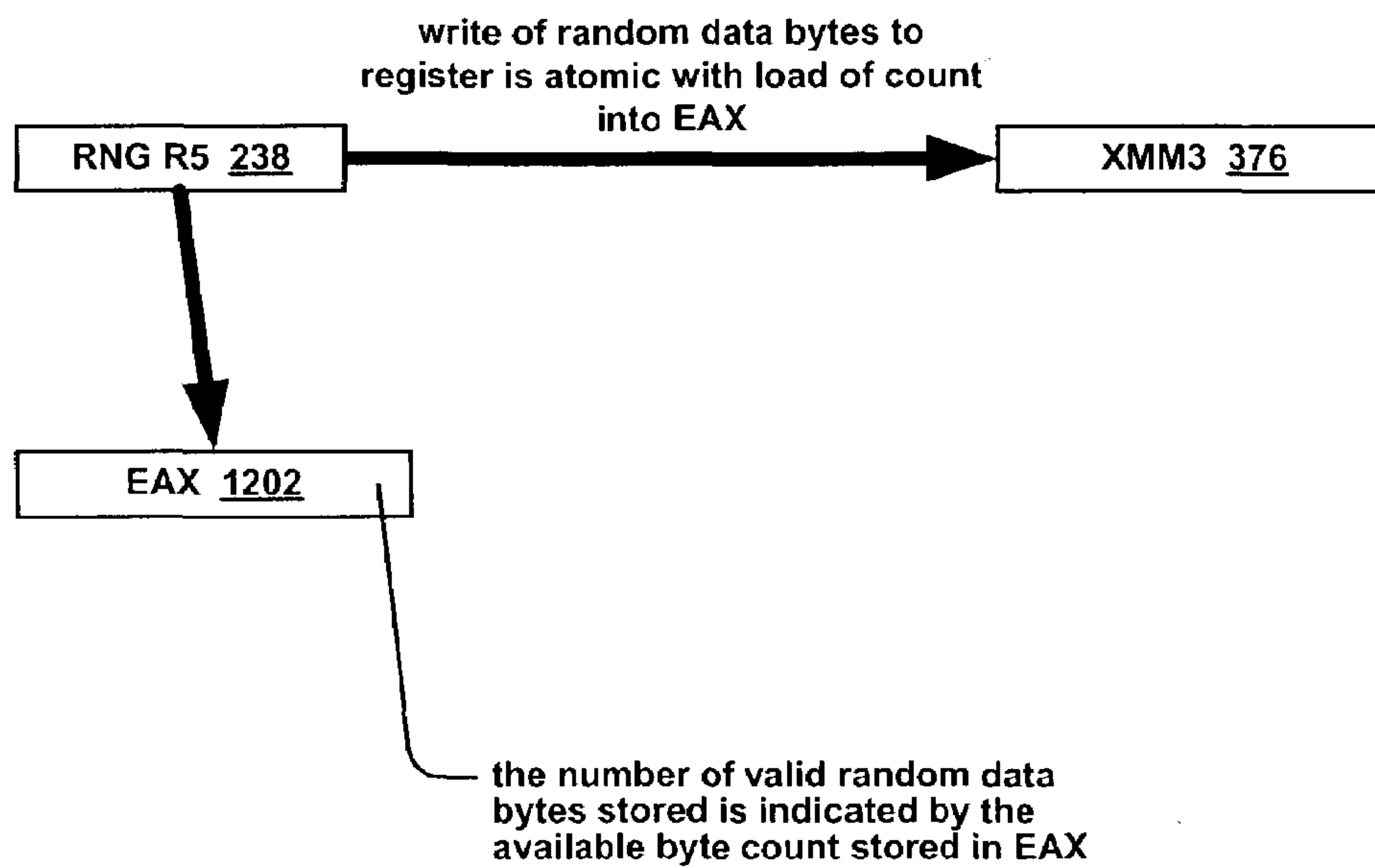
FIG. 15



**RNG Unit Operation (XSTORE XMM5 instruction)**  
**Alternate Embodiment**

FIG. 16

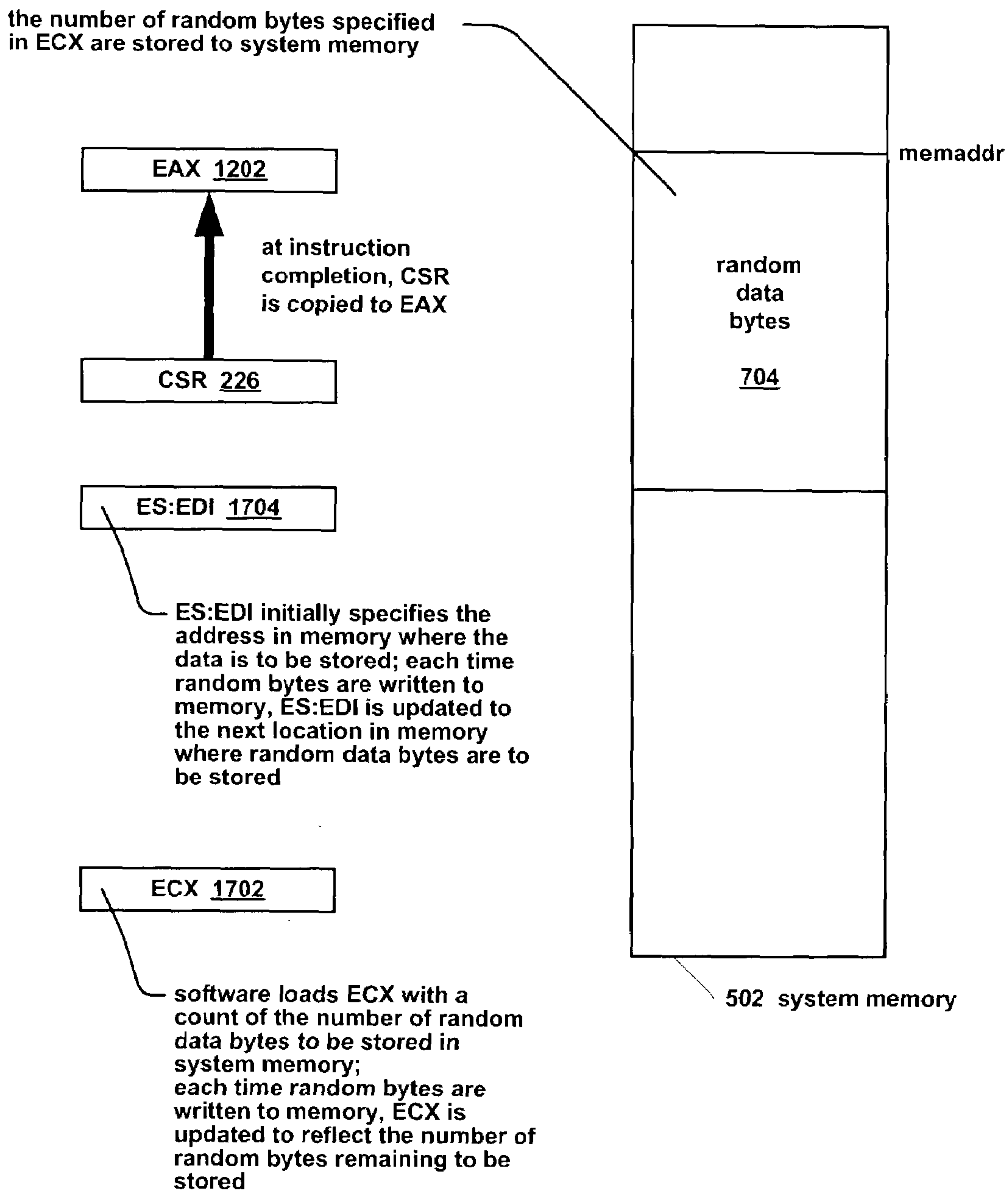
XSTORE xmm3, xmm5



**XSTORE instruction (Alternate Embodiment)**

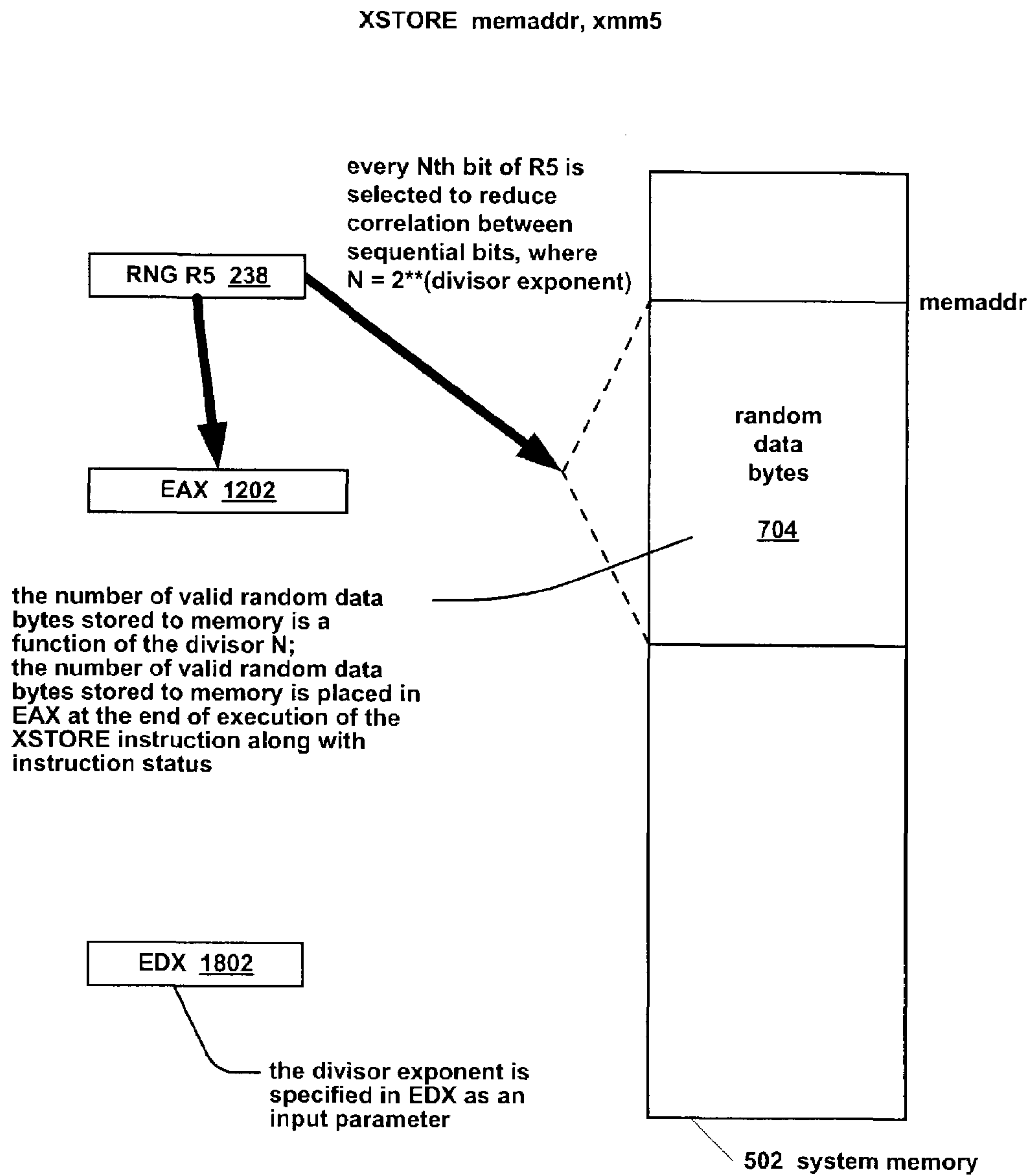
FIG. 17

REP XSTORE memaddr, xmm5



**REP XSTORE instruction**

**FIG. 18**



**XSTORE instruction (Alternate Embodiment)**



**FIG. 19**

```
R5[i] /7777777766666666555555554444444433333333222222221111111100000000
octal \76543210765432107654321076543210765432107654321076543210

R5      1010000111110001010100101011000101010010101000101010001010100011

if EDX == 0, then 8 bytes are stored to memory:
      1010000111110001010100101011000101010010101000101010001010100011

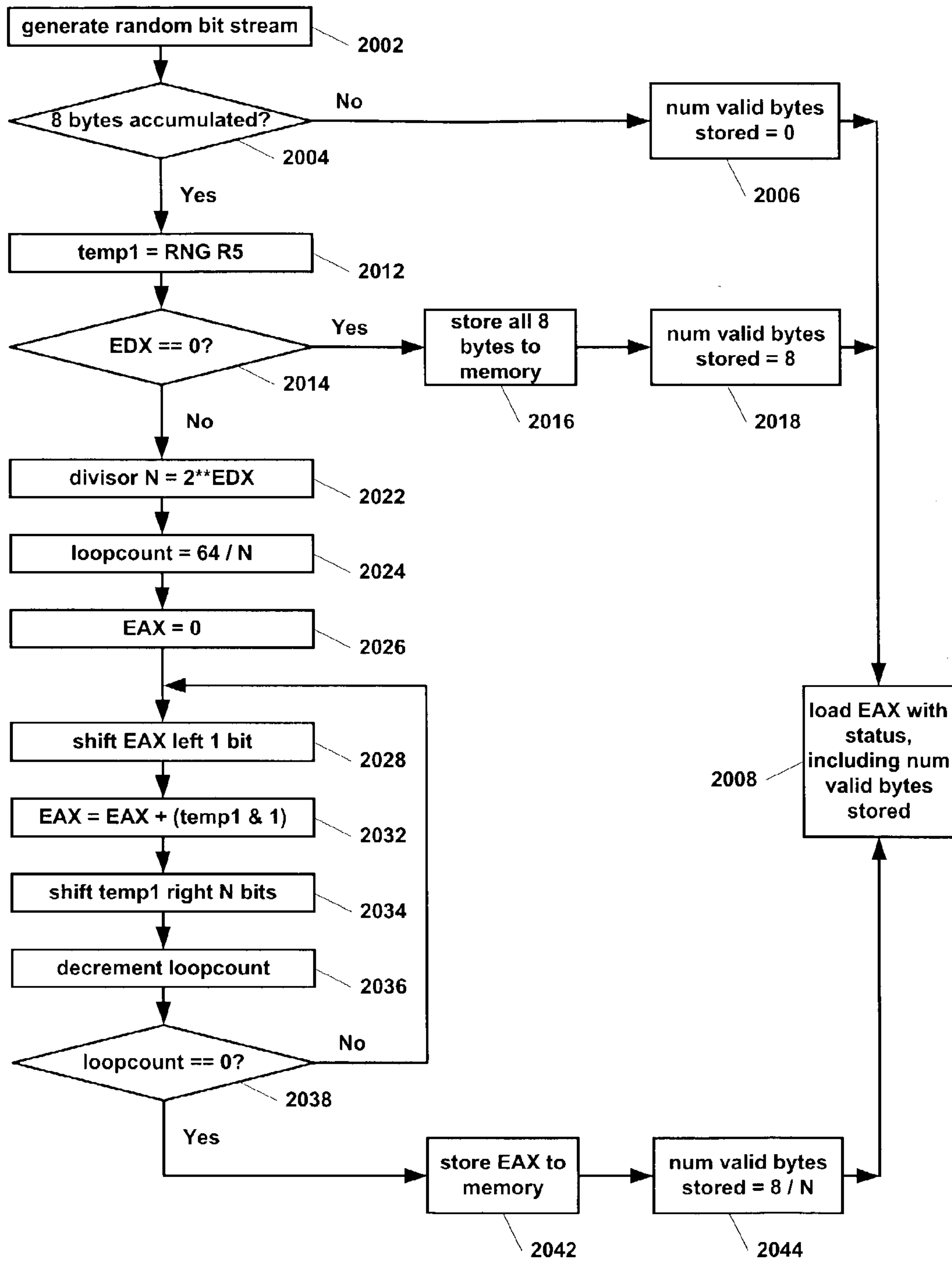
if EDX == 1, then 4 bytes are stored to memory:
      00011101110001011100000000000001

if EDX == 2, then 2 bytes are stored to memory:
      0111101110000001

if EDX == 3, then 1 byte is stored to memory:
      11010001
```

**Sequential Bit Correlation Reduction Example**

FIG. 20



**Sequential Bit Correlation Reducer Operation**

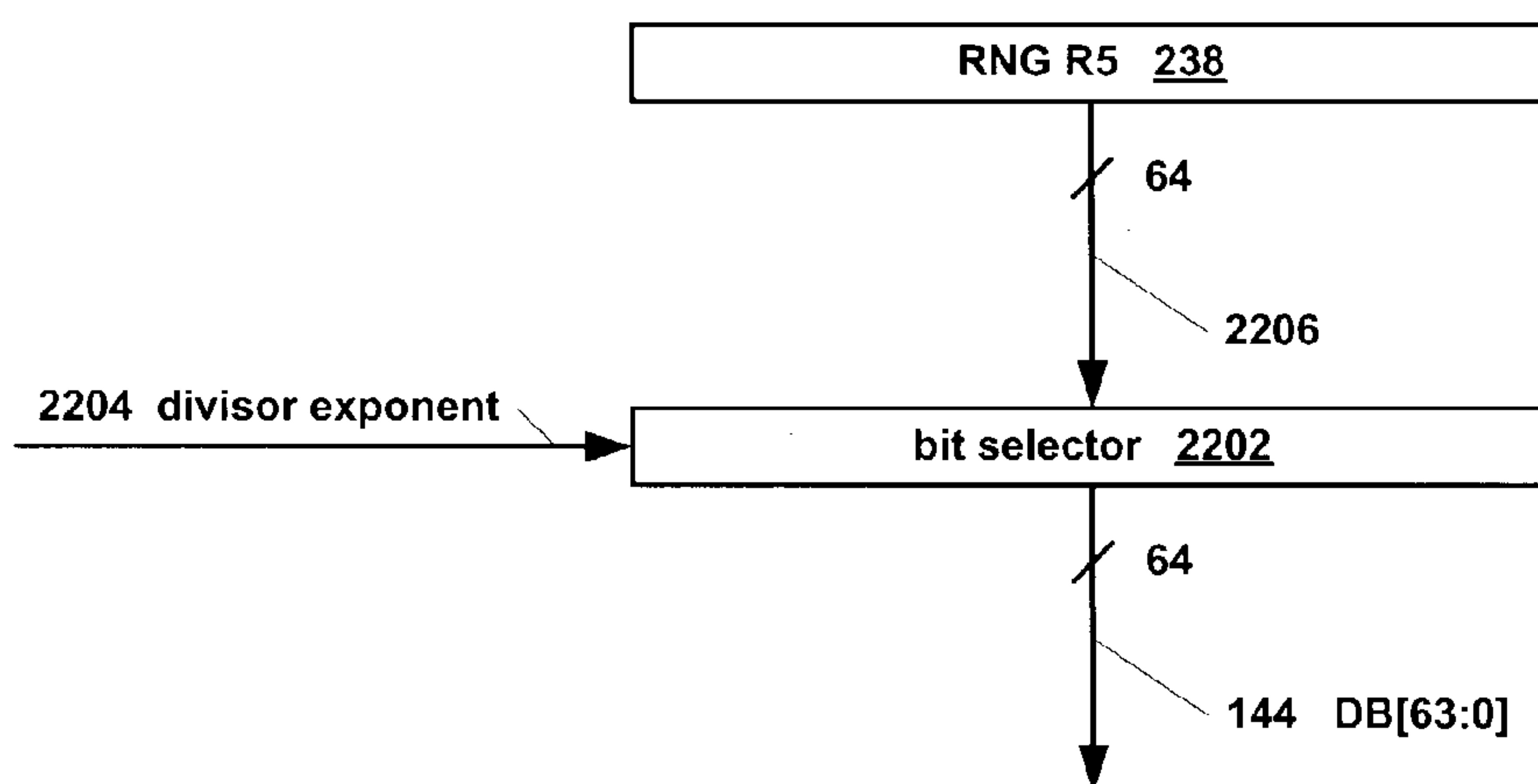
```

00  get_random_data:
01  dmtid      r2, r3          // Load the CSR into r2/r3.
02  andi      r1, r2, 0x08    // If 8 bytes are not available,
03  je.32     r1, 0, no_data  // store 0 bytes to memory.
04  andil     r2, r2, ~BYTE_COUNT_MASK // Strip avail byte count
05          // out of status and save cleared status in r2 in delay slot.
06  // r1 now holds value 8 and r2 holds status without count bits.
07  mfxd.64   xmm5
08  dmtid     r4, r5          // Load RNG R5 into r4/r5.
09
10  // EDX holds the divisor exponent.
11  xandi.32  EDX, EDX, 3     // If EDX==0, i.e., if not dividing,
12  jel.32    EDX, 0, store_all_bits // then store all 64 bits.
13  // r7 = 2**EDX, i.e., the divisor, which specifies
14  // how much to right shift the data [2, 4, or 8].
15  xaddi.32  r7, r0, 1
16  xshl.32   r7, r7, EDX
17  // r6 = 32 / 2**EDX, i.e., the loopcount, which is the number of
18  // bits we keep per 32 original bits.
19  // r1 = number of valid data bytes that will be stored to memory.
20  xaddi.32  r6, r0, 32
21  xshr.32   r6, r6, EDX
22  xshri.32  r1, r6, 2
23
24  // Use EAX to collect data now.  Afterward, load status into EAX.
25  xadd.32   EAX, 0, 0
26
27  first_block:
28  xshli.32  EAX, EAX, 1     // make room for next bit to accumulate
29  xandi.32  r3, r4, 1      // mask lowest order bit
30  xadd.32   EAX, EAX, r3   // ACCUMULATE
31  loopn.32  r6, 1, first_block
32  xshr.32   r4, r4, r7     // Shift the original data so that the
33  // next Nth bit is in the bottom of r4 in the delay slot.
34  // Recalculate the loopcount
35  xaddi.32  r6, r0, 32
36  xshr.32   r6, r6, EDX
37
38  second_block:
39  xshli.32  EAX, EAX, 1
40  xandi.32  r3, r5, 1
41  xadd.32   EAX, EAX, r3
42  loopn.32  r6, 1, second_block
43  xshr.32   r5, r5, r7
44
45  // CORRECTLY PACKED DATA IS IN EAX; cannot be more than 4 bytes
46  xs.32.AS  EAX, ESdesc, EDI, 0 // store accumulated bits to mem
47  return                                // Load EAX by adding status from r2 and
48  xadd.32   EAX, r2, r1 // number of valid random bytes from r1.
49  store_all_bits:
50  xs.32.AS  r4, ESdesc, EDI, 0 // store all 64 bits to memory
51  xs.32.AS  r5, ESdesc, EDI, 4
52  no_data: // Load EAX by adding status from r2 and number
53  return // of valid random bytes from r1, which is 0 or
54  xadd.32   EAX, r2, r1 // 8 depending on how we got here.

```

**FIG. 21****Sequential Bit Correlation Reducer Microcode**

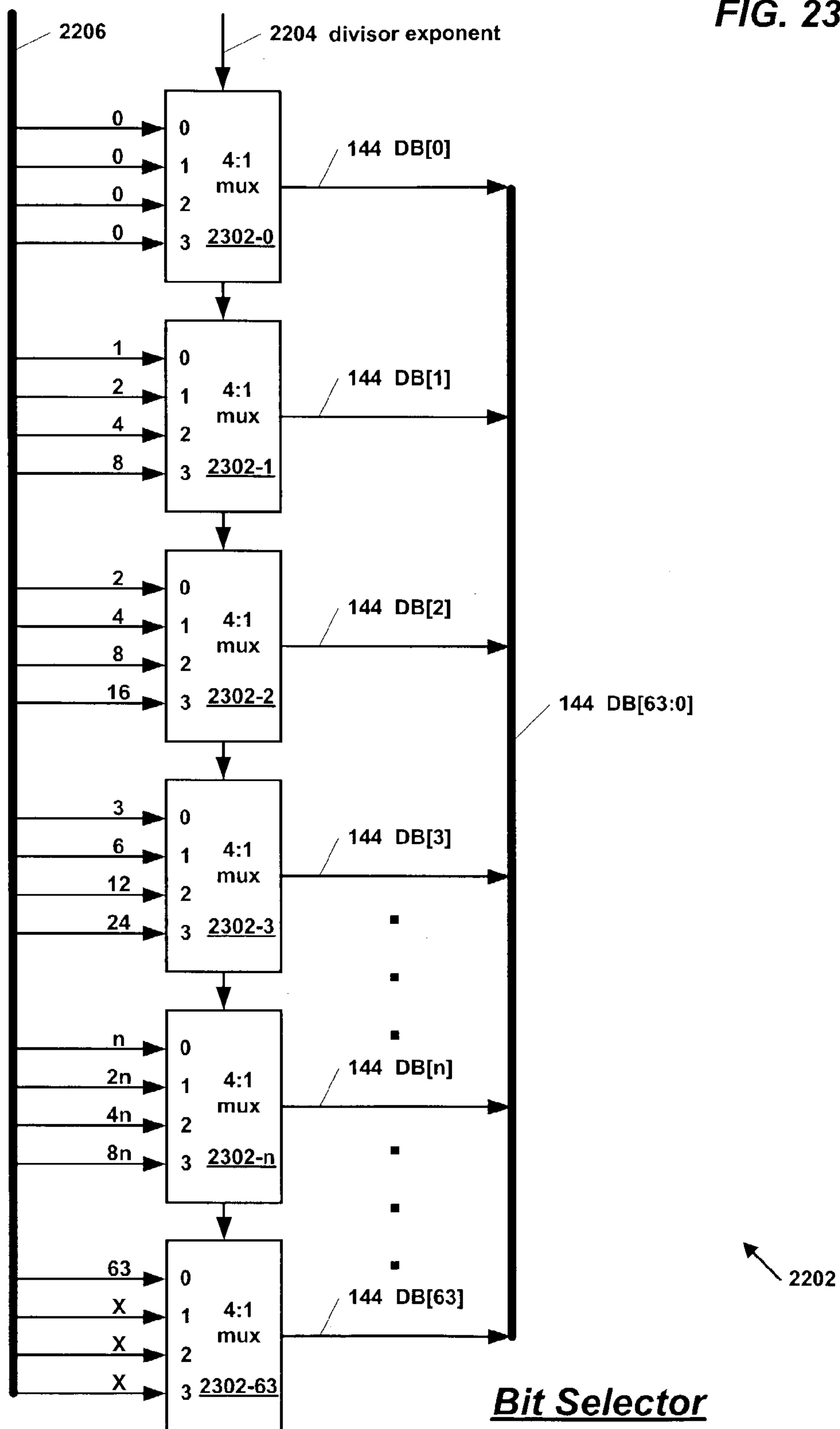
FIG. 22



136 ↗

**Sequential Bit Correlation Reducer Operation**  
**(Alternate Embodiment)**

FIG. 23





1

**APPARATUS AND METHOD FOR  
REDUCING SEQUENTIAL BIT  
CORRELATION IN A RANDOM NUMBER  
GENERATOR**

FIELD OF THE INVENTION

This invention relates in general to the field of random number generation, and particularly to non-random correlation between sequential bits.

BACKGROUND OF THE INVENTION

Historically, many computer software applications require a supply of random numbers. For example, Monte Carlo simulations of physical phenomena, such as large-scale weather simulations, require a supply of random numbers in order to simulate physical phenomenon. Other examples of applications requiring random numbers are casino games and on-line gambling to simulate card shuffling, dice rolling, etc.; lottery number creation; the generation of data for statistical analysis, such as for psychological testing; and use in computer games.

The quality of randomness needed, as well as the performance requirements for generating random numbers, differs among these types of applications. Many applications such as computer games have trivial demands on quality of randomness. Applications such as psychological testing have more stringent demands on quality, but the performance requirements are relatively low. Large-scale Monte Carlo-based simulations, however, have very high performance requirements and require good statistical properties of the random numbers, although non-predictability is not particularly important. Other applications, such as on-line gambling, have very stringent randomness requirements as well as stringent non-predictability requirements.

While these historical applications are still important, computer security generates the greatest need of high-quality random numbers. The recent explosive growth of PC networking and Internet-based commerce has significantly increased the need for a variety of security mechanisms.

High-quality random numbers are essential to all major components of computer security, which are confidentiality, authentication, and integrity.

Data encryption is the primary mechanism for providing confidentiality. Many different encryption algorithms exist, such as symmetric, public-key, and one-time pad, but all share the critical characteristic that the encryption/decryption key must not be easily predictable. The cryptographic strength of an encryption system is essentially the strength of the key, i.e., how hard it is to predict, guess, or calculate the decryption key. The best keys are long truly random numbers, and random number generators are used as the basis of cryptographic keys in all serious security applications.

Many successful attacks against cryptographic algorithms have focused not on the encryption algorithm but instead on its source of random numbers. As a well-known example, an early version of Netscape's Secure Sockets Layer (SSL) collected data from the system clock and process ID table to create a seed for a software pseudo-random number generator. The resulting random number was used to create a symmetric key for encrypting session data. Two graduate students broke this mechanism by developing a procedure for accurately guessing the random number to guess the session key in less than a minute.

2

Similar to decryption keys, the strength of passwords used to authenticate users for access to information is effectively how hard it is to predict or guess the password. The best passwords are long truly random numbers. In addition, in authentication protocols that use a challenge protocol, the critical factor is for the challenge to be unpredictable by the authenticating component. Random numbers are used to generate the authentication challenge.

Digital signatures and message digests are used to guarantee the integrity of communications over a network. Random numbers are used in most digital signature algorithms to make it difficult for a malicious party to forge the signature. The quality of the random number directly affects the strength of the signature. In summary, good security requires good random numbers.

Numbers by themselves are not random. The definition of randomness must include not only the characteristics of the numbers generated, but also the characteristics of the generator that produces the numbers. Software-based random number generators are common and are sufficient for many applications. However, for some applications software generators are not sufficient. These applications require hardware generators that generate numbers with the same characteristics of numbers generated by a random physical process. The important characteristics are the degree to which the numbers produced have a non-biased statistical distribution, are unpredictable, and are irreproducible.

Having a non-biased statistical distribution means that all values have equal probability of occurring, regardless of the sample size. Almost all applications require a good statistical distribution of their random numbers, and high-quality software random number generators can usually meet this requirement. A generator that meets only the non-biased statistical distribution requirement is called a pseudo-random number generator.

Unpredictability refers to the fact that the probability of correctly guessing the next bit of a sequence of bits should be exactly one-half, regardless of the values of the previous bits generated. Some applications do not require the unpredictability characteristic; however, it is critical to random number uses in security applications. If a software generator is used, meeting the unpredictability requirement effectively requires the software algorithm and its initial values be hidden. From a security viewpoint, a hidden algorithm approach is very weak. Examples of security breaks of software applications using a predictable hidden algorithm random number generator are well known. A generator that meets both the first two requirements is called a cryptographically secure pseudo-random number generator.

In order for a generator to be irreproducible, two of the same generators, given the same starting conditions, must produce different outputs. Software algorithms do not meet this requirement. Only a hardware generator based on random physical processes can generate values that meet the stringent irreproducibility requirement for security. A generator that meets all three requirements is called a truly random number generator.

Software algorithms are used to generate most random numbers for computer applications. These are called pseudo-random number generators because the characteristics of these generators cannot meet the unpredictability and irreproducibility requirements. Furthermore, some do not meet the non-biased statistical distribution requirements.

Typically, software generators start with an initial value, or seed, sometimes supplied by the user. Arithmetic operations are performed on the initial seed to produce a first random result, which is then used as the seed to produce a



second result, and so forth. Software generators are necessarily cyclical. Ultimately, they repeat the same sequence of output. Guessing the seed is equivalent to being able to predict the entire sequence of numbers produced. The irreproducibility is only as good as the secrecy of the algorithm and initial seed, which may be an undesirable characteristic for security applications. Furthermore, software algorithms are reproducible because they produce the same results starting with the same input. Finally, software algorithms do not necessarily generate every possible value within the range of the output data size, which may reflect poorly in the non-biased statistical distribution requirement.

A form of random number generator that is a hybrid of software generators and true hardware generators is an entropy generator. Entropy is another term for unpredictability. The more unpredictable the numbers produced by a generator, the more entropy it has. Entropy generators apply software algorithms to a seed generated by a physical phenomenon. For example, a highly used PC encryption program obtains its seed by recording characteristics of mouse movements and keyboard keystrokes for several seconds. These activities may or may not generate poor entropy numbers, and usually require some user involvement. The most undesirable characteristic of most entropy generators is that they are very slow to obtain sufficient entropy.

It should be clear from the foregoing that certain applications, including security applications, require truly random numbers which can only be generated by a random physical process, such as the thermal noise across a semiconductor diode or resistor, the frequency instability of a free-running oscillator, or the amount a semiconductor capacitor is charged during a particular time period. One way to generate random numbers is to generate a series of bits using one or more of the processes mentioned, and to form the bits into bytes or words to be used by the application. However, minor correlation between sequential generated bits has been observed under some environmental conditions. The correlation reduces the randomness of the numbers generated.

Therefore, what is needed is an apparatus and method for reducing the possible correlation between sequential bits generated by a random number generator.

#### SUMMARY OF THE INVENTION

The present invention provides a microprocessor that includes an apparatus and method to reduce the correlation between sequential bits generated by a hardware random number generator by selectively providing only a portion of the series of bits generated. Accordingly, in attainment of the aforementioned object, it is a feature of the present invention to provide a microprocessor. The microprocessor includes a random bit generator that generates a series of random bits, and an arithmetic logic unit (ALU), coupled to the random bit generator, which selects every Nth bit from the series of random bits and accumulates the every Nth bit selected into a register coupled to the ALU. N is an integer greater than 1. The microprocessor also includes an instruction translator that translates an instruction of an instruction set of the microprocessor. The instruction instructs the microprocessor to store the every Nth bit selected and accumulated. The microprocessor also includes a memory, coupled to the ALU, which stores microcode instructions. The microcode instructions include a plurality of instructions for performing the instruction. The plurality of instructions comprises one

or more instructions for instructing the ALU to shift the series of random bits by the N.

In another aspect, it is a feature of the present invention to provide an apparatus for reducing correlation between sequential random bits. The apparatus includes a random bit generator, which generates a stream of random bits. The apparatus also includes a first register, coupled to the random bit generator, which stores a plurality of the stream of random bits. The apparatus also includes a plurality of multiplexers, coupled to the first register, which select every Nth bit of the plurality of the stream of random bits. The plurality of multiplexers selects the every Nth bit based on a control signal. The apparatus also includes a second register, coupled to the plurality of multiplexers, which stores the every Nth bit of the plurality of the stream of random bits selected by the plurality of multiplexers.

An advantage of the present invention is that it potentially reduces the correlation between sequential bits while enabling the user to make the tradeoff between a higher rate of random number delivery and a higher degree of randomness in the random numbers delivered.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a microprocessor according to the present invention.

FIG. 2 is a block diagram illustrating the RNG unit of the microprocessor of FIG. 1 according to the present invention.

FIG. 3 is a block diagram illustrating various registers in the microprocessor of FIG. 1 related to the RNG unit of FIG. 1 according to the present invention.

FIG. 4 is a flowchart illustrating operation of the microprocessor of FIG. 1 when executing an instruction that loads a value into the XMM0 register of FIG. 3 according to the present invention.

FIG. 5 is a block diagram illustrating operation of the microprocessor of FIG. 1 when executing an XLOAD instruction according to the present invention.

FIG. 6 is a flowchart illustrating operation of the microprocessor of FIG. 1 when executing an XLOAD instruction according to the present invention.

FIG. 7 is a block diagram illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to the present invention.

FIG. 8 is a flowchart illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to the present invention.

FIG. 9 is a flowchart illustrating an example of multi-tasking operation of the microprocessor of FIG. 1 with respect to random number generation according to the present invention.

FIG. 10 is a block diagram illustrating the string filter of the RNG unit of FIG. 2 of the microprocessor of FIG. 1 according to the present invention.

FIG. 11 is a flowchart illustrating operation of the string filter of FIG. 10 according to the present invention.

FIG. 12 is a block diagram illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention.

FIG. 13 is a flowchart illustrating multi-buffering operation of the RNG unit of FIG. 2 according to the present invention.



## 5

FIG. 14 is a flowchart illustrating operation of the microprocessor of FIG. 1 when executing an XLOAD instruction according to an alternate embodiment of the present invention.

FIG. 15 is a flowchart illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention.

FIGS. 16 and 17 are block diagrams illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to alternate embodiments of the present invention.

FIG. 18 is a block diagram illustrating operation of the microprocessor of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention.

FIG. 19 is an illustration of an example of operation of the XSTORE instruction of FIG. 18 according to the present invention.

FIG. 20 is a flowchart illustrating operation of the RNG unit of FIG. 1 to reduce sequential bit correlation according to one embodiment of the present invention.

FIG. 21 is a listing of microcode instructions for instructing the microprocessor of FIG. 1 to reduce sequential bit correlation according to the present invention.

FIG. 22 is a block diagram illustrating portions of the RNG unit of FIG. 1 including a bit selector to reduce sequential bit correlation according to an alternate embodiment of the present invention.

FIG. 23 is a block diagram illustrating the bit selector of FIG. 22 in detail according to the present invention.

## DETAILED DESCRIPTION

Referring now to FIG. 1, a block diagram illustrating a microprocessor 100 according to the present invention is shown. Microprocessor 100 of FIG. 1 is a pipelined microprocessor comprising multiple stages, each of which performs a portion of the execution of program instructions as described below.

Microprocessor 100 includes a random number generator (RNG) unit 136. Microprocessor 100 executes operating systems and application programs that may require a supply of random numbers for various functions such as data encryption, simulations of physical phenomena, statistical analysis, or numerical analysis, among others. RNG unit 136 generates random numbers for these uses. RNG unit 136 will be described in more detail below.

Microprocessor 100 also includes an instruction cache 102. Instruction cache 102 caches program instructions fetched from a system memory coupled to microprocessor 100.

Microprocessor 100 also includes an instruction fetcher 104 coupled to instruction cache 102. Instruction fetcher 104 controls the fetching of the instructions from the system memory and/or instruction cache 102. Instruction fetcher 104 selects a value for an instruction pointer maintained by microprocessor 100. The instruction pointer specifies the next memory address from which to fetch instructions. Normally the instruction pointer is sequentially incremented to the next instruction. However, control flow instructions, such as branches, jumps, subroutine calls and returns, may cause the instruction pointer to be updated to a non-sequential memory address specified by the control flow instruction. In addition, interrupts may cause the instruction fetcher 104 to update the instruction pointer to a non-sequential address.

## 6

Microprocessor 100 also includes an interrupt unit 146 coupled to instruction fetcher 104. Interrupt unit 146 receives an interrupt signal 148 and an interrupt vector 152. An entity external to microprocessor 100 may assert the interrupt signal 148 and provide an interrupt vector 152 to cause microprocessor 100 to execute an interrupt service routine. Interrupt unit 146 determines the memory address of an interrupt service routine based on the interrupt vector 152 and provides the interrupt service routine memory address to instruction fetcher 104, which updates the instruction pointer to the interrupt service routine address. Interrupt unit 146 also selectively disables and enables interrupt servicing depending upon the particular instructions being executed by microprocessor 100. That is, if interrupts are disabled, then the instruction pointer will not be changed even though interrupt line 148 is asserted until interrupts are enabled.

Microprocessor 100 also includes an instruction translator 106 coupled to instruction fetcher 104, interrupt unit 146, and RNG unit 136. Instruction translator 106 translates instructions received from instruction cache 102 and/or system memory. Instruction translator 106 translates the instructions and takes appropriate actions based on the type of instruction translated. Instruction translator 106 translates instructions defined in the instruction set of microprocessor 100. Instruction translator 106 generates an illegal instruction exception if it translates an instruction that is not defined in the instruction set of microprocessor 100.

In one embodiment, the instruction set of microprocessor 100 is substantially similar to the instruction set of an Intel® Pentium III® or Pentium IV® microprocessor. However, advantageously microprocessor 100 of the present invention includes additional instructions relating to the generation of random numbers by RNG unit 136. One additional instruction is an XSTORE instruction that stores random numbers generated by RNG unit 136. Another additional instruction is an XLOAD instruction that loads control values from system memory into a control and status register (CSR) 226 in RNG unit 136 and into a Streaming SIMD Extensions (SSE) register XMM0 372, which are described below with respect to FIGS. 2 and 3. The XSTORE and XLOAD instructions are described in more detail below.

Additionally, instruction translator 106 provides information about translated instructions to interrupt unit 146 to enable interrupt unit 146 to appropriately enable and disable interrupts. Furthermore, instruction translator 106 provides information about translated instructions to RNG unit 136. For example, instruction translator 106 provides information to RNG unit 136 about translated XSTORE and XLOAD instructions. In addition, instruction translator 106 informs RNG unit 136 when an instruction is translated that loads values into SSE register XMM0 372, in response to which RNG unit 136 takes certain actions, such as setting a flag to indicate the possible occurrence of a task switch by the operating system, as described below.

In one embodiment, instruction translator 106 translates a macroinstruction, such as a Pentium III or IV instruction, into one or more microinstructions that are executed by the microprocessor 100 pipeline.

Microprocessor 100 also includes a microcode memory 132 coupled to instruction translator 106. Microcode memory 132 stores microcode instructions for provision to instruction translator 106 to be executed by microprocessor 100. Some of the instructions in the instruction set of microprocessor 100 are implemented in microcode. That is, when instruction translator 106 translates one of these instructions, instruction translator 106 causes a routine of



microinstructions within microcode memory **132** to be executed to perform the translated macroinstruction. In one embodiment, the XSTORE and/or XLOAD instructions are implemented in microcode. Additionally, in one embodiment, the XSTORE and XLOAD instructions are atomic because they are uninterruptible. That is, interrupts are disabled during the execution of XSTORE and XLOAD instructions.

Microprocessor **100** also includes a register file **108** coupled to instruction translator **106**. Register file **108** includes the user-visible and non-user-visible registers of microprocessor **100**. In one embodiment, register file **108** includes eight 32-bit general-purpose non-user-visible registers denoted r0 through r7. In one embodiment, the user-visible registers of register file **108** include the user-visible register set of a Pentium III or IV. SSE registers **352** of FIG. **3** are included in register file **108**. SSE registers **352** are used by an SSE unit **134** included in microprocessor **100** and by RNG unit **136**, as described below. In particular, register file **108** includes registers that are known to contemporary operating systems. Consequently, when an operating system switches from a first task to a second task, the operating system saves to system memory the registers in register file **108**, including SSE registers **352**, for the first task and restores from system memory the registers in register file **108**, including SSE registers **352**, for the second task.

Microprocessor **100** also includes an address generator **112** coupled to register file **108**. Address generator **112** generates memory addresses based on operands stored in register file **108** and based on operands supplied by the instructions translated by instruction translator **106**. In particular, address generator **112** generates a memory address specifying the location in system memory to which an XSTORE instruction stores bytes of random data. Additionally, address generator **112** generates a memory address specifying the location in system memory from which an XLOAD instruction loads control values for storage in CSR **226** of FIG. **2** via a data bus **142**.

Microprocessor **100** also includes a load unit **114** coupled to address generator **112**. Load unit **114** loads data from the system memory into microprocessor **100**. Load unit **114** also includes a data cache that caches data read from the system memory. Load unit **114** loads data for provision to execution units in microprocessor **100**, such as SSE unit **134**, RNG unit **136** and execution units included in execute stage **116**, on data bus **142**. In particular, load unit **114** loads control values from system memory for storage in CSR **226** of FIG. **2** to execute an XLOAD instruction.

Microprocessor **100** also includes execute stage **116** coupled to load unit **114** via data bus **142**. Execute stage **116** includes execution units such as an arithmetic logic unit (ALU) **162** for performing arithmetical and logical operations, such as add, subtract, multiply, divide, AND, OR, shift left/right, etc. In one embodiment, execute stage **116** includes an integer unit for performing integer operations and a floating-point unit for performing floating-point operations.

Microprocessor **100** also includes SSE unit **134** coupled to load unit **114** and instruction translator **106**. SSE unit **134** includes arithmetic and logic units for executing SSE instructions, such as those included in the Pentium III and IV SSE or SSE2 instruction set. In one embodiment, although SSE registers **352** of FIG. **3** are included conceptually in register file **108**, they are physically located in SSE unit **134** for storing operands used by SSE unit **134**.

Microprocessor **100** also includes RNG unit **136** coupled to instruction translator **106** and to load unit **114** via data bus

**142**. RNG unit **136** provides on a data bus **144** the random data bytes and a count specifying the number of random data bytes provided for an XSTORE instruction. RNG unit **136** will be described in more detail below with respect to the remaining Figures.

Microprocessor **100** also includes a store unit **118** coupled to execute unit **116**, SSE unit **134**, and RNG unit **136**. Store unit **118** stores data to the system memory and the data cache of load unit **114**. Store unit **118** stores results generated by execute unit **116**, SSE unit **134**, and RNG unit **136** to system memory. In particular, store unit **118** stores XSTORE instruction count and random data bytes provided on data bus **144** by RNG unit **136** to system memory.

Microprocessor **100** also includes a write-back unit **122** coupled to execute unit **116** and register file **108**. Write-back unit **122** writes back instruction results to register file **108**.

Microprocessor **100** also includes write buffers **124** coupled to write-back unit **122**. Write buffers **124** hold data waiting to be written to system memory, such as XSTORE instruction count and data.

Microprocessor **100** also includes a bus interface unit (BIU) **128** coupled to write buffers **124**. BIU **128** interfaces microprocessor **100** with a processor bus **138**. Processor bus **138** couples microprocessor **100** to the system memory. BIU **128** performs bus transactions on processor bus **138** to transfer data between microprocessor **100** and system memory. In particular, BIU **128** performs one or more bus transactions on processor bus **138** to store XSTORE instruction count and data to system memory. Additionally, BIU **128** performs one or more bus transactions on processor bus **138** to load XLOAD instruction control values from system memory.

Microprocessor **100** also includes read buffers **126** coupled to BIU **128** and register file **108**. Read buffers **126** hold data received from system memory by BIU **128** while waiting to be provided to load unit **114** or register file **108**. In particular, read buffers **126** hold XLOAD instruction data received from system memory while waiting to be provided to load unit **114** and subsequently to RNG unit **136**.

Referring now to FIG. **2**, a block diagram illustrating RNG unit **136** of microprocessor **100** of FIG. **1** according to the present invention is shown.

RNG unit **136** includes control logic **244**. Control logic **244** includes a large amount of combinatorial and sequential logic for controlling various elements of RNG unit **136**. Control logic **244** receives an xload signal **272** and an xstore signal **268** that indicate an XLOAD or XSTORE instruction, respectively, is being executed. Control logic **244** also receives a reset signal **248** that indicates RNG unit **136** is being reset. Control logic **244** is described below in detail in connection with the remainder of RNG unit **136**.

RNG unit **136** also includes a self-test unit **202** coupled to control logic **244**. Self-test unit **202** receives a self-test enable signal **292** from a control and status register, referred to as machine specific register (MSR) **212**, which is described in more detail with respect to FIG. **3** below. MSR **212** is also coupled to control logic **244**. Self-test unit **202** provides a self-test fail signal **288** to control logic **244**. Self-test unit **202** performs various self-tests of RNG unit **136** if enabled by self-test enable signal **292**. If the self-tests fail, self-test unit **202** generates a true value on self-test fail signal **288**, which is also provided to MSR **212**. In one embodiment, self-test unit **202** performs statistical random number generator tests as defined by the Federal Information Processing Standards (FIPS) Publication 140-2 at pages 35-36, which are hereby incorporated by reference.



In one embodiment, self-test unit **202** performs the self-tests upon demand by a user. In one embodiment, self-test unit **202** performs the self-tests after a reset of microprocessor **100**. If the self-tests fail, either on demand or on reset, self-test unit **202** generates a true value on self-test fail signal **288**, which is reflected in a self-test failed bit **318** of FIG. **3** of MSR **212**. Control logic **244** examines the self-test failed bit **318** on reset. If the self-test failed bit **318** is true, then control logic **244** asserts a false value on an RNG present signal **286** that is provided to MSR **212** for updating an RNG present bit **314** of FIG. **3**.

RNG present signal **286** is also provided to a CPUID register **204** that includes an RNG present bit **302** of FIG. **3** that is also updated by RNG present signal **286**. That is, RNG present bit **302** of CPUID register **204** is a copy of RNG present bit **314** of MSR **212**. In one embodiment, an application program may read CPUID register **204** by executing a CPUID instruction in the IA-32 instruction set. If RNG present bit **302** is false, then microprocessor **100** indicates that RNG unit **136** is not present and the random number generation features of microprocessor **100** are not available. Advantageously, an application requiring random numbers may detect the absence of RNG unit **136** in microprocessor **100** via RNG present bit **302** and choose to obtain random numbers by another, perhaps lower performance, source if the RNG unit **136** is not present.

RNG unit **136** also includes two random bit generators, denoted random bit generator **0 206** and random bit generator **1 208**, coupled to control logic **244**. Each of the random bit generators **206** and **208** generate a stream of random bits that are accumulated by RNG unit **136** into bytes of random data. Each of the random bit generators **206** and **208** receive a power\_cntrl signal **231** that specifies whether to power down the random bit generators **206** and **208**. In one embodiment, powering down the random bit generators **206** and **208** comprises not providing a clock signal to them. The random bit generators **206** and **208** each generate a series of random data bits based on random electrical characteristics of microprocessor **100**, such as thermal noise.

Random bit generator **0 206** receives a DC bias signal **296** from MSR **212**. DC bias signal **296** conveys a value stored in DC bias bits **322** of FIG. **3** of MSR **212**. The DC bias signal **296** value specifies a direct current bias voltage for partially controlling an operating voltage of free running ring oscillators in random bit generator **0 206**.

Random bit generator **0 206** is described in detail in pending U.S. patent application Ser. Nos. 10/046,055, 10/046,054, and 10/046,057 entitled APPARATUS FOR GENERATING RANDOM NUMBERS, OSCILLATOR BIAS VARIATION MECHANISM, and OSCILLATOR FREQUENCY VARIATION MECHANISM, respectively, which are hereby incorporated by reference in their entirety.

RNG unit **136** also includes a two-input mux **214** whose inputs are coupled to the outputs of random bit generators **206** and **208**. Mux **214** selects one of the two inputs based on a control signal gen select **252** provided by CSR **226**. The gen select signal **252** conveys a value stored in a gen select **336** of FIG. **3** in CSR **226**.

RNG unit **136** also includes a von Neumann whitener, or compressor, **216** coupled to the output of mux **214**. Whitener **216** is selectively enabled/disabled by a raw bits signal **254** received from MSR **212**. The raw bits signal **254** conveys a value stored in raw bits field **324** of FIG. **3** of MSR **212**. If raw bits signal **254** is true, then whitener **216** simply passes the bits received from mux **214** through to its output without performing the whitening function. Whitener **216** functions to significantly reduce residual bias that may exist in random

bit generators **206** and **208** by receiving a pair of bits from mux **214** and outputting either one or one or none bits according to a predetermined input/output function. The input/output function of whitener **216** is described in Table 1 below.

TABLE 1

Input	Output
00	nothing
01	0
10	1
11	nothing

RNG unit **136** also includes an eight-bit shift register **218** coupled to whitener **216**. Shift register **218** buffers random data bits received from whitener **216**, accumulates the random data bits into eight-bit bytes, and outputs the accumulated random data bytes. Shift register **218** asserts a byte\_generated signal **282** to control logic **244** to indicate that it has accumulated and output a random data byte **298**.

RNG unit **136** also includes a continuous number test (CNT) unit **222** coupled to the output of shift register **218**. CNT unit **222** receives random bytes **298** from shift register **218** and performs a continuous random number generator test on the random bytes **298**. CNT unit **222** is selectively enabled/disabled by a CNT enable signal **284** received from CSR **226**. CNT enable signal **284** conveys a value stored in a CNT enable bit **342** of FIG. **3** of CSR **226**. If the continuous random number generator test fails, CNT unit **222** asserts a CNT fail signal **294** provided to CSR **226**, which is stored in CNT failed bit **344** of FIG. **3** in CSR **226**.

In one embodiment, the continuous random number generator test performed by CNT unit **222** substantially conforms to the continuous random number generator test described on page **37** in FIPS **140-2**, which is hereby incorporated by reference. In one embodiment, CNT unit **222** performs the test by employing two eight-byte buffers, referred to as “old” and “new.” After a reset, and after self-test if it is enabled, the first eight bytes delivered by shift register **218** are accumulated in buffer old. The next eight bytes are accumulated in buffer new. When an XSTORE instruction is executed, the eight bytes in buffer old are compared with the eight bytes in buffer new. If the bytes are not equal, then the test passes and the eight bytes in buffer new are moved to buffer old, and buffer new is cleared awaiting accumulation of eight more bytes. However, if the bytes are equal, CNT unit **222** asserts the CNT fail signal **294** to signify that the continuous random number generator test failed.

In one embodiment, XSTORE instructions will return an available byte count of zero as long as the CNT enable **342** and CNT failed **344** bits of FIG. **3** are set. In one embodiment, microprocessor **100** stores the available byte count and random data bytes to system memory on the particular XSTORE instruction execution that triggered the continuous random number generator test that failed.

In one embodiment, the continuous random number generator test is not performed across tasks that do not all have the test enabled. That is, the new and old buffers are updated and the continuous random number generator test is performed only for XSTORE instructions executed when the CNT enable bit **342** is set. Consequently, a given task is guaranteed to never receive two consecutive eight-byte values that are equal. However, if two tasks are running and one sets the CNT enable bit **342** and the other does not, then RNG unit **136** may XSTORE eight bytes to one task, a task



switch occurs, and RNG unit 136 may XSTORE to the other task eight bytes equal to the previous eight bytes; however, the continuous random number generator test will not fail in this case.

RNG unit 136 also includes a string filter 224 coupled to the output of shift register 218. String filter 224 receives random bytes 298 from shift register 218 and selectively discards certain of the random bytes as described below, and outputs the non-discarded random bytes. String filter 224 ensures that no contiguous string of like bits, i.e., no contiguous string of zero bits or contiguous string of one bits, longer than a specified value is generated by RNG unit 136. The value is specified by a max\_cnt signal 258 received from CSR 226. The max\_cnt signal 258 conveys a value specified in string filter max\_cnt field 346 of FIG. 3 in CSR 226. In one embodiment, the default value of max\_cnt 346 is 26 bits. In one embodiment, the value of the string filter max\_cnt field 346 must be at least 8. If string filter 224 detects a contiguous string of like bits exceeding max\_cnt 258, then string filter 224 asserts a filter fail signal 256, which is stored in string filter fail bit 338 of FIG. 3 in CSR 226. String filter 224 is described in more detail below with respect to FIGS. 10 through 12.

RNG unit 136 also includes a second two-input mux 228. One of the inputs is coupled to the output of string filter 224, and the other input is coupled to the output of shift register 218. Mux 228 selects one of the inputs based on a filter enable signal 262 provided by CSR 226, which conveys the value stored in a string filter enable bit 334 of FIG. 3 of CSR 226.

RNG unit 136 also includes a one-input, two-output demultiplexer 232 whose input is coupled to the output of mux 228. A demultiplexer circuit includes a single data input and a plurality of data outputs. A demultiplexer also includes a control input. A demultiplexer selects one of the plurality of data outputs based on the control input and provides the data received on the data input to the selected output. Demux 232 selectively provides a random data byte received on its input to one of its outputs based on a fill\_select signal 264 provided by control logic 244.

RNG unit 136 also includes two data buffers, denoted buf0 242 and buf1 246, coupled to the outputs of demux 232. Buf0 242 and buf1 246 accumulate random data bytes to be stored to system memory by XSTORE instructions. In one embodiment, buf0 242 and buf1 246 each are capable of storing up to 15 bytes of random data. In one embodiment, buf0 242 and buf1 246 each are capable of storing up to 16 bytes of random data.

RNG unit 136 also includes a third two-input mux 236 whose inputs are coupled to the outputs of buf0 242 and buf1 246. Mux 236 selects one of the sets of random data bytes on its inputs based on a store\_select signal 266 provided by control logic 244 to output on a data bus 278.

RNG unit 136 also includes a TSPO flag register 274 coupled to control logic 244. TSPO flag register 274 stores a flag indicating whether a task switch by the operating system possibly occurred. Use of TSPO flag register 274 will be described below in more detail.

RNG unit 136 also includes a second two-output demux 215 coupled to control logic 244. The input of demux 215 is coupled to receive an increment signal 221 generated by control logic 244. Control logic 244 asserts increment signal 221 each time a random data byte is stored into buf0 242 or buf1 246. Demux 215 selectively provides increment signal 221 received on its input to one of its outputs based on fill\_select signal 264.

RNG unit 136 also includes a third two-input demux 217 coupled to control logic 244. The input of demux 217 is coupled to receive a clear signal 223 generated by control logic 244. Control logic 244 asserts clear signal 223 each time an XSTORE instruction is executed such that the valid random data bytes are removed from buf0 242 or buf1 246. Demux 217 selectively provides clear signal 223 received on its input to one of its outputs based on store\_select signal 266.

RNG unit 136 also includes two counters, denoted cntr0 211 and cntr1 213, coupled to demux 215 and demux 217. Cntr0 211 and cntr1 213 each have an increment, or count, input. The count inputs are coupled to the outputs of demux 215. Hence, when control logic 244 asserts increment signal 221, one of cntr0 211 and cntr1 213 specified by fill\_select signal 264 is incremented. Cntr0 211 and cntr1 213 also each have a clear input. The clear inputs are coupled to the outputs of demux 217. Hence, when control logic 244 asserts clear signal 223, one of cntr0 211 and cntr1 213 specified by store\_select signal 266 is cleared to zero.

RNG unit 136 also includes two comparators 225 coupled to the outputs of cntr0 211 and cntr1 213. Comparators 225 compare the counts output by cntr0 211 and cntr1 213 with the number of bytes cntr0 211 and cntr1 213 are capable of storing to determine whether cntr0 211 and cntr1 213 are full and generate a full0 signal 229 and full1 signal 227 to indicate the comparison results to control logic 244.

RNG unit 136 also includes a fourth two-input mux 219 whose inputs are coupled to the output of cntr0 211 and cntr1 213. Mux 219 selects one of the counts on its inputs based on store\_select signal 266 to output as an available byte count 234. The available byte count 234 is also provided to CSR 226.

RNG unit 136 also includes a register denoted RNG R5 238, or R5 238. R5 238 has one input coupled to the output of mux 236 to receive data bytes 278. R5 238 has another input coupled to the output of mux 219 to receive available byte count 234. The output of R5 238 is coupled to data bus 144 of FIG. 1. R5 238 holds the count and data for an XSTORE instruction. In one embodiment, the count is stored in the least significant byte of R5 238 and the valid data bytes are stored in increasingly significant byte locations contiguous to the count. In one embodiment, R5 238 is capable of storing one count byte plus the number of random data bytes capable of being stored by buf0 242 and buf1 246.

In one embodiment, RNG unit 136 includes four buffers rather than two. Each of the buffers is capable of storing up to eight bytes of random data. In this embodiment, demux 215, 217, and 232 comprise four-output demuxes; mux 219 and 236 comprise four-input muxes; comparators 225 comprise four comparators that generate four full outputs; and fill\_select signal 264 and store\_select signal 266 comprise two bits for selecting one of the four counters and buffers.

Referring now to FIG. 3, a block diagram illustrating various registers in microprocessor 100 of FIG. 1 related to RNG unit 136 of FIG. 1 according to the present invention is shown.

FIG. 3 shows CPUID register 204 of FIG. 2. CPUID register 204 includes an RNG present bit 302. RNG present bit 302 is a read-only feature-flags bit. If RNG present bit 302 is 1, then RNG unit 136 is present and enabled on microprocessor 100. If RNG present bit 302 is 0, then RNG unit 136 is not present, and the XLOAD and XSTORE instructions are invalid and if encountered by instruction translator 106 will cause an invalid instruction exception. Additionally, the bits in MSR 212 are undefined when read



## 13

and have no effect when written. RNG present bit 302 is a copy of RNG present bit 314 of MSR 212.

FIG. 3 also shows MSR 212 of FIG. 2. MSR 212 includes an RNG enable bit 312. RNG enable bit 312 is writable. Writing RNG enable bit 312 to a 1 enables RNG unit 136. Writing RNG enable bit 312 to a 0 disables RNG unit 136. If RNG enable bit 312 is 0, then the XLOAD and XSTORE instructions are invalid and if encountered by instruction translator 106 will cause an invalid instruction exception. Additionally, the bits in MSR 212 are undefined when read and have no effect when written. The value of RNG enable bit 312 immediately after reset is 0.

MSR 212 also includes a read-only RNG present bit 314. RNG present bit 314 indicates whether RNG unit 136 exists on microprocessor 100. If RNG present bit 314 is 0, then RNG unit 136 cannot be enabled by setting RNG enable bit 312, and the bits in MSR 212 are undefined when read and have no effect when written. Additionally, RNG present bit 314 is cleared if the RNG unit 136 self-test fails, as described above with respect to FIG. 2.

MSR 212 also includes a read-only statistical self-test enabled bit 316. Self-test enabled bit 316 indicates whether the reset self-test described above with respect to FIG. 2 is currently enabled. If self-test enabled bit 316 is 0, then no self-test is performed after reset. If self-test enabled bit 316 is 1, then a self-test is performed after reset. In one embodiment, a self-test is performed after a warm reset as well as a power-up reset of microprocessor 100.

MSR 212 also includes a read-only statistical self-test failed bit 318. Self-test failed bit 318 indicates whether the last reset self-test described above with respect to FIG. 2 failed or not. In one embodiment, if self-test failed bit 318 is 1, then RNG unit 136 cannot be enabled.

MSR 212 also includes writable DC bias bits 322. In one embodiment, DC bias bits 322 comprise three bits. DC bias bits 322 control the DC bias supplied to random bit generator 0 206, which affects the speed and possible randomness of random bit generator 0 206. In one embodiment, if the statistical self-test is performed at reset, then the self-test unit 202 determines a correct or best value for DC bias bits 322 and sets them to the value. The value of DC bias bits 322 immediately after a reset is 000.

MSR 212 also includes writable raw bits bit 324. If the raw bits bit 324 is set to 0, then whitener 216 of FIG. 2 performs its whitening function described above with respect to FIG. 2 and delivers whitened bits to shift register 218. If the raw bits bit 324 is set to 1, then whitener 216 does not perform its whitening function and instead delivers the raw bits from mux 214 to shift register 218. The value of the raw bits bit 324 immediately after a reset is 0.

FIG. 3 also shows CSR 226 of FIG. 2. In one embodiment, CSR 226 is a 128-bit register. CSR 226 includes a read-only available byte count field 332. The available byte count field 332 specifies how many bytes of random data are currently available in buf0 242 or buf1 246 as selected by store\_select signal 266 for storing via an XSTORE instruction. Software can read the available byte count field 332, if desired, in order to determine the number of random data bytes currently available for storing via an XSTORE instruction. Because RNG unit 136 synchronously accumulates bytes into buf0 242 and buf1 246, the actual number of bytes available to be stored by an XSTORE may be greater at the time the XSTORE is executed than the available byte count 332 previously read by an XLOAD. The value of the available byte count field 332 immediately after RNG unit 136 is enabled is 0.

## 14

CSR 226 also includes a writable string filter enable bit 334. If string filter enable bit 334 is 1, then string filter 224 is enabled; otherwise string filter 224 is disabled. The operation of string filter 224 is described below in more detail with respect to FIGS. 10 through 12. The value of the string filter enable bit 334 immediately after RNG unit 136 is enabled is 0.

CSR 226 also includes a writable gen select bit 336. If gen select bit 336 is set to 0, then random bit generator 0 206 is selected via mux 214 of FIG. 2 to provide the random bit stream for accumulation; otherwise, random bit generator 1 208 is selected. The value of the gen select bit 336 immediately after RNG unit 136 is enabled is 0.

CSR 226 also includes a string filter fail bit 338. String filter fail bit 338 is set to 1 to indicate that string filter 224 detected a contiguous string of like bits longer than a value specified in string filter max\_cnt field 346 as described above with respect to FIGS. 2, and 10 through 12. Only RNG unit 136 can set the string filter fail bit 338 to 1. However, software may clear string filter fail bit 338 by writing a 0 to it. In one embodiment, filter fail bit 338 is set to 1 by a pulse on filter fail signal 256 and remains set to 1 until software clears it. The value of the string filter fail bit 338 immediately after RNG unit 136 is enabled is 0.

CSR 226 also includes a writable CNT enable bit 342. If the CNT enable bit 342 is 1, then CNT unit 222 performs its continuous random number generator tests as described above with respect to FIG. 2. The value of the CNT enable bit 342 immediately after RNG unit 136 is enabled is 0.

CSR 226 also includes a read-only CNT failed bit 344. RNG unit 136 sets CNT failed bit 344 to 1 if the CNT enable bit 342 is 1 and the continuous random number generator tests fail. In one embodiment, an XSTORE instruction executed while both the CNT enable bit 342 and the CNT failed bit 344 are 1 results in the XSTORE storing an available byte count of 0 and no data bytes to system memory. Hence, if a task sets the CNT enable bit 342 and a failure occurs while the task is executing, RNG unit 136 is effectively disabled for the task. However, RNG unit 136 is not disabled for other tasks not setting the CNT enable bit 342. The value of the CNT failed bit 344 immediately after RNG unit 136 is enabled is 0.

CSR 226 also includes a writable string filter max\_cnt field 346. Software writes the string filter max\_cnt field 346 to specify the maximum number of allowable contiguous like bits tolerable, as described with respect to FIGS. 10 through 12 below. In one embodiment, the string filter max\_cnt field 346 comprises 5 bits. In one embodiment, the default value of string filter max\_cnt field 346 is 26.

In one embodiment, various ones of the fields of MSR 212 are included in CSR 226 rather than MSR 212. Hence, the values in MSR 212 are saved and restored with CSR 226 to accommodate multitasking operation as described herein, and particularly with respect to FIGS. 4 through 9.

FIG. 3 also shows RNG R5 register 238 of FIG. 2. R5 238 comprises two fields: an available byte count field 362 and another field 364 for storing random data bytes, as described above. In one embodiment, the valid random data bytes are right adjusted next to the available byte count field 362.

FIG. 3 also shows SSE registers 352. SSE registers 352 comprise eight 128-bit registers denoted XMM0 through XMM7. XMM0 is designated XMM0 372, XMM3 is designated 376, and XMM5 is designated XMM5 374 in FIG. 3. In one embodiment, SSE registers 352 are substantially similar to SSE registers comprised in a Pentium III or IV as described on page 10-4 of IA-32® Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture,



2002, which is hereby incorporated by reference. RNG CSR 226 shadows XMM0 372 and RNG R5 238 shadows XMM5 374 as described below.

In one embodiment, microprocessor 100 includes various fuses that may be temporarily or permanently set during the manufacturing process of microprocessor 100 to select values of various bits in the CSR 226 and MSR 212 at reset time in order to override the reset values described above.

Referring now to FIG. 4, a flowchart illustrating operation of microprocessor 100 of FIG. 1 when executing an instruction that loads a value into XMM0 register 372 of FIG. 3 according to the present invention is shown. An instruction that loads XMM0 372 is an instruction executed by the microprocessor that loads the XMM0 register 372 with a value from system memory, such as a MOVAPS instruction. The MOVAPS instruction moves data from system memory to a specified XMM register, or vice versa, and is described on pages 3-443 through 3-444 of the IA-320 Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference, 2001, which are hereby incorporated by reference. Examples of other instructions that load XMM0 372 from system memory are MOVAPD and MOVDQA. Because XMM0 372 is a register saved to memory and restored from memory by the operating system on a task switch, when a task switch occurs the operating system will execute an instruction such as a MOVAPS instruction to restore the switched-to task's previous value of XMM0 372 from memory. Flow begins at block 402.

At block 402, microprocessor 100 executes an instruction such as the MOVAPS instruction by fetching the value from the location in system memory specified by the instruction and loads the value into XMM0 372. Hence, any time XMM0 372 is loaded from memory, it is possible that a task switch has occurred. Flow proceeds to block 404.

At block 404, instruction translator 106 notifies RNG unit 136 that a MOVAPS instruction, or similar instruction that loads XMM0 372 from memory, has been translated. Once the value has been loaded into XMM0 372, control logic 244 of RNG unit 136 sets the TSPO flag 274 to indicate that a task switch possibly occurred. Flow ends at block 404.

Referring now to FIG. 5, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XLOAD instruction according to the present invention is shown. The XLOAD instruction is the means by which software loads a value into the CSR 226 of FIG. 2 to specify the control values under which RNG unit 136 will operate. A new instruction beyond the Pentium III or IV instruction set is required to load CSR 226 since CSR 226 does not exist in a Pentium III or IV. Advantageously, the XLOAD instruction also loads the control values into XMM0 372 to facilitate multitasking operation with RNG unit 136 as described herein.

FIG. 5 shows the format of an XLOAD instruction specifying XMM0 372, which is:

XLOAD XMM0, memaddr

where memaddr specifies a memory address in system memory 502. The XLOAD instruction operates like the MOVAPS instruction except that CSR 226 is also loaded with the value from memory in addition to XMM0 372. In one embodiment, XLOAD moves 16 bytes of data 504 from memaddr into CSR 226 and also into XMM0 372, as shown. In one embodiment, the opcode value for the XLOAD instruction is 0x0F 0x5A followed by the standard mod R/M register and address format bytes specified by x86 instructions. In another embodiment, the opcode value for the XLOAD instruction is 0x0F 0xA6 0xC0. If an XLOAD

instruction specifies one of the SSE registers 352 other than XMM0 372, then the specified SSE register 352 is loaded; however, CSR 226 is not loaded.

Referring now to FIG. 6, a flowchart illustrating operation of microprocessor 100 of FIG. 1 when executing an XLOAD instruction to XMM0 register 372 of FIG. 3 according to the present invention is shown. Flow begins at block 602.

At block 602, microprocessor 100 loads CSR 226 of FIG. 2 and XMM0 372 of FIG. 3 with the value in system memory 502 at the memory address specified by the XLOAD instruction as shown in FIG. 5. Flow proceeds to block 604.

At block 604, RNG unit 136 discards the contents of buf0 242 and buf1 246 in response to the loading of CSR 226 since the random data bytes accumulated in buf0 242 and buf1 246 may not have been generated with the control values in CSR 226 required by the new task that is now loading CSR 226. Flow proceeds to block 606.

At block 606, RNG unit 136 clears the available byte count to 0 in cntr0 211 and cntr1 213 since the random data bytes in buf0 242 and buf1 246 were discarded at block 604. Flow proceeds to block 608.

At block 608, RNG unit 136 restarts the random number accumulation. That is, the random bit generator 206 or 208 selected by gen select signal 252 generates random bits based on DC bias signal 296 in the case of random bit generator 0 206; whitener 216 selectively whitens the bits based on the raw bits signal 254; CNT unit 222 selectively performs continuous random number generator tests based on CNT enable signal 284; string filter 224 selectively filters the bytes accumulated by shift register 218 based on filter enable signal 262 and max\_cnt signal 258; buf0 242 and buf1 246 accumulate the random data bytes based on fill\_select signal 264; and cntr0 211 and cntr1 213 count the bytes accumulated in buf0 242 and buf1 246 based on fill\_select signal 264. Flow proceeds to block 612.

At block 612, control logic 244 clears TSPO flag 274 since CSR 226 has been updated to the control values desired by the current task. Flow ends at block 612.

Referring now to FIG. 7, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction according to the present invention is shown. The XSTORE instruction is the means by which software stores the count of available random data bytes and the random data bytes themselves from R5 238 to system memory. A new instruction beyond the Pentium III or IV instruction set is required to store RNG R5 238 since it does not exist in a Pentium III or IV. Advantageously, the XSTORE instruction atomically writes the count and data bytes to memory to facilitate multitasking operation with RNG unit 136 as described herein. That is, the XSTORE instruction is not interruptible. Hence, when a task executes an XSTORE instruction, another task may not interrupt the XSTORE instruction to modify the available byte count or random data bytes that will be written to system memory by the XSTORE instruction. Hence, the XSTORE instruction advantageously inherently facilitates multitasking with respect to supplying a variable number of random data bytes by atomically writing both the data and count.

FIG. 7 shows the format of an XSTORE instruction, which is:

XSTORE memaddr, XMM5

Memaddr specifies a memory address in system memory 502. The XSTORE instruction operates like the MOVAPS instruction except that the specified XMM register is not stored to system memory; instead R5 238 is stored to system



memory if XMM5 374 is specified. That is, R5 238 shadows XMM5 374. XSTORE moves the count specifying the available valid random data bytes 362 of FIG. 3 from R5 238 to a location 702 at memaddr in system memory 502, as shown. Additionally, XSTORE moves the valid random bytes of data 364 specified by the count 362 to a location 704 in system memory 502 immediately adjacent to the available byte count 702, as shown.

In one embodiment, the opcode value for the XSTORE instruction is 0x0F 0x5B followed by the standard mod R/M register and address format bytes specified by x86 instructions. In another embodiment, the opcode value for the XSTORE instruction is 0x0F 0xA0 0xC0. In one embodiment, the XSTORE instruction requires that the ES:EDI registers in register file 108 specify memaddr, i.e., point to the starting memory address where the count and random data bytes are to be stored. In one embodiment, the XSTORE does not allow segment overriding. If an XSTORE instruction specifies one of the SSE registers 352 other than XMM5 374, then the results are undefined.

In one embodiment, the number of random data bytes 704 that microprocessor 100 stores to system memory equals the available byte count 702 also written to system memory.

In another embodiment, the number of random data bytes 704 that microprocessor 100 stores to system memory is equal to one less than the size in bytes of RNG R5 238. That is, if RNG R5 238 is a 16-byte register capable of holding up to 15 random data bytes 364 and one byte of available byte count 362, then microprocessor 100 stores 16 bytes to system memory 502: 15 bytes of random data to the random data bytes 704 location and one count byte to the available byte count 702 location in system memory 502. However, some of the 15 bytes written to system memory 502 may not be valid. In one embodiment, the number of bytes written to memory is always a power of 2. Only the first N bytes are valid, where N is the available byte count 702.

In this embodiment, RNG unit 136 clears the buffer, i.e., buf0 242 or buf1 246 of FIG. 2, implicated by an XSTORE operation. By clearing the buffer, microprocessor 100 improves security by avoiding the problem of tasks being able to view one another's random data. For example, assume a first task performs a first XSTORE that stores 15 bytes of random data from buf0 242 to system memory and a second XSTORE that stores 15 bytes of random data from buf1 246 to system memory; then the operating system switches to a second task which immediately executes an XSTORE before RNG unit 136 has accumulated any more bytes of random data into buf0 242. If the RNG unit 136 did not clear buf0 242 after the first XSTORE, then the random data received by the first task would also be stored to the second task's memory location, thereby enabling the second task to view the first task's random data.

In one embodiment, the XSTORE instruction specifies a maximum number of random data bytes to store to system memory. In one embodiment, the maximum number of bytes is specified in one of the general-purpose registers of register file 108, such as ECX. In this embodiment, if more bytes are available in buf0 242 or buf1 246 selected by store\_select 266 than the maximum number specified in ECX, then microprocessor 100 only stores the maximum number of bytes specified in ECX; otherwise, the XSTORE instruction stores the number of valid bytes available. In either case, the XSTORE instruction stores into the available byte count location 702 the number of valid random data bytes stored to the data byte location 704 in system memory 502.

In one embodiment, the XSTORE instruction specifies a required number of random data bytes to store to system

memory. In this embodiment, the required number of bytes is specified in one of the general-purpose registers of register file 108, such as ECX. In this embodiment, the XSTORE instruction is prefixed with an x86 REP prefix. In this embodiment, the REP XSTORE instruction is not atomic. That is, the REP XSTORE is interruptible since the number of random bytes required may be large. However, since the number of random data bytes stored is not variable, i.e., the software knows the number of random data bytes that are to be stored to memory, it is not necessary that the instruction be atomic.

Referring now to FIG. 8, a flowchart illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction from XMM5 register of FIG. 3 according to the present invention is shown. Flow begins at block 802.

At block 802 interrupt unit 146 of FIG. 1 disables interrupts in response to instruction translator 106 of FIG. 1 notifying interrupt unit 146 that an XSTORE instruction was translated. Flow proceeds to decision block 804.

At decision block 804, control logic 244 of FIG. 2 examines TSPO flag 274 to determine whether the flag is set. If so flow proceeds to block 806. Otherwise, flow proceeds to block 816.

At block 806, RNG unit 136 copies the contents of XMM0 372 to CSR 226 and clears the TSPO flag 274. Since TSPO flag 274 indicates that a task switch may have possibly occurred since the last XSTORE or XLOAD, as indicated by a load from system memory of XMM0 372 according to step 402 of FIG. 4, the possibility exists that CSR 226 does not have the correct control values for the task currently executing the XSTORE instruction. Hence, the XSTORE instruction must update the CSR 226 with the correct control values. The correct values are stored in XMM0 372, since the correct control values were originally loaded into XMM0 372 and also into CSR 226 by an XLOAD executed when the task initialized and were restored to XMM0 372 by the operating system when it switched back to the current task. Flow proceeds to block 808.

At block 808, RNG unit 136 discards the contents of buf0 242 and buf1 246 in response to the loading of CSR 226 since the random data bytes accumulated in buf0 242 and buf1 246 may not have been generated with the control values in CSR 226 required by the new task for which new control values were copied into CSR 226 in block 806. Flow proceeds to block 812.

At block 812, RNG unit 136 clears the available byte count to 0 in cntr0 211 and cntr1 213 since the random data bytes in buf0 242 and buf1 246 were discarded at block 808. Flow proceeds to block 814.

At block 814, RNG unit 136 restarts the random number accumulation, as described above with respect to block 608 of FIG. 6. Flow proceeds to block 816.

At block 816, RNG unit 136 atomically stores R5 238 to system memory 502 at the memory address specified by the XSTORE instruction, which holds the value of cntr0 211 or cntr1 213 specified by store\_select signal 266 along with the valid random data bytes from buf0 242 or buf1 246 specified by store\_select signal 266, as shown in FIG. 7. Flow proceeds to block 818.

At block 818, control logic 244 asserts clear signal 223 to clear cntr0 211 or cntr1 213 specified by store\_select signal 266 since the valid random data bytes have been consumed by the store to memory at block 816. Flow proceeds to block 822.



At block 822, control logic 244 updates store\_select signal 266. That is, if store\_select signal 266 was 0, then control logic 244 updates store\_select signal 266 to 1. Conversely, if store\_select signal 266 was 1, then control logic 244 updates store\_select signal 266 to 0. Flow proceeds to block 824.

At block 824, interrupt unit 146 enables interrupts since the XSTORE instruction has completed execution. Flow ends at block 824.

Referring now to FIG. 9, a flowchart illustrating an example of multi-tasking operation of microprocessor 100 of FIG. 1 with respect to random number generation according to the present invention is shown. FIG. 9 comprises two drawing pages denoted FIG. 9A and FIG. 9B. The flowchart of FIG. 9 illustrates a typical scenario in which two tasks each initialize RNG unit 136 and execute XSTORE instructions to store random data bytes to memory. FIG. 9 illustrates how the present invention advantageously supports multitasking between the two tasks, task A and task B, even though the operating system does not include support for saving and restoring the state of RNG unit 136, namely CSR 226. Flow begins at block 902.

At block 902, a reset occurs, which causes control logic 244 to clear TSPO flag 274. Flow proceeds to block 904.

At block 904, the operating system starts up task A, and task A's initialization code executes an XLOAD instruction to XMM0 372 to initialize CSR 226 and XMM0 372 with the desired control values denoted value A. Flow proceeds to block 906.

At block 906, RNG unit 136 discards the contents of buf0 242 and buf1 246, clears cntr0 211 and cntr1 213, restarts random number generation and accumulation, and clears TSPO flag 274 in response to the XLOAD, according to blocks 604, 606, 608, and 612 of FIG. 6. Flow proceeds to block 908.

At block 908, task A executes an XSTORE instruction to store random data generated based on control value A loaded into CSR 226 at block 904. Flow proceeds to block 912.

At block 912, to execute the XSTORE of the previous block, RNG unit 136 atomically stores the count and data to system memory accumulated since the restart at block 906, as shown in FIG. 7 and described in FIG. 8. Flow proceeds to block 914.

At block 914, the operating system performs a task switch from task A to task B. Among other things, the operating system stores the value of XMM0 372, which contains control value A, to system memory to save the state of task A. However, the operating system does not store CSR 226 to memory to save its state because the operating system does not know about CSR 226. Flow proceeds to block 916.

At block 916, RNG unit 136 sets TSPO flag 274 in response to the load of XMM0 372 at block 914, according to step 404 of FIG. 4. Flow proceeds to block 918.

At block 918, the operating system starts up task B, and task B's initialization code executes an XLOAD instruction to XMM0 372 to initialize CSR 226 and XMM0 372 with the desired control values denoted value B. Flow proceeds to block 922.

At block 922, RNG unit 136 discards the contents of buf0 242 and buf1 246, clears cntr0 211 and cntr1 213, restarts random number generation and accumulation, and clears TSPO flag 274 in response to the XLOAD, according to blocks 604, 606, 608, 612 of FIG. 6. Flow proceeds to block 924.

At block 924, task B executes an XSTORE instruction to store random data generated based on control value B loaded into CSR 226 at block 918. Flow proceeds to block 924.

At block 926, to execute the XSTORE of the previous block, RNG unit 136 atomically stores the count and data to system memory accumulated since the restart at block 922, as shown in FIG. 7 and described in FIG. 8. Flow proceeds to block 928.

At block 928, the operating system performs a task switch from task B to task A. Among other things, the operating system stores the value of XMM0 372, which contains control value B, to system memory to save the state of task B. However, the operating system does not store CSR 226 to memory to save its state because the operating system does not know about CSR 226. Additionally, the operating system restores the state of task A, which includes loading into XMM0 372 value A from system memory previously saved at block 914. Flow proceeds to block 932.

At block 932, RNG unit 136 sets TSPO flag 274 in response to the load of XMM0 372 at block 928, according to step 404 of FIG. 4. Flow proceeds to block 934.

At block 934, task A executes an XSTORE instruction to store random data generated based on control value A loaded into CSR 226 at block 904. However, value A was overwritten in CSR 226 at block 918. Hence, the random data bytes currently accumulated in buf0 242 and buf1 246 were not generated based on value A, but instead were generated based on value B. Flow proceeds to block 936.

At block 936, RNG unit 136 determines that TSPO flag 274 is set according to block 804 of FIG. 8, and consequently copies the contents of XMM0 372 to CSR 226, thereby restoring value A to CSR 226, according to block 806 of FIG. 8. In addition, RNG unit 136 clears TSPO flag 274, according to block 806, since CSR 226 has been restored. Flow proceeds to block 938.

At block 938, RNG unit 136 discards the contents of buf0 242 and buf1 246, clears cntr0 211 and cntr1 213, and restarts random number generation and accumulation, in response to the copy into CSR 226 at block 936, according to blocks 808, 812, and 814 of FIG. 8. Flow proceeds to block 942.

At block 942, to execute the XSTORE of block 934, RNG unit 136 atomically stores the count and data to system memory accumulated since the restart at the previous block, as shown in FIG. 7 and described in FIG. 8. In this case, the count is 0 and no valid random data bytes are stored to system memory since cntr0 211 and cntr1 213 were cleared and the contents of buf0 242 and buf1 246 were discarded at the previous block. Flow proceeds to block 944.

At block 944, task A executes an XSTORE instruction to store random data generated based on control value A loaded into CSR 226 at block 904, which was restored to value A at block 936. Flow proceeds to block 946.

At block 946, to execute the XSTORE of the previous block, RNG unit 136 atomically stores the count and data to system memory accumulated since the restart at block 938, as shown in FIG. 7 and described in FIG. 8. Flow proceeds to block 948.

At block 948, task A executes an XSTORE instruction to store random data generated based on control value A loaded into CSR 226 at block 904, which was restored to value A at block 936. Flow proceeds to block 952.

At block 952, to execute the XSTORE of the previous block, RNG unit 136 atomically stores the count and data to system memory accumulated since the restart at block 938, less the bytes stored by the last XSTORE, which was at block 946, as shown in FIG. 7 and described in FIG. 8. Flow ends at block 952.



Referring now to FIG. 10, a block diagram illustrating string filter 224 of RNG unit 136 of FIG. 2 of microprocessor 100 of FIG. 1 according to the present invention is shown.

For the purposes of the present disclosure, leading one bits are defined as the contiguous one bits at the beginning of a byte. A byte may contain between zero and eight, inclusive, leading one bits. For example, the byte 00011111 has five leading one bits; the byte 11111110 has zero leading one bits; and the byte 11111111 has eight leading one bits.

For the purposes of the present disclosure, leading zero bits are defined as the contiguous zero bits at the beginning of a byte. A byte may contain between zero and eight, inclusive, leading zero bits. For example, the byte 11100000 has five leading zero bits; the byte 00000001 has zero leading zero bits; and the byte 00000000 has eight leading zero bits.

For the purposes of the present disclosure, trailing one bits are defined as the contiguous one bits at the end of a byte; however a byte that is all ones is defined as having no trailing one bits. A byte may contain between zero and seven, inclusive, trailing one bits. For example, the byte 11110000 has four trailing one bits; the byte 11111110 has seven trailing one bits; the byte 01111111 has zero trailing one bits; and the byte 11111111 has zero trailing one bits.

For the purposes of the present disclosure, trailing zero bits are defined as the contiguous zero bits at the end of a byte; however a byte that is all zeros is defined as having no trailing zero bits. A byte may contain between zero and seven, inclusive, trailing zero bits. For example, the byte 00001111 has four trailing zero bits; the byte 00000001 has seven trailing zero bits; the byte 10000000 has zero trailing zero bits; and the byte 00000000 has zero trailing zero bits.

String filter 224 includes compare logic 1002. Compare logic 1002 receives random data byte 298 from shift register 218 of FIG. 2. Compare logic 1002 examines the bits in the random data byte 298 and generates various signals used to detect contiguous strings of ones and zeros as now described.

Compare logic 1002 generates a num\_leading\_ones signal 1022A that specifies the number of leading one bits in random data byte 298.

Compare logic 1002 generates a num\_trailing\_ones signal 1028A that specifies the number of trailing one bits in random data byte 298.

Compare logic 1002 also generates an all\_ones signal 1048A that is true if random data byte 298 contains all one bits

Compare logic 1002 also generates a leading\_ones signal 1036A that is true if random data byte 298 contains leading one bits.

Compare logic 1002 also generates a trailing\_ones signal 1038A that is true if random data byte 298 contains trailing one bits.

String filter 224 also includes a first counter 1016A for storing the current count of contiguous one bits. In one embodiment, counter 1016A comprises a six-bit register. The output of counter 1016A is a ones\_cnt signal 1024A.

String filter 224 also includes a first adder 1012A that adds num\_leading\_ones 1022A and ones\_cnt signal 1024A to produce a new ones\_cnt signal 1026A.

String filter also includes a first four-input mux 1014A. Mux 1014A receives on its inputs ones\_cnt signal 1024A, new\_ones\_cnt signal 1026A, num\_trailing\_ones signal 1028A, and a hard coded value of zero 1032A. Mux 1014A selects one of the inputs for outputting to counter 1016A based on a one\_select signal 1042A.

Compare logic 1002 generates a num\_leading\_zeros signal 1022B that specifies the number of leading zero bits in random data byte 298.

Compare logic 1002 generates a num\_trailing\_zeros signal 1028B that specifies the number of trailing zero bits in random data byte 298.

Compare logic 1002 also generates an all\_zeros signal 1048B that is true if random data byte 298 contains all zero bits.

Compare logic 1002 also generates a leading\_zeros signal 1036B that is true if random data byte 298 contains leading zero bits.

Compare logic 1002 also generates a trailing\_zeros signal 1038B that is true if random data byte 298 contains trailing zero bits.

String filter 224 also includes a second counter 1016B for storing the current count of contiguous zero bits. In one embodiment, counter 1016B comprises a six-bit register. The output of counter 1016B is a zeros\_cnt signal 1024B.

String filter 224 also includes a second adder 1012B that adds num\_leading\_zeros 1022B and zeros\_cnt signal 1024B to produce a new zeros\_cnt signal 1026B.

String filter also includes a second four-input mux 1014B. Mux 1014B receives on its inputs zeros\_cnt signal 1024B, new\_zeros\_cnt signal 1026B, num\_trailing\_zeros signal 1028B, and a hard-coded value of zero 1032B. Mux 1014B selects one of the inputs for outputting to counter 1016B based on a zero\_select signal 1042B.

String filter 224 also includes a first comparator 1046A that compares new\_ones\_cnt signal 1026A with max\_cnt signal 258 of FIG. 2. If new\_ones\_cnt signal 1026A is greater than max\_cnt signal 258, then comparator 1046A generates a true value on ones\_exceeded signal 1034A; otherwise, comparator 1046A generates a false value on ones\_exceeded signal 1034A.

String filter 224 also includes a second comparator 1046B that compares new\_zeros\_cnt signal 1026B with max\_cnt signal 258 of FIG. 2. If new\_zeros\_cnt signal 1026B is greater than max\_cnt signal 258, then comparator 1046B generates a true value on zeros\_exceeded signal 1034B; otherwise, comparator 1046B generates a false value on zeros\_exceeded signal 1034B.

String filter 224 also includes a two-input OR gate 1004 whose inputs are coupled to the outputs of comparator 1046A and comparator 1046B. OR gate 1004 receives ones\_exceeded signal 1034A and zeros\_exceeded signal 1034B on its inputs. OR gate 1004 generates a max\_cnt\_exceeded signal 1044, which is provided as an input to select logic 1006.

String filter 224 also includes a two-input AND gate 1008 coupled to OR gate 1004. AND gate 1008 receives cnt\_exceeded signal 1044 from OR gate 1004 on one input filter enable signal 262 of FIG. 2 on its other t. The output of AND gate 1008 is filter fail signal of FIG. 2.

String filter 224 also includes select logic 1006 led to receive all\_ones signal 1048A, leading\_ones al 1036A, trailing\_ones signal 1038A, max\_cnt exceeded al 1044, leading\_zeros signal 1036B, trailing\_zeros al 1038B, and all\_zeros signal 1048B. Select logic generates one\_select signal 1042A and zero\_select al 1042B according to the following code.

```
retain_counts=max_cnt exceeded & filter enable;
increment_zeros all_zeros & (! retain_counts);
load_zeros trailing_zeros & (! retain_counts) & (! increment_zeros);
clear_zeros (!(retain_counts) & (! increment_zeros) & (! load_zeros);
```



```

increment_ones=all_ones & (! retain_counts);
load_ones trailing_ones & (! retain_counts) & (! incremen-
t_ones);
clear_ones=(! retain_counts) & (! increment_ones) & (!
load_ones);

```

---

```

if (retain_counts) {
    zero_select = 3; // select zeros_cnt input
} else if (increment_zeros) {
    zero_select = 2; // select new_zeros_cnt input
} else if (load_zeros) {
    zero_select = 1; // select num_trailing_zeros input
} else if (clear_zeros) {
    zero_select = 0; // select hard-coded 0 input
}
if (retain_counts) {
    one_select = 3; // select ones_cnt input
} else if (increment_ones) {
    one_select = 2; // select new_ones_cnt input
} else if (load_ones) {
    one_select = 1; // select num_trailing_ones input
} else if (clear_ones) {
    one_select = 0; // select hard-coded 0 input
}

```

---

Referring now to FIG. 11, a flowchart illustrating operation of string filter 224 of FIG. 10 according to the present invention is shown. Flow begins at block 1102.

At block 1102, counters 1016A and 1016B are initialized to a zero value. Flow proceeds to block 1104.

At block 1104, RNG unit 136 of FIG. 1 generates a byte of random data on random byte signal 298 of FIG. 2 and compare logic 1002 generates its signals based on examination of random data byte 298. Flow proceeds to block 1106.

At block 1106, adder 1012A adds num\_leading\_ones 1022A and ones\_cnt 1024A to produce new\_ones\_cnt 1026A and adder 1012B adds num\_leading\_zeros 1022B and zeros\_cnt 1024B to produce new\_zeros\_cnt 1026B. Flow proceeds to decision block 1112.

At block 1112, select logic 1006 examines max\_cnt\_exceeded 1044 to determine whether the number of contiguous zeros or ones has exceeded max\_cnt 298. If so, flow proceeds to decisions block 1114. Otherwise, flow proceeds to decision block 1124.

At decision block 1114, AND gate 1008 examines filter enable 262 signal to determine whether string filter 224 is enabled. If so, AND gate 1008 generates a true value on filter fail signal 256 of FIG. 2. Flow proceeds to block 1118.

At block 1118, in response to filter fail signal 256 being true, control logic 244 does not assert the increment signal 221 of FIG. 2 and does not cause random byte 298 to be loaded into buf0 242 or buf1 246, even though shift register 218 has generated a true value on byte\_generated signal 282. Thus, RNG unit 136 discards random byte 298 since random byte 298 has caused the number of contiguous ones or zeros to exceed max\_cnt 258. Flow proceeds to block 1122.

At block 1122, select logic 1006 generates a value of 3 on one\_select signal 1042A and on zero\_select signal 1042B in order to cause muxes 1014A and 1014B, respectively, to retain the current ones\_cnt 1024A and zeros\_cnt 1024B, respectively. Flow returns to block 1104.

At decision block 1124, select logic 1006 examines all\_zeros signal 1048B to determine whether random data byte 298 contains all zeros. If so, flow proceeds to block 1126. Otherwise, flow proceeds to decision block 1128.

At block 1126, select logic 1006 generates a value of 2 on zero\_select signal 1042B to cause mux 1014B to select

new\_zeros\_cnt 1026B and generates a value of 0 on one\_select signal 1042A to cause mux 1014A to select hard-coded 0 input 1032A. Flow proceeds to block 1148.

At decision block 1128, select logic 1006 examines trailing\_zeros signal 1038B to determine whether random data byte 298 contains any trailing zeros. If so, flow proceeds to block 1132. Otherwise, flow proceeds to block 1134.

At block 1132, select logic 1006 generates a value of 1 on zero\_select signal 1042B to cause mux 1014B to select num\_trailing\_zeros 1028B and generates a value of 0 on one\_select signal 1042A to cause mux 1014A to select hard-coded 0 input 1032A. Flow proceeds to block 1148.

At block 1134, select logic 1006 generates a value of 0 on zero\_select signal 1042B to cause mux 1014B to select hard-coded 0 input 1032B. Flow proceeds to decision block 1136.

At decision block 1136, select logic 1006 examines all\_ones signal 1048A to determine whether random data byte 298 contains all ones. If so, flow proceeds to block 1138. Otherwise, flow proceeds to decision block 1142.

At block 1138, select logic 1006 generates a value of 2 on one\_select signal 1042A to cause mux 1014A to select new\_ones\_cnt 1026A. Flow proceeds to block 1148.

At decision block 1142, select logic 1006 examines trailing\_ones signal 1038A to determine whether random data byte 298 contains any trailing ones. If so, flow proceeds to block 1144. Otherwise, flow proceeds to block 1146.

At block 1144, select logic 1006 generates a value of 1 on one\_select signal 1042A to cause mux 1014A to select num\_trailing\_ones 1028A. Flow proceeds to block 1148.

At block 1146, select logic 1006 generates a value of 0 on one\_select signal 1042A to cause mux 1014A to select hard-coded 0 input 1032A. Flow proceeds to block 1148.

At block 1148, control logic 244 causes random data byte 298 to be loaded into buf0 242 or buf1 246 selected by fill\_select signal 264 and asserts increment signal 221 to increment cntr0 211 or cntr1 213 selected by fill\_select signal 264. Flow returns to block 1104.

Referring now to FIG. 12, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention is shown. The XSTORE instruction of FIG. 12 is similar to the XSTORE instruction of FIG. 7, however in the alternate embodiment, the count of valid random data bytes is loaded into one of the general purpose registers in register file 108, such as the EAX 1202 register, rather than being stored to system memory. Advantageously, like the XSTORE instruction of FIG. 7, the XSTORE instruction of FIG. 12 atomically loads the count into EAX along with storing the random data bytes to memory to facilitate multitasking operation with RNG unit 136. That is, the XSTORE instruction of FIG. 12 is also not interruptible.

Referring now to FIG. 13, a flowchart illustrating multi-buffering operation of RNG unit 136 of FIG. 2 according to the present invention is shown. Flow begins at block 1302.

At block 1302, reset signal 248 is asserted. Flow proceeds to block 1304.

At block 1304, control logic 244 of FIG. 2 initializes fill\_select signal 264 and store\_select signal 266 to 0, and clears cntr0 211 and cntr1 213 in response to the reset at block 1302. Flow proceeds to decision block 1306.

At decision block 1306, control logic 244 determines whether an XSTORE instruction is being executed by examining xstore signal 268. If so, flow proceeds to decision block 1308. Otherwise, flow proceeds to decision block 1322.



## 25

At decision block 1308, control logic 244 determines whether random bit generator 0 206 or random bit generator 1 208 selected by gen select signal 252 is powered off. If so, flow proceeds to block 1312. Otherwise, flow proceeds to block 1314.

At block 1312, control logic 244 powers up the selected random bit generator via power\_cntrl signal 231. Flow proceeds to block 1314.

At block 1314, microprocessor 100 atomically stores to system memory the value in cntr0 211 or cntr1 213 selected by store\_select signal 266 and the valid data bytes in buf0 242 or buf1 246 selected by store\_select signal 266, according to block 816 of FIG. 8 and as shown in FIG. 7. Flow proceeds to block 1316.

At block 1316, control logic 244 asserts clear signal 223 to clear cntr0 211 or cntr1 213 selected by store\_select signal 266. Flow proceeds to block 1318.

At block 1318, control logic 244 updates store\_select signal 266 to select the other buffer and counter. In embodiments in which RNG unit 136 includes more than two buffers, store\_select signal 266 comprises more than one bit, and updating store\_select signal 266 comprises incrementing store\_select signal 266 and wrapping around back to zero when incrementing past the number of buffers. Flow proceeds to decision block 1322.

At decision block 1322, control logic 244 determines whether a good random data byte was generated by examining byte\_generated signal 282 to see if it is true and examining filter fail signal 256 to see if it is false. If so, flow proceeds to block 1324. Otherwise, flow returns to decision block 1306.

At block 1324, control logic 244 loads the good random data byte into buf0 242 or buf1 246 selected by fill\_select signal 264 and increments cntr0 211 or cntr1 213 selected by fill\_select signal 264. Flow proceeds to decision block 1326.

At decision block 1326, control logic 244 examines full0 signal 229 or full1 signal 227 specified by fill\_select signal 264 to determine whether buf0 242 or buf1 246 selected by fill\_select signal 264 is full. If so, flow proceeds to block 1328. Otherwise, flow returns to block 1306.

At block 1328, control logic 244 updates fill\_select signal 264. In one embodiment in which RNG unit 136 includes two buffers, updating fill\_select signal 264 comprises toggling fill\_select signal 264. In embodiments in which RNG unit 136 includes more than two buffers, fill\_select signal 264 comprises more than one bit, and updating fill\_select signal 264 comprises incrementing fill\_select signal 264 and wrapping around back to zero when incrementing past the number of buffers. Flow proceeds to decision block 1332.

At decision block 1332, control logic 244 examines full0 signal 229 or full1 signal 227 specified by fill\_select signal 264 as updated at block 1328 to determine whether buf0 242 or buf1 246 selected by fill\_select signal 264 is full, i.e., to determine whether all the buffers are full. If so, flow proceeds to block 1334. Otherwise, flow returns to block 1306.

At block 1334, control logic 244 powers off random bit generator 0 206 and random bit generator 1 208 via power\_cntrl signal 231 since all the buffers are full. Flow returns to decision block 1306.

Referring now to FIG. 14, a flowchart illustrating operation of microprocessor 100 of FIG. 1 when executing an XLOAD instruction of FIG. 3 according to an alternate embodiment of the present invention is shown. The flowchart of FIG. 14 is identical to the flowchart of FIG. 6 and like numbered blocks are the same, except that FIG. 14 includes an additional decision block 1403. Flow proceeds

## 26

from block 602 to decision block 1403. At decision block 1403, control logic 244 of FIG. 2 determines whether relevant bits in CSR 226 have been changed by the load of CSR 226 at block 602. If so flow proceeds to block 604 as in FIG. 6. Otherwise, flow proceeds to block 612, as shown.

The alternate embodiment has the advantage of not unnecessarily discarding already accumulated random bytes and restarting random byte accumulation. That is, if the load of CSR 226 did not change any of the values affecting the generation of random numbers by RNG unit 136, then there is no need to discard already accumulated random bytes and restart random byte accumulation since the random bytes were generated using the desired control values. In one embodiment, the relevant CSR 226 bits are string filter enable bit 334, gen select bit 336, CNT enable bit 342, and string filter max\_cnt 346.

Referring now to FIG. 15, a flowchart illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction of FIG. 3 according to an alternate embodiment of the present invention is shown. The flowchart of FIG. 15 is identical to the flowchart of FIG. 8 and like numbered blocks are the same, except that FIG. 15 includes an additional decision block 1507. Flow proceeds from block 806 to decision block 1507. At decision block 1507, control logic 244 of FIG. 2 determines whether relevant bits in CSR 226 have been changed by the copy to CSR 226 at block 806. If so flow proceeds to block 808 as in FIG. 8. Otherwise, flow proceeds to block 816, as shown.

The alternate embodiment has the advantage of not unnecessarily discarding already accumulated random bytes and restarting random byte accumulation. That is, if the copy to CSR 226 did not change any of the values affecting the generation of random numbers by RNG unit 136, then there is no need to discard already accumulated random bytes and restart random byte accumulation since the random bytes were generated using the desired control values. In one embodiment, the relevant CSR 226 bits are string filter enable bit 334, gen select bit 336, CNT enable bit 342, and string filter max\_cnt 346.

Referring now to FIG. 16, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention is shown. The XSTORE instruction of FIG. 16 is similar to the XSTORE instruction of FIG. 12, however in the alternate embodiment of FIG. 16, the destination operand of the XSTORE instruction of FIG. 16 specifies a register of microprocessor 100, such as an XMM register or a floating-point register or an MMX register or one of the integer unit registers, such as EBX, rather than specifying an address in system memory. That is, the valid random data bytes are atomically written into one of the user-visible registers in register file 108, rather than being stored to system memory. In the example of FIG. 16, the XSTORE instruction specifies the XMM3 register 376 register of SSE registers 352 of FIG. 3 to write the valid random data bytes into, as shown. Advantageously, like the XSTORE instruction of FIG. 12, the XSTORE instruction of FIG. 16 atomically writes the random data bytes into the user-visible register along with loading the count to EAX 1202 to facilitate multitasking operation with RNG unit 136. That is, the XSTORE instruction of FIG. 16 is also not interruptible.

Referring now to FIG. 17, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention is shown. The XSTORE instruction of FIG. 17 is similar to the XSTORE instruction



of FIG. 12, however in the alternate embodiment of FIG. 17, the XSTORE instruction includes an x86 architecture REP prefix. With the REP XSTORE instruction, the count of bytes of random data to be stored to system memory is specified as an input parameter in the ECX register 1702 of register file 108, as shown. Software loads into ECX 1702 the desired count of random data bytes to be stored to system memory prior to executing the REP XSTORE instruction.

In one embodiment, the REP XSTORE is interruptible between stores of random data bytes to system memory. The memory address is initially specified in general purpose registers of register file 108. In the example of FIG. 17, the memory address is specified in ES:EDI 1704 of register file 108, as shown. Each time one or more random data bytes are written to system memory, ES:EDI 1702 is updated to the next location in system memory where the random data bytes are to be stored. Additionally, each time one or more random data bytes are stored to system memory, ECX 1702 is updated to reflect the number of random bytes remaining to be stored. Assume, for example, a REP XSTORE instruction specifies in ECX 1702 a byte count of 28 and a memory address of 0x12345678. Assume the RNG unit 136 has 8 bytes available in one of buf0 242 and buf1 246 and writes the 8 bytes to system memory while more random data bytes are accumulating. When the 8 bytes are written to memory, ECX 1702 is updated to 20 to indicate that 20 more random data bytes must be written to system memory. Additionally, the address is updated to 0x12345680 as the next location in system memory where the next chunk of random data bytes will be written. An interrupt may occur at this point, and software can examine the updated values. When the interrupt has been serviced and control is returned to the REP XSTORE instruction, the REP XSTORE will resume execution using the updated values in ECX 1702 and ES:EDI 1704. In addition, at completion of the REP XSTORE instruction, the current value of CSR 226 of FIG. 2 is copied to the EAX register 1202 of register file 108.

Referring now to FIG. 18, a block diagram illustrating operation of microprocessor 100 of FIG. 1 when executing an XSTORE instruction according to an alternate embodiment of the present invention is shown. The XSTORE instruction of FIG. 18 is similar to the XSTORE instruction of FIG. 12; however, in the alternate embodiment of FIG. 18, only a portion of the random data bits held in R5 238 are stored to system memory 502. Instead, a divisor, N, is provided such that only every Nth bit of R5 238 is selected for storage to system memory 502, where N is equal to  $2^{**}(\text{divisor exponent})$ . That is, N is equal to 2 to an exponent referred to as the divisor exponent. The divisor exponent is an input parameter to the XSTORE instruction of FIG. 18 that is specified in the EDX 1802 register, as shown. EDX 1802 is one of the user-visible general purpose registers in register file 108.

In one embodiment, the number of random data bytes that may be held in R5 238 is 8 bytes, or 64 bits, the allowable values of the divisor exponent specified in EDX 1802 are 0, 1, 2, and 3, and the possible values of N are 1, 2, 4, and 8. Consequently, the number of valid random data bytes stored to system memory 502 by the XSTORE instruction in the embodiment of FIG. 18 is equal to  $8/N$ , i.e., 8, 4, 2, or 1. In another embodiment, the allowable values of the divisor exponent specified in EDX 1802 are 1, 2, and 3, and the possible values of N are 2, 4, and 8. The number of valid random data bytes stored to system memory 502 is placed in EAX 1202 at the end of execution of the XSTORE instruction along with the status of the instruction.

The XSTORE instruction of FIG. 18 also includes other embodiments with features described in other embodiments of the XSTORE instructions with respect to previous Figures. For example, The XSTORE instruction of FIG. 18 may store the every Nth selected and accumulated bits to a register in the microprocessor rather than to memory, such as described with respect to the embodiment of FIG. 16; or the valid byte count may be stored to memory rather than to the EAX register, such as described with respect to the embodiment of FIG. 7; or a REP prefix may be included, such as described with respect to the embodiment of FIG. 17.

Referring now to FIG. 19, an illustration of an example of operation of the XSTORE instruction of FIG. 18 according to the present invention is shown. An example binary random data bit value is shown in R5 238. Above each bit is shown its bit position within R5 238 in octal. Also shown is the random data value that is stored to system memory 502 of FIG. 18 given each of the four allowable values specified in EDX. As shown, if EDX is 0, then all 64 bits from R5 238 will be stored to system memory 502. If EDX is 1, then only 32 bits comprised of every other bit of R5 238 will be stored to system memory 502. If EDX is 2, then only 16 bits comprised of every fourth bit of R5 238 will be stored to system memory 502. If EDX is 3, then only 8 bits comprised of every eighth bit of R5 238 will be stored to system memory 502.

Advantageously, the XSTORE instruction of FIG. 18 potentially reduces correlation between sequential bits generated by RNG unit 136 by enabling the user to specify the divisor exponent in EDX 1802 for selecting every Nth bit of R5 238, where N is  $2^{**}\text{EDX}$ , in exchange for a lower random data rate.

Referring now to FIG. 20, a flowchart illustrating operation of RNG unit 136 of FIG. 1 to reduce sequential bit correlation according to one embodiment of the present invention is shown. In the embodiment of FIG. 20, the apparatus for performing the sequential bit correlation reduction function comprises various elements of microprocessor 100 of FIG. 1, such as registers 108, address generator 112, load unit 114, execute unit 116 (including ALU 162), RNG unit 136, store unit 118, write-back stage 122, write buffers 124, and bus interface unit 128. Microcode instructions stored in the microcode memory 132 of FIG. 1 control the microprocessor 100 elements according to the program listing shown in FIG. 21. The flowchart of FIG. 20 generally describes the microcode instructions of the program listing of FIG. 21. Flow begins at block 2002.

At block 2002, RNG unit 136 of FIG. 2 generates a stream of random bits via random bit generator 206 or 208, mux 214, and whitener 216, and the stream of random bits is accumulated into bytes by shift register 218, string filter 224, mux 228, demux 232, buf0 242 and buf1 246, mux 236, R5 238, and control logic 244 of FIG. 2 as described above with respect to the previous figures. Flow proceeds to decision block 2004.

At decision block 2004, microprocessor 100 determines whether 8 random data bytes have been accumulated in buf0 242 or buf1 246 by examining the available byte count 332 from CSR 226 of FIG. 3. If so, flow proceeds to block 2012. Otherwise, flow proceeds to block 2006.

At block 2006, microprocessor 100 sets the number of valid random data bytes to 0 since 8 bytes had not been accumulated. Flow proceeds to block 2008.

At block 2008, microprocessor 100 loads EAX 1202 with the status obtained from CSR 226 and with the number of valid random data bytes that have been stored to memory. If



block **2008** was reached from block **2006**, the number of valid data bytes is 0. If block **2008** was reached from block **2018**, the number of valid data bytes is 8. If block **2008** was reached from block **2044**, the number of valid data bytes is a function of the divisor exponent specified in EDX **1802**, in particular  $2^{*(3-\text{divisor exponent})}$ . Flow ends at block **2008**.

At block **2012**, microprocessor **100** loads the contents of R5 **238** into a temporary storage location, referred to in FIG. **20** as temp1. In one embodiment, only the random data bytes from R5 **238** are loaded into temp1, not the available byte count. In the embodiment of the microcode listing of FIG. **21**, two 32-bit temporary registers, r4 and r5, are used collectively as temp1. Flow proceeds to decision block **2014**.

At decision block **2014**, microprocessor **100** determines whether the divisor exponent specified in EDX **1802** is 0, i.e., whether all the bits from R5 **238** will be stored to memory. If so, flow proceeds to block **2016**. Otherwise, flow proceeds to block **2022**.

At block **2016**, microprocessor **100** stores all eight valid random data bytes accumulated in R5 **238** to system memory **502** of FIG. **18**. Flow proceeds to block **2018**.

At block **2018**, microprocessor **100** sets the number of valid random data bytes to 8 since all 8 bytes were stored to system memory **502** at block **2106**. Flow proceeds to block **2008**.

At block **2022**, microprocessor **100** calculates the divisor, N, as 2 to the divisor exponent value stored as an input parameter value to the XSTORE instruction in EDX **1802**. Flow proceeds to block **2024**.

At block **2024**, microprocessor **100** calculates a loopcount value, which is 64 divided by the divisor N. The loopcount is also the number of bits that will be stored to system memory **502**. Flow proceeds to block **2026**.

At block **2026**, microprocessor **100** clears EAX **1202** to 0. Flow proceeds to block **2028**.

At block **2028**, microprocessor **100** shifts EAX **1202** left one bit to make room in EAX **1202** for the next bit to be selected and accumulated from the original data taken from R5 **238**. Flow proceeds to block **2032**.

At block **2032**, microprocessor **100** selects and accumulates the next Nth bit by taking temp1 and isolating its bottom bit (i.e., masking off all but the bottom bit) and adding the isolated bit to EAX **1202**. Flow proceeds to block **2034**.

At block **2034**, microprocessor **100** shifts temp1 right by N bits, thereby placing the next Nth bit to be selected into the bottom bit location of temp1. By shifting temp1 right by N bits, the bits between the bits selected and accumulated in block **2032** are discarded. Flow proceeds to block **2036**.

At block **2036**, microprocessor **100** decrements the loopcount by one. Flow proceeds to decision block **2038**.

At decision block **2038**, microprocessor **100** determines whether the loopcount has reached zero. If so, flow proceeds to block **2042**. Otherwise, flow returns to block **2028**.

At block **2042**, microprocessor **100** stores EAX **1202** to system memory **502**. EAX **1202** includes every Nth random data bit selected and accumulated from R5 **238**. In one embodiment, the entire contents of EAX **1202** are stored to system memory **502** even though some of the bytes in EAX **1202** may not contain valid random data bytes. However, the number of valid data bytes stored to system memory **502** is reflected in EAX **1202** at the completion of the XSTORE instruction per block **2008**, thereby enabling the program to determine the number of valid random data bytes stored to system memory **502**. For example, if EDX **1802** is 2, then only two bytes of the four bytes stored to system memory

**502** are valid, and the number of valid data bytes will be set to 2 along with the status in EAX **1202**. Flow proceeds to block **2044**.

At block **2044**, microprocessor **100** sets the number of valid random data bytes to 8 divided by N since N was 2, 4, or 8 and all 8/N bytes were stored to system memory **502** at block **2042**. Flow proceeds to block **2008**.

Referring now to FIG. **21**, a listing of microcode instructions for instructing microprocessor **100** of FIG. **1** to reduce sequential bit correlation according to the present invention is shown. The following discussion is helpful in understanding the microcode listing.

The listing includes branch instructions, namely jump instructions (je.32, and jel.32), a loop instruction (loopn.32), and a return instruction (return). The instruction location immediately following all branch instructions is referred to as a delay slot. The instruction in the delay slot executes regardless of whether the branch is taken. Thus, if the branch is not taken, then the instruction in the delay slot and next the instruction following the instruction in the delay slot are executed; if the branch is taken, the instruction in the delay slot is executed and next the instruction at the branch target address is executed.

The microcode instructions use eight 32-bit general purpose registers comprised in register file **108**, referred to in the listing as r0 through r7. In one embodiment, r0 through r7 are not user-visible registers. The value stored in r0 is zero at all times. In one embodiment, the arithmetic and logical operations specified by the microcode instructions—such as the and, add, and shift instructions—are mainly performed by ALU **162** of FIG. **1**.

The three-operand instructions, except for the branch instructions, are of the form:

<opcode> <destination> <source1> <source2>.

The mfxd. **64 xmm5** instruction at line **07** followed by the dmtid r4, r5 instruction at line **08** causes the contents of the 64-bit R5 **238** register of FIG. **2**, which is shadowed with the XMM5 register **374** of FIG. **3**, to be copied to the two 32-bit registers r4 and r5. With respect to the dmtid r2, r3 instruction at line **01**, the portion of the microcode that branched to get\_random\_data included an mfxd. **64 xmm0** (i.e., CSR **226**) instruction in the delay slot after the branch. Hence, the combination of the two instructions causes the contents of the 64-bit CSR **226** to be copied to the two 32-bit registers r2 and r3.

Referring now to FIG. **22**, a block diagram illustrating portions of RNG unit **136** of FIG. **1** including a bit selector **2202** to reduce sequential bit correlation according to an alternate embodiment of the present invention is shown. RNG unit **136** of FIG. **22** is similar to RNG unit **136** of FIG. **2**; however, only register R5 **238** of FIG. **2** is shown in FIG. **22**. Unlike FIG. **2**, in FIG. **22**, R5 **238** is not coupled directly to data bus **144**. Instead, the output of R5 **238** is coupled to an intermediate data bus **2206**. RNG unit **136** of FIG. **22** also includes a bit selector **2202**. The input of bit selector **2202** is coupled to intermediate data bus **2206** and the output of bit selector **2202** is coupled to data bus **144** of FIG. **1**, denoted DB **144** in FIG. **22**. In the embodiment of FIG. **22**, intermediate data bus **2206** and DB **144** are 64-bit buses and R5 **238** includes 64-bits for storing random data bytes, i.e., stores 8 bytes of random data. Bit selector **2202** also includes a control input which receives a divisor exponent signal **2204**, which is the value specified as an input parameter to the XSTORE instruction in EDX **1802** of FIG. **18**. In one embodiment, bit selector **2202** selects every bit, every other bit, every fourth bit, or every eighth bit from intermediate data bus **2206** to provide eight, four, two, or one



random data bytes, respectively, on data bus 144 based on the value of divisor exponent 2204, as described above and as shown in the example of FIG. 19.

Referring now to FIG. 23, a block diagram illustrating bit selector 2202 of FIG. 22 in detail according to the present invention is shown. Bit selector 2202 includes sixty-four 4-to-1 muxes, denoted 2302-0 through 2302-63, and referred to collectively as muxes 2302. Each of muxes 2302 includes four inputs denoted 0, 1, 2, and 3. Each of muxes 2302 also includes a control input coupled to divisor exponent 2204 of FIG. 22. If divisor exponent 2204 equals 0, muxes 2302 select their 0 input for provision on the output; if divisor exponent 2204 equals 1, muxes 2302 select their 1 input for provision on the output; if divisor exponent 2204 equals 2, muxes 2302 select their 2 input for provision on the output; if divisor exponent 2204 equals 3, muxes 2302 select their 3 input for provision on the output.

In FIG. 23, muxes 2302-0, 2302-1, 2302-2, 2302-3, 2302-n, and 2302-63 are shown. In FIG. 23, "n" corresponds to the bit number of DB 144, and mux 2302-n refers generically to the mux 2302 whose output is coupled to DB[n] 144. The output of mux 2302-0 is coupled to DB[0] 144 of FIG. 22, i.e., to bit 0 of DB 144; the output of mux 2302-1 is coupled to DB[1] 144; the output of mux 2302-2 is coupled to DB[2] 144; the output of mux 2302-3 is coupled to DB[3] 144; the output of mux 2302-n is coupled to DB[n] 144; and the output of mux 2302-63 is coupled to DB[63] 144, as shown.

Each mux 2302-n receives on its 0 input intermediate data bus 2206 signal n, receives on its 1 input intermediate data bus 2206 signal 2n, receives on its 2 input intermediate data bus 2206 signal 4n, and receives on its 3 input intermediate data bus 2206 signal 8n. Hence, mux 2302-0 receives on its 0 input intermediate data bus 2206 signal 0, receives on its 1 input intermediate data bus 2206 signal 0, receives on its 2 input intermediate data bus 2206 signal 0, and receives on its 3 input intermediate data bus 2206 signal 0; mux 2302-1 receives on its 0 input intermediate data bus 2206 signal 1, receives on its 1 input intermediate data bus 2206 signal 2, receives on its 2 input intermediate data bus 2206 signal 4, and receives on its 3 input intermediate data bus 2206 signal 8; mux 2302-2 receives on its 0 input intermediate data bus 2206 signal 2, receives on its 1 input intermediate data bus 2206 signal 4, receives on its 2 input intermediate data bus 2206 signal 8, and receives on its 3 input intermediate data bus 2206 signal 16; mux 2302-3 receives on its 0 input intermediate data bus 2206 signal 3, receives on its 1 input intermediate data bus 2206 signal 6, receives on its 2 input intermediate data bus 2206 signal 12, and receives on its 3 input intermediate data bus 2206 signal 24; and mux 2302-63 receives on its 0 input intermediate data bus 2206 signal 63, as shown. Any inputs to muxes 2302 with a value greater than 63 are don't cares.

As mentioned above, the present inventor has observed minor correlation under some environmental conditions between sequential generated bits that reduces the randomness of the numbers generated. Advantageously, by selecting every Nth bit generated by the random bit generators as described herein, the present inventor has observed a Shannon entropy increase and approximate associated minimum random bit generation rate as follows:

EDX/N	Shannon Entropy (bits/byte)	Data Rate (Megabits/second)
0/1	7.98	4
1/2	7.995	2
2/4	7.999	1
3/8	7.99982	0.5

Although the present invention and its objects, features, and advantages have been described in detail, other embodiments are encompassed by the invention. For example, although in the embodiments described the divisor is a power of two, the invention is adaptable to other divisor values. Furthermore, although in the embodiments described the divisor is computed as two the power programmed in a register, the divisor may be specified by other methods. For example, the divisor could be specified directly as the value stored in the register.

Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiments as a basis for designing or modifying other structures for carrying out the same purposes of the present invention without departing from the spirit and scope of the invention as defined by the appended claims.

I claim:

1. A microprocessor, comprising:

a random bit generator, for generating a series of random bits;

an arithmetic logic unit (ALU), coupled to said random bit generator, for selecting every Nth bit from said series of random bits, wherein N is an integer greater than 1, and for accumulating said every Nth bit selected into a register coupled to said ALU;

an instruction translator, for translating an instruction of an instruction set of the microprocessor, said instruction instructing the microprocessor to store said every Nth bit selected and accumulated; and

a memory, coupled to said ALU, for storing microcode instructions, said microcode instructions including a plurality of instructions for performing said instruction, wherein said plurality of instructions comprises one or more instructions for instructing said ALU to shift said series of random bits by said N.

2. The microprocessor of claim 1, further comprising:

a programmable register, coupled to said ALU, for storing a value used to compute said N.

3. The microprocessor of claim 2, wherein said N equals 2 to an exponent equal to said value stored in said programmable register.

4. The microprocessor of claim 2, wherein said N equals said value stored in said programmable register.

5. The microprocessor of claim 1, wherein said instruction stores said every Nth bit selected and accumulated to a memory coupled to the microprocessor.

6. The microprocessor of claim 1, wherein said instruction stores said every Nth bit selected and accumulated to a second register coupled to said ALU.

7. The microprocessor of claim 1, wherein said N is an input parameter to said instruction.

8. The microprocessor of claim 7, wherein said N is an input parameter to said instruction stored in a general purpose register of the microprocessor.

9. The microprocessor of claim 1, wherein said plurality of instructions comprises one or more instructions for

33

instructing said ALU to perform logical operations to isolate ones of said shifted series of random bits.

10. The microprocessor of claim 9, wherein said logical operations to isolate said ones of said shifted series of random bits comprise a logical AND operation.

11. The microprocessor of claim 9, wherein said plurality of instructions comprises one or more instructions for instructing said ALU to perform arithmetic or logical operations to accumulate said ones of said shifted series of random bits into said register.

12. The microprocessor of claim 11, wherein said arithmetic or logical operations to accumulate said ones of said shifted series of random bits into said register comprise an addition operation.

13. The microprocessor of claim 11, wherein said arithmetic or logical operations to accumulate said ones of said shifted series of random bits into said register comprise a shift operation.

14. The microprocessor of claim 1, wherein said N is greater than 0.

15. An apparatus for reducing correlation between sequential random bits, comprising:

a random bit generator, for generating a stream of random bits;

34

a first register, coupled to said random bit generator, for storing a plurality of said stream of random bits;

a plurality of multiplexers, coupled to said first register, for selecting every Nth bit of said plurality of said stream of random bits, said plurality of multiplexers selecting said every Nth bit based on a control signal; and

a second register, coupled to said plurality of multiplexers, for storing said every Nth bit of said plurality of said stream of random bits selected by said plurality of multiplexers.

16. The apparatus of claim 15, wherein said N is programmable.

17. The apparatus of claim 15, wherein said N equals 2 to an exponent, wherein said exponent equals a value specified on said control signal.

18. The apparatus of claim 15, wherein said N is an integer greater than 0.

19. The apparatus of claim 15, wherein said N is an integer greater than 1.

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