

US007091572B2

(12) **United States Patent**
Andoh et al.

(10) **Patent No.:** **US 7,091,572 B2**
(45) **Date of Patent:** **Aug. 15, 2006**

(54) **FAST RECOVERY DIODE WITH A SINGLE LARGE AREA P/N JUNCTION**

(56) **References Cited**

(75) Inventors: **Kohji Andoh**, El Segundo, CA (US);
Silvestro Fimiani, Turin (IT); **Fabrizio Rue Redda**, Casalle (IT); **Davide Chiola**, Redondo Beach, CA (US)

(73) Assignee: **International Rectifier Corporation**, El Segundo, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/233,760**

(22) Filed: **Sep. 23, 2005**

(65) **Prior Publication Data**
US 2006/0017130 A1 Jan. 26, 2006

Related U.S. Application Data
(63) Continuation of application No. 10/115,757, filed on Apr. 2, 2002, now abandoned.
(60) Provisional application No. 60/280,972, filed on Apr. 2, 2001.

(51) **Int. Cl.**
H01L 29/861 (2006.01)
H01L 31/107 (2006.01)

(52) **U.S. Cl.** **257/481; 257/484; 257/104; 257/603**

(58) **Field of Classification Search** **257/104, 257/481, 484, 603**
See application file for complete search history.

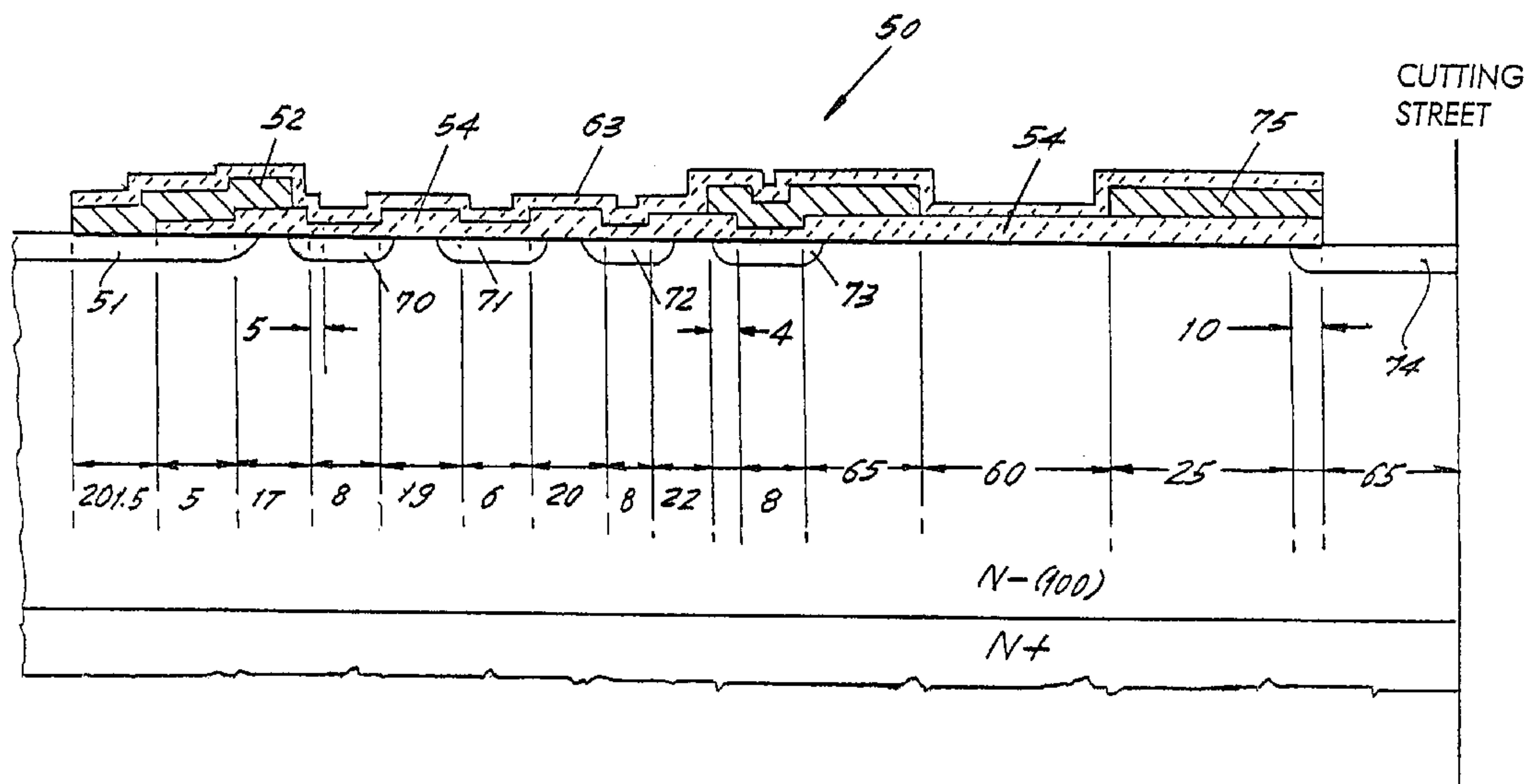
U.S. PATENT DOCUMENTS			
4,567,502 A	1/1986	Nakagawa et al.	357/53
4,862,229 A	8/1989	Mundy et al.	357/15
4,901,120 A	2/1990	Weaver et al.	357/15
5,283,202 A	2/1994	Pike, Jr. et al.	437/31
5,523,604 A	6/1996	Merrill	257/356
5,859,465 A	1/1999	Spring et al.	257/484
6,221,688 B1	4/2001	Fujihira et al.	438/92
6,222,248 B1	4/2001	Fragapane	257/565
6,525,389 B1	2/2003	Ahmed	257/486

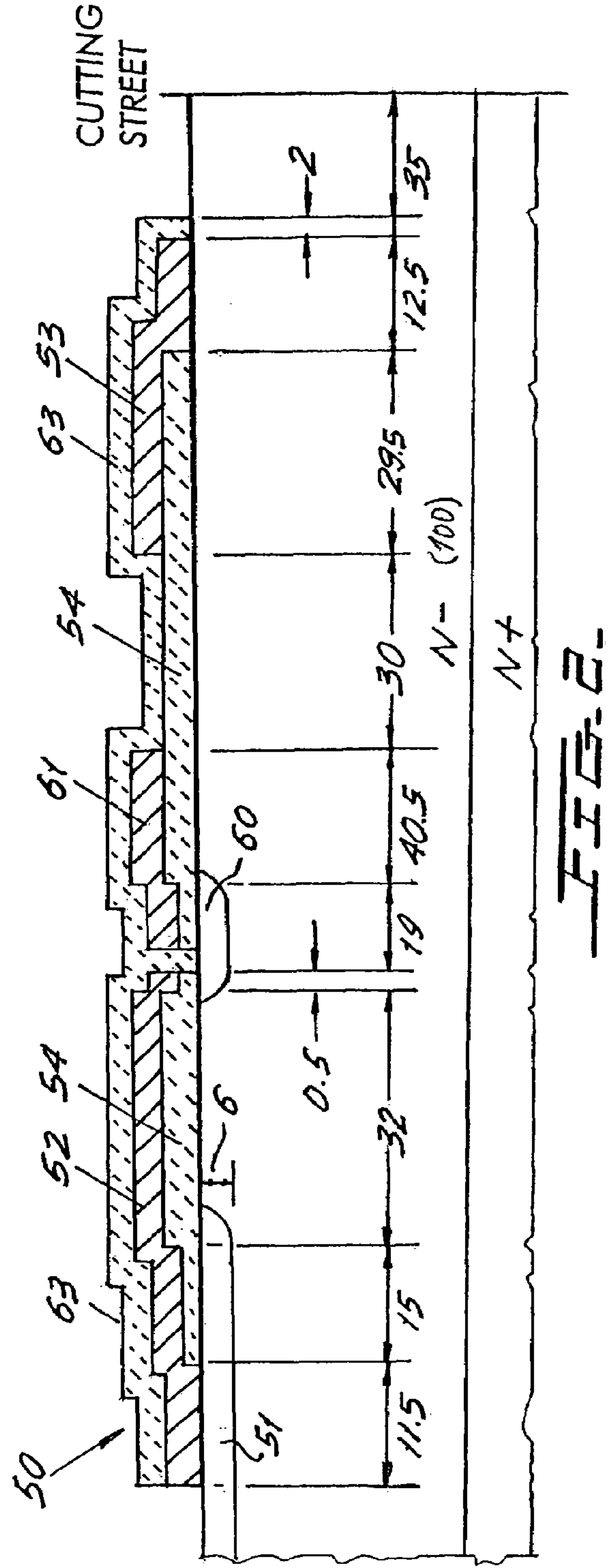
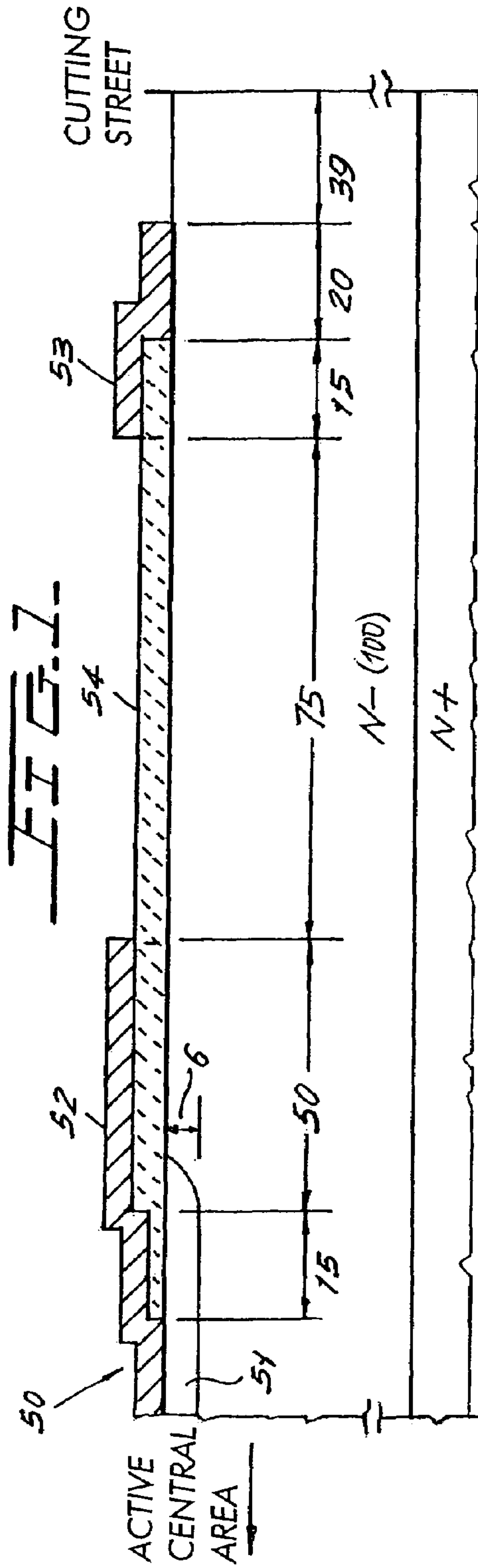
FOREIGN PATENT DOCUMENTS			
EP	1 033 756	9/2000	
JP	2000082825	3/2000	
JP	2000114550	4/2000	
JP	2002033326	1/2002	

Primary Examiner—Mary Wilczewski
Assistant Examiner—Monica Lewis
(74) *Attorney, Agent, or Firm*—Ostrolenk, Faber, Gerb & Soffen, LLP

(57) **ABSTRACT**
A fast recovery diode has a single large area P/N junction surrounded by a termination region. The anode contact in contact with the central active area extends over the inner periphery of an oxide termination ring and an EQR metal ring extends over the outer periphery of the oxide termination ring. Platinum atoms are diffused into the back surface of the device. A three mask process is described. An amorphous silicon layer is added in a four mask process, and a plurality of spaced guard rings are added in a five mask process.

5 Claims, 2 Drawing Sheets





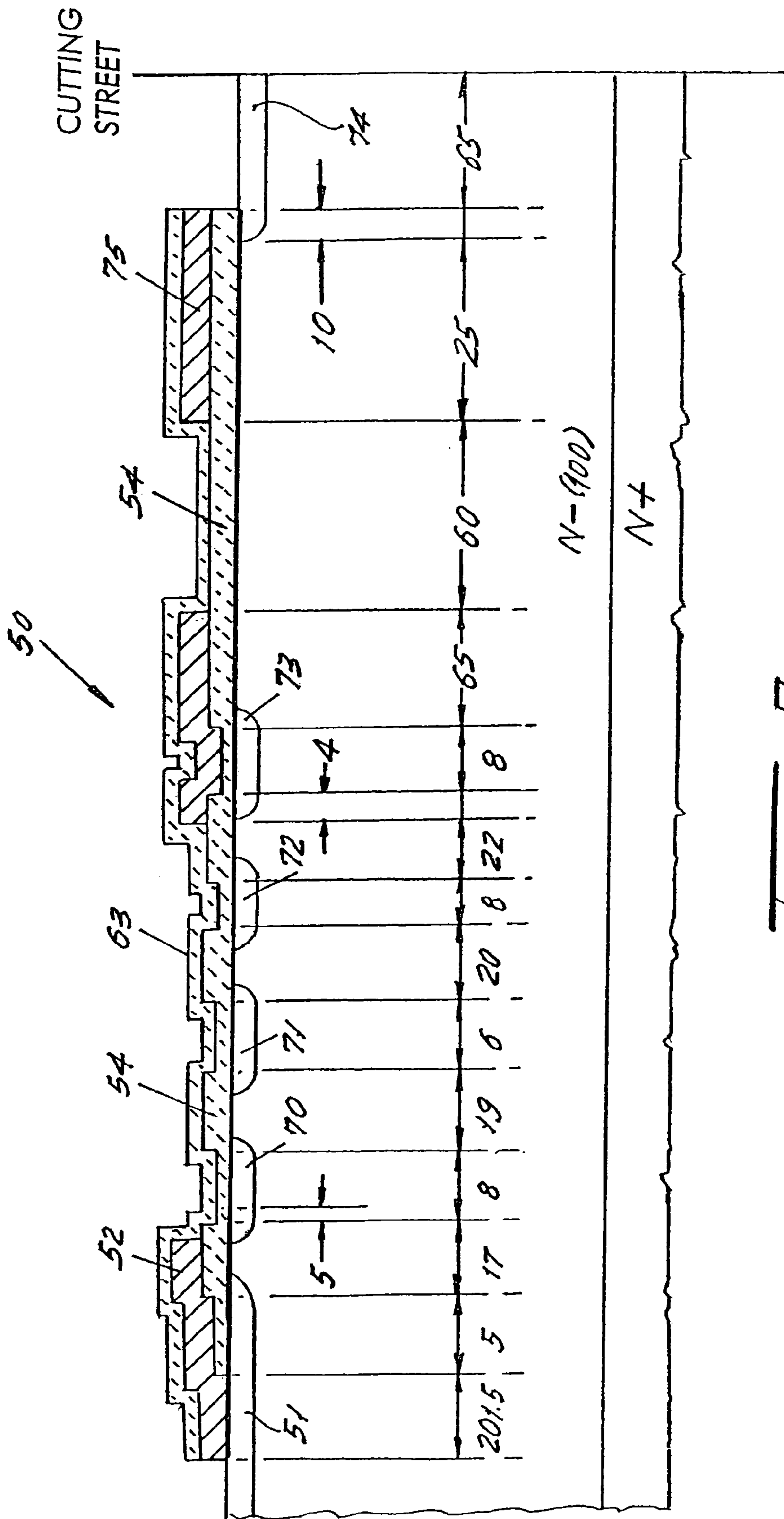


FIG. 3.

FAST RECOVERY DIODE WITH A SINGLE LARGE AREA P/N JUNCTION

RELATED APPLICATION

This application is a continuation of U.S. patent application Ser. No. 10/115,757, filed Apr. 2, 2002, now abandoned which is based upon and claims priority to U.S. Provisional Application Ser. No. 60/280,972, filed Apr. 2, 2001.

FIELD OF THE INVENTION

This invention relates to semiconductor devices and processing and more specifically relates to a low cost process for the manufacture of a fast recovery diode and to a novel fast recovery diode structure.

BACKGROUND OF THE INVENTION

Fast recovery diodes are well known. The processes used for the manufacture of such devices frequently employ cellular and/or stripe and/or trench technologies in a silicon die with electron irradiation for lifetime killing. Such devices use a high mask count and are relatively expensive.

It would be desirable to make a fast recovery diode (FRED) with a reduced mask count and lifetime killing but with equal or better characteristics to those of existing FRED devices.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention a novel FRED is formed using a simple single large area junction with platinum lifetime killing. A simplified termination structure is employed using a simple field plate termination at low voltages (200 volts); amorphous silicon on the field plate at intermediate voltage (400 volts); and plural floating guard rings and an equipotential ring in the cutting street in a higher voltage (600 volts) device. Three, four and five masks are used for the 200 volt, 400 volt and 600 volt devices respectively. Excellent characteristics, equivalent to or better than those of existing FREDs with higher mask counts, are obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-section of a portion of a novel FRED die made in accordance with the invention by a 3 mask process for a 200 volt device.

FIG. 2 is a cross-section of a portion of a novel FRED die made in accordance with the invention by a 4 mask process for a 400 volt device.

FIG. 3 is a cross-section of a portion of a novel FRED device made in accordance with the invention by a 5 mask process for a 600 volt device.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 shows, in cross-section, a portion of a fast recovery diode die **50** and its termination. The diode consists of a simple large area P type diffusion **51** in an N type epitaxial layer **100** atop the die **50**. Diffusion **51** is a boron diffusion having a depth of 6 μm and a peak concentration of $2\text{E}19/\text{cm}^3$. A field oxide **54**, such as silicon dioxide, is formed atop the silicon surface and a conductive (aluminum) field plate **52** which is an extension of the anode electrode is also formed. A metal (aluminum) EQR ring **53** completes

the termination. An anode contact is connected to the P type diffusion **51** over substantially the full top area of die **50** and a cathode contact (not shown) is connected to its bottom surface. Platinum atoms are diffused into the back surface of the die (wafer) which are driven in from a 10 \AA thick layer of platinum for 30 minutes at 950° C. Note that the dimensions on FIG. 1 (and FIGS. 2 and 3) are out of scale and are in microns.

The novel structure of FIG. 1 is made by the following novel 3 mask process of the invention for a FRED rated at 200 volts. The starting wafer has an N⁺ arsenic doped substrate which has an N⁻ phosphorus doped epitaxial layer **100**. The epitaxial layer thickness is 25 μm and has a resistivity of 10 ohm-cm. The process steps used are given in the following Table:

STEP	NOTE
Field Ox 54 <u>MASK 1</u>	Oxide grown to 1.4 μm thick
Oxide Etch BBr3 Preclean BBr3 Dep BBr3 Deglass	BOE Etch; 17 minutes Time out 2 h before a BBr3 dep Target sheet resistance 55 ohm/square 4 min etch in 50:1 H ₂ O:HF, 15 min timeout after BBr3 Dep
BBr3 Ox preclean BBr3 Ox POC13 dep POC13 deglass POC13 OX <u>MASK 2</u>	time out 2 h before BBr3 ox Target xj = μm Target sheet resistance 14.5 ohm square Etch time 1 min. time out after POC13 dep 2 hrs. Dry oxidation. Oxide thickness 100 \AA . (open active area and termination)
Oxide Etch Preclean Pt. evap Platinum drive in Preclean Al/Si sputter (52) <u>MASK 3</u>	Etch time 15 min 50:1 H ₂ O:HF 10 \AA on wafer back. 30 min at 950° C. Quick extraction. 50:1 H ₂ O:HF Al/Si sputtering, 3 μm thickness
Al etch Defreckle Photoresist Strip Al sinter Wafer Tape Wafer backgrind Wafer detape Backside metal Test	7 min in aluminum etch solution 1 min in Ashland Defreckle solution Standard process 30 min, 420° C., Forming gas atmosphere. Tape on wafer front 14 mil Standard process CrNiAg sputtering. Probe Test for 200 V FRED.

FIG. 2 shows a cross-section like that of FIG. 1, but with a termination modified to make the device a 400 volt device with a 4 mask process. Components similar to those of FIG. 1 have similar identifying numerals.

In order to withstand 400 volts, the device of FIG. 2 employs an added diffusion defining termination P ring **60** (also referred to as a floating guard ring diffusion), an added field plate **61** and an amorphous silicon layer **63** on top of the termination surface, including field plates **52** and **61** and EQR ring **53**.

The device of FIG. 2 is made by a novel 4 mask process to increase the device rating to 400 volts. The process begins with a wafer like that of FIG. 1, except that the epitaxial layer **100** is 47 μm thick, and has a resistivity of 15 ohm-cm.

The process for the devices of FIG. 2 starts with steps 1 to 22 above up to ("photoresist strip" and before "Al sinter") for the device of FIG. 1. Following step 22, and before Al sinter, a layer **63** of amorphous silicon, 1800 \AA thick, is deposited atop the wafer surface. A mask 4 step is then

3

carried out to etch the amorphous silicon to open the active area; specifically, a wet etch (DFK) process.

FIG. 3 is a cross-section like that of FIGS. 1 and 2 with elements added to permit the device to operate at 600 volts. The process used is a 5 mask process. The elements added are P diffusion rings 70 to 73 (also referred to as spaced floating guard ring diffusions) and N⁺ diffusion 74 in the cutting street and surrounding the die edge to act as an N⁺ EQR ring, and a modified metal EQR ring 75. The starting wafer for the 600 volt device has an epitaxial layer 100 thickness of 61 μm and resistivity of 21.5 ohm-cm. The novel 5 mask process for making the device of FIG. 3 employs the steps used for the 400 volt device of FIG. 2, except that a further mask step is used after step 8 above and following the B Br Ox step. Following this added mask step, there is a BOE etch for 17 minutes to open windows for the guard ring diffusions and the process continues as described for FIGS. 1 and 2.

In each of FIGS. 1, 2 and 3, the novel FRED device employs a single large P diffusion for the active area and platinum atoms for life time killing. In FIGS. 2 and 3, the device termination is covered with amorphous silicon.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art.

What is claimed is:

1. A fast recovery diode comprising a silicon die having a substrate of a first conductivity type; a single central diffusion of a second conductivity type extending onto the upper surface of said die defining a single continuous P-N

4

junction; a termination region surrounding the outer periphery of said diffusion and including a silicon dioxide layer which overlies the outer edge of said diffusion and which defines the diffusion window for said diffusion; an anode contact metal in contact with the surface of said diffusion and overlying the inner peripheral edge of said silicon dioxide layer such that said anode contact metal is insulated from said substrate and defines a first field plate; an EQR conductive ring which is separated from said anode contact and which extends over the outer peripheral edge of said silicon dioxide layer; platinum atoms diffused into the back surface of said die to act as life time killers; and at least one floating guard ring diffusion disposed beneath and laterally adjacent to said field plate.

2. The diode of claim 1, which further includes an amorphous silicon layer deposited atop said termination region.

3. The diode of claim 2, which further includes a conductive second field plate in said termination region disposed between said first field plate and said EQR ring, with said amorphous silicon layer overlying said first named field plate, said second field plate and said EQR ring.

4. The diode of claim 3, which further includes a plurality of spaced floating guard ring diffusions in said upper surface and between said first named field plate and said second field plate and further includes a guard ring in the peripheral edge of said die.

5. The diode of claim 1, wherein said first conductivity type is the N type.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,091,572 B2
APPLICATION NO. : 11/233760
DATED : August 15, 2006
INVENTOR(S) : Kohji Andoh et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, Item (75), change the second Inventor to:

--Silvestro Fimiani, Torino (IT)--.

Signed and Sealed this

Twenty-eighth Day of November, 2006

A handwritten signature in black ink on a dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS

Director of the United States Patent and Trademark Office