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(54) **PCRAM MEMORY CELL AND METHOD OF MAKING SAME**

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See application file for complete search history.

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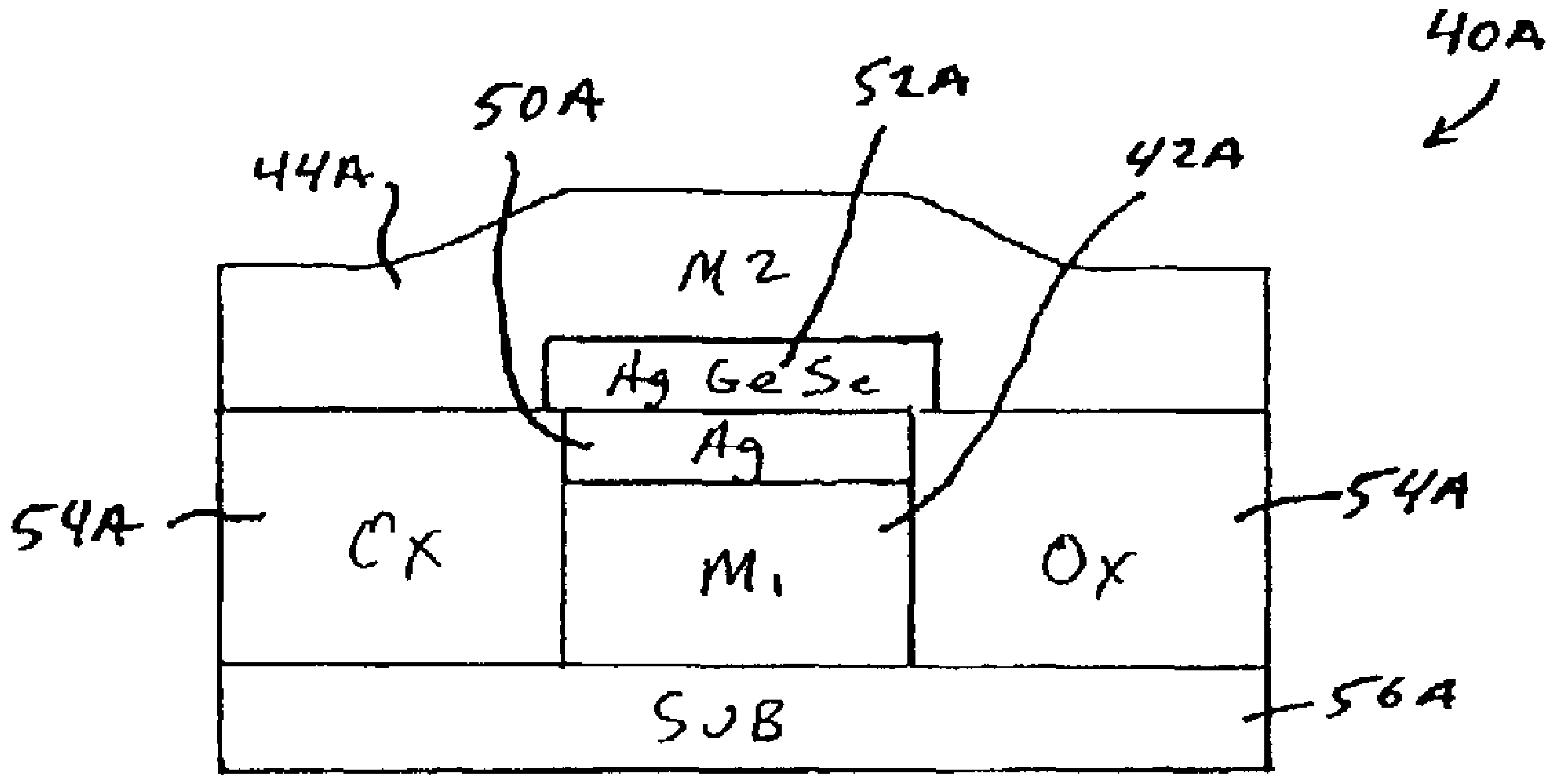
(57) **ABSTRACT**

An inverted PCRAM cell is formed by plating the bottom electrode, made of copper for example, with a conductive material, such as silver. Chalcogenide material is disposed over the plated electrode and subjected to a conversion process so that ions from the plated material diffuse into the chalcogenide material.

36 Claims, 8 Drawing Sheets



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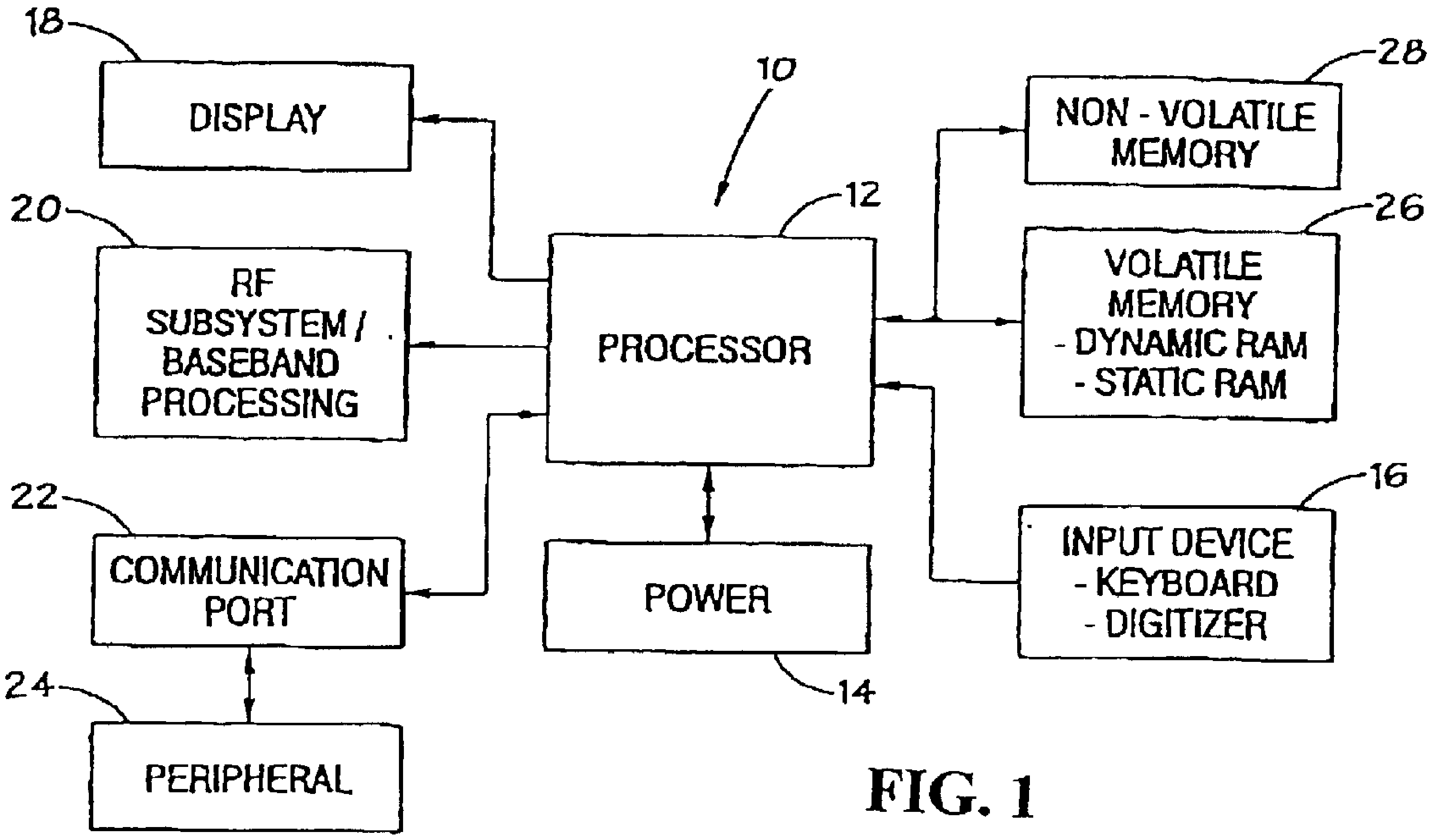
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DISPLAY
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28
NON - VOLATILE MEMORY
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20
RF SUBSYSTEM / BASEBAND PROCESSING
PROCESSOR
26
VOLATILE MEMORY
- DYNAMIC RAM
- STATIC RAM
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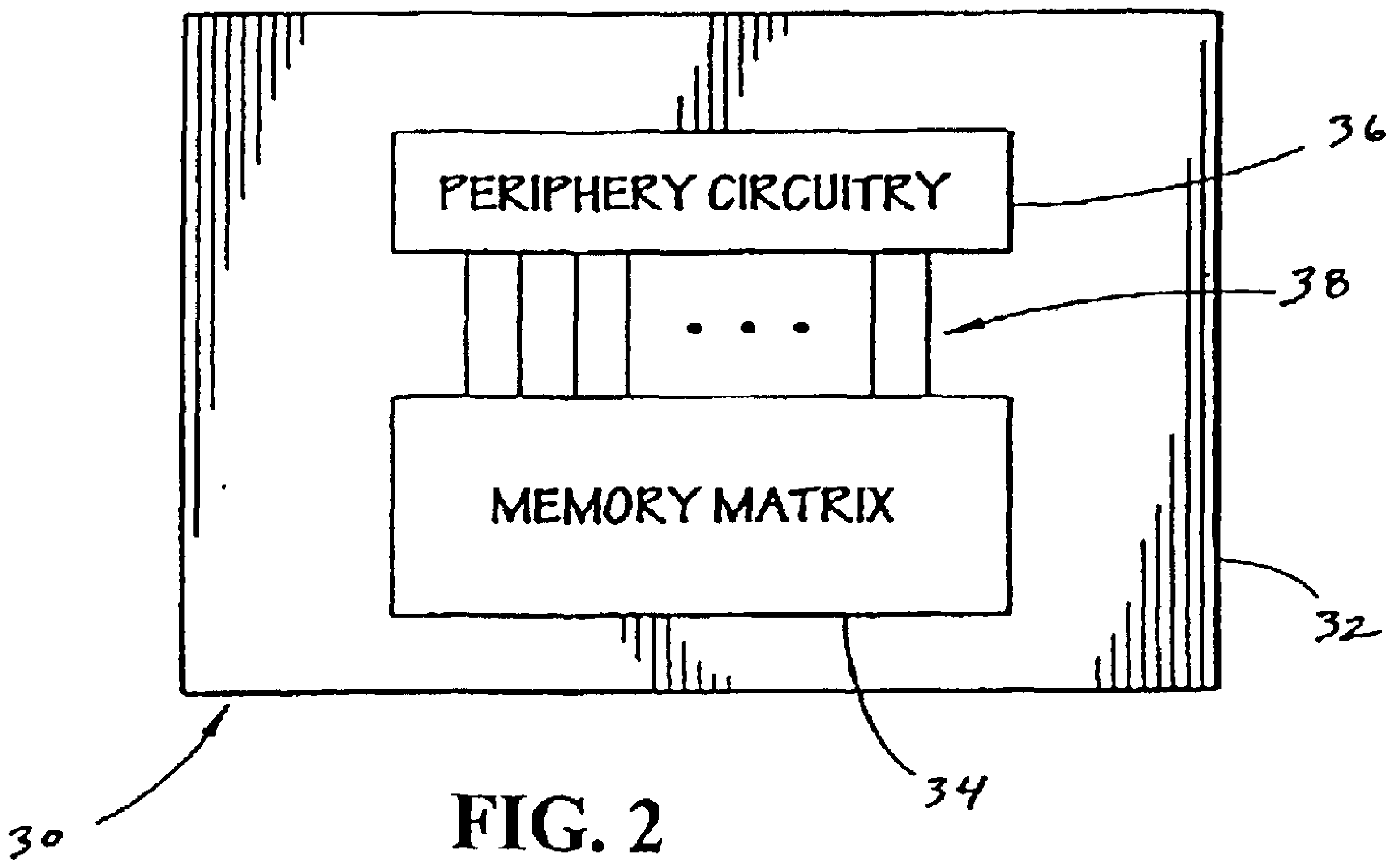
COMMUNICATION PORT
POWER
16
INPUT DEVICE
- KEYBOARD
- DIGITIZER
24
14
PERIPHERAL

FIG. 1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38
MEMORY MATRIX
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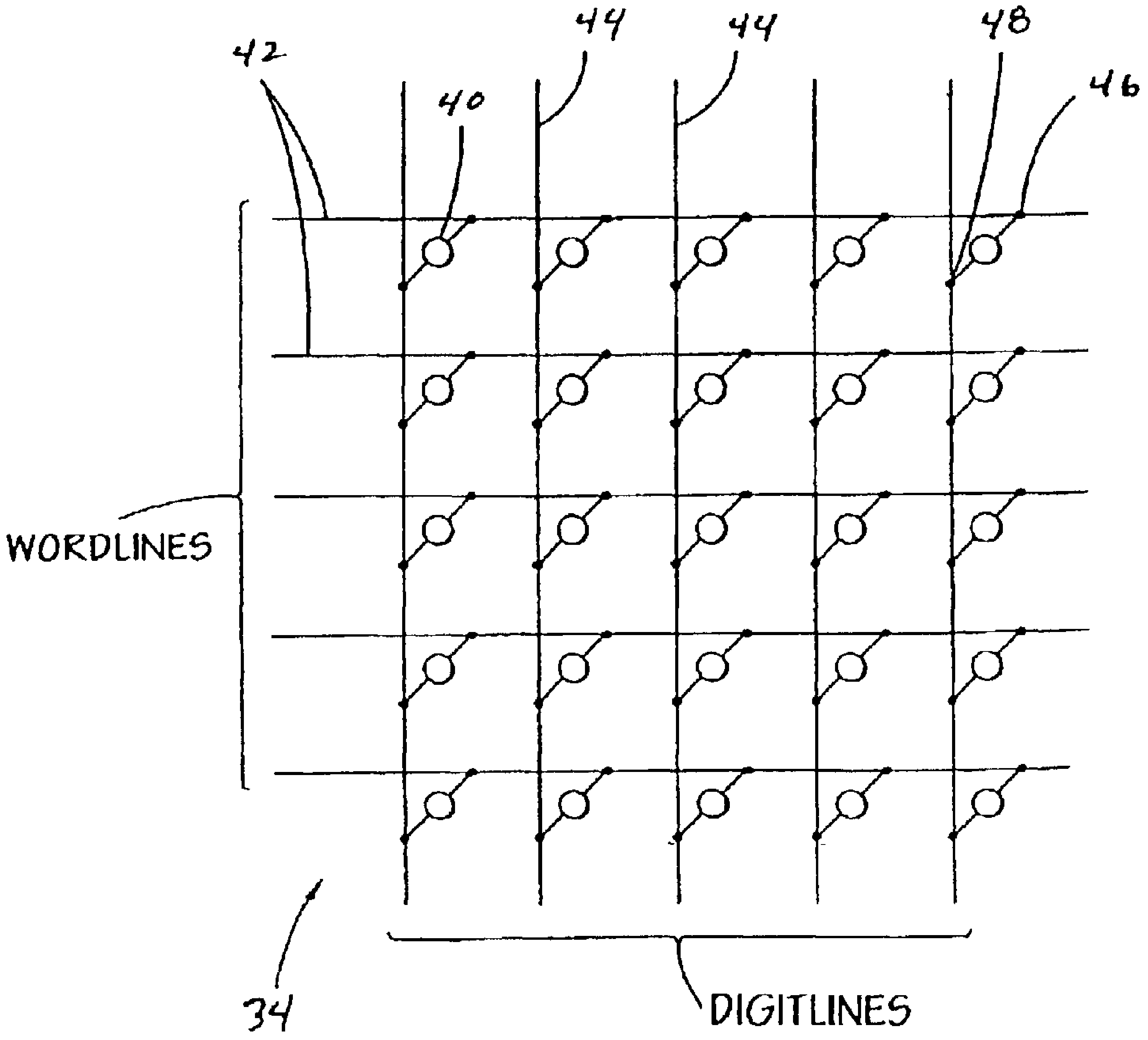
34
30

FIG. 2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DIGITLINES

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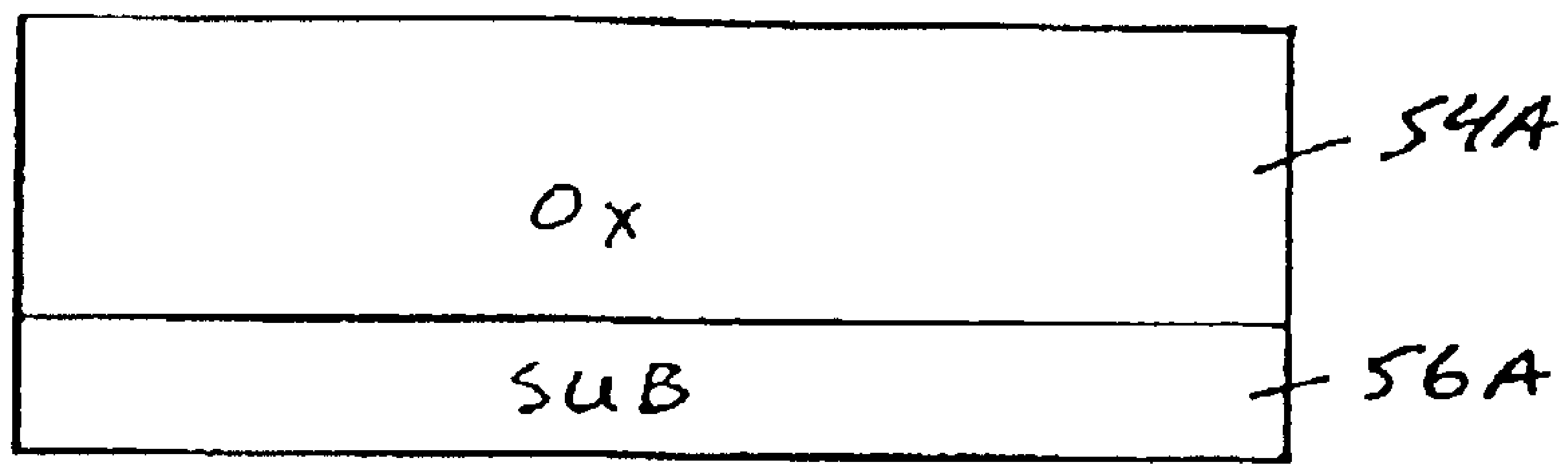

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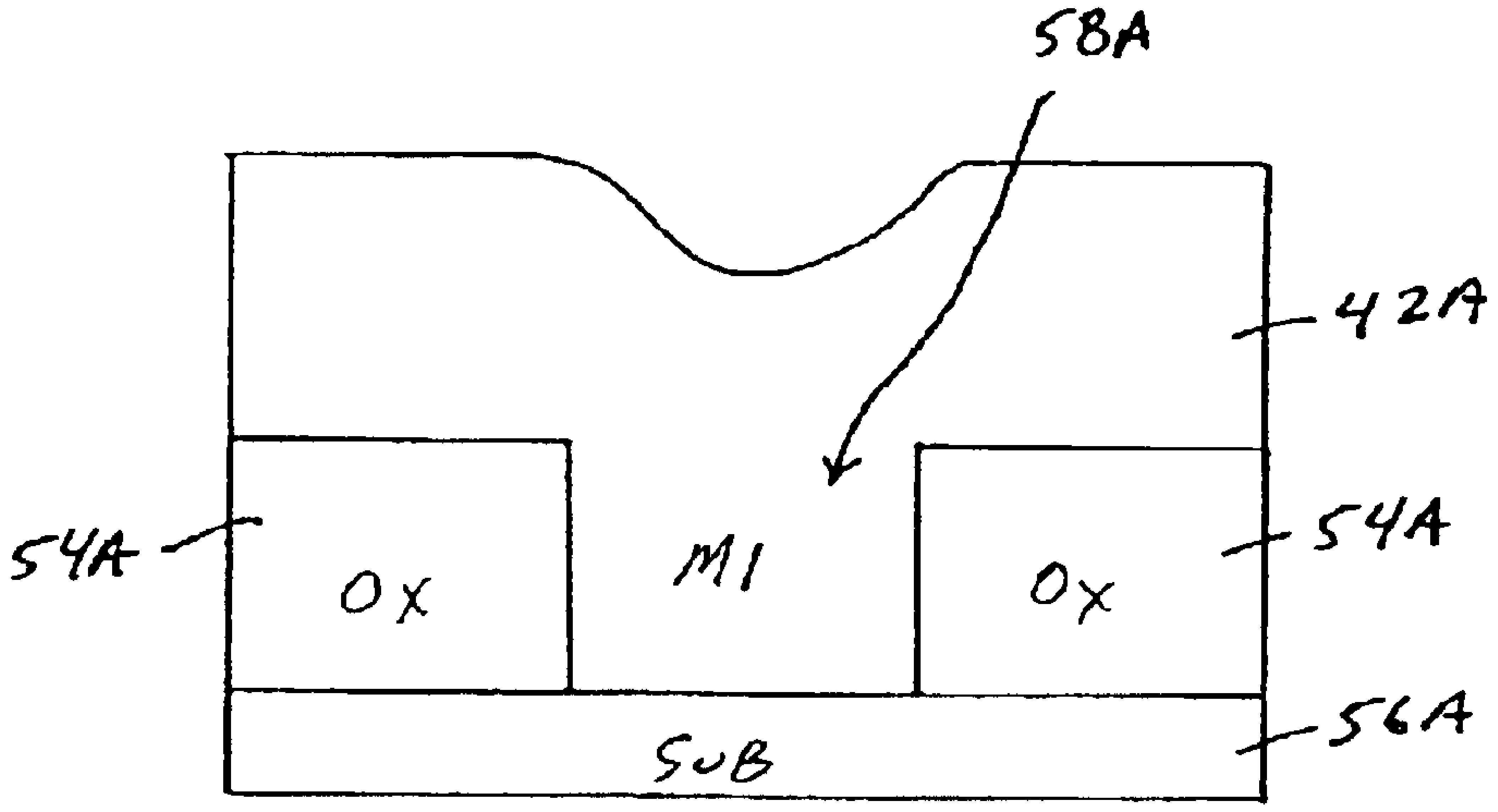

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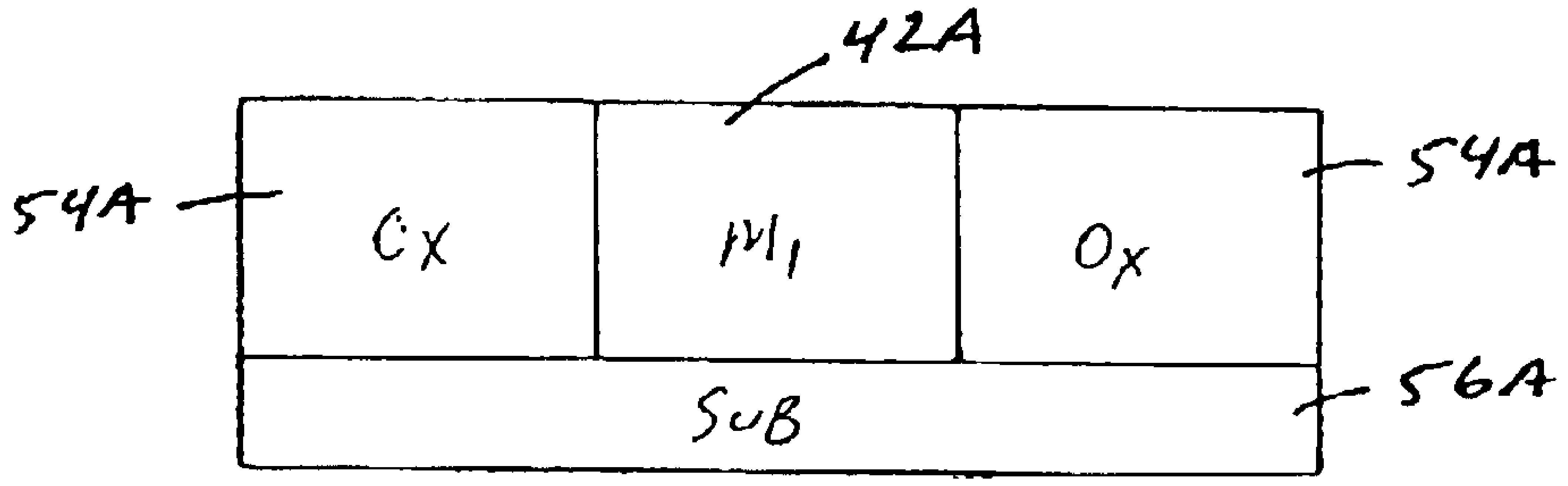

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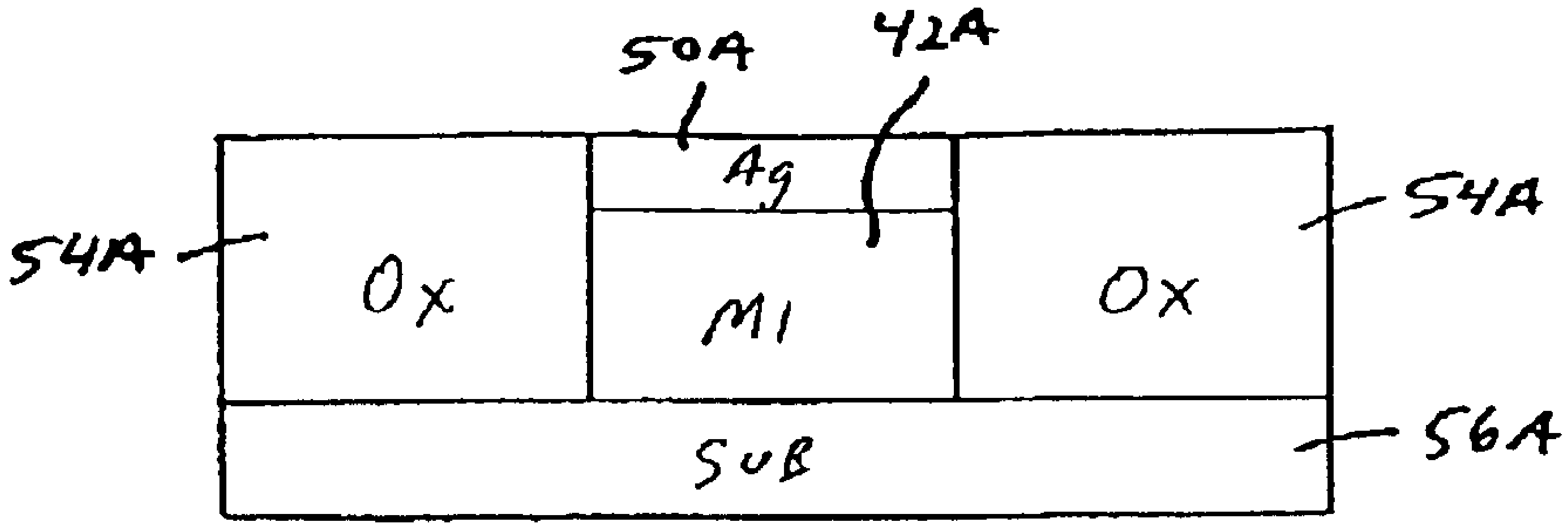
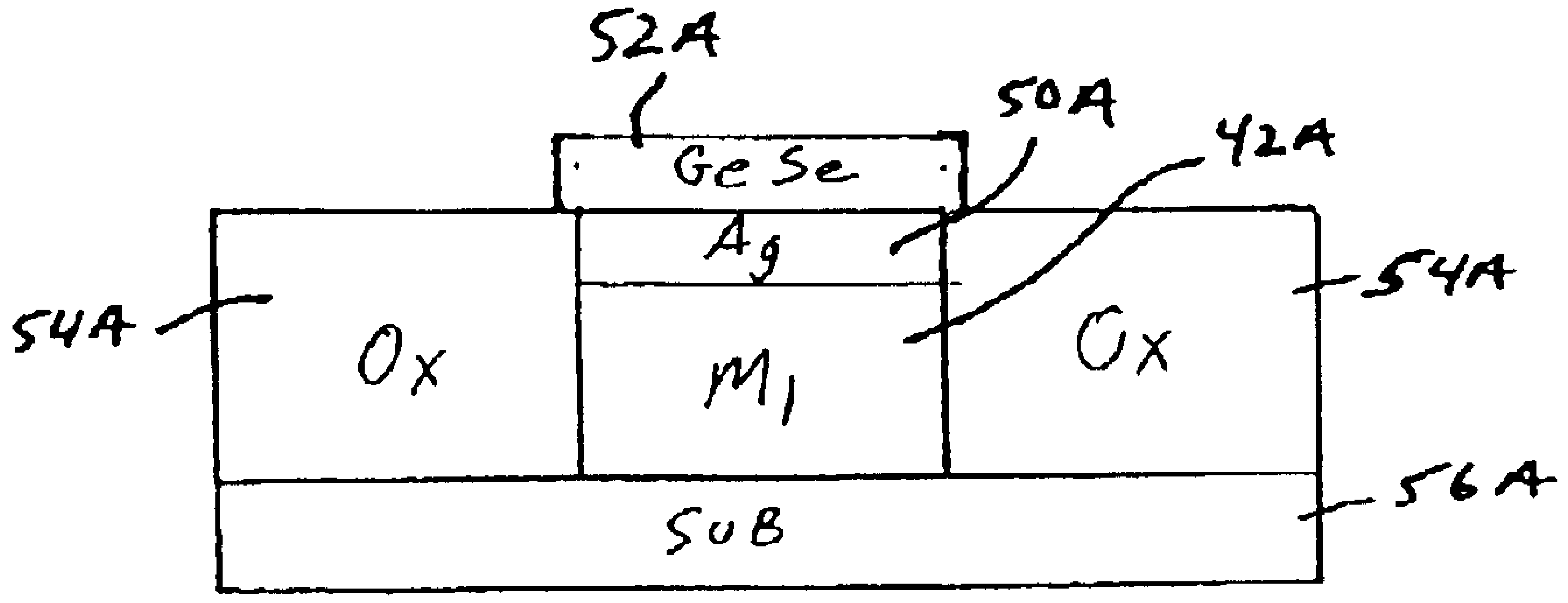


FIG. 7



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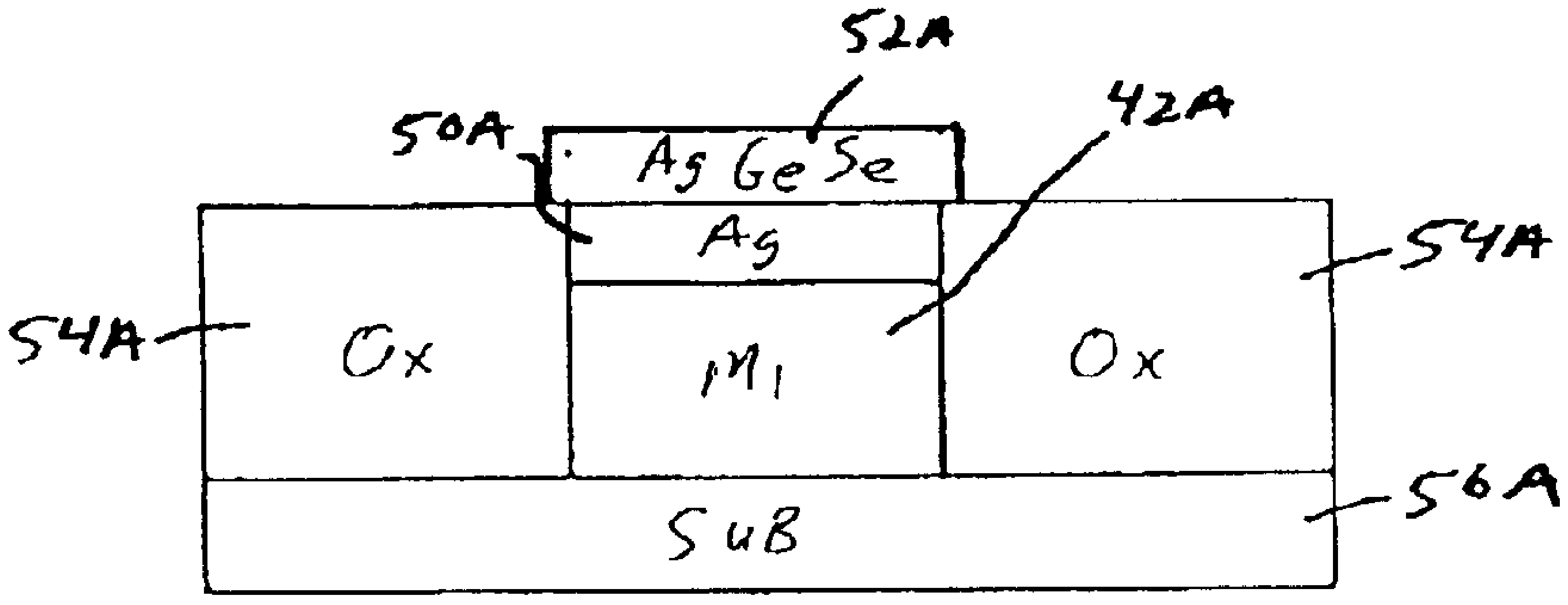

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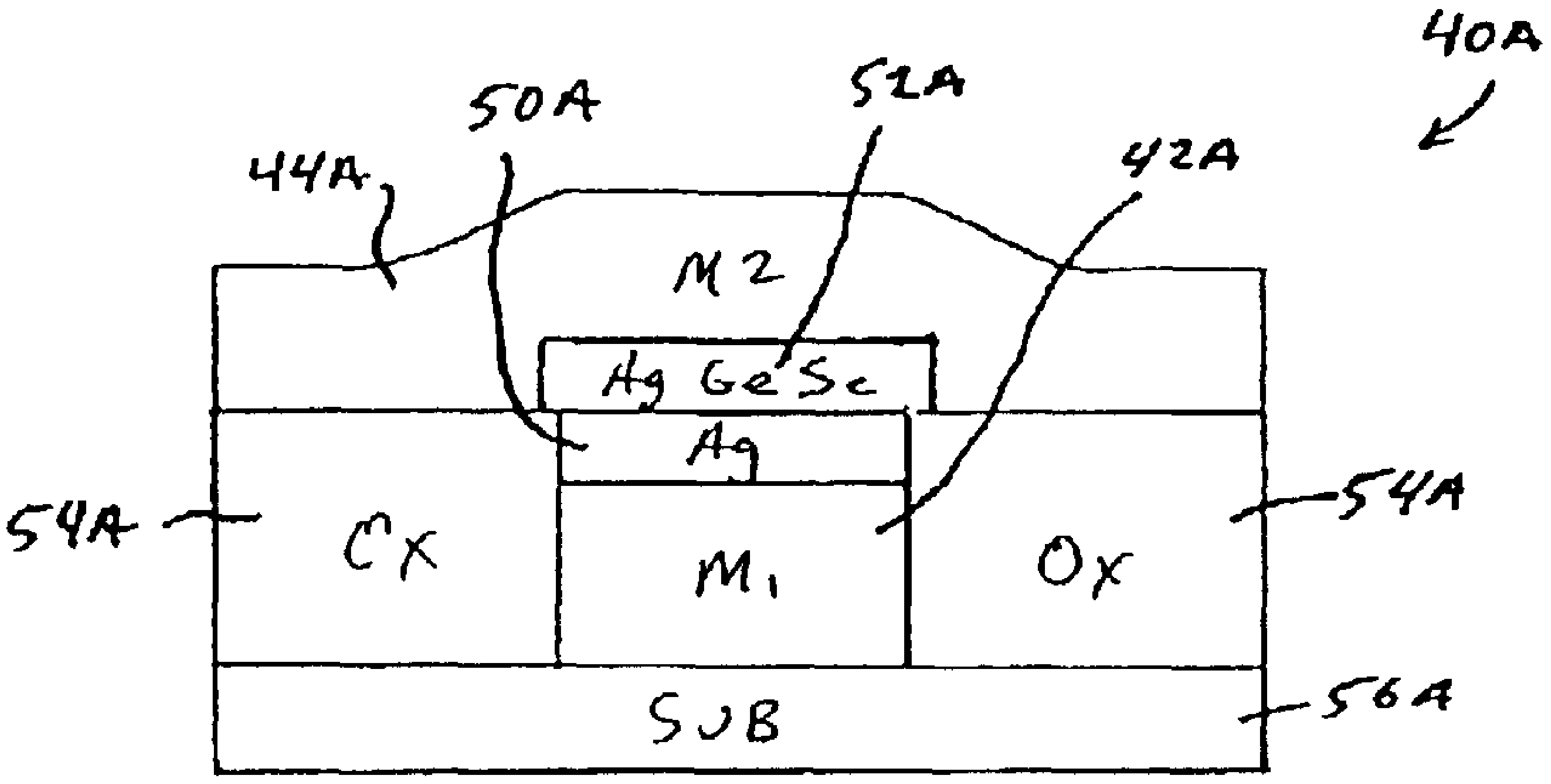

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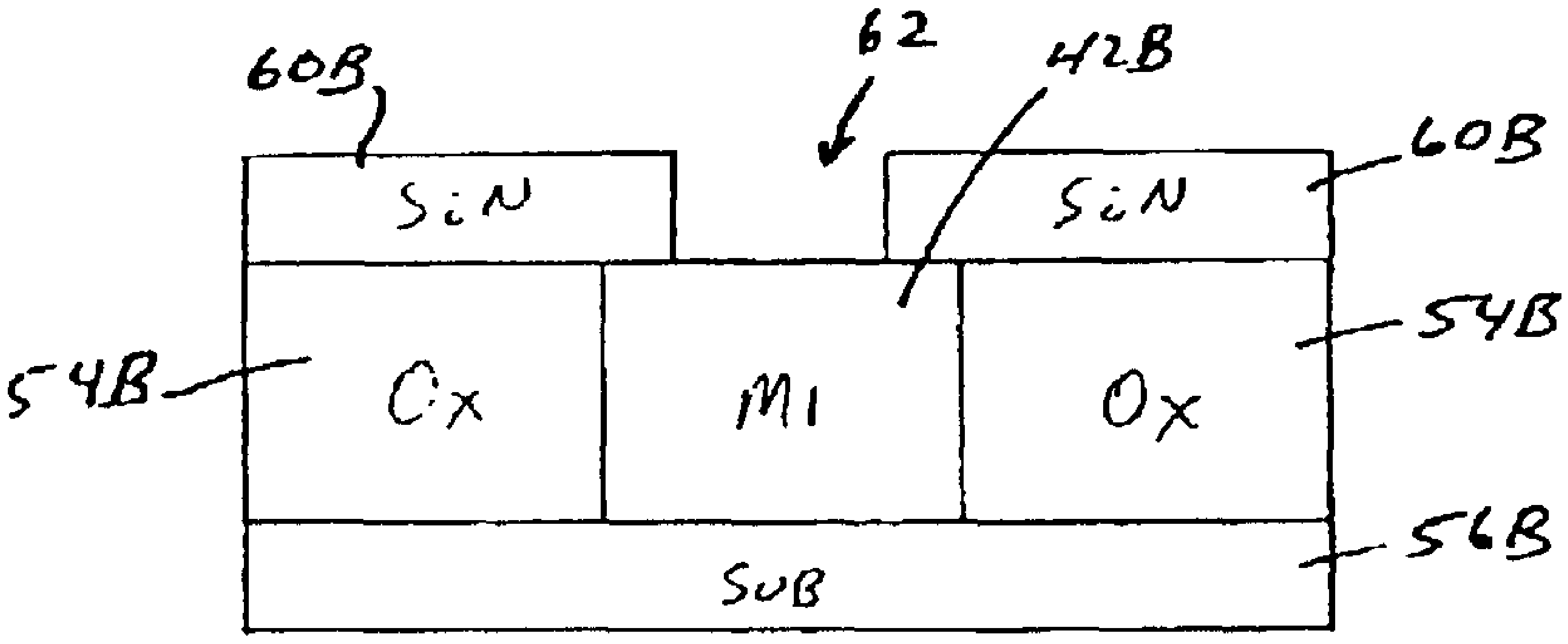

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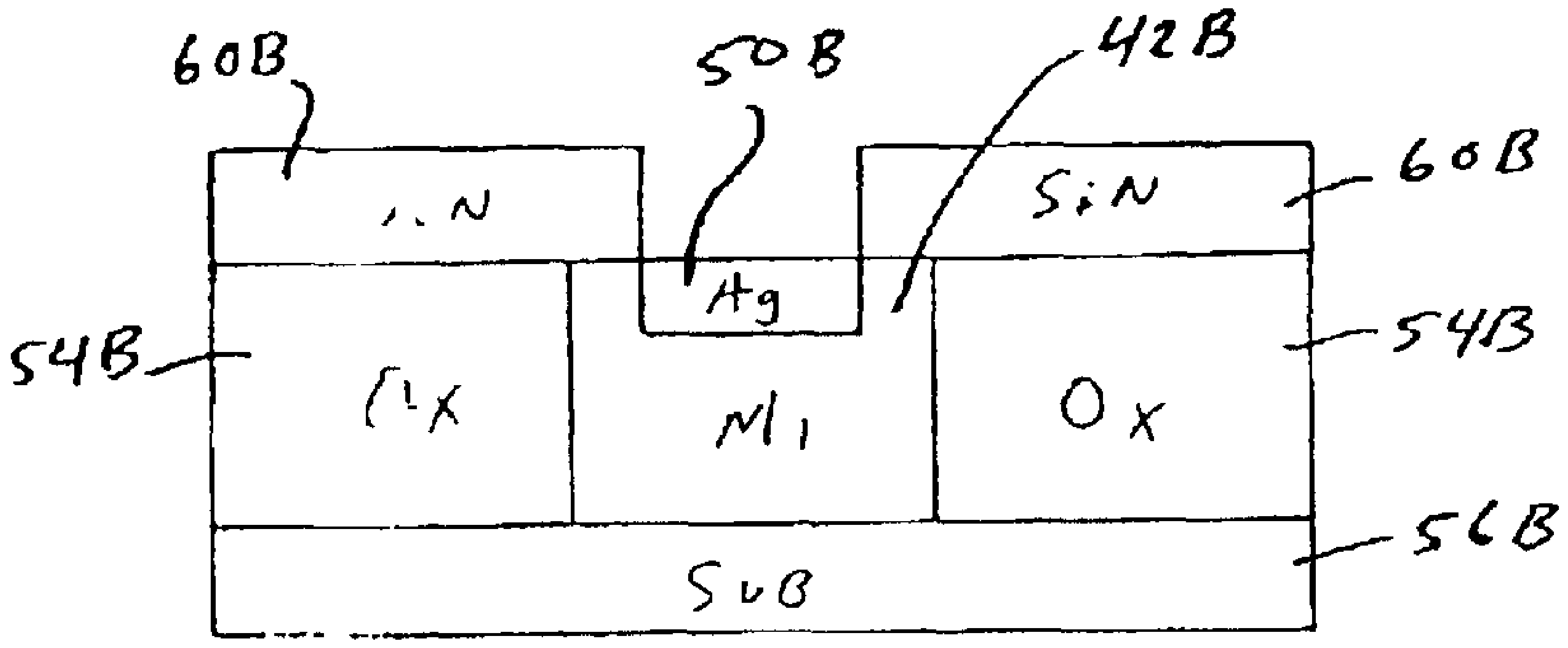

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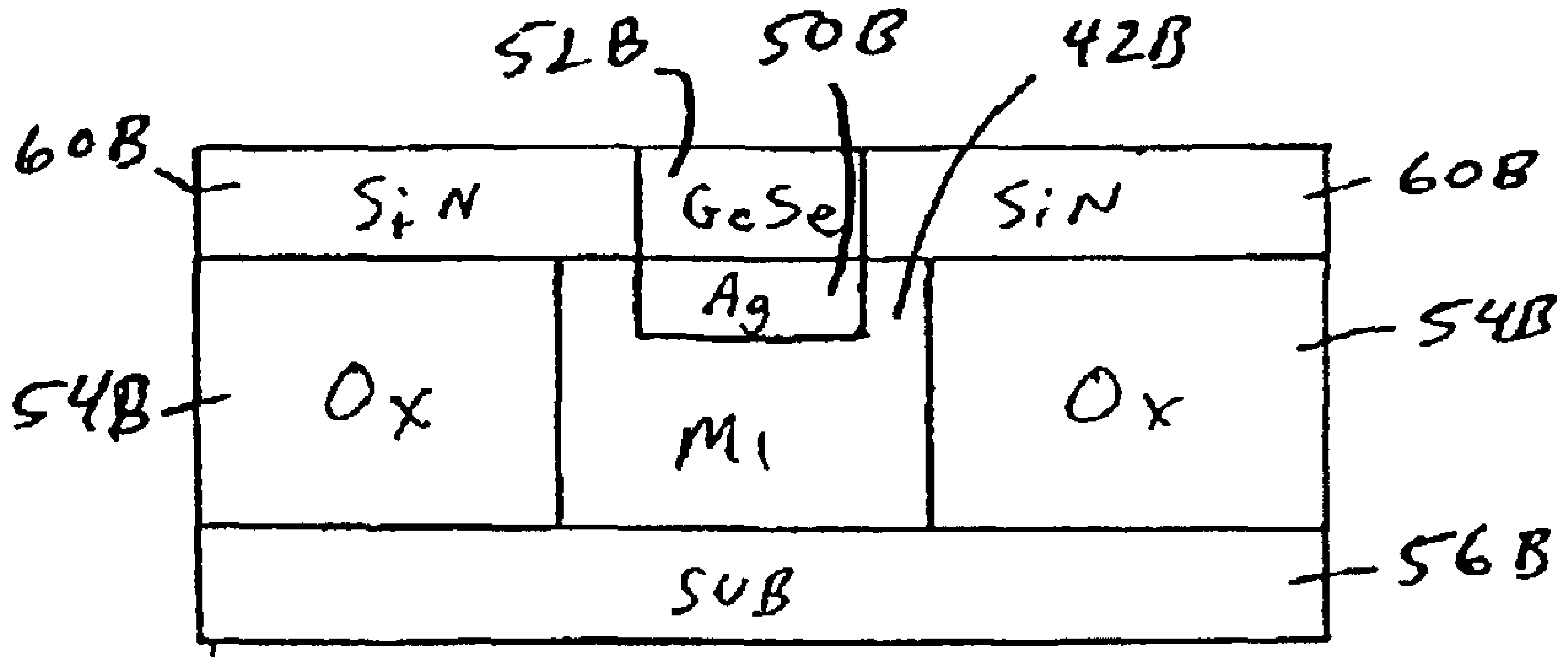


FIG. 13

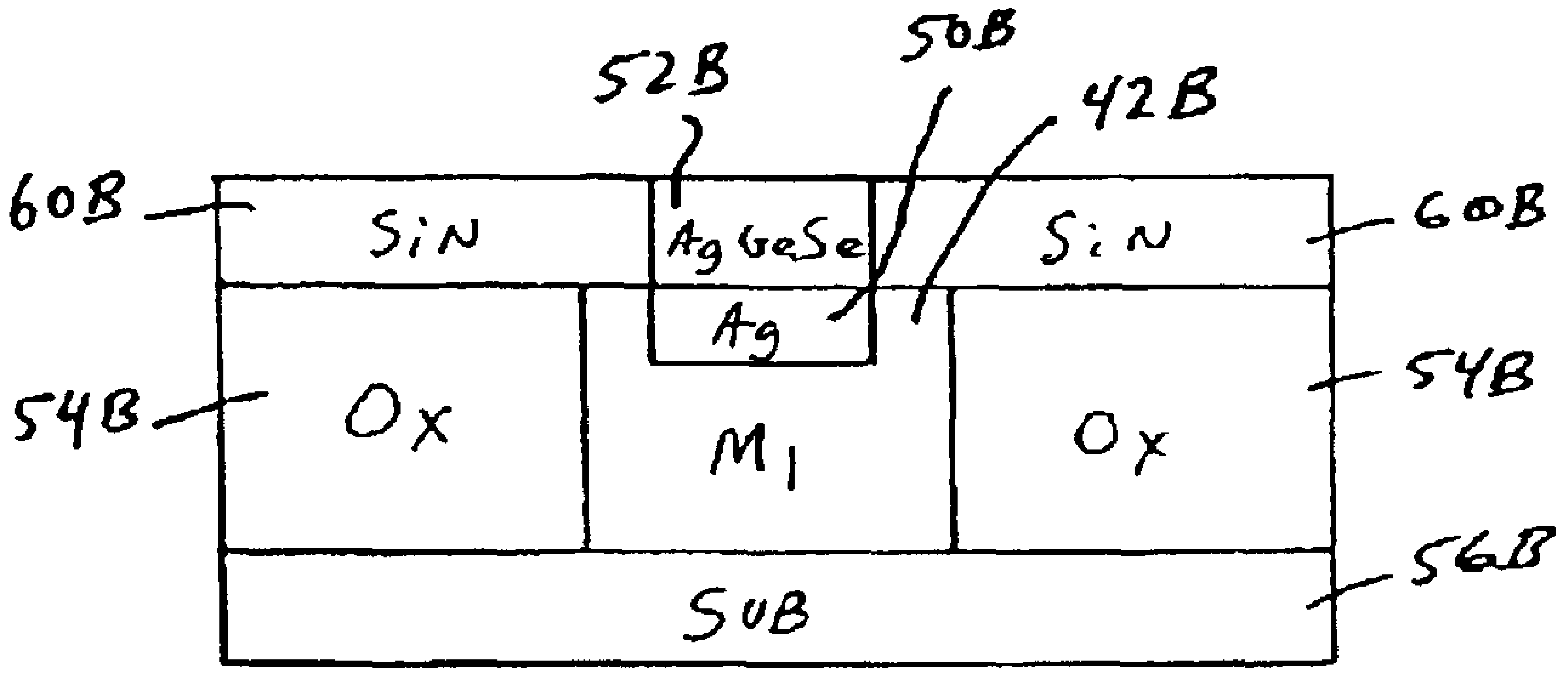


FIG. 14

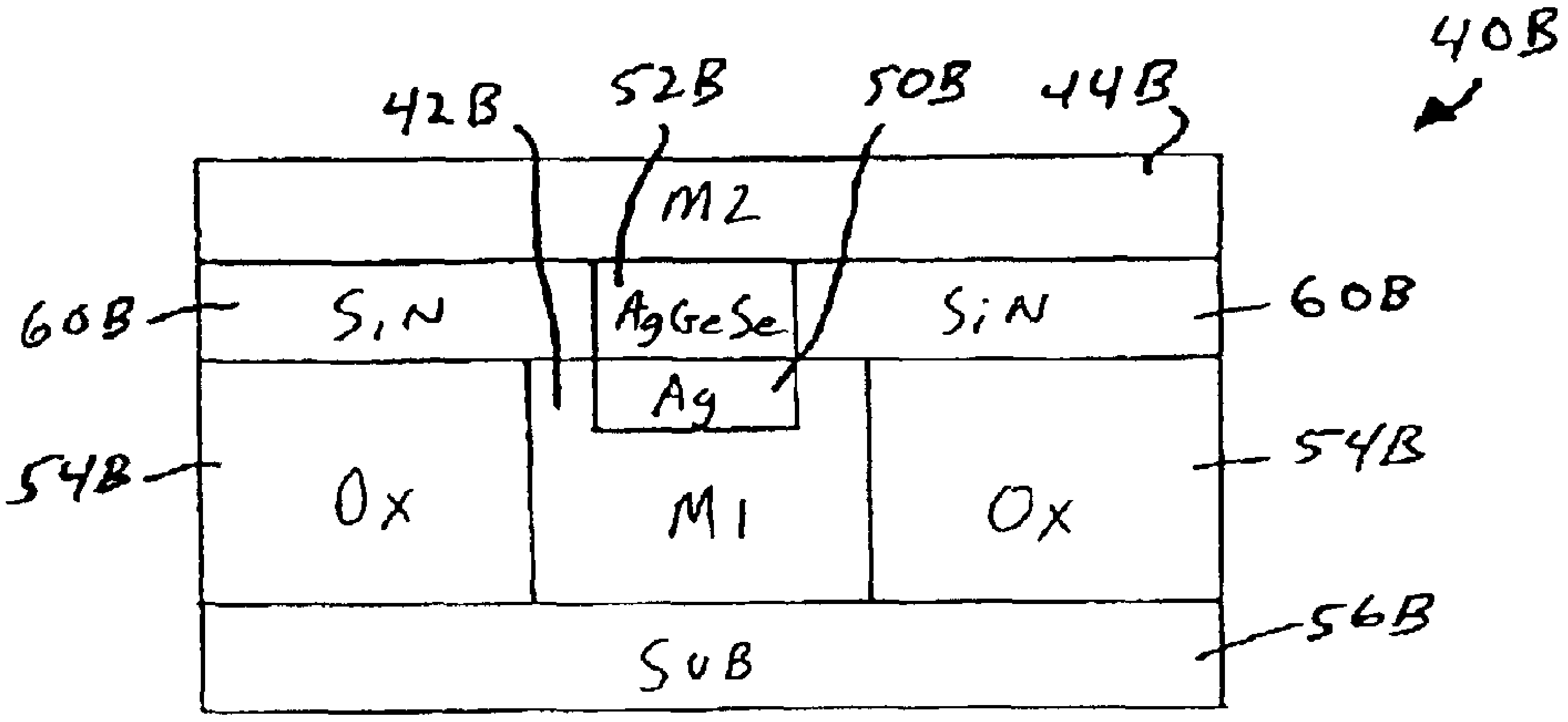
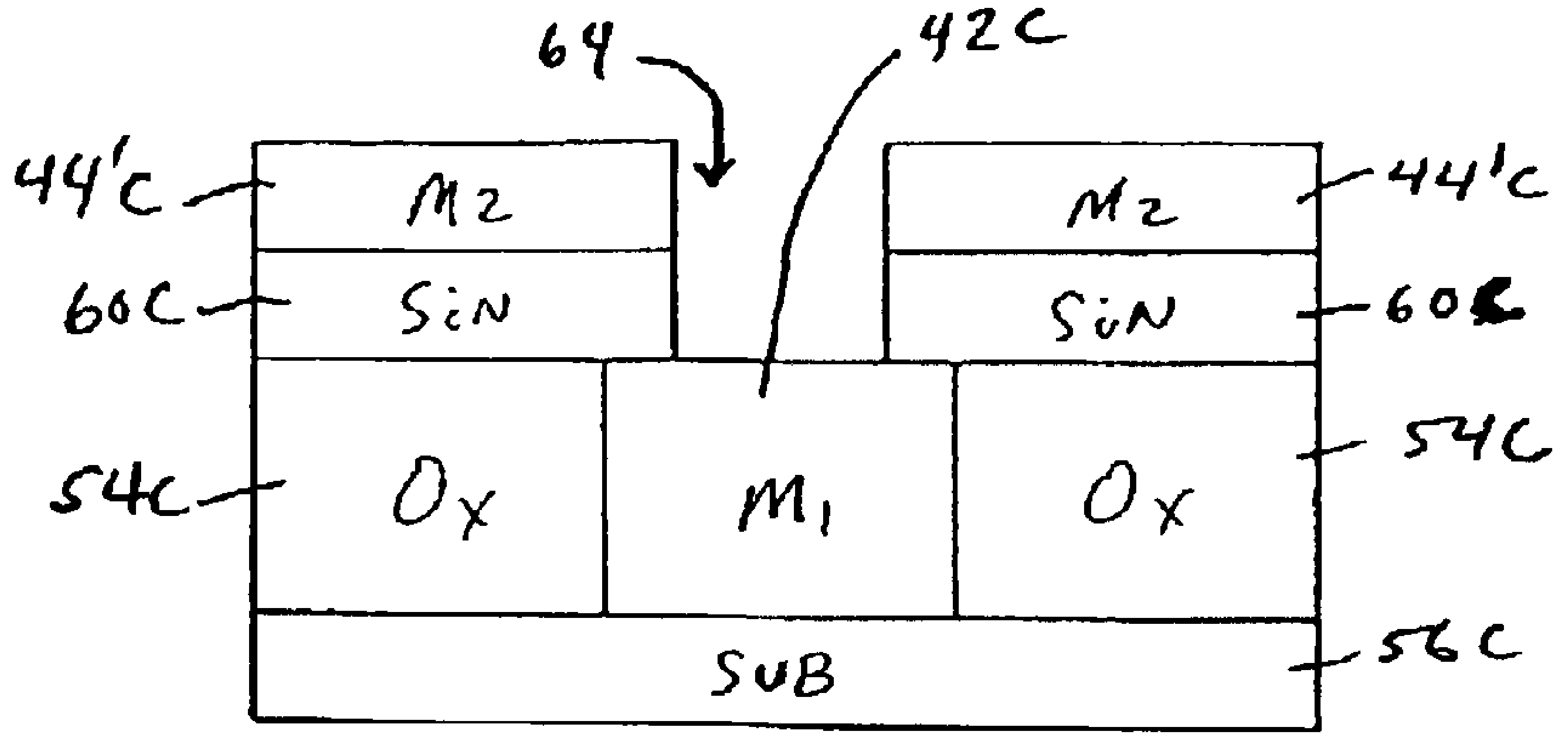


FIG. 15



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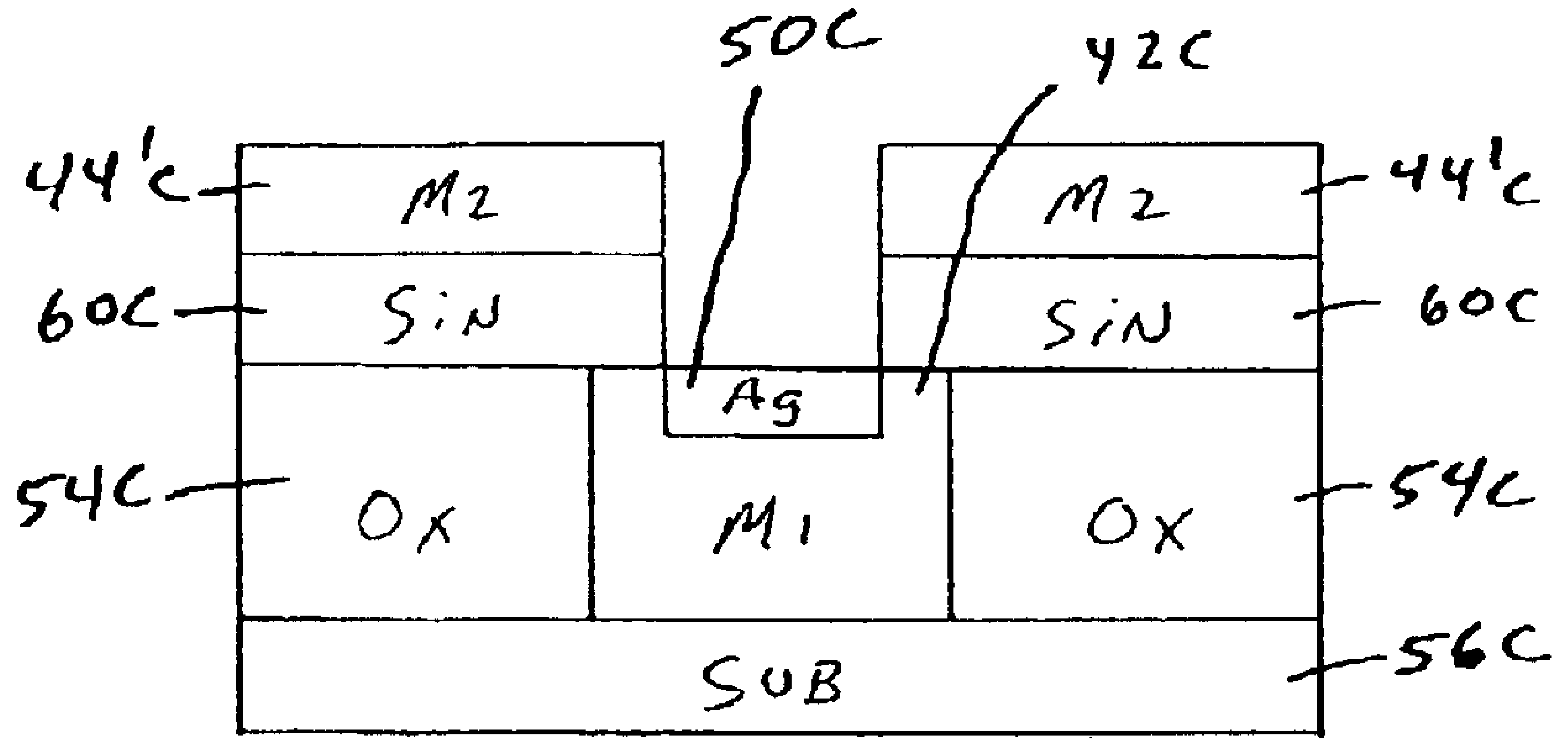


FIG. 17

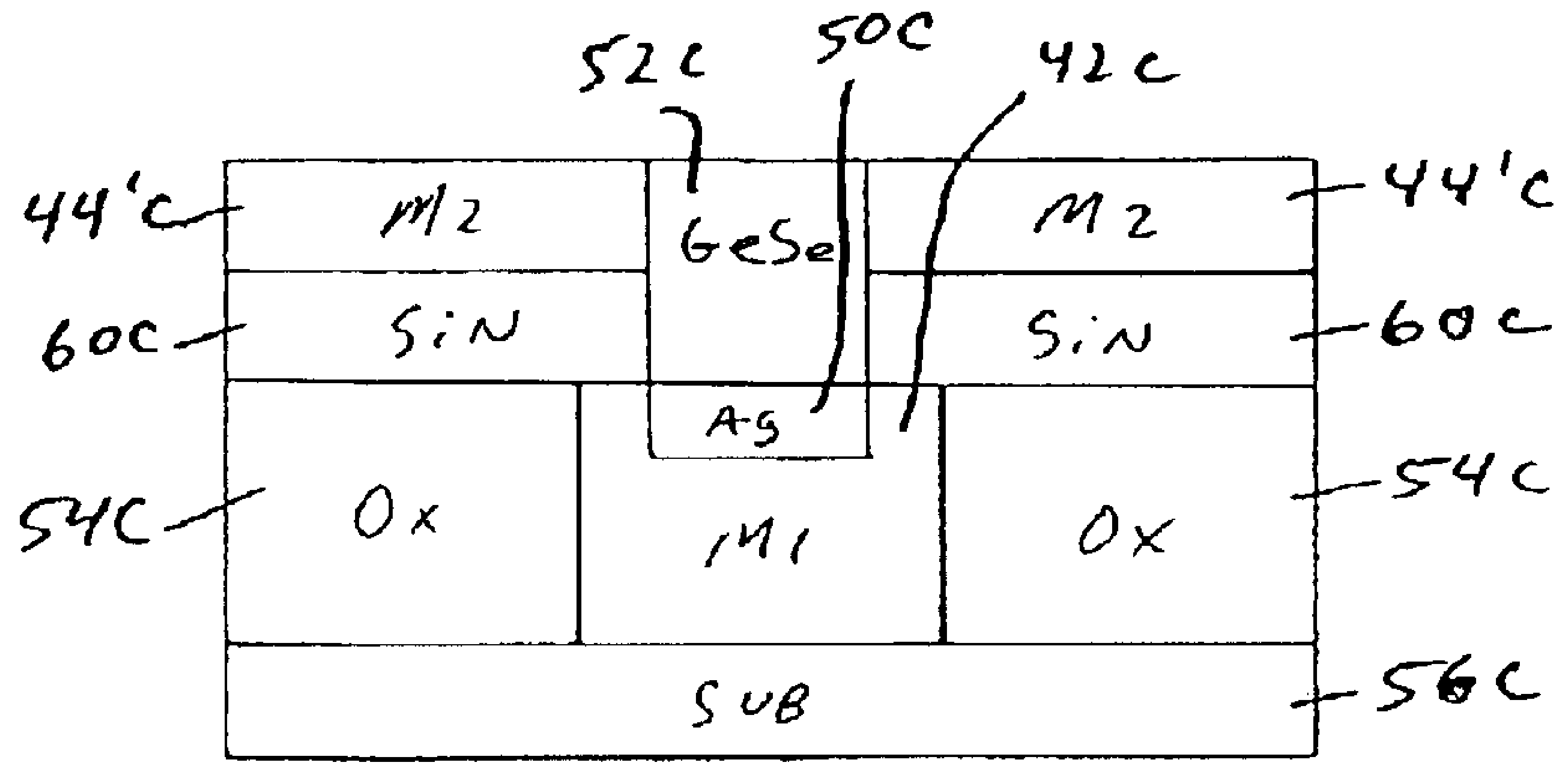
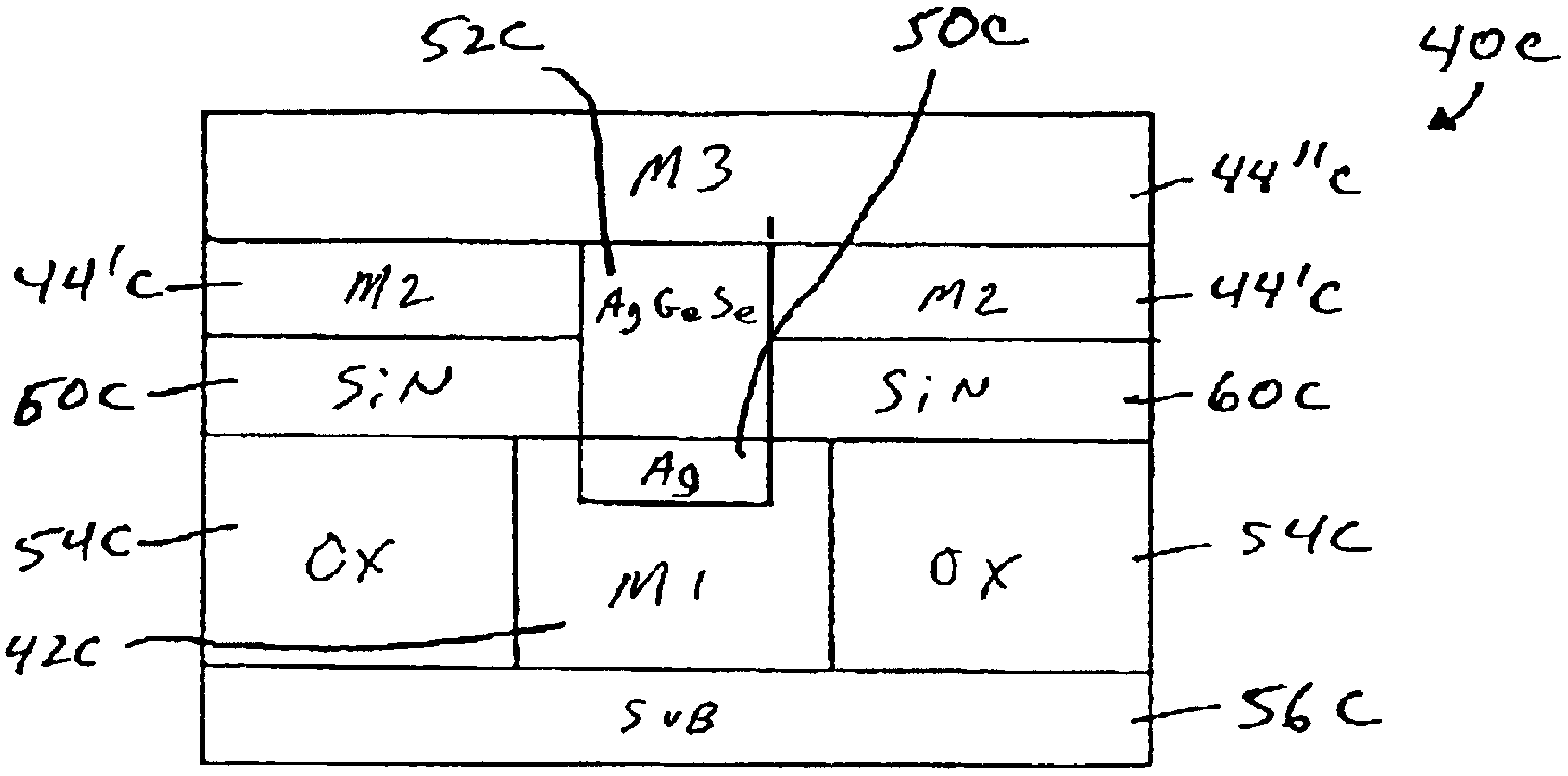


FIG. 18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60c
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60c
Ag
54c
OX
M1
OX
54c
42c
SuB
56c

FIG. 19

PCRAM MEMORY CELL AND METHOD OF MAKING SAME

This application is a continuation of Ser. No. 09/853,233 filed May 11, 2001.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates generally to the field of semiconductor devices and fabrication and, more particularly, to memory elements and methods for making memory elements.

2. Background of the Related Art

This section is intended to introduce the reader to various aspects of art which may be related to various aspects of the present invention that are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

Microprocessor-controlled integrated circuits are used in a wide variety of applications. Such applications include personal computers, vehicle control systems, telephone networks, and a host of consumer products. As is well known, microprocessors are essentially generic devices that perform specific functions under the control of a software program. This program is stored in one or more memory devices that are coupled to the microprocessor. Not only does the microprocessor access memory devices to retrieve the program instructions, but it also stores and retrieves data created during execution of the program in one or more memory devices.

There are a variety of different memory devices available for use in microprocessor-based systems. The type of memory device chosen for a specific function within a microprocessor-based system depends largely upon what features of the memory are best suited to perform the particular function. For instance, volatile memories, such as dynamic random access memories (DRAMs), must be continually powered in order to retain their contents, but they tend to provide greater storage capability and programming options and cycles than non-volatile memories, such as read only memories (ROMs). While non-volatile memories that permit limited reprogramming exist, such as electrically erasable and programmable "ROMs," all true random access memories, i.e., those memories capable of 10^{14} programming cycles are more, are volatile memories. Although one time programmable read only memories and moderately reprogrammable memories serve many useful applications, a true nonvolatile random access memory (NVRAM) would likely be needed to surpass volatile memories in usefulness.

Efforts have been underway to create a commercially viable memory device that is both random access and nonvolatile using structure changing memory elements, as opposed to the charge storage memory elements used in most commercial memory devices. The use of electrically writable and erasable phase change materials, i.e., materials which can be electrically switched between generally amorphous and generally crystalline states or between different resistive states while in crystalline form, in memory applications is known in the art and is disclosed, for example, in U.S. Pat. No. 5,296,716 to Ovshinsky et al. The Ovshinsky patent contains a discussion of the general theory of operation of chalcogenide materials, which are a particular type of structure changing material.

As disclosed in the Ovshinsky patent, such phase change materials can be electrically switched between a first structural state, in which the material is generally amorphous, and a second structural state, in which the material has a generally crystalline local order. The material may also be electrically switched between different detectable states of local order across the entire spectrum between the completely amorphous and the completely crystalline states. In other words, the switching of such materials is not required to take place in a binary fashion between completely amorphous and completely crystalline states. Rather, the material may be switched in incremental steps reflecting changes of local order to provide a "gray scale" represented by a multiplicity of conditions of local order spanning the spectrum from the completely amorphous state to the completely crystalline state.

These memory elements are monolithic, homogeneous, and formed of chalcogenide material typically selected from the group of Te, Se, Sb, Ni, and Ge. This chalcogenide material exhibits different electrical characteristics depending upon its state. For instance, in its amorphous state the material exhibits a higher resistivity than it does in its crystalline state. Such chalcogenide materials may be switched between numerous electrically detectable conditions of varying resistivity in nanosecond time periods with the input of picojoules of energy. The resulting memory element is truly non-volatile. It will maintain the integrity of the information stored by the memory cell without the need for periodic refresh signals, and the data integrity of the information stored by these memory cells is not lost when power is removed from the device. The memory material is also directly overwritable so that the memory cells need not be erased, i.e., set to a specified starting point, in order to change information stored within the memory cells. Finally, the large dynamic range offered by the memory material theoretically provides for the gray scale storage of multiple bits of binary information in a single cell by mimicking the binary encoded information in analog form and, thereby, storing multiple bits of binary encoded information as a single resistance value in a single cell.

Traditionally, the operation of chalcogenide memory cells requires that a region of the chalcogenide memory material, called the "active region," be subjected to a current pulse to change the crystalline state of the chalcogenide material within the active region. Typically, a current density of between about 10^5 and 10^7 amperes/cm^2 is needed. To obtain this current density in a commercially viable device having at least one million memory cells, for instance, one theory suggests that the active region of each memory cell should be made as small as possible to minimize the total current drawn by the memory device.

However, such traditional chalcogenide memory cells have evolved into what is referred to as a programmable metallization cell or a plated chalcogenide memory cell for use in a plated chalcogenide random access memory (PCRAM) device. Such a cell includes a chalcogenide material between opposing electrodes. A fast ion conductor material is incorporated into the chalcogenide material. The resistance of such material can be changed between highly resistive and highly conductive states.

To perform a write operation with the memory cell in its normal high resistive state, a voltage potential is applied to a certain one of the electrodes, with the other of the electrode being held at zero voltage or ground. The electrode having the voltage applied to it functions as an anode, while the electrode held at zero or ground functions as a cathode. The nature of the fast ion conductor material is such that it undergoes a chemical and structural change at a certain applied voltage level. Specifically, at some suitable threshold voltage, the metal ions within the chalcogenide material begin to plate on the cathode and progress through the chalcogenide material toward the anode. The process continues until a conductive dendrite or filament extends between the electrodes, effectively interconnecting the top and bottom electrodes to create an electrical short circuit.

Once this occurs, dendrite growth stops, and the dendrite is retained when the voltage potentials are removed. This results in the resistance of the chalcogenide material between the electrodes dropping by a factor of about 1,000. The material can be returned to its highly resistive state by reversing the voltage potential between the anode and cathode to cause the dendrite to disappear. Again, the highly resistive state is maintained when the reverse voltage potential is removed. Accordingly, such a device can, for example, function as a reprogrammable memory cell of non-volatile random access memory circuit.

As mentioned above, the variable resistance material disposed between the electrodes typically is a chalcogenide material having metal ions diffused therein. A specific example is germanium selenide with silver ions. Typically, to provide the silver ions within the germanium selenide material, germanium selenide is deposited onto the first electrode using chemical vapor deposition. A thin layer of silver is then deposited on the glass, for example by physical vapor deposition or another technique. The layer of silver is then irradiated with ultraviolet radiation. The thin nature of the deposited silver allows the energy to pass through the silver to the silver/glass interface to cause the silver to diffuse into the chalcogenide material. The applied energy and overlying silver result in the silver migrating into the glass layer such that a homegenous distribution of silver throughout the layer is ultimately achieved.

Unfortunately, chalcogenide materials are relatively delicate. The nature of the deposition technique used to deposit the silver can damage the chalcogenide material, and, thus, adversely affect the resulting memory cell. Furthermore, it can be challenging to etch and polish chalcogenide materials. Accordingly, it would be desirable to develop memory cell fabrication methods that avoid steps that can damage such materials.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

FIG. **1** illustrates a block diagram of an exemplary processor-based device;

FIG. **2** illustrates an exemplary memory device;

FIG. **3** illustrates a more detailed view of the memory array of the memory device illustrated in FIG. **2**;

FIGS. **4**–**10** illustrate cross-sectional views of a memory cell during different stages of fabrication;

FIGS. **11**–**15** illustrate cross-sectional views of an alternate embodiment of a memory cell during different stages of fabrication; and

FIGS. **16**–**19** illustrate cross-sectional views of another alternate embodiment of a memory cell during different stages of fabrication.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Specific embodiments of microprocessor-based systems, memories, memory elements, and methods of making such memory elements are described below as they might be implemented for use in semiconductor memory circuits. In the interest of clarity, not all features of an actual implementation are described in this specification. It should be appreciated that in the development of any such actual implementation, as in any engineering project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill having the benefit of this disclosure.

Turning now to the drawings, and referring initially to FIG. **1**, a block diagram depicting an exemplary processor-based device, generally designated by the reference numeral **10**, is illustrated. The device **10** may be any of a variety of different types, such as a computer, pager, cellular telephone, personal organizer, control circuit, etc. In a typical processor-based device, one or more processors **12**, such as a microprocessor(s), control many of the functions of the device **10**.

The device **10** typically includes a power supply **14**. For instance, if the device **10** is portable, the power supply **14** would advantageously include permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **14** may also include an A/C adapter, so that the device may be plugged into a wall outlet, for instance. In fact, the power supply **14** may also include a D/C adapter, so that the device **10** may be plugged into a vehicle's cigarette lighter, for instance.

Various other devices may be coupled to the processor(s) **12**, depending upon the functions that the device **10** performs. For instance, a user interface **16** may be coupled to the processor(s) **12**. The user interface **16** may include an input device, such as buttons, switches, a keyboard, a light pin, a mouse, and/or a voice recognition system, for instance. A display **18** may also be coupled to the processor(s) **12**. The display **18** may include an LCD display, a CRT, LEDs, and/or an audio display. Furthermore, an RF subsystem/baseband processor **20** may also be coupled to the processor(s) **12**. The RF subsystem/baseband processor **20** may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). A communication port **22** may also be coupled to the processor(s) **12**. The communication port **22** may be adapted to be coupled to a peripheral device **24**, such as a modem, a printer, or a computer, for instance, or to a network, such as a local area network or the Internet.

Because the processor(s) **12** controls the functioning of the device **10** generally under the control of software programming, memory is coupled to the processor(s) **12** to store and facilitate execution of the software program. For instance, the processor(s) **12** may be coupled to volatile memory **26**, which may include dynamic random access memory (DRAM), static random access memory (SRAM), Double Data Rate (DDR) memory, etc. The processor(s) **12** may also be coupled to non-volatile memory **28**. The non-volatile memory **28** may include a read only memory (ROM), such as an EPROM or Flash Memory, to be used in conjunction with the volatile memory. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. The volatile memory, on the other hand, is typically quite large so that it can store dynamically loaded applications. Additionally, the non-volatile memory **28** may include a high capacity memory such as a disk drive, tape drive memory, CD ROM drive, DVD, read/write CD ROM drive, and/or a floppy disk drive.

An exemplary memory device is illustrated in FIG. **2** and generally designated by a reference numeral **30**. The memory device **30** is an integrated circuit memory that is advantageously formed on a semiconductor substrate **32**. The memory device **30** includes a memory matrix or array **34** that includes a plurality of memory cells for storing data, as described below. The memory matrix **34** is coupled to periphery circuitry **36** by the plurality of control lines **38**. The periphery circuitry **36** may include circuitry for addressing the memory cells contained within the memory matrix **34**, along with circuitry for storing data in and retrieving data from the memory cells. The periphery circuitry **36** may also include other circuitry used for controlling or otherwise insuring the proper functioning of the memory device **30**.

A more detailed depiction of the memory matrix **34** is illustrated in FIG. **3**. As can be seen, the memory matrix **34** includes a plurality of memory cells **40** that are arranged in generally perpendicular rows and columns. The memory cells **40** in each row are coupled together by a respective word line **42**, and the memory cells **40** in each column are coupled together by a respective digit line **44**. Specifically, each memory cell **40** includes a word line node **46** that is coupled to a respective word line **42**, and each memory cell **40** includes a digit line node **48** that is coupled to a respective digit line **44**. The conductive word lines **42** and digit lines **44** are collectively referred to as address lines. These address lines are electrically coupled to the periphery circuitry **36** so that each of the memory cells **40** can be accessed for the storage and retrieval of information.

Turning now to FIGS. **4**–**10**, a first exemplary embodiment of a memory cell **40** will be described. FIG. **10** illustrates the finished memory cell **40**A, and FIGS. **4**–**9** illustrate the memory cell **40**A at various stages of fabrication. The suffix "A" is used in describing this first embodiment for clarity so that similar reference numerals may be used to describe subsequent embodiments. As illustrated in FIG. **10**, the finished memory cell **40**A includes a word line **42**A, which is often referred to as a Metal 1 (M1) layer. The word line **42**A has a layer of conductive material **50**A, such as silver (Ag), disposed thereon. A layer of chalcogenide material **52**A, such as germanium selenide (GeSe), having metal ions diffused therein is disposed over the conductive layer **50**A. The metal ions diffused in the chalcogenide material **52**A typically originate in the layer of conductive material **50**A. The digit line **44**A, often referred to as a Metal 2 (M2) layer, is disposed over the chalcogenide layer **52**A. Each memory cell **40**A is typically isolated from adjacent memory cells by oxide regions **54**A, and each memory cell **40**A is typically fabricated on a substrate **56**A.

One method of fabricating the memory cell **40**A is disclosed with reference to the various stages of fabrication illustrated in FIGS. **4**–**9**. Referring first to FIG. **4**, a substrate **56**A is typically used as a base upon which the memory cells **40**A of the memory array **44** are formed. In this discussion, the substrate **56**A is generally used in a generic sense, because it is possible for the substrate **56**A to take various forms depending upon the nature of the circuit design. For example, the substrate **56**A may be a suitable semiconductor substrate, such as silicon or galium arsenide, or a suitable dielectric substrate, such as PECVD silicon dioxide. Furthermore, the substrate **56**A may include layers, devices, and/or structures upon which or around which the memory cells **40**A may be fabricated.

A layer of dielectric material **54**A, for example an oxide such as silicon dioxide, is formed over the substrate **56**A, as illustrated in FIG. **5**. The layer of dielectric material **54**A may be formed by any suitable process, such as by chemical vapor deposition. A window **58**A is formed in the layer of dielectric material **54**A. The window may extend partially through the layer of dielectric material **54**A, or completely through the layer of dielectric material **54**A to the substrate **56**A, as illustrated in FIG. **5**. The window **58**A may be formed by any suitable process, such as by the use of standard photolithographic techniques.

As illustrated in FIGS. **5** and **6**, a layer of conductive material is deposited into the window **58**A and planarized to form the word line **42**A. Again, any suitable deposition technique, such as sputtering, and any suitable planarization technique, such as chemical mechanical planarization (CMP), may be used. The conductive material used to form the word line **42**A is typically a metal, such as copper, tungsten, nickel, or aluminum. Although the word line **42**A is illustrated as being formed in a dielectric material **54**A in this embodiment, it should be appreciated that the word line **42**A may be formed in other manners as well. For example, the word line **42**A may be buried in the substrate **56**A.

A fast ion conductive material is then disposed on the word line **42**A. The fast ion conductive material is selected to cooperate with a subsequently applied layer of chalcogenide material to form the memory element of the memory cell **40**A. In this embodiment, the word line **42**A is plated with the conductive material **50**A using an immersion plating process. In general, immersion plating replaces a less noble metal with a more noble metal. It is an ion exchange process that requires neither external electricity nor a catalyst. Immersion plating can be used in a self-limiting process, and it usually plates thinner films than other plating methods. Immersion plating depends on the base metal, i.e., the less noble metal. Many factors can influence immersion plating, such as the type of ligand used to take up the base metal and to keep the base metal in solution.

In this exemplary embodiment, the base metal of the word line **42**A is selected to be copper, and the more noble metal of the conductive layer **50**A is selected to be silver. Of course, it should be recognized that other base metals, such as nickel, aluminum, or tungsten, for example, may be used in place of copper, and that alloys of such metals may be used as well. In addition, various "more noble" metals, such as gold, may be used in place of silver. However, for the purposes of this exemplary embodiment utilizing copper and silver, a silver immersion solution called "argentomerse" available from Technic, Inc. may be used. This silver immersion solution utilizes a cyanide salt chemistry, which essentially represents a general purpose immersion plating solution. A silver immersion solution such as argentomerse should suffice for plating silver on base metals such as nickel or copper. However, for immersion plating of silver on tungsten, it may be desirable to utilize another silver immersion solution in order to optimize the chemistry. The structure illustrated in FIG. **6** is immersed in the silver immersion solution for a sufficient amount of time to form the layer of conductive material **50**A. For example, the structure may be immersed in the solution for 15 to 30 minutes to form the conductive layer **50**A having a thickness of 500A to 2000A.

After the conductive layer **50**A has been formed on the word line **42**A, a layer of chalcogenide material **52**A, such as germanium selenide, may be formed over the conductive layer **50**A, as illustrated in FIG. **8**. The layer of chalcogenide material **52**A may be formed by any suitable process, such as chemical vapor deposition. The layer of chalcogenide material **52**A may have a thickness in the range of 200A to 800A, for example.

Once the layer of chalcogenide material **52**A is formed over the layer of conductive material **50**A, the structure illustrated in FIG. **8** is processed in a manner that causes at least a portion of the material in the conductive layer **50**A to migrate into the layer of chalcogenide material **52**A. In this embodiment, the structure illustrated in FIG. **8** is subjected to ultraviolet radiation and heat to cause silver atoms in the layer of conductive material **50**A to migrate into the layer of chalcogenide material **52**A. For example, the structure in FIG. **8** may be submitted to ultraviolet radiation in the range of 160 nm to 904 nm, e.g., 405 nm, at an intensity of 10 microjoules to 10 millijoules for a period of 5 to 30 minutes, and heat at a temperature of 50 to 85 degrees Celsius for a period of 5 to 20 minutes. Typically, the heat cycle is performed first, followed by the UV cycle.

After this conversion process, the layer of chalcogenide material **52**A has metal ions in it, as illustrated in FIG. **9**. Then, the Metal 2 (M2) layer, which forms the digit line **44**A, may be disposed over the layer of chalcogenide material **52**A, as illustrated in FIG. **10**, to complete the memory cell **40**A.

It should be appreciated from the discussion of the structure and method of fabrication of the memory cell **40**A that it represents an inverted PCRAM memory cell. As discussed previously, a typical PCRAM memory cell is fabricated by forming a layer of chalcogenide material on the Metal 1 layer, thus requiring the conductive layer, such as silver, to be disposed on the chalcogenide layer. However, because chalcogenide is a very delicate material as discussed previously, known methods of depositing silver on chalcogenide are difficult to control in a reliable and repeatable fashion. However, by inverting the traditional PCRAM memory cell so that the conductive layer, such as silver, is disposed on the Metal 1 layer, the delicate nature of the subsequently deposited chalcogenide material does not pose a problem.

FIGS. **11**–**15** illustrate a second embodiment of the memory cell **40**. FIG. **15** illustrates the finished memory cell **40**B, and FIGS. **11**–**14** illustrate the memory cell **40**B at various stages of fabrication. The suffix "B" is used in describing this second embodiment for clarity so that similar reference numerals may be used. As illustrated in FIG. **15**, the finished memory cell **40**B includes a word line **42**B, which is again referred to as a Metal 1 (M1) layer. The word line **42**B has a layer of conductive material **50**B, such as silver (Ag), disposed thereon. A layer of chalcogenide material **52**B, such as germanium selenide (GeSe), having metal ions diffused therein is disposed over the conductive layer **50**B. Unlike the first embodiment, the layer of conductive material **50**B and the layer of chalcogenide material **52**B are disposed in a window created in a layer of dielectric material **60**B. The digit line **44**B, again referred to as a Metal 2 (M2) layer, is disposed over the chalcogenide layer **52**B. Each memory cell **40**B is typically isolated from adjacent memory cells by oxide regions **54**B, and each memory cell **40**B is typically fabricated on a substrate **56**B.

One method of fabricating the memory cell **40**B is disclosed with reference to, the various stages of fabrication illustrated in FIGS. **11**–**14**. However, before discussing FIGS. **11**–**14**, it should be understood that the memory cell **40**B first undergoes the stages of fabrication illustrated in FIGS. **4**–**6**. Then, as illustrated in FIG. **11**, a layer of dielectric material **60**B is deposited over the structure, and a window **62** is formed in the layer of dielectric material **60**B to expose at least a portion of the underlying word line **42**B. The layer of dielectric material **60**B may be deposited in any suitable manner, such as by chemical vapor deposition, and it may include any suitable dielectric, such as silicon nitride. The thickness of the layer of dielectric material **60**B may be in the range of 200A to 1000A, for example.

A fast ion conductive material is then disposed on the portion of the word line **42**B exposed by the window **62**. The selection of the fast ion conductive material and the manner in which it may be applied does not differ from the previous embodiment. Accordingly, for the sake of clarity, in this exemplary embodiment, the base metal of the word line **42**B is selected to be copper, and the more noble metal of the conductive layer **50**B is selected to be silver. The structure illustrated in FIG. **11** is immersed in the silver immersion solution for a sufficient amount of time to form the layer of conductive material **50**B, as illustrated in FIG. **12**.

After the conductive layer **50**B has been formed on the word line **42**B, a layer of chalcogenide material **52**B, such as germanium selenide, may be deposited in the window **62** over the conductive layer **50**B, as illustrated in FIG. **13**. The layer of chalcogenide material **52**B may be formed by any suitable process, such as chemical vapor deposition. The deposited layer of chalcogenide material **52**B is then planarized, by chemical mechanical planarization for example, so that the layer of chalcogenide material **52**B remains only within the window **62**. Thus, the thickness of the layer of chalcogenide material **52**B is approximately the same as the thickness of the layer of dielectric material **60**B.

Once the layer of chalcogenide material **52**B is formed in the window **62**, the structure illustrated in FIG. **13** is processed in a manner that causes at least a portion of the material in the conductive layer **50**B to migrate into the layer of chalcogenide material **52**B. As in the previous embodiment, the structure illustrated in FIG. **13** is subjected to ultraviolet radiation and heat to cause silver atoms in the layer of conductive material **50**B to migrate into the layer of chalcogenide material **52**B.

After this conversion process, the layer of chalcogenide material **52**B has metal ions in it, as illustrated in FIG. **14**. Then, the Metal 2 (M2) layer, which forms the digit line **44**B, may be disposed over the layer of dielectric material **60**B and over the layer of chalcogenide material **52**B, as illustrated in FIG. **15**, to complete the memory cell **40**B.

FIGS. **16**–**19** illustrate a third embodiment of the memory cell **40**. FIG. **19** illustrates the finished memory cell **40**C, and FIGS. **16**–**18** illustrate the memory cell **40**C at various stages of fabrication. The suffix "C" is used in describing this third embodiment for clarity so that similar reference numerals may be used. As illustrated in FIG. **19**, the finished memory cell **40**C includes a word line **42**C, which is again referred to as a Metal 1 (M1) layer. The word line **42**C has a layer of conductive material **50**C, such as silver (Ag), disposed thereon. A layer of chalcogenide material **52**C, such as germanium selenide (GeSe), having metal ions diffused therein is disposed over the conductive layer **50**C. Unlike the previous embodiments, the layer of conductive material **50**C and the layer of chalcogenide material **52**C are disposed in a window created in a layer of dielectric material **60**C and in a layer of conductive material **44'**C. The layer of conductive material **44'**C. forms a portion of the digit line and is again referred to as a Metal 2 (M2) layer. The other portion of the digit line is formed by a layer of conductive material **44"**C, which is disposed over the chalcogenide layer **52**C and over the Metal 2 layer. The layer of conductive material **44"**C is referred to as the Metal 3 (M3) layer. Each memory cell **40**C is typically isolated from adjacent memory cells by oxide regions **54**C, and each memory cell **40**C is typically fabricated on a substrate **56**C.

One method of fabricating the memory cell **40**C is disclosed with reference to the various stages of fabrication illustrated in FIGS. **16**–**18**. However, before discussing FIGS. **16**–**18**, it should be understood that the memory cell **40**C first undergoes the stages of fabrication illustrated in FIGS. **4**–**6**. Then, as illustrated in FIG. **16**, a layer of dielectric material **60**C is deposited over the structure, and a layer of conductive material **44**'C. (the Metal 2 layer) is deposited over the layer of dielectric material **60**C. The layer of dielectric material **60**C may be deposited in any suitable manner, such as by chemical vapor deposition, and it may include any suitable dielectric, such as silicon nitride. The layer of conductive material **44**'C. may be deposited in any suitable manner, such as by sputtering, and it may include any suitable conductive material, such as platinum, aluminum, or tungsten. The thickness of the layer of dielectric material **60**C may be in the range of 200A to 1000A, for example, and the thickness of the layer of conductive material **44**'C. may be in the range of 500A to 2000A, for example.

A window **64** is formed in the layer of dielectric material **60**C and in the layer of conductive material **44**'C. to expose at least a portion of the underlying word line **42**C. The window **64** may be formed in any suitable manner, such as by the use of standard photolithographic techniques.

A fast ion conductive material is then disposed on the portion of the word line **42**C exposed by the window **64**. The selection of the fast ion conductive material and the manner in which it may be applied does not differ from the previous embodiments. Accordingly, for the sake of clarity, in this exemplary embodiment, the base metal of the word line **42**C is selected to be copper, and the more noble metal of the conductive layer **50**C is selected to be silver. The structure illustrated in FIG. **16** is immersed in the silver immersion solution for a sufficient amount of time to form the layer of conductive material **50**C, as illustrated in FIG. **17**.

After the conductive layer **50**C has been formed on the word line **42**C, a layer of chalcogenide material **52**C, such as germanium selenide, may be deposited in the window **64** over the conductive layer **50**C, as illustrated in FIG. **18**. The layer of chalcogenide material **52**C may be formed by any suitable process, such as chemical vapor deposition. The deposited layer of chalcogenide material **52**C is then planarized, by chemical mechanical planarization for example, so that the layer of chalcogenide material **52**C remains only within the window **64**. Thus, the thickness of the layer of chalcogenide material **52**C is approximately the same as the thickness of the layers of dielectric material **60**C and conductive material **44**'C.

Once the layer of chalcogenide material **52**C is formed in the window **64**, the structure illustrated in FIG. **18** is processed in a manner that causes at least a portion of the material in the conductive layer **50**C to migrate into the layer of chalcogenide material **52**C. As in the previous embodiments, the structure illustrated in FIG. **18** is subjected to ultraviolet radiation and heat to cause silver atoms in the layer of conductive material **50**C to migrate into the layer of chalcogenide material **52**C.

After this conversion process, the layer of chalcogenide material **52**C has metal ions in it, as illustrated in FIG. **19**. Then, a layer of conductive material **44**"C (the Metal 3 layer), which forms the remainder of the digit line, may be disposed over the layer of conductive material **44**'C. and over the layer of chalcogenide material **52**C to complete the memory cell **40**C.

As previously mention, chalcogenide material is somewhat susceptible to damage from planarization techniques, such as chemical mechanical planarization. However, it should be noted that the memory cell **40**C is relatively immune to any "over planarization" of the chalcogenide material **52**C within the window **64**. Although the planarization step can remove some of the relatively delicate chalcogenide material **52**C from the top of the window **64**, the electrical path from the digit line **44**C through the chalcogenide material **52**C typically does not extend directly from the layer of conductive material **44**"C. Rather, the shortest path typically extends from the edge of the layer of conductive material **44**'C. Thus, for over planarization to affect the memory cell **40**C adversely, chalcogenide material **52**C below the level of the dielectric layer **60**C would have to be removed. Since over planarization to such an extent is unlikely, the memory cell **40**C typically provides for relatively repeatable and consistent memory operation.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A method of fabricating a memory cell, the method comprising the acts of:

a. disposing a first line over a substrate, the first line being formed of a first metal;

b. plating the first line with a second metal by immersion in a solution containing the second metal;

c. disposing a layer of chalcogenide material over the second metal;

d. transferring ions of the second metal into the chalcogenide material; and

e. disposing a second line over the layer of chalcogenide material, the second line being formed of a third metal.

2. The method, as set forth in claim **1**, wherein act (a) comprises the act of: disposing at least one of copper, nickel, and tungsten over the substrate.

3. The method, as set forth in claim **1**, wherein the second metal comprises silver.

4. The method, as set forth in claim **1**, wherein act (c) comprises the act of: disposing germanium selenide over the second metal.

5. The method, as set forth in claim **1**, wherein act (d) comprises the act of: heating the second metal and the chalcogenide material.

6. The method, as set forth in claim **1**, wherein act (d) comprises the act of: irradiating the second metal and the chalcogenide material with ultraviolet radiation.

7. The method, as set forth in claims **1**, wherein acts (a) through (e) are performed in the order recited.

8. The method, as set forth in claim **7**, further comprising the act of: prior to transferring ions of the second metal into the chalcogenide material, planarizing the chalcogenide material disposed over the second metal.

9. A method of fabricating a memory cell, the method comprising the acts of:

a. disposing a layer of dielectric material over a substrate;

b. forming a window in the layer of dielectric material;

c. disposing a first metal in the window;

d. plating the first metal with a second metal by immersion in a solution containing the second metal;

e. disposing a layer of chalcogenide material over the second metal;

f. transferring ions of the second metal into the chalcogenide material; and

g. disposing a third metal over the layer of chalcogenide material.

10. The method, as set forth in claim **9**, wherein act (a) comprises the act of: disposing a layer of oxide over the substrate.

11. The method, as set forth in claim **9**, wherein act (c) comprises the act of: disposing at least one of copper, nickel, and tungsten in the window.

12. The method, as set forth in claim **9**, wherein the second metal comprises silver.

13. The method, as set forth in claim **9**, wherein act (e) comprises the act of: disposing germanium selenide over the second metal.

14. The method, as set forth in claim **9**, wherein act (f) comprises the act of: heating the second metal and the chalcogenide material.

15. The method, as set forth in claim **9**, wherein act (f) comprises the act of: irradiating the second metal and the chalcogenide material with ultraviolet radiation.

16. The method, as set forth in claim **9**, wherein acts (a) through (g) are performed in the order recited.

17. A method of fabricating a memory cell, the method comprising the acts of:

a. disposing a first layer of dielectric material on a substrate;

b. forming a first window in the first layer of dielectric material;

c. disposing a first metal in the first window;

d. disposing a second layer of dielectric material over the first metal and the first layer of dielectric material;

e. forming a second window in the second layer of dielectric material to expose at least a portion of the first metal in the first window;

f. plating the first metal exposed by the second window with a second metal by immersion in a solution containing the second metal;

g. disposing a layer of chalcogenide material over the second metal;

h. transferring ions of the second metal into the chalcogenide material; and

i. disposing a third metal over the layer of chalcogenide material.

18. The method, as set forth in claim **17**, wherein act (a) comprises the act of: disposing a layer of oxide over the substrate.

19. The method, as set forth in claim **17**, wherein act (c) comprises the act of: disposing at least one of copper, nickel, and tungsten in the window.

20. The method, as set forth in claim **17**, wherein act (d) comprises the act of: disposing a layer of silicon nitride over the first metal and the first layer of dielectric material.

21. The method, as set forth in claim **17**, wherein the second metal comprises silver.

22. The method, as set forth in claim **17**, wherein act (g) comprises the act of: disposing germanium selenide over the second metal.

23. The method, as set forth in claim **17**, wherein act (h) comprises the act of: heating the second metal and the chalcogenide material.

24. The method, as set forth in claim **17**, wherein act (h) comprises the act of: irradiating the second metal and the chalcogenide material with ultraviolet radiation.

25. The method, as set forth in claim **17**, wherein acts (a) through (i) are performed in the order recited.

26. The method, as set forth in claim **25**, further comprising the act of: prior to transferring ions of the second metal into the chalcogenide material, planarizing the chalcogenide material disposed over the second metal.

27. A method of fabricating a memory cell, the method comprising the acts of:

a. disposing a first layer of dielectric material on a substrate;

b. forming a first window in the first layer of dielectric material;

c. disposing a first metal in the first window;

d. disposing a second layer of dielectric material over the first metal and the first layer of dielectric material;

e. disposing a layer of a second metal over the second layer of dielectric material

f. forming a second window in the second layer of dielectric material and in the layer of the second metal to expose at least a portion of the first metal in the first window;

g. plating the first metal exposed by the second window with a third metal by immersion in a solution containing the third metal;

h. disposing a layer of chalcogenide material over the third metal;

i. transferring ions of the third metal into the chalcogenide material; and

j. disposing a fourth metal over the layer of chalcogenide material.

28. The method, as set forth in claim **27**, wherein act (a) comprises the act of: disposing a layer of oxide over the substrate.

29. The method, as set forth in claim **27**, wherein act (c) comprises the act of: disposing at least one of copper, nickel, and tungsten in the window.

30. The method, as set forth in claim **27**, wherein act (d) comprises the act of: disposing a layer of silicon nitride over the first metal and the first layer of dielectric material.

31. The method, as set forth in claim **27**, wherein the third metal comprises silver.

32. The method, as set forth in claim **27**, wherein act (h) comprises the act of: disposing germanium selenide over the third metal.

33. The method, as set forth in claim **27**, wherein act (i) comprises the act of: heating the third metal and the chalcogenide material.

34. The method, as set forth in claim **27**, wherein act (i) comprises the act of: irradiating the third metal and the chalcogenide material with ultraviolet radiation.

35. The method, as set forth in claim **27**, wherein acts (a) through (j) are performed in the order recited.

36. The method, as set forth in claim **35**, further comprising the act of: prior to transferring ions of the third metal into the chalcogenide material, planarizing the chalcogenide material disposed over the third metal.

* * * * *

CERTIFICATE OF CORRECTION

PATENT NO.	: 7,071,021 B2	Page 1 of 3
APPLICATION NO.	: 10/205387	
DATED	: July 4, 2006	
INVENTOR(S)	: Steven T. Harshfield et al.	

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On title page in Item (63) Related U.S. Application Data, and also in the sentence following the title of the patent just before the Specification, the word "continuation" should read --divisional--.

In the Item [56] Other Publications portion of the References Cited section, the following publication should be added:

--HELBERT et al., *Intralevel hybrid resist process with submicron capability*, SPIE Vol. 333 SUBMICRON LITHOGRAPHY, pp. 24-29 (1982).--

Also, in the Item [56] Other Publications portion, the following errors are corrected:

"El Bouchairi, B.; Bernede, J.C.; Burgaud, P., Propeties of $Ag_{2-x}Se_{1+x/n}$-Si diodes, Thin Solid Films 110 (1983) 107-113."

Should read

--El Bouchairi, B.; Bernede, J.C.; Burgaud, P., Properties of $Ag_{2-x}Se_{1+x/n}$-Si diodes, Thin Solid Films 110 (1983) 107-113.--;

"Hajto, J.; McAuley, B.; Snell, A.J.; Owen, A.E., Theory of room temperature quantized resistance effects in metal-a-Si:H-metal thin film structuress, J. Non-Cryst. Solids 198-200 (1996) 825-828."

Should read

--Hajto, J.; McAuley, B.; Snell, A.J.; Owen, A.E., Theory of room temperature quantized resistance effects in metal-a-Si:H-metal thin film structures, J. Non-Cryst Solids 198-200 (1996) 825-828.--;

"Hegab, N.A.; Fadel, M.; Sedeek, K., Memory switching pehnomena in thin films of chalcogenide semiconductors, Vacuum 45 (1994) 459-462."

Should read

--Hegab, N.A.; Fadel, M.; Sedeek, K., Memory switching phenomena in thin films of chalcogenide semiconductors, Vacuum 45 (1994) 459-462.--.

CERTIFICATE OF CORRECTION

PATENT NO. : 7,071,021 B2

APPLICATION NO. : 10/205387
DATED : July 4, 2006
INVENTOR(S) : Steven T. Harshfield et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

"Kotkata, M.F.; Afif, M.A.; Labib, H.H.; Hegab, N.A.; Abdel-Aziz, M.M., Memory switching in amorphous GeSeTI chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146."

Should read

--Kotkata, M.F.; Afifi, M.A.; Labib, H.H.; Hegab, N.A.; Abdel-Aziz, M.M., Memory switching in amorphous GeSeTI chalcogenide semiconductor films, Thin Solid Films 240 (1994) 143-146.--;

"McHardy et al., *The dissolution of metals in amorphous chalcogenides and the effects o electron and ultraviolet radiation*, 20 J. Phys. C.: Solid State Phys., pp. 4055-4075 (1987)f."

Should read

--McHardy et al., *The dissolution of metals in amorphous chalcogenides and the effects of electron and ultraviolet radiation*, 20 J. Phys. C.: Solid State Phys., pp. 4055-4075 (1987).--; and

"Tranchant, S.; Peytavin, S.; Ribes, M.; Flank, A.M.; Dexpert, H.; Lagarde, J.P., Silver chalcogenide glasses Ag-Ge-Se: Ionic conduction and exafs structural investigation, Transport-structure relations in fast ion and mixed conductors Proceedings of the 6th Riso International symposium, Sep. 9-13, 1985."

Should read

--Tranchant, S.; Peytavin, S.; Ribes, M.; Flank, A.M.; Dexpert, H.; Lagarde, J.P., Silver chalcogenide glasses Ag-Ge-Se: Ionic conduction and EXAFS structural investigation, Transport-structure relations in fast ion and mixed conductors, Proc. of the 6th RISO Int'l Symp., Sep. 9-13, 1985.--

In the Specification, the following error is corrected:

Column 1, line 49, "are more" should read --or more--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,071,021 B2
APPLICATION NO. : 10/205387
DATED : July 4, 2006
INVENTOR(S) : Steven T. Harshfield et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, No. 83 on the application should be added as follows:

Col. 12, lines 65-66

--37. The method, as set forth in claim 16, further comprising the act of:

prior to transferring ions of the second metal into the chalcogenide material, planarizing the chalcogenide material disposed over the second metal.--

Signed and Sealed this

Thirteenth Day of November, 2007

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office