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(12) **United States Patent**
King

(10) **Patent No.: US 6,980,467 B2**
(45) **Date of Patent: Dec. 27, 2005**

(54) **METHOD OF FORMING A NEGATIVE DIFFERENTIAL RESISTANCE DEVICE**

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(73) Assignee: **Progressant Technologies, Inc.**, Mountain View, CA (US)

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(21) Appl. No.: **10/314,735**

(22) Filed: **Dec. 9, 2002**

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(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/159**; 365/174
(58) **Field of Search** 365/159, 174, 365/148; 257/192, 197; 438/492, 606

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(57) **ABSTRACT**

A negative differential resistance (NDR) field-effect transistor element is disclosed, formed on a silicon-based substrate using conventional MOS manufacturing operations. Methods for improving a variety of NDR characteristics for an NDR element, such as peak-to-valley ratio (PVR), NDR onset voltage (V_{NDR}) and related parameters are also disclosed.

4 Claims, 22 Drawing Sheets

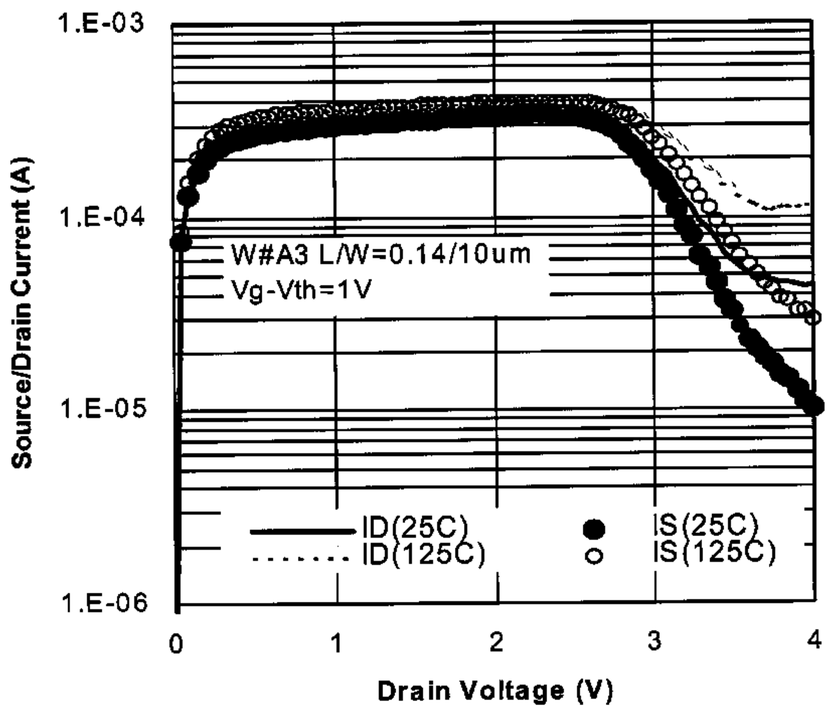

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Fig. 1

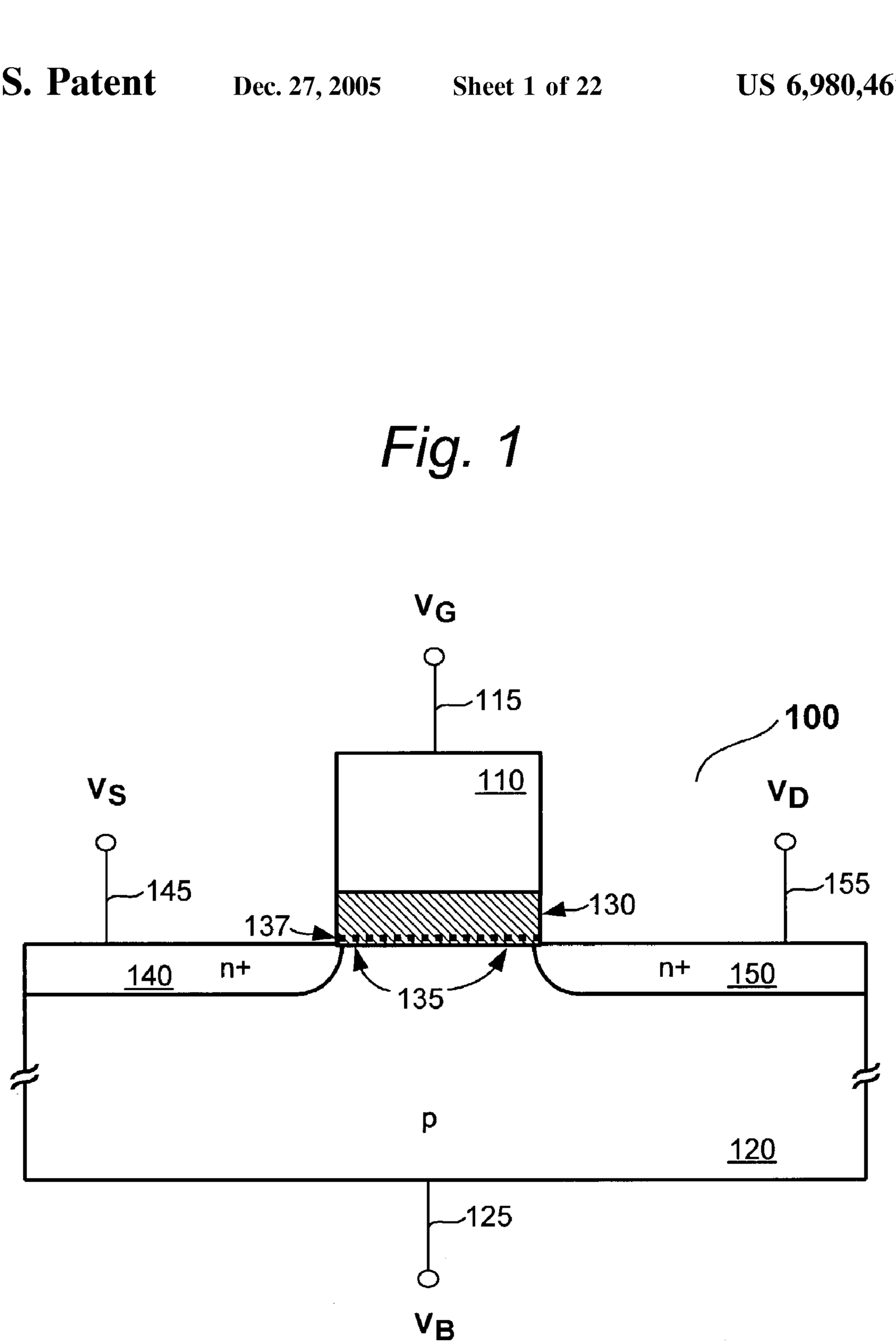


Fig. 2

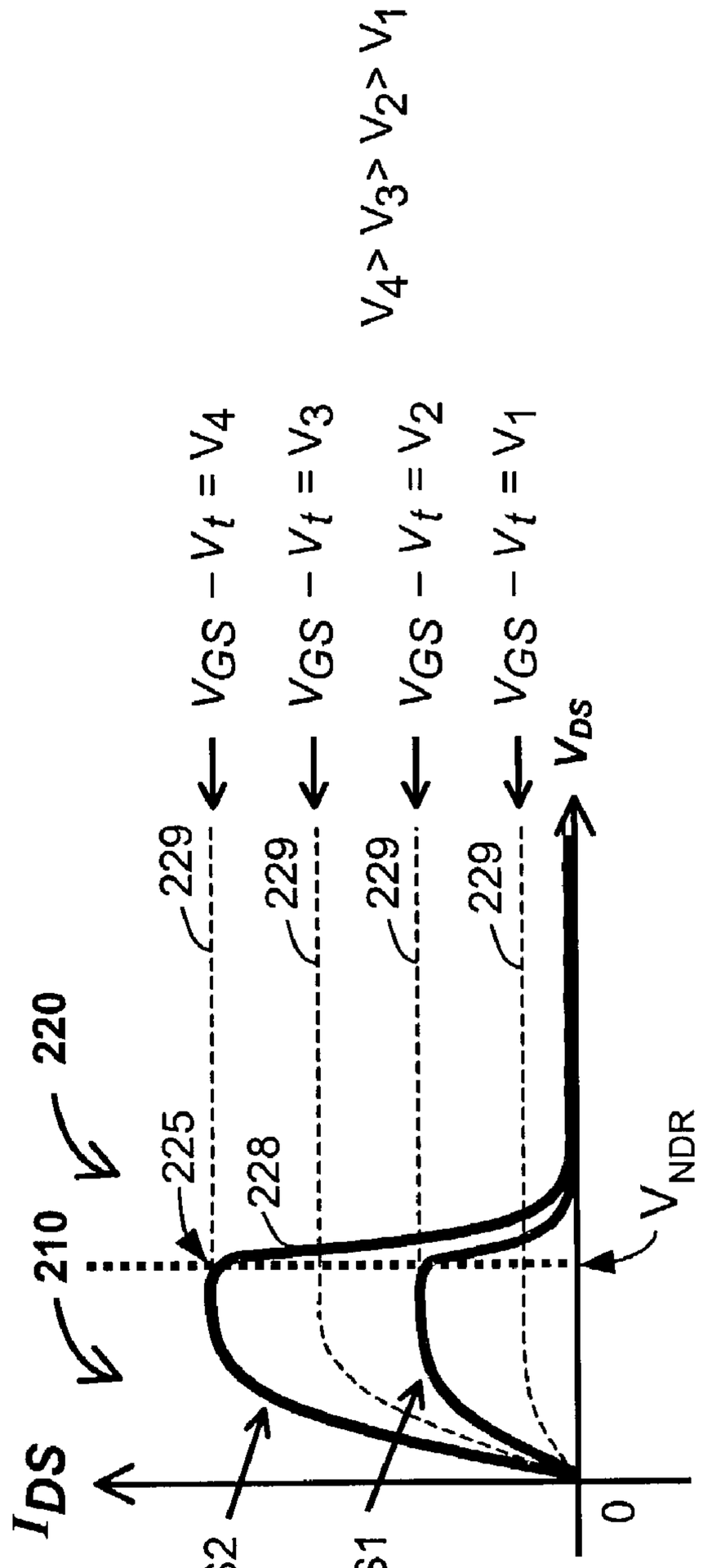

$V_4 > V_3 > V_2 > V_1$
$V_t = V_4$
$V_t = V_3$
$V_t = V_2$
$V_t = V_1$
V_{GS}
V_{DS}
229
220
210
225
228
V_{NDR}
I_{DS}
2
1
0
$V_{GS} = V_{GS2} > V_{GS1}$
$V_{GS2} > V_{GS1}$

Fig.3A

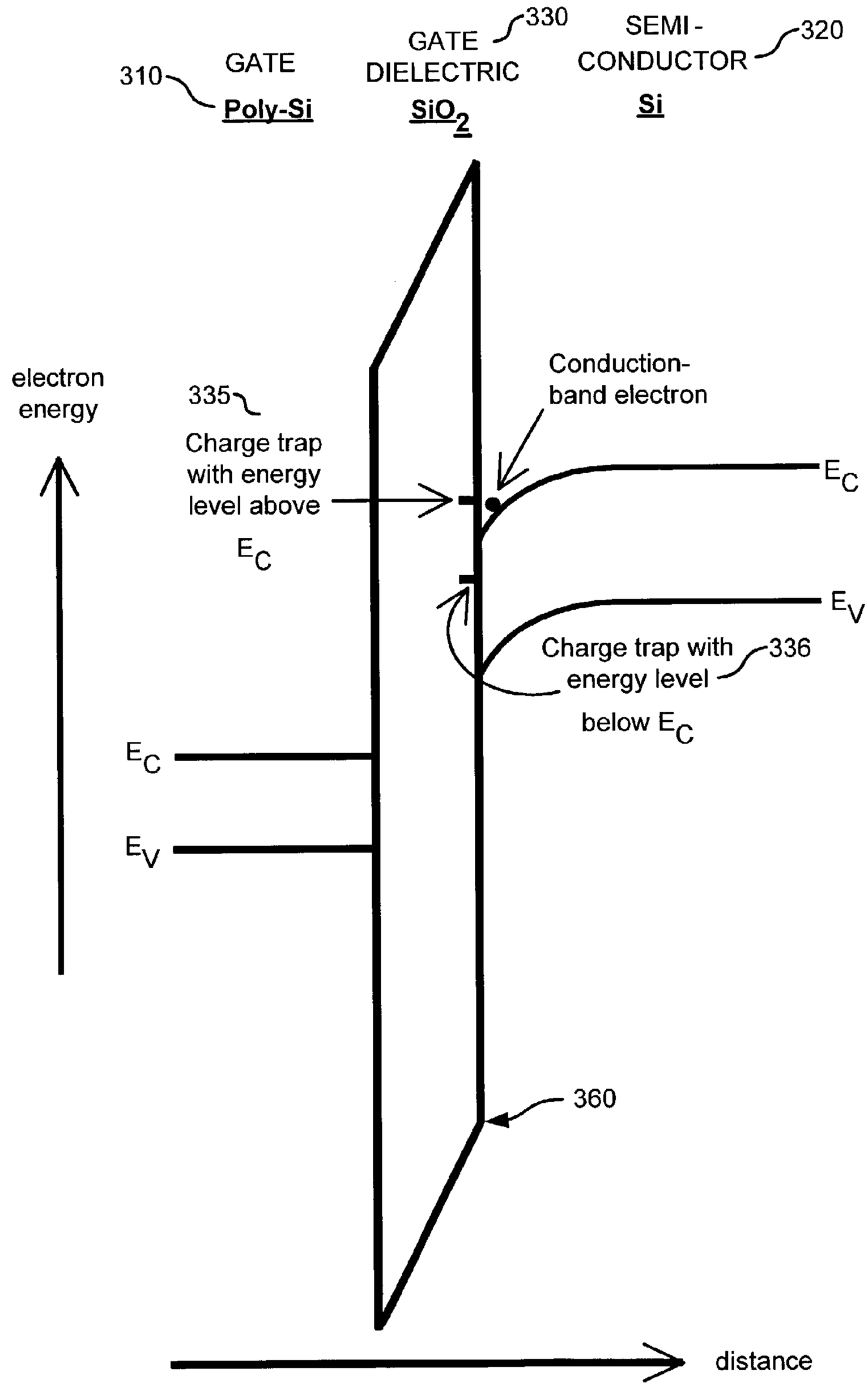

310
GATE
Poly-Si
GATE DIELECTRIC
330
SiO2
SEMI-CONDUCTOR
320
Si
electron energy
335
Charge trap with energy level above EC
EC
Conduction-band electron
EC
EV
Charge trap with energy level below EC
336
EC
EV
360
distance

Fig.3B

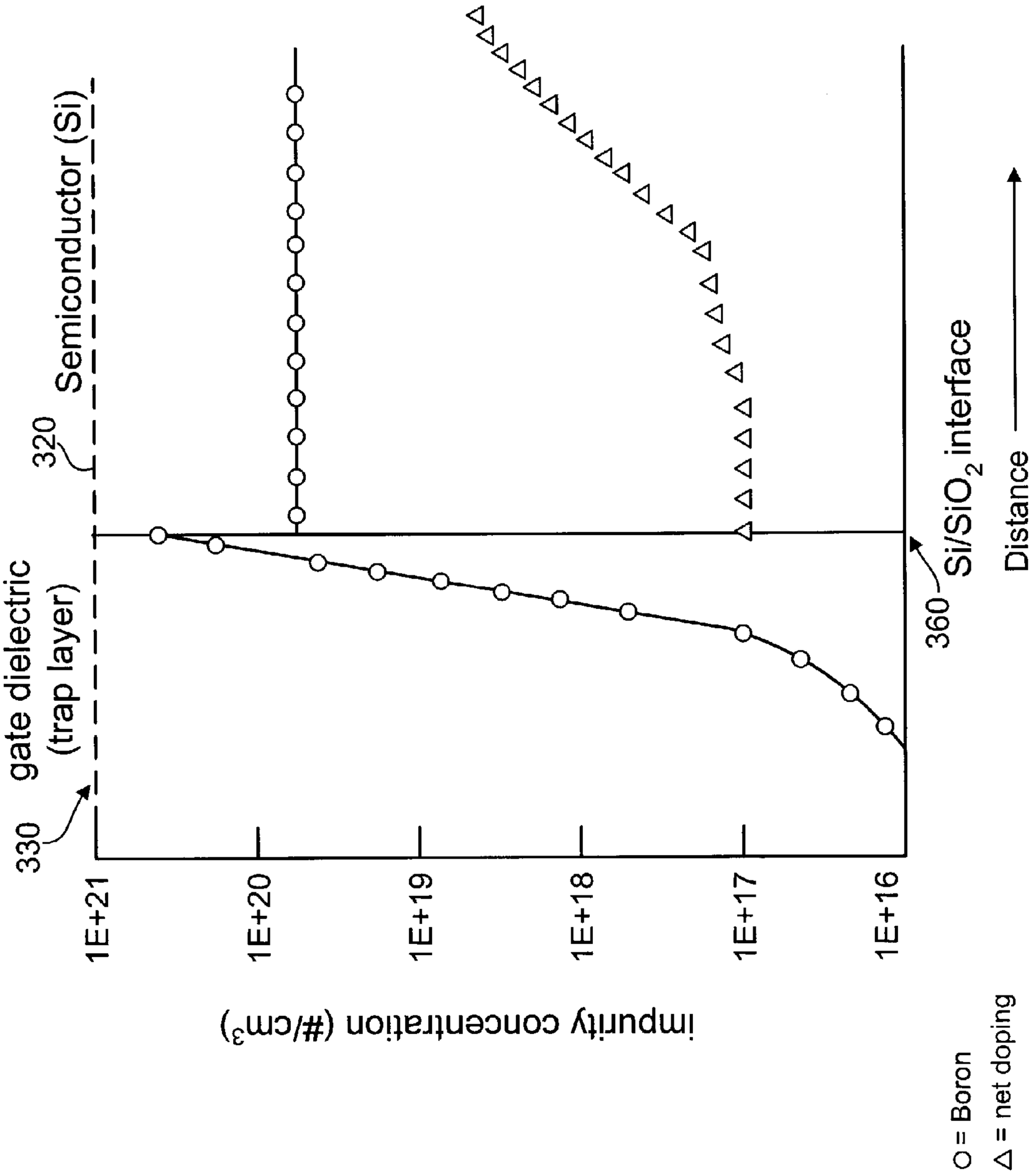

Semiconductor (Si)
320
gate dielectric
(trap layer)
330
Si/SiO2 interface
360
Distance
impurity concentration (#/cm3)
1E+21
1E+20
1E+19
1E+18
1E+17
1E+16
O = Boron
Δ = net doping

Fig. 4

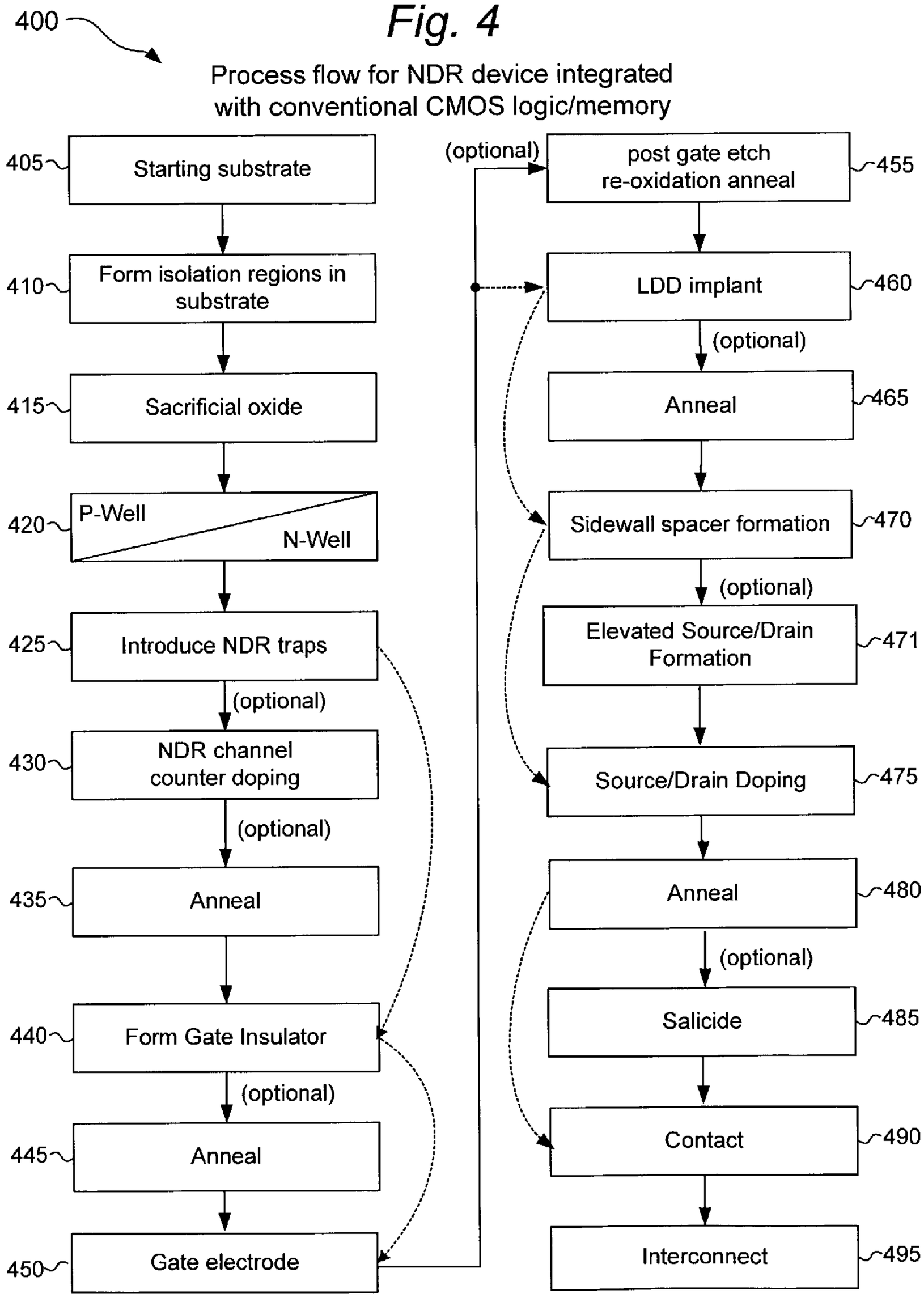

400
Process flow for NDR device integrated with conventional CMOS logic/memory
405
Starting substrate
410
Form isolation regions in substrate
415
Sacrificial oxide
420
P-Well
N-Well
425
Introduce NDR traps
(optional)
430
NDR channel counter doping
(optional)
435
Anneal
440
Form Gate Insulator
(optional)
445
Anneal
450
Gate electrode
(optional)
455
post gate etch re-oxidation anneal
460
LDD implant
(optional)
465
Anneal
470
Sidewall spacer formation
(optional)
471
Elevated Source/Drain Formation
475
Source/Drain Doping
480
Anneal
(optional)
485
Salicide
490
Contact
495
Interconnect

Fig. 5

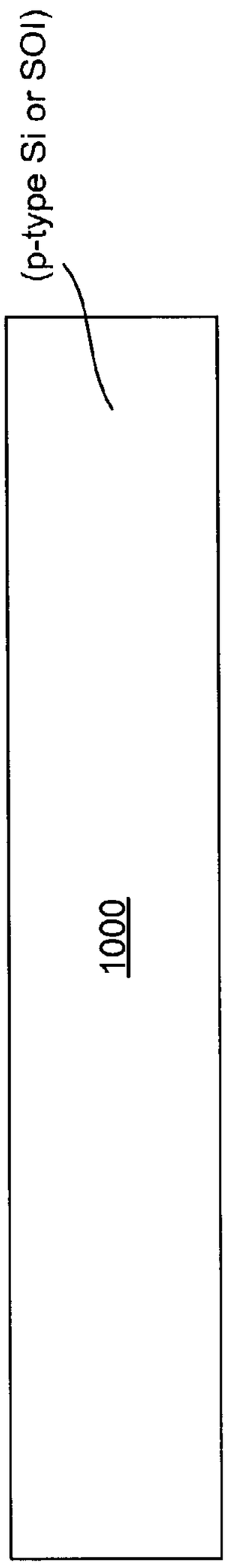

(p-type Si or SOI)
1000

Fig. 6

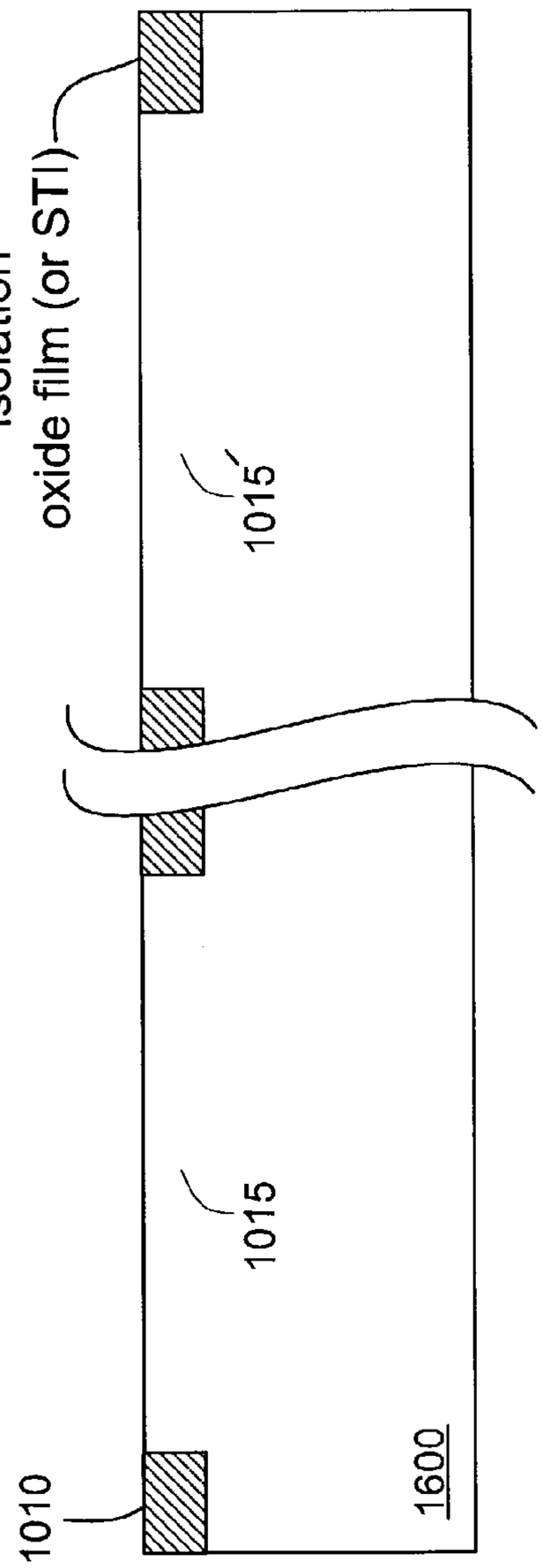

isolation oxide film (or STI)
1015
1015
1010
1600

Fig. 7

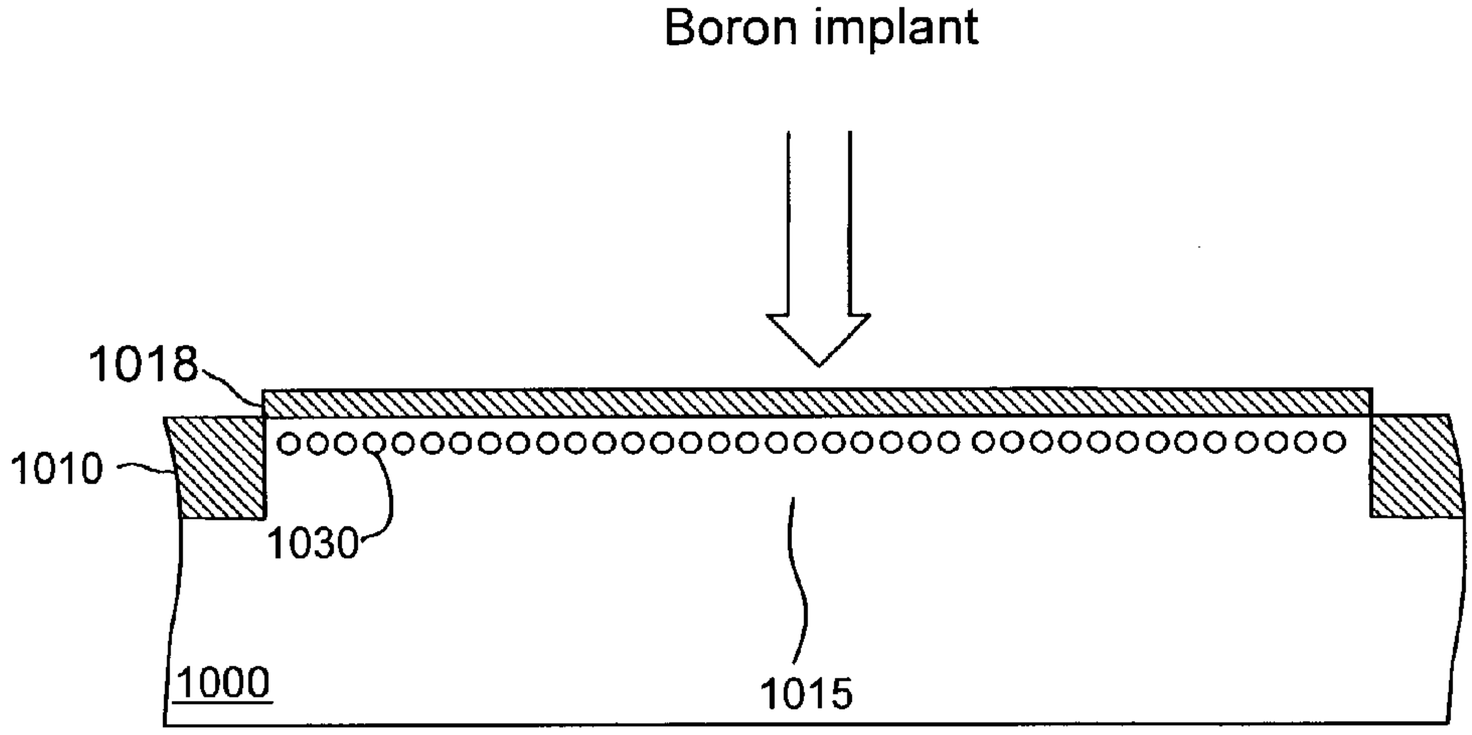

Boron implant
1018
1010
1030
1000
1015

Fig. 8

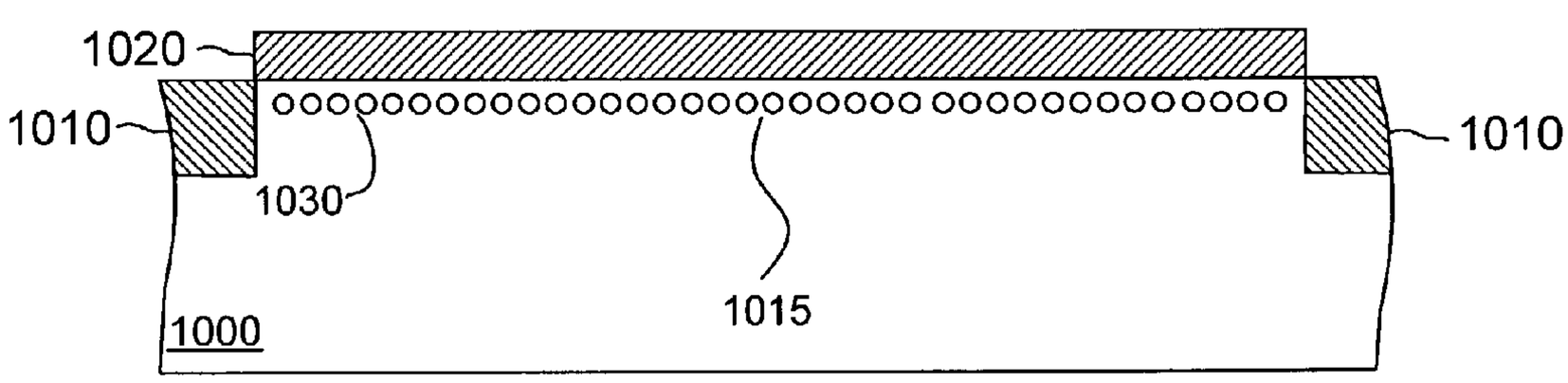

1020
1010
1030
1015
1010
1000

Fig. 9

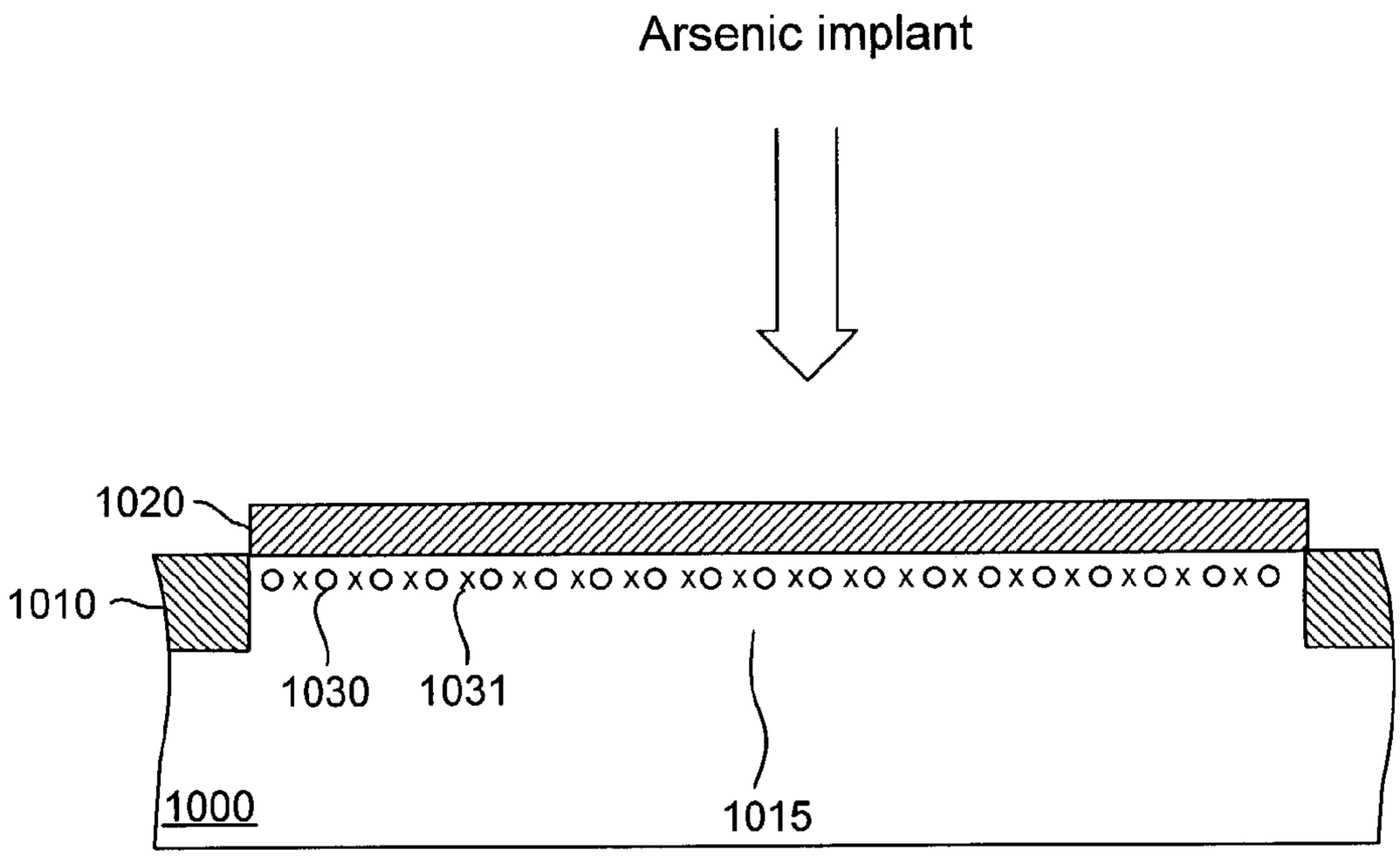


Fig. 10

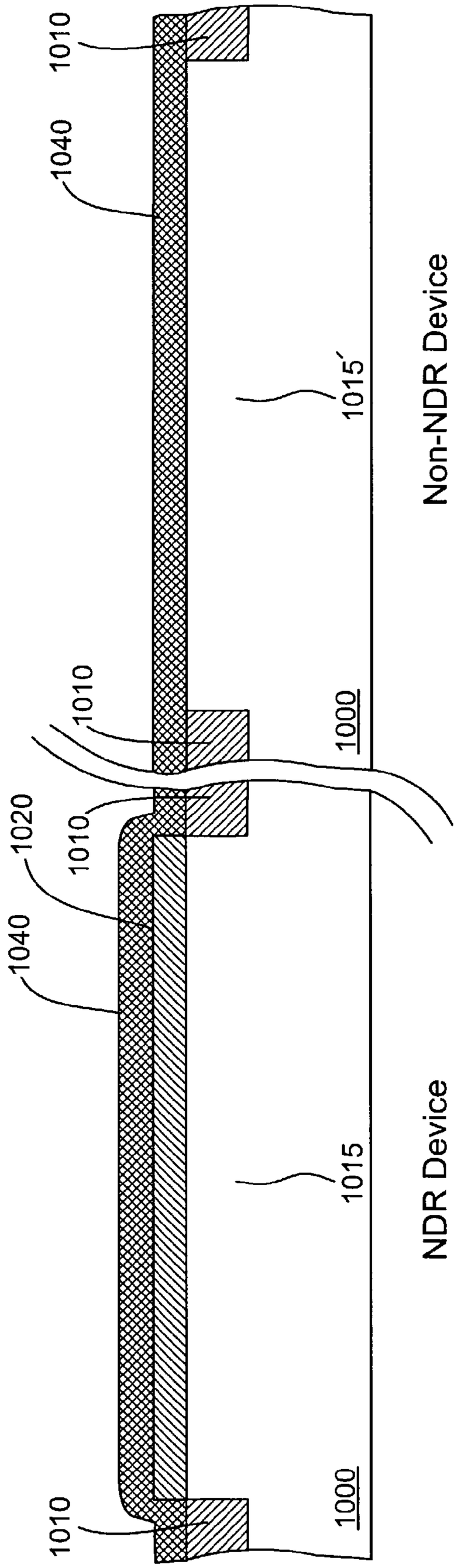

1010
1040
1015'
Non-NDR Device
1000
1010
1020
1010
1040
1015
NDR Device
1000
1010

Fig. 11

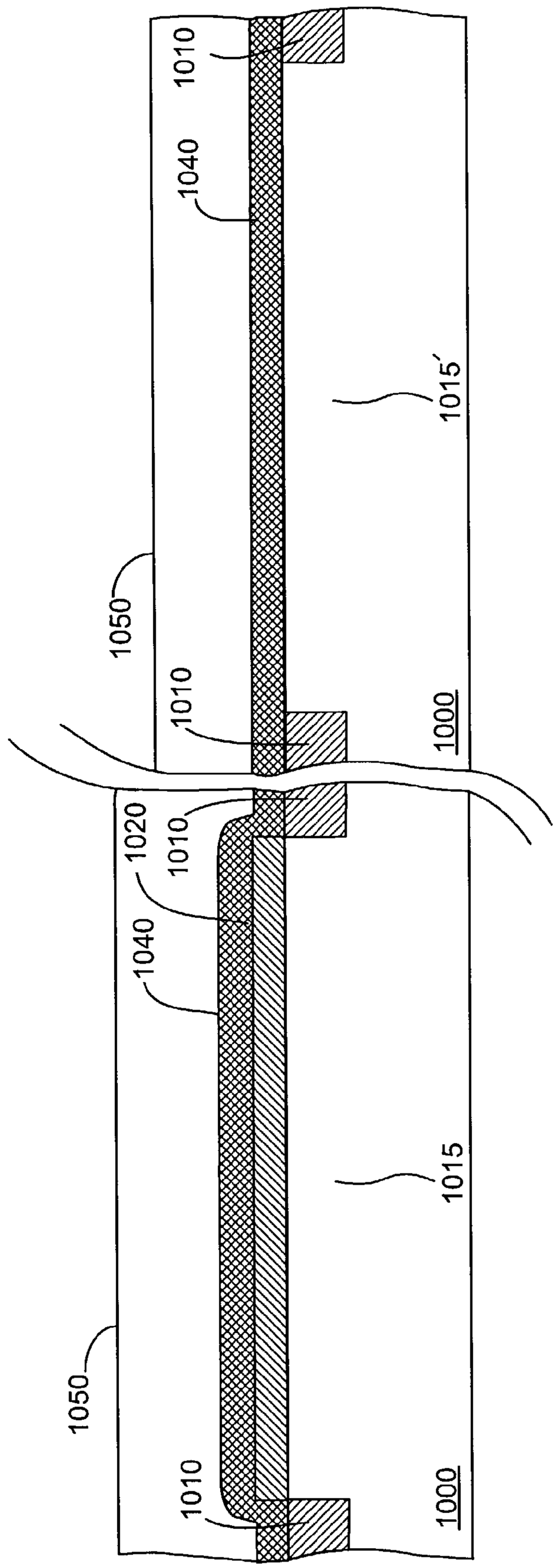

1010
1040
1015'
1050
1010
1000
1020
1010
1040
1015
1050
1010
1000

Fig. 12

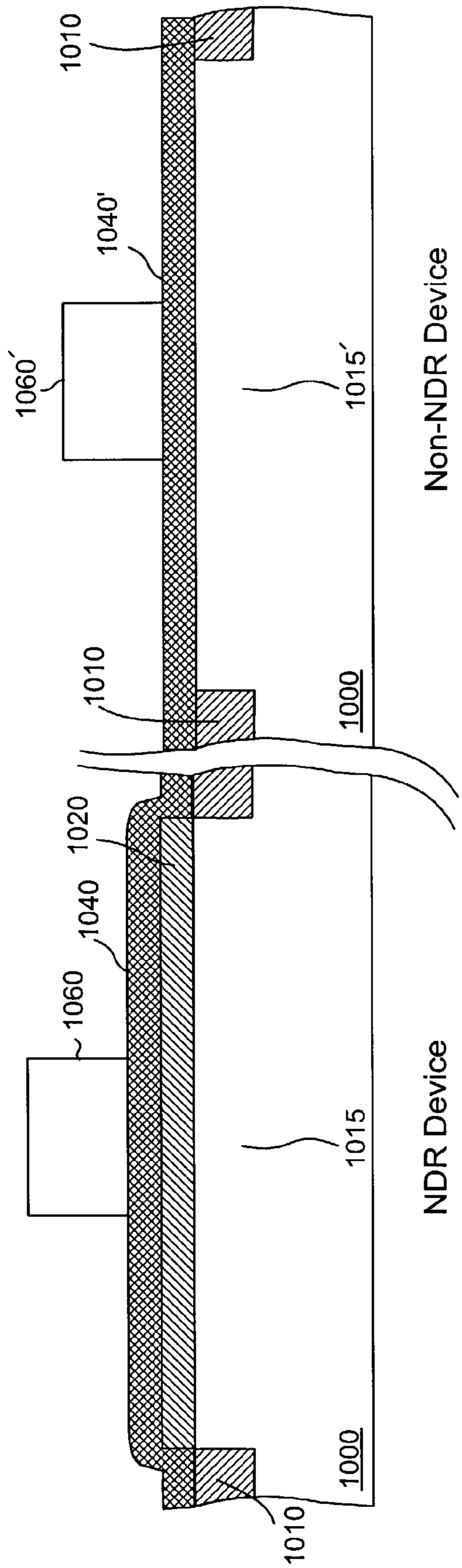

1010
1040'
1060'
1015'
Non-NDR Device
1010
1000
1020
1040
1060
1015
NDR Device
1000
1010

Fig. 13

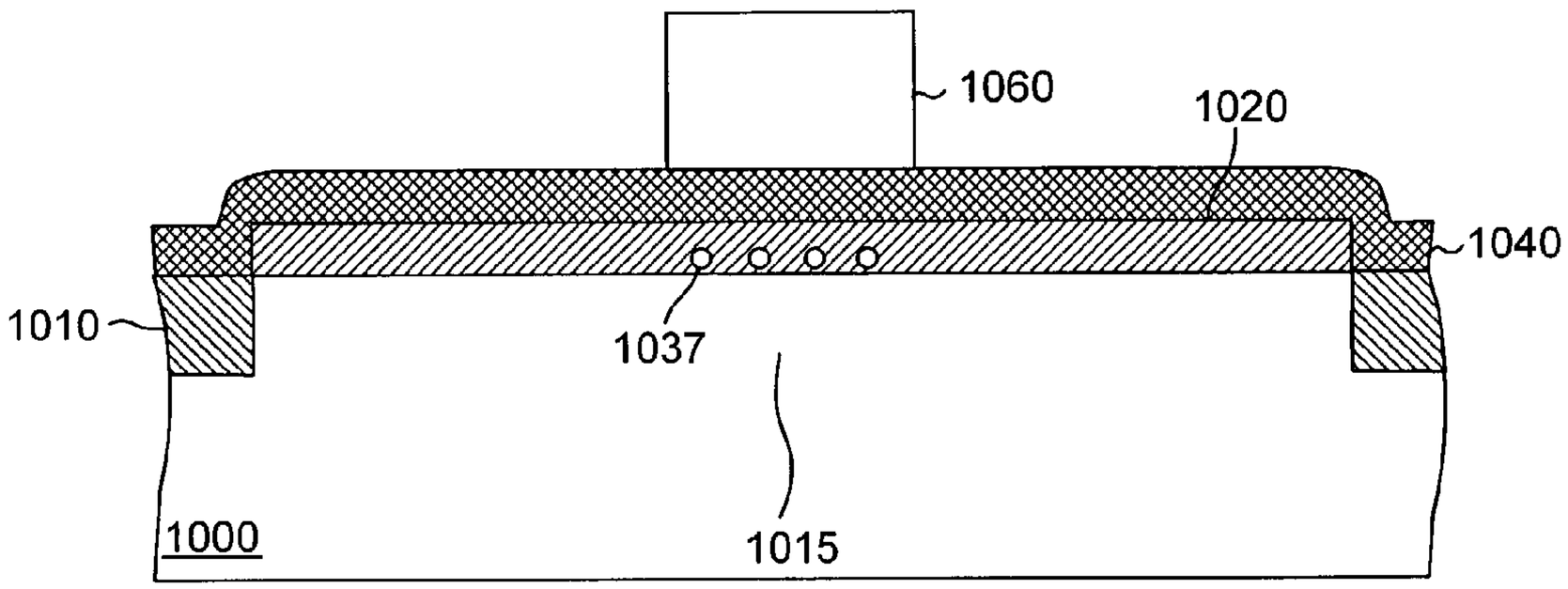


Fig. 14

LDD implant

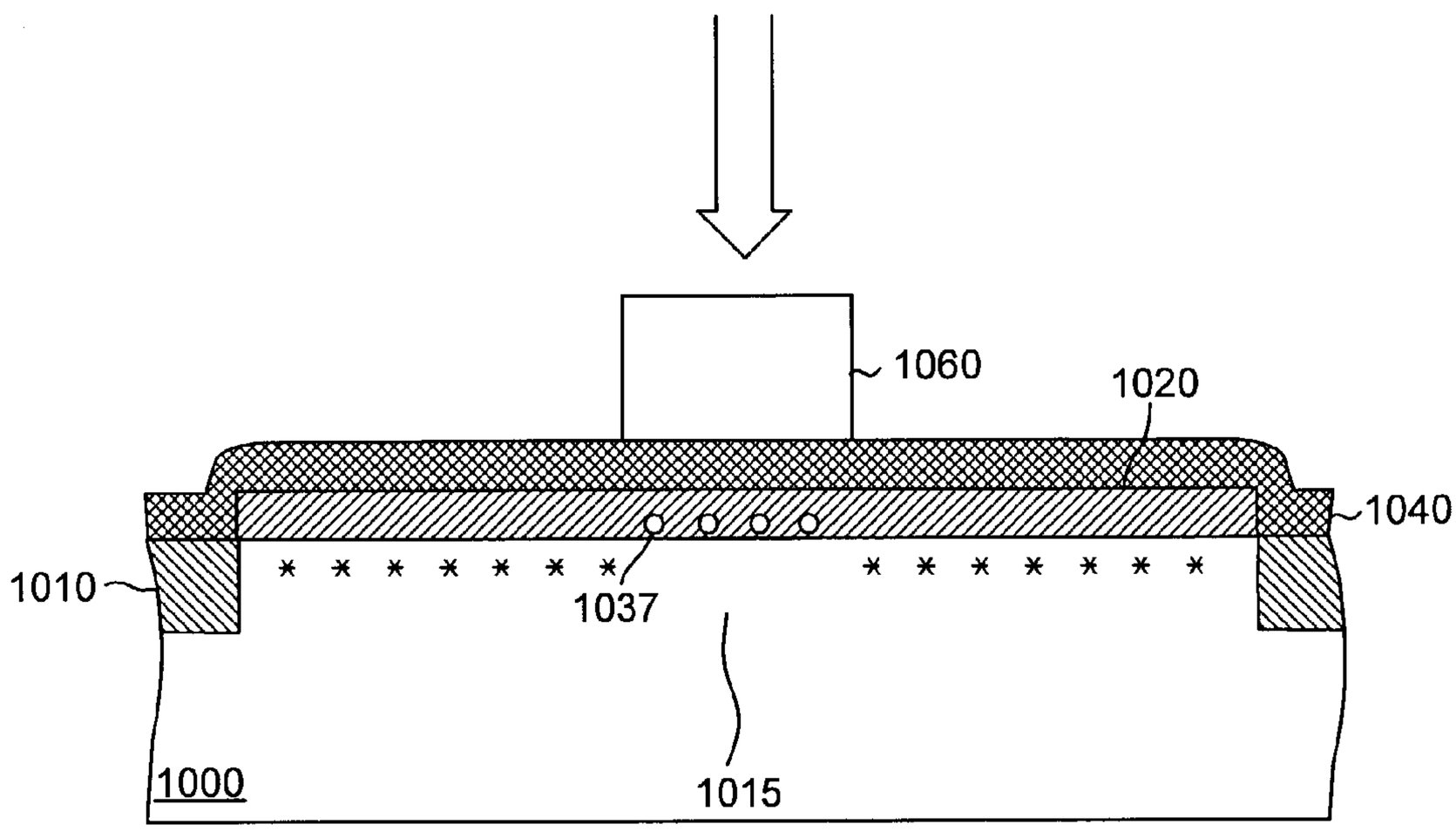


Fig. 15

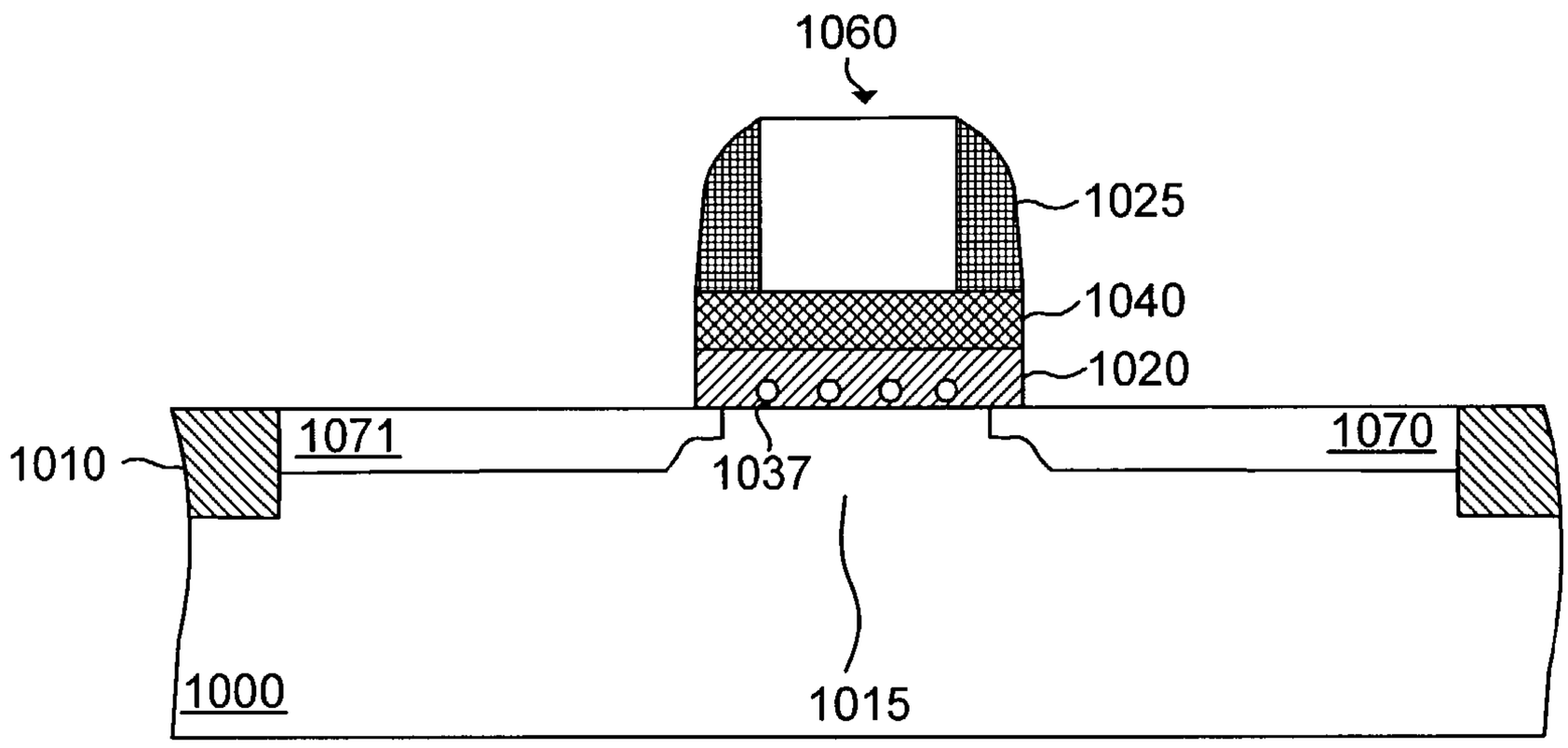


Fig. 16

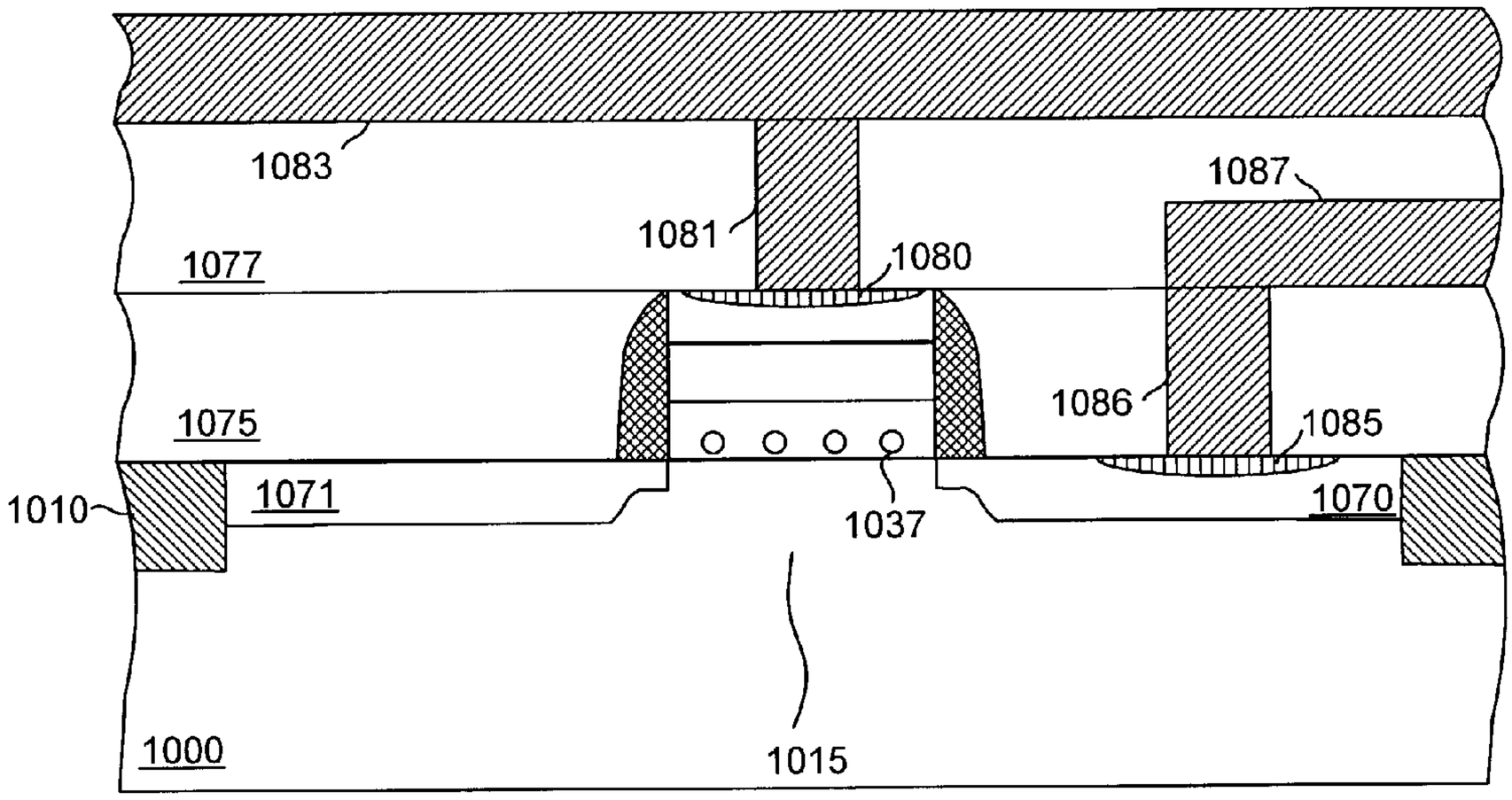

1083
1081
1087
1077
1080
1086
1085
1075
1071
1010
1037
1070
1000
1015

Fig. 17A

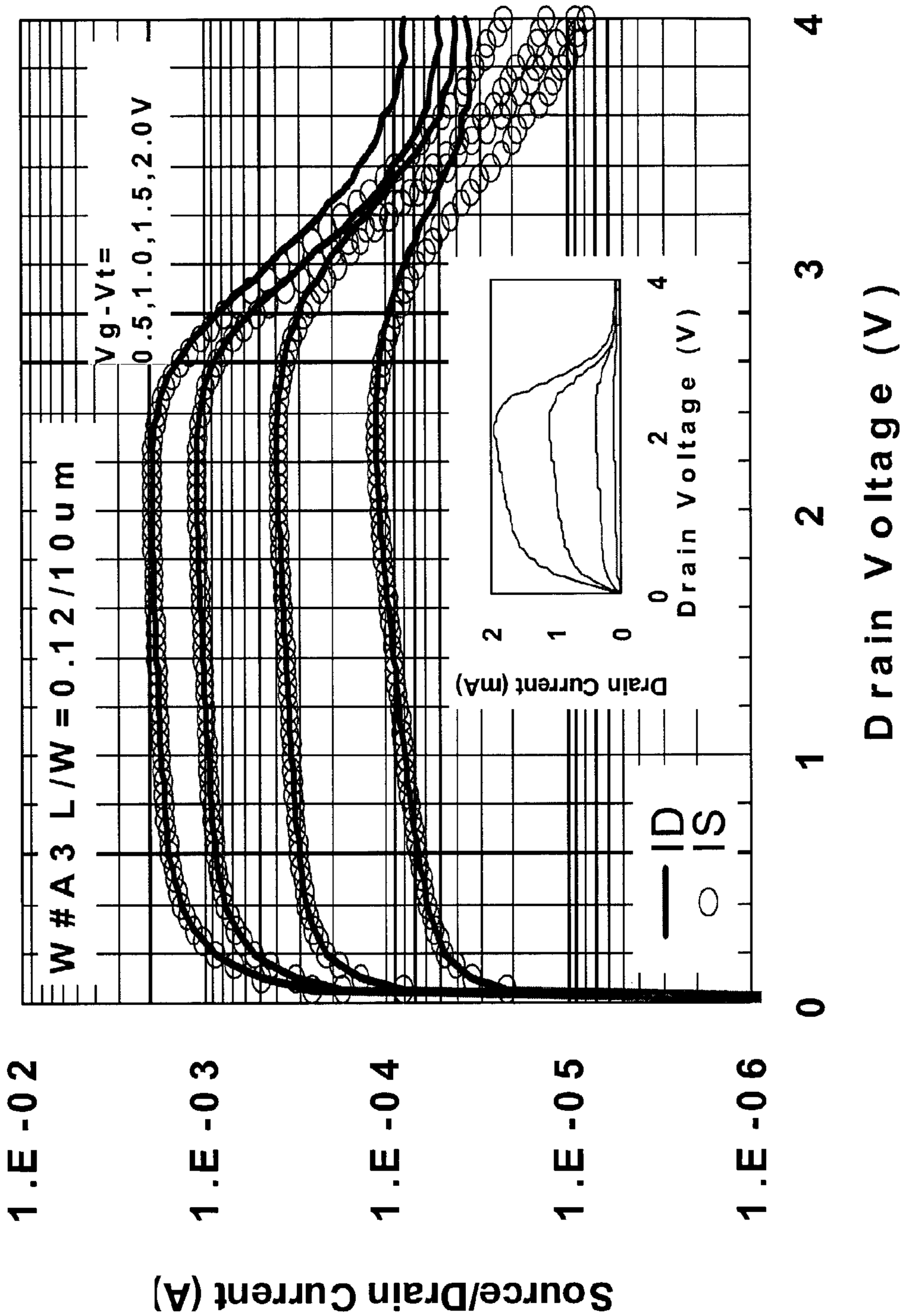

W # A 3 L/W = 0.12/10um
Vg-Vt= 0.5,1.0,1.5,2.0V
ID
IS
Drain Current (mA)
2
1
0
Drain Voltage (V)
0
1
2
3
4
Drain Voltage (V)
Source/Drain Current (A)
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06

Fig. 17B

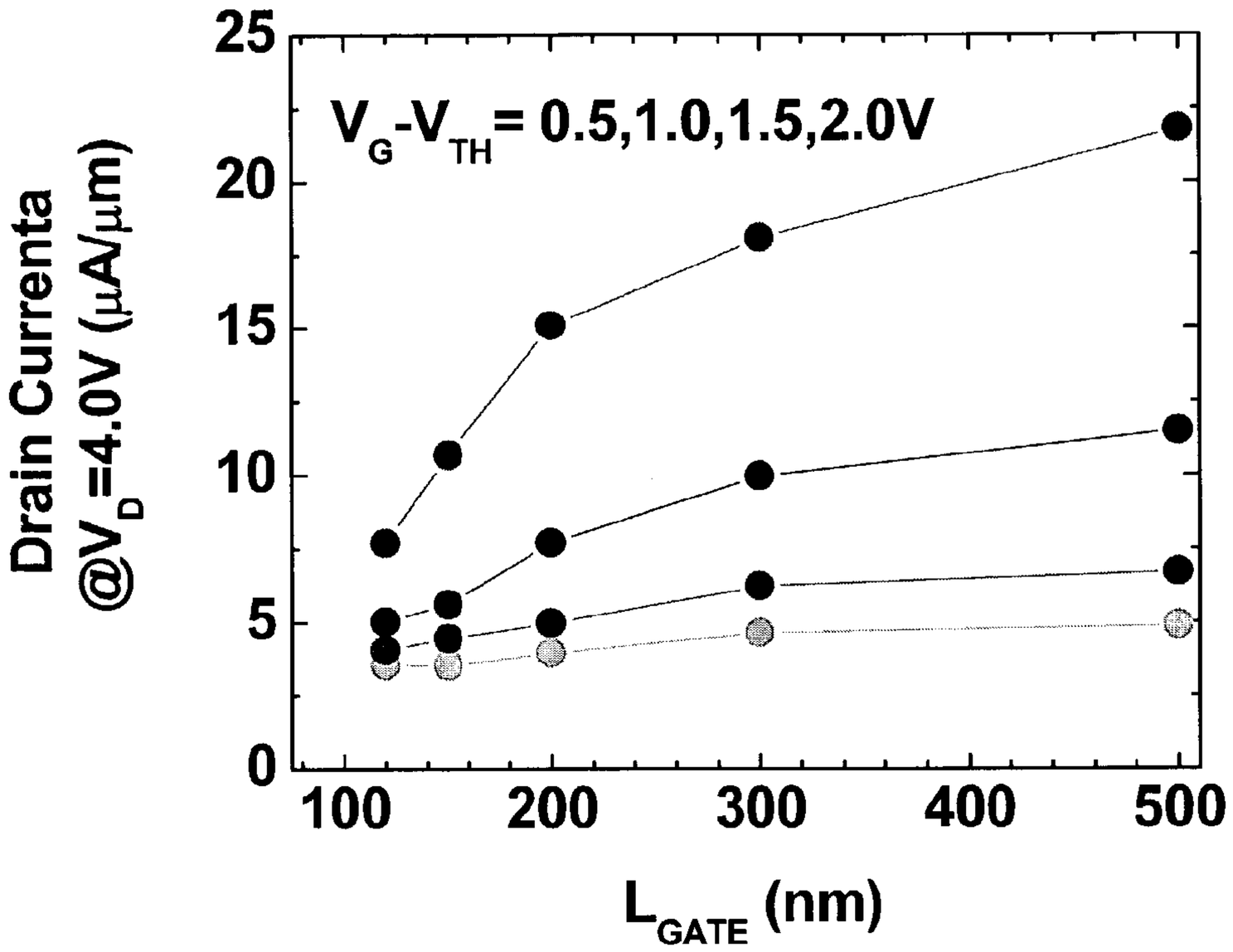


Fig. 17C

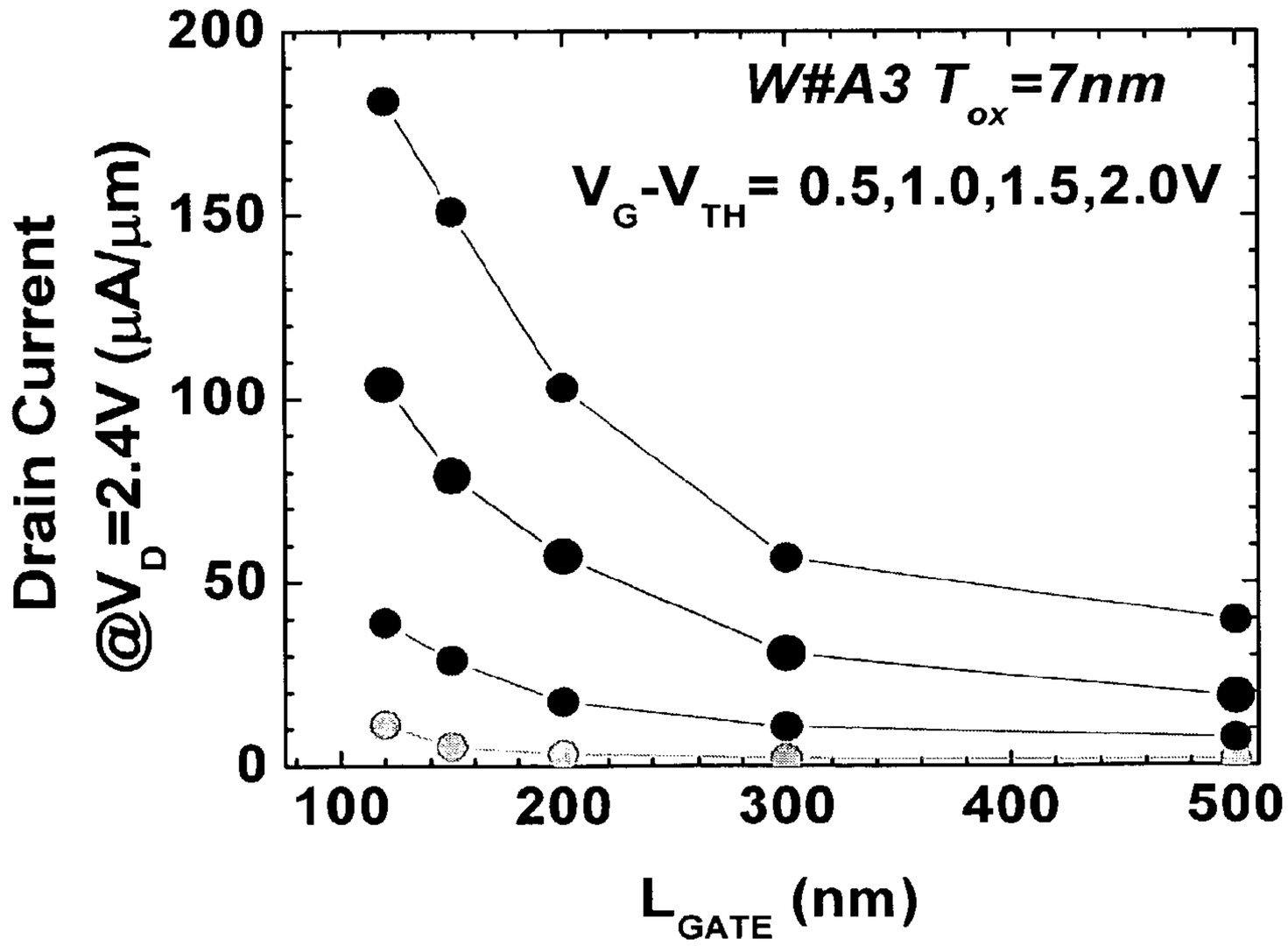


Fig. 17D

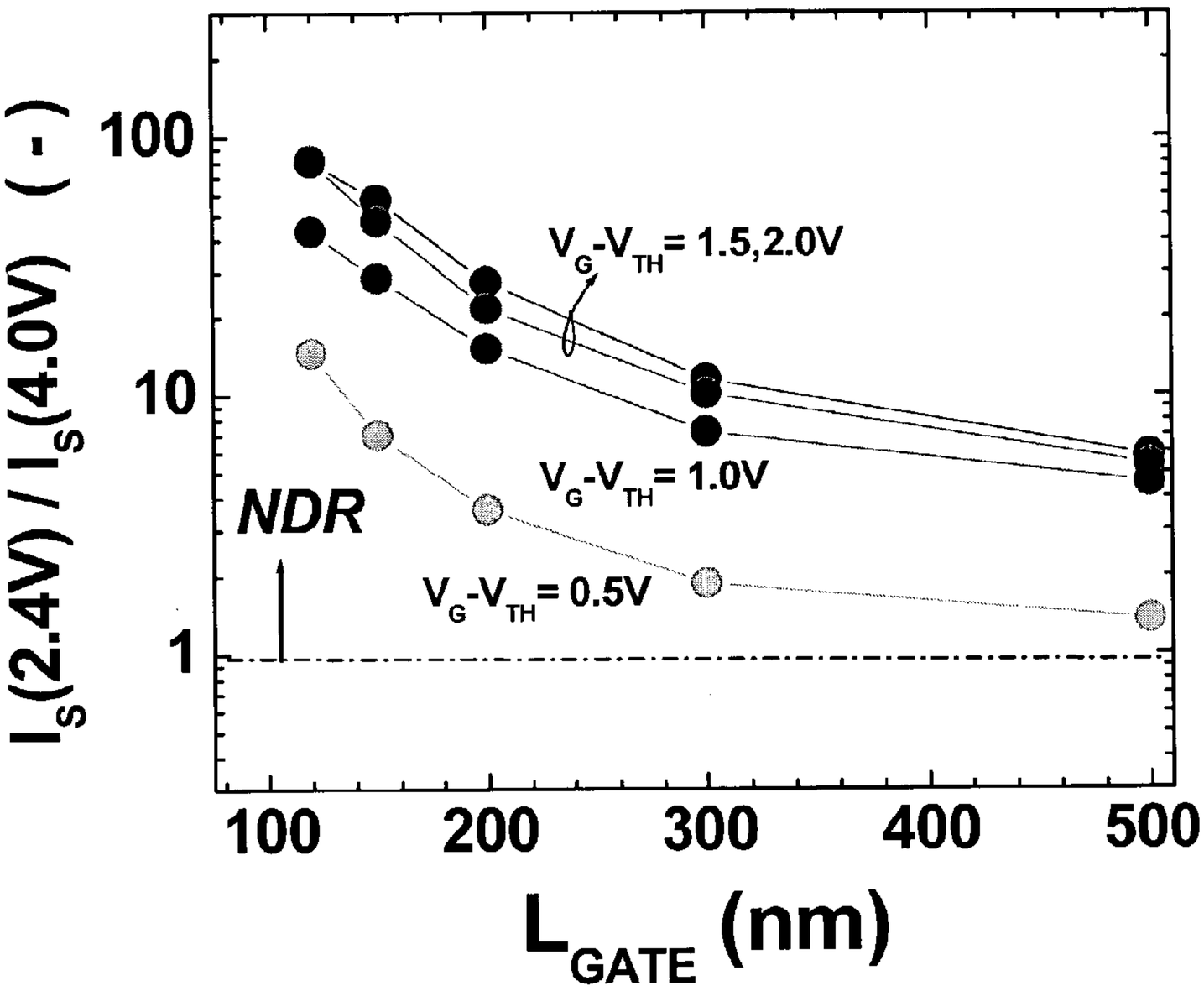


Fig. 17E

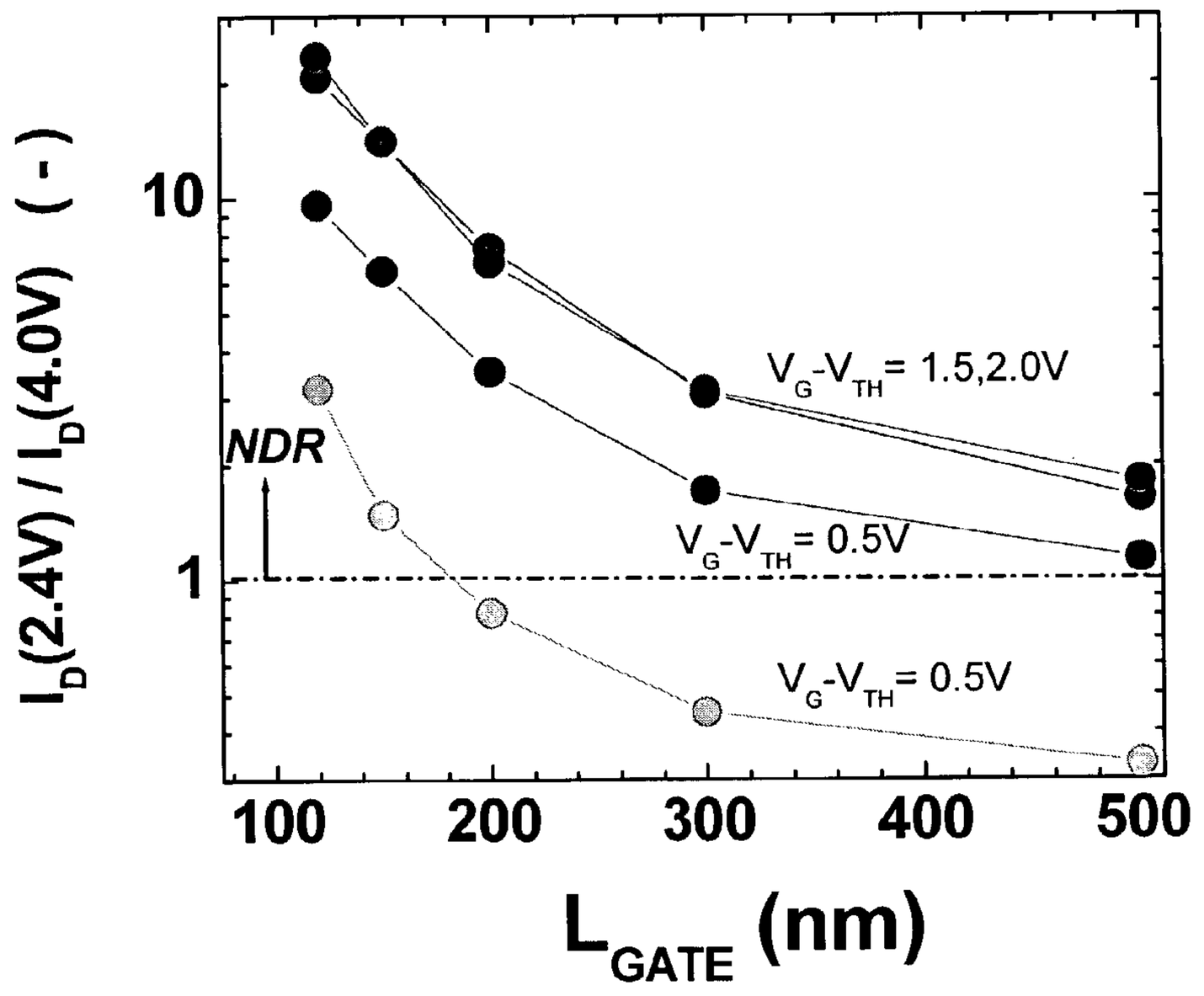


Fig. 17F

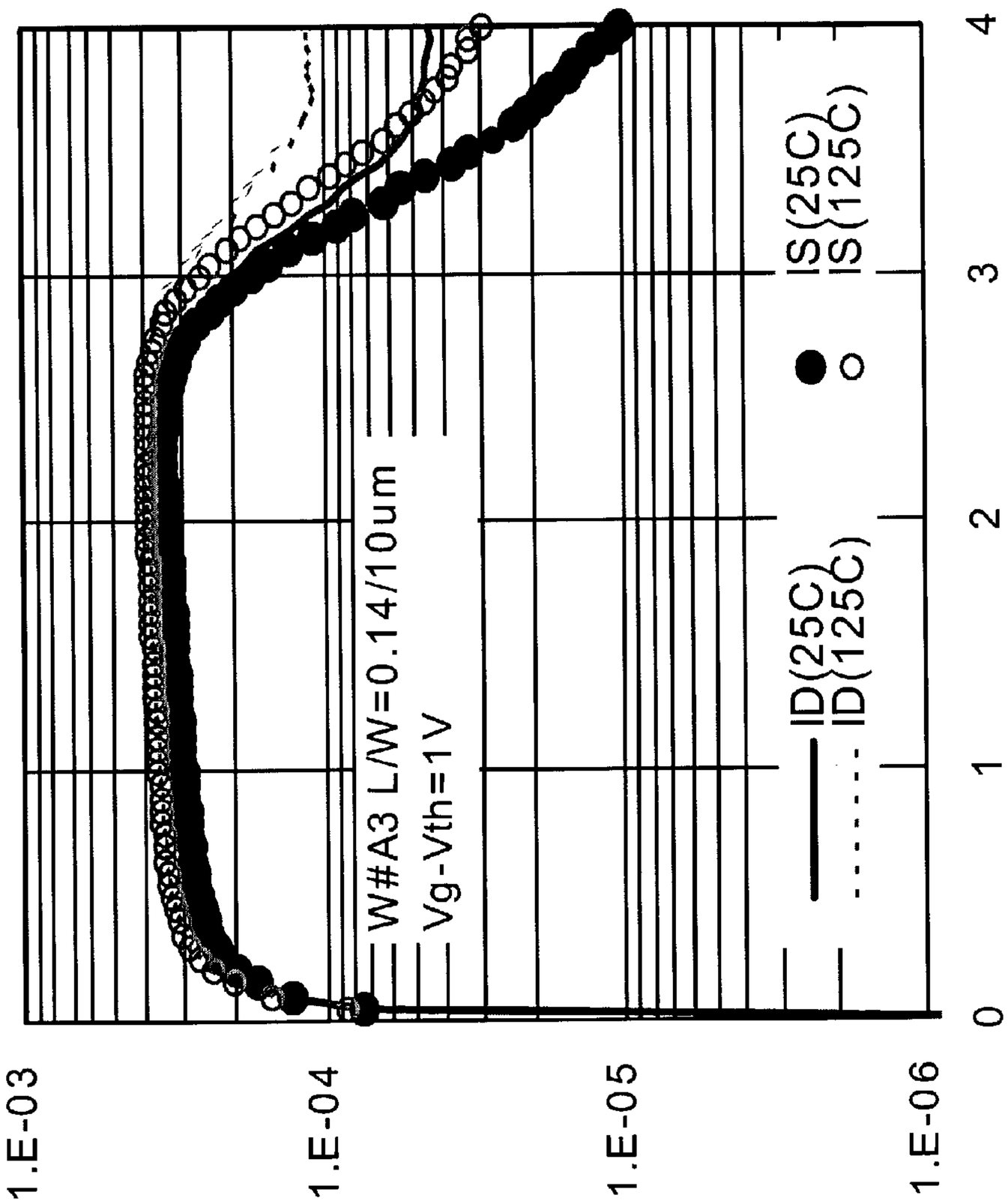

W#A3 L/W=0.14/10um
Vg-Vth=1V
ID(25C)
ID(125C)
IS(25C)
IS(125C)
Drain Voltage (V)
Source/Drain Current (A)
0
1
2
3
4
1.E-03
1.E-04
1.E-05
1.E-06

Fig. 17G

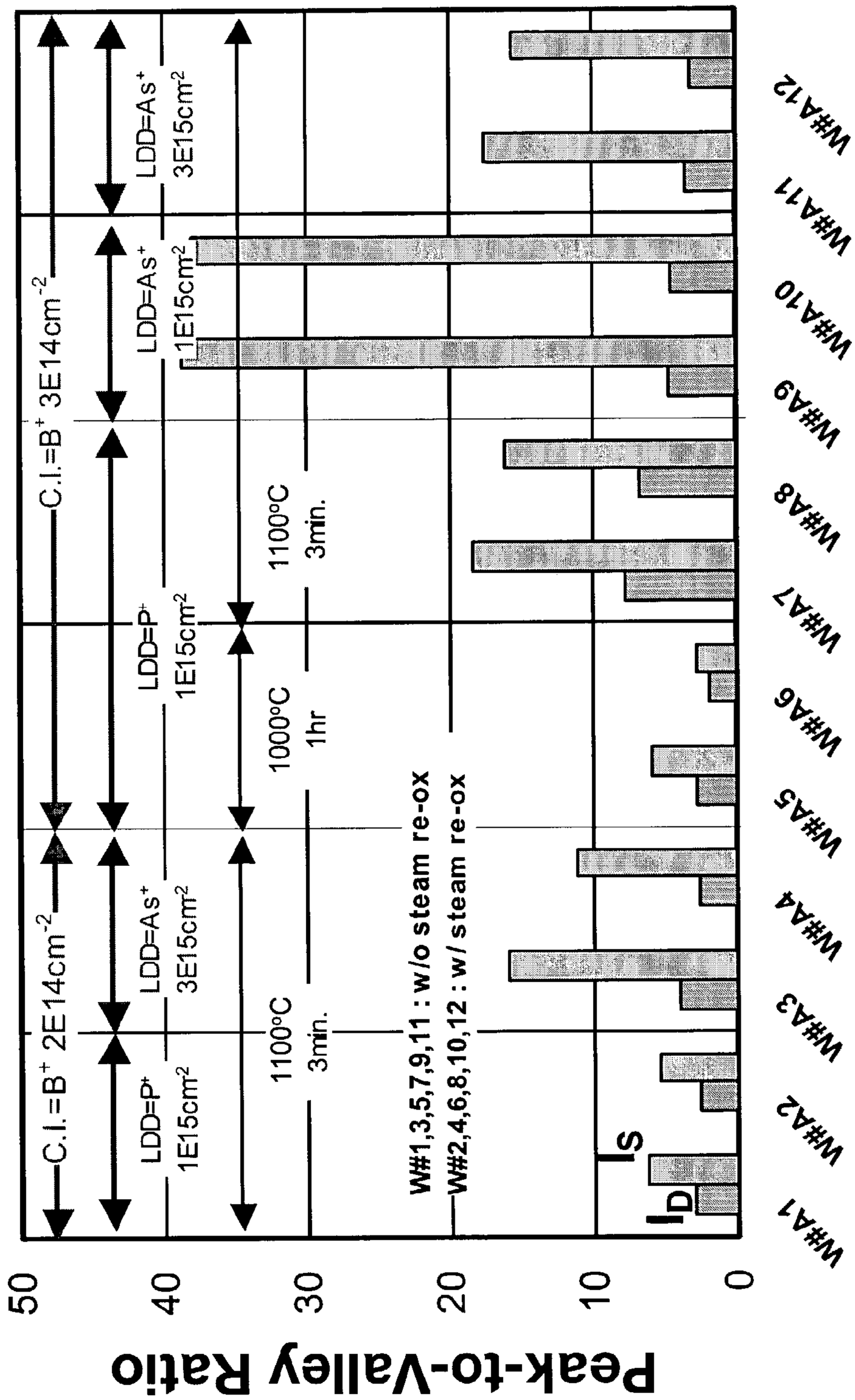

Peak-to-Valley Ratio
50
40
30
20
10
0
W#A1
W#A2
W#A3
W#A4
W#A5
W#A6
W#A7
W#A8
W#A9
W#A10
W#A11
W#A12
I_S
I_D
W#1,3,5,7,9,11 : w/o steam re-ox
W#2,4,6,8,10,12 : w/ steam re-ox
1000°C 1hr
1100°C 3min.
LDD=P+ 1E15cm-2
C.I.=B+ 3E14cm-2
LDD=As+ 3E15cm-2
LDD=As+ 1E15cm-2

Fig. 17H

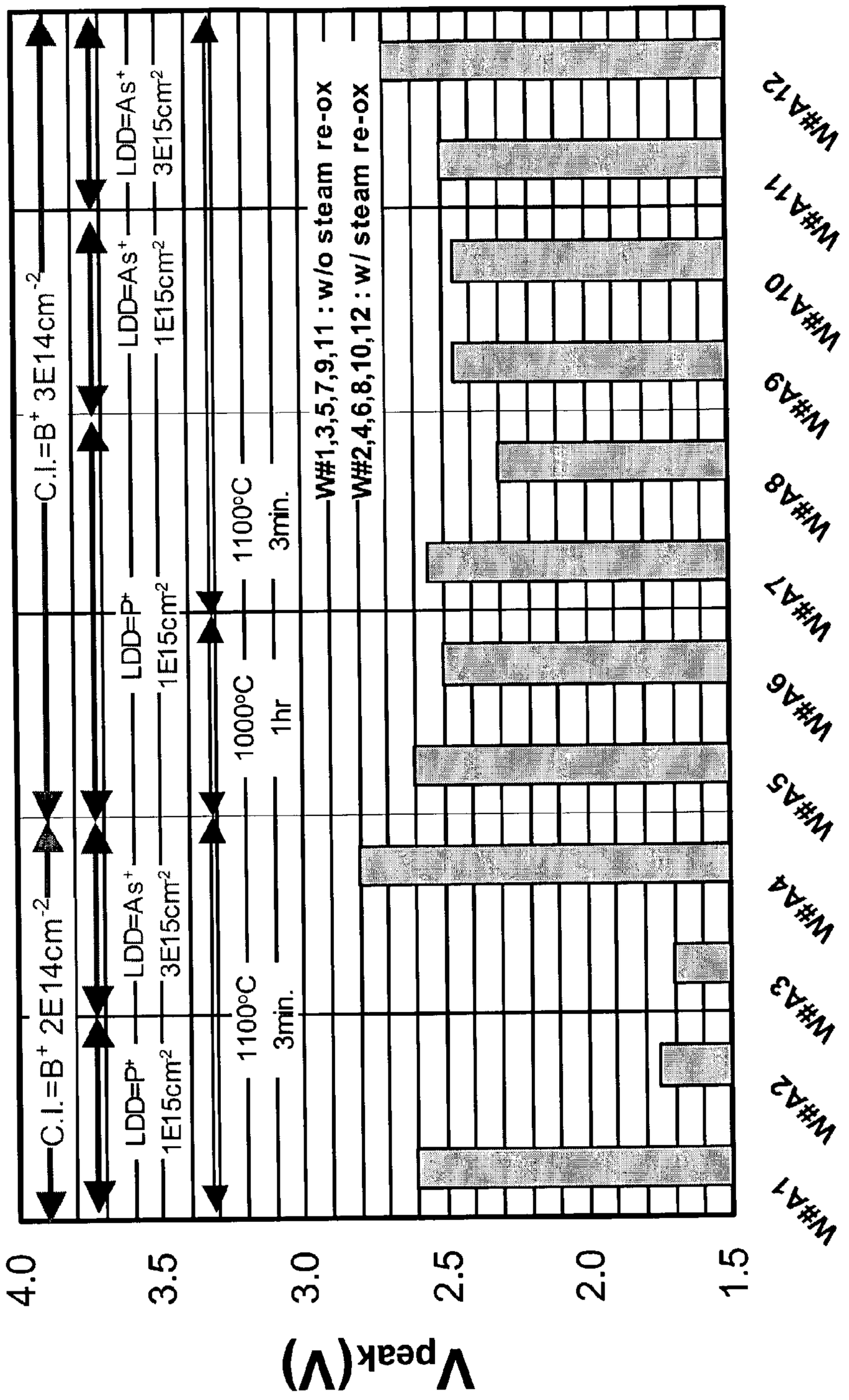

C.I.=B+ 3E14cm-2
LDD=As+
3E15cm-2
C.I.=B+ 2E14cm-2
LDD=As+
3E15cm-2
C.I.=B+ 3E14cm-2
LDD=P+
1E15cm-2
C.I.=B+ 2E14cm-2
LDD=P+
1E15cm-2
1000°C
1hr
1100°C
3min.
W#1,3,5,7,9,11 : w/o steam re-ox
W#2,4,6,8,10,12 : w/ steam re-ox
W#A12
W#A11
W#A10
W#A9
W#A8
W#A7
W#A6
W#A5
W#A4
W#A3
W#A2
W#A1
4.0
3.5
3.0
2.5
2.0
1.5
Vpeak(V)

Fig. 17J

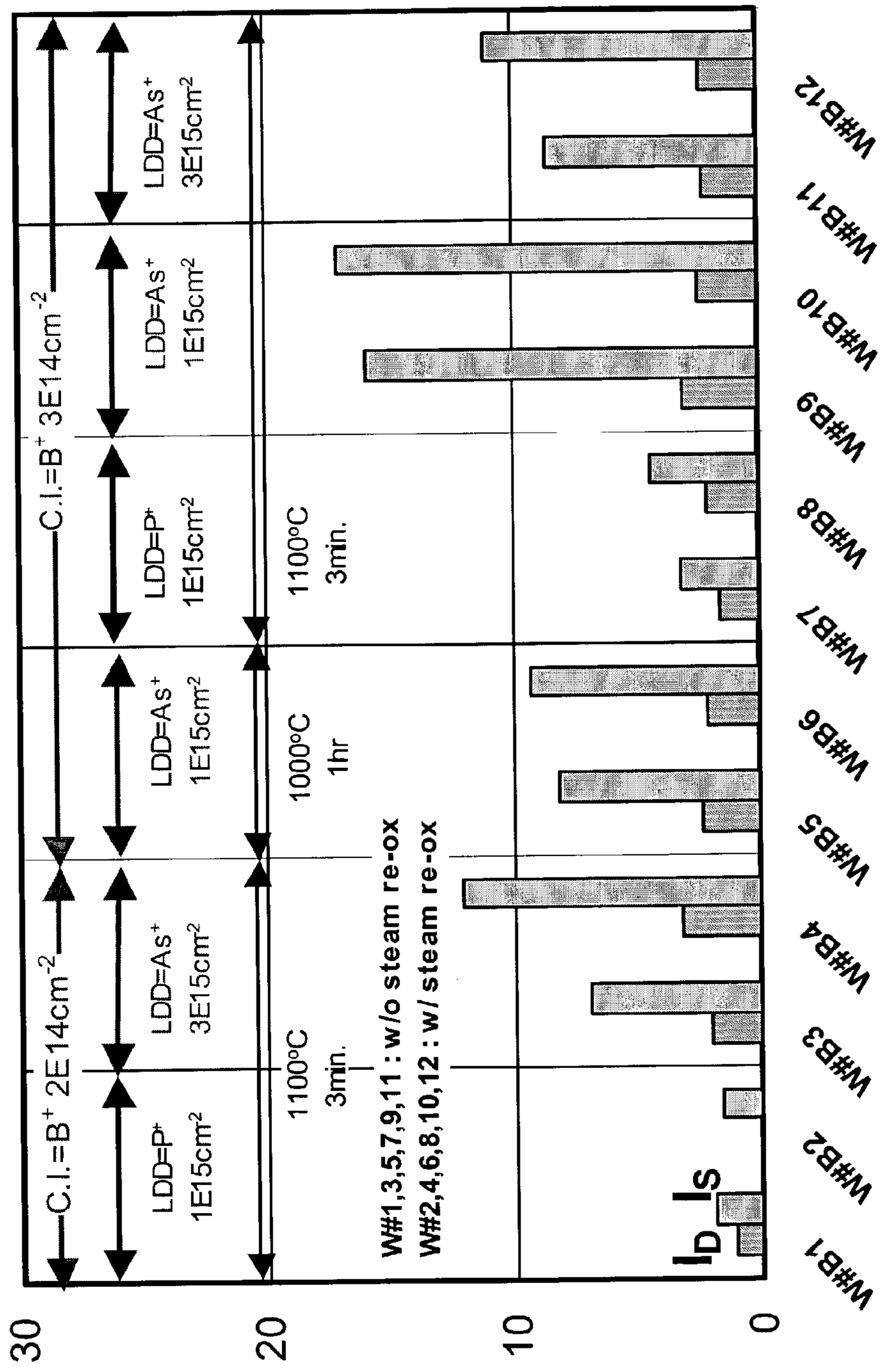
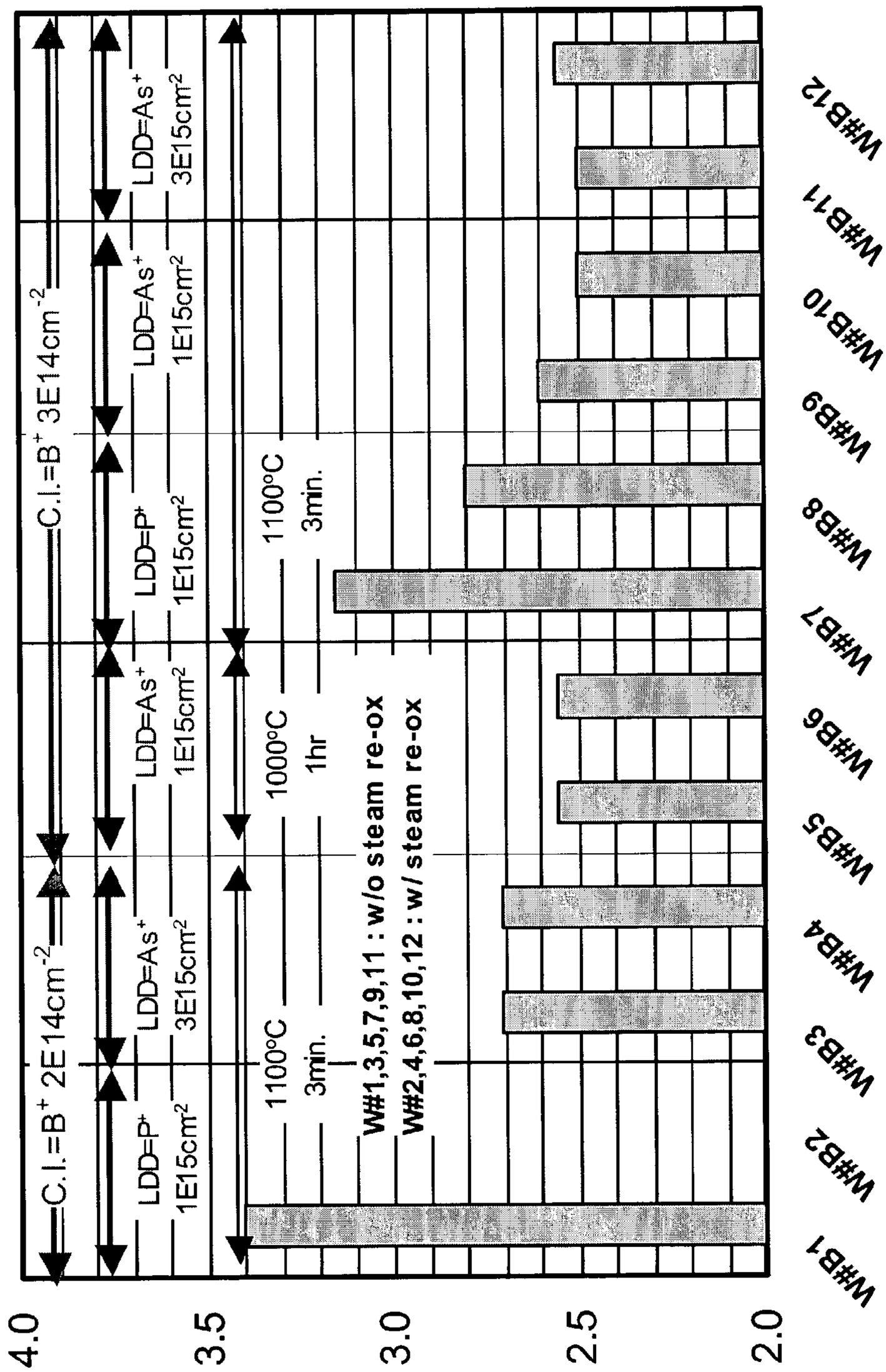

Peak-to-Valley Ratio
30
20
10
0
I_D I_S
W#B1
W#B2
W#B3
W#B4
W#B5
W#B6
W#B7
W#B8
W#B9
W#B10
W#B11
W#B12
W#1,3,5,7,9,11 : w/o steam re-ox
W#2,4,6,8,10,12 : w/ steam re-ox
3min.
1100°C
1hr
1000°C
3min.
1100°C
LDD=P+ 1E15cm-2
LDD=As+ 3E15cm-2
C.I.=B+ 2E14cm-2
LDD=As+ 1E15cm-2
LDD=P+ 1E15cm-2
LDD=As+ 1E15cm-2
C.I.=B+ 3E14cm-2
LDD=As+ 3E15cm-2

Fig. 17K


W#B12
W#B11
W#B10
W#B9
W#B8
W#B7
W#B6
W#B5
W#B4
W#B3
W#B2
W#B1
C.I.=B+ 3E14cm-2
LDD=As+ 3E15cm2
C.I.=B+ 2E14cm-2
LDD=As+ 1E15cm2
LDD=P+ 1E15cm2
1000°C 1hr
1100°C 3min.
W#1,3,5,7,9,11 : w/o steam re-ox
W#2,4,6,8,10,12 : w/ steam re-ox
4.0
3.5
3.0
2.5
2.0
Vpeak(V)

METHOD OF FORMING A NEGATIVE DIFFERENTIAL RESISTANCE DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to the following applications, all of which are filed simultaneously herewith, and which are hereby incorporated by reference as if fully set forth herein:

Process for Controlling Performance Characteristics of a Negative Differential Resistance (NDR) Device; Ser. No. 10/314,785;

Integrated Circuit Having Negative Differential Resistance (NDR) Devices With Varied Peak-to-Valley Ratios (PVRs); Ser. No. 10/321,031;

FIELD OF THE INVENTION

This invention is directed to processes for making semiconductor devices, circuits, dies and systems, particularly those that utilize negative differential resistance (NDR) field-effect transistor (FET) elements.

BACKGROUND OF THE INVENTION

Silicon based devices that exhibit a negative differential resistance (NDR) characteristic have long been sought after in the history of semiconductor devices. A new type of CMOS compatible, NDR capable FET is disclosed in the following King et al. applications:

Ser. No. 09/603,101 entitled "A CMOS-PROCESS COMPATIBLE, TUNABLE NDR (NEGATIVE DIFFERENTIAL RESISTANCE) DEVICE AND METHOD OF OPERATING SAME"; and

Ser. No. 09/603,102 entitled "CHARGE TRAPPING DEVICE AND METHOD FOR IMPLEMENTING A TRANSISTOR HAVING A NEGATIVE DIFFERENTIAL RESISTANCE MODE" now issued as U.S. Pat. No. 6,479,862 on Nov. 12, 2002; and

Ser. No. 09/602,658 entitled "CMOS COMPATIBLE PROCESS FOR MAKING A TUNABLE NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICE;

all of which were filed Jun. 22, 2000 and which ate hereby incorporated by reference as if fully set forth herein. The advantages of such device are well set out in such materials, and are not repeated here.

As also explained in such references, NDR devices can be used in a number of circuit applications, including multiple-valued logic circuits, static memory (SRAM) cells, latches, and oscillators to name a few. The aforementioned King et al. applications describe a break-through advancement that allows NDR devices to be implemented in silicon-based IC technology, using conventional planar processing techniques as for complementary metal-oxide-semiconductor (CMOS) FET devices. The integration of NDR devices with CMOS devices provides a number of benefits for high-density logic and memory circuits.

It is clear, from the advantages presented by the above-described NDR device, that overall improvements in manufacturing, testing and operation of the same are desirable to refine and proliferate such technologies.

In addition, enhancements in trap location control, trap energy level control, and trap formation, are also useful for these types of NDR devices, and could be beneficial to other types of trap-based devices as well.

Furthermore, the prior art to date has been limited generally to devices in which the peak-to-valley ratio (PVR) is not easily adjustable. It would be useful, for example, to be able to control the PVR directly during manufacture, so as to permit a wide variety of NDR behaviors for different circuits on a single die/wafer. Alternatively, the ability to control PVR during normal operation of a device would also be useful, but is generally not possible with current NDR technologies.

SUMMARY OF THE INVENTION

The object of the present invention, therefore, is to address the aforementioned limitations in the prior art, and to provide additional embodiments of trapping devices, NDR devices, and methods of making, operating and testing the same. These and other objects are accomplished by various embodiments of the present invention as described in detail below, it being understood by those skilled in the art that many embodiments of the invention will not use or require all aspects of the invention as described herein.

A first aspect of the invention, therefore, concerns a method of forming a silicon based negative differential resistance (NDR) field effect transistor (FET) comprising the preferred steps of: providing a substrate; forming a first NDR region for the NDR FET over a first portion of the substrate using a first impurity, the first NDR region being adapted for imparting an NDR characteristic to the NDR FET; placing a second impurity in the first portion of the substrate to adjust a threshold voltage characteristic of the NDR FET; performing a first thermal treatment operation for the NDR FET after the above are completed; forming a gate insulating layer for the NDR FET over the first portion of the substrate; performing a second thermal treatment operation for the NDR FET; forming a gate electrode for the NDR FET; forming a source region and a separate drain region for the NDR FET adjacent to the gate electrode, the source region and drain region being coupled through an NDR FET channel located in the first portion of the substrate.

In this manner, an NDR FET preferably operates with a negative differential resistance characteristic when sufficient charge carriers from the channel are temporarily trapped in the first NDR region. The first impurity is preferably a first type dopant, and the second impurity is preferably a second type dopant, which is opposite to the first type dopant. The first thermal treatment operation is preferably performed with a furnace, while the second thermal treatment operation is preferably performed with a rapid thermal anneal system. Furthermore, in addition to the above, a third thermal treatment operation is preferably performed after the gate electrode is formed.

In later steps, a silicide contact to the gate electrode and/or one or both of the source region and the drain region can be formed.

Some embodiments of the invention, therefore, are silicon based negative differential resistance (NDR) field effect transistor (FET) which have a peak-to-valley current ratio (PVR) that exceeds ten (10) over a temperature range of 50° C. In some instances, a PVR can exceed one thousand (1000) over a temperature range of 100° C.

In other embodiments, a silicon on insulator (SOI) substrate is used; a variety of substrates are suitable for the present invention, including silicon carbide (SiC) or strained Si.

The impurities added to the FET are used as charge trapping sites, which preferably have an energy characteristic that is higher than a conduction band edge of the substrate.

In other embodiments, an NDR FET and a non-NDR FET are made at the same time using common manufacturing operations. The non-NDR FET is formed in a second region of the semiconductor substrate. For example, isolation regions, LDD implants, gate insulators, gate electrodes, contacts, source/drain implants, etc., can be done using a common processing step. In such instances, an NDR region for an NDR device is preferably constructed from a gate insulator region for an NDR FET.

In still other embodiments, two different types of NDR devices can be formed in a common substrate. Thus, a second NDR region for another NDR element is formed over a third region of the semiconductor substrate, the second NDR region being adapted for imparting a second NDR characteristic different from an NDR characteristic for a first NDR FET.

A related aspect of the invention, therefore, pertains to a charge-trap based negative differential resistance (NDR) element, which operates with an NDR characteristic defined by a peak current and a valley current. By appropriate distribution of charge traps in a trapping region of the NDR element, including controlling a concentration and energy of the same, a peak-to-valley current ratio (PVR) for the NDR element can be imparted which exceeds ten (10) over a temperature range spanning 50° C.

In other embodiments the PVR can be constructed to vary by less than a factor of five in an operating temperature spanning 25° C. and 125° C. In still other embodiments, the PVR exceeds 1000 in an operating temperature spanning 25° C. and 125° C. The trapping region preferably forms an interface with a channel of a field effect transistor associated with the NDR element.

Other embodiments of charge trapping devices can be similarly constructed to achieve similar performance.

Another aspect of the invention concerns a method of forming a negative differential resistance (NDR) device comprising the steps of: forming a gated silicon-based NDR element; and setting a peak-to-valley ratio (PVR) characteristic of the gated silicon-based NDR element during manufacture of the silicon-based semiconductor transistor to a target PVR value located in a range between a first PVR value and a second PVR value. Thus, a target PVR value can be varied during manufacturing of the NDR device within a semiconductor process such that the NDR device can be configured to have a PVR value ranging between a first usable PVR value and a second usable PVR value, where the first usable PVR value and the second PVR value vary by at least a factor of ten (10).

In some instances, a desired PVR value can be set using a single processing operation, such as an implant.

A preferred approach uses only metal oxide semiconductor (MOS) compatible processing operations. The inventive process is flexible enough so that within a particular manufacturing facility, a first semiconductor substrate on a first wafer and a second separate semiconductor substrate on a second wafer can have different target PVR values imparted at different times. The different PVR values can be programmed into a semiconductor processing apparatus such as an implanter, a furnace, an anneal chamber, a deposition reactor, etc. An NDR voltage onset point (VNDR) is also preferably set during manufacture.

In still other more specific embodiments, a PVR (and/or a VNDR) value can be set during manufacture by controlling one or more general process parameters.

For example, in some embodiments, a PVR and/or VNDR can be set during manufacture by controlling a thickness of a gate insulator grown for the NDR device. In particular, a PVR characteristic can be increased simply by increasing a thickness of the gate insulator. The gate insulator is preferably at least 5 nm thick, and can be a single layer, or a composite of two different materials. In some applications the gate will include both a thermal oxide and a deposited oxide based material. Thus, it is possible in some applications to have a common substrate that includes a silicon based NDR device with a first PVR characteristic using a first gate insulator thickness and a second silicon based NDR device with a second PVR characteristic using a second gate insulator thickness.

In another embodiment, a PVR and/or VNDR can be set during manufacture by controlling a channel length used for a silicon based NDR FET. Because the present invention scales very well, a PVR characteristic tracks a channel length, so that a higher PVR can be achieved by using a smaller channel, and a lower PVR can be achieved by using a longer channel. Accordingly, PVR characteristics can be established through conventional masking operations which define a channel length, and/or which define a source/drain region implant. The channel can also have a size that is defined by a variable sized spacer formed on the sidewalls of a gate electrode. Thus, a PVR value can be increased significantly through even small reductions in channel lengths.

In still another embodiment, a PVR and/or VNDR can be set during manufacture by controlling an impurity species and/or impurity dose introduced into a charge trapping layer associated with the NDR element to match a target charge trap profile. In a preferred approach Boron is selected as the impurity at a dose ranging from $1*10^{14}/cm^2$ to $3*10^{14}$ atoms/cm^2 and an energy of $\leqq$10 keV. This results in a target charge trap profile in which a concentration of charge traps is greater than about $1*10^{19}$ atoms/cm^3 at a trapping region of the charge trapping layer, and less than about $1*10^{18}$ atoms/cm^3 at a bulk region of the charge trapping layer. A PVR can thus be altered merely by selecting another impurity, another dosage, etc. For example, increasing an impurity dose of Boron by 50% can result in an increase of greater than 100% in a PVR characteristic. As with the other PVR processing embodiments, an NDR voltage onset point (VNDR) can also be controlled in this fashion.

In still another embodiment, a PVR and/or VNDR can be set during manufacture by controlling an overall trap distribution, such as a target location of the charge traps and a target concentration of the charge traps. In a preferred embodiment, the charge traps are distributed within a target location is a region that is less than about 0.5 nm thick. Furthermore, a concentration of traps is arranged so that an interface concentration is least an order of magnitude greater than in bulk areas of the charge trapping layer.

In other embodiments, a PVR and/or VNDR can be set during manufacture by controlling a rapid thermal anneal (RTA) operation. A preferred approach is to use a short cycle at a temperature that exceeds 1000° C. for at least part of the cycle in a conventional lamp based chamber. This type of operation serves to focus and concentrate charge traps at a channel interface region, as opposed to bulk regions.

In still other embodiments, a PVR and/or VNDR can be set during manufacture by controlling a lightly doped drain operation, including an implant species and/or dosage, per-

formed during formation of a lightly doped drain region operation. In a preferred embodiment, arsenic is used as the dopant species at a dosage in excess of $1*10^{15}$ atoms/cm^2 to effectuate the implant operation. In other embodiments, phosphorus is used as the dopant species at a dosage in excess of $1*10^{15}$ atoms/cm^2 to effectuate the implant operation. Since Arsenic achieves a PVR that is at least 2 times greater than Phosphorus, it is preferred for those applications where PVR is more critical to the operation of a circuit.

Related aspects of the invention concern a semiconductor processing apparatus for manufacturing a negative differential resistance (NDR) device on a silicon wafer which can be programmed to tailor a specific PVR value on a wafer-by-wafer basis (or even die by die). The apparatus is preferably located in a conventional semiconductor fab, and includes a programmable controller responsive to a negative differential resistance (NDR) related process recipe associated with making the NDR device. An NDR related process recipe includes one or more processing steps associated with effectuating a target peak-to-valley current ratio (PVR) for an NDR device. The processing chamber coupled to the programmable controller is configured to perform at least one semiconductor processing operation on the silicon wafer based on the NDR related process recipe. The semiconductor processing operation can be varied within the processing chamber to achieve a PVR value that varies between a first value, and a second value that is at least twice the first value.

In other embodiments, the PVR value can be varied between 10 and 100 in the semiconductor processing apparatus. The process chamber can be an implanter, an RTA chamber, a deposition reactor etc.

Other aspects of the invention concern different types of optimizations for charge trap profiling for charge trap devices, including NDR devices.

In an NDR FET embodiment, counter-doping is performed to improve a threshold voltage. Thus, a semiconductor device having a control gate, a source region, and a drain region is formed using the steps of: providing a substrate having a first type of conductivity; forming a channel between the source and drain region for carrying the charge carriers between the source and drain regions; the channel is doped in two separate operations such that: during a first channel doping operation the channel is doped with first channel impurities that also have the first type of conductivity; during a second channel doping operation the channel is counter-doped with second channel impurities that have a second type of conductivity. The second type of conductivity is opposite to the first type of conductivity. As a result of the first channel doping operation and the second channel doping operation the channel region as formed has a net first type of conductivity. A charge trapping region that has an interface with the channel is also formed. The charge trapping region has charge trapping sites, which temporarily trap charge carriers along the interface and permit the device to operate with a negative differential resistance characteristic. The charge trapping sites are derived at least in part from the first channel impurities forming a charge trap distribution that is substantially concentrated at the interface.

In a preferred embodiment, Arsenic is used for the second channel doping operation, while Boron is used for the first channel doping operation. While silicon is used as a preferred substrate, other substrates could be used, such as SOI, SiC, strained Si, etc. Moreover, different crystal orientation variants of silicon (111, 100, 110) may result in different charge trapping characteristics.

The charge trapping region is typically formed as part of gate insulator for the semiconductor device. In other variations, the charge traps can be directly implanted through a gate insulator after the latter is completed. In still further variants, the charge traps can be formed as part of a two layer trapping region, such as would be derived from a combined thermal oxide and deposited oxide.

In other variations, the charge trapping region can be engineered to not extend throughout an entire length of the interface with the channel. In other instances, the charge trapping region extends from a source region to enhance source side trapping. In still other embodiments, trapping sites are distributed unevenly along the interface to effectuate a variable trapping rate for the energetic carries along the interface. A trapping rate can also be controlled in some instances, so that it varies substantially proportional to a distance along the interface, and/or is preferentially greater in one region over another—i.e., such that in a source region it is greater than that near a drain region.

In other embodiments, the charge trapping sites are formed in two distinct operations. For example, an implant operation is used for forming a first set of charge trapping sites, and a heat treatment operation (such as in an steam ambient) forms a second set of charge trapping sites. In still other embodiments, different implants could be used of the same species, or different atomic species to create different types of charge traps (i.e., such as Boron and silicon or metal nanoparticles).

A further related aspect of the invention concerns using annealing operations to help ensure that impurities are preferentially concentrated at an interface, where they can form appropriate trap sites. This is achieved by forming a silicon based negative differential resistance (NDR) semiconductor device with the steps of: providing a substrate; and forming a channel region for carrying a current of charge carriers for the silicon based NDR semiconductor device; and implanting first impurities into the channel region; and forming a first dielectric layer that has an interface with the channel; and annealing the channel region to reduce implantation defects and distribute the first impurities so as to concentrate them along the interface with the channel. The first impurities as distributed along the interface form charge trapping sites with an energy level adapted for temporarily trapping the charge carriers to effectuate an NDR characteristic.

In a preferred embodiment, the first impurities have a first conductivity (p) type that is the same as the substrate. The silicon based NDR semiconductor device is typically a field effect transistor (FET), but can include other charge trap based NDR devices.

In still another variant, additional annealing operations can be performed to further enhance a trap distribution. Thus, this implementation involves performing a plurality of separate annealing operations on the semiconductor structure, wherein at least a first one of the separate annealing operations is adapted so as to distribute and concentrate the carrier trapping sites along an interface with the transistor channel region and with a reduced concentration in a bulk region of the trapping layer. Later separate annealing operations are adapted to alter a concentration and/or arrangement of the charge trapping sites along the interface.

A further related aspect, therefore, concerns a silicon based field effect transistor (FET) comprising a trapping layer proximate to a transistor channel region for the FET, the trapping layer including a carrier trapping sites configured for trapping and de-trapping carriers from the channel region. The carrier trapping sites are distributed such that a

concentration of the carrier trapping sites in a bulk region of the trapping layer is at least one order of magnitude less than it is along an interface with the transistor channel region. In this fashion, the FET can exhibit negative differential resistance as a result of the trapping and de-trapping of carriers.

In a preferred embodiment, a concentration of the carrier trapping sites at the interface per cubic centimeter is at least two orders of magnitude greater than a concentration of the carrier trapping sites within the bulk region of the trapping layer. Furthermore, the concentration of an impurity per cubic centimeter used for the carrier trapping sites is at least two times higher at a trapping layer-channel interface than in the channel region.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a preferred embodiment of a negative differential resistance (NDR) field effect transistor (FET) of the present invention;

FIG. **2** is a representative plot of the current-vs.-voltage characteristic of the NDR FET of FIG. **1**;

FIG. **3**A is a band diagram generally illustrating the energy relationship of conduction bands, valence bands and charge trapping sites of a charge trapping region, including variants which can be used in a preferred embodiment of the present invention;

FIG. **3**B is a plot of the impurity concentration vs. depth in one embodiment of the NDR FET;

FIG. **4** depicts the overall steps used in a preferred process to make NDR devices, including an NDR FET of the present invention;

FIGS. **5** to **16** generally illustrate the steps used in a preferred embodiment of an NDR device manufacturing process of the present invention.

FIG. **5** shows a schematic cross-sectional view of a starting substrate used to manufacture an NDR element—including a preferred NDR FET embodiment of the present invention—as well as other conventional semiconductor elements and devices;

FIG. **6** is a schematic cross-sectional view showing the step of forming electrically isolated active areas in surface regions of the substrate;

FIG. **7** is a schematic cross-sectional view showing the step of forming a sacrificial insulating layer on the surface of the substrate in an area where an NDR FET of a preferred embodiment is to be formed;

FIG. **8** is a schematic cross-sectional view showing the step of selectively introducing a first type of impurities into the surface of the substrate in an area where an NDR-FET of a preferred embodiment is to be formed;

FIG. **9** is a schematic cross-sectional view showing the step of selectively introducing a second type of impurities into the surface of the substrate in an area where an NDR-FET of a preferred embodiment is to be formed, as part of a counter-doping step;

FIG. **10** is a schematic cross-sectional view showing the step of forming an additional insulating layer on various regions of the surface of the substrate where active devices, including NDR FET and other conventional FETs, are to be formed;

FIG. **11** is a schematic cross-sectional view showing the step of depositing a gate film for both NDR FETs and conventional FETs;

FIG. **12** is a schematic cross-sectional view showing the step of patterning the gate film into gate electrodes for both NDR FETs and conventional FETs;

FIG. **13** is a schematic cross-sectional view showing the effects of one or more post-gate oxidation anneal steps used to increase a density of charge traps at a channel interface of the NDR FET of a preferred embodiment;

FIG. **14** is a schematic cross-sectional view showing the step of forming source and drain extension regions with an Arsenic implant;

FIG. **15** is a schematic cross-sectional view showing the step of forming more heavily doped source/drain contact regions for an NDR FET and other conventional FETs;

FIG. **16** is a schematic cross-sectional view showing the final results of depositing an electrically insulating interlayer film, forming contact holes in the interlayer film, and depositing a metal layer and patterning the metal layer to form interconnections to the NDR-FET and conventional FETs.

FIGS. **17**A–**17**K are charts, graphs and other depictions of experimental data obtained for various embodiments of an NDR FET device.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is now described with reference to the Figures provided herein. It will be appreciated by those skilled in the art that the present examples are but one of many possible implementations of the present teachings, and therefore the present invention is not limited by such.

The present invention is expected to find substantial uses in the field of integrated circuit electronics as an additional fundamental "building block" for digital memory, digital logic, and analog circuits. Thus, it can be included within a memory cell, within a Boolean function unit, and similar such environments.

Brief Summary of Prior Art

FIG. **1** shows a prior art NDR FET **100** of the type described in the King et al. applications noted earlier. This device is essentially a silicon based MISFET that includes an NDR characteristic as well. Thus, the features of device **100** are created with conventional MOS based FET processing, modified where appropriate as to include operations for effectuating an NDR behavior.

Accordingly, in FIG. **1**, a gate electrode **110** is coupled to a gate terminal **115** for receiving a gate select signal. The device **100** is formed within a substrate **120** (preferably p-type) and includes a well-known source **140** and drain region **150** coupled by a channel **135**. A body contact terminal **125** provides a body bias to device **100**, and source/drain voltages are provided through conventional source/drain terminals **145** and **155** respectively. A gate insulator layer **130** is situated between channel **135** and gate electrode **110**. Again, these features are all common to most standard MISFETs; additional conventional features (such as retrograde substrate doping, "halo" or "pocket" doping, gate-sidewall spacers, shallow source and drain junctions) are not shown for purposes of better illustrating the nature of the invention.

The additional features in device **100** which are somewhat different from a conventional FET and which impart an NDR behavior include the following: (1) a slightly thicker gate electrode **130**; (2) a lightly p-type doped channel surface region; and (3) a charge trapping region **137**. These modifications cooperate to impart an NDR behavior to such FET for reasons set out in detail in the aforementioned King et al. applications.

This behavior is illustrated in FIG. **2**, where device drain current versus drain voltage is plotted for two different gate voltages to show how an NDR mode can be affected by a suitable selection of a gate voltage as well. It can be seen that for a fixed gate voltage V_{GS} relative to the source, a drain current I_{DS} firstly increases in a first region **210** with drain-to-source voltage V_{DS}, similarly to the behavior that is seen in drain current in a conventional n-channel MOS transistor. However, in region **220**, beyond a certain drain voltage level, drain current decreases with further increases in voltage, i.e. the device exhibits an NDR mode with NDR characteristics. The drain voltage at which the drain current begins to decrease (i.e., point **225** where $V_{DS}=V_{NDR}$) is adjustable through suitable selections of impurity species, channel length, threshold voltage, etc.

As seen also in FIG. **2**, the invention can be seen as exploiting the fact that, as the threshold voltage V_t dynamically increases (because of the accumulation of trapped charges) with increasing drain-to-source voltage V_{DS}, a drain current I_{DS} (which is proportional to V_g-V_t) will decrease. Thus, a current value depicted in curve **228** will generally follow the set of continuous curves **229** shown in FIG. **2** for a given V_g and varying V_t. Unlike other prior art devices, the so-called "peak-to-valley ratio," a key figure of merit in NDR devices, as well as the NDR onset voltage, can also be precisely tuned through suitable combinations of impurity species, doping concentrations, device geometries and applied voltages. Furthermore, an NDR behavior of the present invention can achieve a PVR well in excess of 100, 1000, or even 10^6 across a wide temperature range (−40° C. to +150° C.), which far exceeds the capabilities of conventional NDR devices.

It will be appreciated by those skilled in the art that the entirety of the preceding description is merely provided by way of background to better illustrate the context of the present inventions, and thus, by necessity, is somewhat abbreviated. It is not intended to be, nor should it be taken, as a complete analysis of the structural, operational or physical of the aforementioned King et al. inventions. Nor should it in any way be construed as limiting in any way of the inventions disclosed therein.

Trap Energy Characteristics

FIG. **3**A illustrates a preferred energy-band diagram (electron energy vs. distance in the direction perpendicular to a semiconductor surface) of device **100** depicted in FIG. **1**. When a gate bias is applied, an inversion layer of electrons is formed at the semiconductor surface, i.e. the FET is turned on. A gate **310** is shown to be heavily doped polycrystalline-silicon (poly-Si), a gate dielectric **330** is shown to be SiO_2, and a silicon semiconductor substrate **320** is p-type as is the case in modern CMOS technologies. Again, it will be understood that other materials known in the art can be substituted instead.

A lower edge E_c of the conduction band of allowed electron energy states for semiconductor material **320** is shown, as well as an upper edge E_v of a valence band of allowed electron energy states. Conventional device physics theories mandates that there are no allowed electron energy states within a band gap corresponding to a range of energies from E_v to E_c. Accordingly, no mobile electron in semiconductor material **320** can have an energy within this range.

As seen in FIG. **3**A, a conduction-band electron in a channel region (near an interface of gate dielectric **330** and semiconductor substrate **320** must lose energy (e.g via a lattice collision) in order to become trapped by a first type of charge trap **336** which has an energy level below E_c. Afterwards, it must be supplied with energy (e.g. from lattice vibrations) in order to be detrapped back into the conduction band in silicon semiconductor substrate **320**. For reasons, which are apparent from the aforementioned King et al. applications, this type of trap, therefore, is not particularly useful for effectuating an NDR characteristic.

In contrast, a second type of charge trap **335**, which has an energy level very near but above E_c can trap a conduction-band electron with total energy equal to its energy level, without requiring a lattice collision. Of course, charge trap **335** has an additional benefit in that it can also trap conduction-band electrons which have energies higher than an energy level of such trap. For these second type of traps, a trapped electron can easily move back into an allowed energy state in the conduction band, and hence it is easily detrapped. These second types of traps are particularly suited for adapting a conventional FET to operate with an NDR characteristic. In will be noted that interface traps which are energetically located well above the semiconductor conduction band edge (not shown) will have no effect on FET performance until a significant percentage of the mobile carriers in the channel have sufficient kinetic energy to become trapped.

Thus, a preferred primary mechanism for achieving NDR behavior in an insulated gate field-effect transistor is to trap energetic ("hot") carriers from a channel with traps that also rapidly de-trap. The traps should be configured preferably so that a trap energy level should be higher than the semiconductor conduction band edge, in order for it to primarily (if not exclusively) trap hot carriers. For example, a trap which is energetically located 0.5 eV above the semiconductor conduction band edge can only trap electrons from the semiconductor which have kinetic energy equal to or greater than 0.5 eV. For high-speed NDR FET operation, it is desirable to have the carrier trapping and de-trapping processes occur as quickly as possible, as this permits a rapid and dynamic change in a threshold voltage for the FET.

Thus, the King et al. NDR device uses tunneling to a charge trap, and not tunneling to a conduction band per se as required in some conventional NDR devices such as tunnel diodes. All that is required is that the carriers be given sufficient energy to become trapped in localized allowed energy states within one or more dielectric layers (including for example a gate insulator layer made up of conventional dielectric materials). It is not necessary to set up a complicated set of precisely tuned layers in a particular fashion to achieve a continuous set of conduction bands as required in conventional NDR devices, and this is another reason why such invention is expected to achieve more widespread use than competing technologies.

Finally, the physical distribution of such traps is also described in the King et al. applications, and an approximate illustration of the same is shown in FIG. **3**B. This chart illustrates a general relationship between charge trap concentration and distance. The left side of the graph represents a bulk region of a trapping layer (in this case gate dielectric **330**), which as can be seen, preferably has a very low concentration of charge traps (i.e., something less than 10^{16} atoms/cm^3. The concentration increases rapidly near an interface **360**, and the latter contains a maximum concentration of impurities (in this case Boron as noted with circles) useable as charge traps, preferably in excess of 10^{19} atoms/cm^3, and most preferably in excess of 10^{20} atoms/cm^3. The concentration of Boron then decreases and is less again on a substrate side **320**. The areal concentration of traps should not be excessive, however (i.e., greater than $10^{14}/cm^2$), because this can also lead to undesirable electron

conduction between the source and drain via trap-to-trap hopping or channel-to-trap-to-channel hopping.

As can be seen in FIG. **3**B, a majority of the charge traps should be placed in close proximity to the channel, i.e. within 0.5 nm to 1.5 nm of the gate-dielectric/semiconductor interface, or right at the interface itself. This can be achieved using a low-energy implant of Boron at approximate dose of 2 to $3*10^{14}$ atoms/cm^2. It will be understood by those skilled in the art that the above figures are merely representative, and it is expected that such values (distances, concentrations) will vary in accordance with a particular process geometry, device operational requirements, etc. Thus, the present invention is not limited to any particular arrangement of such traps. A triangle symbol designates an overall "net" p-type doping in the channel, which, for reasons set forth herein, should not be too highly doped p-type, as this will undesirably increase a threshold voltage.

In operation, a trapping/de-trapping mechanism preferably starts at a drain end of the channel, and proceeds towards a source side of the channel, to rapidly shut off the transistor. This is a result of the fact that the electrons have a maximum kinetic energy by the time they teach the drain side of the channel, and thus are more likely to be trapped first in that region. As the voltage on the drain increases past V_{NDR}, the electrons will acquire more and more energy as a result of the increased field, at locations closer to the source. It can be seen from this mechanism as well that the NDR FET has good scaling capabilities, because as a channel length shortens, the trapping/detrapping mechanism can "switch" the transistor off even more rapidly.

This extra degree of freedom—i.e. the ability to independently control a FET channel conductivity through a source/drain bias voltage (in additional to the conventional gate voltage modulation) provides yet another example of the advantages presented by the present invention. Furthermore, this particular channel shut-off mechanism scales as well or better than conventional MOSFET turn-off techniques, which, as is well known, must rely on thinner and thinner oxides (or esoteric materials) to achieve a sufficiently large field to deplete the channel of carriers in the conventional fashion (i.e., through an applied gate voltage).

Overview of Process Flow

A preferred process flow for manufacturing an NDR device that is integrable into a conventional MOS manufacturing process is illustrated in FIG. **4**. The advantage of such process, as described in earlier applications assigned to the applicant, is that additional conventional non-NDR circuitry (memory and logic) can thus be manufactured at the same time.

Thus, as shown in FIG. **4**, an initial substrate is chosen at step **405**, which in a preferred embodiment is silicon, but which could be silicon germanium, silicon on insulator, strained silicon, silicon carbide, or any other desired material. Of course it will be understood that if a non-silicon substrate were selected to implement the present inventions, many of the processing steps below would have to be modified in accordance with well-understood principles known to skilled artisans in this field of art.

At step **410** isolation regions are formed in the substrate, which, in a preferred approach are shallow trench isolation (STI) regions. At step **415**, a sacrificial oxide layer is grown. At step **420**, P wells and N wells are formed in the substrate as well.

At step **425**, impurities are introduced into NDR device regions, designed to facilitate a trapping/de-trapping mechanism noted earlier. Again, a variety of techniques are available for doing this as referenced in the aforementioned King et al. applications, including, for example, a relatively high dose implantation of boron (in excess of $1*10^{14}$ atoms/cm^2) into channel regions of NDR FETs.

At step **430**, an optional NDR channel counter-doping step (n-type dopant implant) is performed, to counter some of the effects of a NDR trap implant, and thus reduce a net p-type channel doping concentration. This results in lowered voltage thresholds, a steeper subthreshold swing, and correspondingly higher PVR values.

At step **435**, an optional thermal anneal is performed, to remove damage to the semiconductor crystal lattice and thereby ensure proper distribution and concentration of the traps within a trapping region step. This is done to ensure that the traps do not migrate too far into the trapping region, causing excessive leakage, slow operation, and poor reliability.

At step **440**, the sacrificial oxide layer is optionally selectively removed and a gate insulator is formed which can be used for both an NDR FET and a regular FET. This insulator can be comprised of multiple layers of dielectric materials, and can be of different thickness and composition in an NDR FET region than in a regular FET region.

At step **445**, an optional thermal anneal is performed (preferably a rapid thermal anneal, or "RTA"), to increase a density of charge traps at a channel/insulator interface.

At step **450**, a gate electrode is formed which, again, can be used for both an NDR FET and a regular FET.

At step **455**, an optional post gate-etch re-oxidation anneal is performed to further modify (if needed) a distribution and density of charge traps at a channel/insulator interface and/or to heal the gate insulator in the regions along the edges of the gate electrodes.

At step **460**, a "lightly doped drain" (LDD) implant is performed to form shallow source and drain regions (which can be for either/both NDR and non-NDR FETs).

At step **465**, an optional anneal is performed to repair any damage to the semiconductor crystal lattice caused by the LDD implant.

At step **470**, spacers are formed (which can be for either/both NDR and non-NDR FETs) along the sidewalls of the gate electrodes to offset the deep source/drain contact regions.

At step **471**, optional raised source and drain contact regions are formed, preferably by selective epitaxial growth of silicon or a silicon-germanium alloy, which can be for either/both NDR and non-NDR FETs.

At step **475**, a high-dose source/drain implant step is performed to form heavily doped source/drain contact regions, which, again, can be for either/both NDR and non-NDR FETs.

At step **480**, an anneal is performed to repair any damage caused by the source/drain implant and to activate the implanted dopant atoms.

At step **485**, an optional silicidation process module is used to form low resistance contacts as required at gate and/or source/drain regions—again, for either/both NDR and non-NDR FETs.

At step **490**, an electrically insulating passivation layer is deposited and holes are formed within this layer to allow electrical contact to regions of either/both NDR and non-NDR FETs.

At step **495**, electrical interconnections (which can be made using copper, aluminum, or other low resistivity material) are formed over the NDR and non-NDR FETs to complete wiring of the devices and form an integrated circuit. Such interconnections can be formed with multiple

layers of conductive material separated from each other by interposing insulating layers with holes ("vias") to allow for selective electrical connection between layers.

Final passivation layers are then typically added in the back end of the manufacturing process as well.

A further detailed description now follows for those steps above which are more germane to the present invention. As many of these steps are conventional, however, they are not explained herein in detail. Many of the particular structures, and formation steps for these layers and regions will depend on desired performance characteristics and process requirements, and thus a variety of techniques are expected to be suitable. Furthermore, while examples of various techniques are presented herein for a manufacturing process embodying the present invention, it will be understood by those skilled in the art that these ate merely exemplary of current state of the art approaches. Thus, the present invention is intended to encompass other yet-to-be developed processes currently unknown to the inventor over time that may replace such techniques and yet still be entirely suitable for use with the present invention.

Details of Process Flow

FIGS. **5** to **16** generally illustrate the detailed operational steps used in a preferred embodiment of an NDR device manufacturing process of the present invention.

In particular, FIG. **5** shows a schematic cross-sectional view of a starting substrate used to manufacture an NDR element (in accordance with step **405** described earlier) —including a preferred NDR FET embodiment of the present invention—as well as other conventional semiconductor elements and devices. As seen in FIG. **5**, a preferred substrate **1000** consisting substantially of silicon (Si) is prepared. Because the NDR-FET and IGFET are n-channel devices, the portions of the substrate in which the NDR-FET(s) and IGFET(s) are to be formed are preferably p-type.

In this regard it will be understood that starting substrate **1000** in FIG. **5** could also refer to a p-type well formed in the surface (within the top 1000 nm) of a starting substrate by ion implantation and/or diffusion, either before or after the definition of "active" areas, in any number of known techniques known to those skilled in the art. It should be noted that substrate **1000** could also be silicon-on-insulator (SOI), and may eventually contain one or more additional layers of silicon-germanium alloy material or silicon carbide material (not shown). When selecting these latter substrates, of course, those skilled in the art will appreciate that the later processing steps described below would have to be modified in well-known ways to accommodate such change.

FIG. **6** is a schematic cross-sectional view showing the step of forming electrically isolated active areas in surface regions of the substrate (in accordance with step **410** described earlier) including in a first area **1015** where an NDR element (such as an NDR FET) is to be formed, and a second area **1015'** where a non-NDR element (such as a conventional FET) is to be formed. To better emphasize the present teachings, in FIG. **6** (and other figures below) the later processing steps are shown in a "split" view to help explain the different impact and result on NDR regions and non-NDR regions across the substrate **1000** for various operational steps described herein. It will be understood by those skilled in the art that these figures are not intended to be to scale, and that actual substrate profiles will likely deviate (perhaps significantly) in an actual manufacturing embodiment. Nonetheless they are helpful to understand the important aspects of the present invention.

Consequently, in FIG. **6**, electrically isolated "field" areas **1010** in a surface of substrate **1000** are formed by any of several current well-established techniques, including local oxidation of silicon (LOCOS) and/or shallow trench isolation (STI). The thickness of an isolation oxide layer **1010** typically falls in a range from 100 nm to 700 nm, while a depth of shallow trench isolation structures typically falls in the range from 100 nm to 1000 nm. Other later developed techniques will be useable with the present invention as well.

Moreover, it should be noted that the precise details of these areas are not critical to the operation of the present invention, but a significant advantage of course lies in the fact that such structures (however formed) can be share by both conventional active devices as well as the NDR devices in accordance with the present teachings. Of course, in some applications it may not be necessary to use such types of isolation regions, and the present invention is by no means limited to embodiments which include the same.

A sacrificial oxide layer **1018** is then grown. It will be understood by skilled artisans that since steps **415** and **420** are conventional and not material to the present teachings, that consequently, they are not explained in detail herein. Additional conventional processing steps (threshold adjusts for example, other insulating layers, or etch stop layers, or plasma/heat treatments) that ate incidental to the present teachings are also omitted to better explain the present invention.

Accordingly, as seen in FIG. **7**, an ion implantation step is performed (as part of step **425** noted earlier) of an impurity species (such as Boron) (shown as circles **1030**) through sacrificial oxide layer **1018** at a dose of approximately 2 to $3*10^{14}$ atoms/cm^2. For reasons set out in the prior King et al. applications, it is preferable to introduce charge traps at or near an interface of substrate **1000**, in those areas **1015** where an NDR element is to be formed. This can be accomplished by one of several known approaches, including ion implantation and/or diffusion of an appropriate species, or deposition of a trap-containing dielectric layer.

While Boron introduced by an implant is preferably used herein, other elemental species may be used as charge traps as well, including silicon, indium, arsenic, phosphorus, antimony, fluorine, chlorine, germanium, or a metallic species. In some instances it may be possible form traps using water (from a steam ambient) as well. Other mechanisms for introducing the impurities can also be used, such as deposition of a layer of material containing the charge traps or charge-trapping species. For example, a doped silicon film can be deposited and oxidized to form an oxide film containing a high density of charge traps.

An advantage of the present invention is that the onset of NDR behavior can be controlled through selecting a target trap energy level. In turn, the trap energy level can be engineered through suitable process control parameters such as through selection of a particular impurity species and/or trapping layer dielectric.

A mask can be used to selectively form the charge trapping region in those areas **1015** where an NDR element is to be formed, and in some instances so that it does not extend across an entire region **1015** of substrate **1000**, but is instead limited to some smaller area corresponding to a later gate region of an NDR FET, or even a limited portion of such gate region. In some cases, for example, it may be desirable to form a trapping region only near a source region, or only near a drain region, depending on the expected device biasing and operational characteristics. To

maximize "source side" trapping, for example, charge traps can be selectively arranged to extend from a source region, and not extend entirely through the channel to a drain side. A variable distribution of traps might be employed along a length of the channel so as to effectuate a trapping rate that varies correspondingly and results in a faster switching speed.

It is expected that routine experimentation will yield a variety of trap distributions for optimizing different characteristics of an NDR FET, such as switching speed, V_{NDR}, noise immunity, leakage, subthreshold swing, V_t, etc. Thus it will be understood by those skilled in the art that while it is shown as extending throughout all of region **1015**, the invention is not limited to such implementations, and in fact a variety of charge trapping structures may be used advantageously for different applications.

Thus, the present detailed description continues with a discussion of FIG. **8**, which is a schematic cross-sectional view showing the step of forming an initial insulating layer (after sacrificial oxide layer **1018** is removed) on the surface of the substrate in a first region **1015** where an NDR FET of a preferred embodiment is to be formed as part of step **425** described above. This initial insulating layer **1020** functions as part of a gate insulator for a to-be-formed NDR FET, and can also serve as a charge trapping region for such NDR FET. It is formed on the surface of substrate **1000** in active areas **1015** by one of several well-known techniques, including thermal oxidation of silicon. Physical vapor deposition and chemical vapor deposition can also be used. This electrically insulating layer **1020** can consist entirely or in part of SiO_2, SiO_xN_y, Si_3N_4, or a high-permittivity dielectric material such as metal oxide or metal silicate or their laminates, or, of course, as a combination of one or more different material layers.

As with other processing steps noted herein, an advantage of the present invention lies in the fact that this layer (as patterned later) can be shared by both conventional and NDR FET devices. Alternatively viewed, from a process integration impact, the existence of such layer in non-NDR regions during these NDR FET formational steps does not negatively impact the structure, performance or reliability of any non-NDR elements. Nonetheless, in some applications it may be desirable to mask and etch layer **1020** in those areas where non-NDR elements are to be formed, so that charge trapping regions are not formed later across all regions of the substrate.

In an alternate embodiment, traps are formed by directly implanting the gate insulator layer **1020** using a combination of energies and species that ensure a high concentration at a channel interface and a low concentration in a bulk region of layer **1020**.

In yet other embodiment, multiple charge trap formation steps could be employed, either as part of a standard process for making a single NDR device, part of a fine-tuning process, or even part of a standard process for making different kinds of NDR devices on the same substrate. For example, some traps could be introduced in the channel region before the gate insulator layer **1020**, and some could be introduced after to achieve a target trap profile, including trap energy, trap concentration and trap distribution. The two different sets of traps could also be different impurities and/or implant species if it is desired to have multiple trap profiles, such as different trap energies to trap different types of charge carriers, or different trap types which trap/de-trap at different rates. In the case where different NDR devices are being made at the same time on a substrate, appropriate masking steps could be used to ensure that any additional subsequent trap formation operations are only performed for selected NDR devices.

FIG. **9** is a schematic cross-sectional view showing the step of selectively introducing a second type of impurity (at least in regions **1015** where an NDR-FET of a preferred embodiment is to be formed) having an opposite conductivity to Boron as part of a counter-doping step **430** noted above. In a preferred approach, this second type of impurity is Arsenic (shown with an "x" **1031** in FIG. **9**) implanted at a concentration of about $1*10^{14}$ atoms/cm^2 and at relatively low energy. This step has the effect of lowering a net p-type concentration later in a surface region of the channel of an NDR FET. This leads to improvements in both threshold (V_t) and sub-threshold swing (S) characteristics. In particular, a V_t of an NDR FET can be reduced, and a steep subthreshold swing can also be realized, both factors which are critical for ensuring proper scaling performance in subsequent generations of submicron devices. These improvements can also be exploited in the form of lower gate bias voltages and larger PVRs for integrated circuit applications using the present inventions.

After the implantation step(s) (for traps and/or counter-doping) are completed, a thermal annealing step (corresponding to step **435** in FIG. **4**) is preferably performed to reduce implantation-induced damage. This can be done in an inert ambient (Ar or N_2) or an oxidizing ambient (O_2 or H_2O) for a predetermined time (e.g., several hours) at a predetermined temperature (e.g, 550° C.). Other techniques (e.g. RTA), temperatures, and times will be apparent to skilled artisans from the present teachings and from routine experimentation for any particular implementation. The purpose of this step is to further ensure that the trap distribution will be concentrated at an interface with the channel, rather than within a bulk region of trapping layer **1020**.

In the absence of an anneal step, for example, Boron may undesirably diffuse rapidly with the aid of point defects into a bulk region of the trapping layer, resulting in a high level of gate leakage current. It is preferable to have a high concentration of traps at a channel/gate-insulator interface, and a relatively low concentration in a bulk region of the gate insulator. These concentrations should preferably be at least two or three orders of magnitude in difference measured in terms of atoms per cubic centimeter. By keeping the trapping sites in this region (i.e., within about 0.5 nm of the channel interface) gate leakage current is further minimized. The size of this region will vary, of course, from geometry to geometry for any particular generation of process technologies.

Other generally accepted techniques for reducing such implant damage that are known in the art (at this time or later developed) will also be equally useable with the present invention. Again, it will be understood by those skilled in the art that a trap formation process that does not use an implant, or does not result in excessive trap sites in the bulk of the gate region, will not necessarily require such an annealing step. For example, as discussed herein, if the traps are implanted (placed) directly through the gate layer at a later time, their distribution can be concentrated in a particular region through a suitable selection of energies. Alternatively, a composite gate oxide can be used (i.e., an implant, a thermal oxidation, and then a deposition; or a deposition, an implant, and then a thermal oxidation) to incorporate the traps at an interface using a thermal cycle instead. Further variations will be apparent to those skilled in the art from the present teachings.

In any event, at least in those implementations where trapping layer **1020** is formed over the entire substrate, it is then selectively removed (not shown) from the areas where conventional FETs are to be formed (region **1015'**), and from any other areas (including in region **1015**) where it is not needed/desired.

FIG. **10** is a schematic cross-sectional view showing the step of forming an additional insulating layer **1040** on substrate **1000** to serve as a high quality gate insulator for both NDR FET and other conventional FETs (corresponding to step **440** in FIG. **4**). Gate insulating film **1040** can be formed by one of several techniques, including physical vapor deposition and chemical vapor deposition. Gate insulating film **1040** can consist entirely or in part of SiO_2, SiO_xN_y, Si_3N_4, combinations of the same, or a high-permittivity dielectric material such as metal oxide or metal silicate or their laminates.

If the gate insulating layer **1040** is formed by thermal oxidation, then it may be located beneath layer **1020**, and may be thinner in the areas where NDR FETs are to be formed (region **1015**) than in other areas (including in region **1015'**). In this case, the layer **1040** will serve as the charge trapping layer rather than as a high-quality gate insulator, with charge traps formed via the incorporation of impurity species during the thermal oxidation process or subsequent process steps.

It should be noted that additional layer **1040** is unnecessary in those cases where conventional FETs are not being made at the same time, because a single oxide layer can be grown with sufficient thickness of course as part of layer **1020**. Nonetheless, a composite gate is preferred in mixed embodiments of NDR and non-NDR FET elements to accommodate the need for additional gate insulators in the latter devices.

After the gate insulator is formed, an additional thermal annealing operation (corresponding to step **445** in FIG. **4**) is preferably performed to further optimize a distribution of the charge traps—i.e. increase their concentration at a channel/gate-insulator interface. This operation is preferably performed with a rapid thermal anneal (RTA) at 1100° C. for a short time—i.e. between 1 and 10 minutes. Other temperatures and times will be apparent to skilled artisans from the present teachings and from routine experimentation for any particular implementation. The inventor has further determined that an RTA operation is superior to a conventional furnace operation (i.e., 1 hour at 1000° C. in a N_2 ambient) in terms of enhancing a distribution of trapping sites near the Si/SiO_2 interface.

As the distribution of trapping sites affects the ultimate peak-to-valley ratio (PVR) of the NDR device of the present invention, selection/control of this process step can be exploited to set such PVR to a target value. In other words, different applications requiring different PVRs could be manufactured by simply adjusting a time or temperature of an RTA, or by selecting an RTA operation over a furnace operation to increase a PVR value.

FIG. **11** is a schematic cross-sectional view showing the step of depositing a gate electrode layer **1050** for both NDR FETs and conventional FETs. The gate electrode material **1050** may be polycrystalline silicon (poly-Si) or a silicon-germanium alloy poly-SiGe), or it may be a metal or metal alloy or conductive metal nitride or conductive metal oxide. An advantage of the present invention, again, is apparent because the gates of both NDR FETs and conventional FETs can be made of the same material, and formed at the same time.

If gate electrode material **1050** is poly-Si or poly-SiGe, it may be doped in-situ during the deposition process or it may be doped ex-situ by ion implantation and/or diffusion, to achieve low resistivity and a proper work function value. The final gate electrode also may consist of a multi-layered stack, with a lowest layer providing a desired gate work function and overlying layer(s) providing sufficient thickness and conductivity.

The gate electrode layer **1050** is then patterned using standard lithography and etching processes to form multi-layer gate electrodes **1060** and **1060'** (FIG. **12**) which corresponds to step **450** (FIG. **4**). At this point, an optional post-gate-etch re-oxidation anneal operation (step **455** in FIG. **4**) is performed in some instances to heal any damage to the gate insulator along the edges of the gate electrodes and possibly to further enhance a concentration (or formation) of charge traps.

While a steam anneal can be used (e.g., 10 minutes at 750° C. in steam ambient, followed by 1 minute at 1050° C. in N_2) for some embodiments, the beneficial aspects of such approach are not uniform across all implementations. In other words, while some thinner (i.e., 5.5 nm) gate insulator applications may benefit from such operation, other relatively thicker gate (i.e., 7 nm) insulator applications may not. This is because it is believed that while the steam may assist in forming new water based traps near an Si/SiO_2 interface, the temperature exposure also serves to counteract this effect by driving some of the trap-associated impurity atoms away from such interface into a bulk region. When the gate is relatively thick, this results in a greater migration/dilution of the trap concentration near the interface, thus resulting in reduced performance. Thus, the inventor believes that a conventional post-gate reoxidation anneal may be more useful for thinner gate oxides. Nonetheless, any comparable annealing mechanism that both creates new traps and yet minimizes diffusion of existing traps could also be employed for either application (thin or thick gate insulators).

FIG. **13** is a schematic cross-sectional view depicting a simplified explanation of the resulting effects of one or more annealing steps, which, as noted above, are used to increase a density of charge traps **1037** at a channel interface of the NDR FET of a preferred embodiment. It will be understood that this figure, and many elements therein—the traps, the trap location, etc., are not drawn to scale, and that the depiction is merely intended as an instructive tool for comprehending the present teachings.

FIG. **14** is a schematic cross-sectional view showing the step of forming lightly doped source/drain regions corresponding to step **460** in FIG. **4**. In a preferred embodiment, an n-type dopant such as Arsenic (shown with an * symbol) is implanted with an energy of 10 keV and a dosage of $3*10^{15}$ atoms/cm^2. The inventor has determined that Arsenic is superior to Phosphorus in terms of achieving a higher overall PVR for an NDR device of the present invention. While the reasons for this are not entirely clear, it is believed that As diffuses more slowly than P so that a higher doping concentration can be achieved with the former. This in turn results in a higher peak electric field in a drain region of the channel, creating more energetic electrons, and thus more charge trapping. A lower V_{NDR} can be achieved for similar reasons.

Accordingly, a desired PVR value can also be controlled to some extent for an NDR device through suitable selection of an LDD dopant species, energy, etc. It should be noted that the shallow source/drain extension regions may be formed in the NDR-FET areas **1015** simultaneously with the

shallow source/drain extension regions in the IGFET areas **1015**'. The dopant concentration and junction depth of the shallow source/drain extensions for the NDR-FET can be made to be the same, or different from those for the NDR-FET, if necessary, by selective (masked) ion implantation. Furthermore, in some embodiments, it may be desirable to form the shallow source/drain regions after the heavily doped source/drain regions described below.

A conventional anneal operation may be performed after the LDD implant (as noted in step **465**) to anneal out any damage, and further control a target PVR.

FIG. **15** is a schematic cross-sectional view showing the step of forming more heavily doped drain/source regions **1070** and **1071** for an NDR FET and other conventional FETs (as noted in steps **470–475**). In this case, deep source and drain regions are offset from the edges of the gate electrode by spacers **1025** formed along the sidewalls of the gate electrodes. The sidewall spacers are formed by conformal deposition and anisotropic etching of a spacer film in conventional fashion. The thickness of this spacer film determines the width of the sidewall spacers and hence the offset from the gate electrode. A variety of such spacer techniques are known in the art and can be used with the present invention. Again, preferably, sidewall spacers are formed at the same time for both NDR and non-NDR FETs.

Source and drain regions (step **475** in FIG. **4**) **1070** and **1071** are formed by ion implantation of n-type dopants such as arsenic and/or phosphorus and subsequent thermal annealing (step **480**) using conventional techniques to remove damage and to activate the dopants. In this particular implementation, gate electrodes **1060** are sufficiently thick to prevent implanted ions from entering the surface of substrate **1000** underneath the gate electrodes.

As shown in a simplified perspective in FIG. **16**, device fabrication is completed (steps **485**, **490** and **495** in FIG. **4**) by formation of silicide **1085**, **1080** on the surfaces of the source and drain contact regions and possibly the gate electrode to provide low-resistance metal-to-semiconductor contacts, followed by deposition of one or more electrically insulating interlayer films **1075**, **1077**, formation of contact holes and filing of these holes with metal plugs **1081**, **1086**, deposition and patterning of one or more metal layers **1083** and **1087** to form interconnections, and a low-temperature (350° C.–450° C.) anneal in a hydrogen-containing or deuterium-containing ambient (forming gas).

Multiple layers of metal wiring, if necessary, may be formed by deposition and patterning of alternate layers of insulating material and metal. It will be understood that the silicide contacts **1080** and **1085** may be formed of low resistivity phases of titanium silicide, molybdenum silicide, cobalt silicide, or nickel silicide compounds, and may be connected to only one of the gate or source/drain regions depending on the particular application. The plugs **1081** and **1086** may be formed of Tungsten, Aluminum, Copper or other metallic materials. Insulating films **1075** and **1077** may be CVD films, spin-on glass, and/or any other accepted insulating material, including air gaps. Metal interconnect layers **1083**, **1087** may be Aluminum, Copper, or some other low resistivity metal.

In this manner, a semiconductor device comprising one or more IGFET elements and one or more NDR-FET elements can be manufactured on a common substrate utilizing a fabrication sequence utilizing conventional processing techniques. Those skilled in the art, of course, will appreciate that the aforementioned steps might be useful in other processing environments as well, including for manufacturing other NDR devices such as silicon based resonant tunneling diodes, two-terminal NDR FETs adapted as diodes, thyristors, etc.

While not shown explicitly, an NDR FET and a conventional IGFET have a number of regions that are formed from common layers that are later patterned, including: a common substrate **1000**; a gate insulator film **1040** and **1040**'; a conductive gate electrode layer **1060** and **1060**'; interlayer insulation layers **1075** and **1077**; metal plugs/layers **1081**, **1083** and **1086** and **1087**. Furthermore, they also share certain isolation areas **1010**, and have source/drain regions **1070**, **1071** and **1070**', **1071**' formed at the same time with common implantation/anneal steps.

In some cases, there can be direct sharing of such regions of course, so that the drain of an NDR FET can correspond to a drain/source of an IGFET, or vice versa. Regions can be shared, of course, with two terminal NDR FETs adapted as diodes, as well. It will be understood that other processing steps and/or layers may be performed in addition to those shown above, and these examples are provided merely to illustrate the teachings of the present inventions. For example, additional interconnect and/or insulation layers are typically used in ICs and can also be shared.

Experimental Data Results

Experimental NDR FET devices with drawn gate lengths down to 125 nm were fabricated with the following basic parameters: 7 nm gate oxide thickness; 2×10^{14} cm^{-2} channel implant dose; 1100° C. post-gate-oxidation RTA anneal; 3×10^{15} cm^{-2} arsenic-doped LDD.

It should be noted right away that this prototyping process is not identical to the preferred process described earlier. For example, no thermal anneal was performed before a gate oxide was deposited. Nor was a counter-doping implant performed in the channel (e.g., of As), to lower the V_t and subthreshold swing. A single layer of gate insulating material was used. Thus, this prototyping process was intentionally designed and primarily crafted for purposes of testing/characterizing the expected behavior and performance of NDR devices, and verifying their scalability and suitability for conventional MOS circuit applications. Consequently, the results obtained are not necessarily reflective of the actual results that would be obtained for a commercial production, or for any particular actual implementation of the present invention in a particular channel geometry, within a particular fabrication facility, using a particular set of design rules, or a using a particular set of processing equipment.

Nonetheless the inventor submits that these test results are useful for illustrating a number of basic key features and advantages of the present invention. Furthermore, they serve to further validate the basic operational features of the invention, including a FET with switchable negative differential resistance.

Dependences on Gate Bias and Gate Length

The dependences of NDR FET current-vs.-voltage (I-V) characteristics on gate bias and gate length were measured. FIG. **17**A shows how the transistor current varies with gate bias. Fairly typical behavior is observed for drain biases below V_{NDR}, with the transistor current increasing ~linearly with increasing gate drive V_{gs}~V_t. For drain biases above V_{NDR}, the current decreases exponentially with increasing V_d. The valley current increases with increasing gate drive, but not as rapidly as the peak current.

FIGS. **17**B and **17**C show how the peak current and valley current respectively vary with gate bias and gate length.

In FIG. **17**B it can be seen that a peak drain current increases with increasing gate drive and also with decreasing gate length, as expected.

In FIG. **17**C it can be seen that a valley drain current also increases with increasing gate drive, which is reasonable. However, the valley drain current decreases with decreasing gate length. This is also reasonable, because energetic carriers (generated at a drain end of the channel) ate trapped at high drain biases to effect an increase in V_t. As the gate length is decreased, these carriers are trapped closer to the source end of the channel and hence they increase the transistor V_t more effectively.

As seen in FIG. **17**D, the net effect of a decrease in gate length is a significant increase in the peak-to-valley ratio. It should be noted that at high drain biases, reverse-bias pn-junction breakdown current is a significant component of the drain current because of the relatively high level of doping in the channel. Thus, to see the true valley current of the NDR transistor, the source current must be monitored. The dependence of the PVR for source current is plotted in FIG. **17**E. The PVR increases to ~100 as the gate length is scaled down to 125 nm. Consequently, as can be seen in this test data, NDR embodiments of the present invention are extremely scalable, thus ensuring their utility in future deep submicron silicon processing technologies.

Ideally, the valley current of the present NDR device should compare quite favorably with the off-state leakage current of a conventional MOSFET. In the present NDR FET device in fact, the off-current can be controlled quite effectively (and differently than a current state of the art FET) by the areal trap density N_T (number of traps per unit area)

Temperature Dependence Data

The present invention is expected from a theoretical perspective to show temperature performance superior to other NDR alternatives, because, among other things, the average kinetic energy of an electron is higher at elevated temperatures. Thus, the trapping and de-trapping rates can be expected to increase, i e. the response time of the NDR-FET should improve with increasing temperature. However, since the mean free path of an electron in the channel will decrease, it is conceivable that higher electric fields may be needed to generate electrons which are energetic enough to cause the NDR behavior. The latter can be achieved, of course, in any number of ways previously described.

Additional temperature dependence data for one embodiment of an NDR device is thus illustrated in FIG. **17**F. Again, while this device was constructed as a test vehicle, it demonstrates certain operational behaviors of various embodiments of the present invention, including the fact that an overall PVR value is substantially constant over a wide temperature range of 25° C. to 125° C. This is because, as can be seen in the figures, while a peak current increases with temperature, a valley current also increases. Accordingly, some embodiments of the present invention can be tailored to operate with relative temperature independence over a reasonably wide temperature range.

As can be seen in the graphs of FIG. **17**F both the peak current and valley current increase slightly as the temperature increases to 125° C. The annotations on this graph include lines corresponding to a drain current I_d, and symbols corresponding to a source current I_s. The solid symbols and line are for 25° C. measurement; open symbols and dashed line are for 125° C. measurement.

The peak current increases by about 20%, while the valley current increases by a factor of ~3 over the entire temperature range; this is relatively small compared to a conventional MOSFET, in which the leakage current increases exponentially with temperature. Overall, however, the NDR-FET peak-to-valley current ratio (the key performance metric for a NDR device) remains fairly constant over a wide range of temperatures.

Hence, the NDR FET of the present invention can clearly meet the operating temperature specifications for commercial IC products. In fact, it is expected that optimized embodiments of the present invention using the aforementioned preferred processes described above can achieve a PVR in excess of 10^6 across a very wide temperature range, making them particularly suitable for military, aerospace, automotive, and similar temperature demanding environments. This feature, in addition to its compatibility with a conventional CMOS process, makes the NDR-FET stands out among all known NDR devices in its promise for high density IC applications.

It should be noted that prior-art NDR devices such as the tunnel diode, resonant tunneling diode, thyristor, real-space transfer transistors, etc. show significantly degraded performance at elevated temperatures. For instance, a thyristor-based memory must operate with a relatively high (>1 nA) holding current in order to guarantee stable operation at 75° C. A so-called single transistor (DRAM-based) SRAM will have significant power consumption at elevated operating temperatures because higher refresh rates must be used to compensate for higher pass-transistor leakage.

PVR & V_{NDR} Control Through Various Process Parameters

The effects of various process parameters on PVR and V_{NDR} characteristics were also examined. This was done by examining PVR and V_{NDR} values for various experimental splits which yielded working devices. Thus, as seen in FIG. **17**G, the 7 nm gate oxide NDR test device wafer which yielded the results of FIGS. **17**A to **17**F is designated as W#A**3**, corresponding to Wafer A**3**. Additional wafer prototypes were also tested with various processing variations, including:

(1) different channel implant dosages for forming the traps (i.e., Boron at $2*10^{14}$ or $3*10^{14}$ atoms/cm^2);

(2) different lightly doped drain species (P^+ or As^+) and dosages;

(3) different post-gate-oxidation annealing conditions (RTA or furnace)

(4) different steam re-oxidation conditions

(5) different gate insulator thicknesses

PVR and V_{NDR} values are summarized in FIG. **17**G and FIG. **17**H, respectively, for NDR FETs with drawn gate length 180 nm; drain current values are noted with hashed bars, while source current values are shown with solid bars. Several key observations can be made from this test data, which is extremely useful from the perspective of effectuating precise PVR and/or V_{NDR} control for a particular embodiment of an NDR device. In particular, it can be seen that a desired target PVR/V_{NDR} value can be obtained by fine tuning one or more standard process operations during a manufacturing process. This allows for a wide variety of PVR and/or V_{NDR} values, and further ensures that predictable, reliable yields and results can be obtained for an NDR process.

In a preferred embodiment, V_{NDR} is set to be slightly lower than one-half the power-supply voltage V_{dd}, i.e. $V_{NDR}<=V_{dd}/2$. Nonetheless, different V_{NDR}s can be achieved at different areas of a semiconductor substrate through appropriate process controls as disclosed herein.

Thus, as the test data shows, as a result of the unique structure and operational features of the present invention, a desired PVR and/or V_{NDR} characteristic is easily set and controlled within a conventional MOS manufacturing facility using one or more conventional processing operations. This ease of manufacturability ensures that appropriate target values for PVR and V_{NDR} can be achieved for a wide variety of target applications. While the present disclosure provides a number of examples of process variations which can be used to control a PVR and V_{NDR} behavior, other examples will be apparent to skilled artisans from the present teachings. Thus, the present invention is by no means limited to any single variant, or combinations of variants of such PVR and/or V_{NDR} process control techniques.

PVR and V_{NDR} Control Through Channel Implant Dose Control

FIG. **17**G shows that higher PVR values are achieved with higher boron implant dose. This is expected because the density of traps is correlated with the concentration of boron incorporated into the oxide near the Si/SiO_2 interface. As noted earlier, however, the concentration of traps should not be made too high, in order to avoid trap-to-trap conduction.

FIG. **17**H shows that V_{NDR} is slightly lower for higher boron implant dose because of the higher average vertical electric field in the inversion channel. (Larger values of V_g are required to achieve 1 V gate drive, because V_t is larger.) For a larger vertical electric field, the lateral electric field (hence V_d) does not need to be as high in order to create the hot electrons which can be trapped.

Accordingly, a desired or target PVR/V_{NDR} value can also be effectuated by controlling the type of implant/dosage used in any particular manufacturing environment.

PVR and V_{NDR} Control Through Post-Gate-Oxidation Anneal

As seen in FIG. **17**G, significantly higher PVR values are achieved with an 1100° C. RTA as compared with the 1000° C. furnace anneal. This indicates that a higher density of traps at the Si/SiO_2 interface is achieved with an 1100° C. RTA. Thus a desired PVR value can also be effectuated by controlling the type of thermal annealing step performed in any particular manufacturing environment.

At this time, the experimental data (as seen in FIG. **17**H) does not show that V_{NDR} has a strong dependence on post-gate-oxidation annealing conditions.

PVR and V_{NDR} Control Through LDD Implant Dose

Significantly higher PVR values are obtained with As-doped LDD as compared with P-doped LDD as seen in FIG. **17**G. The inventor believes this is the case because As diffuses more slowly than P so that a higher LDD doping concentration is achieved with As. This in turn provides a higher peak electric field in the drain region of the channel, hence hotter electrons and more charge trapping. Apparently, in the experimental wafers, the LDD ion implantation damage was not completely annealed out for the higher dose (3×10^{15} cm^{-2}) As implant, which resulted in lower peak current and higher valley current and hence degraded PVR. Again this can be corrected using known annealing techniques.

In FIG. **17**H, it can be seen that V_{NDR} is lower for As-doped LDD as compared with P-doped LDD. This is because the drain bias required to achieve the critical peak electric field in the drain region of the channel is lower (due to the higher LDD doping concentration).

Consequently, an LDD operation provides yet another mechanism for setting or fine-tuning a desired PVR/V_{NDR} value using conventional MOS process operations.

PVR and V_{NDR} Control Through Gate-Oxide Thickness

FIG. **17**J and FIG. **17**K show similar test data for PVR and V_{NDR}, respectively, except for a slightly thinner gate oxide (5.5 nm). This data is also useful because it illustrates yet another tool available for process designers to effectuate a variable PVR value. Namely, as seen in this figure, for all other parameters being equal, an overall PVR value is lower than for comparable NDR devices having a 7 nm gate oxide.

Accordingly, higher PVR values are also achieved with thicker gate oxide. This is expected because a given density of charge traps (N_T) will effect a larger increase in V_t for a thicker gate dielectric:

$$\Delta V_t \approx q^* N_T / C_{ox}$$

As an example, for $N_T=5\times10^{12}$ $/cm^2$ and 7 nm SiO_2 gate dielectric, $V_t\approx1.6$ V, so that a "peak to valley ratio" (PVR) close to 10^6 should be attainable (assuming $V_{gs}-V_t=1$V and S is about 100 mV/dec). The effective PVR also can be enhanced (by up to 100×) by dynamically varying the gate bias to either enhance the peak current and/or to lower the valley current. This type of in-circuit PVR adjustment, during operation of an NDR device, is another benefit of the present inventions that can be used in some embodiments.

In FIG. **17**K, it can be seen that V_{NDR} is slightly lower for a thicker gate oxide because of the higher average vertical electric field in the inversion channel. (Larger values of V_g are required to achieve 1 V gate drive, because V_t is larger.) For a larger vertical electric field, the lateral electric field (hence V_d) does not need to be as high in order to create the energetic electrons which can be trapped.

For these reasons, a desired PVR/V_{NDR} value can also be effectuated by controlling the type and thickness of a gate insulator used in any particular manufacturing environment.

PVR and V_{NDR} Control Through Steam Anneal

The effect of the steam anneal cannot be clearly ascertained from the experimental results. As seen in FIG. **17**J, for a relatively thin gate oxide (5.5 nm), the PVR is consistently higher if a steam anneal was employed. As seen in FIG. **17**G, however, for thick gate oxide, however, the PVR is marginally (but consistently) lower if a steam anneal was employed.

V_{NDR} is generally lower in all cases if a steam anneal was employed.

These results suggest that, as noted earlier, a steam anneal is helpful for forming additional charge traps near the Si/SiO_2 interface. However, in some cases it also enhances boron diffusion away from the interface (and thereby lowers the trap-state density at the interface) if the gate oxide is thick.

Accordingly, it appears that for some geometries, a desired PVR/V_{NDR} value can also be effectuated by using a steam anneal process to manufacture an NDR device.

NDR FET Reliability

In the NDR FET, carriers tunnel through an ultra-thin interfacial oxide into and out of traps when $V_d>V_{NDR}$. The vast majority of these carriers will not have sufficient kinetic energy to cause new traps to be formed in the "tunnel oxide". Even if new traps were to be formed in the "tunnel oxide" (e.g. by high-energy electrons in the tail region of the electron energy distribution), they would likely serve to

enhance the speed of the NDR FET, because these new traps would be formed closer to the Si/SiO_2 interface than the original traps.

Although reliability issues for the NDR FET were not tested explicitly, the inventor believes that the existing body of knowledge on SiO_2 points to the fact that such devices should be as good or better than conventional MOSFETs. Based on the trend of increasing charge-to-breakdown Q_{BD} (to infinity as oxide thickness decreases to zero) with decreasing oxide thickness, it is reasonable to expect that the "cycle-ability" of the NDR FET will be very high (e.g. $>>10^{12}$ cycles between high-V_t and low-V_t states).

It is known that conventional hot carriers in the channel (i.e., >3.1 eV) are responsible for degradation in MOSFET performance, because of the damage which they cause to the oxide interface as well as in the bulk of the oxide. The NDR FET in fact should provide superior results, because in such device, the amount of hot carriers is limited because only energetic carriers are generated (i.e. about 0.5 eV) and the transistor turns itself off at high V_{ds}. The energetic electrons which tunnel into the traps embedded within the oxide are generally not "hot" enough to cause damage. Thus, the inventor expects the NDR FET to have reasonably good reliability in commercial applications.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. It will be clearly understood by those skilled in the art that foregoing description is merely by way of example and is not a limitation on the scope of the invention, which may be utilized in many types of integrated circuits made with conventional processing technologies. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. Such modifications and combinations, of course, may use other features that are already known in lieu of or in addition to what is disclosed herein. It is expected, given the unique characteristics of the inventive device and methods (which permit a variety of manifestations), and the rapid progress in the arts of this field, that additional embodiments utilizing different yet-to-be developed materials, structures and processes will most certainly be developed based on the present teachings.

It is therefore intended that the appended claims encompass any such modifications, improvements and future embodiments. While such claims have been formulated based on the particular embodiments described herein, it should be apparent the scope of the disclosure herein also applies to any novel and non-obvious feature (or combination thereof) disclosed explicitly or implicitly to one of skill in the art, regardless of whether such relates to the claims as provided below, and whether or not it solves and/or mitigates all of the same technical problems described above. Finally, the applicants further reserve the right to pursue new and/or additional claims directed to any such novel and non-obvious features during the prosecution of the present application (and/or any related applications).

What is claimed is:

1. In a charge-trap based negative differential resistance (NDR) element which operates with an NDR characteristic having a peak current and a valley current, the improvement comprising:

distributing charge traps in a trapping region of the NDR element with a concentration and energy adapted so as to impart a peak-to-valley current ratio (PVR) for the NDR element which exceeds ten (10) over a temperature range greater than 0° C. and spanning at least 50° C.

2. The NDR element of claim **1**, wherein said PVR varies by less than a factor of five in an operating temperature spanning 25° and 125°.

3. The NDR element of claim **1**, wherein said PVR exceeds 1000 in an operating temperature range spanning from 25° to 125°.

4. The NDR element of claim **1**, wherein said trapping region forms an interface with a channel of a field effect transistor associated with the NDR element.

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