US006945110B2

(12) **United States Patent**
Selvakumar et al.

(10) **Patent No.: US 6,945,110 B2**
(45) **Date of Patent: Sep. 20, 2005**

(54) **SENSOR DESIGN AND PROCESS**

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(73) Assignee: **Input/Output, Inc.**, Stafford, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 79 days.

(21) Appl. No.: **10/896,602**

(22) Filed: **Jul. 21, 2004**

(65) **Prior Publication Data**

US 2005/0000082 A1 Jan. 6, 2005

Related U.S. Application Data

(62) Division of application No. 09/936,640, filed as application No. PCT/US00/40039 on Mar. 16, 2000.

(60) Provisional application No. 60/125,076, filed on Mar. 17, 1999.

(51) **Int. Cl.**[7] **G01P 15/00**; H01L 21/76

(52) **U.S. Cl.** **73/514.16**; 73/514.24; 438/15

(58) **Field of Search** 73/514.16, 514.15, 73/514.23, 514.24; 438/14, 15

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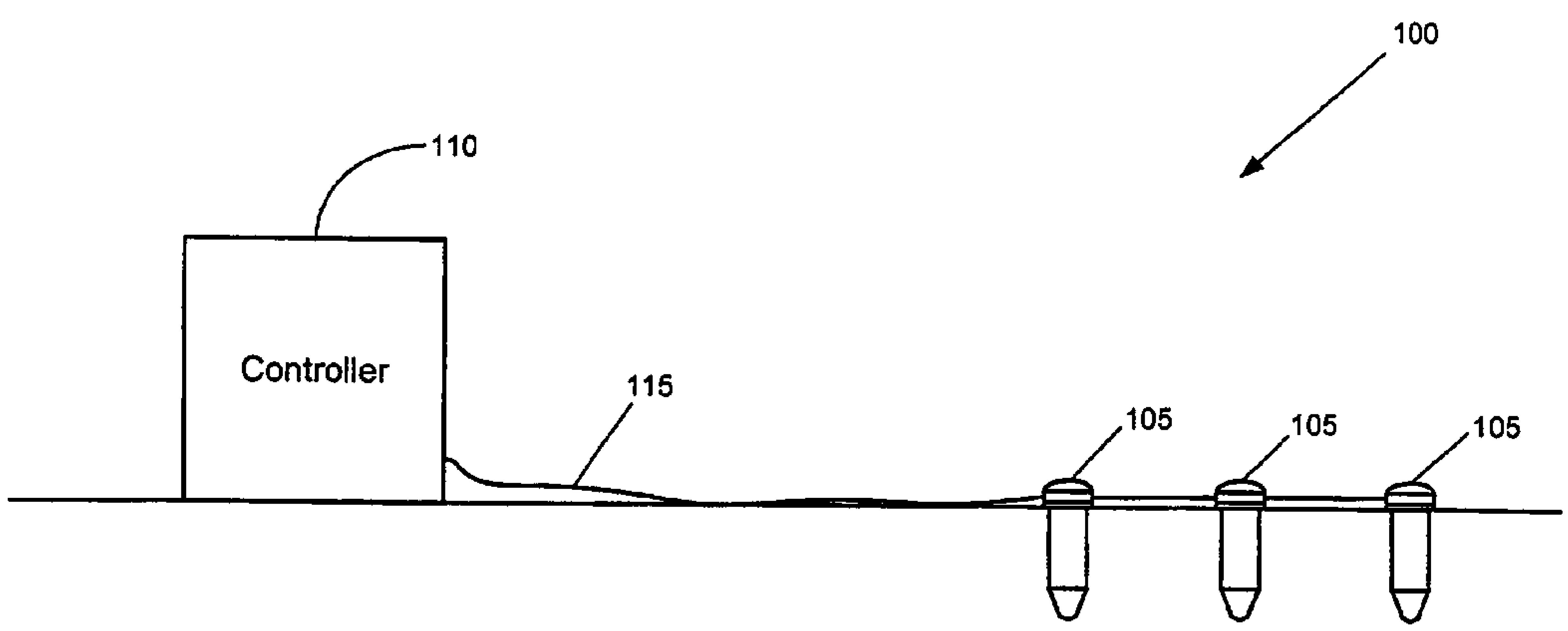
Assistant Examiner—Jacques M. Saint-Surin
(74) *Attorney, Agent, or Firm*—Madan, Mossman & Sriram, P.C.

(57) **ABSTRACT**

An accelerometer (**305**) for measuring seismic data. The accelerometer (**305**) includes an integrated vent hole for use during a vacuum sealing process and a balanced metal pattern for reducing cap wafer bowing. The accelerometer (**305**) also includes a top cap press frame recess (**405**) and a bottom cap press frame recess (**420**) for isolating bonding pressures to specified regions of the accelerometer (**305**). The accelerometer (**305**) is vacuum-sealed and includes a balanced metal pattern (**730**) to prevent degradation of the performance of the accelerometer (**305**). A dicing process is performed on the accelerometer (**305**) to isolate the electrical leads of the accelerometer (**305**). The accelerometer (**305**) further includes overshock protection bumpers (**720**) and patterned metal electrodes to reduce stiction during the operation of the accelerometer (**305**).

18 Claims, 41 Drawing Sheets



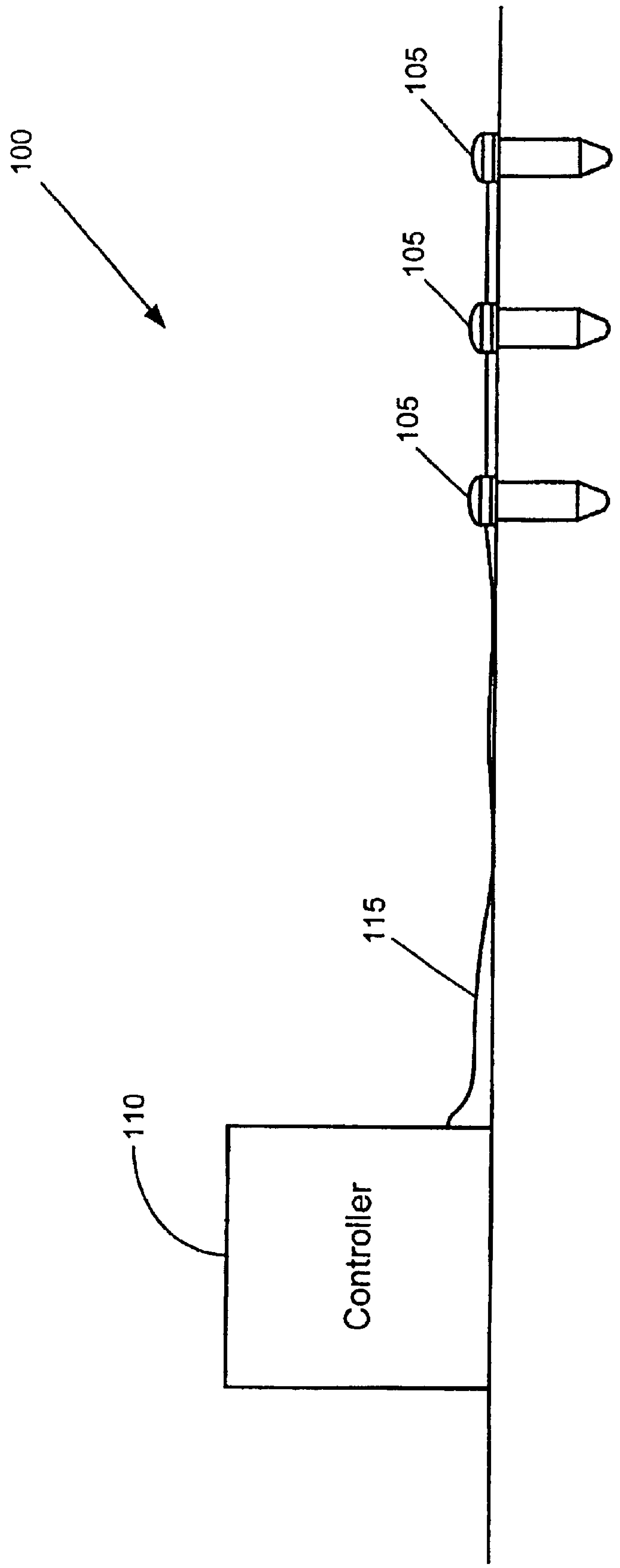


FIGURE 1

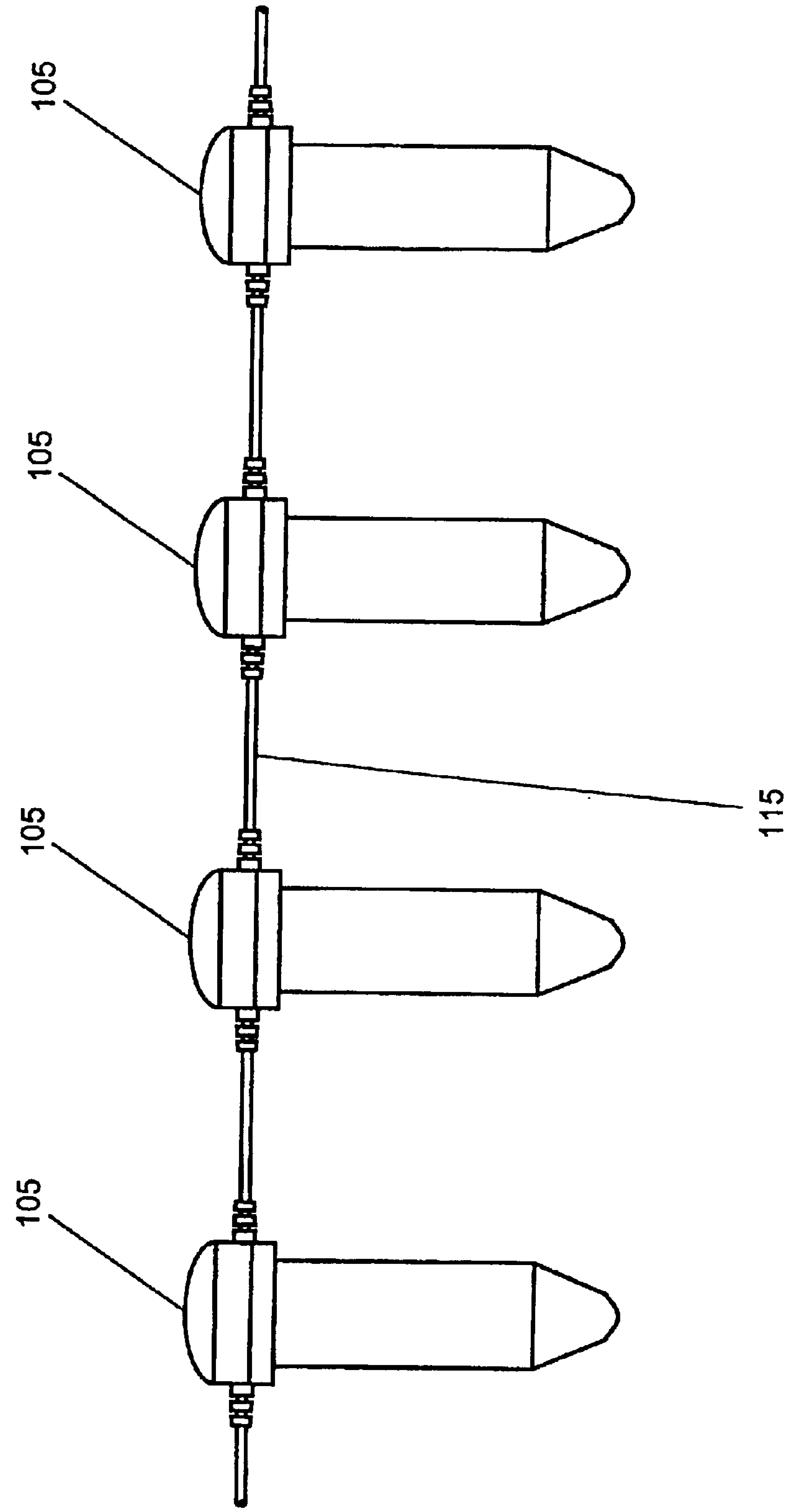


FIGURE 2

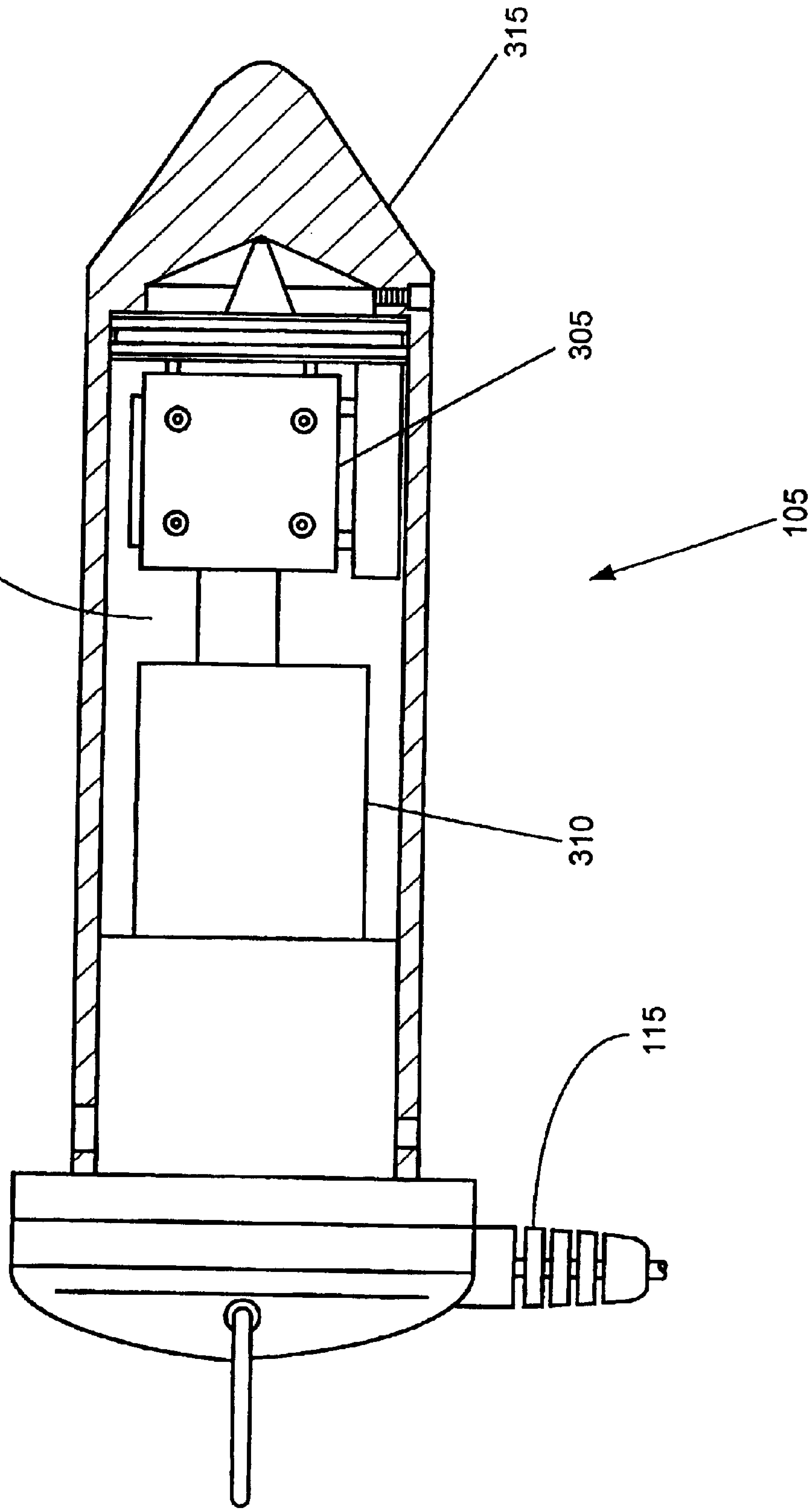


FIGURE 3a

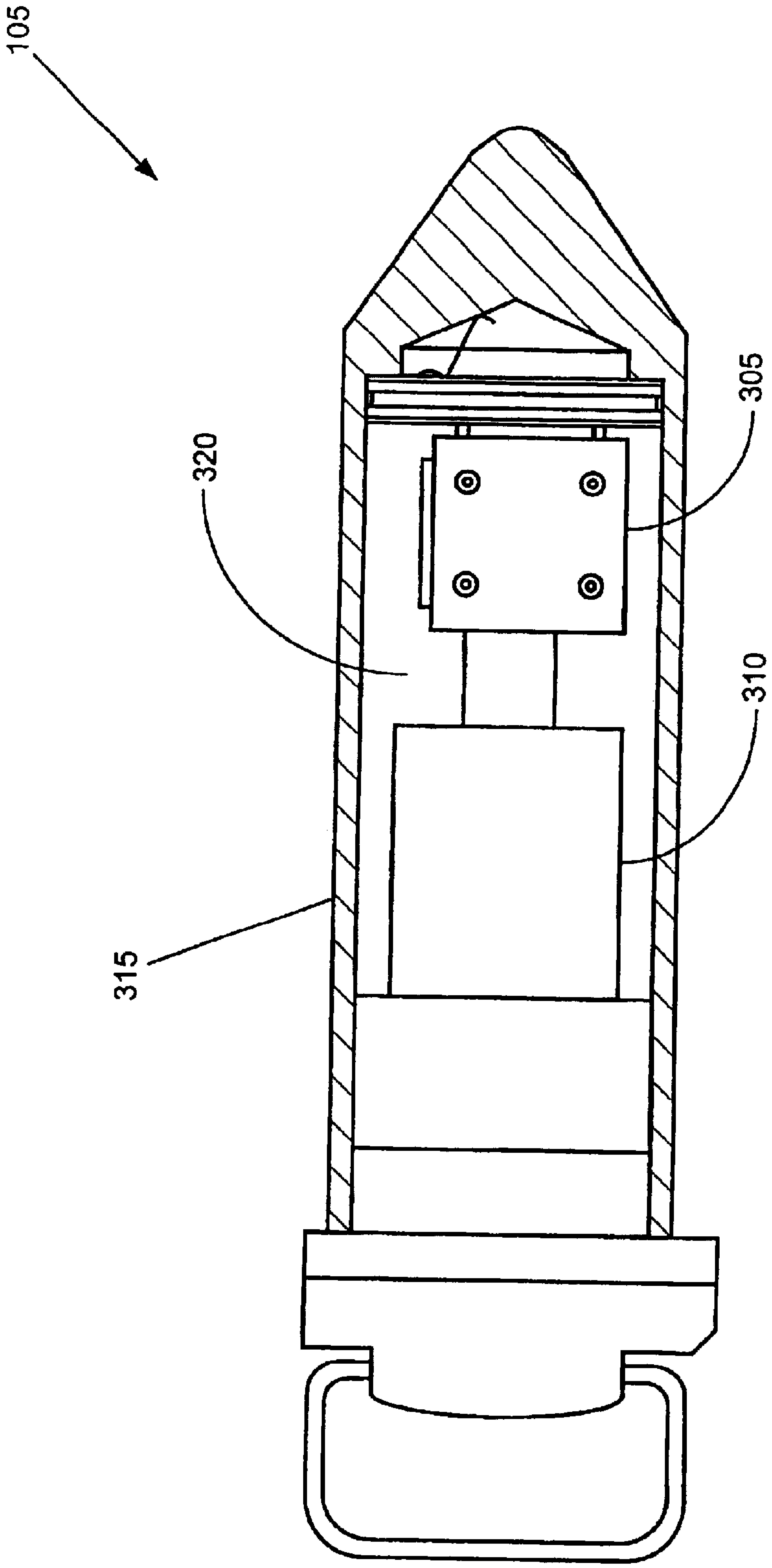
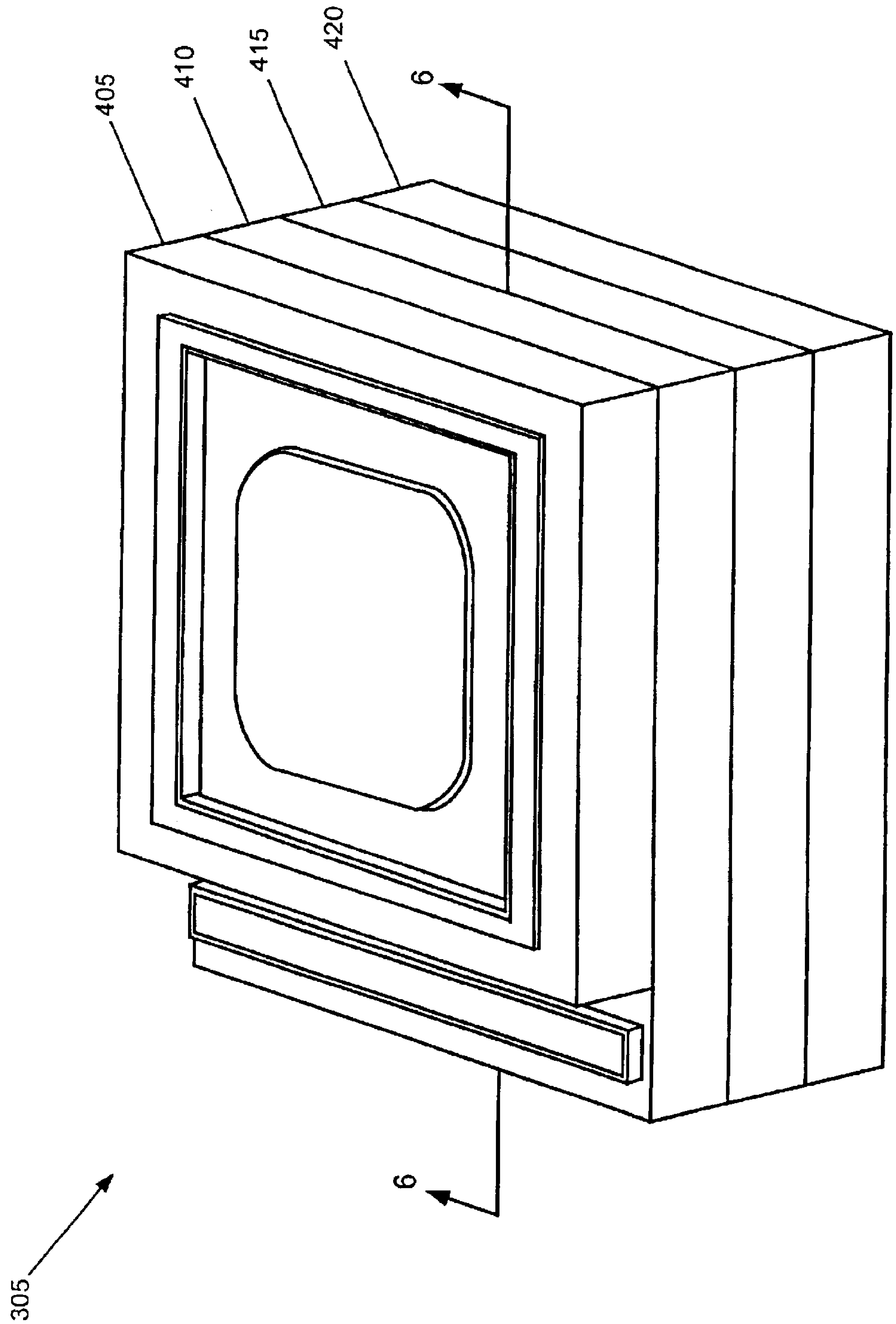


FIGURE 3b



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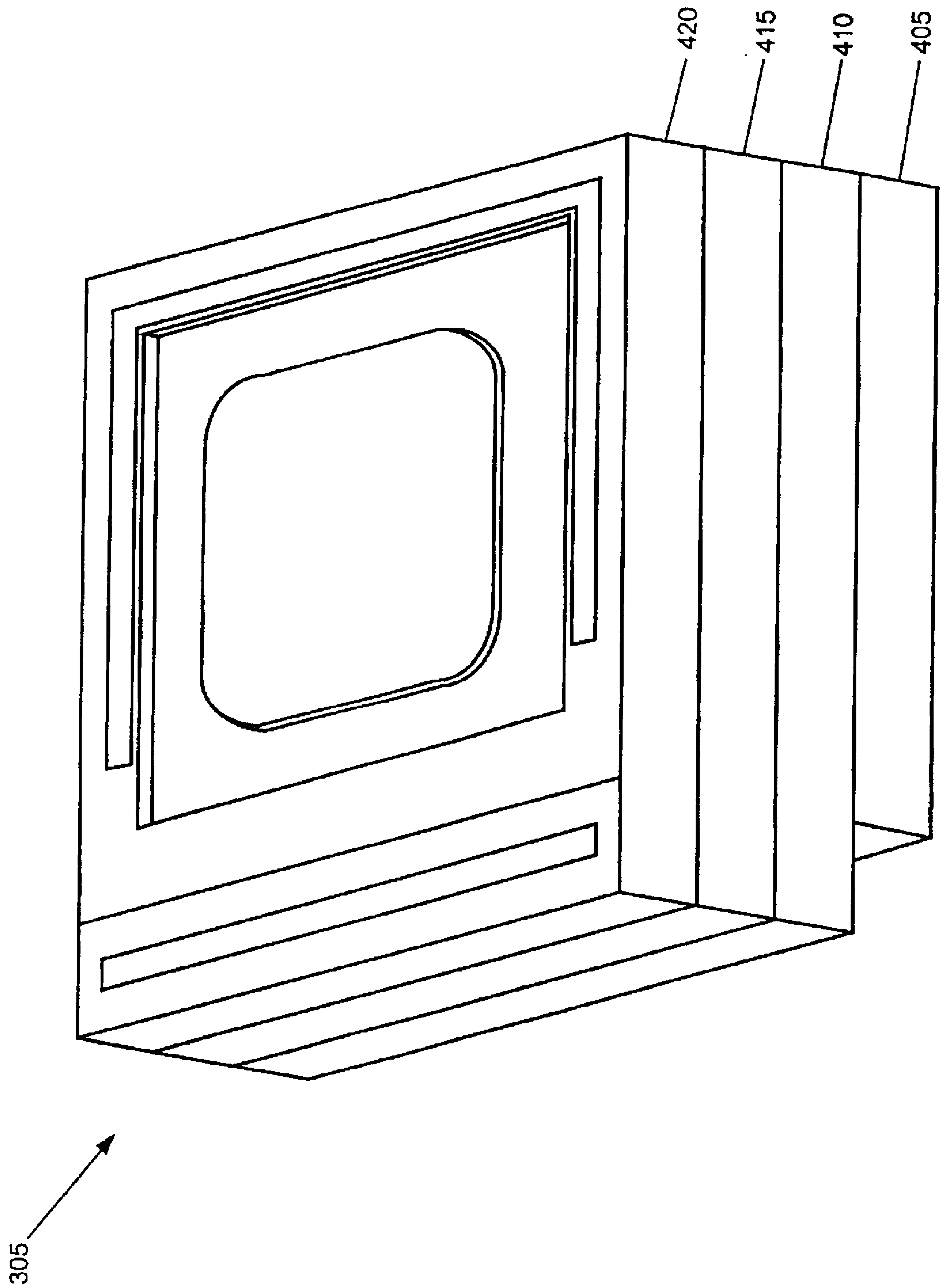
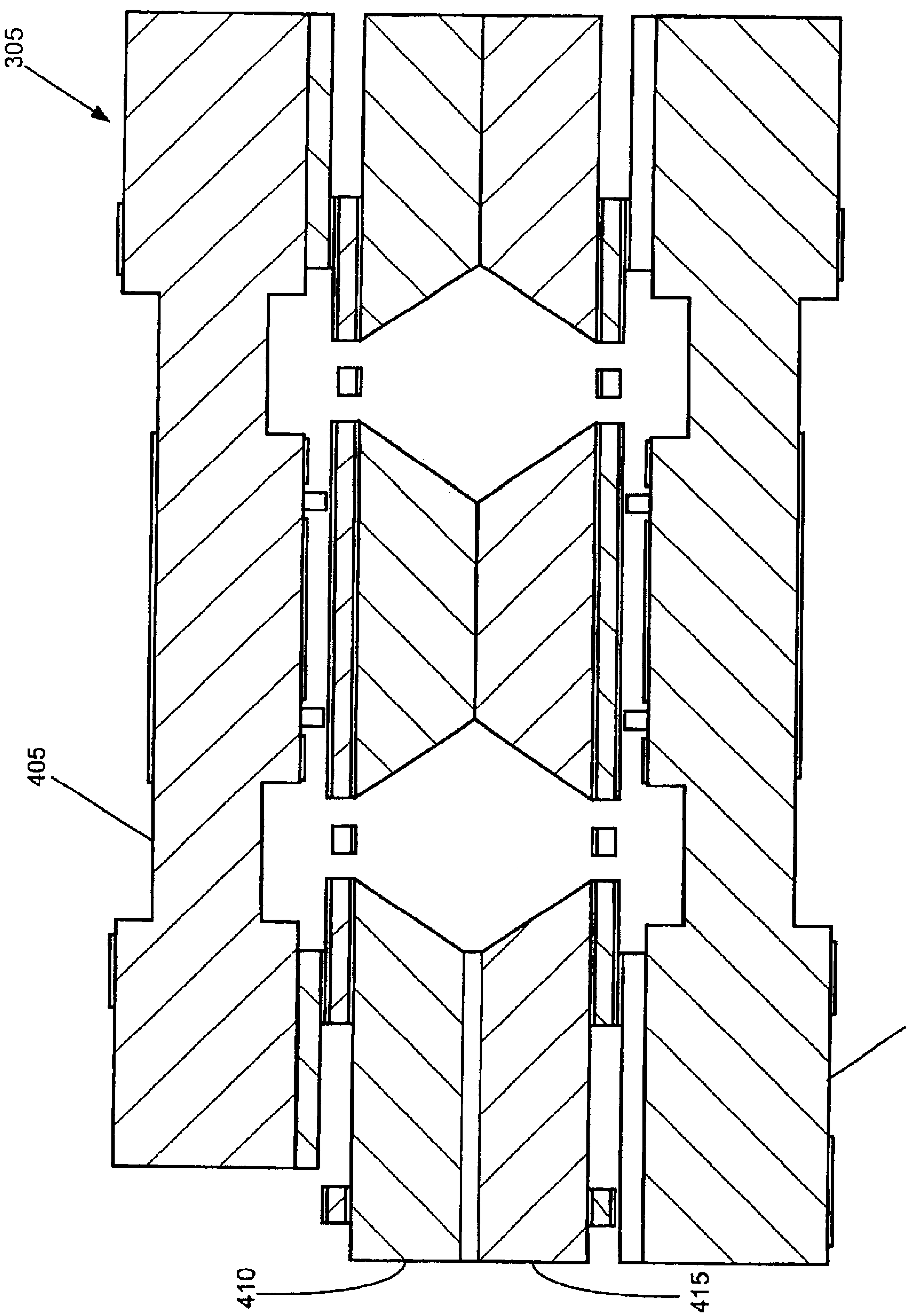


FIGURE 5



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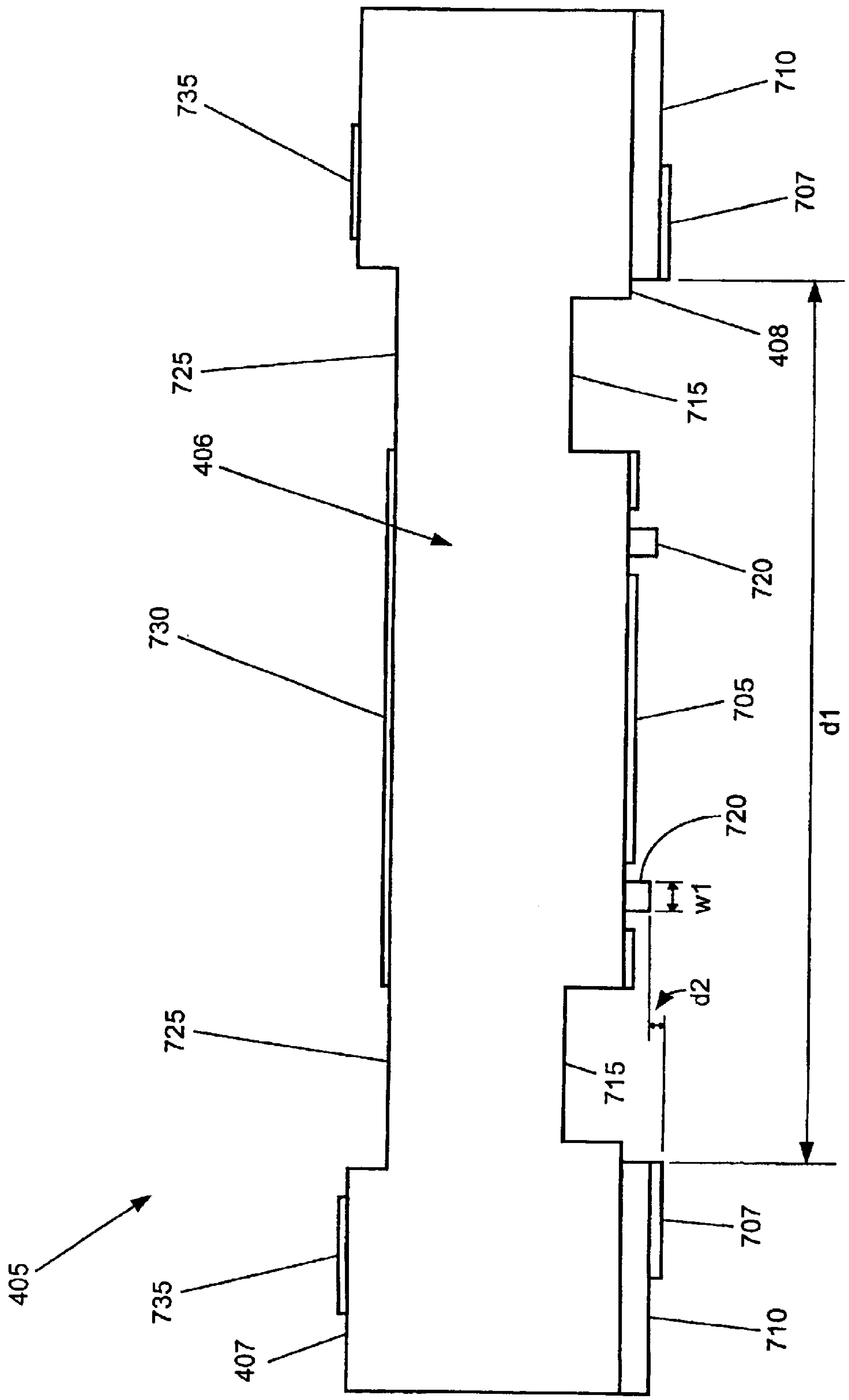
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FIGURE 7a

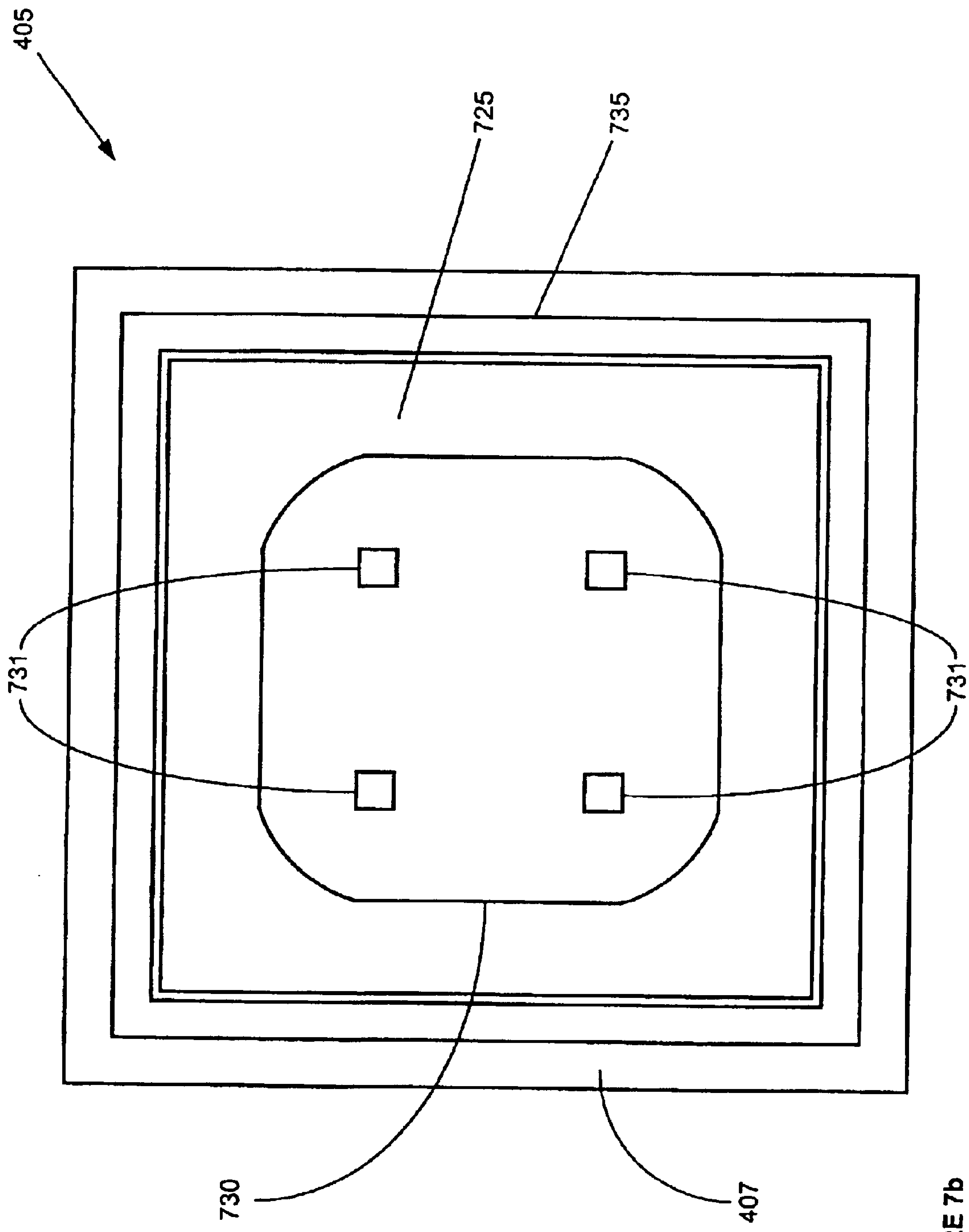

FIGURE 7b

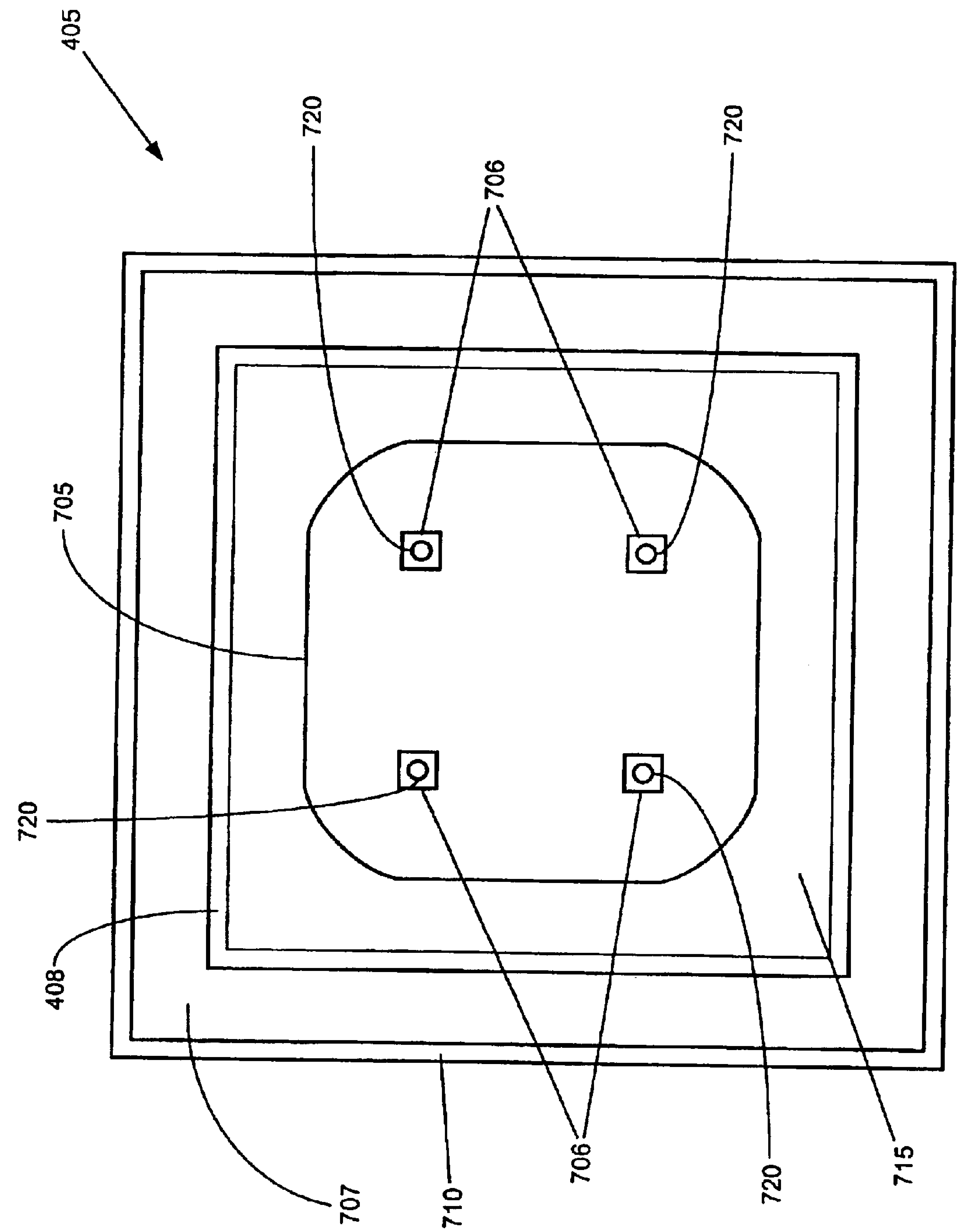

FIGURE 7c

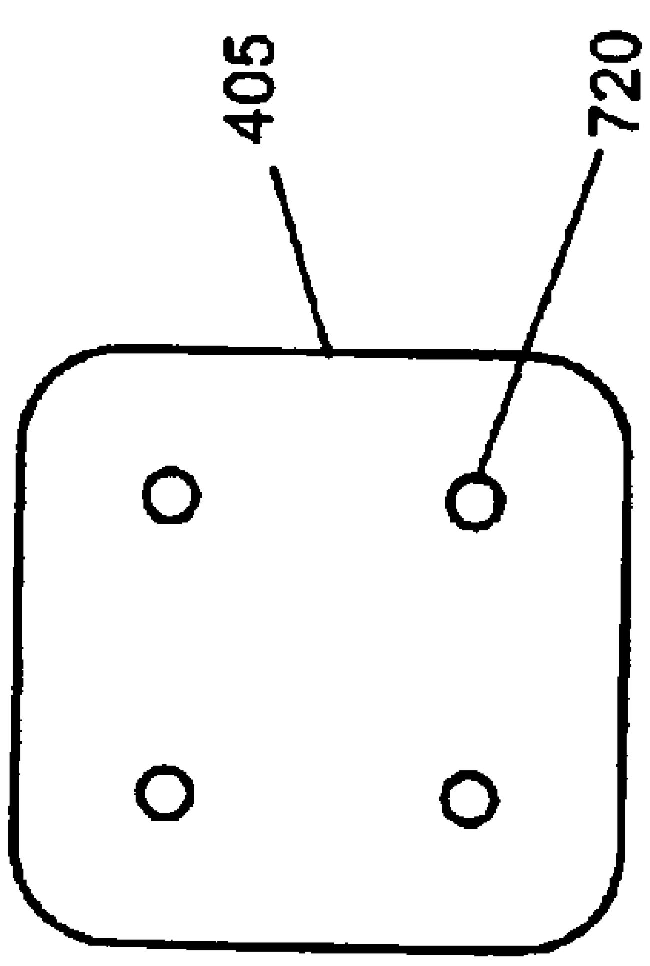

FIGURE 7d

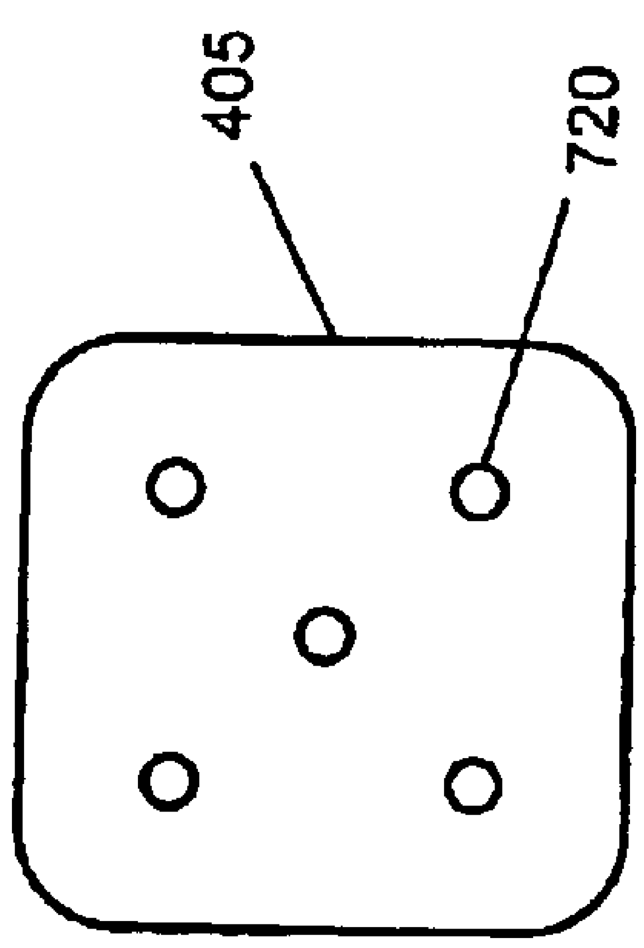

FIGURE 7e

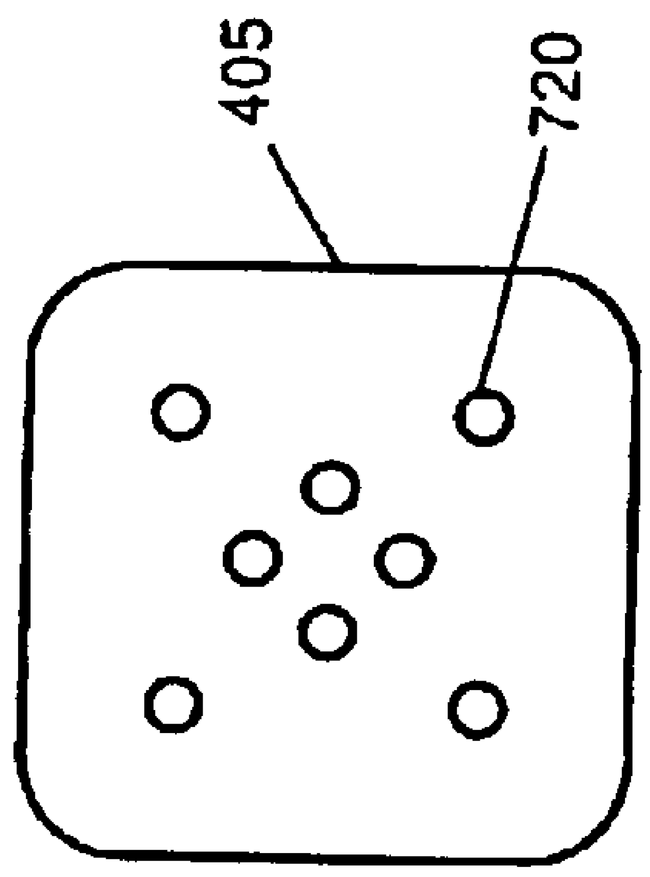

FIGURE 7f

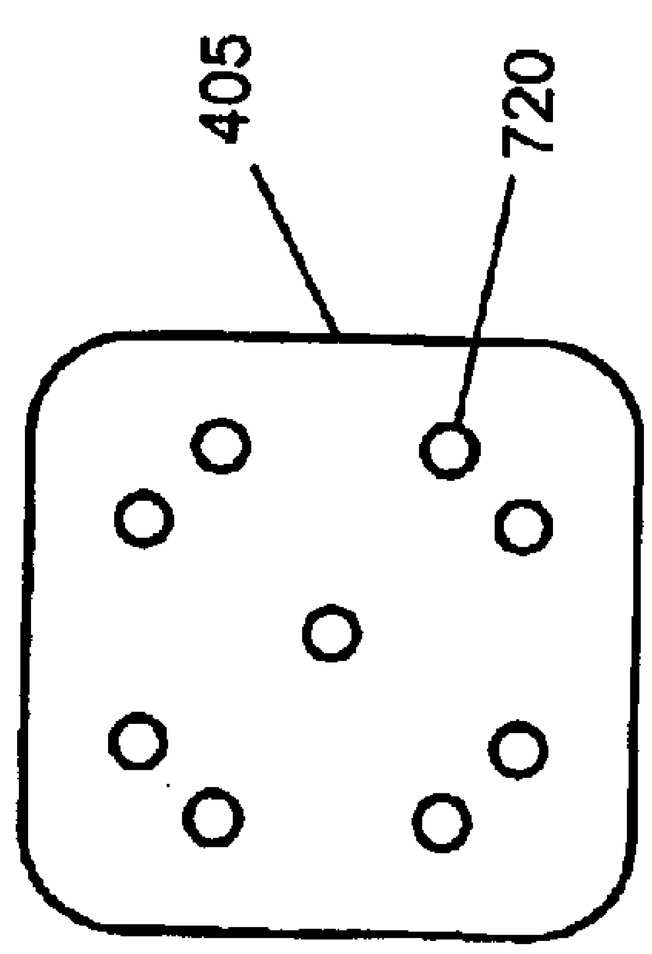

FIGURE 7g

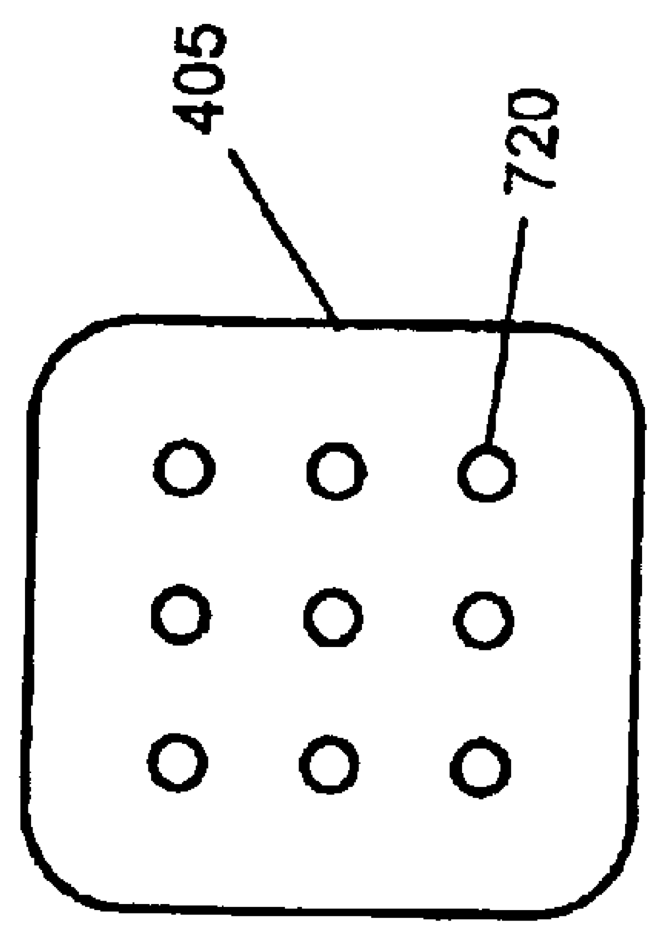

FIGURE 7h

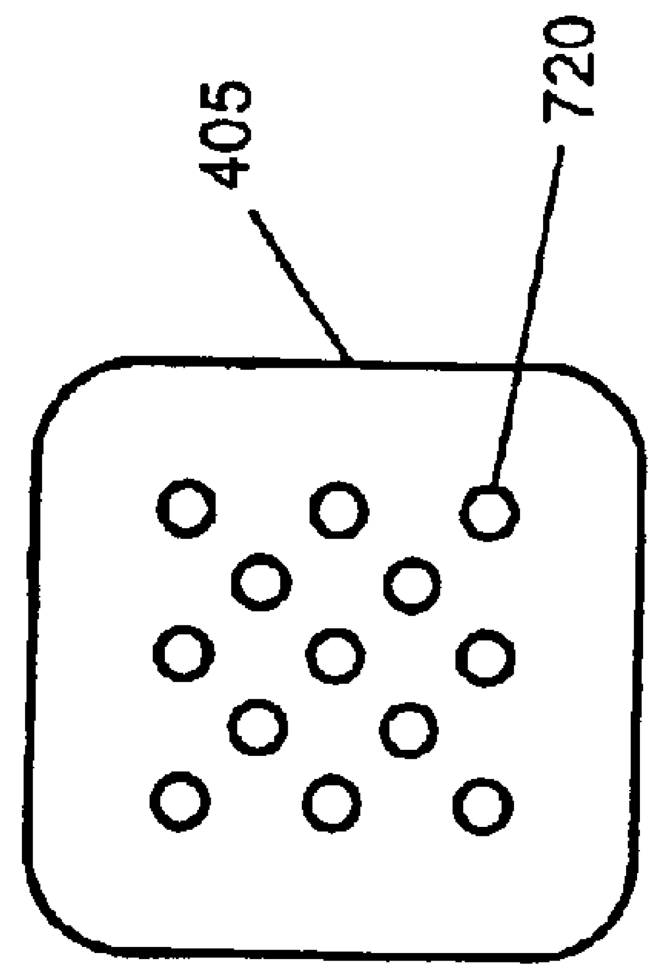

FIGURE 7i

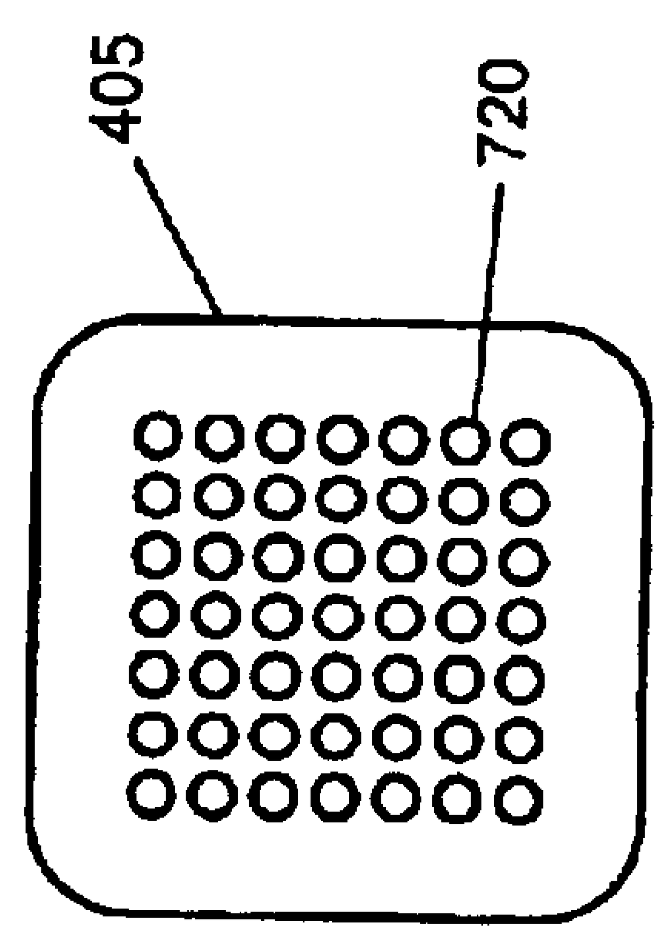

FIGURE 7j

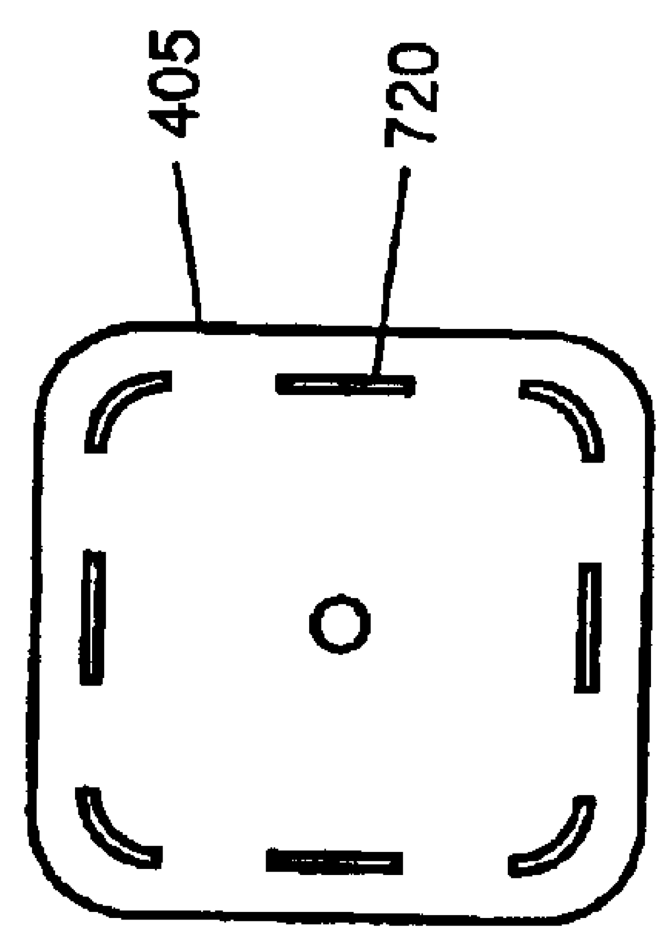

FIGURE 7k

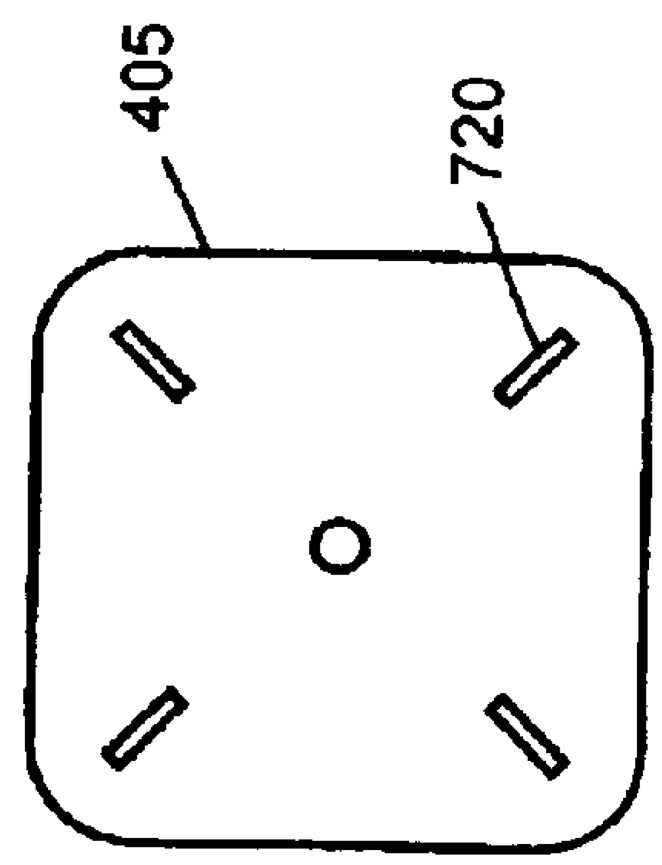

FIGURE 7l

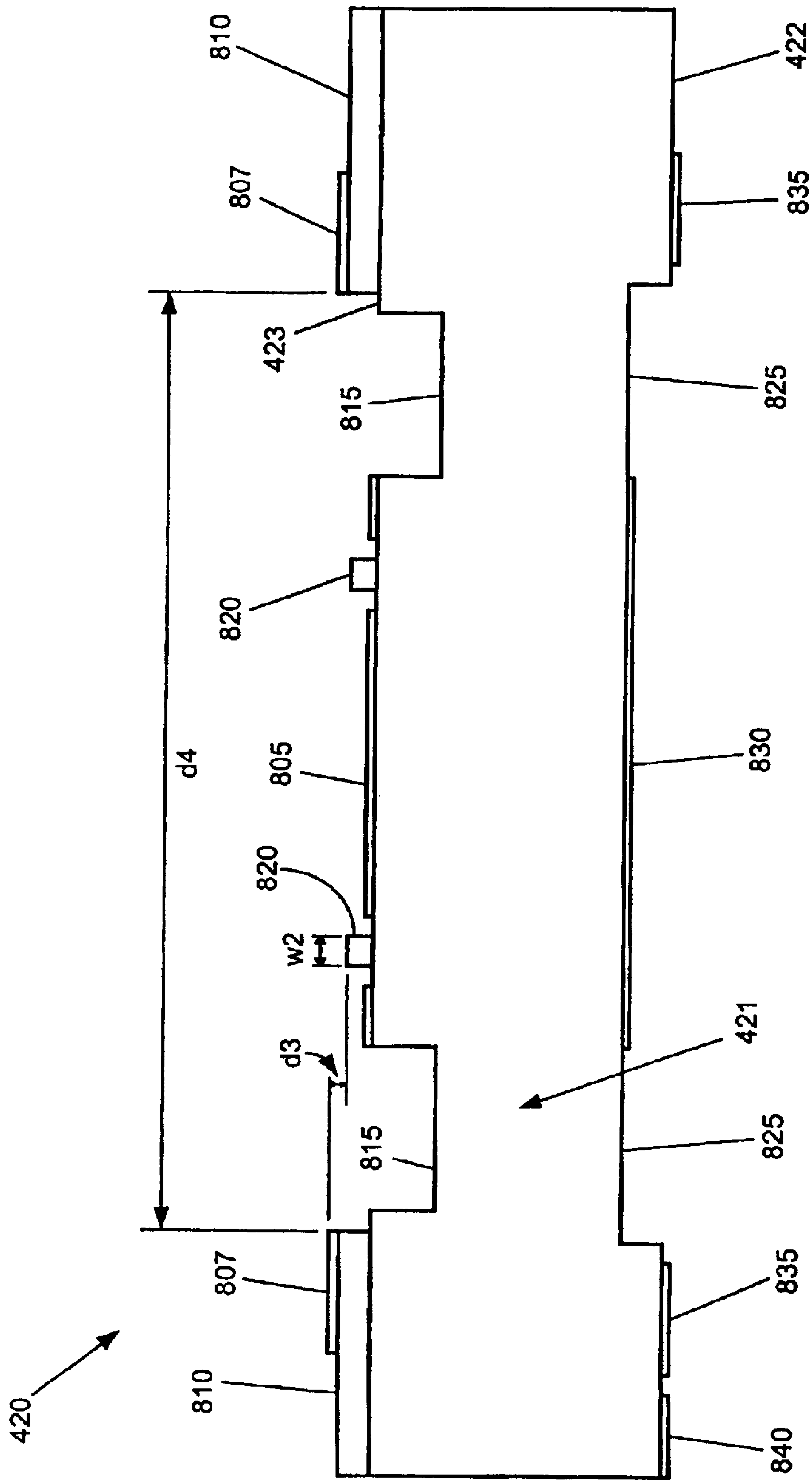

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FIGURE 8a

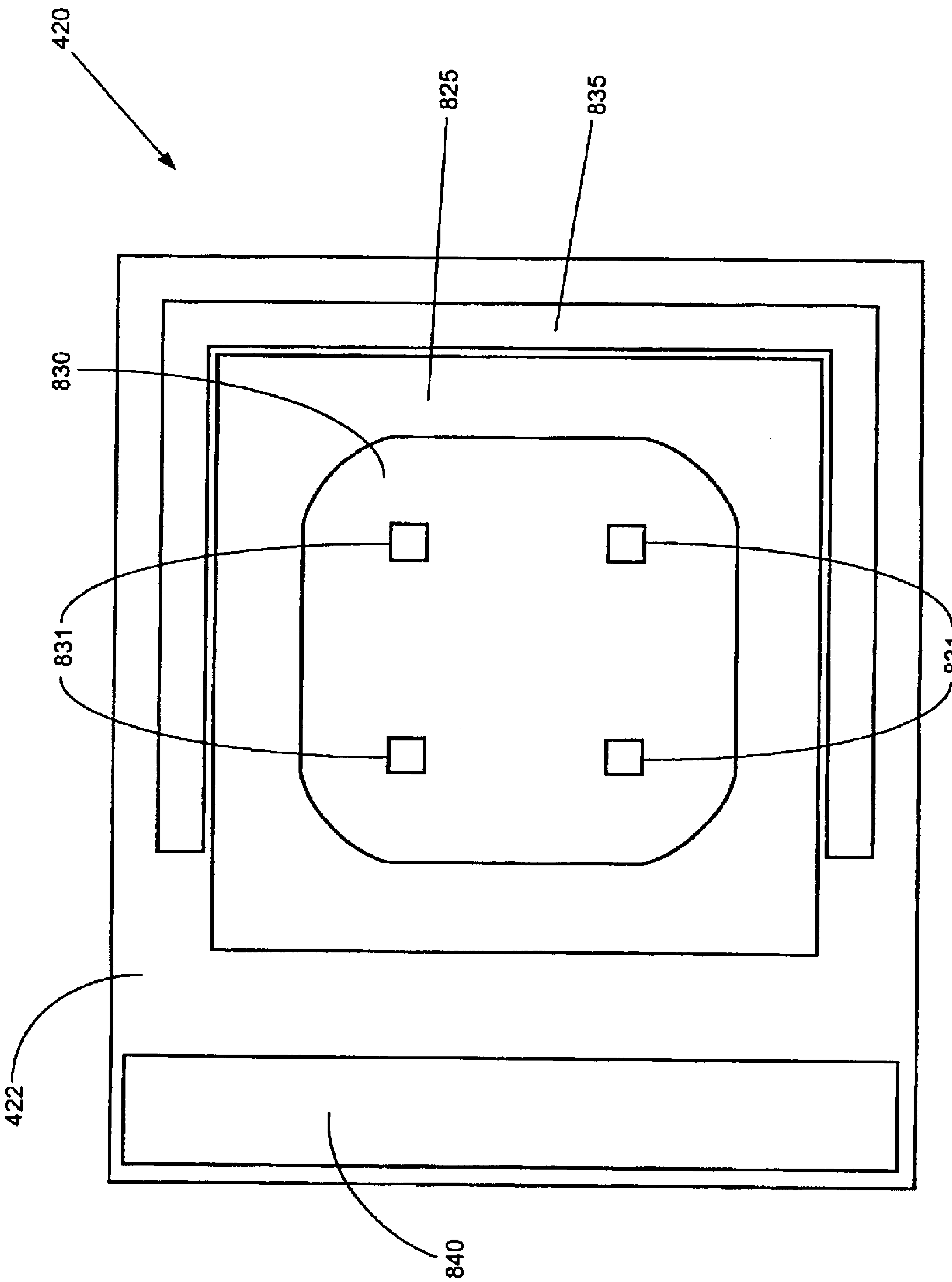

FIGURE 8b

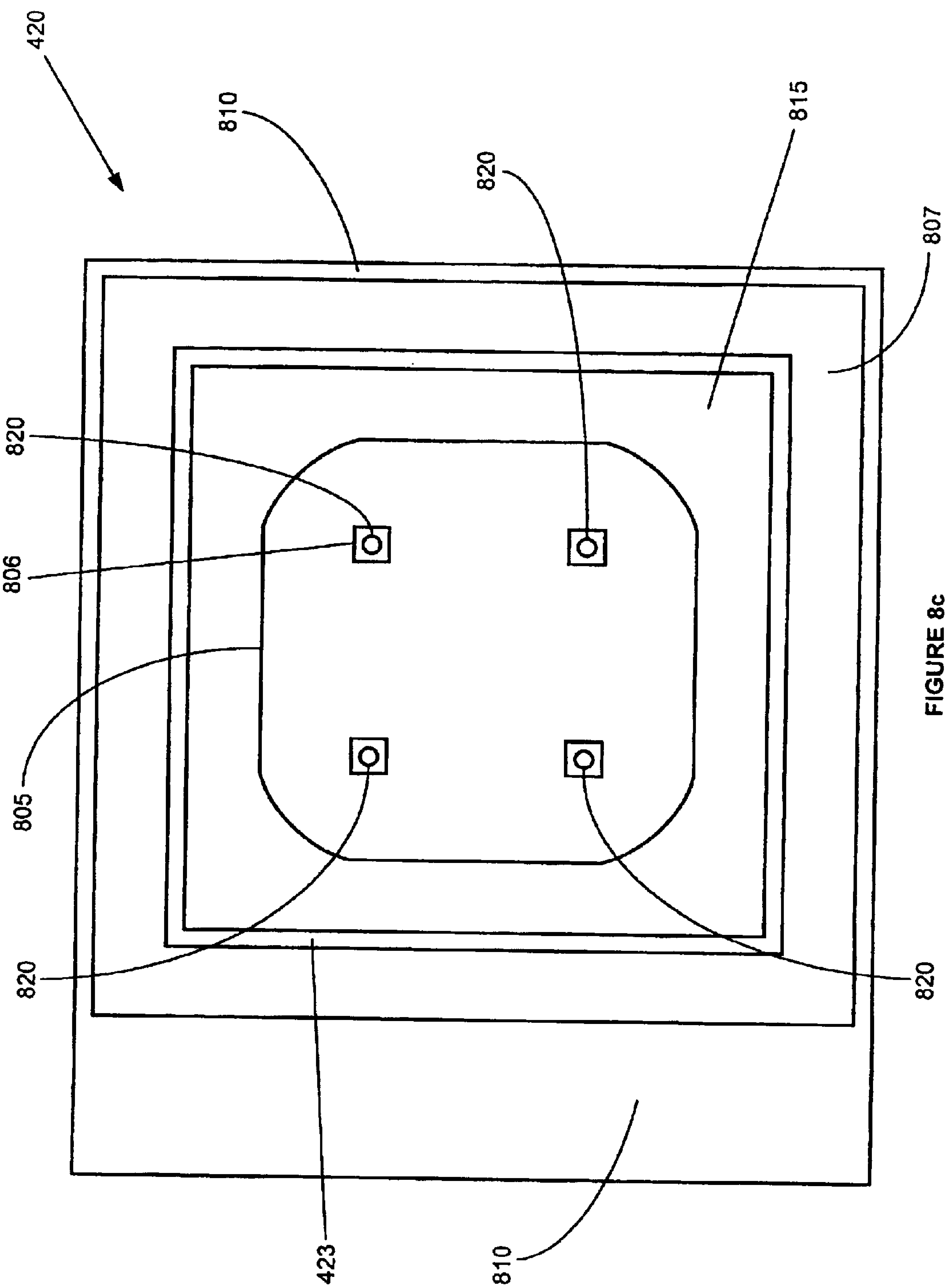

FIGURE 8c

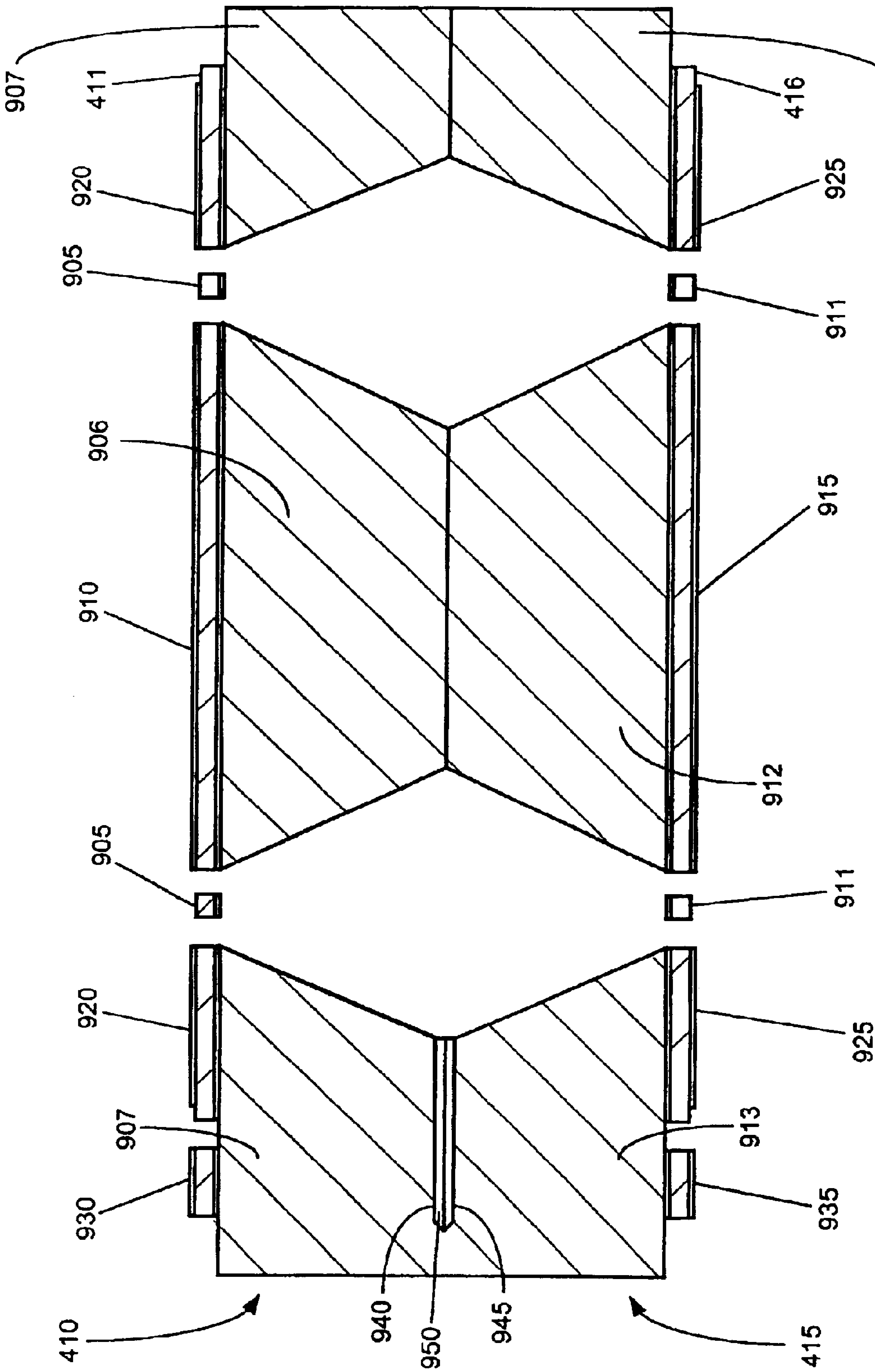
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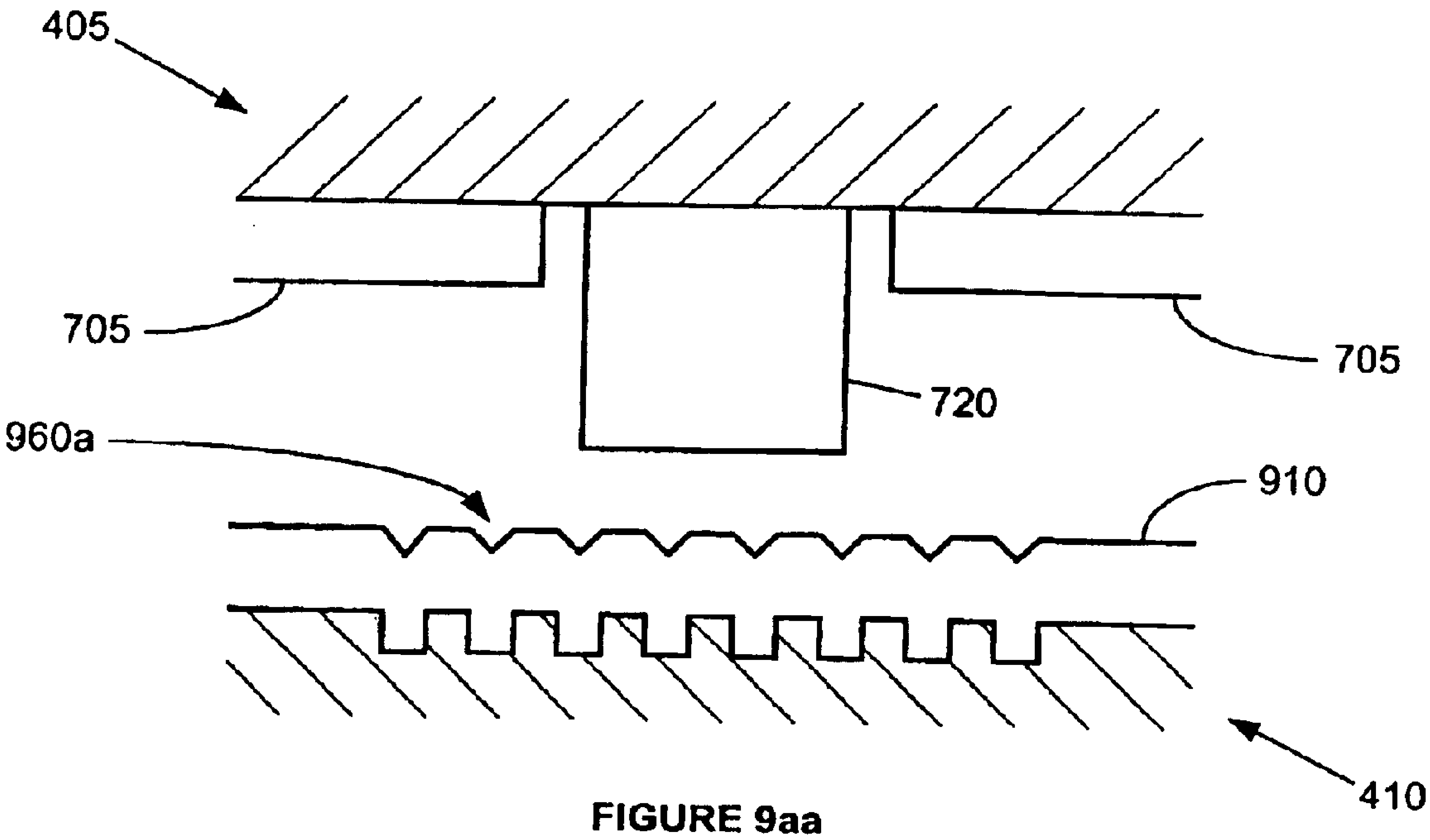
FIGURE 9a



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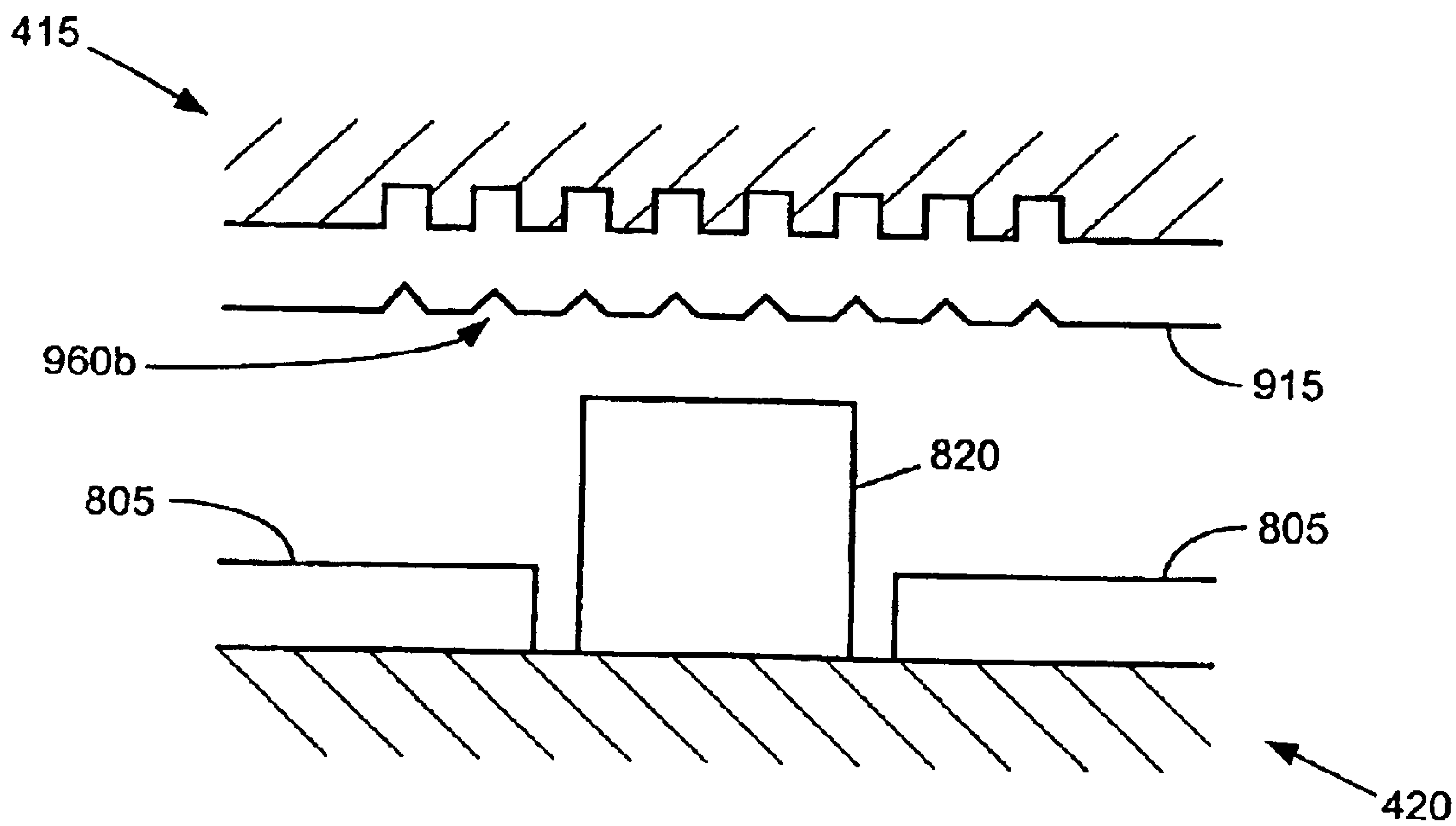

FIGURE 9ab

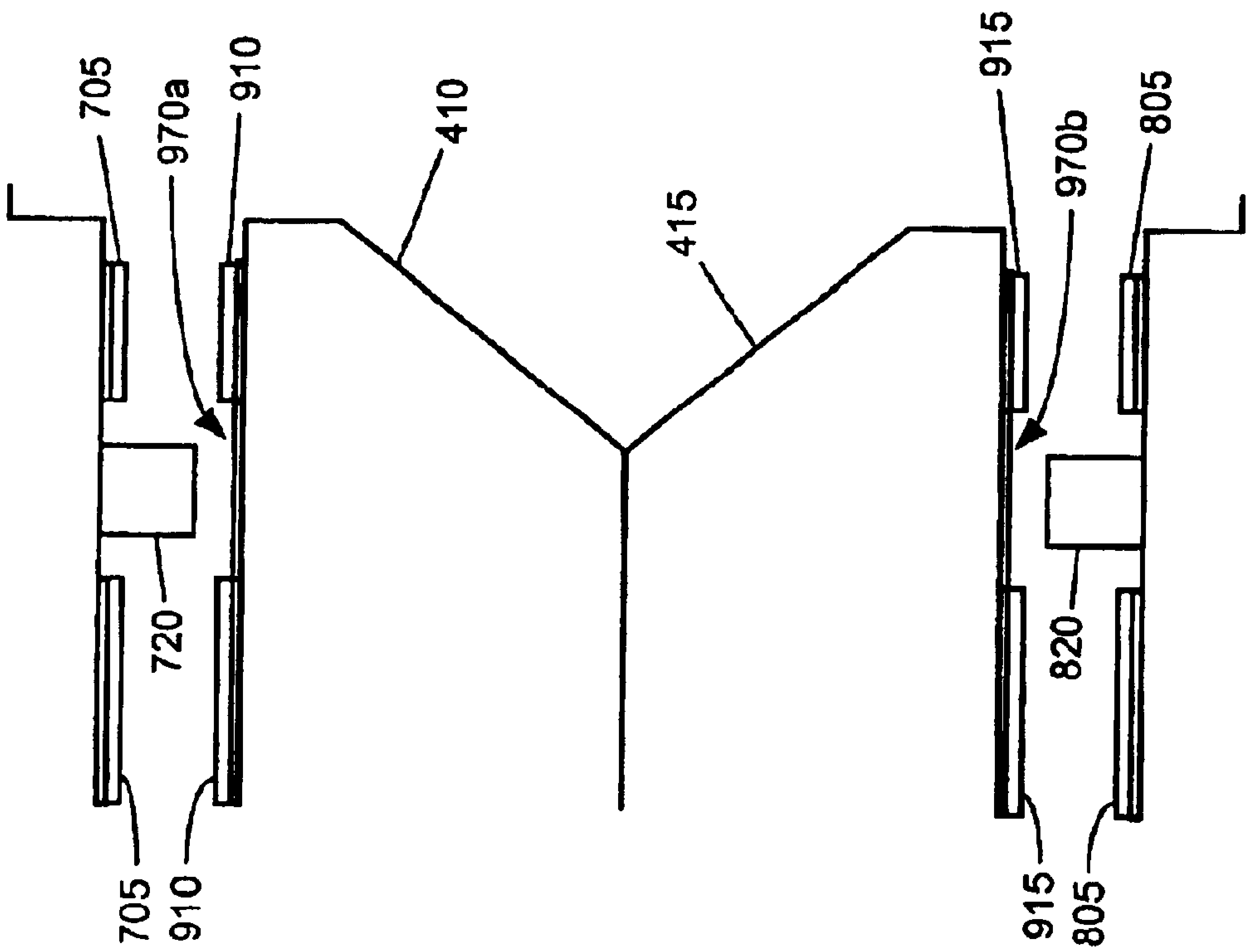

FIGURE 9ac

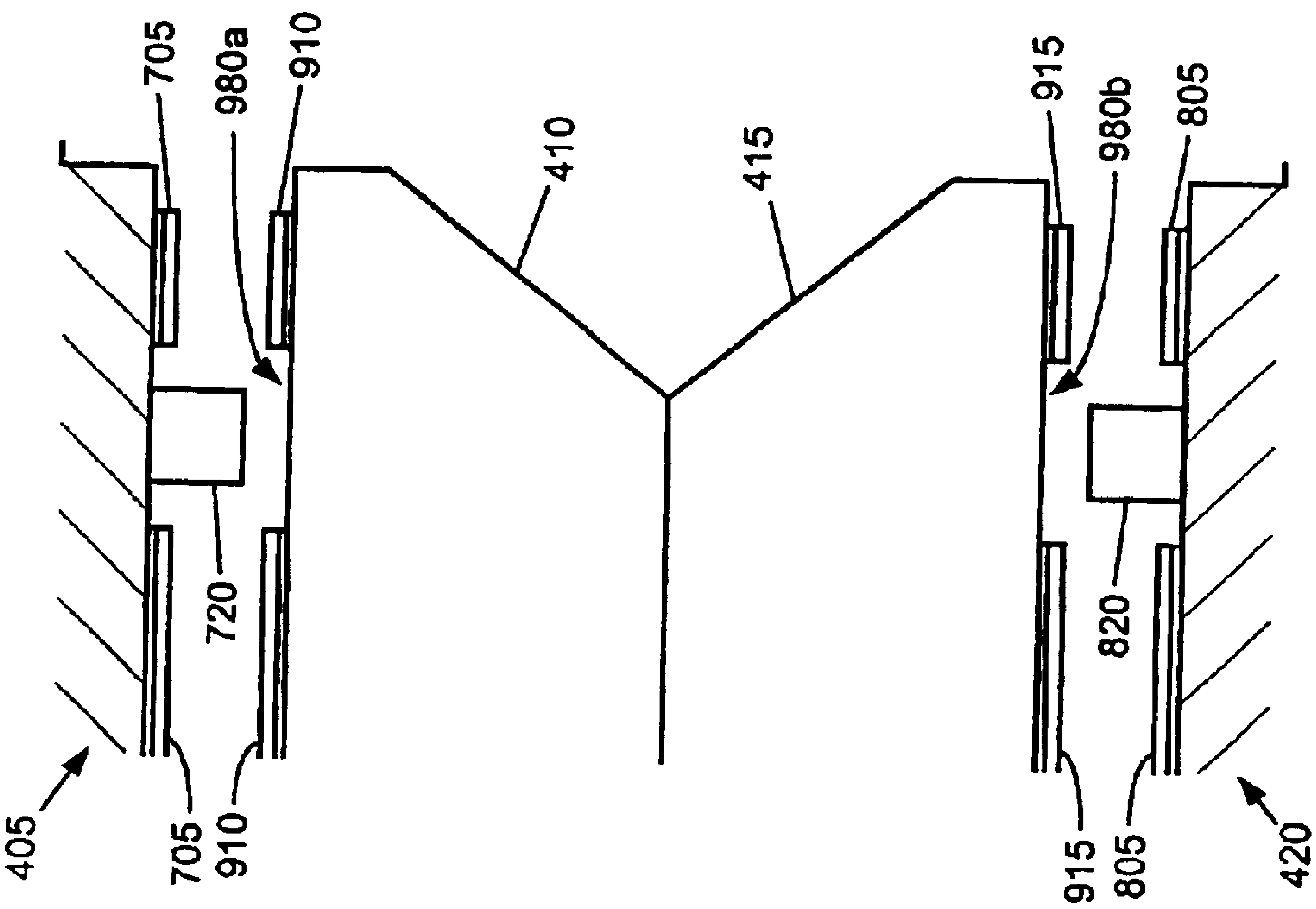
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FIGURE 9ad

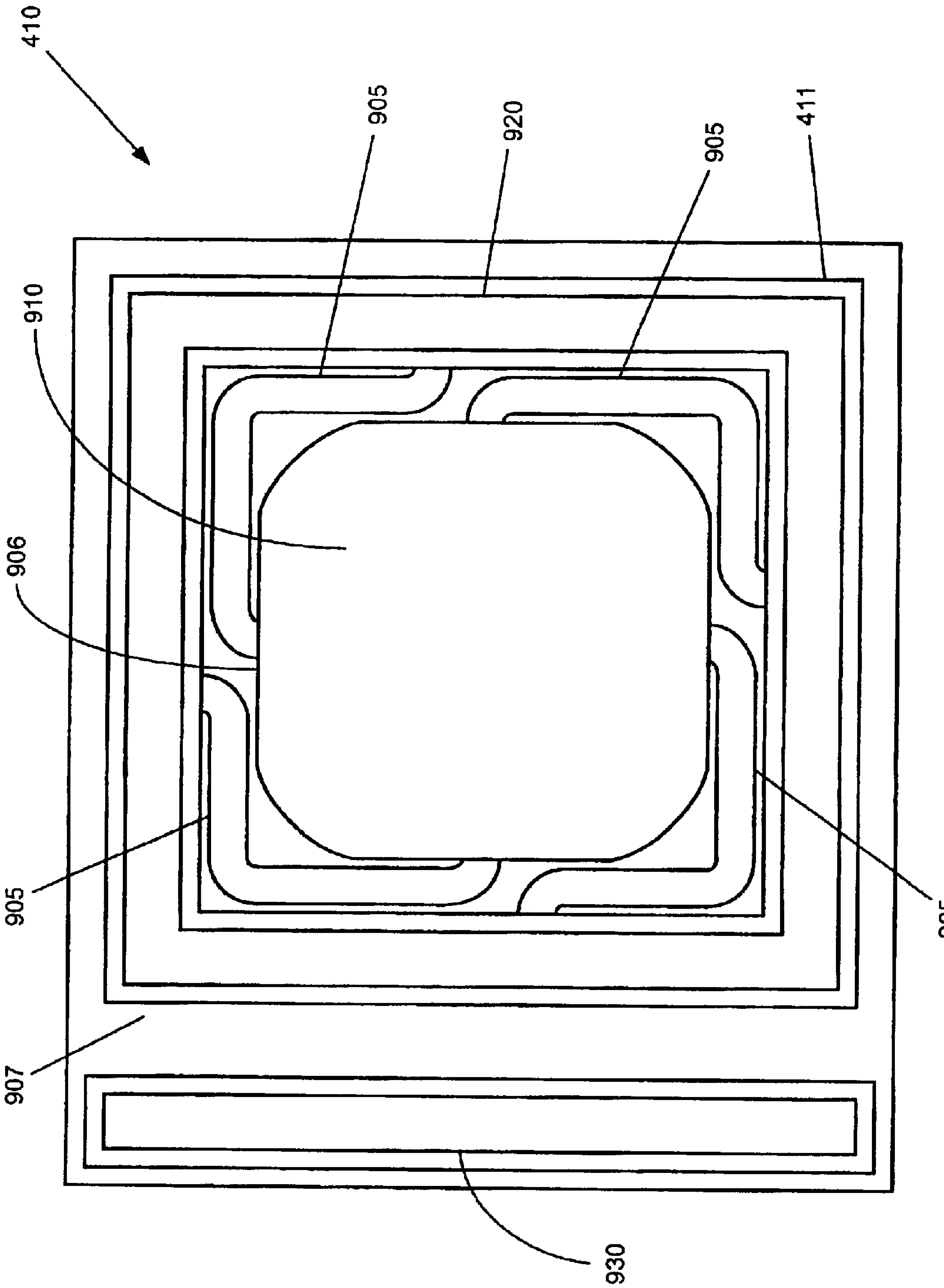
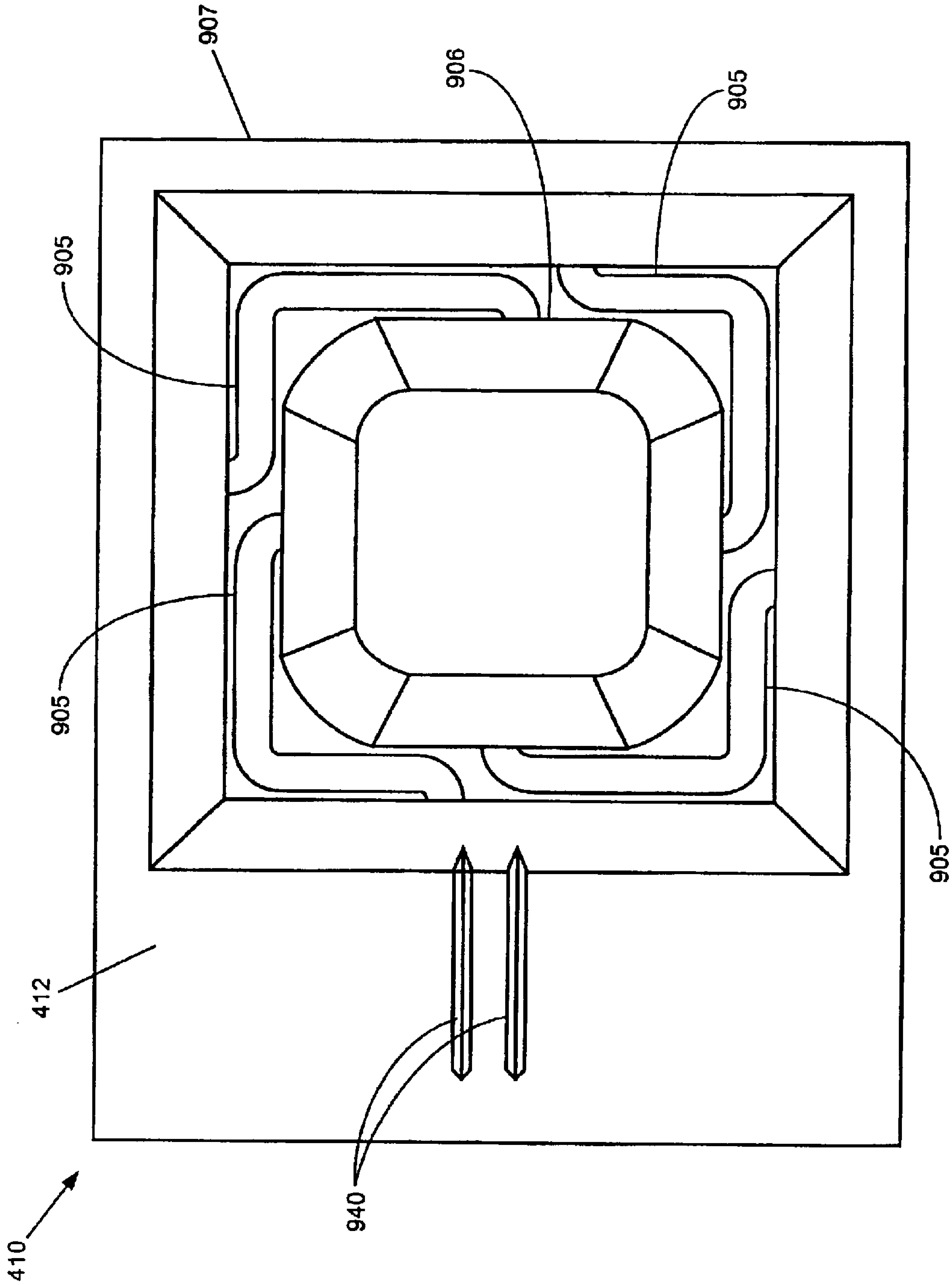


FIGURE 9b



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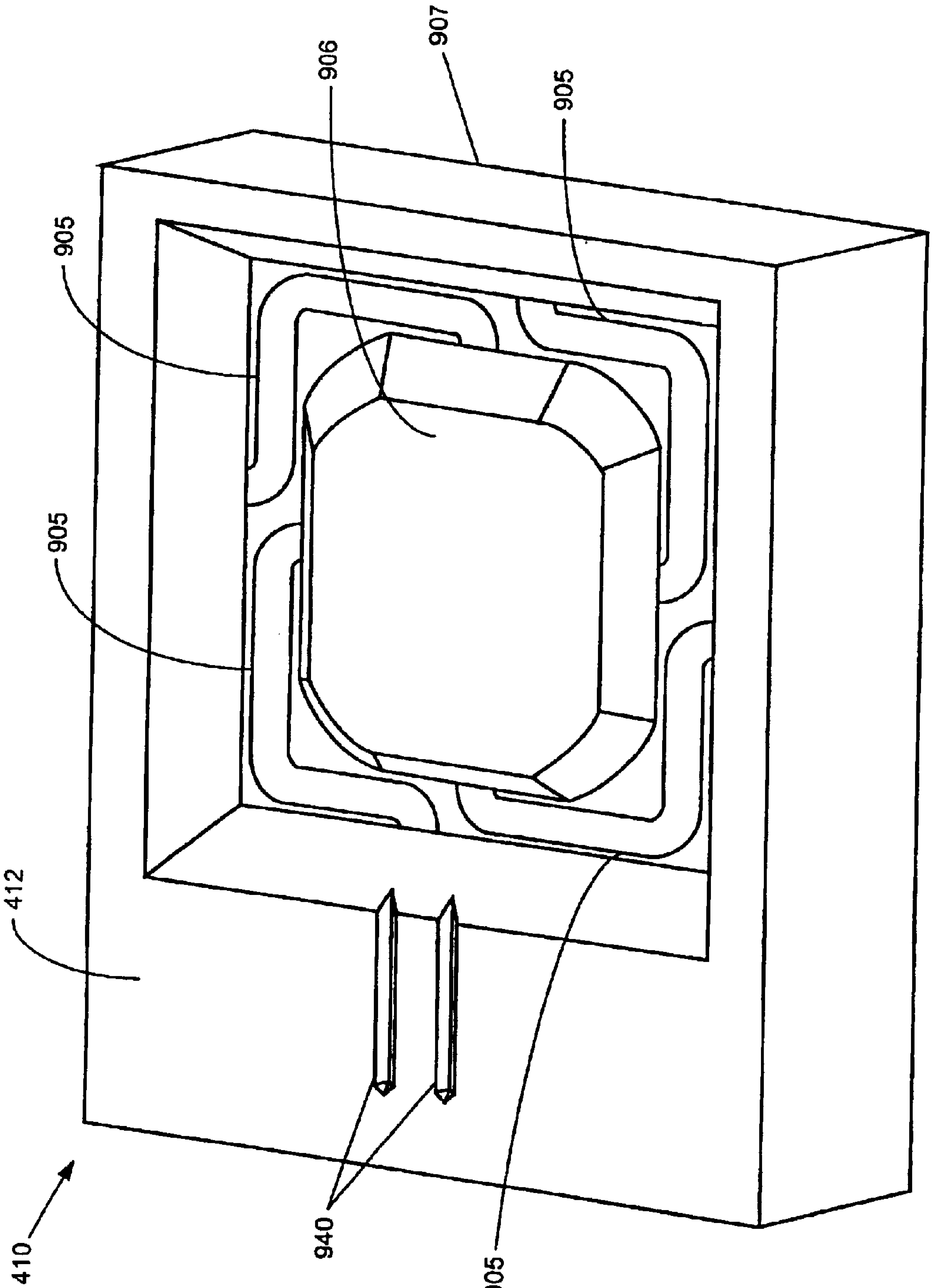


FIGURE 9d

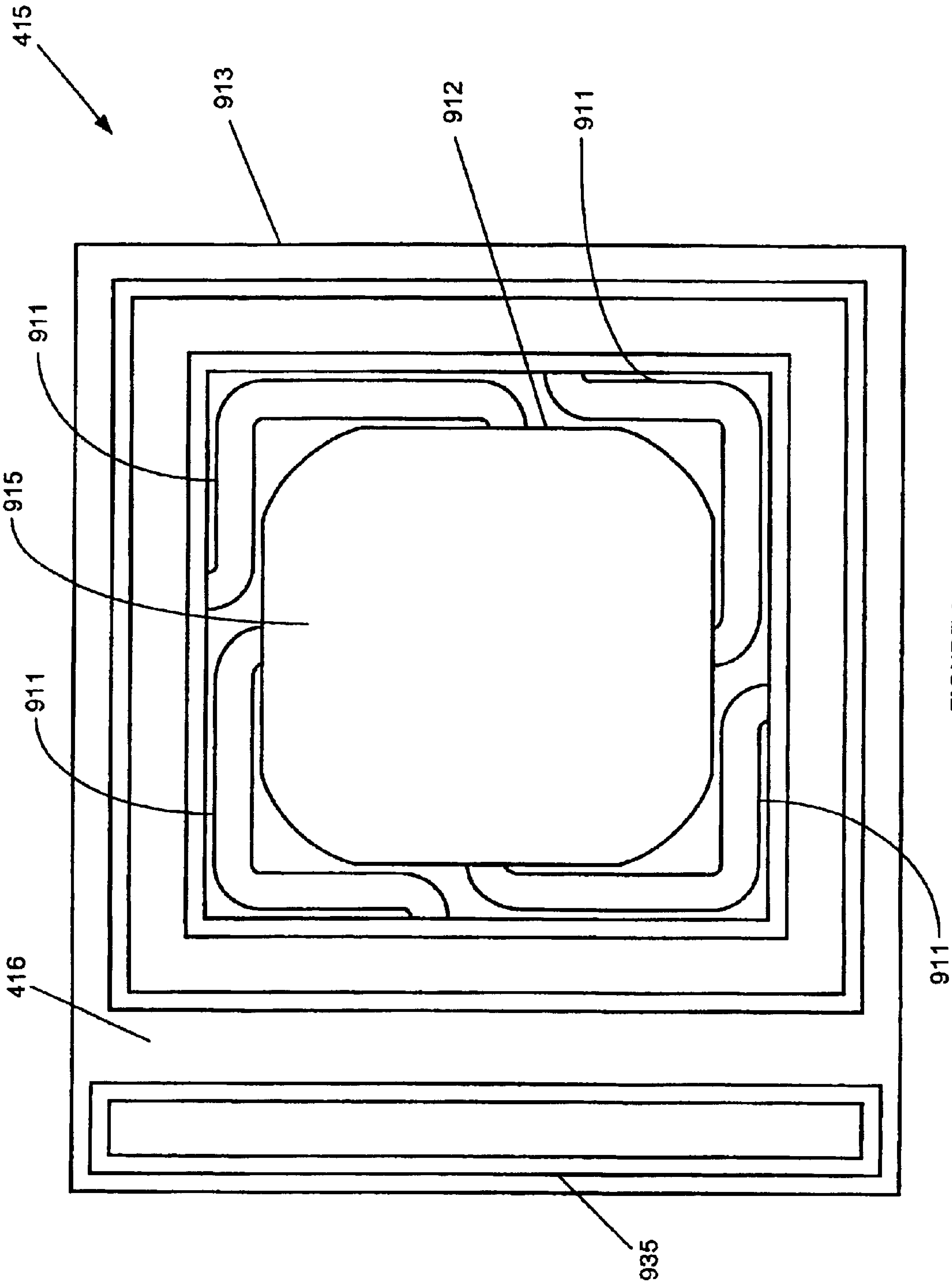
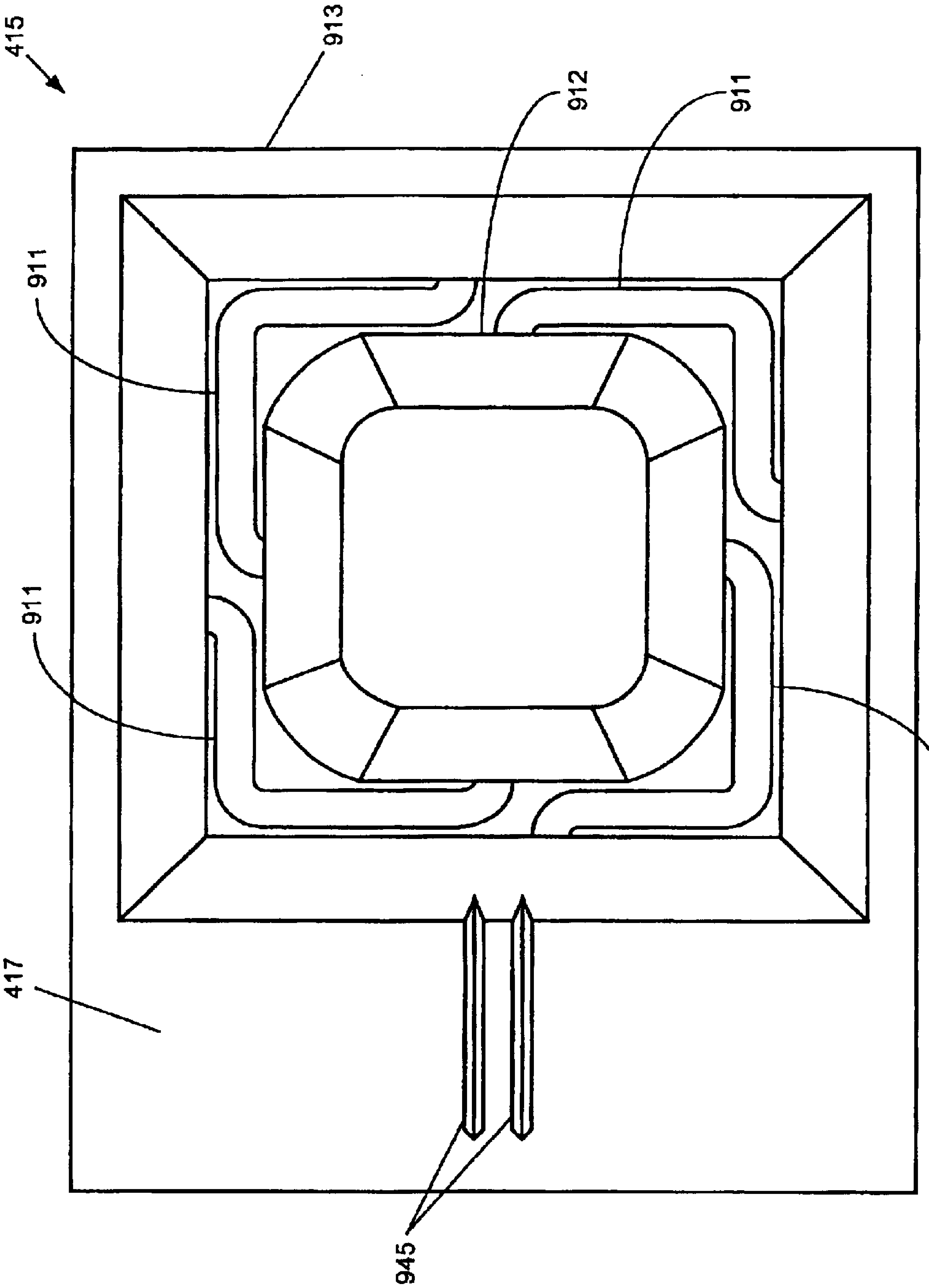


FIGURE 9e



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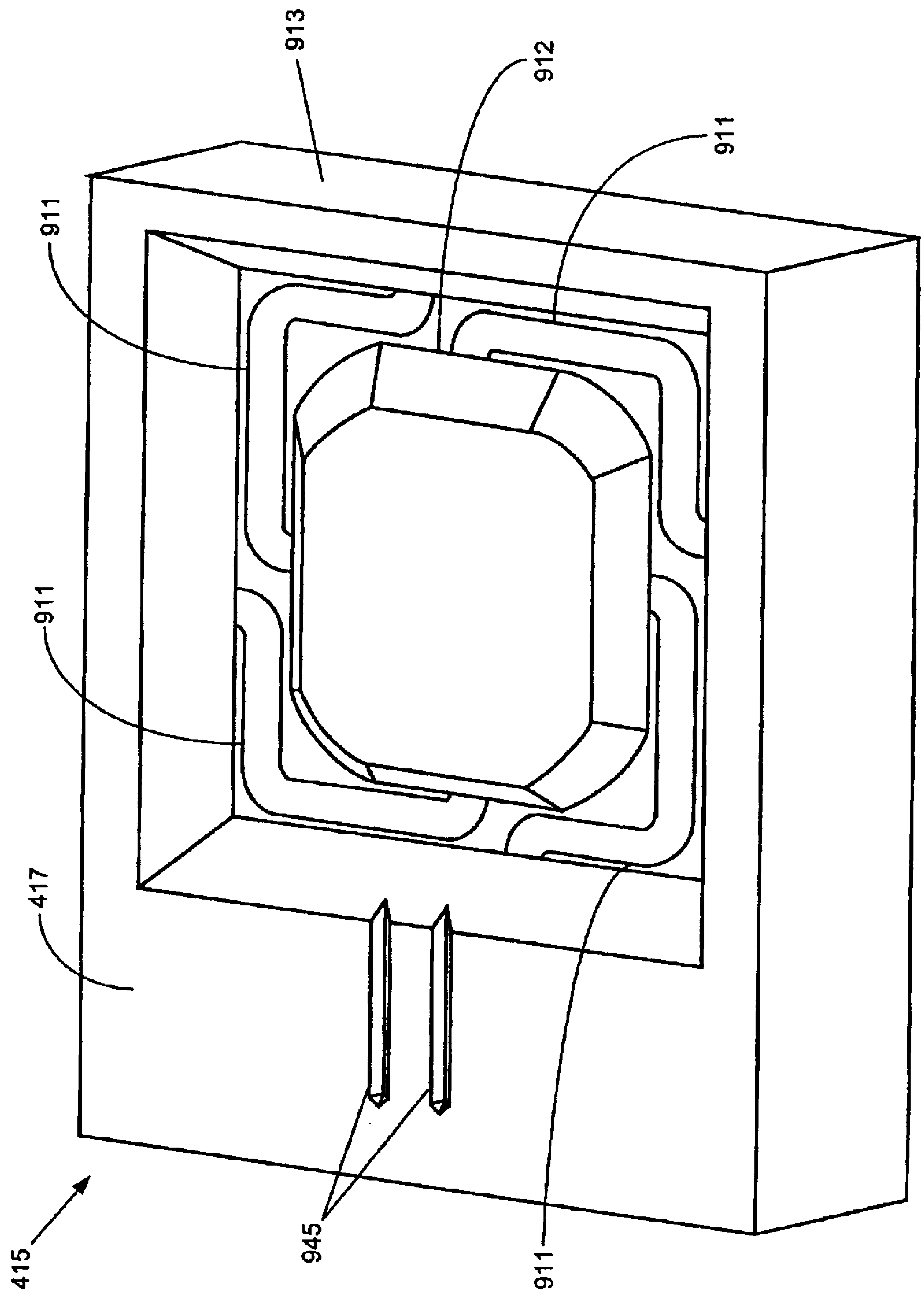

FIGURE 9g

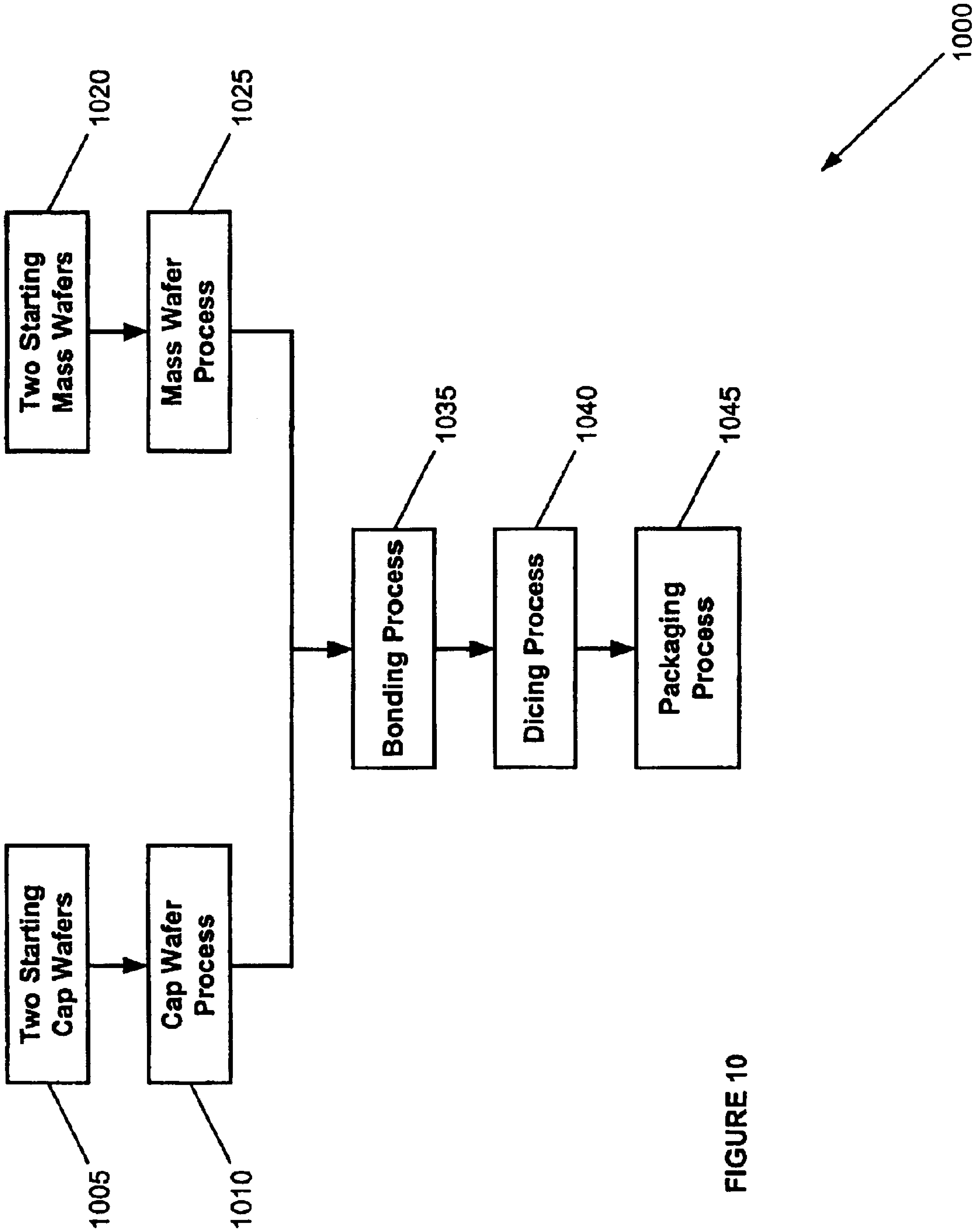
Two Starting Mass Wafers
Mass Wafer Process
Two Starting Cap Wafers
Cap Wafer Process
Bonding Process
Dicing Process
Packaging Process
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FIGURE 10

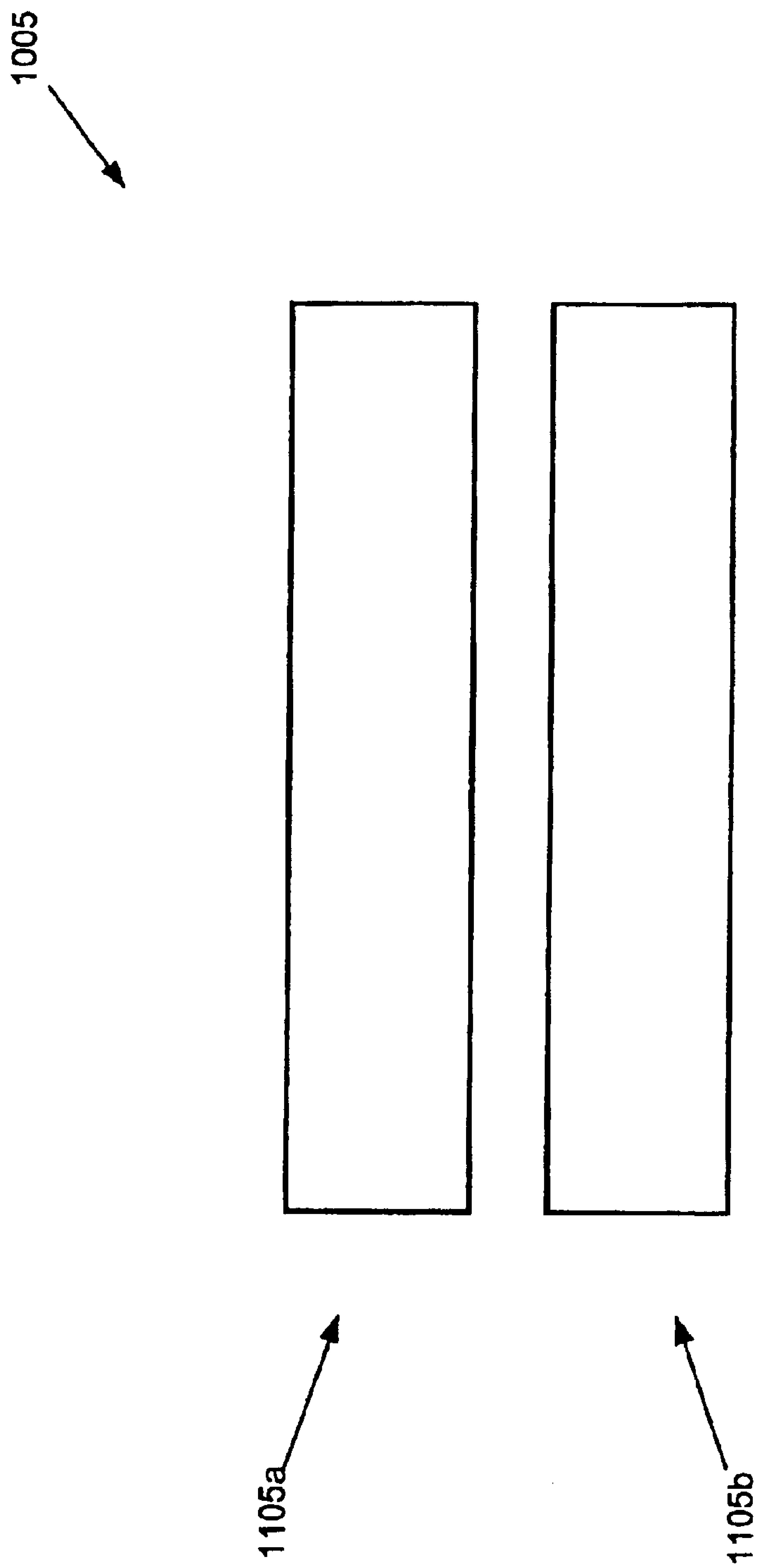


FIGURE 11a

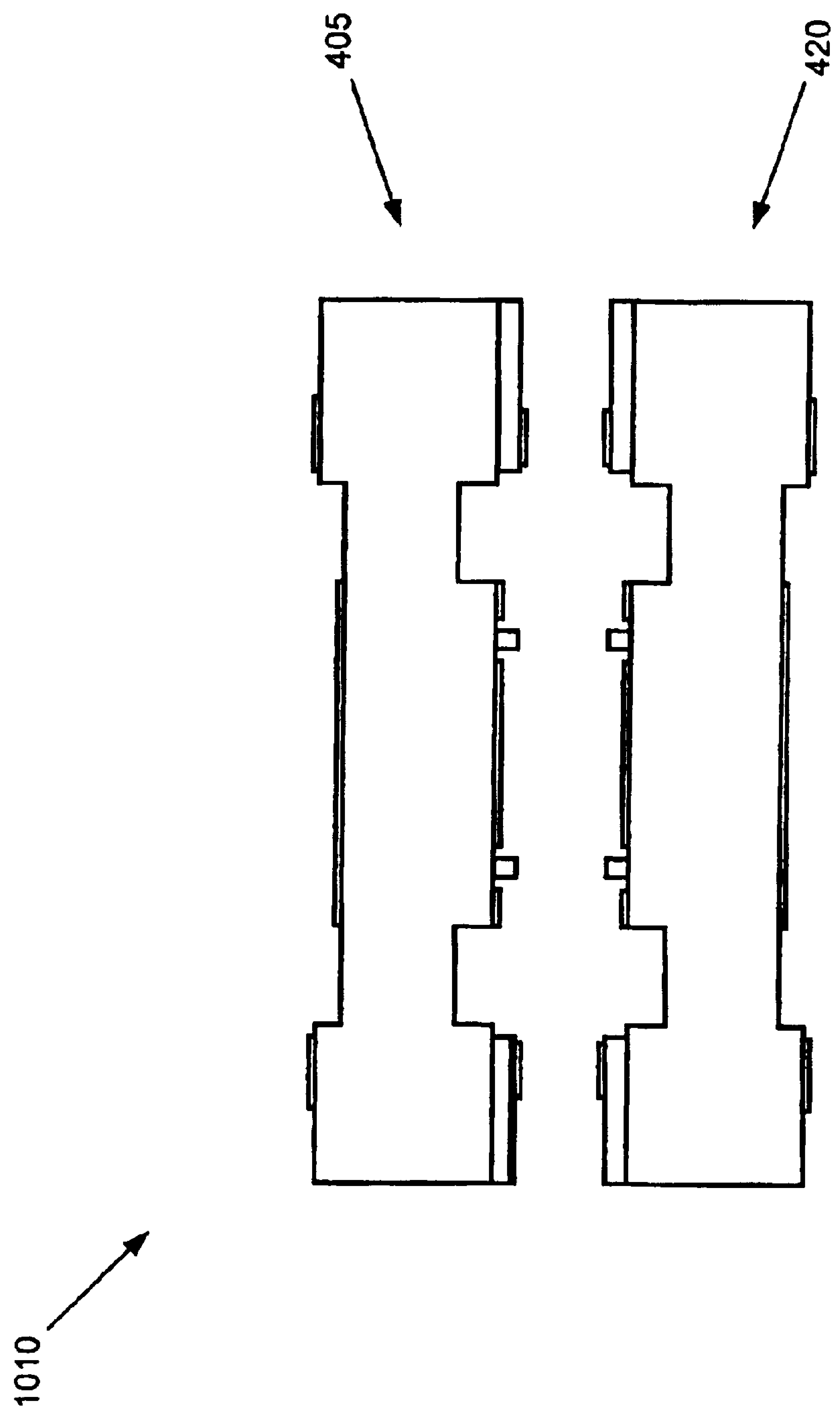
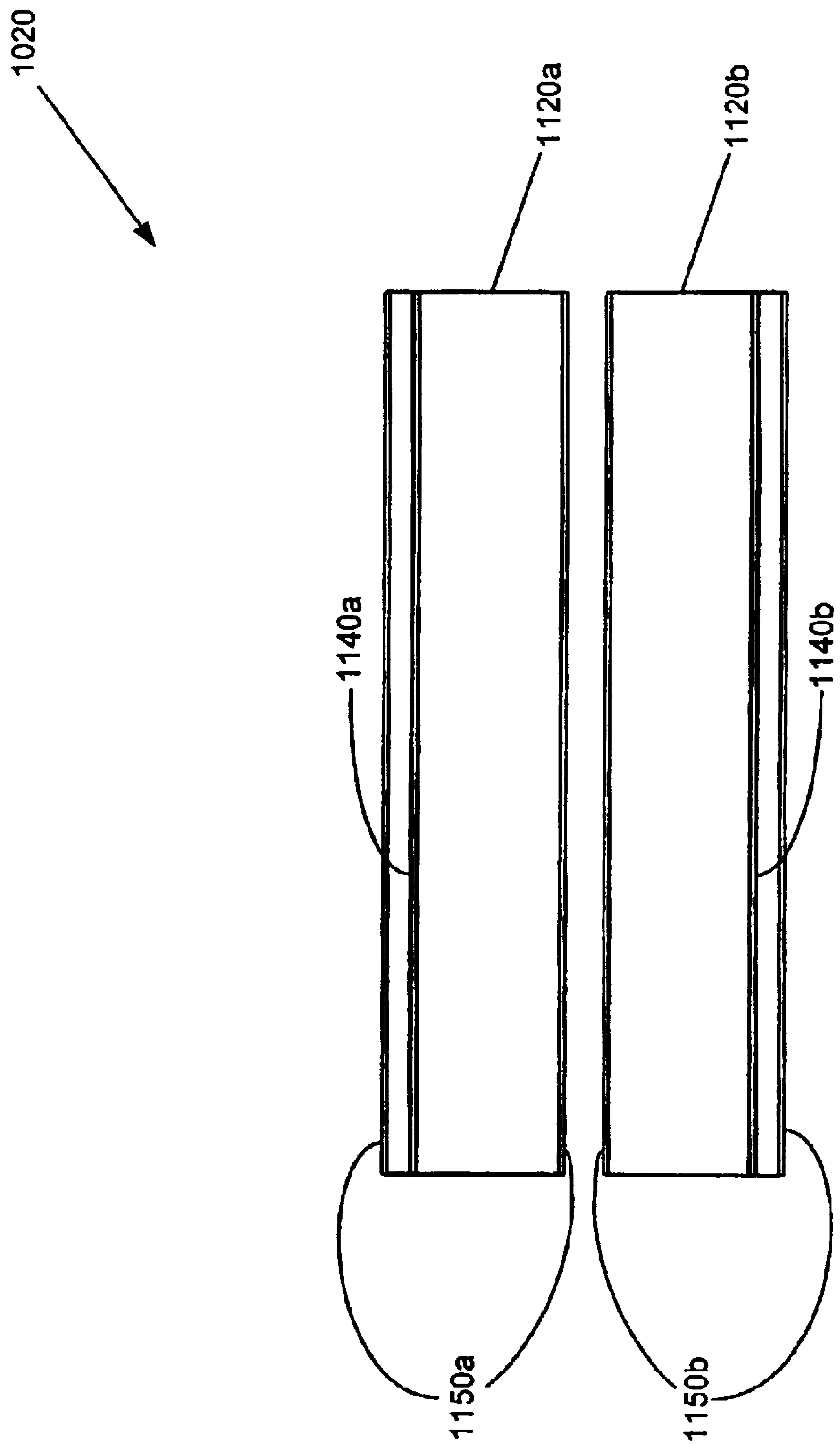


FIGURE 11b



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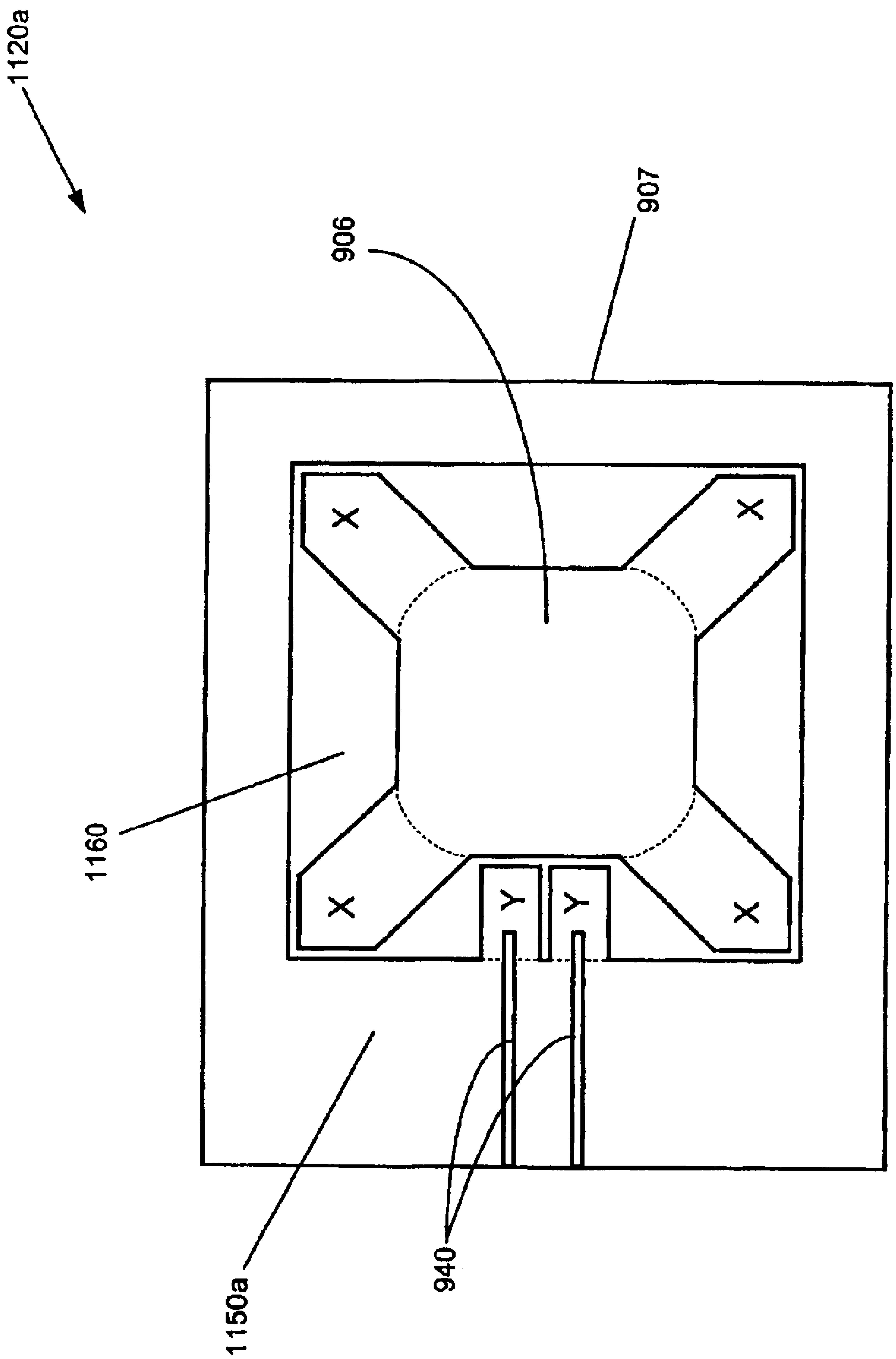

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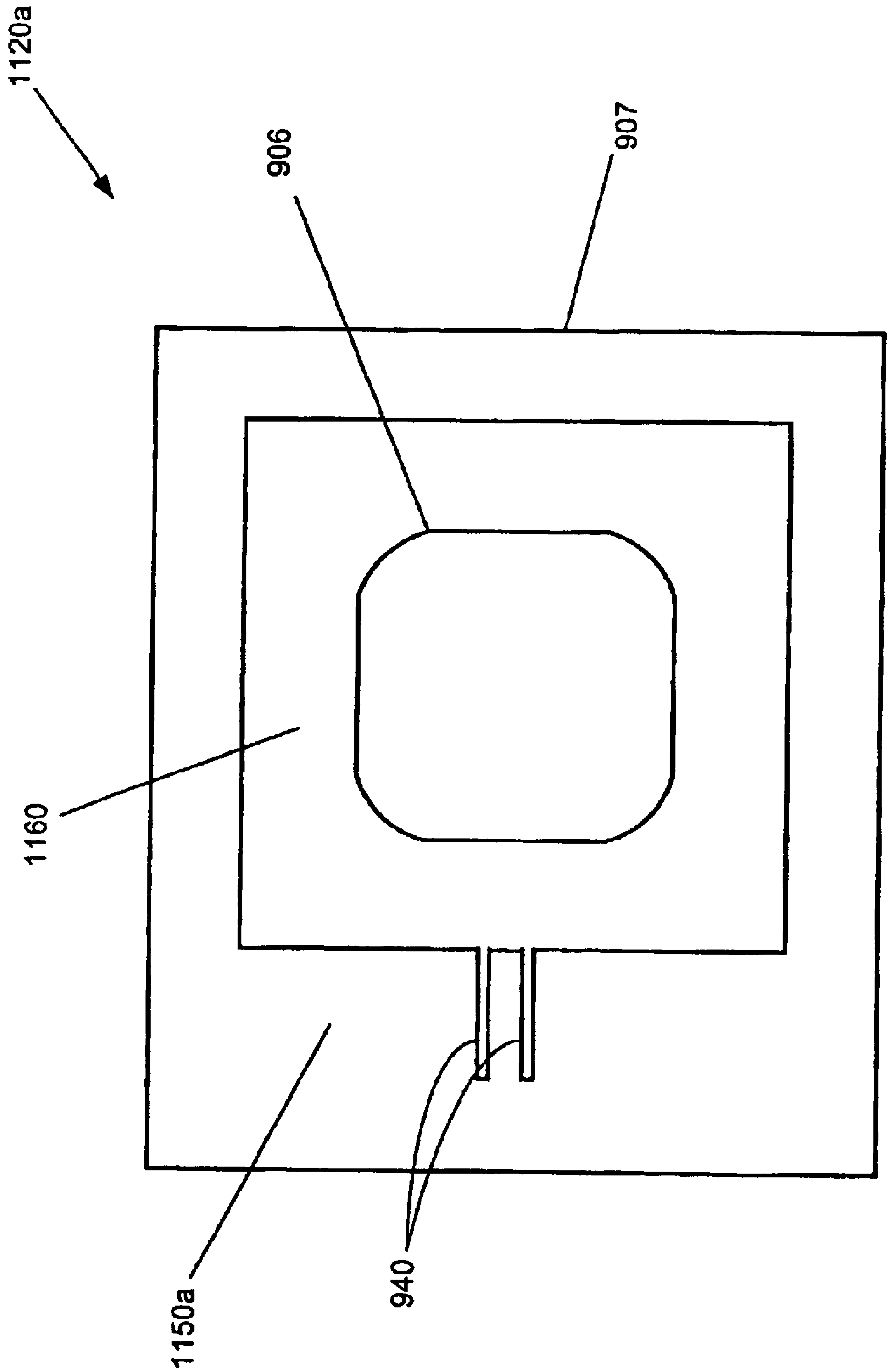

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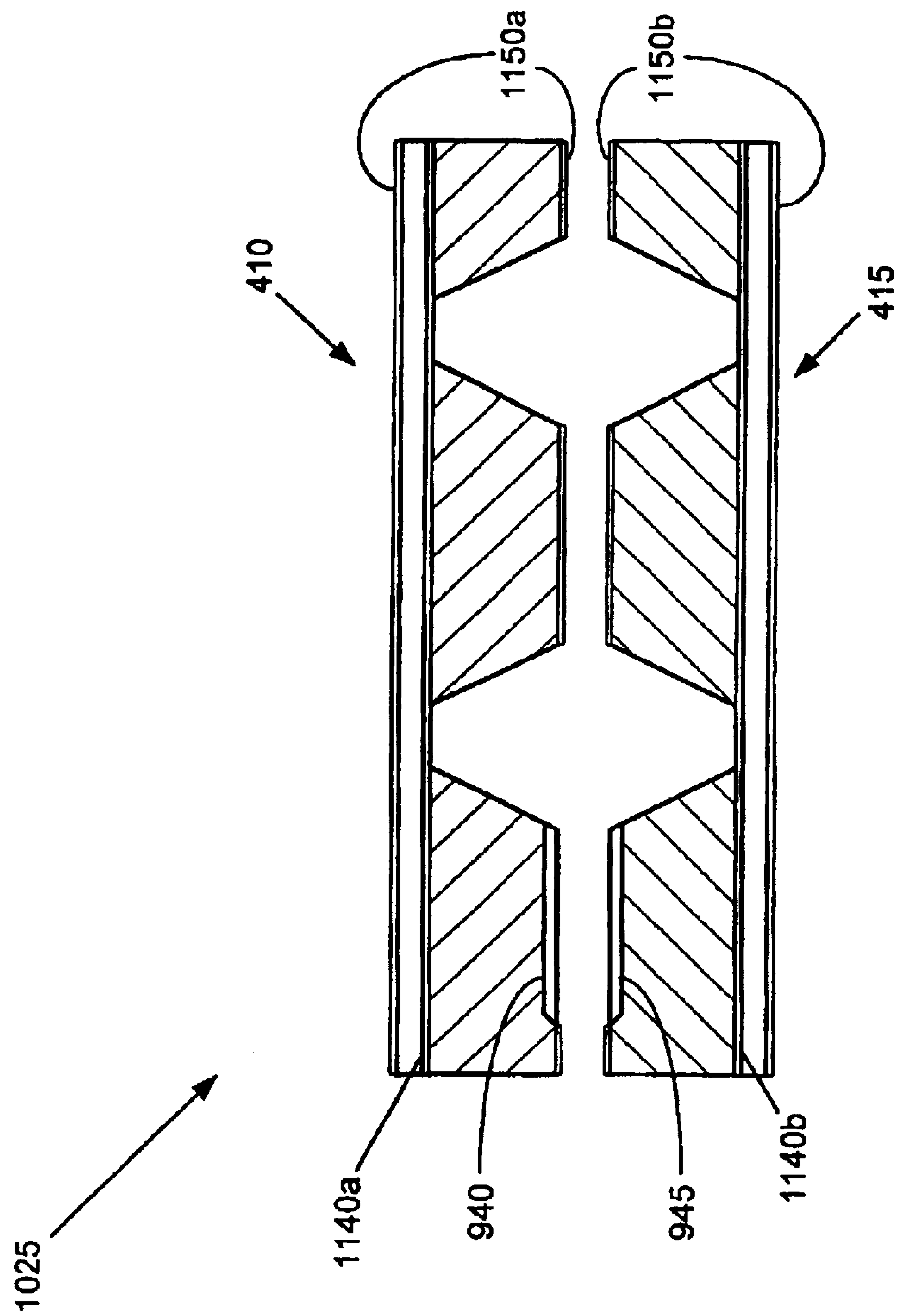

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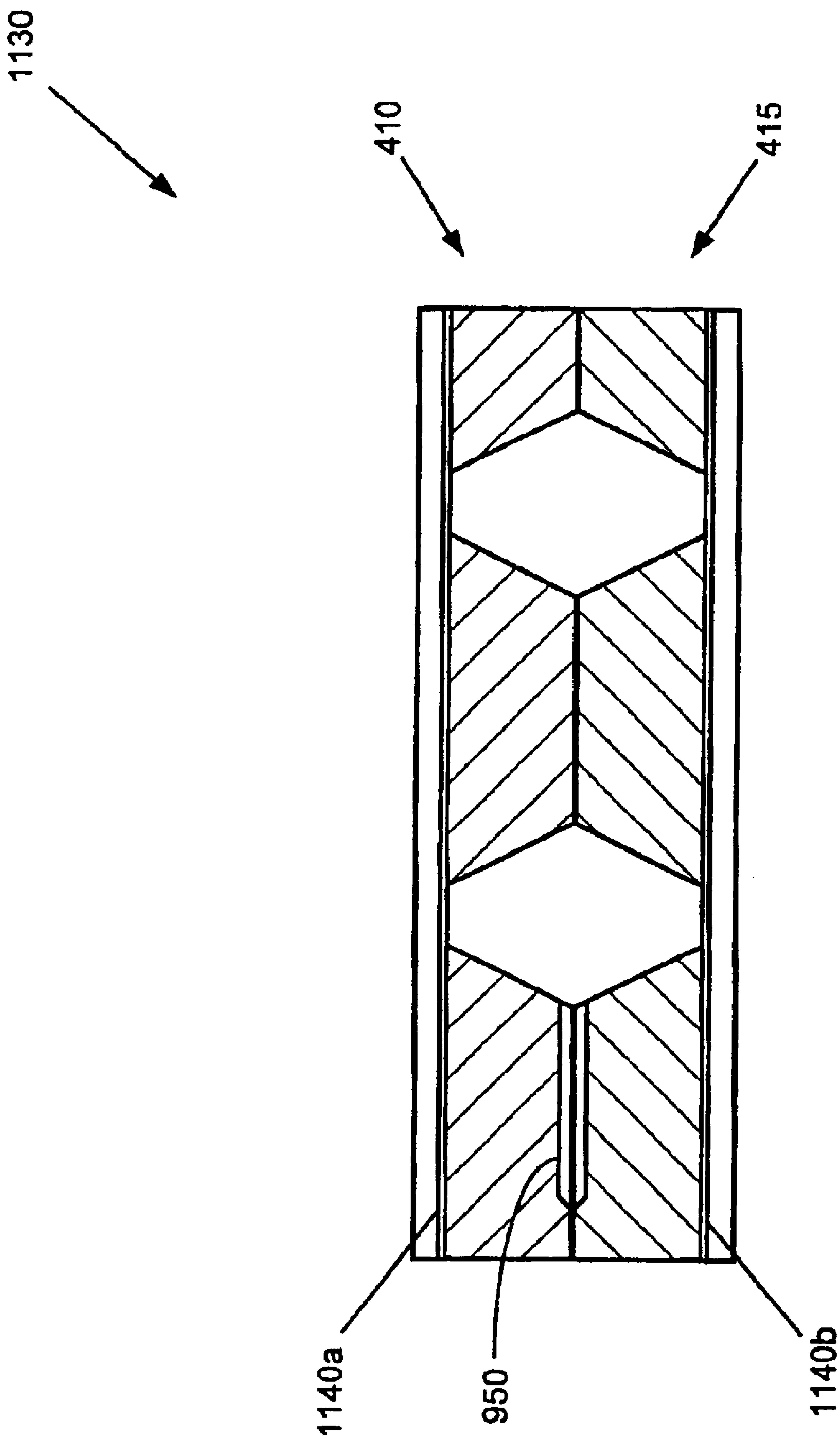

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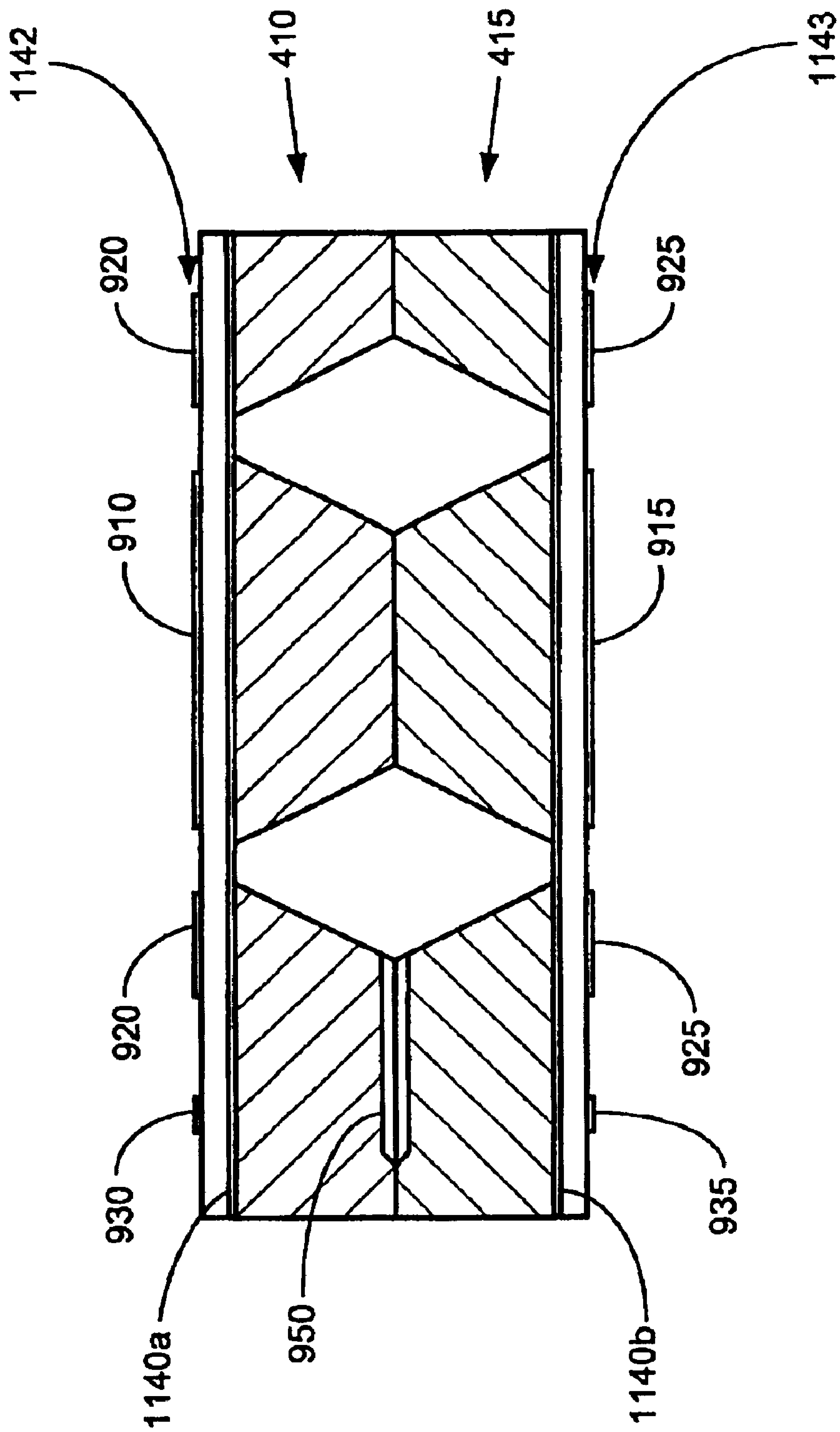
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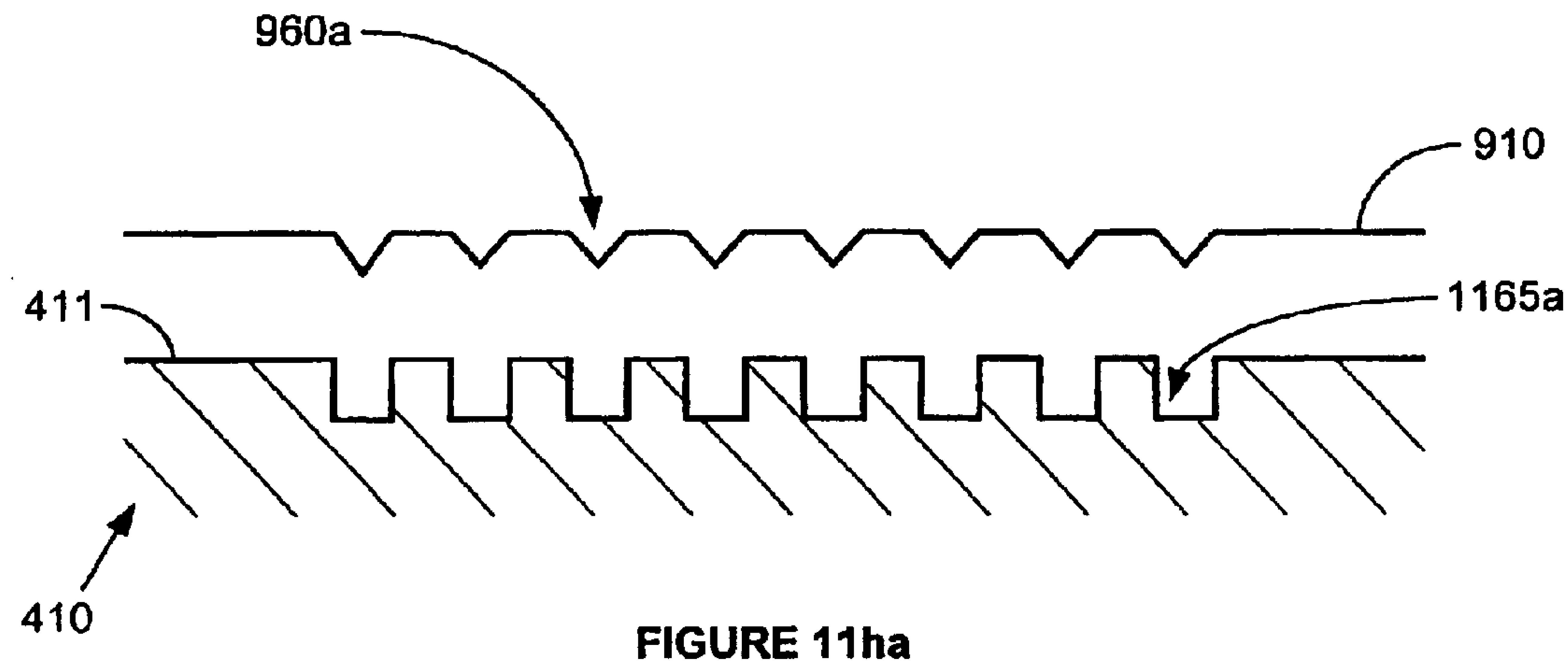
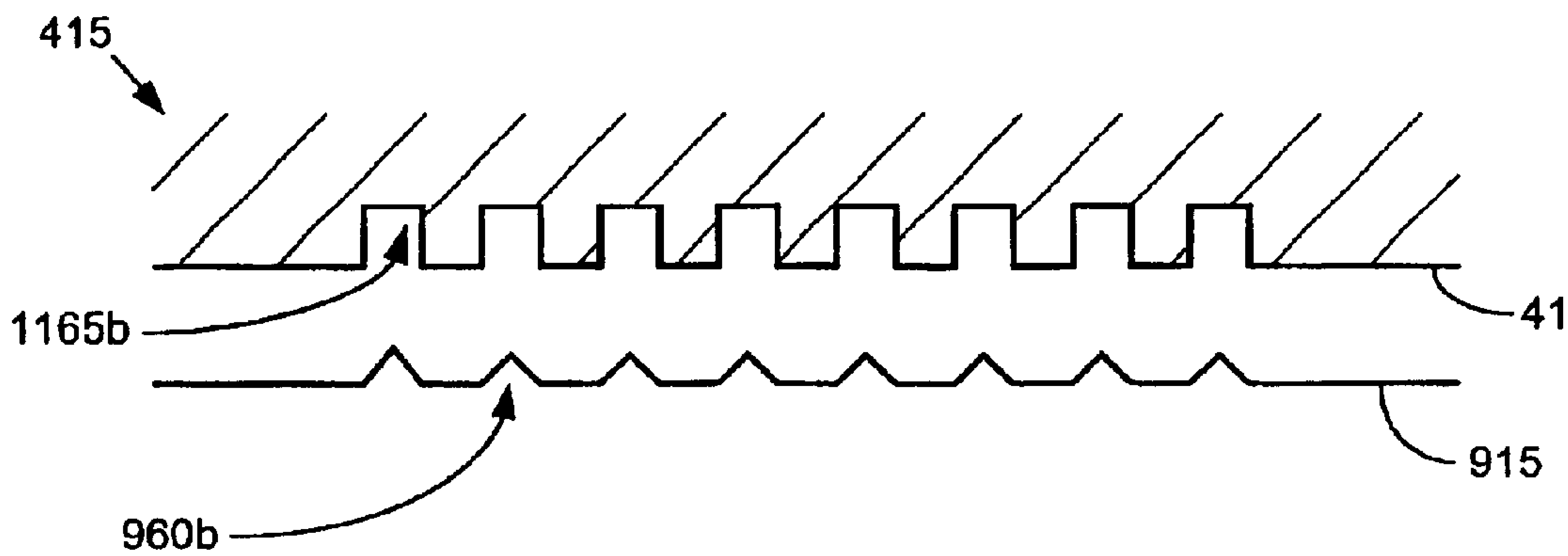


FIGURE 11ha



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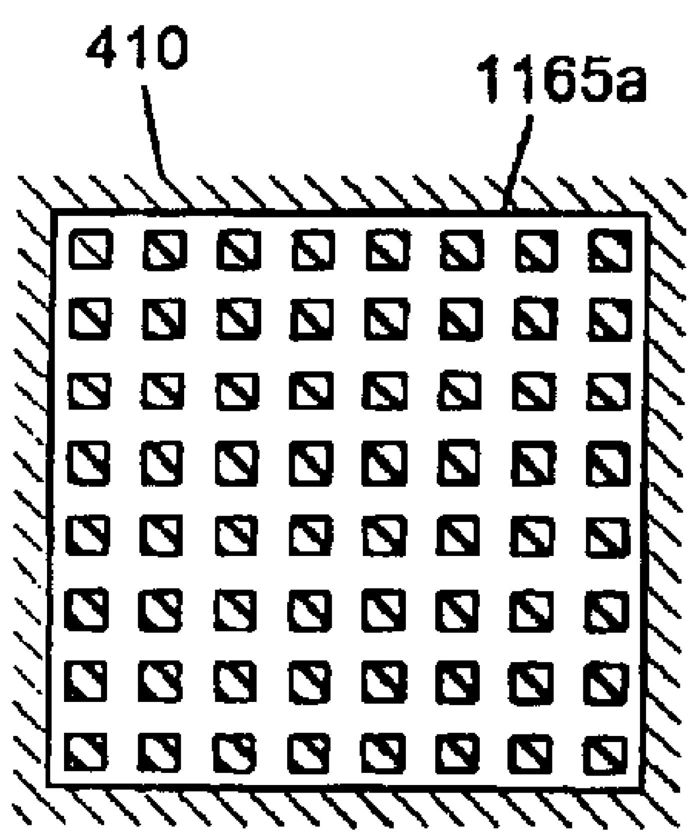

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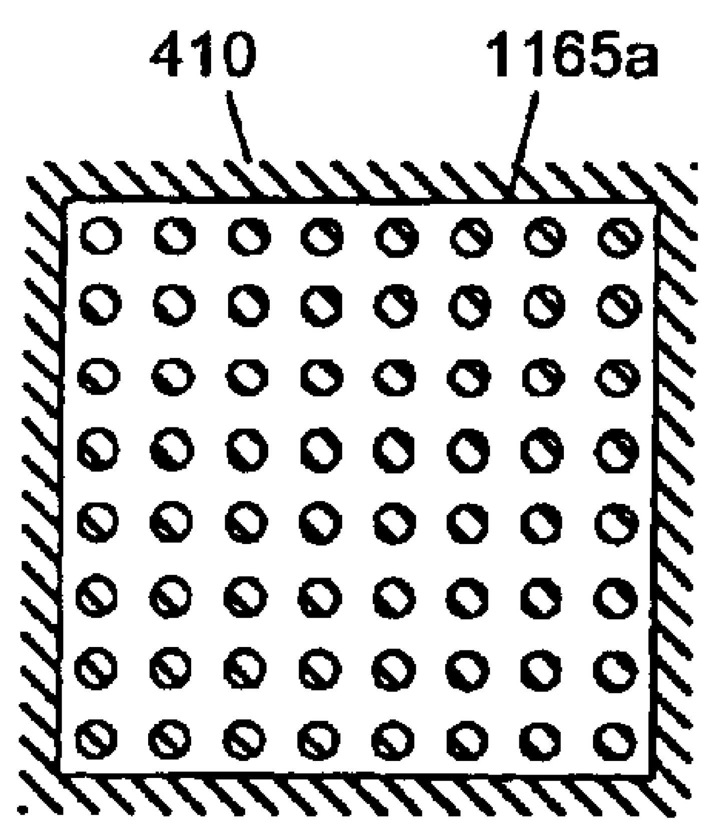

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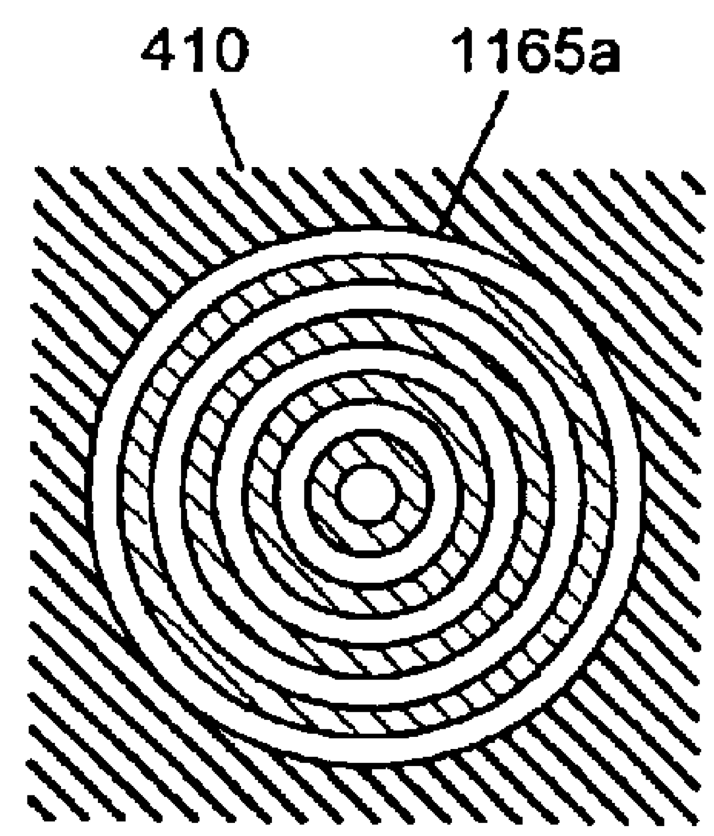

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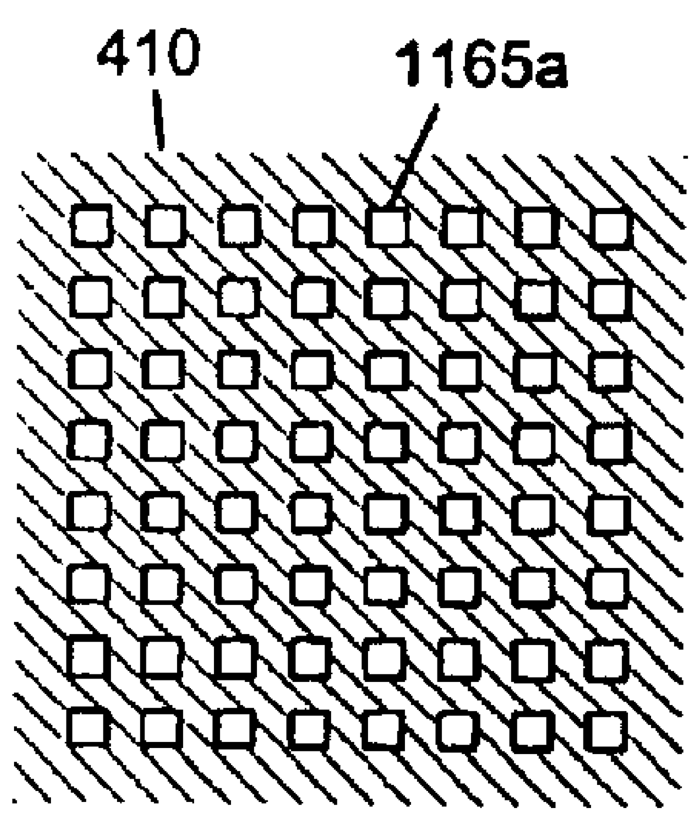
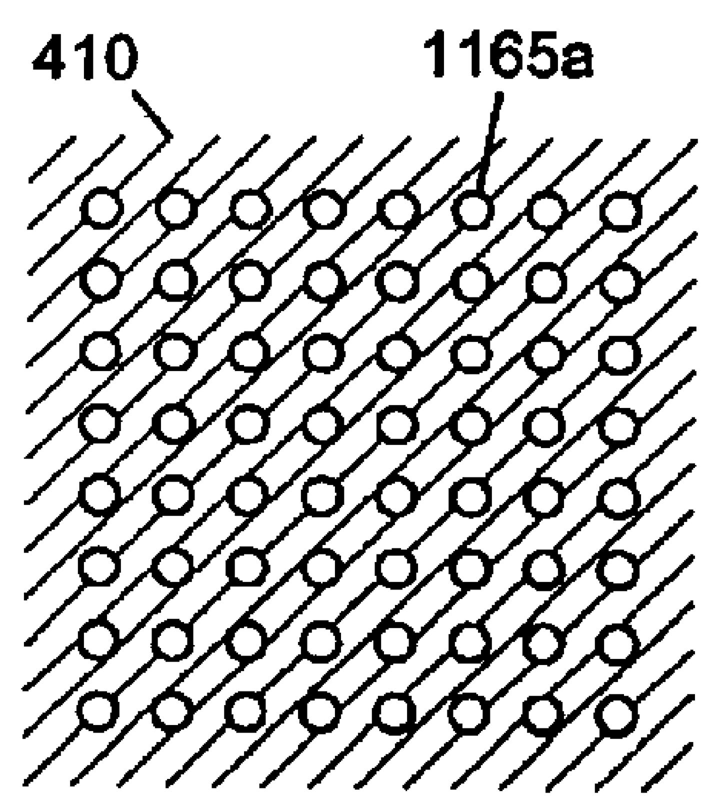


FIGURE 11hf



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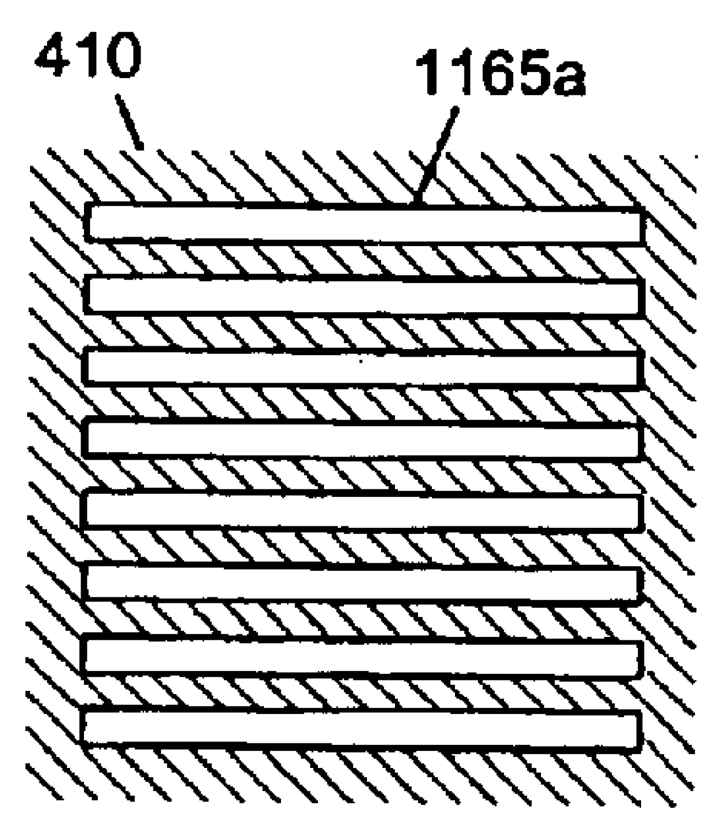

FIGURE 11hh

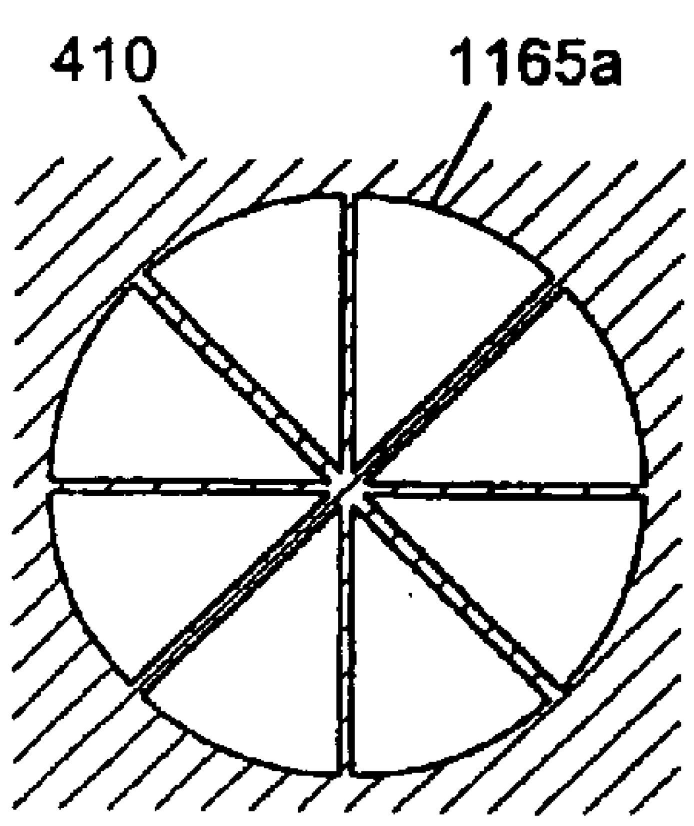

FIGURE 11hi

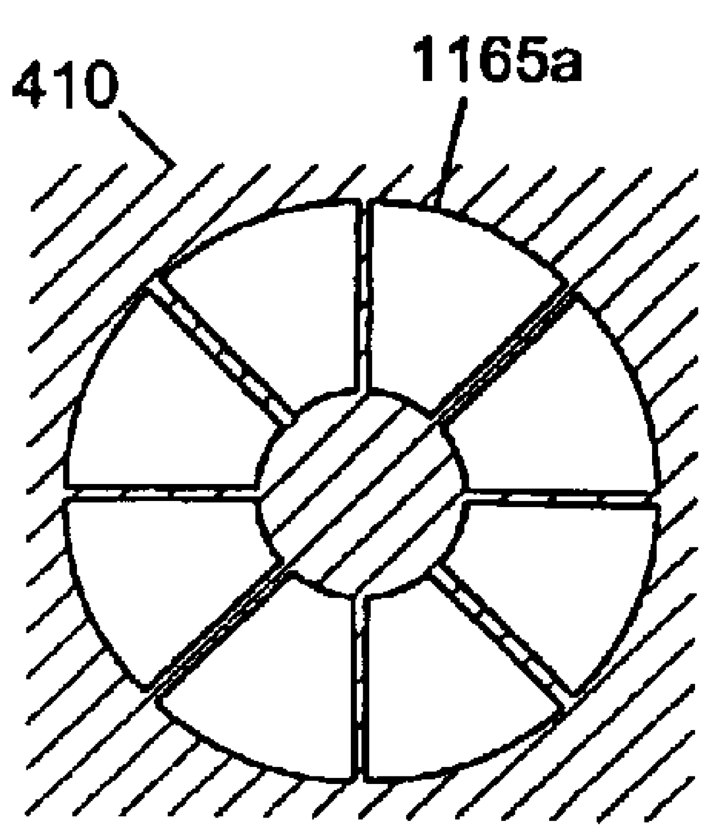

FIGURE 11hj

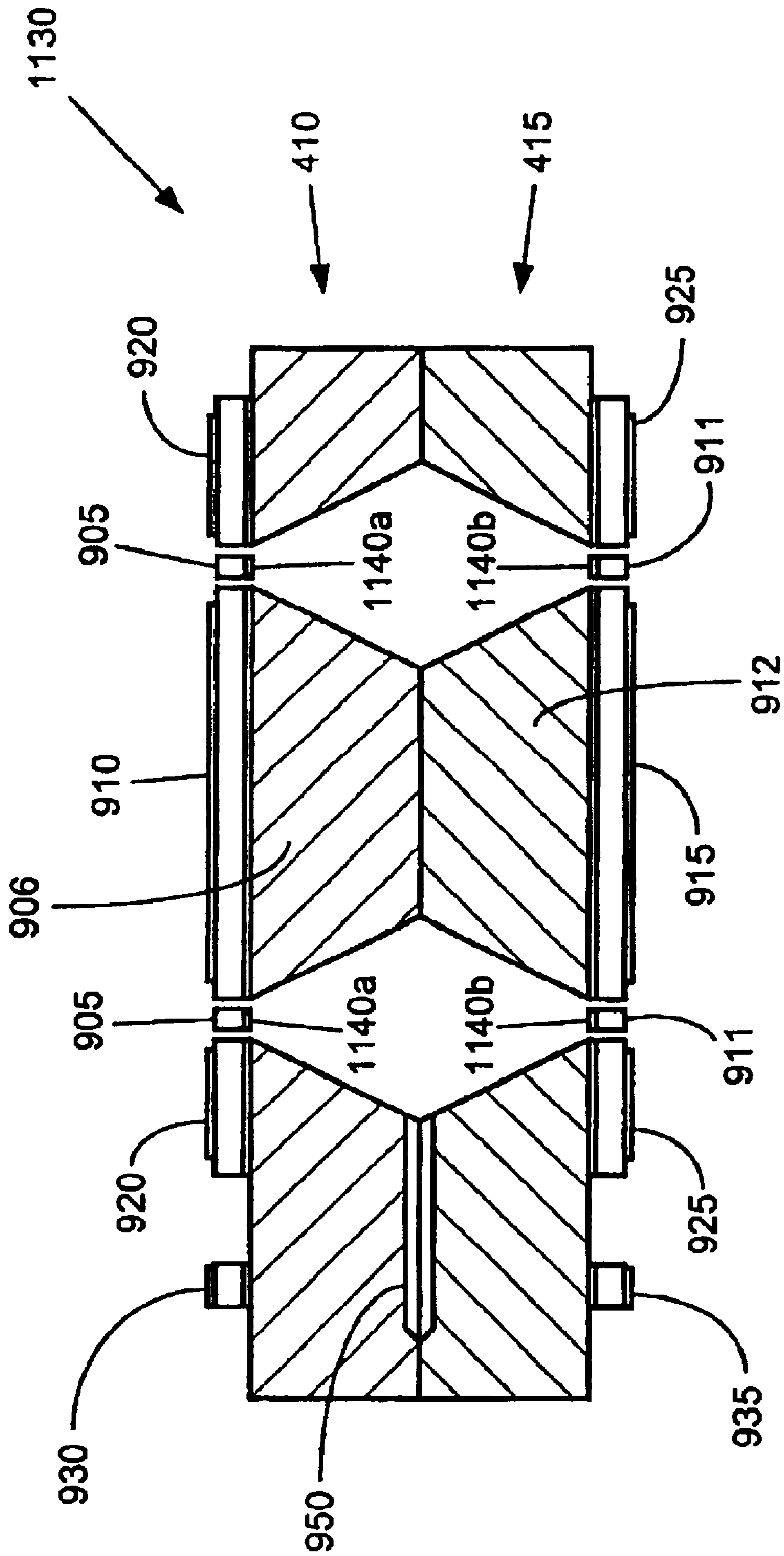
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FIGURE 11I

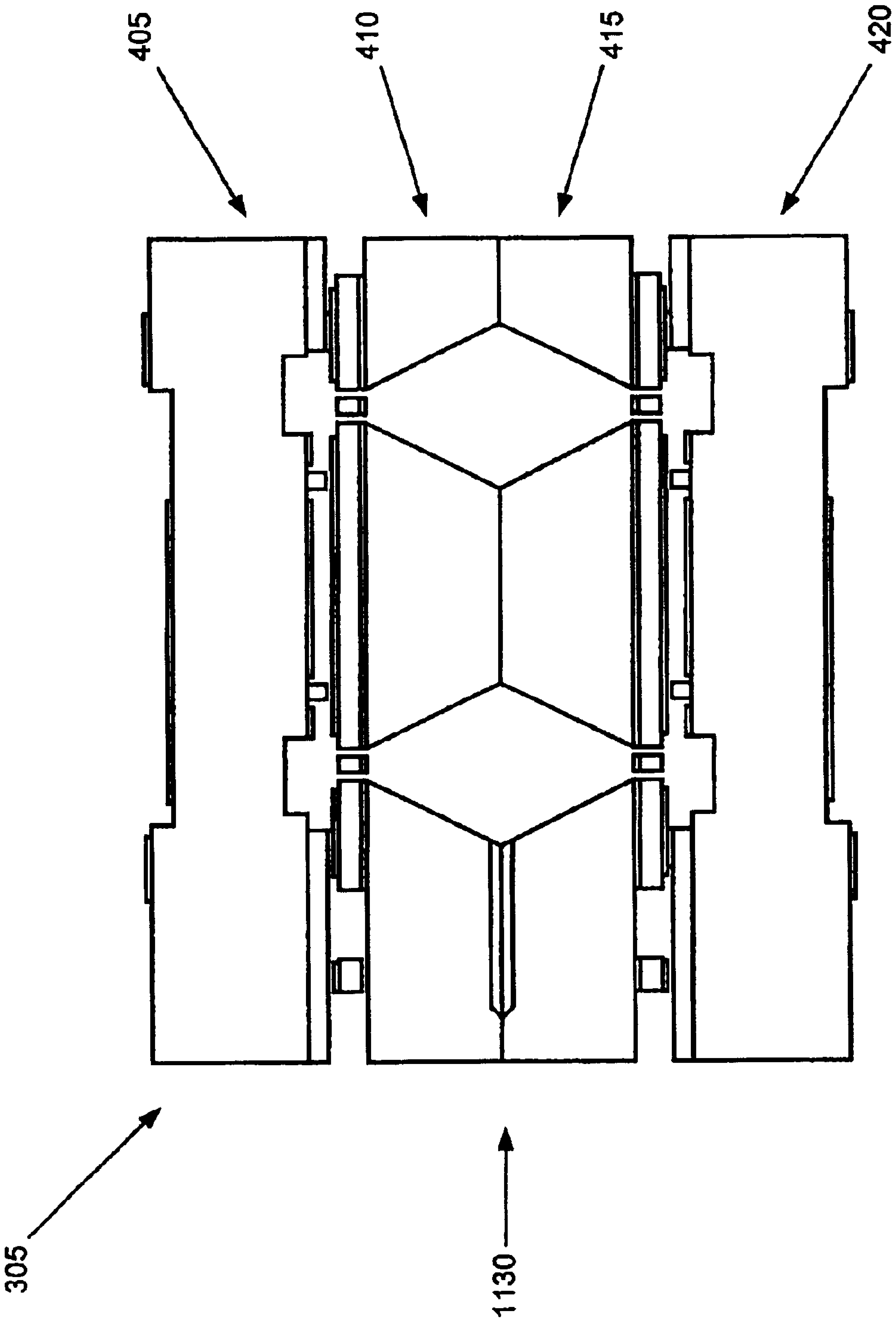

FIGURE 11j

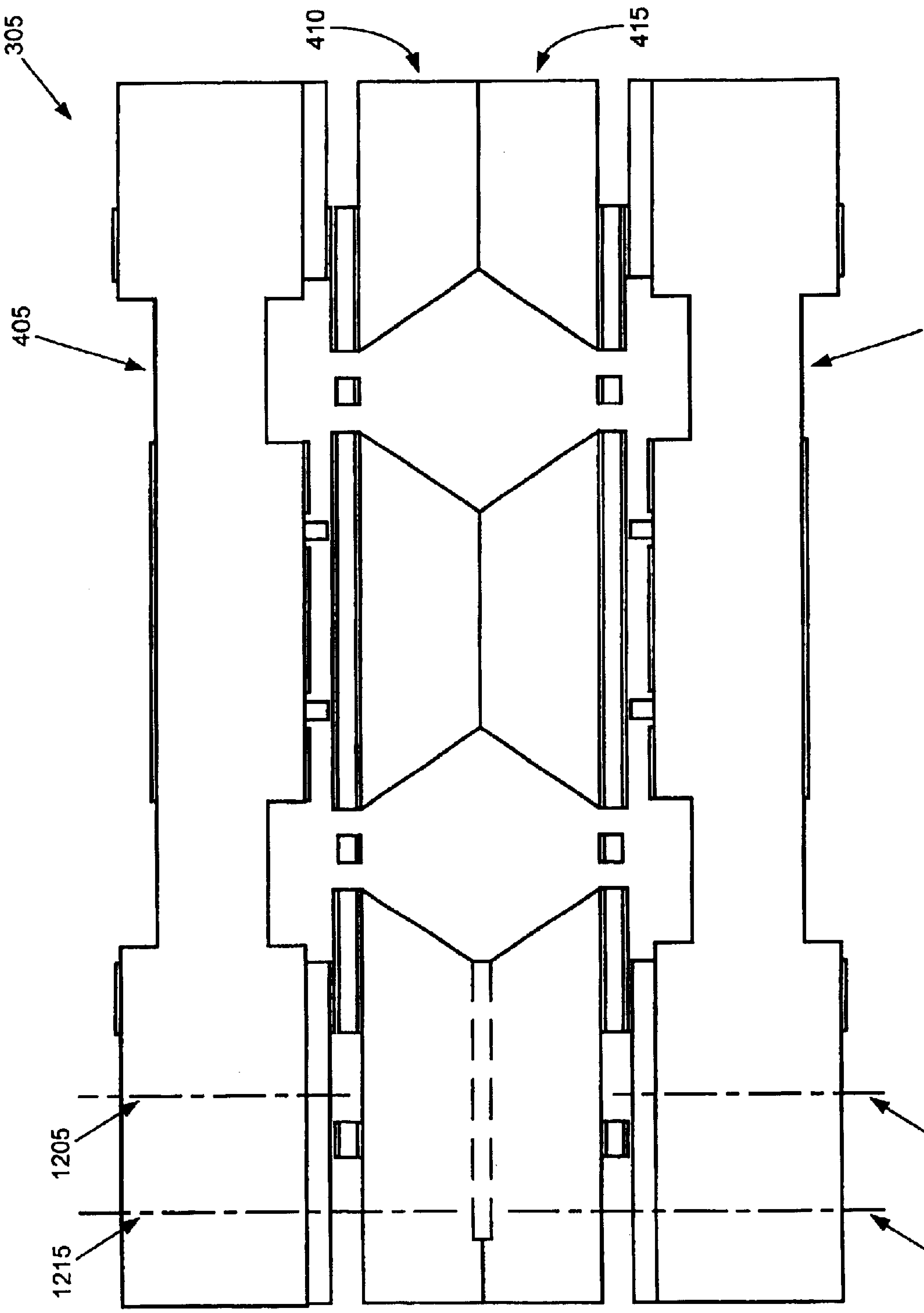

FIGURE 12a

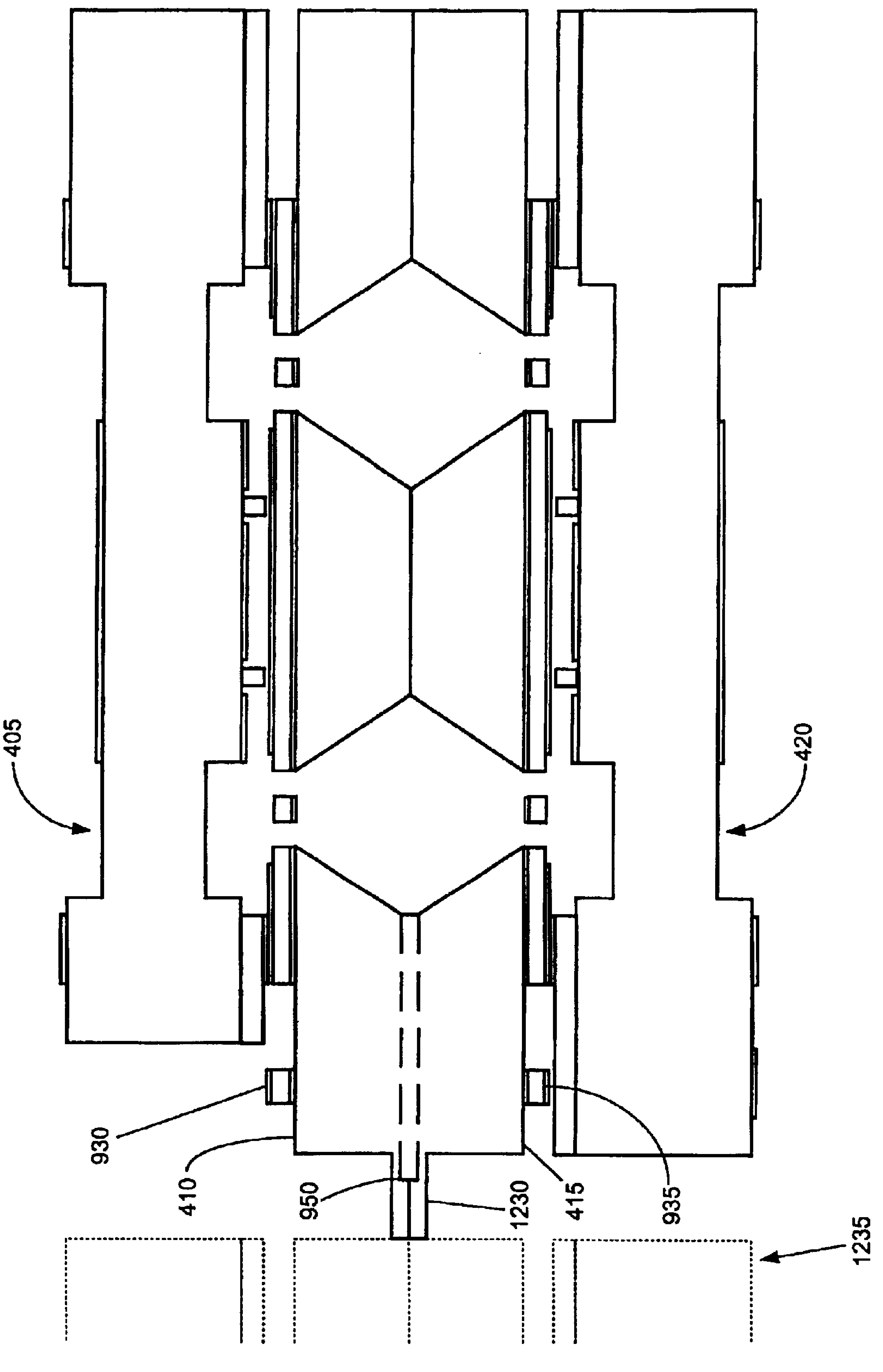

FIGURE 12b

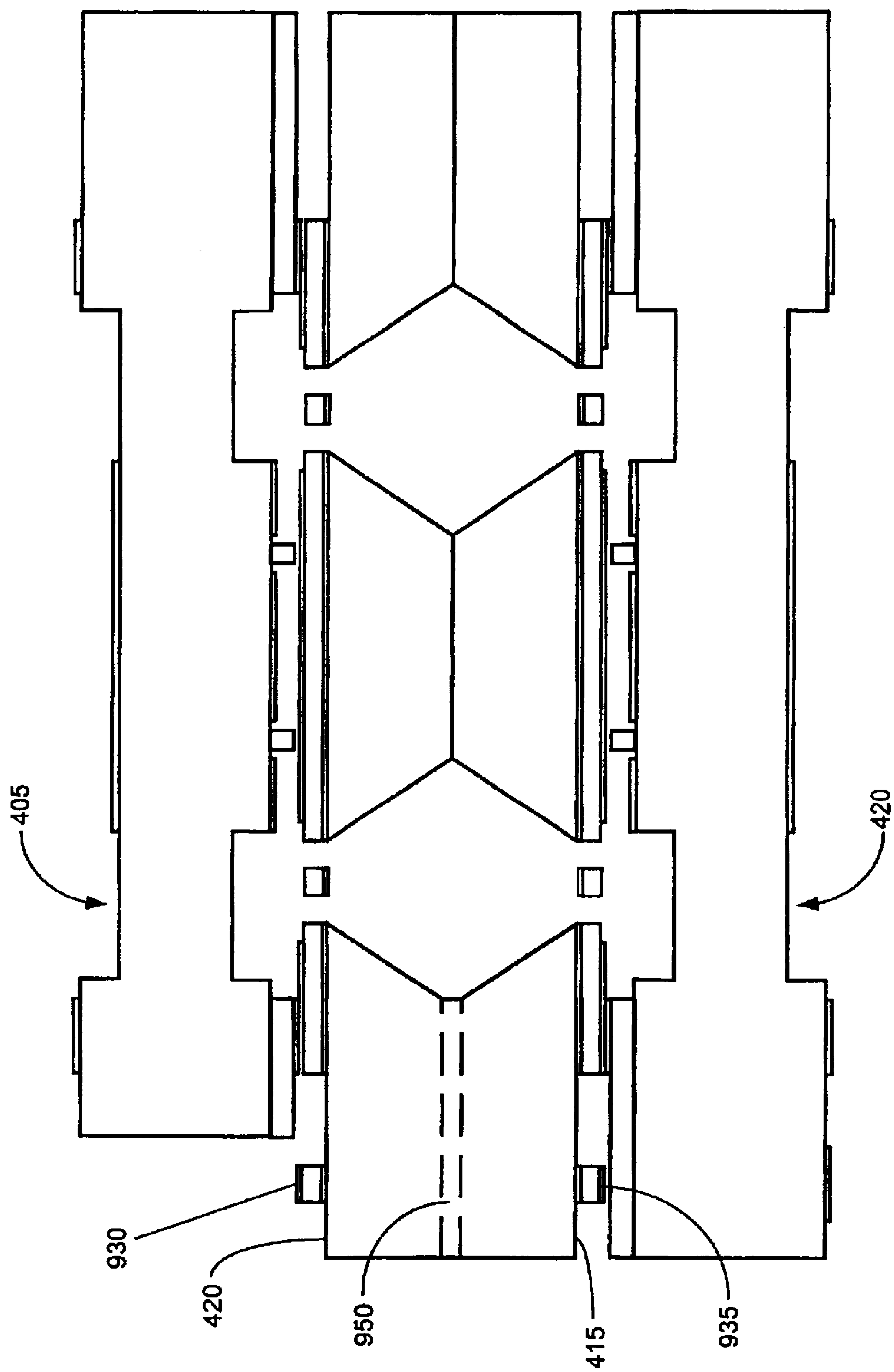

FIGURE 12c

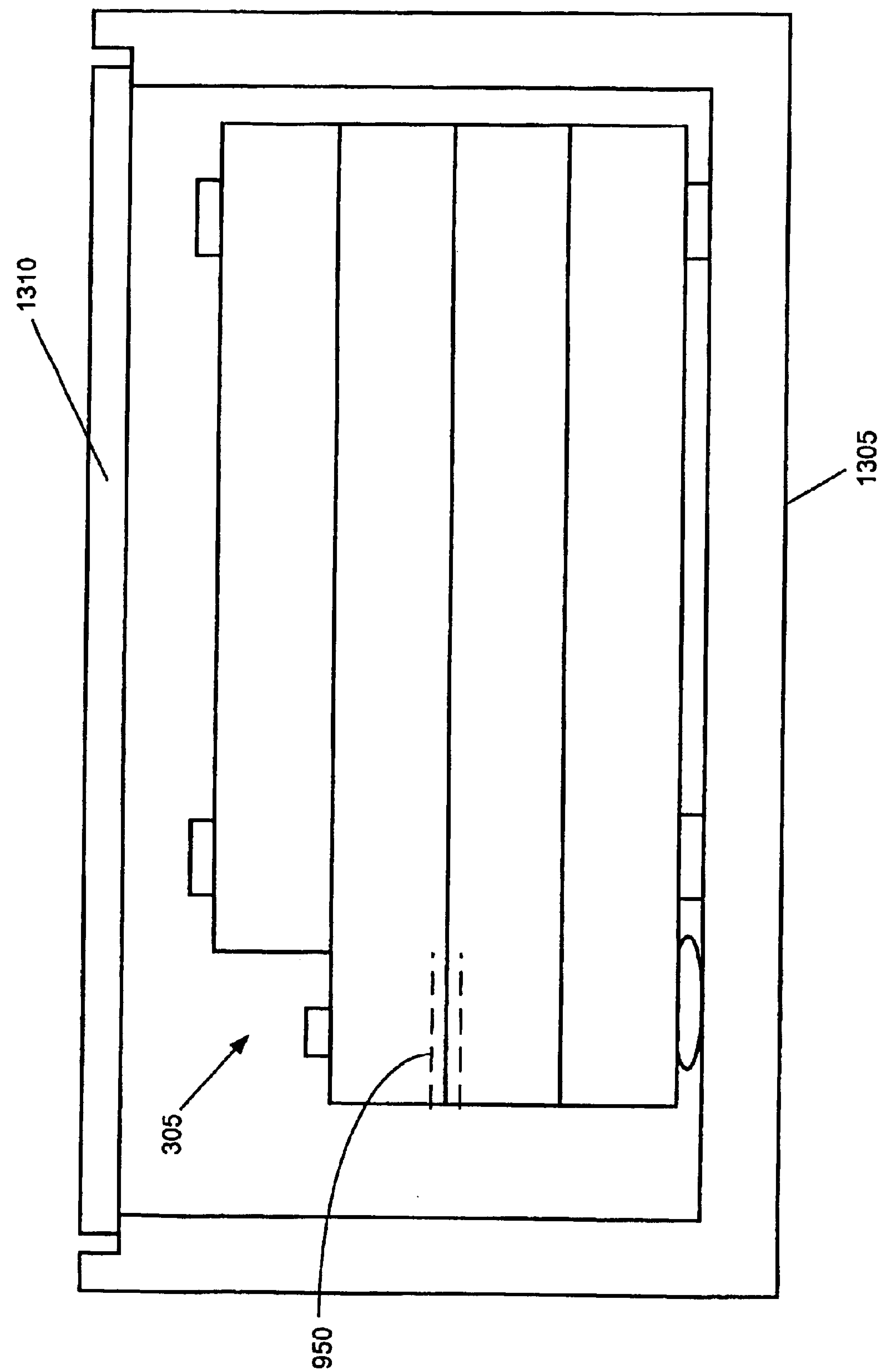

FIGURE 13

SENSOR DESIGN AND PROCESS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. patent application Ser. No. 09/936,640 filed on Apr. 9, 2002, which is a national phase application of international application PCT/US00/40039 filed on Mar. 16, 2000, which claims priority from U.S. provisional patent application 60/125,076 filed on Mar. 17, 1999. The entire contents of each referenced application are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention relates generally to an accelerometer and more particularly to a method of fabricating an accelerometer that reduces bowing of wafer bodies and facilitates the creation of a low-pressure environment within the accelerometer.

Accelerometers are used to detect and record environmental data. In particular, accelerometers are often used in seismic applications to gather seismic data. Existing accelerometers suffer from a number of limitations. These limitations include bowing of cap wafers due to thermal induced stress and an inability to achieve a large dynamic range due to the effects of Brownian noise, both of which adversely affect the quality of data acquired by these accelerometers. Many existing accelerometers fail to provide a large dynamic range, sub micro-G level sensitivity, high shock withstanding, and good cross-axis rejection in a cost-effective technology.

The present invention is directed to overcoming one or more of the limitations of the existing accelerometers.

SUMMARY

According to one embodiment of the present invention, an accelerometer is provided that includes a measurement mass for detecting acceleration, including a housing having a cavity, a spring mass assembly positioned within the cavity, and one or more metal electrode patterns coupled to the spring mass assembly, a top cap wafer coupled to the measurement mass, including a top capacitor electrode, a top cap balanced metal pattern, a top cap press frame recess, and top cap overshock bumpers, and a bottom cap wafer coupled to the measurement mass, including a bottom capacitor electrode, a bottom cap balanced metal pattern, a bottom cap press frame recess, and bottom cap overshock bumpers.

According to another embodiment of the present invention, a method of fabricating an accelerometer is provided that includes fabricating a measurement mass for detecting acceleration that includes a housing having a cavity, and a spring mass assembly positioned within the cavity, fabricating a top cap wafer, fabricating a bottom cap wafer, vertically stacking the measurement mass, the top cap wafer, and the bottom cap wafer in an approximately parallel manner, bonding the top cap wafer to a side of the measurement mass using a bonding process, bonding the bottom cap wafer to another side of the measurement mass using the bonding process, and making one or more dicing cuts at predetermined locations on the accelerometer.

According to another embodiment of the present invention, a method of bonding an accelerometer is provided that includes fabricating a measurement mass that includes a housing having a cavity, a spring mass assembly positioned within the cavity, and one or more bond rings coupled to the housing, fabricating a top cap wafer that includes a top bond ring and a top cap press frame recess, fabricating a bottom cap wafer that includes a bottom bond ring and a bottom cap press frame recess, vertically stacking the measurement mass, the top cap wafer, and the bottom cap wafer in an approximately parallel manner, bonding the top cap wafer to a side of the measurement mass using a bonding process, and bonding the bottom cap wafer to another side of the measurement mass using the bonding process.

According to another embodiment of the present invention, a method of shaping a wafer to create components for a sensor is provided that includes applying a protective layer to the wafer, patterning the protective layer to create an area of exposure, applying one or more etching agents to the area of exposure to remove the protective layer within the area of exposure, applying one or more etching agents to the area exposure to shape the wafer into a housing, a measurement mass, and one or more springs, and maintaining the etch-stop layer on the springs.

According to another embodiment of the present invention, a sensor for measuring data is provided that includes a measurement mass assembly including a housing, a measurement mass including one or more electrodes, and a plurality of springs for coupling the measurement mass to the housing, a top cap wafer coupled to the measurement mass assembly including a top cap overshock bumper pattern designed to reduce stiction within the sensor, and a bottom cap wafer coupled to the measurement mass assembly including a bottom cap overshock bumper pattern designed to reduce stiction within the sensor.

According to another embodiment of the present invention, a metal electrode pattern for use in a sensor is provided that includes a metal electrode including a stiction-reducing pattern.

According to another embodiment of the present invention, a method of creating a stiction-reducing metal electrode pattern for use within a sensor is provided that includes etching a surface pattern onto a surface of the sensor, and applying a metal layer to the surface of the sensor including the surface pattern, and molding the metal layer to create the stiction-reducing metal electrode pattern.

According to another embodiment of the present invention, a method of creating a metal electrode pattern including reduced-thickness recesses for reducing stiction between the metal electrode pattern and overshock bumpers within an accelerometer is provided that includes creating a lower metal electrode pattern layer, applying an upper metal electrode pattern layer on top of the lower metal electrode pattern layer, and selectively removing one or more portions of the upper metal electrode pattern layer to create the reduced-thickness recesses and expose the underlying lower metal electrode pattern layer within the metal electrode pattern.

According to another embodiment of the present invention, a method of creating a metal electrode pattern including cavities for reducing stiction between the metal electrode pattern and overshock bumpers within an accelerometer is provided that includes creating a lower metal electrode pattern layer, applying an upper metal electrode pattern layer on top of the lower metal electrode pattern layer, and selectively removing one or more portions of the upper metal electrode pattern layer and the lower metal electrode pattern layer to create the cavities within the metal electrode pattern.

The present embodiments of the invention provide an accelerometer for providing reliable data measurements.

The accelerometer is vacuum-sealed and includes a balanced metal pattern to prevent degradation of the performance of the accelerometer. A dicing process is performed on the accelerometer to isolate the electrical leads of the accelerometer. The accelerometer further includes overshock protection bumpers and patterned metal electrodes to reduce stiction during the operation of the accelerometer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an embodiment of a system used to acquire environmental data measurements.

FIG. **2** illustrates an embodiment of sensors and cabling used within the system of FIG. **1**.

FIG. **3***a* is a cross-sectional side view of the positioning of an accelerometer within the sensor of FIG. **1**.

FIG. **3***b* is a cross-sectional top view of the positioning of an accelerometer within the sensor of FIG. **1**.

FIG. **4** illustrates a top perspective view of an embodiment of the accelerometer of FIG. **3***a*.

FIG. **5** illustrates a bottom perspective view of the accelerometer of FIG. **4**.

FIG. **6** illustrates a cross-sectional view of the accelerometer of FIG. **4**.

FIG. **7***a* illustrates a cross-sectional view of, a top cap wafer of the accelerometer of FIG. **4**.

FIG. **7***b* illustrates a top view of the top cap wafer of FIG. **7***a*.

FIG. **7***c* illustrates a bottom view of the top cap wafer of FIG. **7***a*.

FIG. **7***d* illustrates an embodiment of an arrangement of overshock bumpers on the top cap wafer of FIG. **7***a*.

FIG. **7***e* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***f* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***g* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***h* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***i* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***j* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***k* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **7***l* illustrates an embodiment of an alternative arrangement of the overshock bumpers of FIG. **7***d*.

FIG. **8***a* illustrates a cross-sectional view of a bottom cap wafer of the accelerometer of FIG. **4**.

FIG. **8***b* illustrates a bottom view of the bottom cap wafer of FIG. **8***a*.

FIG. **8***c* illustrates a top view of the bottom cap wafer of FIG. **8***a*

FIG. **9***a* illustrates a cross-sectional view of a mass wafer pair of the accelerometer of FIG. **4**.

FIG. **9***aa* illustrates a cross-sectional view of a top cap overshock bumper and a patterned metal electrode within the accelerometer of FIG. **6**.

FIG. **9***ab* illustrates a cross-sectional view of a bottom cap overshock bumper and a patterned metal electrode within the accelerometer of FIG. **6**.

FIG. **9***ac* illustrates an embodiment of metal electrodes including reduced-thickness recesses within the accelerometer of FIG. **6**.

FIG. **9***ad* illustrates an embodiment of metal electrodes including cavities within the accelerometer of FIG. **6**.

FIG. **9***b* is a top view of a top mass half of the mass wafer pair of FIG. **9***a*FIG. **9***c* is a bottom view of the top mass half of FIG. **9***b*.

FIG. **9***d* is a bottom perspective view of the top mass half of FIG. **9***c*.

FIG. **9***e* is a bottom view of a bottom mass half of the mass wafer pair of FIG. **9***a*

FIG. **9***f* is a top view of the bottom mass half of FIG. **9***e*.

FIG. **9***g* is a top perspective view of the bottom mass half of FIG. **9***e*.

FIG. **10** is a flowchart of a fabrication process for the accelerometer of FIG. **4**.

FIG. **11***a* illustrates an embodiment of the two starting cap wafers of FIG. **10**.

FIG. **11***b* illustrates a cross-sectional view of a top cap wafer and a bottom cap wafer resulting from the cap wafer process of FIG. **10**.

FIG. **11***c* illustrates an embodiment of the starting mass wafers of FIG. **10**.

FIG. **11***d* illustrates a top view of an embodiment of a photomask outline including corner compensation structures applied to the starting mass wafers during the mass wafer process of FIG. **10**.

FIG. **11***e* illustrates a bottom view of the top starting mass wafer after an etching phase of the mass wafer process of FIG. **10**.

FIG. **11***f* illustrates a cross-sectional view of the top starting mass wafer and the bottom starting mass wafer after an etching phase of the mass wafer process of FIG. **10**.

FIG. **11***g* illustrates a cross-sectional view of a bonded mass wafer pair during the mass wafer process of FIG. **10**.

FIG. **11***h* illustrates a cross-sectional view of the bonded mass wafer pair of FIG. **11***g* including electrodes and bond rings.

FIG. **11***ha* illustrates an embodiment of a metal electrode including a patterned surface on an upper surface of the mass wafer pair of FIG. **9***a*.

FIG. **11***hb* illustrates an embodiment of a metal electrode including a patterned surface on a lower surface of the mass wafer pair of FIG. **9***a*.

FIG. **11***hc* illustrates an embodiment of a patterned surface on the mass wafer pair of FIG. **9***a*.

FIG. **11***hd* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***he* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***hf* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***hg* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***hh* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***hi* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***hj* illustrates an alternative embodiment of the patterned surface of FIG. **11***hc*.

FIG. **11***i* illustrates a cross-sectional view of the bonded mass wafer pair of FIG. **11***h* including springs.

FIG. **11***j* illustrates a cross-sectional view of an accelerometer after the bonding process of FIG. **10**.

FIG. **12***a* is a side view illustrating the relative positioning of dicing cuts on the accelerometer die of FIG. **6**.

FIG. **12***b* is an illustration of the accelerometer die after the dicing cuts of FIG. **12***a* have been completed.

FIG. **12***c* is an illustration of an embodiment of the accelerometer of FIG. **12***b* after an integrated passage has been exposed.

FIG. **13** is an illustration of an embodiment of the accelerometer of FIG. **12***c* packaged within a housing.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENTS

Referring initially to FIG. **1**, a preferred embodiment of a system **100** designed to record data measurements is illustrated. The system **100** preferably includes one or more sensors **105**, a controller **110**, and cabling **115**.

Within the system **100**, the sensors **105** are used to detect data measurements. In a preferred embodiment, the system **100** is used in seismic applications to record seismic data measurements. The sensors **105** may be any number of conventional commercially available sensors, such as, for example, a geophone, a hydrophone, or an accelerometer. In a preferred embodiment, each of the sensors **105** is an accelerometer.

The controller **110** is used to monitor and control the sensors **105**. The controller **110** is preferably coupled to the sensors **105** by the cabling **115**. The controller **110** may be any number of conventional commercially available controllers suitable for controlling the sensors **105**, such as, for example, a seismic data acquisition device, a PID controller, or a microcontroller. In a preferred embodiment, the controller **110** is a seismic data acquisition device.

The cabling **115** couples the sensors **105** and the controller **110**. The cabling **115** may be any cabling suitable for transmitting information between the sensors **105** and controller **110**, such as, for example, wire or fiber optics. In a preferred embodiment, the cabling **115** is a wire.

Referring to FIG. **2**, a preferred embodiment of the alignment of the sensors **105** and the cabling **115** within the system **100** is illustrated. The sensors **105** and the cabling **115** may be aligned linearly or non-linearly. In a preferred embodiment, the sensors **105** and cabling **115** are aligned linearly.

The sensors **105** may include any number of conventional commercially available components suitable for creating a sensor. Referring to FIGS. **3***a* and **3***b*, in a preferred embodiment, the sensors **105** include one or more accelerometers **305**, and a housing **315** having a cavity **320**. In another preferred embodiment, the sensors **105** further include a measurement device **310**. In a preferred embodiment, the sensors **105** each include three accelerometers **305**. The accelerometers **305** are preferably placed in the cavity **320** within the housing **315** of the sensor **105**. The accelerometers **305** may be coupled to the measurement device **310**, or may operate independently within the sensor **105**. In a preferred embodiment, the accelerometers **305** operate independently within the sensor **105**. The measurement device **310** may be any number of conventional commercially available devices suitable for coupling with the accelerometer **305** to create a sensor **105**, such as, for example, a geophone or a hydrophone. In a preferred embodiment, the measurement device **310** is a hydrophone.

The accelerometer **305** may include any number of components suitable for forming an accelerometer. Referring to FIGS. **4**, **5**, and **6**, in a preferred embodiment, the accelerometer **305** includes a top cap wafer **405**, a top measurement mass half **410**, a bottom measurement mass half **415**, and a bottom cap wafer **420**. The operation of the accelerometer **305** is preferably provided substantially as described in U.S. Pat. No. 5,852,242, the disclosure of which is incorporated herein by reference.

The top cap wafer **405** may include any number of conventional commercially available components suitable for forming a top cap wafer. In a preferred embodiment, as illustrated in FIGS. **7***a*, **7***b*, **7***c*, **7***d*, **7***e*, **7***f*, **7***g*, **7***h*, **7***i*, **7***j*, **7***k*, and **7***l*, the top cap wafer **405** includes a top cap wafer body **406**, an upper surface **407**, a bottom surface **408**, a top capacitor electrode **705**, a top bond ring **707**, a top bond oxide ring **710**, a top cap parasitic groove **715**, top cap overshock bumpers **720**, a top cap press frame recess **725**, a top cap balanced metal pattern **730**, and a top cap contact pad **735**.

The top cap wafer body **406** may be fabricated from any number of conventional commercially available materials suitable for creating a cap wafer body, such as, for example, glass, quartz, ceramic, or silicon. In a preferred embodiment, the top cap wafer body **406** is made of silicon.

The top capacitor electrode **705** is preferably used for the time-based multiplexing of electrical signals from an external circuit, the operation of which is substantially as described in U.S. patent application Ser. No. 09/936,630, filed on Sep. 14, 2001, the disclosure of which is incorporated herein by reference. The top capacitor electrode **705** is preferably located on the bottom surface **408** of the top cap wafer body **406**, within an area circumscribed by the top cap parasitic groove **715**. In a preferred embodiment, as illustrated in FIG. **7***c*, the top capacitor electrode **705** includes slots **706** into which the top cap overshock bumpers **720** are fabricated. The top capacitor electrode **705** may be fabricated from any number of conductive materials suitable for creating an electrode, such as, for example, metals, silicides, or doped semiconductors. In a preferred embodiment, the top capacitor electrode **705** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide.

The top bond ring **707** and the top bond oxide ring **710** preferably bond the top cap wafer **405** to the top measurement mass half **410** and help establish a narrow gap between the top capacitor electrode **705** and an electrode located on an upper surface of the top measurement mass half **410**. The top bond oxide ring **710** preferably provides electrical isolation between the top cap wafer **405** and the top measurement mass half **410**. The top bond ring **707** and the top bond oxide ring **710** are preferably located on the bottom surface **408** of the top cap wafer body **406**. The top bond ring **707** may be fabricated from any number of materials suitable for making a bond ring, such as, for example, gold, silver, or aluminum. In a preferred embodiment, the top bond ring **707** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The bond ring **707** may have any dimensions suitable for use within the accelerometer **305**. In a preferred embodiment, as illustrated in FIG. **7***a*, the bond ring **707** has a width d**1** that is smaller than the width of the top cap press frame recess **725**. In a preferred embodiment, the bond ring **707** extends below the top cap overshock bumpers **720** by a distance d2. The top bond oxide ring **710** may be fabricated from any number of conventional commercially available materials suitable for making a bond oxide ring, such as, for example, silicon dioxide or dielectrics. In a preferred embodiment, the top bond oxide ring **710** is fabricated from silicon dioxide.

The top cap parasitic groove **715** preferably minimizes the coupling of electrostatic feedback of an external close-loop circuit to springs included in the top measurement mass half **410**. The top cap parasitic groove **715** preferably is a groove within the bottom surface **408** of the top cap wafer body **406**. The top cap parasitic groove **715** preferably circumscribes the top capacitor electrode **705** and is surrounded by the top bond oxide ring **710**. The top cap parasitic groove **715** may include any dimensions suitable for creating an adequate parasitic groove. In a preferred embodiment, the top cap parasitic groove **715** measures greater than about 5 μm in depth and has a width wider than the width of the springs within the top measurement mass half **410**.

The top cap overshock bumpers **720** preferably provide out-of-plane shock protection to the top measurement mass half **410**. The top cap overshock bumpers **720** are preferably located on the bottom surface **408** of the top cap wafer body **406**, and are exposed through the cutouts **706** in the top capacitor electrode **705**. The top cap overshock bumpers **720** may be fabricated from any number of conventional commercially available materials suitable for creating overshock bumpers, such as, for example, silicon dioxide or dielectrics. In a preferred embodiment, the top cap overshock bumpers **720** are made of silicon dioxide. In a preferred embodiment, as illustrated in FIG. **7***a*, the top cap overshock bumpers **720** have a width w**1**. The top cap wafer **405** may include any number of top cap overshock bumpers **720**. The design and layout of the top cap overshock bumpers **720** may be affected by any number of factors. In a preferred embodiment, the design and layout of the top cap overshock bumpers **720** balances the need for shock protection with the need for minimal stiction between the top cap overshock bumpers **720** and a metal electrode pattern **910** located on the top measurement mass half **410**. Stiction occurs when the top cap overshock bumpers **720** stick to the metal electrode pattern **910** on the top measurement mass half **410** during the operation of the accelerometer **305**. The stiction between the top cap overshock bumpers **720** and the metal electrode pattern located on the top measurement mass half **410** may be caused by any number of sources, such as, for example, imprinting of the top cap overshock bumpers **720** onto the metal electrode pattern **910** located on the top measurement mass half **410**, Van Der Waals forces, electrostatic forces, surface residues resulting from the fabrication of the accelerometer **305**, or package-induced stresses. In a preferred embodiment, as illustrated in FIG. **7***d*, the top cap wafer **405** includes four bumpers. In an alternative embodiment, as illustrated in FIG. **7***e*, the top cap wafer **405** includes five top cap overshock bumpers **720**. In an alternative embodiment, as illustrated in FIG. **7***f*, the top cap wafer **405** includes eight geometrically arranged top cap overshock bumpers **720**. In an alternative embodiment, as illustrated in FIG. **7***g*, the top cap wafer **405** includes nine geometrically arranged top cap overshock bumpers **720**. In an alternative embodiment, as illustrated in FIG. **7***h*, the top cap wafer **405** includes nine top cap overshock bumpers **720** arranged in three linear, parallel rows with each row having three bumpers **720**. In an alternative embodiment, as illustrated in FIG. **7***i*, the top cap wafer **405** includes thirteen geometrically arranged top cap overshock bumpers **720**. In an alternative embodiment, as illustrated in FIG. **7***j*, the top cap wafer **405** includes forty nine top cap overshock bumpers **720**. In an alternative embodiment, as illustrated in FIGS. **7***k* and **7***l*, the top cap wafer **405** includes a plurality of geometrically arranged top cap overshock bumpers **720** in the shape of circles and ridges.

The top cap press frame recess **725** is preferably located on the upper surface **407** of the top cap wafer body **406** between the top cap balanced metal pattern **730** and the top cap contact pad **735**. The top cap press frame recess **725** preferably ensures that bond forces applied during a bonding process are localized to the top bond oxide ring **710** region. By localizing bond forces to the top bond oxide ring **710** region rather than to the region of the narrow gap between the top capacitor electrode **705** and the electrode located on an upper surface of the top measurement mass half **410**, the narrow gap between the electrodes is maintained. The top cap press frame recess **725** may be formed using any number of processing steps suitable for forming a press frame recess such as, for example, silicon etching. In a preferred embodiment, the top cap press frame recess **725** is etched into the upper surface **407** of the top cap wafer body **406**. The top cap press frame recess **725** may include any dimensions suitable for creating a press frame recess. In a preferred embodiment, the top cap press frame recess **725** measures greater than about 20 μm in depth, and has a width wider than the width d**1** of the bond ring **707**.

The top cap contact pad **735** is preferably located on the upper surface **407** of the top cap wafer body **406**. The top cap contact pad **735** is preferably available for wire bonding. The top cap contact pad **735** may include any number of conventional commercially available materials suitable for creating a contact pad such as, for example, gold, aluminum, or silver. In a preferred embodiment, the top cap contact pad **735** is made of gold. In another preferred embodiment, the top cap contact pad **735** is made of a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide.

The top cap balanced metal pattern **730** is used to minimize bowing of the top cap wafer body **406**. Bowing of the top cap wafer body **406** is undesirable because it has an adverse effect on the performance of the accelerometer **305**.

Bowing of the top cap wafer body **406** typically results from thermal coefficient of expansion (TCE) differences between the material of the top cap wafer body **406** and the metal of the top capacitor electrode **705**. In a preferred embodiment, the material of the top cap wafer body **406** is silicon. In a preferred embodiment, the top cap balanced metal pattern **730** is approximately identical in pattern and thickness to the top capacitor electrode **705** and is placed within the top cap press frame recess **725**, substantially opposite the top capacitor electrode **705**. In a preferred embodiment, the top cap balanced metal pattern **730** includes cutouts **731** to offset the cutouts **705** in the top capacitor electrode **705**. This alignment preferably creates a balanced metal/silicon/metal sandwich that helps minimize the TCE mismatch effects on accelerometer **305** performance.

The bottom cap wafer **420** may include any number of conventional commercially available components suitable for forming a bottom cap wafer. In a preferred embodiment, as illustrated in FIGS. **8***a*, **8***b*, and **8***c*, the bottom cap wafer **420** includes a bottom cap wafer body **421**, an upper surface **423**, a bottom surface **422**, a bottom capacitor electrode **805**, a bottom bond ring **807**, a bottom bond oxide ring **810**, a bottom cap parasitic groove **815**, bottom cap overshock bumpers **820**, a bottom cap press frame recess **825**, a bottom cap balanced metal pattern **830**, a bottom cap contact pad **835**, and an extended cap solder attach (ECSA) metal bond pad **840**.

The bottom cap wafer body **421** may be fabricated from any number of conventional commercially available materials suitable for creating a cap wafer body such as, for example, glass, quartz, ceramic, or silicon. In a preferred embodiment, the bottom cap wafer body **421** is made of silicon.

The bottom capacitor electrode **805** is preferably used for the time-based multiplexing of electrical signals from an external circuit, the operation of which is substantially as described in U.S. patent application Ser. No. 09/936,630, filed on Sep. 14, 2001, the disclosure of which is incorporated herein by reference. The bottom capacitor electrode **805** is preferably located on the upper surface **423** of the bottom cap wafer body **421**, within an area circumscribed by the bottom cap parasitic groove **815**. In a preferred embodiment, as illustrated in FIG. **8***c*, the bottom capacitor electrode **805** includes cutouts **806** into which the bottom cap overshock bumpers **820** are fabricated. The bottom capacitor electrode **805** may be fabricated using any number of conductive materials suitable for creating an electrode such as, for example, metals, silicides, or doped semiconductors. In a preferred embodiment, the bottom capacitor electrode **805** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide.

The bottom bond ring **807** and the bottom bond oxide ring **810** preferably bond the bottom cap wafer **420** to the bottom measurement mass half **415** and help establish a narrow gap between the bottom capacitor electrode **805** and an electrode located on a lower surface of the bottom measurement mass half **415**. The bottom bond oxide ring **810** preferably provides electrical isolation between the bottom cap wafer **420** and the bottom measurement mass half **415**. The bottom bond ring **807** and the bottom bond oxide ring **810** are preferably located on the upper surface **423** of the bottom cap wafer body **421**. The bottom bond ring **807** may be fabricated from any number of materials suitable for making a bond ring such as, for example, aluminum, silver, or gold. In a preferred embodiment, the bottom bond ring **807** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. In a preferred embodiment, the bond ring **807** has a width d**4** that is smaller than the width of the bottom cap press frame recess **825**. In a preferred embodiment, the bond ring **807** extends beyond the bottom cap overshock bumpers **820** by a distance d**3**. The bottom bond oxide ring **810** may include any number of conventional commercially available materials suitable for making a bond oxide ring such as, for example, dielectrics. In a preferred embodiment, the bottom bond oxide ring **810** is fabricated from silicon dioxide.

The bottom cap parasitic groove **815** preferably minimizes the coupling of electrostatic feedback of an external close-loop circuit to springs included in the bottom measurement mass half **415**. The bottom cap parasitic groove **815** preferably is a groove within the upper surface **423** of the bottom cap wafer body **421**. The bottom cap parasitic groove **815** preferably circumscribes the bottom capacitor electrode **805**, and is surrounded by the bottom bond oxide ring **810**. The bottom cap parasitic groove **815** may include any dimensions suitable for creating an adequate parasitic groove. In a preferred embodiment, the bottom cap parasitic groove **815** measures greater than about 5 μm in depth and has a width wider than the width of the springs within the bottom measurement mass half **415**.

The bottom cap overshock bumpers **820** preferably provide out-of-plane shock protection to the bottom measurement mass half **415**. The bottom cap overshock bumpers **820** are preferably located on the upper surface **423** of the bottom cap wafer body **421**, and are exposed through the cutouts **806** in the bottom capacitor electrode **805**. The bottom cap overshock bumpers **820** may be fabricated from any number of conventional commercially available materials suitable for creating overshock bumpers, such as, for example, dielectrics or silicon dioxide. In a preferred embodiment, the bottom cap overshock bumpers **820** are made of silicon dioxide. In a preferred embodiment, the bottom cap overshock bumpers **820** have a width w**2**. The bottom cap wafer **420** may include any number of bottom cap overshock bumpers **820**. The design and layout of the bottom cap overshock bumpers **820** may be affected by any number of factors. In a preferred embodiment, the design and layout of the bottom cap overshock bumpers **820** balances the need for good shock protection with the need for minimal stiction between the bottom cap overshock bumpers **820** and a metal electrode pattern **915** located on the bottom measurement mass half **415**. Stiction occurs when the bottom cap overshock bumpers **820** stick to the metal electrode pattern **915** on the bottom measurement mass half **415** during the operation of the accelerometer **305**. The stiction between the bottom cap overshock bumpers **820** and the metal electrode pattern located on the bottom measurement mass half **415** may be caused by any number of sources, such as, for example, imprinting of the bottom cap overshock bumpers **820** onto the metal electrode pattern **915** located on the bottom measurement mass half **415**, Van Der Waals forces, electrostatic forces, surface residues resulting from the manufacture of the accelerometer **305**, or package-induced stresses. In a preferred embodiment, the number of bottom cap overshock bumpers **820** on the bottom cap wafer **420** equals the number of top cap overshock bumpers **720** on the top cap wafer **405**, the variations of which are illustrated in FIGS. **7***d*, **7***e*, **7***f*, **7***g*, **7***h*, **7***i*, **7***j*, **7***k*, and **7***l*.

The bottom cap press frame recess **825** is preferably located on the bottom surface **422** of the bottom cap wafer body **421** between the bottom cap balanced metal pattern **830** and the outer edge of the bottom surface **422**. The bottom cap press frame recess **825** ensures that bond forces applied during a bonding process are localized to the bottom bond oxide ring **810** region. By localizing bond forces to the bottom bond oxide ring **810** region rather than to the region of the narrow gap between the bottom capacitor electrode **805** and the electrode located on an bottom surface of the bottom measurement mass half **415**, the narrow gap between the electrodes is maintained. The bottom cap press frame recess **825** may formed using any number of processing steps suitable for forming a press frame recess such as, for example, silicon etching. In a preferred embodiment, the bottom cap press frame recess **825** is etched into the bottom surface **422** of the bottom cap wafer body **421**. The bottom cap press frame recess **825** may include any dimensions suitable for creating a press frame recess. In a preferred embodiment, the bottom cap press frame recess **825** measures greater than about 20 μm in height and has a width wider than the width d**4** of the bond ring **807**.

The bottom cap contact pad **835** is preferably located on the bottom surface **422** of the bottom cap wafer body **421**. The bottom cap contact pad **835** is preferably available for wafer probing. The bottom cap contact pad **835** may include any number of conventional commercially available materials suitable for creating a contact pad such as, for example, gold, aluminum, or silver. In a preferred embodiment, the bottom cap contact pad **835** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide.

The bottom cap balanced metal pattern **830** is used to minimize bowing of the bottom cap wafer body **421**. Bowing of the bottom cap wafer body **421** is undesirable because it has an adverse effect on the performance of the accelerometer **305**. Bowing of the bottom cap wafer body **421** typically results from thermal coefficient of expansion (TCE) differences between the material that makes up the bottom cap wafer body **421** and the metal of the bottom capacitor electrode **805**. In a preferred embodiment, the material that makes up the bottom cap wafer body **406** is silicon. In a preferred embodiment, the bottom cap balanced metal pattern **830** is approximately identical in pattern and thickness to the bottom capacitor electrode **805** and is placed within the bottom cap press frame recess **825**, substantially opposite the bottom capacitor electrode **805**. As illustrated in FIG. **8***b*, the bottom cap balanced metal pattern **830** preferably includes cutouts **831** designed to offset the cutouts **806** in the bottom capacitor electrode **805**. This alignment preferably creates a balanced metal/silicon/metal sandwich that helps minimize the TCE mismatch effects on accelerometer **305** performance.

The ECSA metal bond pad **840** is preferably available for conductive die-attach to an external package into which the accelerometer **305** is placed. The operation of the ECSA metal bond pad **840** is preferably as described in U.S. patent application Ser. No. 09/914,421, filed on Mar. 15, 2000, the disclosure of which is incorporated herein by reference.

The top measurement mass half **410** may include any number of conventional commercially available materials suitable for creating a measurement mass half. In a preferred embodiment, as illustrated in FIGS. **9***a*, **9***aa*, **9***ac*, **9***ad*, **9***b*, **9***c*, and **9***d*, the top measurement mass half **410** includes an upper surface **411**, a lower surface **412**, one or more springs **905**, a top measurement mass **906**, a housing **907**, the metal electrode pattern **910**, a bond ring **920**, and a top mass contact pad **930**. In another preferred embodiment, the top measurement mass half **410** further includes a groove **940**.

The springs **905** preferably couple the top measurement mass **906** to the housing **907** and provide a conductive path between the top measurement mass **906** and the housing **907**. The springs **905** may be fabricated from any number of conventional commercially available materials suitable for creating springs such as, for example, quartz, metals, or silicon. In a preferred embodiment, the springs **905** are made of silicon, and are micromachined out of the top measurement mass half **410** wafer. The springs **911** are preferably designed to maintain cross-axis rejection while providing lateral shock protection for the top measurement mass **906**. The springs **905** are preferably linear L-shaped springs, the design of which is described in U.S. Pat. Nos. 5,652,384 and 5,777,226, the disclosures of which are incorporated herein by reference.

The top measurement mass **906** is used to detect measurement data. The top measurement mass **906** may be used in any application in which its use is suitable. In a preferred embodiment, the top measurement mass **906** is used in seismic applications to detect acceleration. The top measurement mass **906** is preferably coupled to the housing **907** by the springs **905**. The top measurement mass **906** may be fabricated from any number of conventional commercially available materials suitable for creating a measurement mass such as, for example, metals, quartz, or silicon. In a preferred embodiment, the top measurement mass **906** is made of silicon, and is micromachined out of the top measurement mass half **410** wafer.

The housing **907** surrounds the top measurement mass **906** and is coupled to the top measurement mass **906** by the springs **905**. The housing **907** may be fabricated from any number of conventional commercially available materials suitable for creating a housing such as, for example, metals, quartz, or silicon. In a preferred embodiment, the housing **907** is fabricated from silicon, and is micromachined out of the top measurement mass half **410** wafer.

The metal electrode pattern **910** is used for the time-based multiplexing of electrical signals from an external circuit. In a preferred embodiment, the metal electrode pattern **910** includes a single electrode. In a preferred embodiment, the metal electrode pattern **910** is located on the upper surface **411** of the top measurement mass half **410**, on top of the top measurement mass **906**. The metal electrode pattern **910** may include any number of conventional commercially available materials suitable for creating an electrode pattern such as, for example, aluminum, silver, or gold. In a preferred embodiment, the metal electrode pattern **910** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The metal electrode pattern **910** may be of any size or shape suitable for forming an electrode pattern such as, for example, circular, square, or rectangular. The metal electrode pattern **910** is preferably substantially identical in size and shape to the top capacitor electrode **705**. In an alternative embodiment, the metal electrode pattern **910** is substantially equal in thickness to the bond ring **920**. In a preferred embodiment, the thicknesses of the metal electrode pattern **910** and the bond ring **920** are smaller than the thickness of the top bond ring **707**. The difference in thickness between the metal electrode pattern **910**, the bond ring **920**, and the top bond ring **707** preferably reduces stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910** during the operation of the accelerometer **305** by reducing the imprinting of the top cap overshock bumpers **720** on the metal electrode pattern **910**. In another preferred embodiment, as illustrated in FIG. **9***aa*, the metal electrode pattern **910** includes one or more patterns **960***a* designed to minimize stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910** during the operation of the accelerometer **305**. The patterns **960***a* may include any shape suitable for reducing stiction within the accelerometer **305**. The patterns **960***a* in the metal electrode pattern **910** preferably reduce stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910** by minimizing the surface area of the region of intimate contact between the top cap overshock bumpers **720** and the metal electrode pattern **910**. In another preferred embodiment, as illustrated in FIG. **9***ac*, the metal electrode pattern **910** includes one or more reduced-thickness recesses **970***a* at areas in which the top cap overshock bumpers **720** come in contact with the metal electrode pattern **910**. The reduced-thickness recesses **970***a* in the metal electrode pattern **910** are preferably designed to reduce stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910**. The reduced-thickness recesses **970***a* may be formed using any suitable method for forming reduced-thickness recesses in the metal electrode pattern **910**. In a preferred embodiment, the reduced-thickness recesses **970***a* are formed by removing the gold layer from the metal electrode pattern **910** to expose the underlying titanium layer. The reduced-thickness recesses **970***a* may have any shape suitable for reducing stiction within the accelerometer **305**. In a preferred embodiment, the reduced-thickness recesses **970***a* are wider than the width w**1** of the top cap overshock bumpers **720**, and are located on the metal electrode pattern **910** at areas in which the top cap overshock bumpers **720** come in contact with the metal electrode pattern **910**. The reduced-thickness recesses **970***a* in the metal electrode pattern **910** preferably reduce stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910** by reducing the amount of imprinting in the metal electrode pattern **910** that occurs when the top cap overshock bumpers **720** come in contact with the metal electrode pattern **910**. In another preferred embodiment, as illustrated in FIG. **9***ad*, the metal electrode pattern **910** includes one or more cavities **980***a* The cavities **980***a* in the metal electrode pattern **910** are preferably designed to eliminate stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910**. The cavities **980***a* may be formed using any suitable method for forming cavities in the metal electrode pattern **910**. In a preferred embodiment, the cavities **980***a* are formed by selectively removing the gold layer and the titanium layer from the metal electrode pattern **910** to expose the underlying top measurement mass half **410**.

The cavities **980***a* may have any shape suitable for reducing stiction within the accelerometer **305**. In a preferred embodiment, the cavities **980***a* are wider than the width w**1** of the top cap overshock bumpers **720**, and are located on the metal electrode pattern **910** at areas in which the top cap overshock bumpers **720** come in contact with the metal electrode pattern **910**. The cavities **980***a* in the metal electrode pattern **910** preferably reduce stiction between the top cap overshock bumpers **720** and the metal electrode pattern **910** by eliminating imprinting in the metal electrode pattern **910** that occurs when the top cap overshock bumpers **720** come in contact with the metal electrode pattern **910**. The operation of the metal electrode pattern **910** is substantially as that described in U.S. patent application Ser. No. 09/936,630, filed on Sep. 14, 2001, the disclosure of which is incorporated herein by reference.

The bond ring **920** facilitates bonding of the top measurement mass half **410** to the top cap wafer **405**. The bond ring **920** may include any number of conventional commercially available materials suitable for creating a bond ring such as, for example, gold, aluminum, or silver. In a preferred embodiment, the bond ring **920** is fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The bond ring **920** is preferably located on the upper surface **411** of the top measurement mass half **410**, adjacent to the inner edge of the housing **907**.

The top mass contact pad **930** is preferably used to make electrical contact to the top measurement mass half **410**. The top mass contact pad **930** may be located anywhere on the upper surface **411** of the housing **907**. In a preferred embodiment, the top mass contact pad **930** is located on the outer edge of the upper surface **411** of the housing **907**, away from the metal electrode pattern **910**. The top mass contact pad **930** may be fabricated from any materials suitable for creating a contact pad such as, for example, silver, aluminum, or gold. In a preferred embodiment, the top mass contact pad **930** is made of a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The top mass contact pad **930** may include any dimensions suitable for creating a contact pad. In a preferred embodiment, the top mass contact pad **930** is sufficiently large for enabling a conventional wire bond.

The groove **940** is preferably located on the lower surface **412** of the housing **907** and extends from the outer edge of the housing **907** to the inner edge of the housing **907**. The groove **940** preferably forms a passage **950** when the top measurement mass half **410** is bonded to the bottom measurement mass half **415**. The passage **950** is preferably used to remove air from a cavity within the accelerometer **305**, creating a vacuum or a low-pressure environment within the accelerometer **305** when the accelerometer **305** is sealed within a vacuum package. The groove **940** may be shaped in any way suitable for creating a passage for venting air. In a preferred embodiment, the groove **940** is V-shaped. In a preferred embodiment, the groove **940** is designed to allow for the fluidic flow of air from within the accelerometer **305** during a vacuum pump-down. The top measurement mass half **410** may include any number of grooves **940**. In a preferred embodiment, the top measurement mass half **410** includes two grooves **940**. In an alternative embodiment, the top measurement mass half **410** includes one groove **940**. In an alternative embodiment, the top measurement mass half **410** includes a plurality of grooves **940**. In an alternative embodiment, the top measurement mass half **410** includes no groove **940**. The shape of the groove **940** may be affected by any number of factors. In a preferred embodiment, the groove **940** is designed to achieve an optimal pumpdown time for air passing through the passage **950**. The conductance of air through the passage **950** is preferably given by:

$$C = \frac{8}{3\sqrt{\pi}}\left(\frac{2kT}{m}\right)^{1/2}\left(\frac{A^2}{BL}\right), \tag{1}$$

where:

C=the conductance of the passage **950**,

k=Boltzman's constant,

T=absolute temperature,

m=mass of gas atom,

A=cross-sectional area of the passage **950**,

B=periphery of the cross-sectional area of the passage **950**, and

L=the length of the passage **950**.

The dimensions of the passage **950**, such as the length L, the cross-sectional area A, and the periphery B, are preferably designed to optimize the conductance of air through the passage **950**. In a preferred embodiment, the optimal conductance C through the passage **950** produces an optimal pumpdown time for removing air from within the accelerometer **305**. The pumpdown time is the amount of time it takes to remove enough air from within the accelerometer

305 to achieve the desired pressure within the accelerometer 305. The pumpdown time is preferably given by:

$$t \approx \left(\frac{V}{S}\right)[1 + S/C]\ln\left(\frac{Pi - Pu}{P - Pu}\right), \tag{2}$$

where:

t=pumpdown time,

V=volume of the internal cavities within the accelerometer 305,

S=speed of a vacuum pump used to remove air from the accelerometer 305,

C=conductance of the passage 950 from equation (1),

Pi=initial pressure within the accelerometer 305 (typically 1 atm),

P=desired pressure within the accelerometer 305,

Pu=(1+S/C)*Po, and

Po=lowest pressure of the pump.

The bottom measurement mass half 415 may be fabricated from any number of conventional commercially available materials suitable for creating a measurement half. In a preferred embodiment, as illustrated in FIGS. 9*a*, 9*ab*, 9*ac*, 9*ad*, 9*e*, 9*f*, and 9*g*, the bottom measurement mass half 415 includes an upper surface 417, a lower surface 416, one or more springs 911, a bottom measurement mass 912, a housing 913, the metal electrode pattern 915, a bond ring 925, a bottom mass contact pad 935, and a groove 945.

The springs 911 preferably couple the bottom measurement mass 912 to the housing 913 and provide a conductive path between the bottom measurement mass 912 and the housing 913. The springs 911 may be fabricated from any number of conventional commercially available materials suitable for creating springs such as, for example, metals, quartz, polysilicon, or silicon. In a preferred embodiment, the springs 911 are made of silicon, and are micromachined out of the bottom measurement mass half 415 wafer. The springs 911 are preferably designed to maintain cross-axis rejection while providing lateral shock protection for the bottom measurement mass 912. The springs 911 are preferably linear L-shaped springs, the design of which is described in U.S. Pat. Nos. 5,652,384 and 5,777,226, the disclosures of which are incorporated herein by reference.

The bottom measurement mass 912 is used to detect measurement data. The bottom measurement mass 912 may be used in any application in which its use is suitable. In a preferred embodiment, the bottom measurement mass 912 is used in seismic applications to detect acceleration forces. The bottom measurement mass 912 is preferably coupled to the housing 913 by the springs 911. The bottom measurement mass 912 may be fabricated from any material suitable for creating a measurement mass such as, for example, silicon or quartz. In a preferred embodiment, the bottom measurement mass 912 is made of silicon, and is micromachined out of the bottom measurement mass half 415 wafer.

The housing 913 surrounds the bottom measurement mass 912 and is coupled to the bottom measurement mass 912 by the springs 911. The housing 913 may be fabricated from any material suitable for creating a housing such as, for example, quartz or silicon. In a preferred embodiment, the housing 913 is fabricated from silicon, and is micromachined out of the bottom measurement mass half 415 wafer.

The metal electrode pattern 915 is used for the time-based multiplexing of electrical signals from an external circuit. In a preferred embodiment, the metal electrode pattern 915 includes a single electrode. In a preferred embodiment, the metal electrode pattern 915 is located on the lower surface 416 of the bottom measurement mass half 415, on a surface of the bottom measurement mass 912. The metal electrode pattern 915 may include any number of conventional commercially available materials suitable for creating an electrode pattern such as, for example, silver, aluminum, or gold. In a preferred embodiment, the metal electrode pattern 915 is made of a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The metal electrode pattern 915 may be of any size or shape suitable for forming an electrode pattern such as, for example, circular, square, or rectangular. The metal electrode pattern 915 is preferably identical in size and shape to the bottom capacitor electrode 805. In a preferred embodiment, the metal electrode pattern 915 is substantially equal in thickness to the bond ring 925. In a preferred embodiment, the thicknesses of the metal electrode pattern 915 and the bond ring 925 are smaller than the thickness of the bottom bond ring 807. The differences in thickness between the metal electrode pattern 915, the bond ring 925, and the bottom bond ring 807 preferably reduces stiction between the bottom cap overshock bumpers 820 and the metal electrode pattern 915 during the operation of the accelerometer 305 by reducing the imprinting of the bottom cap overshock bumpers 820 on the metal electrode pattern 915. In another preferred embodiment, as illustrated in FIG. 9*ab*, the metal electrode pattern 915 includes one or more patterns 960*b* designed to minimize stiction between the bottom cap overshock bumpers 820 and the metal electrode pattern 915 during the operation of the accelerometer 305. The patterns 960*b* in the metal electrode pattern 915 preferably reduce stiction between the bottom cap overshock bumpers 820 and the metal electrode pattern 915 by minimizing the surface area of the region of intimate contact between the bottom cap overshock bumpers 820 and the metal electrode pattern 915. In another preferred embodiment, as illustrated in FIG. 9*ac*, the metal electrode pattern 915 includes one or more reduced-thickness recesses 970*b* at areas in which the bottom cap overshock bumpers 820 come in contact with the metal electrode pattern 915. The reduced-thickness recesses 970*b* in the metal electrode pattern 915 are preferably designed to reduce stiction between the bottom cap overshock bumpers 820 and the metal electrode pattern 915. The reduced-thickness recesses 970*b* may be formed using any suitable method for forming reduced-thickness recesses in the metal electrode pattern 915. In a preferred embodiment, the reduced-thickness recesses 970*b* are formed by removing the gold layer from the metal electrode pattern 915 to expose the underlying titanium layer. The reduced-thickness recesses 970*b* may have any shape suitable for reducing stiction within the accelerometer 305. In a preferred embodiment, the reduced-thickness recesses 970*b* are wider than the width w2 of the bottom cap overshock bumpers 820, and are located on the metal electrode pattern 915 at areas in which the bottom cap overshock bumpers 820 come in contact with the metal electrode pattern 915.

The reduced-thickness recesses 970*b* preferably reduce stiction between the bottom cap overshock bumpers 820 and the metal electrode pattern 915 by reducing the amount of imprinting in the metal electrode pattern 915 that occurs when the bottom cap overshock bumpers 820 come in contact with the metal electrode pattern 915. In another preferred embodiment, as illustrated in FIG. 9*ad*, the metal electrode pattern 915 includes one or more cavities 980*b*.

The cavities **980***b* in the metal electrode pattern **915** are preferably designed to eliminate stiction between the bottom cap overshock bumpers **820** and the metal electrode pattern **915**. The cavities **980***b* may be formed using any suitable method for forming cavities in the metal electrode pattern **915**. In a preferred embodiment, the cavities **980***b* are formed by selectively removing the gold layer and the titanium layer from the metal electrode pattern **915** to expose the underlying bottom measurement mass half **415**. The cavities **980***b* may have any shape suitable for reducing stiction within the accelerometer **305**. In a preferred embodiment, the cavities **980***b* are wider than the width w**2** of the bottom cap overshock bumpers **820**, and are located on the metal electrode pattern **915** at areas in which the bottom cap overshock bumpers **820** come in contact with the metal electrode pattern **915**. The cavities **980***b* preferably reduce stiction between the bottom cap overshock bumpers **820** and the metal electrode pattern **915** by eliminating imprinting in the metal electrode pattern **915** that occurs when the bottom cap overshock bumpers **820** come in contact with the metal electrode pattern **915**. The operation of the metal electrode pattern **915** is substantially as that described in U.S. patent application Ser. No. 09/936,630, filed on Sep. 14, 2001, the disclosure of which is incorporated herein by reference.

The bond ring **925** preferably facilitates bonding of the bottom measurement mass half **415** to the bottom cap wafer **420**. The bond ring **925** may include any number of conventional commercially available materials suitable for creating a bond ring such as, for example, gold, aluminum, or silver. In a preferred embodiment, the bond ring **925** is made of a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The bond ring **925** is preferably located on the lower surface **416** of the bottom measurement mass half **415**, adjacent to the inner edge of the housing **913**.

The bottom mass contact pad **935** is preferably used to create an electrical contact to the bottom measurement mass half **415**. The bottom mass contact pad **935** may be located anywhere on the lower surface **416** of the housing **913**. In a preferred embodiment, the bottom mass contact pad **935** is located on the outer edge of the lower surface **416** of the housing **913**, away from the metal electrode pattern **915**. The bottom mass contact pad **935** may include any number of conventional commercially available materials suitable for creating a contact pad such as, for example, aluminum, silver, or gold. In a preferred embodiment, the bottom mass contact pad **935** is made of a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The bottom mass contact pad **935** may include any dimensions suitable for a contact pad. In a preferred embodiment, the bottom mass contact pad **935** is sufficiently large for enabling conventional wire bonding.

The groove **945** forms a passage **950** when the bottom measurement mass half **415** is bonded to the top measurement mass half **410**. The passage **950** is preferably used to remove air from a cavity within the accelerometer **305**, creating a vacuum within the accelerometer **305** when the accelerometer **305** is sealed within a vacuum package. The groove **945** may be shaped in any way suitable for creating a passage for venting air. In a preferred embodiment, the groove **945** is V-shaped. In a preferred embodiment, the groove **945** is designed to allow for the fluidic flow of air from within the accelerometer **305** during a vacuum pump down. The shape of the groove **945** is preferably substantially identical to the shape of the groove **940**, as described above. The groove **945** is preferably located on the upper surface **417** of the housing **913** and extends from the outer edge of the housing **913** to the inner edge of the housing **913**. The bottom measurement mass half **415** may include any number of grooves **945**. In a preferred embodiment, the bottom measurement mass half **415** includes two grooves **945**. In an alternative embodiment, the bottom measurement mass half **415** includes one groove **945**. In an alternative embodiment, the bottom measurement mass half **415** includes a plurality of grooves **945**. In an alternative embodiment, the bottom measurement mass half **415** includes no groove **945**.

Referring to FIGS. **10**, **11***a*, **11***b*, **11***c*, **11***d*, **11***e*, **11***f*, **11***g*, **11***h*, **11***ha*, **11***hb*, **11***hc*, **11***hd*, **11***he*, **11***hf*, **11***hg*, **11***hh*, **11***hi*, **11***hj*, **11***i*, **11***j*, **12***a*, **12***b*, **12***c*, and **13**, a method **1000** of fabricating the accelerometer **305** will now be described. In a preferred embodiment, the method **1000** of fabricating the accelerometer **305** includes: acquiring two starting cap wafers in step **1005**, shaping the two starting wafers using a cap wafer process in step **1010**, acquiring two starting mass wafers in step **1020**, shaping the two starting mass wafers using a mass wafer process in step **1025**, bonding the wafers to form the accelerometer **305** using a bonding process in step **1035**, making dicing cuts on the accelerometer **305** in step **1040**, and packaging the accelerometer **305** in step **1045**.

As illustrated in FIG. **11***a*, in step **1005** the two starting cap wafers **1105***a* and **1105***b* are fabricated. In a preferred embodiment, the two starting cap wafers **1105***a* and **1105***b* are identically sized and shaped. The starting cap wafers **1105***a* and **1105***b* may be fabricated from any number of conventional commercially available materials. In a preferred embodiment, the starting cap wafers **1105***a* and **1105***b* are made of silicon.

As illustrated in FIG. **11***b*, in step **1010** the two starting cap wafers **1105***a*and **1105***b* undergo a cap wafer process. In a preferred embodiment, the cap wafer process transforms the starting cap wafers **1105***a* and **1105***b* into the top cap wafer **405** and the bottom cap wafer **420**, respectively. In an alternative embodiment, the cap wafer process includes a merged mask micro-machining process substantially as disclosed in one or more of the following: U.S. patent application Ser. No. 09/352,835, filed on Jul. 13, 1999, and U.S. patent application Ser. No. 09/352,025, filed on Jul. 13, 1999, the disclosures of which are incorporated herein by reference.

As illustrated in FIG. **11***c*, in step **1020** the two starting mass wafers **1120***a* and **1120***b* are fabricated. In a preferred embodiment, the two starting mass wafers **1120***a* and **1120***b* are identically sized and shaped. The starting mass wafers **1120***a* and **1120***b* may be fabricated from any number of conventional commercially available materials. In a preferred embodiment, the starting mass wafers **1120***a* and **1120***b* are made of silicon. In a preferred embodiment, each of the starting mass wafers **1120***a* and **1120***b* includes an etch-stop layer **1140***a* and **1140***b*, respectively. In a preferred embodiment, each of the starting mass wafers **1120***a* and **1120***b* includes an etch-masking layer **1150***a* and **1150***b*, respectively.

As illustrated in FIGS. **11***id*, **11***e*, **11***f*, **11***g*, **11***h*, **11***ha*, **11***hb*, **11***hc*, **11***hd*, **11***he*, **11***hf*, **11***hg*, **11***hh*, **11***hi*, **11***hj* and **11***i*, in step **1025** the two starting mass wafers **1120***a* and **1120***b* undergo a mass wafer process that transforms the two starting mass wafers **1120**a and **1120**b into the top measurement mass half **410** and the bottom measurement mass half **415**, respectively. In a preferred embodiment, the mass wafer process is substantially as that described in U.S. Pat. No. 5,484,073, the disclosure of which is incorporated herein by reference. In an alternative embodiment, the mass wafer process includes a merged mask micromachining process substantially as disclosed in U.S. patent application Ser. No. 09/352,835, filed on Jul. 13, 1999, and U.S. patent application Ser. No. 09/352,025, filed on Jul. 13, 1999, the disclosures of which are incorporated herein by reference.

As illustrated in FIG. **11**d, the mass wafer process of step **1025** begins by photolithigraphically patterning the etch-masking layer **1150**a to create an area of exposure **1160** on the etch-masking layer **1150**a. In a preferred embodiment, the etch-masking layer **1150**a is photolithigraphically patterned to create the area of exposure **1160** in the shape of the top measurement mass **906**, the housing **907**, and the grooves **940**. In a preferred embodiment, the photolithigraphically patterned area of exposure **1160** includes corner compensation structures X and Y.

In a preferred embodiment, as illustrated in FIG. **11**e, an etching process is performed to shape the starting mass wafer **1120**a into the top measurement mass half **410**. The etching process may include any number of conventional commercially available processes suitable for etching. In a preferred embodiment, the etching process begins by removing the etch-masking layer **1150**a from the starting mass wafer **1120** within the area of exposure **1160**. The etch-masking layer **1150**a may be removed using any suitable process for removing an etch-masking layer, such as, for example, plasma etching. In a preferred embodiment, the etch-masking layer **1150**a is removed from the starting mass wafer **1120**a within the area of exposure **1160** by using an etchant. In a preferred embodiment, removal of the etch-masking layer **1150**a exposes the material from which the starting mass wafer **1120**a is fabricated. In a preferred embodiment, the material from which the starting mass wafer **1120**a is fabricated is silicon. In a preferred embodiment, the corner compensation structures X prevent the etchant from attacking and corroding convex corners within the area of exposure **1160**. The corner structures Y preferably allow the grooves **940** to be simultaneously formed during the etching process used to define the measurement mass **906** and the housing **907**. In a preferred embodiment, the corner compensation structures Y reduce etchant-induced corner erosion at an intersection between the grooves **940** and the area of exposure **1160**.

In a preferred embodiment, a wet etching chemical is then applied to the exposed silicon on the starting mass wafer **1120**a. The wet etching chemical may be any number of conventional commercially available wet etching chemicals suitable for etching silicon. In a preferred embodiment, the wet etching chemical is potassium hydroxide (KOH). The KOH preferably controllably etches through the silicon and terminates at the etch-stop layer **1140**a of the starting mass wafer **1120**a. In a preferred embodiment, as illustrated in FIG. **11**f, the KOH etches the starting mass wafer **1120**a into the shape of the top measurement mass **406**, the housing **407**, and the groove **940**. In a preferred embodiment, the etch-stop layer **1140**a remains on the backside surface of the springs **905** after the wet chemical etching process has been completed. In an alternative embodiment, the etch-stop layer **1140**a is removed from the springs **905** during the wet chemical etching process.

Following the wet etching process, the remaining etch-masking layer **1150**a on the starting mass wafer **1120**a is removed from the starting mass wafer **1120**a using a standard wet etchant.

An identical etching process is preferably used on the second starting mass wafer **1120**b to shape the second starting mass wafer **1120**b into the bottom measurement mass half **415**.

In a preferred embodiment, as illustrated in FIG. **11**g, the top measurement mass half **410** and the bottom measurement mass half **415** are bonded together to form a mass wafer pair **1130**. The wafer bonding process may be any number of bonding processes suitable for bonding the top measurement mass half **410** and the bottom measurement mass half **415**. In a preferred embodiment, the wafer bonding process is a fusion bonding process. In a preferred embodiment, the groove **940** in the top measurement mass half **410** is aligned with the groove **945** in the bottom measurement mass half **415** during the wafer bonding process to form the passage **950**.

In a preferred embodiment, a metal layer **1142** is deposited onto the upper surface of the mass wafer pair **1150**, which corresponds to the upper surface **411** of the top measurement mass half **410**. Additionally, a metal layer **1143** is deposited onto the lower surface of the mass wafer pair **1130**, which corresponds to the lower surface **416** of the bottom measurement mass half **415**. The metal layers **1142** and **1143** may include any number of conventional commercially available materials suitable for creating a metal layer such as, for example, aluminum, silver, or gold. In a preferred embodiment, the metal layers **1142** and **1143** are fabricated from a combination of gold and titanium. In a preferred embodiment, the combination of gold and titanium includes a layer of gold located on top of a layer of titanium. The layer of titanium preferably improves the adhesion of the gold to silicon and silicon dioxide. The metal layers **1142** and **1143** are preferably patterned using an etch-masking layer. The etch-masking layer may be any etch-masking layer suitable for patterning metal layers. In a preferred embodiment, the etch-masking layer is photoresist. The metal layers **1142** and **1143** may be shaped into any pattern suitable for use within the accelerometer **305**. In a preferred embodiment, as illustrated in FIG. **11**h, the metal layer **1142** on the upper surface of the mass wafer pair **1130** is shaped to form the metal electrode pattern **910**, the bond ring **920**, and the top mass contact pad **930**. In a preferred embodiment, as illustrated in FIG. **11**h, the metal layer **1143** on the lower surface of the mass wafer pair **1130** is shaped to form the metal electrode pattern **915**, the bond ring **925**, and the bottom mass contact pad **935**.

In a preferred embodiment, as illustrated in FIG. **11**ha, the metal electrode pattern **910** includes a pattern **960**a designed to reduce stiction between the metal electrode pattern **910** and the top cap overshock bumpers **720** during the operation of the accelerometer **305**. In a preferred embodiment, as illustrated in FIG. **11**hb, the metal electrode pattern **915** includes a pattern **960**b designed to reduce stiction between the metal electrode pattern **915** and the bottom cap overshock bumpers **820** during the operation of the accelerometer **305**. The patterns **960**a and **960**b may be created on the metal electrode patterns **910** and **915** using any number of methods suitable for creating patterns on the metal electrode patterns **910** and **915**. In a preferred embodiment, as illustrated in FIG. **11**ha, the pattern **960**a is created by etching a pattern into the upper surface **411** of the top measurement mass half **410** to create a patterned surface **1165**a, and depositing the metal layer **1142** onto the patterned surface **1165**a. The metal layer **1142** preferably molds into the metal electrode **910** including the pattern **960**a. In a preferred embodiment, as illustrated in FIG. **11***hb*, the pattern **960***b* is created by etching a pattern into the lower surface **416** of the bottom measurement mass half **415** to create a patterned surface **1165***b*, and depositing the metal layer **1143** onto the patterned surface **1165***b*. The metal layer **1143** preferably molds into the metal electrode **915** including the pattern **960***b*. The patterned surface **1165***a* etched into the upper surface **411** of the top measurement mass half **410** and the patterned surface **1165***b* etched into the lower surface **416** of the bottom measurement mass half **415** may include any number of patterns suitable for reducing the stiction between the metal electrode patterns **910** and **915** and the overshock protection bumpers **720** and **820**, respectively. In a preferred embodiment, as illustrated in FIGS. **11***hc* and **11***hf*, the patterned surfaces **1165***a* and **1165***b* include a plurality of geometrically arranged squares. In another preferred embodiment, as illustrated in FIGS. **11***hd* and **11***hg*, the patterned surfaces **1165***a* and **1165***b* include a plurality of geometrically arranged circles. In another preferred embodiment, as illustrated in FIG. **11***he*, the patterned surfaces **1165***a* and **1165***b* include a series of concentric circles. In another preferred embodiment, as illustrated in FIG. **11***hh*, the patterned surfaces **1165***a* and **1165***b* include a series of geometrically arranged rectangles. In another preferred embodiment, as illustrated in FIGS. **11***hi* and **11***hj*, the patterned surfaces **1165***a* and **1165***b* include a series of geometrically arranged pie-shaped segments.,

In a preferred embodiment, as illustrated in FIG. **11***i*, the springs **905** are formed to couple the top measurement mass **906** to the housing **907**, and the springs **911** are formed to couple the bottom measurement mass **912** to the housing **913**. The springs **905** and **911** may be formed using any number of conventional commercially available methods suitable for creating spring members in the mass wafer pair **1130**. In a preferred embodiment, the springs **905** and **911** are formed using a DRIE plasma etching technique. In a preferred embodiment, the etching technique is substantially as that described in U.S. Pat. No. 5,484,073, the disclosure of which is incorporated herein by reference. The springs **905** and **911** are preferably linear L-shaped springs, the design of which is described in U.S. Pat. Nos. 5,652,384 and 5,777,226, the disclosures of which are incorporated herein by reference. The springs **905** and **911** are preferably designed to maintain cross-axis rejection while providing lateral shock protection for the top measurement mass **906** and the bottom measurement mass **911**, respectively. In a preferred embodiment, the etch-stop layers **1140***a* and **1140***b* remain on backside surfaces of the springs **905** and **911**, respectively, after the plasma etching process has been completed. The etch-stop layers **1140***a* and **1140***b* on the springs **905** and **911** preferably improve the uniformity of the thickness of the springs **905** and **911**. In addition, the etch-stop layers **1140***a* and **1140***b* on the springs **905** and **911** preferably improve the dimensional control of the springs **905** during the operation of the accelerometer **305**. In another preferred embodiment, the etch-stop layers **1140***a* and **1140***b* are removed from the springs **905** and **911**, respectively, during the plasma etching process.

As illustrated in FIG. **11***j*, in step **1035** the top cap wafer **405**, the bottom cap wafer **420**, and the mass wafer pair **1130** preferably undergo a bonding process to form the accelerometer **305**. The bonding process of step **1035** may be any number of bonding processes such as, for example, fusion bonding, thermocompression, eutectic bonding, anodic bonding, or glass frit bonding. In a preferred embodiment, the bonding process of step **1035** is a thermocompression bonding process.

During the bonding process of step **1035**, the top cap wafer **405** is bonded to the upper surface of the mass wafer pair **1130**, which corresponds to the upper surface **411** of the top measurement mass half **410**. In a preferred embodiment, the top bond ring **707** bonds with the bond ring **920**, coupling the top cap wafer **405** and the top measurement mass half **410**. The top bond ring **707** and the bond ring **920** are preferably bonded using the thermocompression bonding process.

The top bond oxide ring **710** preferably extends below the bottom surface **408** of the top cap wafer body **406**. As a result, the bonding process preferably creates a narrow capacitor electrode gap between the top capacitor electrode **705** and the metal electrode pattern **910**. During the bonding process, bond forces are preferably applied to the upper surface **407** of the top cap wafer **405**, away from the top cap press frame recess **725**. In a preferred embodiment, the top cap press frame recess **725** is positioned on the upper surface **407** of the top cap wafer **405** in a location that ensures that bond forces applied during the bonding process are localized to the bond ring regions and away from the narrow capacitor electrode gap region.

Also during the bonding process of step **1035**, the bottom cap wafer **420** is bonded to the lower surface of the mass wafer pair **1130**, which corresponds to the lower surface **416** of the bottom measurement mass half **415**. In a preferred embodiment, the bottom bond ring **807** bonds with the bond ring **925**, coupling the bottom cap wafer **420** and the bottom measurement mass half **415**. The bottom bond ring **807** and the bond ring **925** are preferably bonded using the thermocompression bonding process.

The bottom bond oxide ring **810** preferably extends above the upper surface **423** of the bottom cap wafer body **421**. As a result, the bonding process preferably creates a narrow capacitor electrode gap between the bottom capacitor electrode **805** and the metal electrode pattern **915**. During the bonding process, bond forces are preferably applied to the bottom surface **422** of the bottom cap wafer **420**, away from bottom cap press frame recess **825**. In a preferred embodiment, the bottom cap press frame recess **825** is positioned on the bottom surface **422** of the bottom cap wafer **420** in a location that ensures that bond forces applied during the bonding process are localized to the bond ring regions and away from the narrow capacitor electrode gap region.

As illustrated in FIGS. **12***a*, **12***b*, and **12***c*, in step **1040** the accelerometer **305** undergoes a dicing process. Dicing cuts **1205**, **1210**, **1215**, **1220** are preferably made at predetermined locations on the accelerometer **305**. The dicing cuts **1205**, **1210**, **1215**, **1220** serve a variety of purposes. In a preferred embodiment, the dicing cuts **1205**, **1215**, **1220** are made to separate the accelerometer **305** die from a wafer **1235**, expose electrical leads from the electrodes **910** and **915**, separate the electrical leads, and expose the passage **950**. In another preferred embodiment, the dicing cut **1210** is made in addition to the dicing cuts **1205**, **1215**, **1220** to separate the accelerometer **305** die from the wafer **1235**, expose electrical leads from the electrodes **910** and **915**, separate the electrical leads, and expose the passage **950**.

In a preferred embodiment, a cut **1205** is made on the top cap wafer **405**. The cut **1205** preferably extends vertically through the top cap wafer body **406**, resulting in the removal of a section of the top cap wafer body **406**. In a preferred embodiment, the cut **1205** exposes the top mass contact pad **930**. The cut **1205** may be performed using any number of conventional commercially available methods of performing a dicing cut such as, for example, using a diamond blade wafer saw. In a preferred embodiment, the cut **1205** is made by using a diamond blade wafer saw.

In a preferred embodiment, a cut **1215** is made extending vertically through the top cap wafer body **406** and into the housing **907** of the top measurement mass half **410**. The cut **1215** is preferably stopped within the housing **907** before the cut **1215** reaches the passage **950**. The cut **1215** may be stopped any distance before reaching the passage **950**. In a preferred embodiment, the cut **1215** is stopped more than about 2 mils from the passage **950**. The cut **1215** may be performed using any number of conventional commercially available methods of performing a dicing cut such as, for example, using a diamond blade wafer saw. In a preferred embodiment, the cut **1215** is made by using a diamond blade wafer saw.

In a preferred embodiment, a cut **1220** is made extending vertically through the bottom cap wafer body **421** and into the housing **913** of the bottom measurement mass half **415**. The cut **1220** is preferably stopped within the housing **913** before the cut **1220** reaches the passage **950**. The cut **1220** may be stopped any distance before reaching the passage **950**. In a preferred embodiment, the cut **1220** is stopped more than about **2** mils from the passage **950**. The cut **1220** may be performed using any number of conventional commercially available methods of performing a dicing cut such as, for example, using a diamond blade wafer saw. In a preferred embodiment, the cut **1215** is made by using a diamond blade wafer saw.

In an alternative preferred embodiment, a cut **1210** is made on the bottom cap wafer body **421**. The cut **1210** preferably extends vertically through the bottom cap wafer body **421**, resulting in the removal of a section of the bottom cap wafer body **421**. In a preferred embodiment, the cut **1210** exposes the bottom mass contact pad **935**. The cut **1210** may be performed using any number of conventional commercially available methods of performing a dicing cut such as, for example, using a diamond blade wafer saw. In a preferred embodiment, the cut **1210** is made by using a diamond blade wafer saw.

The cuts **1205**, **1210**, **1215**, **1220** may be performed individually, or the cuts **1205**, **1210**, **1215**, **1220** may be made in any combination to achieve the accelerometer **305** shape most suitable for a particular application. In a preferred embodiment, as illustrated in FIG. **12***b*, cuts **1205**, **1215**, and **1220** are performed on the accelerometer **305**. In an alternative embodiment, cut **1210** is performed on the accelerometer **305** in addition to the cuts **1205**, **1215**, and **1220**. Cut **1205** preferably exposes the top mass contact pad **930**. Cut **1210** preferably exposes the bottom mass contact pad **935**. Cuts **1215**, **1220** preferably create a scribe lane **1230** surrounding the passage **950**. The scribe lane **1230** is preferably attached to another die **1235**.

During the dicing process, the scribe lane **1230** may remain attached to the accelerometer **305** and die **1235** to keep the accelerometer **305** hermetically sealed, or the scribe lane **1230** may be snapped to expose the passage **950** and separate the accelerometer **305** from the die **1235**. In a preferred embodiment, as illustrated in FIG. **12***c*, the scribe lane **1230** is removed to expose the passage **950** and separate the accelerometer **305** from the die **1235**. The exposed passage **950** is preferably used as a channel for removing air from within the accelerometer **305** to create a vacuum within the accelerometer **305** during packaging.

As illustrated in FIG. **13**, in step **1045** the accelerometer **305** is packaged within a package **1305**. The package **1305** may include any number of packages suitable for storing the accelerometer **305**. In a preferred embodiment, the package **1305** is a housing. In another preferred embodiment, the package **1305** is a substrate.

The housing **1305** may be any number of housings suitable for storing the accelerometer **305**. In a preferred embodiment, the housing **1305** includes a body **1310** and a lid **1315**. The housing **1305** is preferably a conventional multi-layered ceramic package.

The accelerometer **305** is preferably placed within the body **1310** of the housing **1305**. The accelerometer **305** may be placed within the housing **1305** using any number of methods suitable for securing the accelerometer **305** within the housing **1305**. In a preferred embodiment, the accelerometer **305** is placed within the housing **1305** using a solder-die attachment process substantially as disclosed in U.S. patent application Ser. No. 09/914,421, filed on Mar. 15, 2000, the disclosure of which is incorporated herein by reference.

The lid **1315** is then preferably fastened to the body **1310** to seal the accelerometer **305** within the housing **1305**. In a preferred embodiment, a vacuum process is used to remove air from the housing prior to fastening the lid **1315** to the body **1310**, creating a vacuum or a low-pressure environment within the housing **1305**. When the passage **950** is exposed, air is removed from within the accelerometer **305** during the vacuum process, creating a vacuum within the accelerometer **305** in the housing **1305**.

In another preferred embodiment, the bonding process of step **1035** is performed in a vacuum environment, creating a vacuum within the cavity in the accelerometer **305** during the bonding process. In this embodiment, the passage **950** is preferably removed from the design of the accelerometer **305**. The vacuum-sealed accelerometer **305** is then preferably placed in the housing **1305**, and the housing is sealed by fastening the lid **1315** to the body **1310**.

Although illustrative embodiments of the invention have been shown and described, a wide range of modification, changes and substitution is contemplated in the foregoing disclosure. In some instances, some features of the present invention may be employed without a corresponding use of the other features. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.

What is claimed is:

1. A method of fabricating a sensor element, comprising:

using a first process to fabricate a measurement mass wafer for detecting acceleration, the measurement mass wafer including a mass housing having a cavity, and a spring mass assembly positioned within the cavity;

fabricating a top cap wafer using the first process;

fabricating a bottom cap wafer using the first process;

bonding the top cap wafer to a side of the measurement mass wafer using a bonding process;

bonding the bottom cap wafer to another side of the measurement mass wafer using the bonding process; and

making one or more dicing cuts at predetermined locations on the sensor element.

2. The method of claim **1** further comprising etching a surface of the measurement mass wafer, applying a metal layer on the etched surface, and molding the metal layer to form a stiction-reducing electrode pattern.

3. The method of claim **1**, wherein fabricating the measurement mass wafer further includes fabricating a passage for venting air from the cavity.

4. The method of claim **3**, wherein the passage comprises a V-shaped groove.

5. The method of claim 3, wherein the dicing cuts are made through the top cap wafer and the bottom cap wafer and into the measurement mass wafer, stopping at a predetermined distance from the passage within the measurement mass wafer.

6. The method of claim 5 further comprising opening the passage after the dicing cuts are made to open an air vent to the passage.

7. The method of claim 6 further comprising a second process to expose the passage within the measurement mass wafer, wherein air is removed from the cavity through the passage to create a low pressure environment in the cavity, and wherein the passage is sealed to maintain the low pressure environment within the cavity.

8. The method of claim 6, further comprising packaging the sensor element in a sensor housing and using a vacuum process to remove substantially all air from the sensor housing during packaging to create a low pressure environment within the sensor housing; wherein air is removed from the accelerometer though the passage during the vacuum process; and wherein the sensor housing is sealed to maintain the low pressure environment.

9. The method of claim 1, wherein fabricating the top cap wafer further comprises forming a press frame recess in the top cap wafer.

10. The method of claim 1, wherein fabricating the bottom cap wafer further comprises forming a press frame recess in the bottom cap wafer.

11. The method of claim 1, wherein the dicing cuts penetrate through the top cap wafer, the bottom cap wafer, and at least partially through the measurement mass wafer.

12. The method of claim 1, wherein the top cap wafer includes a balanced metal pattern on an upper surface of the top cap wafer.

13. The method of claim 1, wherein the bottom cap wafer includes a balanced metal pattern on a lower surface of the bottom cap wafer.

14. The method of claim 1, wherein the spring-mass assembly comprises springs.

15. The method of claim 14, wherein the springs include an etch-stop layer on one or more surfaces of the springs.

16. The method of claim 1, wherein the measurement mass wafer includes one or more mass contact pads; and wherein the dicing cuts are made through the top cap wafer to expose the mass contact pads on the measurement mass wafer.

17. The method of claim 1, wherein the measurement mass wafer includes one or more mass contact pads; and wherein the dicing cuts are made through the bottom cap wafer to expose the mass contact pad on the measurement mass wafer.

18. The method of claim 1, wherein the measurement mass includes one or more mass contact pads and the dicing cuts are made:

through the top cap wafer to expose the mass contact pads on the measurement mass wafer; and

through the bottom cap wafer to expose the mass contact pads on the measurement mass wafer.

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