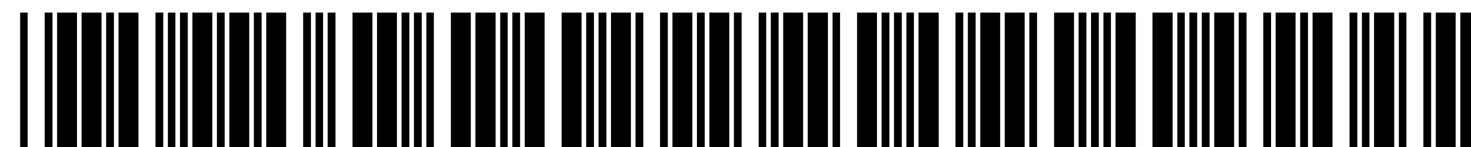

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(54) **SILICON BUILDING BLOCKS IN INTEGRATED CIRCUIT PACKAGING**

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(52) **U.S. Cl.** **438/113**; 357/23.6; 357/23.4; 357/23.11; 136/201; 438/745; 438/753

(58) **Field of Search** 357/23.6, 23.4, 357/23.11; 136/201; 438/745, 753

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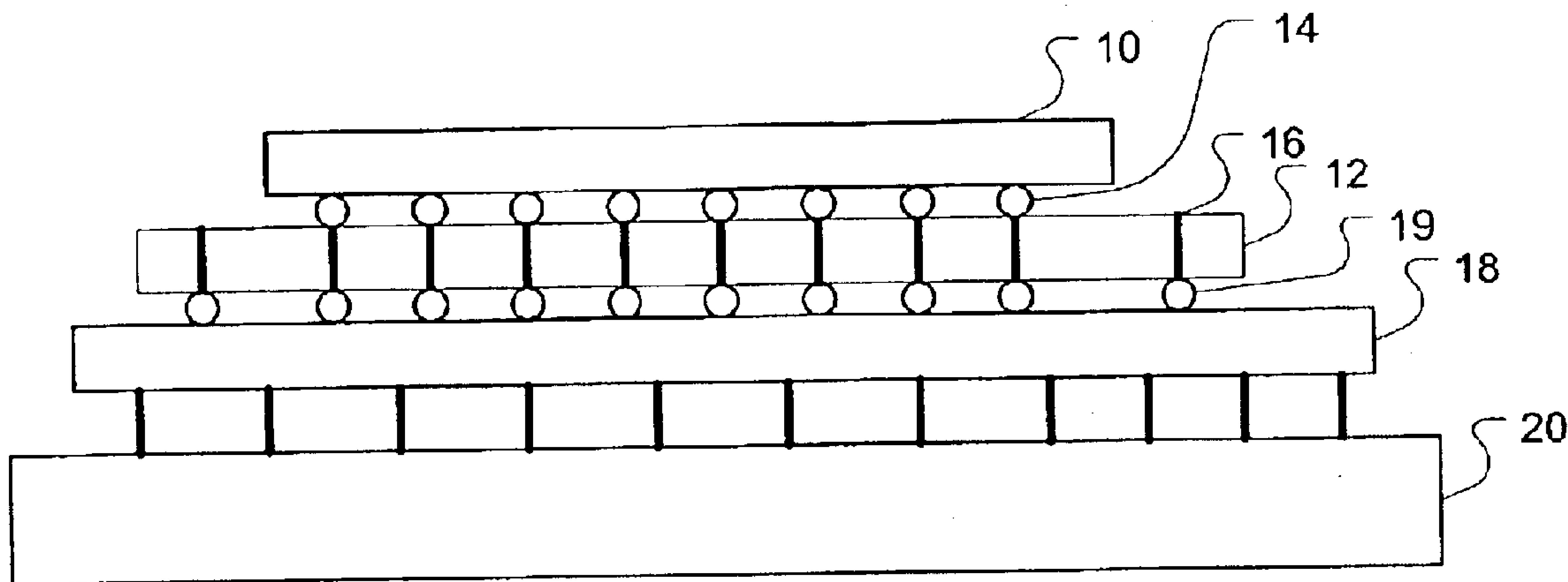
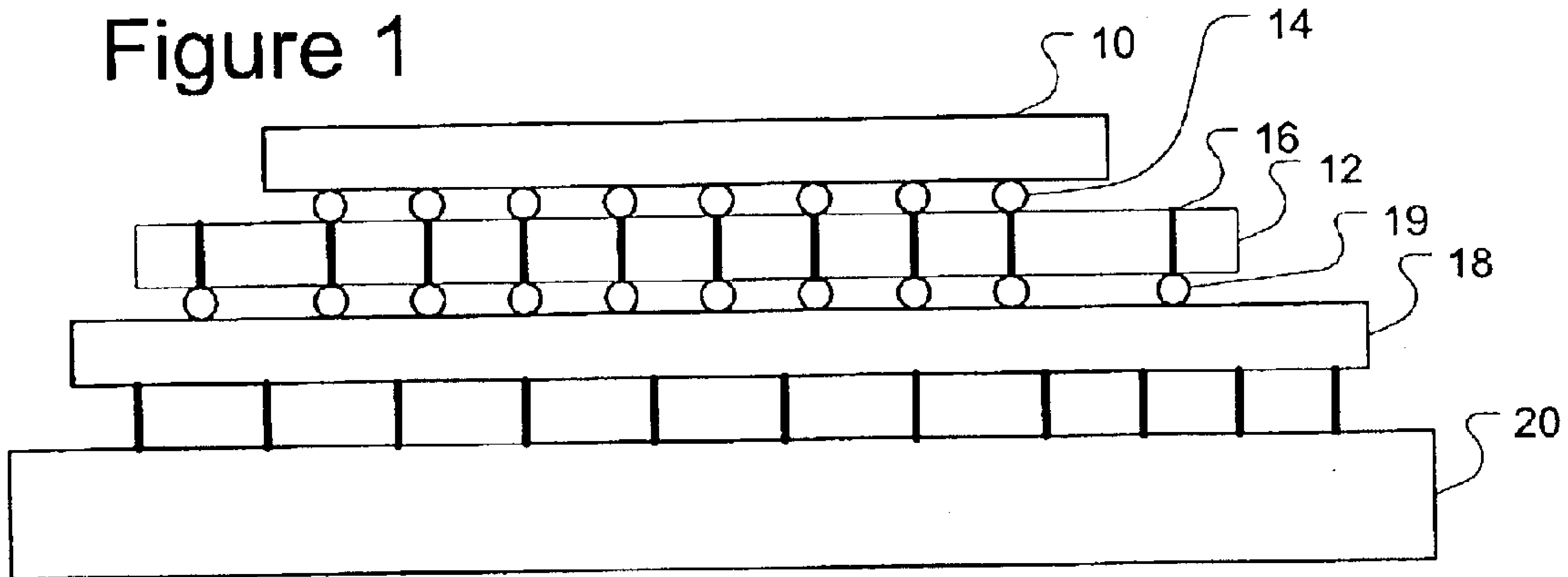
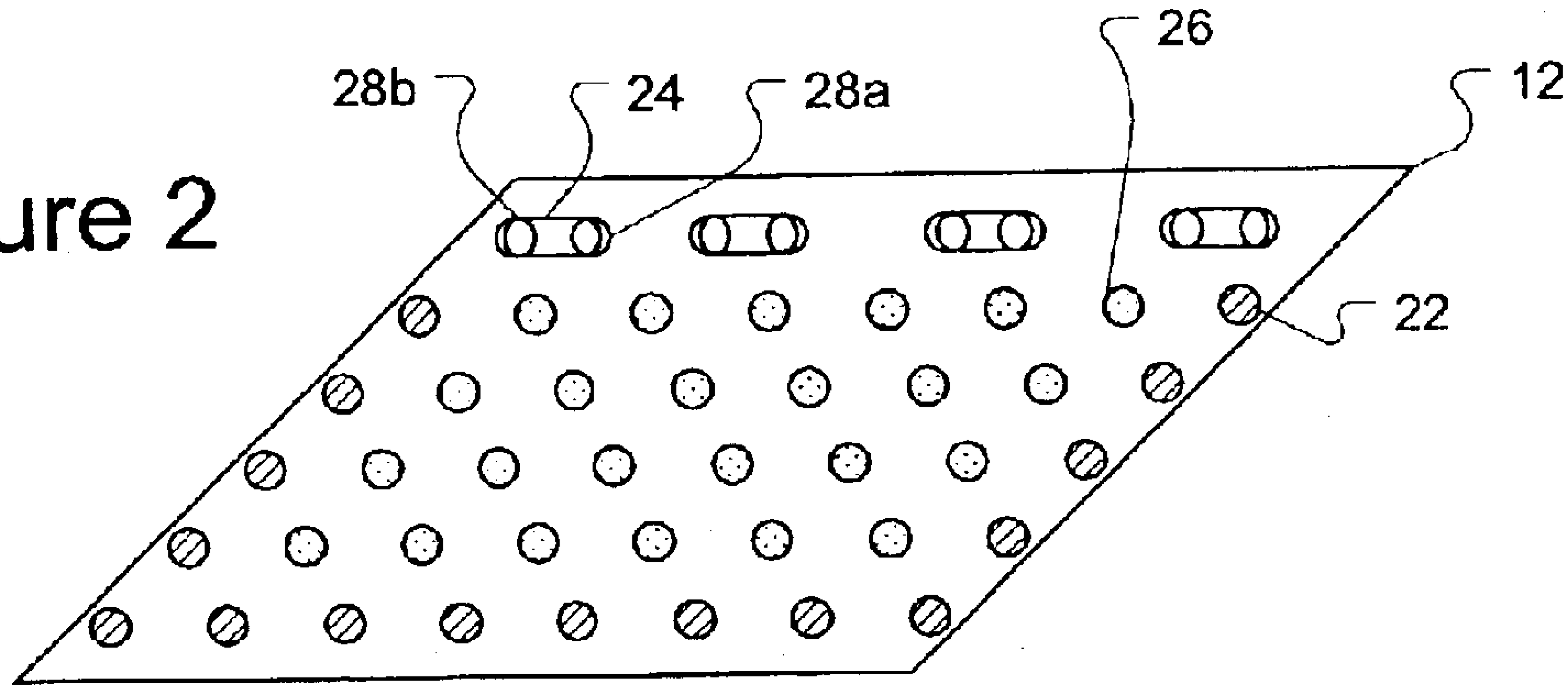
(57) **ABSTRACT**

An improved silicon building block is disclosed. In an embodiment, the silicon building block has at least two vias through it. The silicon building block is doped and the vias filled with a first material, and, optionally, selected ones of the vias filled instead with a second material. In an alternative embodiment, regions of the silicon building block have metal deposited on them.

6 Claims, 2 Drawing Sheets







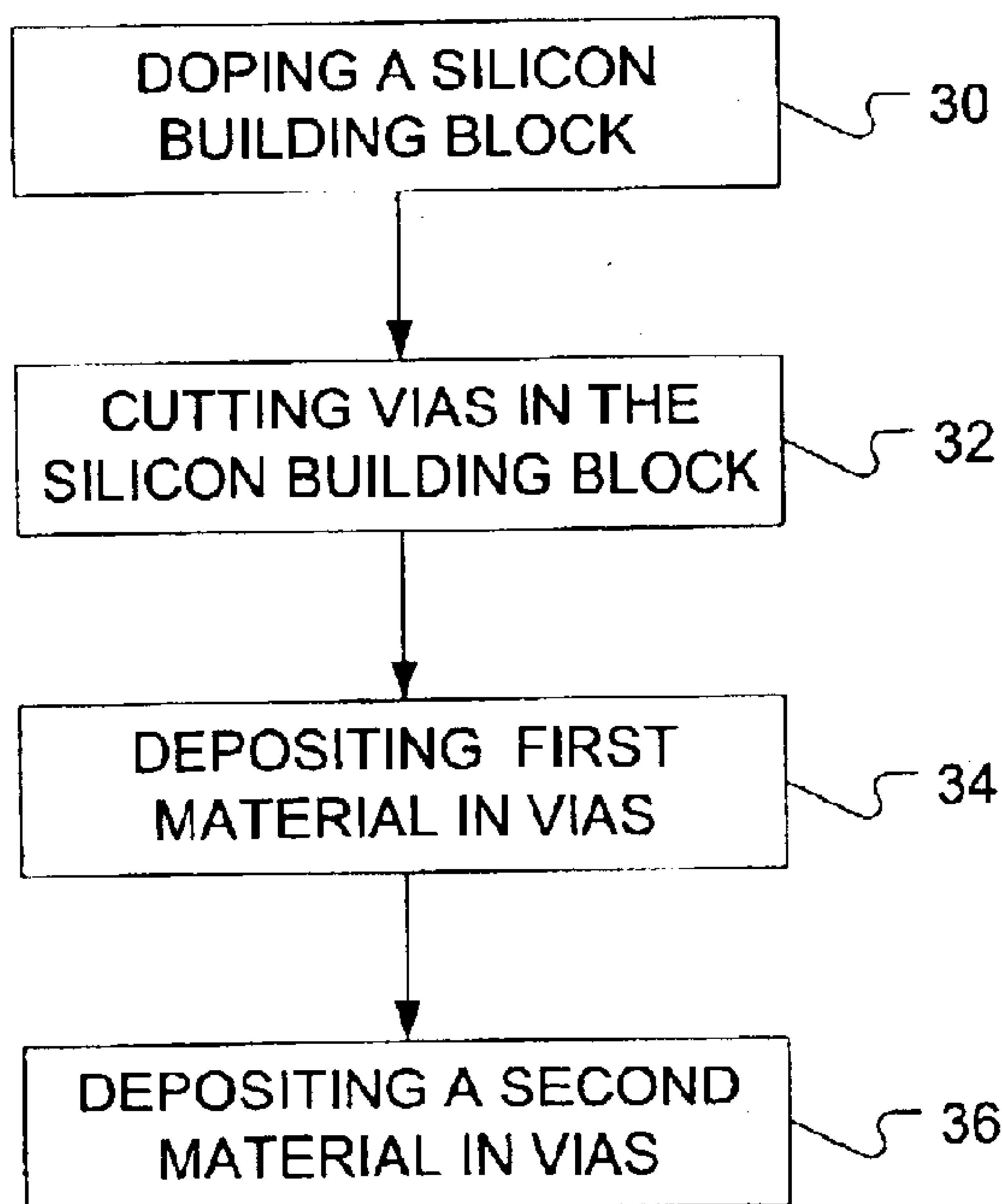


Figure 3

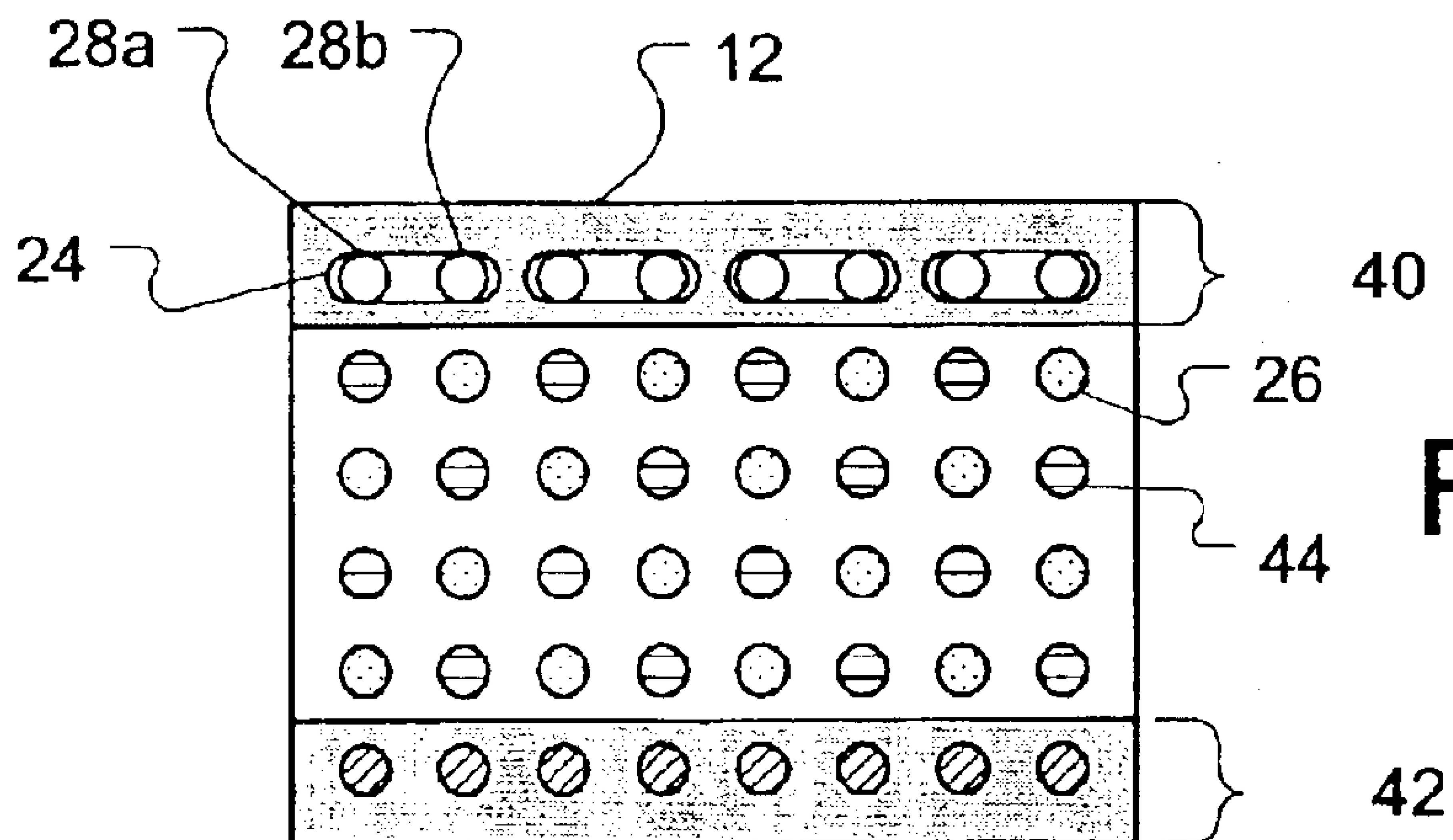
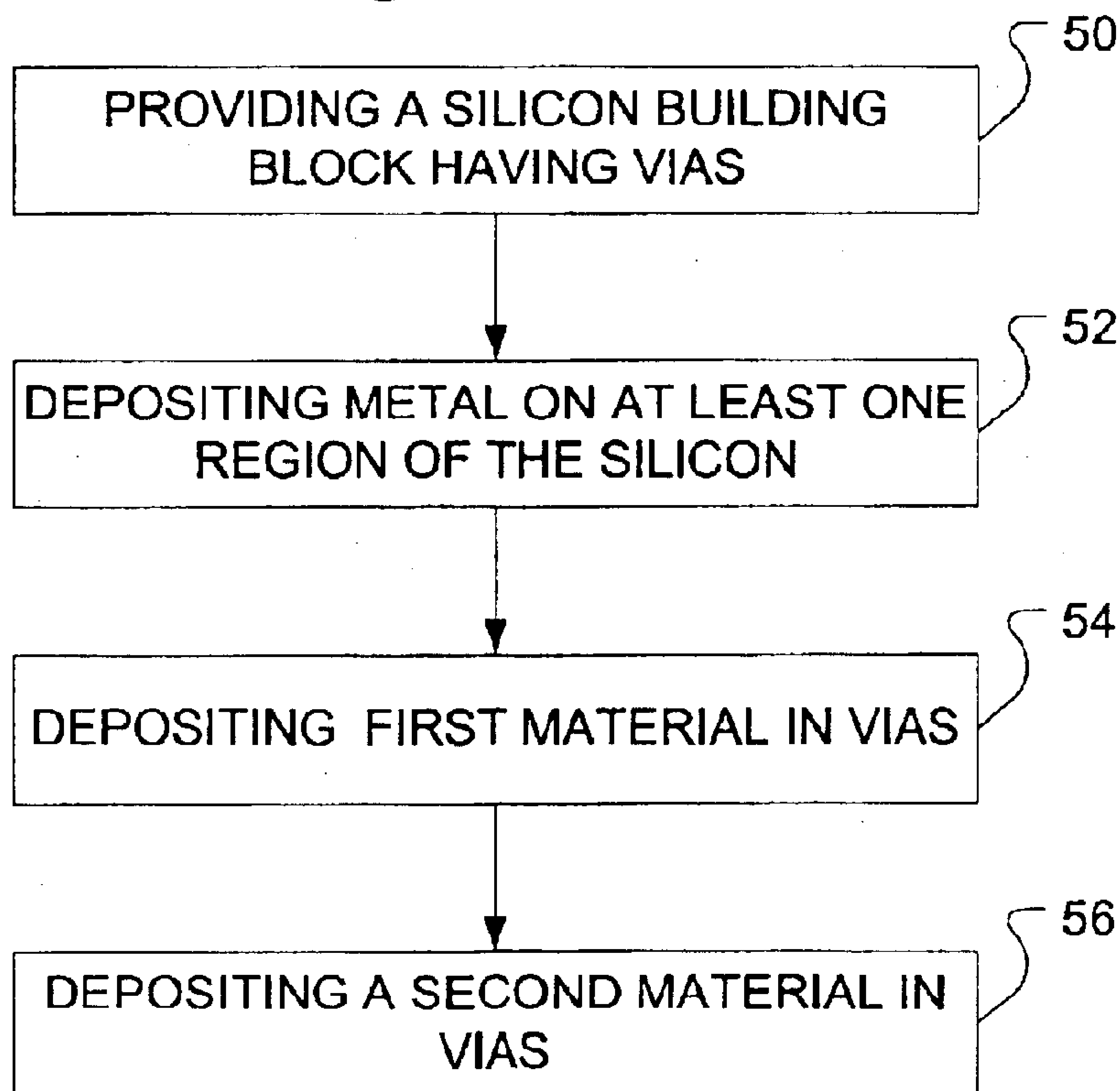


Figure 4

Figure 5



SILICON BUILDING BLOCKS IN INTEGRATED CIRCUIT PACKAGING

BACKGROUND

As the speed and density of semiconductor integrated circuits increase, thermal and electrical connectivity issues have raised the requirements for packaging. Many integrated circuits are packaged using organic materials, materials and their processes not necessarily compatible with the expertise and capability of the semiconductor integrated circuit manufacturers. Some manufactures have taking to using a block of silicon between the integrated circuit die and the printed circuit board upon which it is to be mounted.

Generally, the integrated circuit die is mounted on the silicon building block, which in turn may be mounted on a plastic, or other material, substrate or package. This entire apparatus is then mounted on the printed circuit board. Mounting to the printed circuit board generally involves a ball grid array or pin grid array to complete the electrical connections between the integrated circuit and the printed circuit board.

The addition of silicon building blocks has loosened some of the manufacturing requirements of the package, reducing costs and making the packaging process less prohibitive to semiconductor manufacturers. However, the addition of the silicon building block has led to some problems such as large insertion loss, high return loss, cross talk and a high impedance path for power delivery. The silicon building block has high dielectric loss, resulting in large insertion loss. The return loss results from the impedance mismatch between the silicon building block and the die. Cross talk problems arise because of the higher order mode that propagates through the silicon building block. The small vias used for Vcc and Vss result in a high impedance path for power delivery.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention may be best understood by reading the disclosure with reference to the drawings, wherein:

FIG. **1** shows a cross sectional view an embodiment of an integrated circuit package with a silicon building block.,

FIG. **2** shows a top view of an embodiment of a doped silicon building block.

FIG. **3** shows a flowchart of an embodiment of a method of manufacturing a doped silicon building block.

FIG. **4** shows a top view of an embodiment of a silicon building block having at least one metal region.

FIG. **5** shows a flowchart of an embodiment of a method of manufacturing a silicon building block with a metal region.

DETAILED DESCRIPTION OF THE EMBODIMENTS

FIG. **1** shows a cross sectional view of an example of an integrated circuit being packaged using a silicon building block. An integrated circuit die **10** contains the operational components of an integrated circuit, such as a microprocessor, controller or other integrated circuit. It is to be mounted onto the printed circuit board **20**, in which there are electrical connection paths, or traces, with which the operational components of the integrated circuit **10** must become electrically coupled. In between the die **10** and the printed circuit board **20** are a silicon building block **12** and a plastic, or other material, interposer substrate **18**.

"The electrical connection paths are maintained through the silicon building block y the solder balls **14** between the integrated circuit **10** and the silicon building block **12**, and the solder balls **19** between the silicon building block and the interposer substrate. In the silicon building block, vias such as **16**, filled with the appropriate material allow the connections between the integrated circuit and the printed circuit board to be completed."

In previous implementations of the silicon building block, there is large insertion loss due to the high dielectric loss, high return loss due to the impedance mismatch created by the building block, large amounts of cross talk generated by the higher order mode propagating through the building block and a high impedance path for power delivery due to small sizes of the Vcc and Vss vias.

In the embodiment of the silicon building block of FIG. **1**, the silicon building block is doped to avoid these problems. This particular implementation has the silicon building block N-doped, that is, doped with a material such as antimony, arsenic and phosphorous. Essentially, this causes the silicon building block **12** to act as a ground plane, providing a common reference for all of the signals that pass through the vias.

FIG. **2** shows a top view of an embodiment of a silicon building block having vias. The silicon building block itself is heavily N-doped, causing it to act as a ground plane. Vias such as **22** have a first material deposited inside them that is for single-ended signals. Single-ended signals, as that term is used here, as signals that have one-bit per wire, such as digital data signals. Via **24** actually has two smaller vias within it, for differential signals. Differential signals typically have a plus and a minus component, each of which signal has its own 'wire,' or in this case, via. Differential signals may be better understood as signals of one-bit of data having two wires.

Both single-ended and differential signals benefit from having a common reference signal. Differential signals require that the plus and minus components have a common reference, although the reality is that there is often a variation between the reference for the positive component and the reference for the negative component. This can cause problems for the differential signals, as it is the difference of each component from the common reference that determines the state of the bit. Using the heavily doped silicon building block as the common reference alleviates this problem.

Similarly, the use of the silicon building block as the ground plane eliminates the high impedance problems previously experienced in power delivery through the previous implementation of the silicon building block. Having the ground plane essentially between the wires, in this case the filled vias act as wires, also prevents cross talk and reduces the insertion and return loss. In one embodiment, the different vias for the different types of paths needed through the vias have different materials.

For example, as can be seen by the vias with the diagonal stripes, such as **22**, the vias for the single-ended signals has a first type of material deposited in them. The vias **28***a* and **28***b* for the differential signals may be of the same material or of a different material. For example, it may be advantageous to use a low-loss material with a low average dielectric constant (K). A low-K material, as that term is used here, would have a K value in the range of 1.3 to 2.5, inclusive. For the power vias such as **26**, using a high-K material may be advantageous as well, where a high K material would

have an average dielectric constant of 100 or more, even as high as greater than 1000.

An embodiment of a method of manufacturing a doped silicon building block is shown in FIG. **3**. The silicon building block is doped at **30**. Vias are then cut into the block at **32**, more than likely by standard semiconductor processing techniques such as masking, patterning and etching the vias. At **34** a first material is deposited in selected ones of the vias, such as the low-K, low-loss material mentioned above. At **36**, a second material is depositing in selected ones of the vias. However, it should be noted that the use of a second material is optional. For cost reduction and manufacturing simplicity, the same material could be used for both the power paths and the signal paths, although that material would more than likely not be a low-loss, low-K material.

An alternative embodiment of an improved silicon building block is shown in FIG. **4**. In this embodiment, the silicon building block **12** has at least one region upon which is deposited metal. In the particular embodiment of FIG. **4**, there are two regions of metal, **40** and **42**. The first region of metal **40** is in the region where the vias **24** for the differential signal vias **28***a* and **28***b* reside. The second region of metal **42** is in the region where the vias for the single-ended signals **22** reside. As the silicon building block does not act as a ground plane in this embodiment, there are two different types of vias for power delivery, the horizontally lined vias such as **44** for Vss and the dotted vias for Vcc.

In this manner a coaxial transmission line structure is created. The metal provides signal reference for the high-speed differential signals and the single-ended signals, while separating the signaling vias from the power vias. This will alleviate the signaling problems caused by insertion loss, return loss and crosstalk, while allowing better impedance control of the power delivery.

FIG. **5** shows an embodiment of a method of manufacturing a silicon building block with at least one metal region. At **50**, a silicon building block having vias is provided. It is probably more efficient and cost-effective to etch the vias prior to depositing the metal, as it is easier to etch silicon than metal. The metal is deposited on the silicon building block at **52**. A first material is deposited in the vias at **54**. A second material is deposited in the vias at **54**.

As mentioned above, the use of a second material is optional. However, using the low-K, low-loss material discussed above for the signaling vias and a high-K material for the power vias has several advantages. If one material is used for the vias, it is more than likely not going to be either a low-K or a high-K material, but something suitable for both power delivery and signaling paths. If two materials are used, the first material would be deposited in first selected ones of the vias, and the second in second selected ones. With only one material, the first selected ones would constitute all of the vias.

In either of these alternative embodiments as well as all the variations and combinations thereof, a silicon building block is adapted to provide improved signal and power characteristics for the integrated circuit package. Use of the improved silicon building block alleviates problems with cross talk, insertion and return losses and impedance control for power delivery. The improvements to the silicon building block are semiconductor-compatible processes that leverage the expertise of the semiconductor manufacturers.

Thus, although there has been described to this point a particular embodiment for a method and apparatus for packages with improved silicon building blocks, it is not intended that such specific references be considered as limitations upon the scope of this invention except in-so-far as set forth in the following claims.

What is claimed is:

1. A method, comprising:

doping a piece of silicon;

cutting vias completely through the piece of silicon; and

depositing a first material in first selected ones of the vias.

2. The method of claim **1** further comprising depositing a second material in second selected ones of the vias.

3. The method of claim **1** wherein doping the piece of silicon further comprises N-doping the piece of silicon.

4. The method of claim **3** wherein N-doping the piece of silicon further comprises doping the piece of silicon with one of the group comprised of: antimony, arsenic and phosphorous.

5. A method, comprising:

cutting vias completely through a piece of silicon;

depositing metal on at least one region of the piece of silicon containing at least some of the vias;

depositing a first material in first selected ones of the vias; and

depositing a second material in second selected ones of the vias.

6. The method of claim **5** wherein depositing metal further comprised depositing metal on two regions, each containing some of the vias, arranged at opposite ends of the piece of silicon.

* * * * *