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Choi et al.

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(54) **METHOD OF MANUFACTURING NON-VOLATILE MEMORY DEVICE**

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(22) Filed: **May 28, 2003**

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(51) **Int. Cl.**⁷ **H01L 21/336**

(52) **U.S. Cl.** **438/294; 438/197**

(58) **Field of Search** 438/142, 197,
438/218, 221, 223, 224, 231, 275, 294,
299, 301

Primary Examiner—David A. Zamela

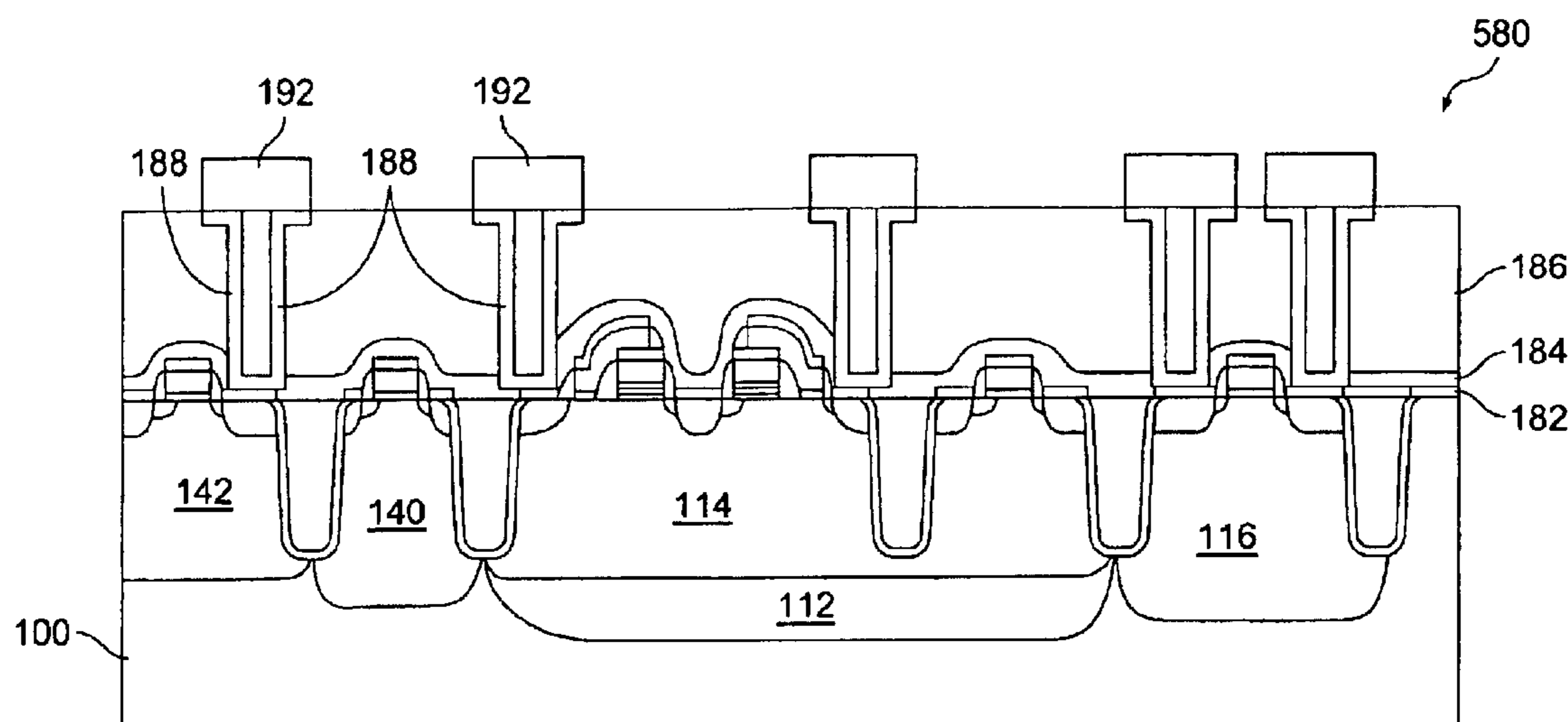
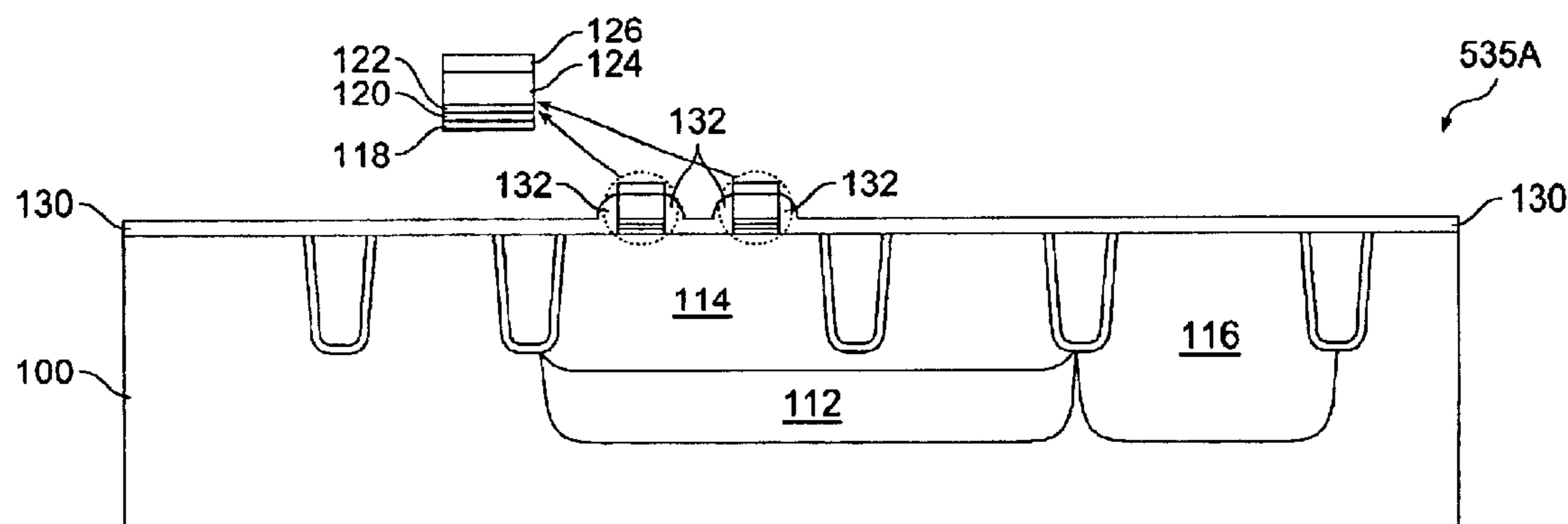
Assistant Examiner—Scott B. Geyer

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(57) **ABSTRACT**

A method of forming an integrated circuit, includes, in part: forming trench isolation in a semiconductor substrate, forming a first well between the trench isolation, forming a second well above the first well, forming a first oxide layer above a first portion of the second well, forming a first dielectric layer above the first oxide layer, forming a first polysilicon gate layer above the first dielectric layer, forming a second dielectric layer above the first polysilicon layer, forming a first spacer above the body region and adjacent the first polysilicon layer, forming a second oxide layer above a second portion of the second well not covered by the first spacer, forming a second polysilicon gate layer above the second oxide layer, the first spacer and a portion of the second dielectric layer, and forming a second spacer to define source and drain regions.

10 Claims, 10 Drawing Sheets



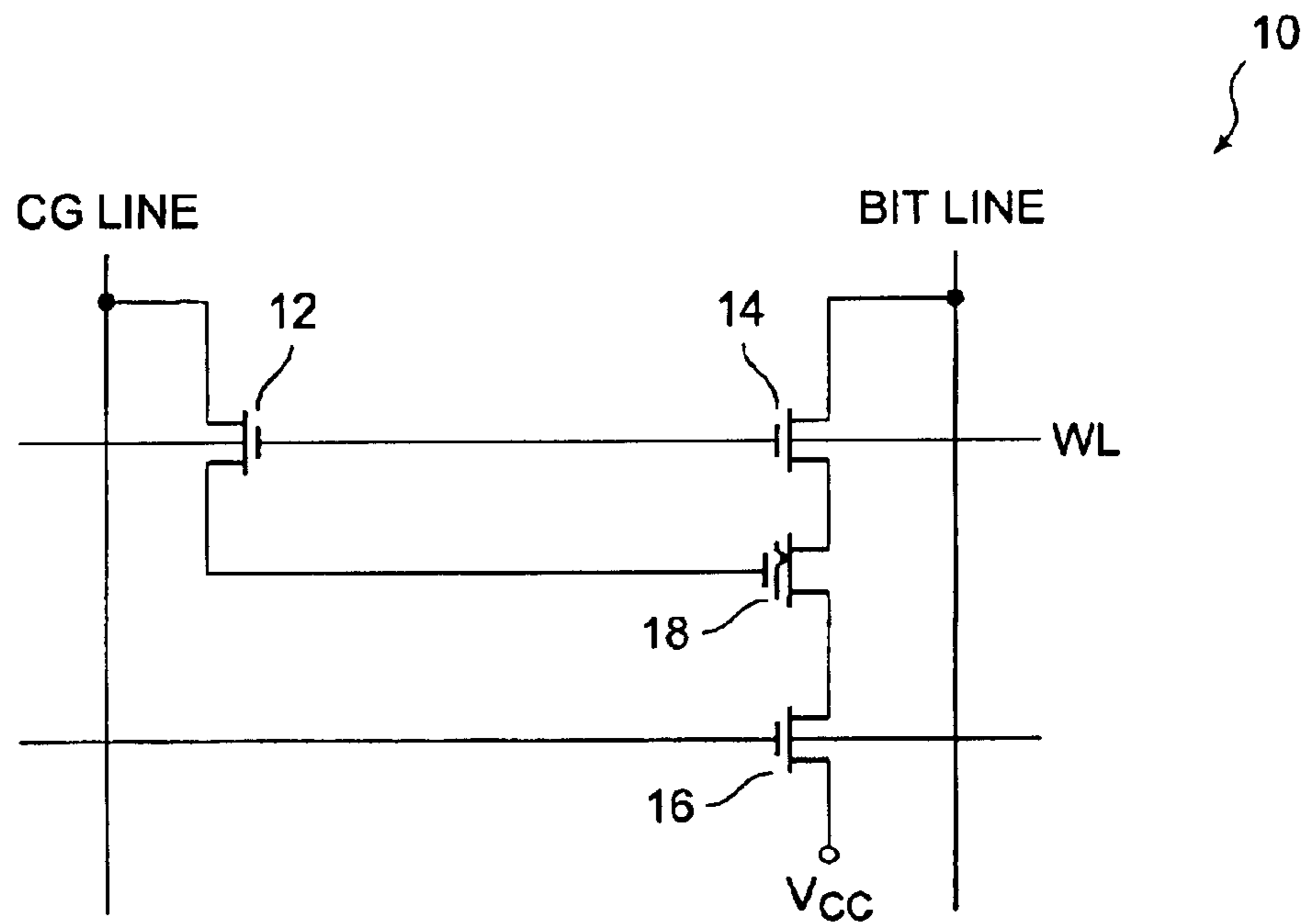


FIG. 1
Prior art

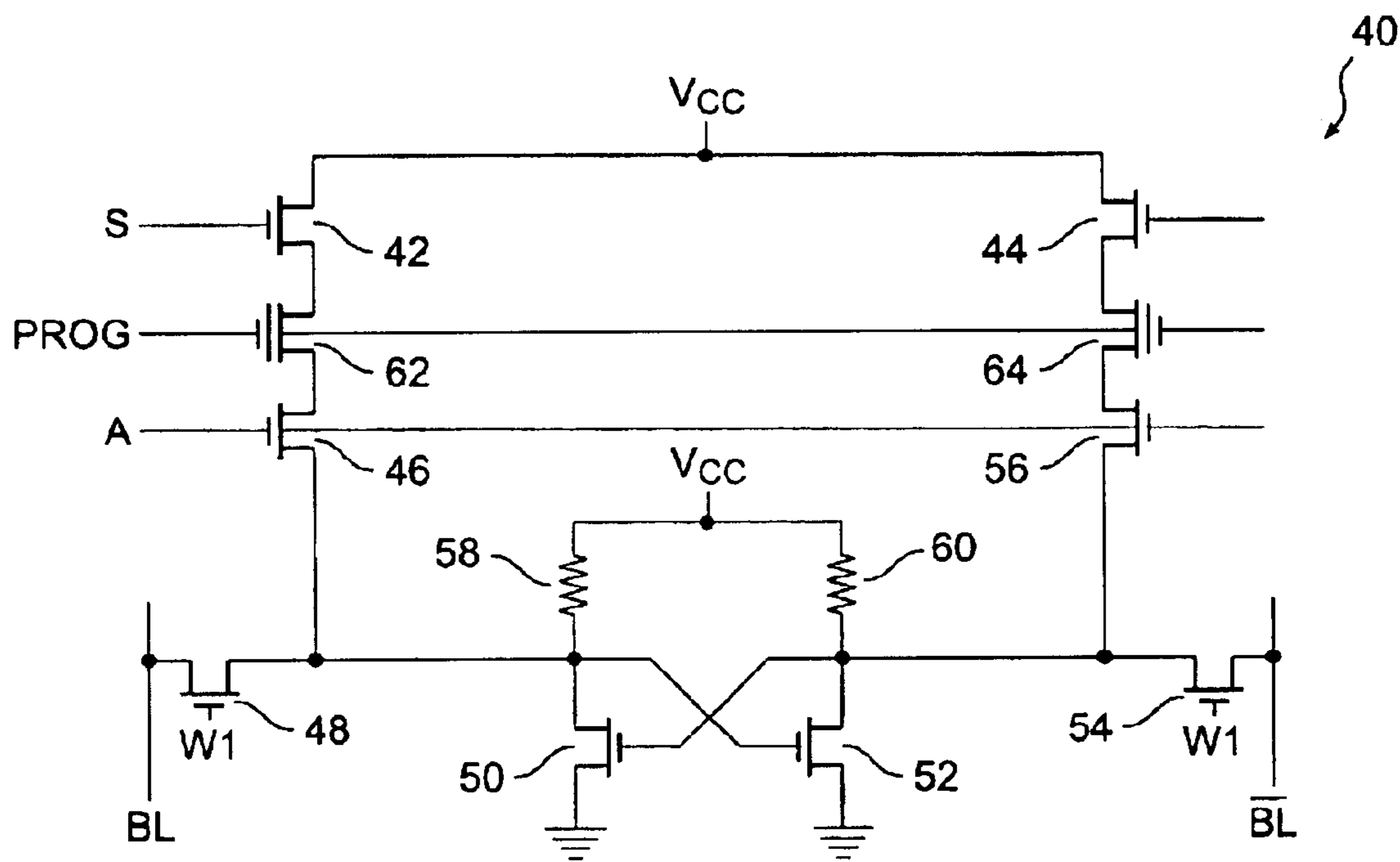


FIG. 2
Prior Art

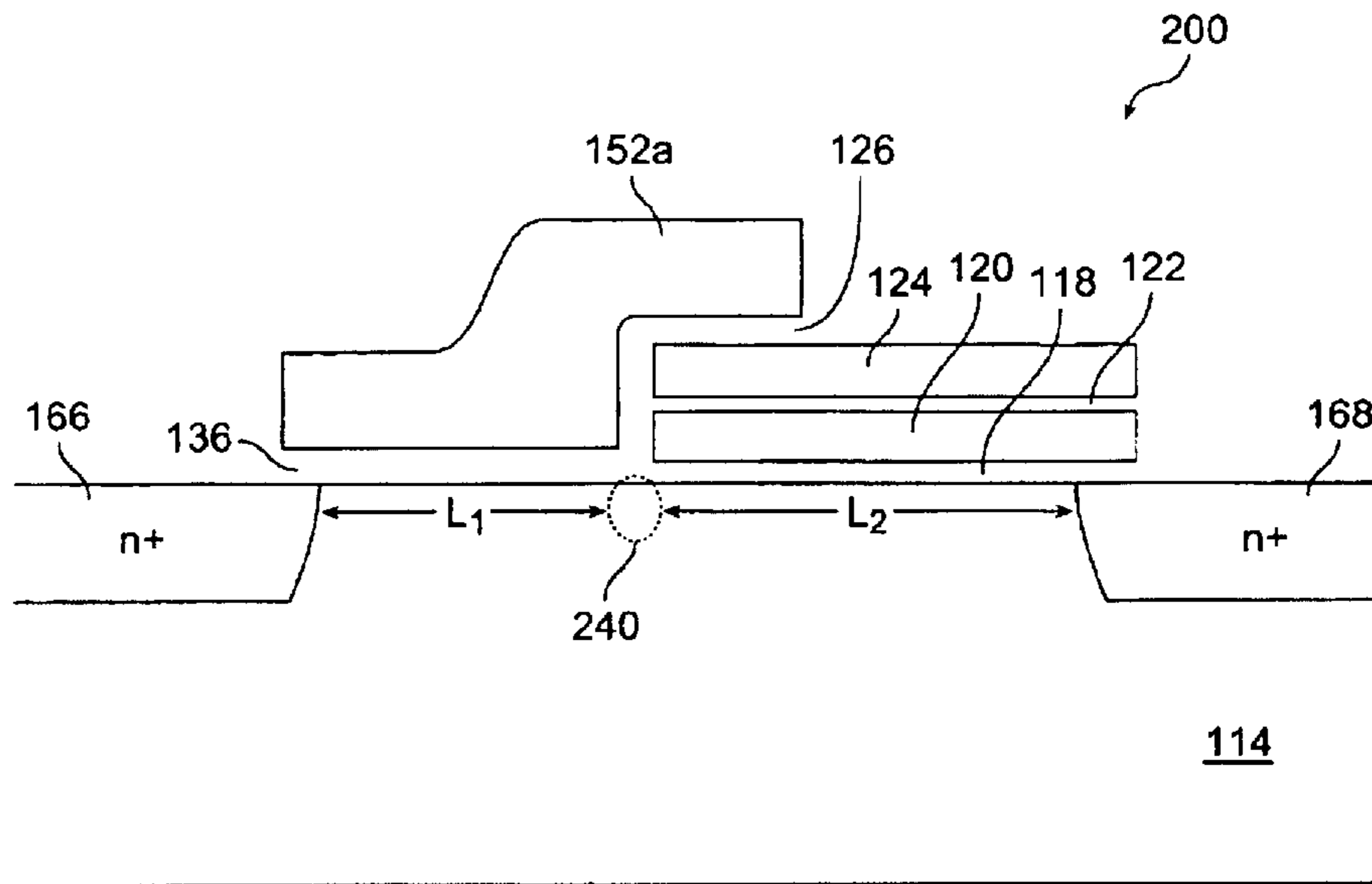


FIG. 3

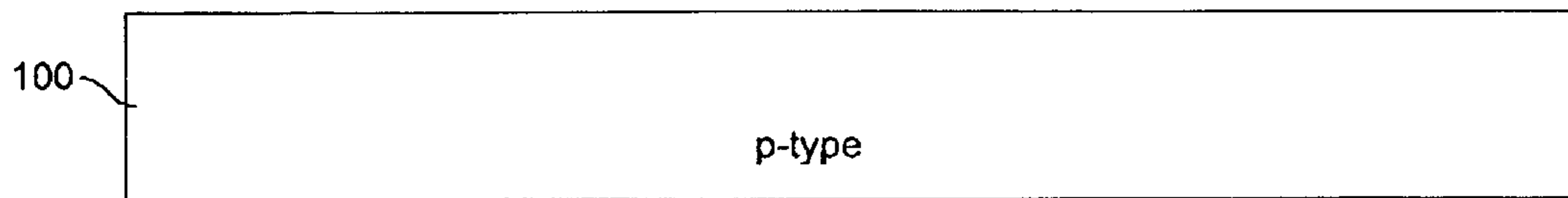


FIG. 4

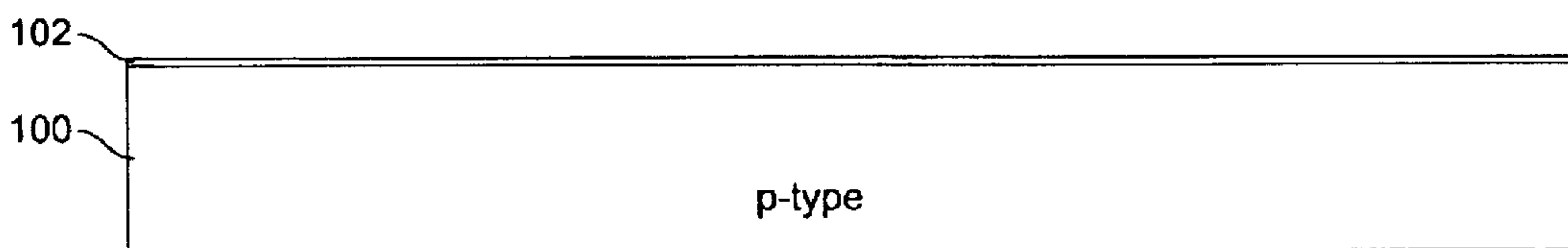


FIG. 5

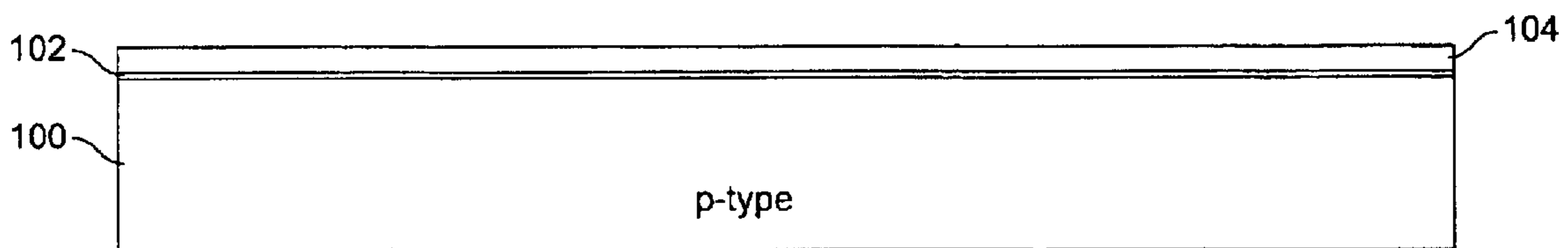


FIG. 6

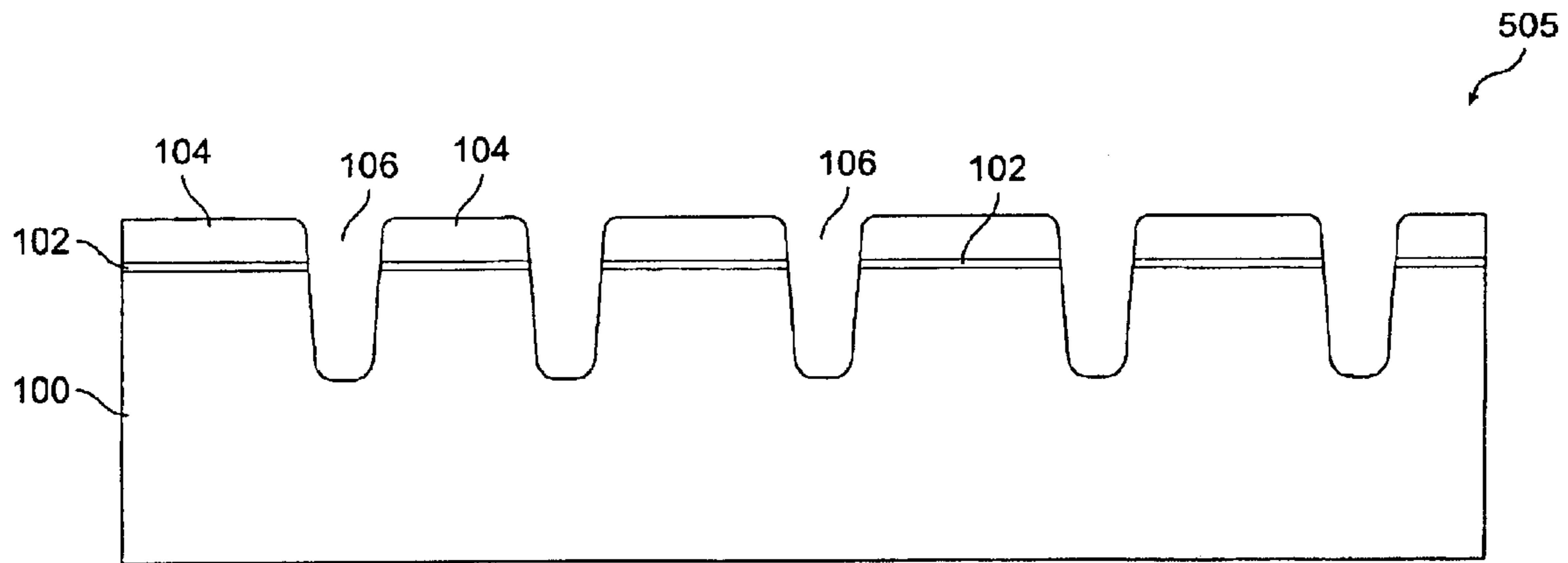


FIG. 7

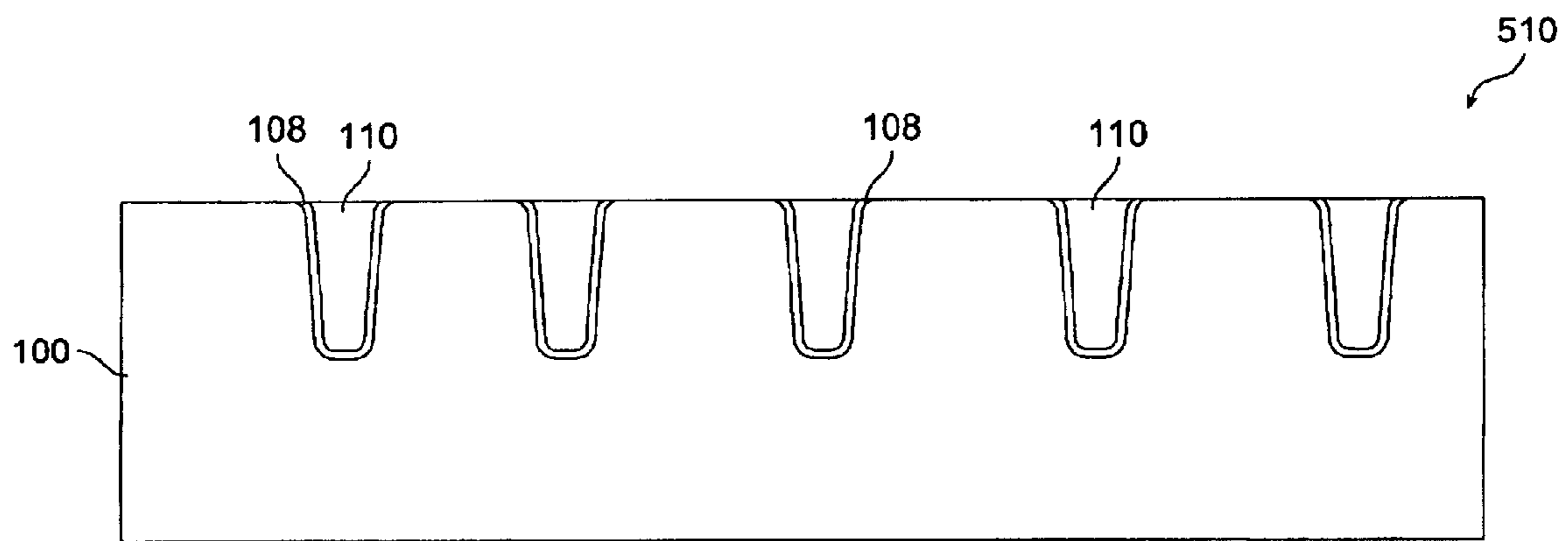


FIG. 8

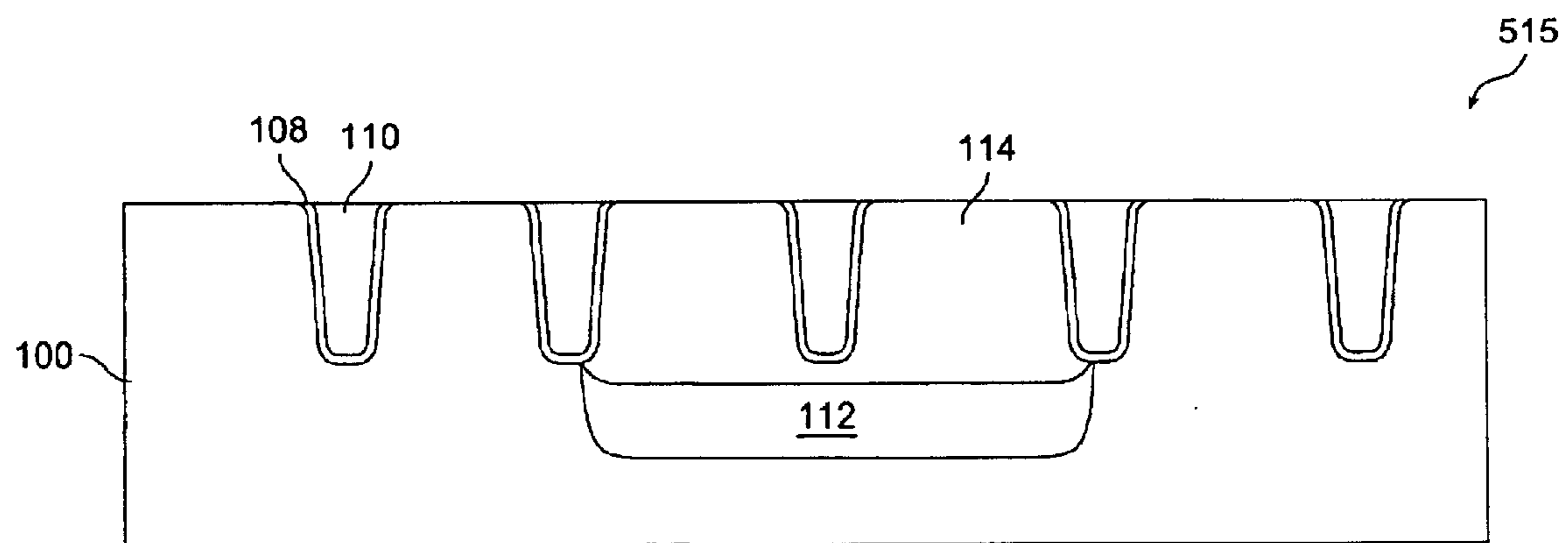


FIG. 9

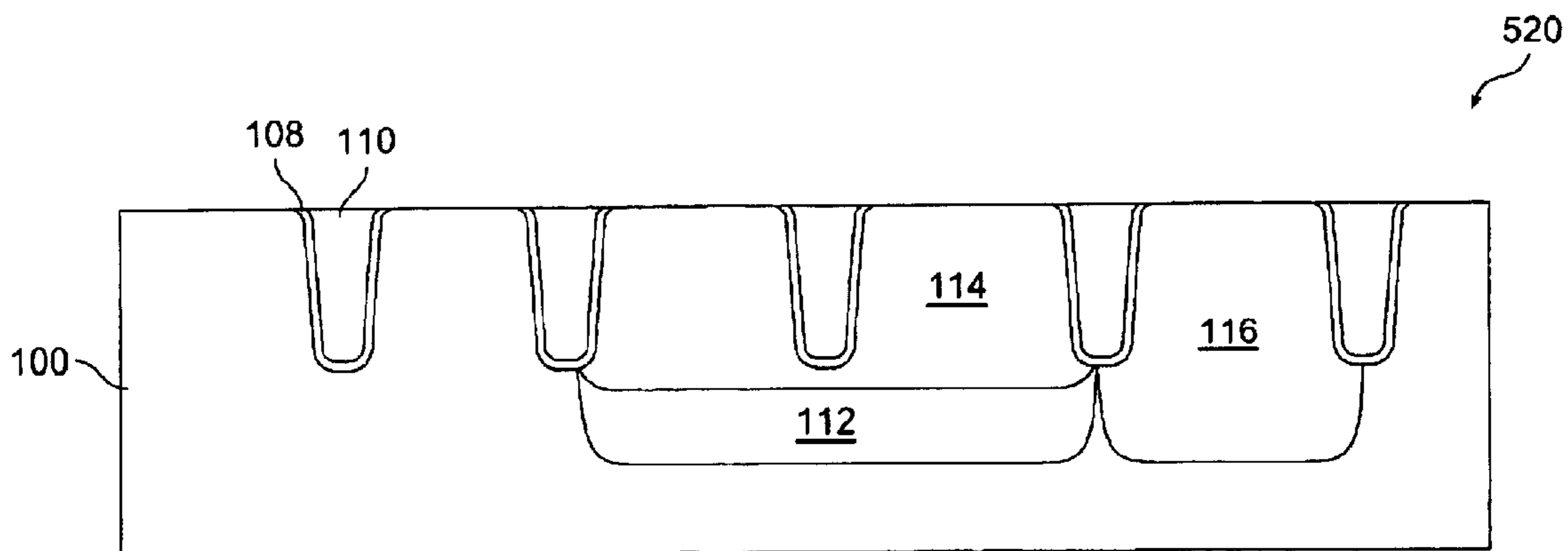


FIG. 10

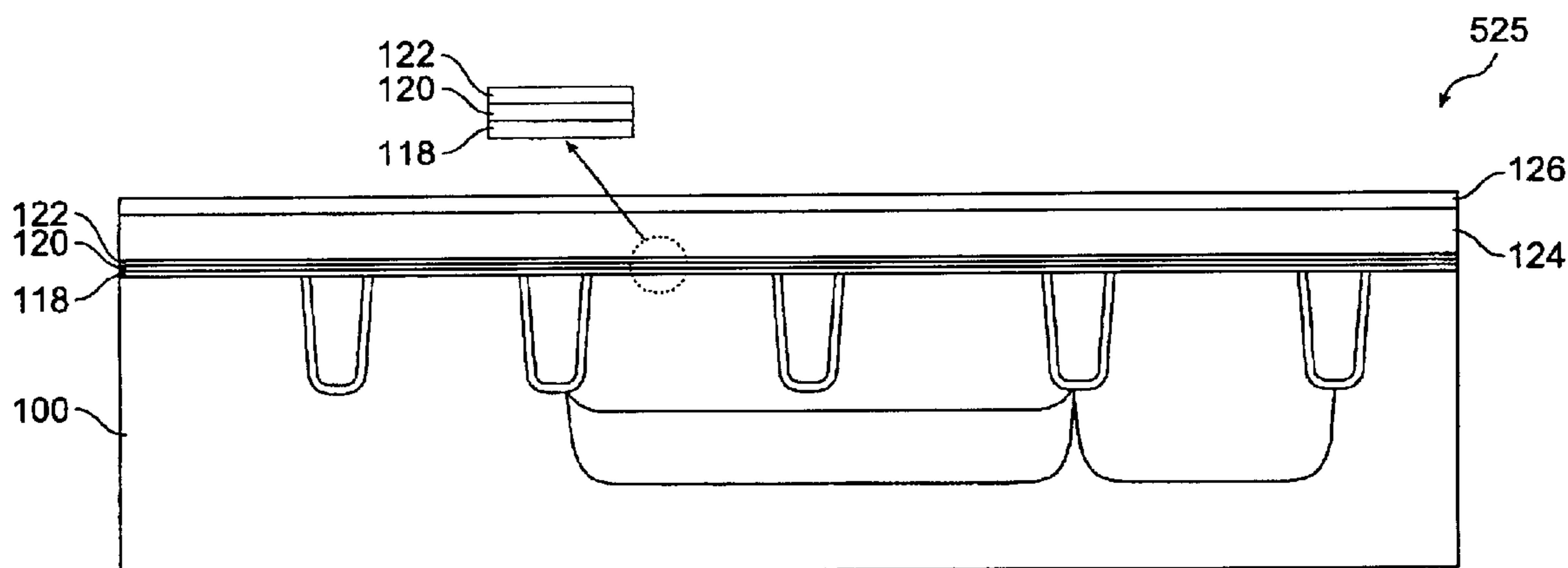


FIG. 11

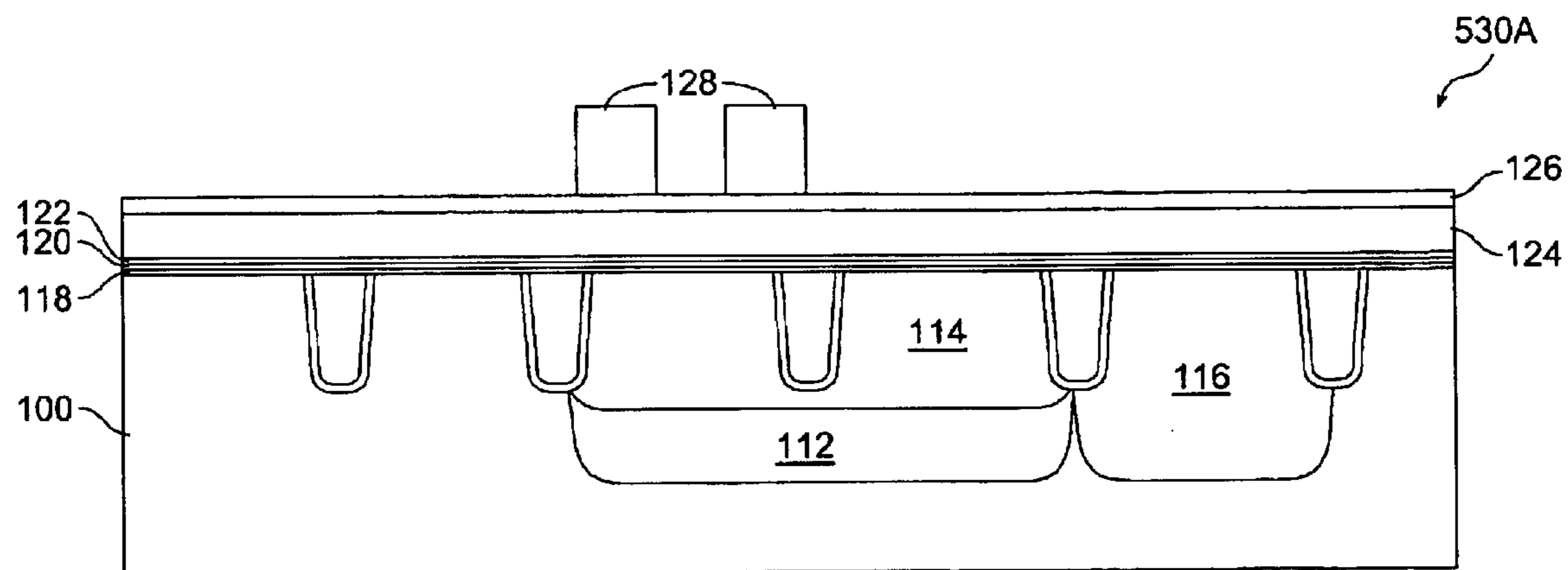


FIG. 12A

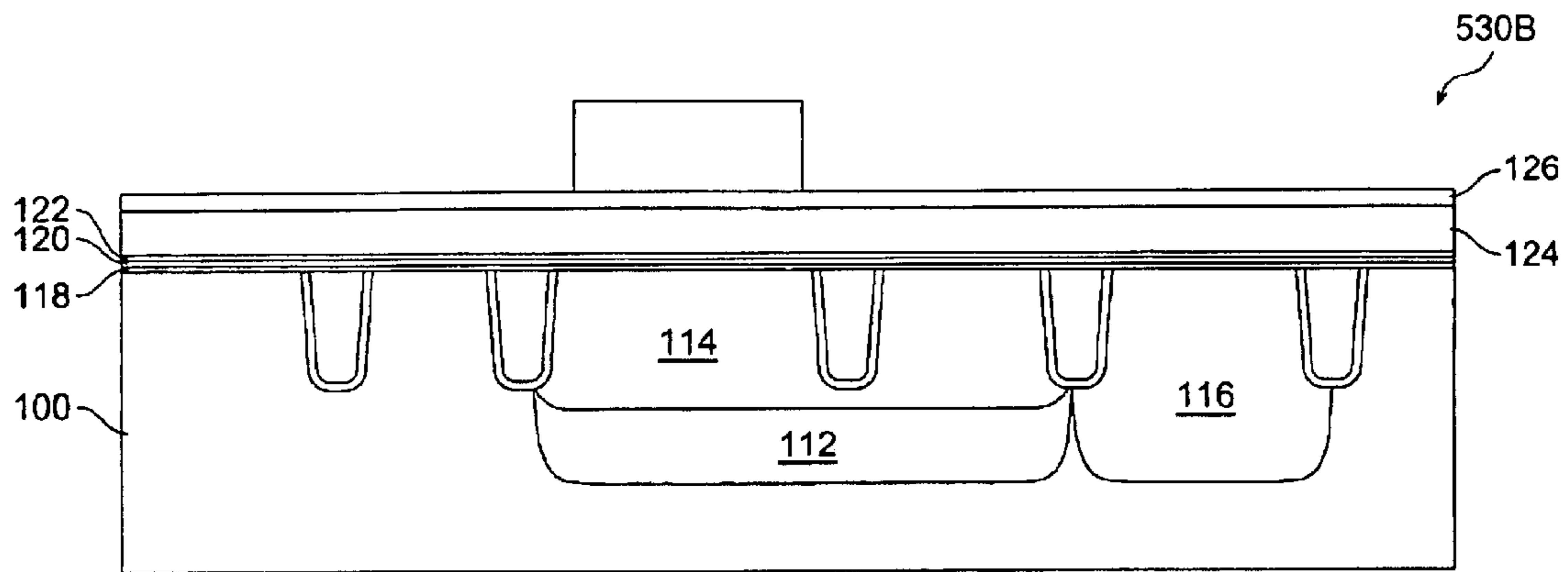


FIG. 12B

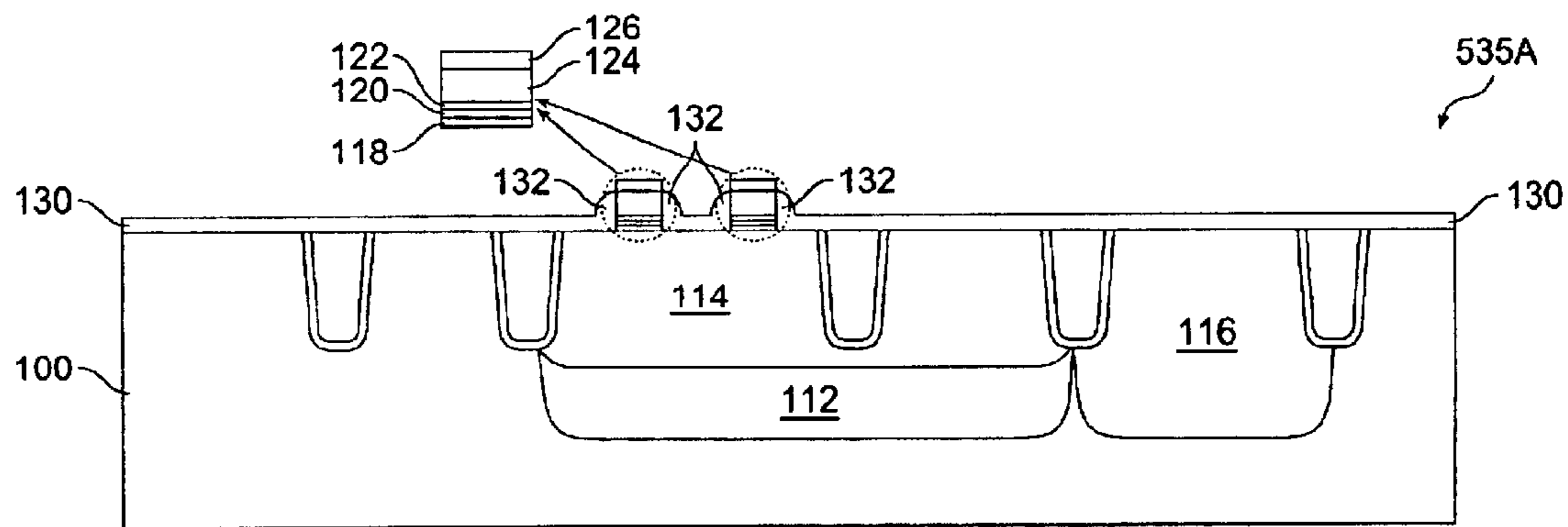


FIG. 13A

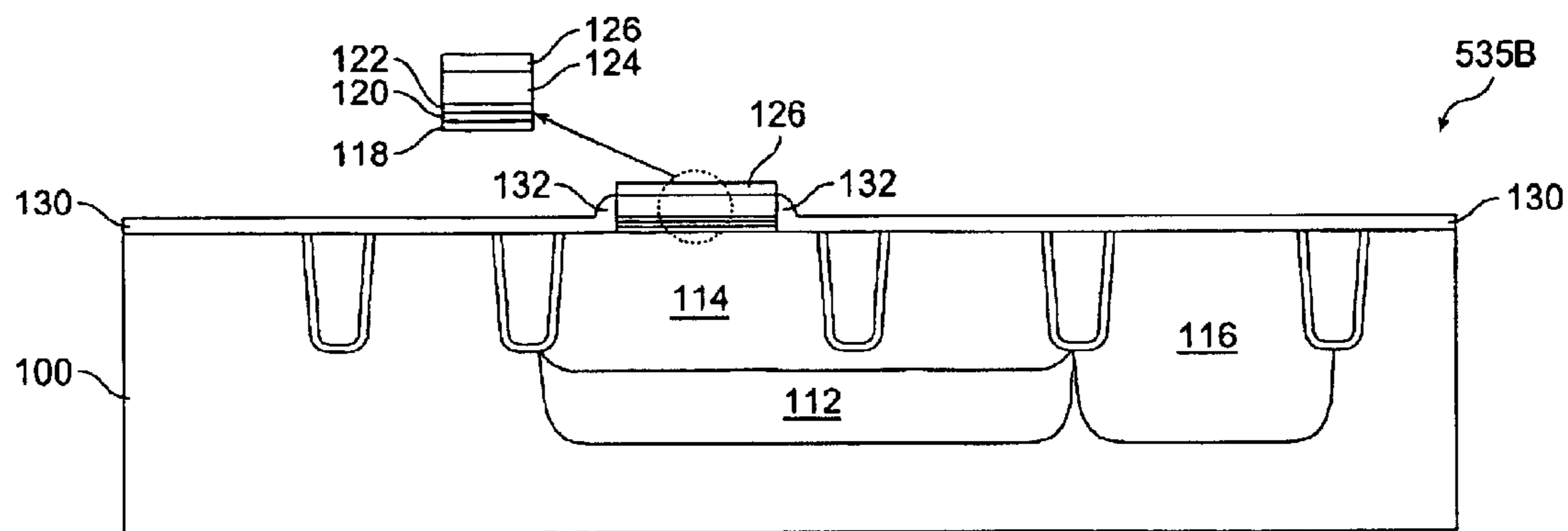


FIG. 13B

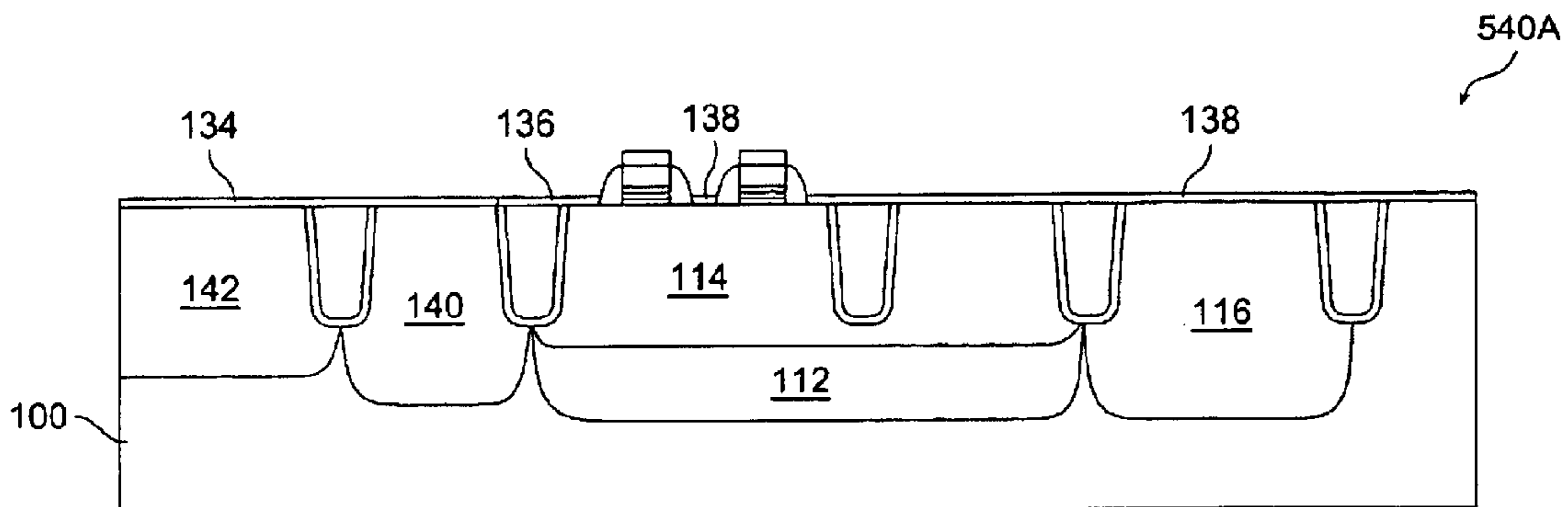


FIG. 14A

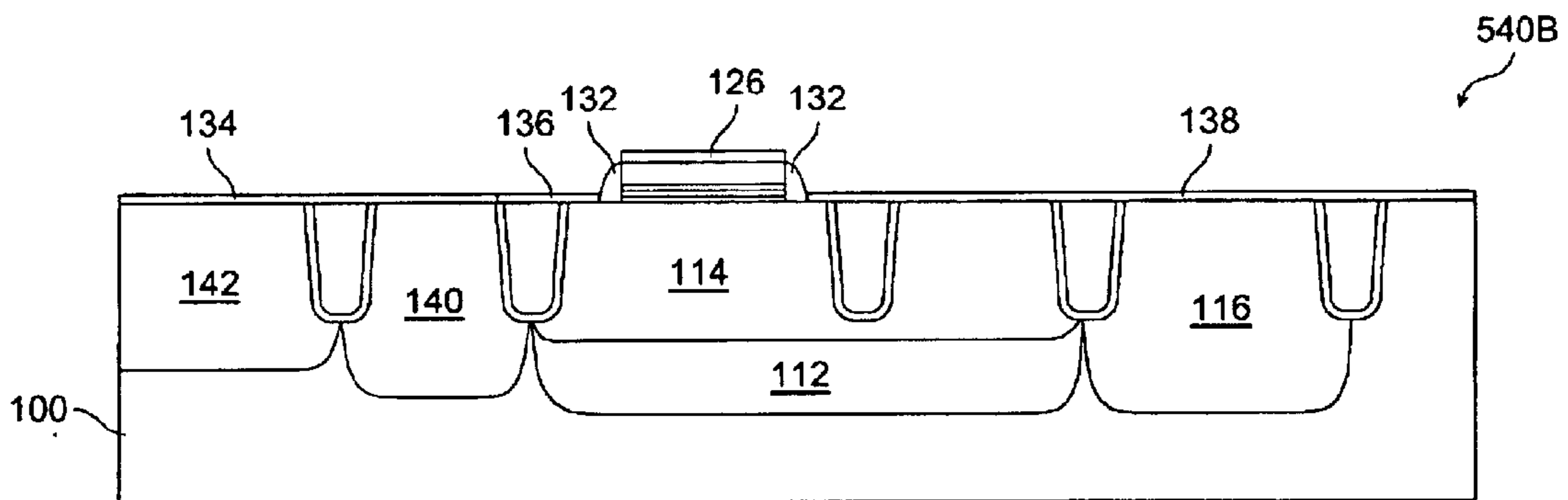


FIG. 14B

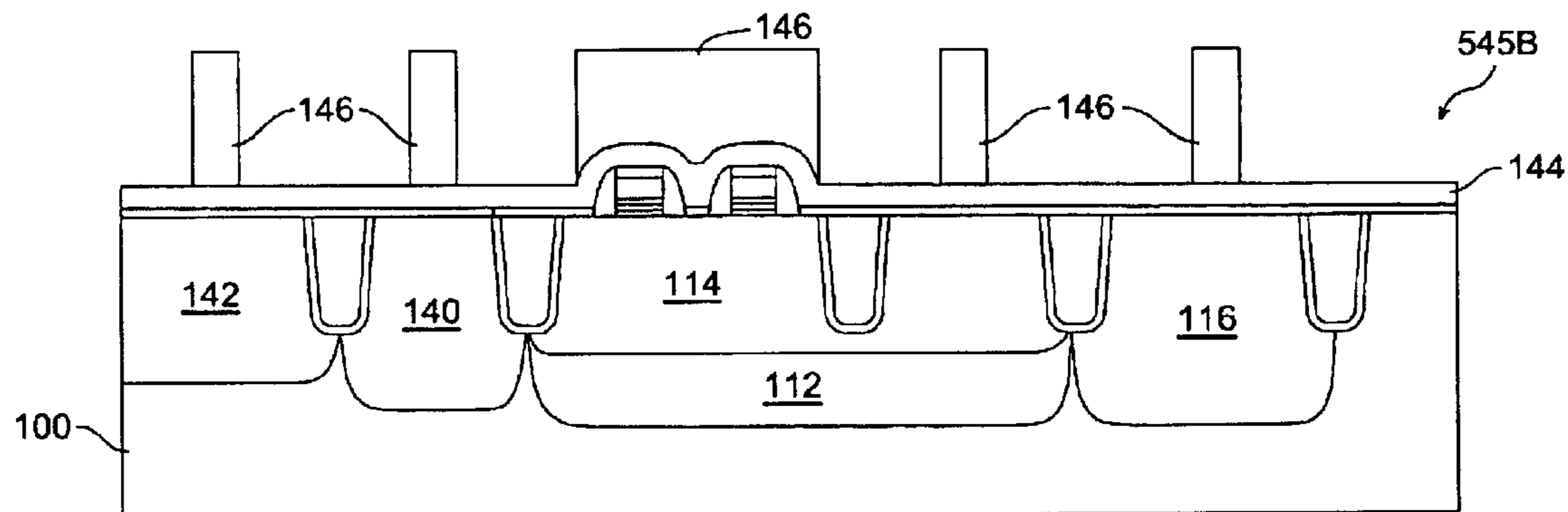


FIG. 15A

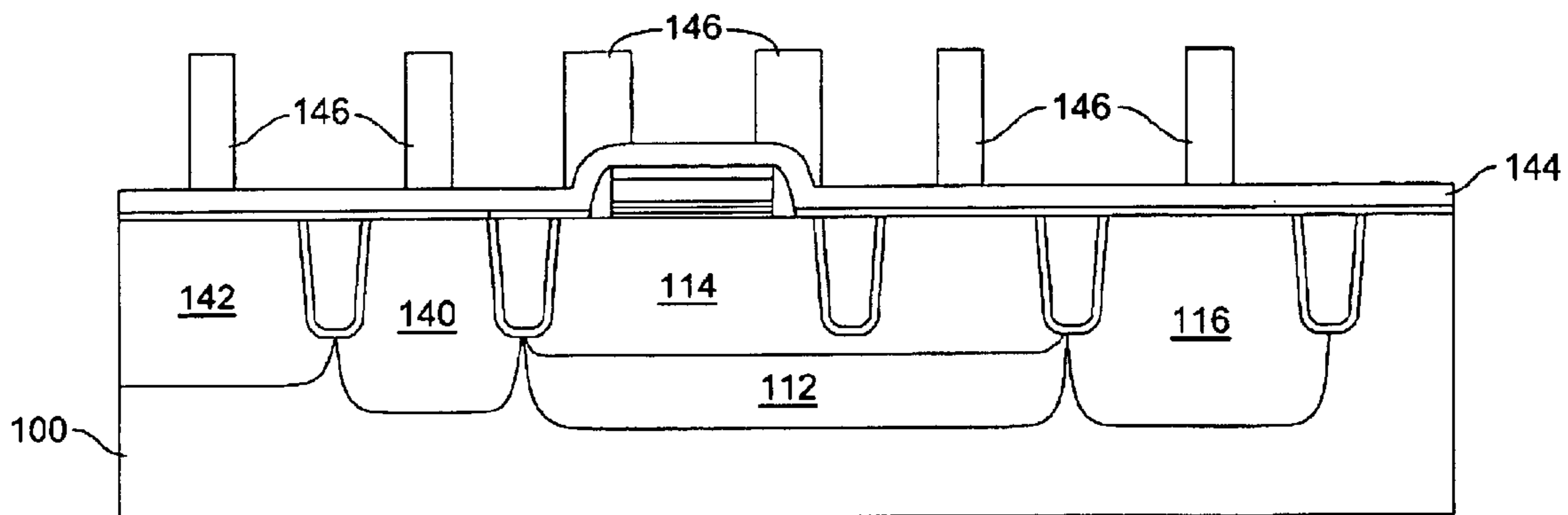


FIG. 15B

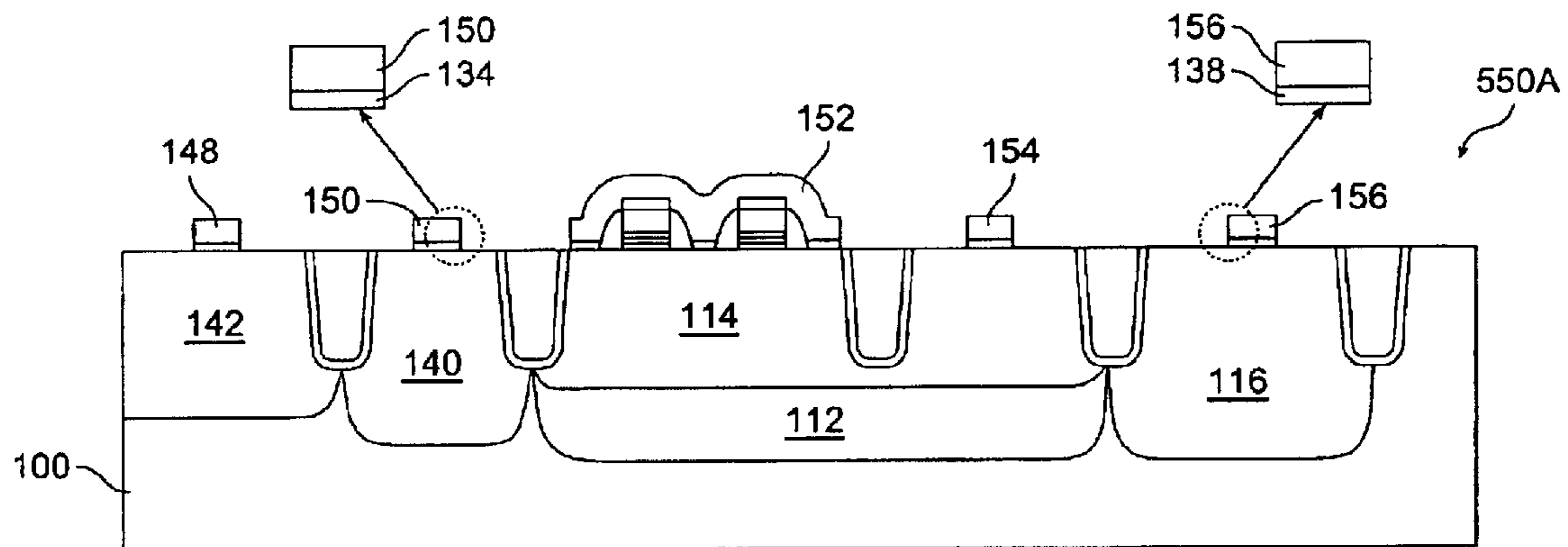


FIG. 16A

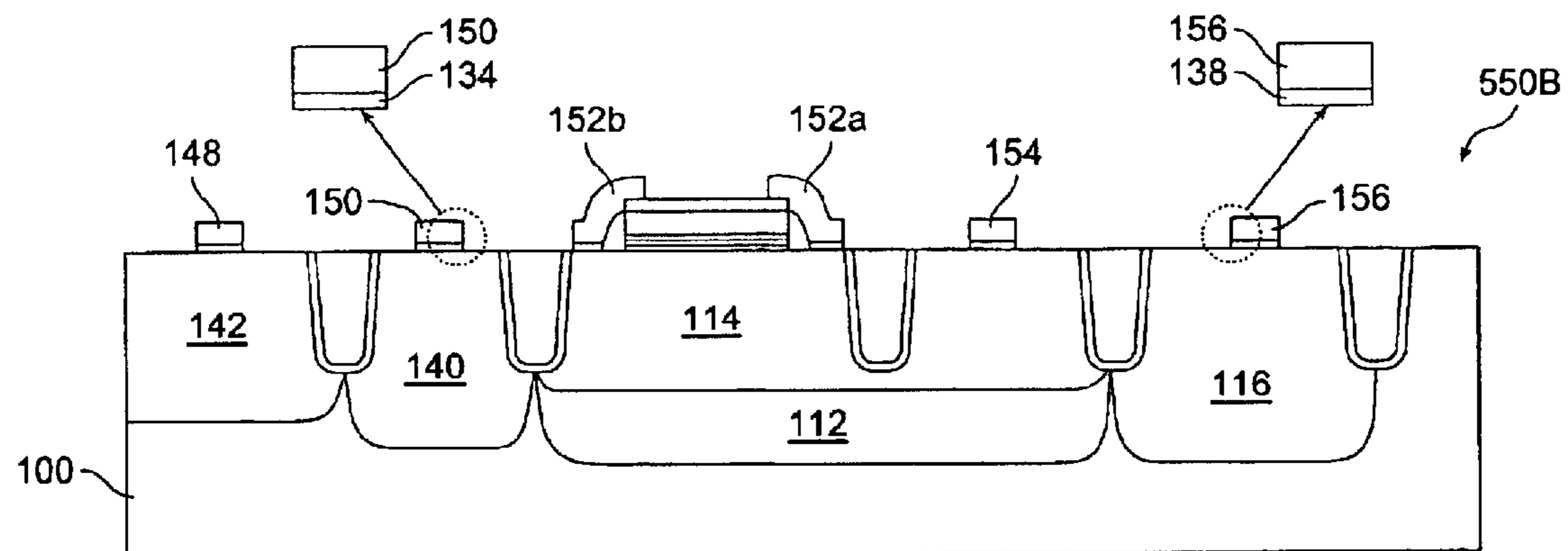


FIG. 16B

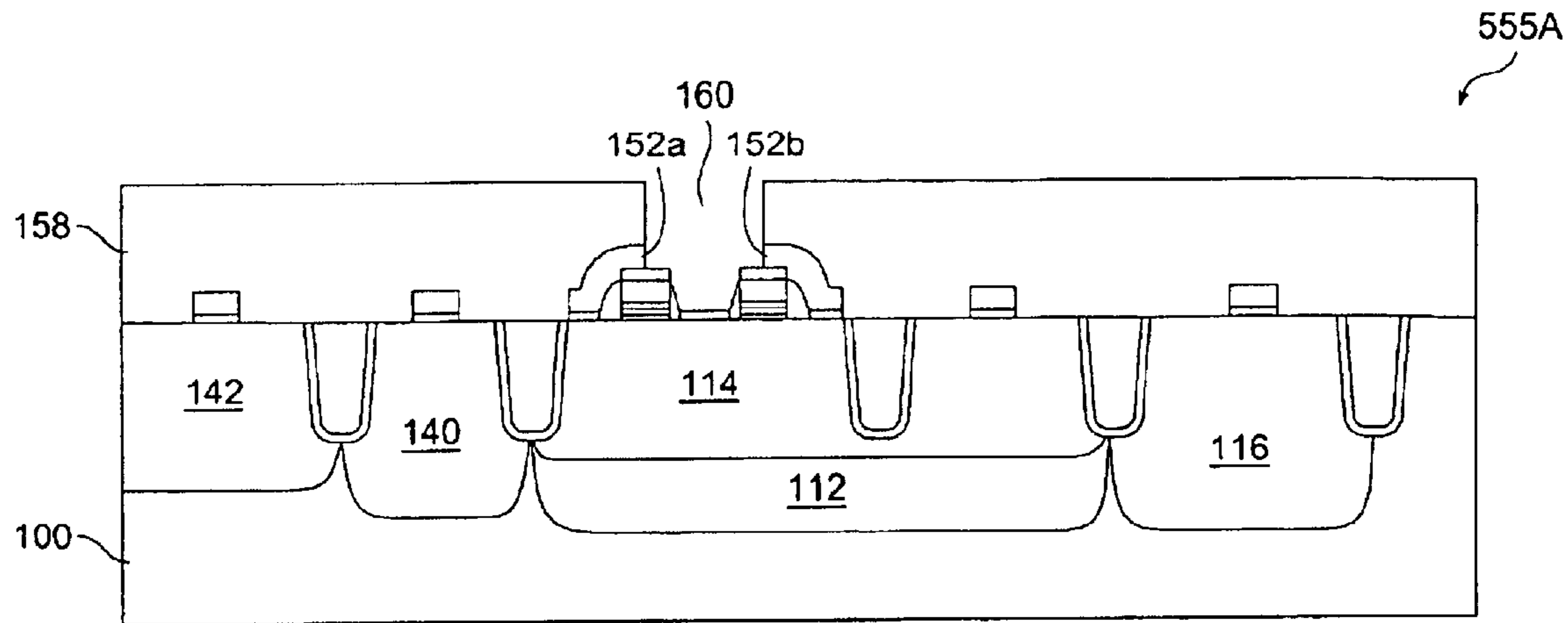


FIG. 17A

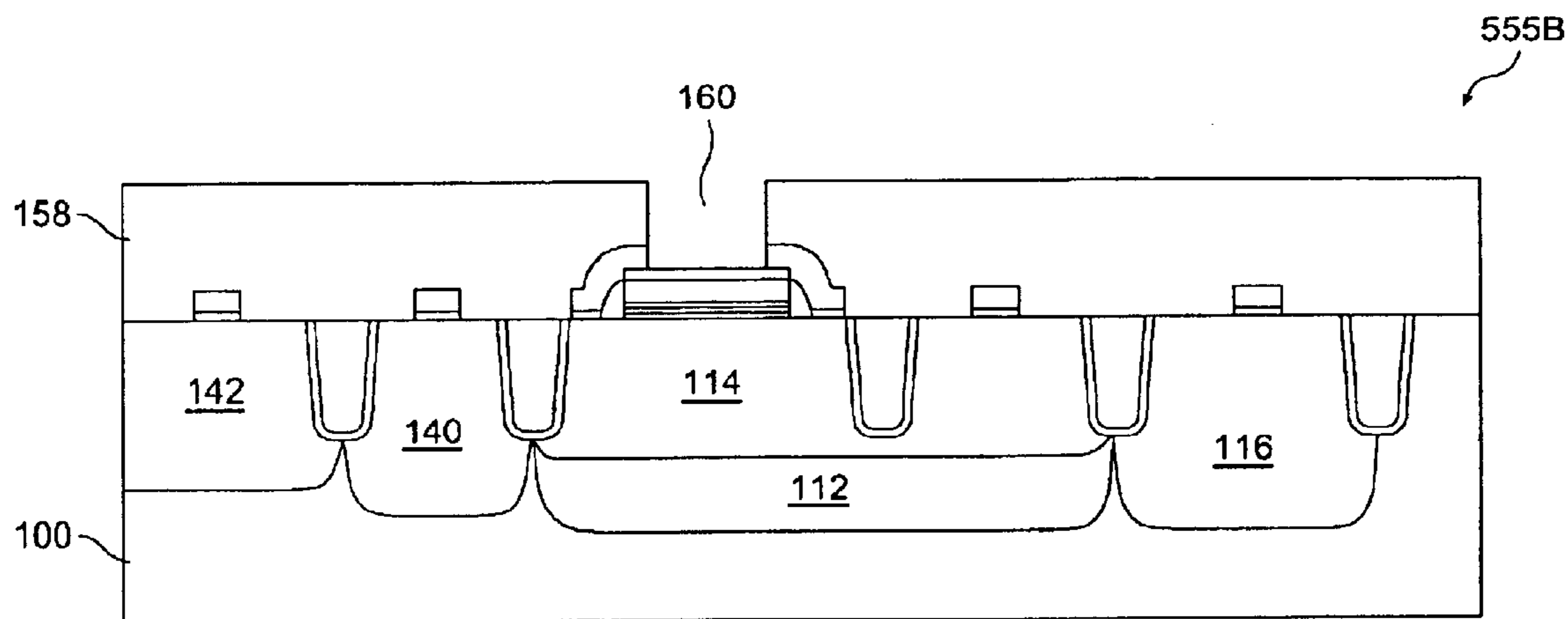


FIG. 17B

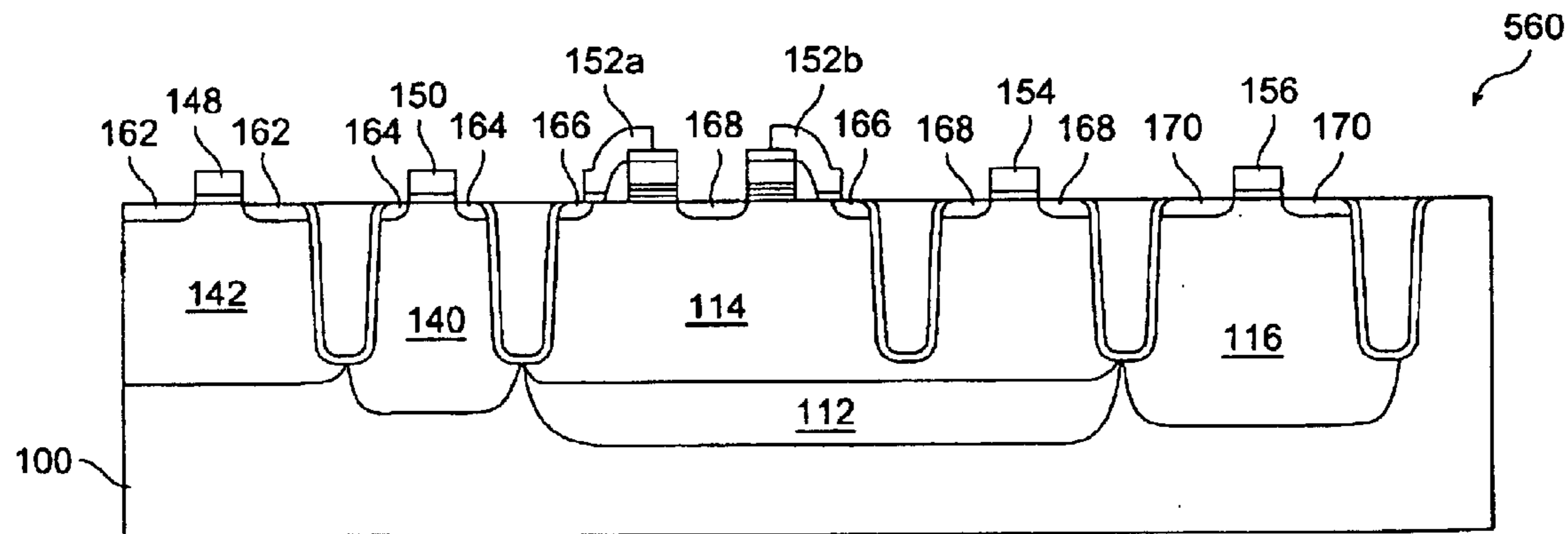


FIG. 18

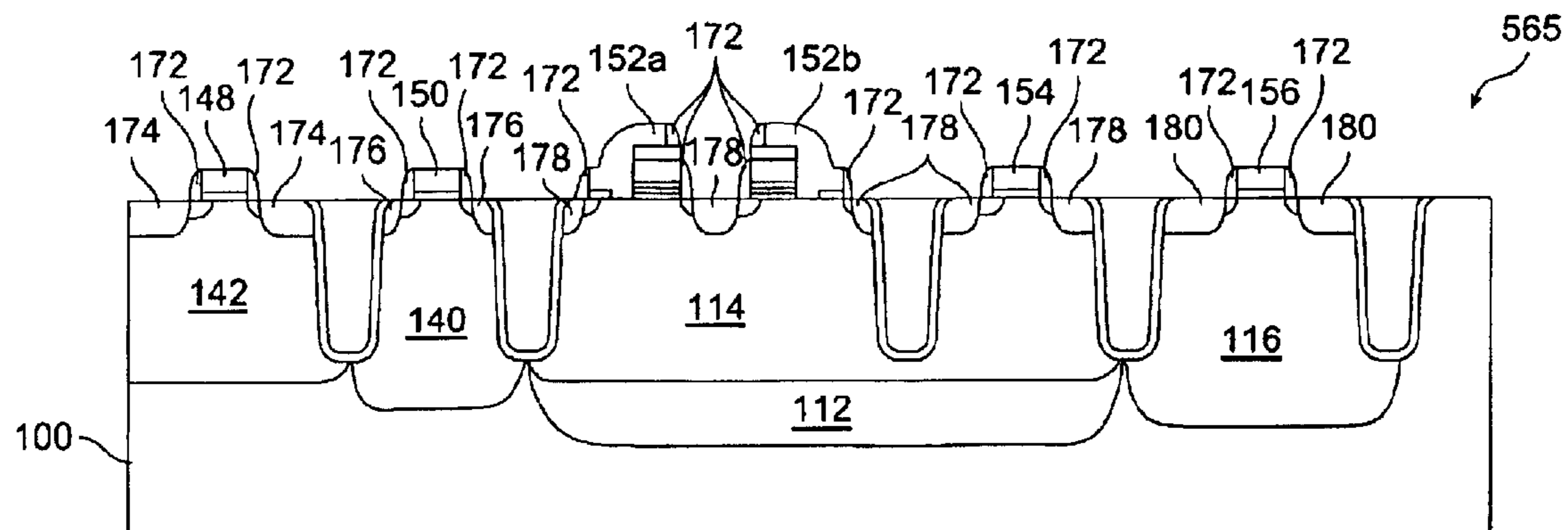


FIG. 19

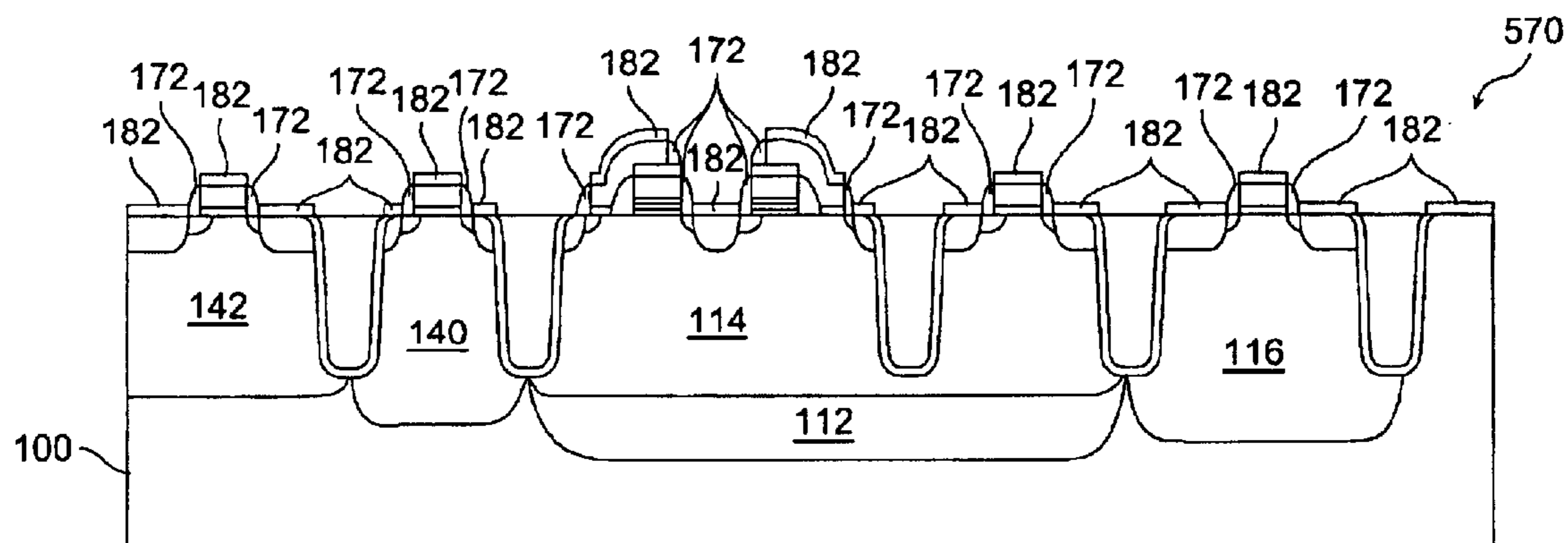


FIG. 20

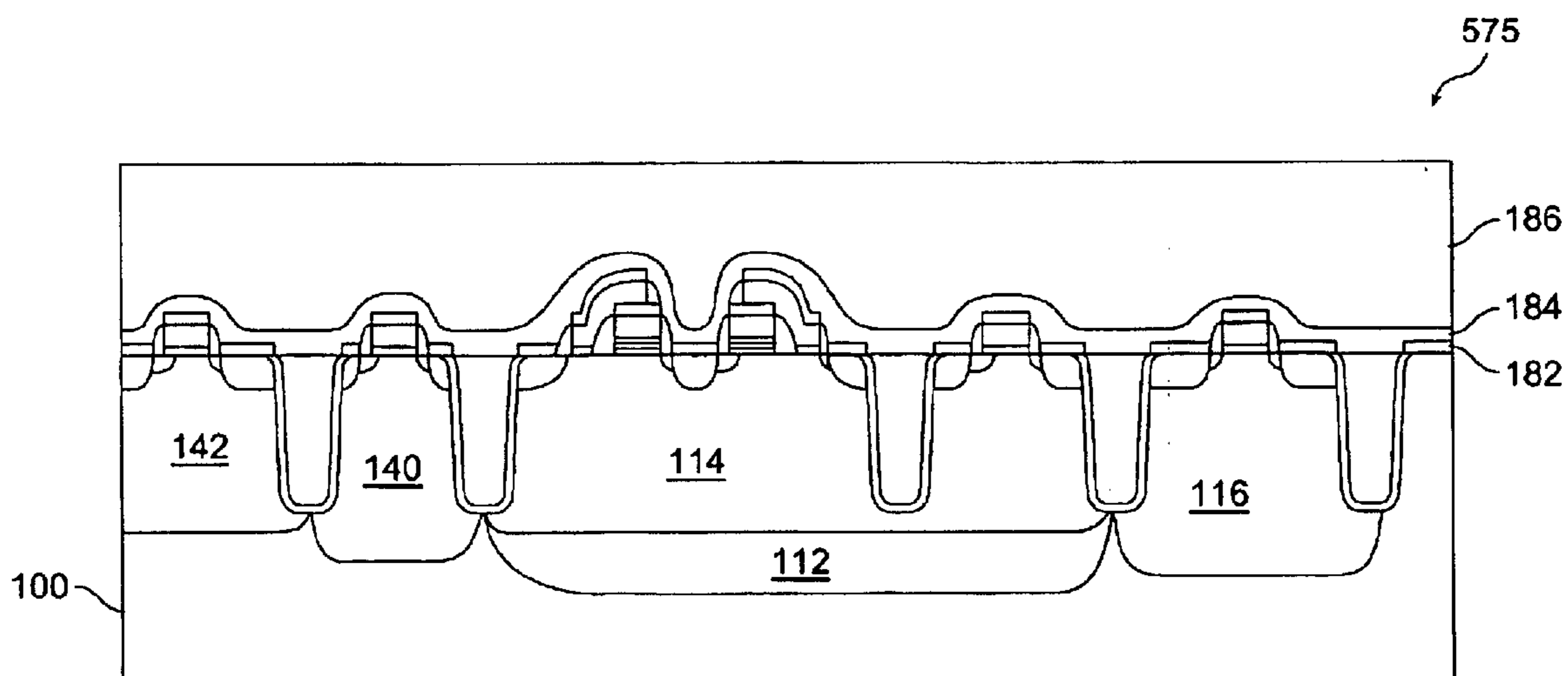


FIG. 21

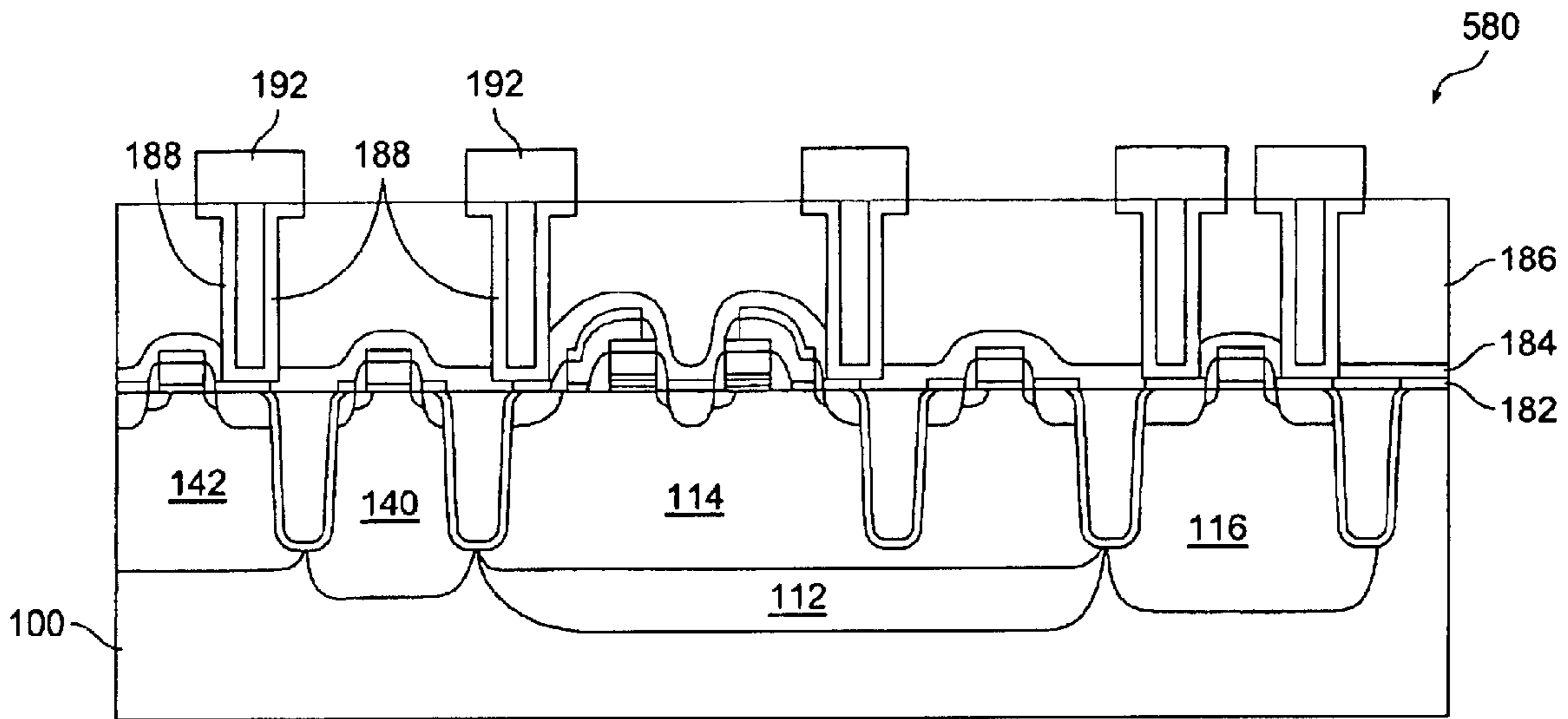


FIG. 22

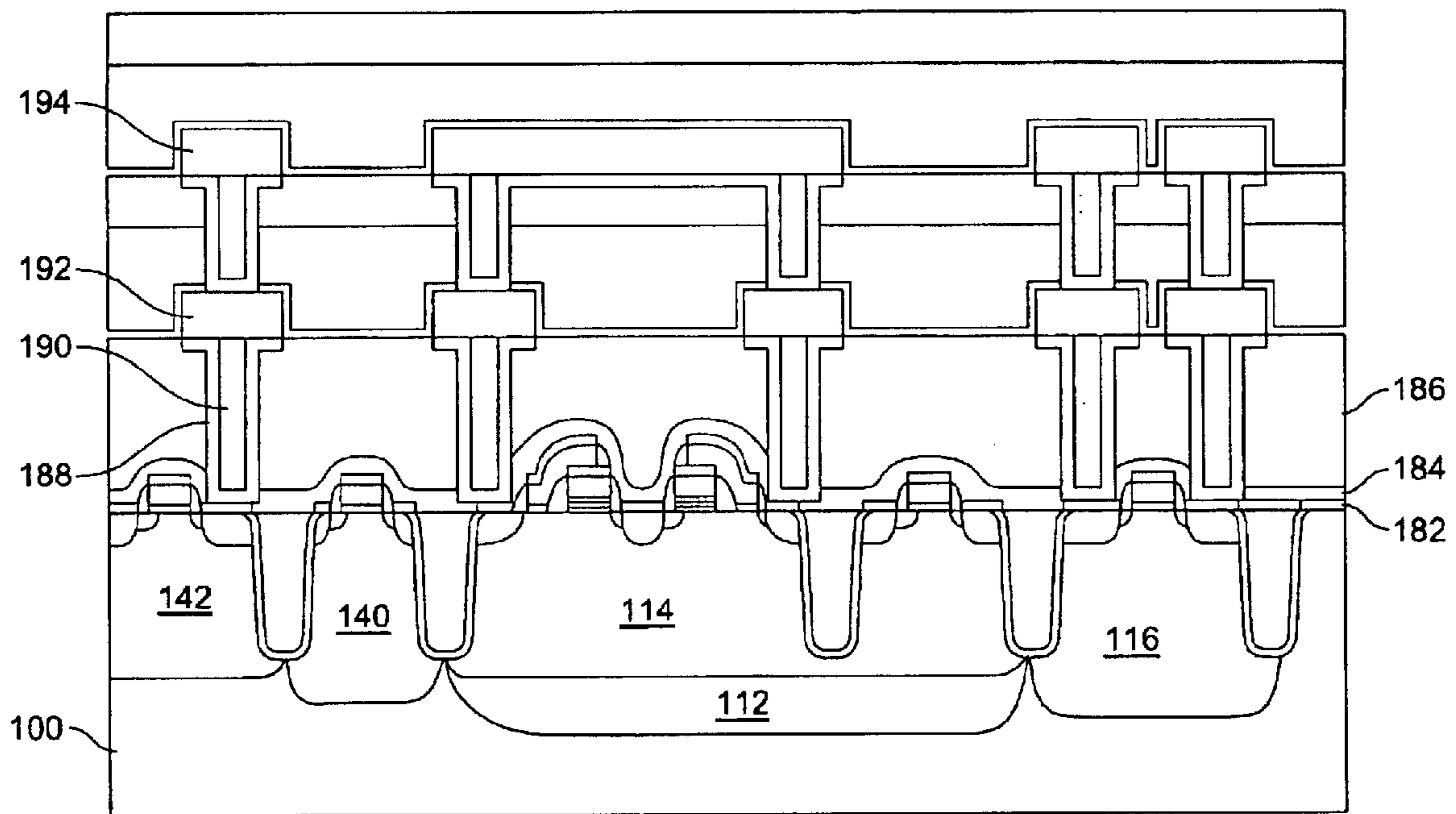


FIG. 23

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METHOD OF MANUFACTURING NON-VOLATILE MEMORY DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

The present application claims benefit of the filing date of U.S. provisional application No. 60/383,860 filed on May 28, 2002, entitled "Integrated RAM and Non-Volatile Memory" the entire content of which is incorporated herein by reference.

The present application is related to copending application Ser. No. 10/394,417, filed on Mar. 19, 2003, entitled "Non-Volatile Memory Device", Attorney Docket No. 021801-2.10US, assigned to the same assignee, and incorporated herein by reference in its entirety.

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

REFERENCE TO A "SEQUENCE LISTING," A TABLE, OR A COMPUTER PROGRAM LISTING APPENDIX SUBMITTED ON A COMPACT DISK.

Not Applicable

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor integrated circuits. More particularly, the invention provides a semiconductor memory that has integrated non-volatile and static random access memory cells. Although the invention has been applied to a single integrated circuit device in a memory application, there can be other alternatives, variations, and modifications. For example, the invention can be applied to embedded memory applications, including those with logic or micro circuits, and the like.

Semiconductor memory devices have been widely used in electronic systems to store data. There are generally two types of memories, including non-volatile and volatile memories. The volatile memory, such as a Static Random Access Memory (SRAM) or a Dynamic Random Access Memory (DRAM), loses its stored data if the power applied has been turned off. SRAMs and DRAMs often include a multitude of memory cells disposed in a two dimensional array. Due to its larger memory cell size, an SRAM is typically more expensive to manufacture than a DRAM. An SRAM typically, however, has a smaller read access time and a lower power consumption than a DRAM. Therefore, where fast access to data or low power is needed, SRAMs are often used to store the data.

Non-volatile semiconductor memory devices are also well known. A non-volatile semiconductor memory device, such as flash Erasable Programmable Read Only Memory (Flash EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM) or, Metal Nitride Oxide Semiconductor (MOS), retains its charge even after the power applied thereto is turned off. Therefore, where loss of data due to power failure or termination is unacceptable, a non-volatile memory is used to store the data.

Unfortunately, the non-volatile semiconductor memory is typically slower to operate than a volatile memory. Therefore, where fast store and retrieval of data is required, the non-volatile memory is not typically used. Furthermore, the non-volatile memory often requires a high voltage, e.g.,

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12 volts, to program or erase. Such high voltages may cause a number of disadvantages. The high voltage increases the power consumption and thus shortens the lifetime of the battery powering the memory. The high voltage may degrade the ability of the memory to retain its charges due to hot-electron injection. The high voltage may cause the memory cells to be over-erased during erase cycles. Cell over-erase results in faulty readout of data stored in the memory cells.

The growth in demand for battery-operated portable electronic devices, such as cellular phones or personal organizers, has brought to the fore the need to dispose both volatile as well as non-volatile memories within the same portable device. When disposed in the same electronic device, the volatile memory is typically loaded with data during a configuration cycle. The volatile memory thus provides fast access to the stored data. To prevent loss of data in the event of a power failure, data stored in the volatile memory is often also loaded into the non-volatile memory either during the configuration cycle, or while the power failure is in progress. After power is restored, data stored in the non-volatile memory is read and stored in the volatile memory for future access. Unfortunately, most of the portable electronic devices may still require at least two devices, including the non-volatile and volatile, to carry out backup operations. Two devices are often required since each of the devices often rely on different process technologies, which are often incompatible with each other.

To increase the battery life and reduce the cost associated with disposing both non-volatile and volatile memory devices in the same electronic device, non-volatile SRAMs and non-volatile DRAMs have been developed. Such devices have the non-volatile characteristics of non-volatile memories, i.e., retain their charge during a power-off cycle, but provide the relatively fast access times of the volatile memories. As merely an example, FIG. 1 is a transistor schematic diagram of a prior art non-volatile DRAM 10. Non-volatile DRAM 10 includes transistors 12, 14, 16 and EEPROM cell 18. The control gate and the drain of EEPROM cell 18 form the DRAM capacitor. Transistors 12 and 14 are the DRAM transistors. Transistor 16 is the mode selection transistor and thus selects between the EEPROM and the DRAM mode.

FIG. 2 is a transistor schematic diagram of a prior art non-volatile SRAM 40. Non-volatile SRAM 40 includes transistors 42, 44, 46, 48, 50, 52, 54, 56, resistors 58, 60 and EEPROM memory cells 62, 64. Transistors 48, 50, 52, 54 and resistors 58, 60 form a static RAM cell. Transistors 42, 44, 46, 56 are select transistors coupling EEPROM memory cells 62 and 64 to the supply voltage Vcc and the static RAM cell. Transistors 48 and 54 couple the SRAM memory cell to the true and complement bitlines BL and \overline{BL} .

EEPROM 18 of non-volatile DRAM cell 10 (FIG. 1) and EEPROM 62, 64 of non-volatile SRAM cell 40 (FIG. 2) may consume require a high programming voltage and thus may suffer from high-voltage related stress. Accordingly, a need continues to exist for a relatively small non-volatile memory device that, among other things, is adapted for use in a non-volatile SRAM or DRAM and consume less power than those known in the prior art.

While the invention is described in conjunction with the preferred embodiments, this description is not intended in any way as a limitation to the scope of the invention. Modifications, changes, and variations, which are apparent to those skilled in the art can be made in the arrangement, operation and details of construction of the invention disclosed herein without departing from the spirit and scope of the invention.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, a method of forming an integrated circuit in a semiconductor substrate, includes, in part, the steps of: forming at least two trench isolation regions in the semiconductor substrate, forming a first well between the two trench isolation regions, forming a second well between the two trench isolation regions and above the first well to define a body region, forming a first oxide layer above a first portion of the body region, forming a first dielectric layer above the first oxide layer, forming a first polysilicon layer—that forms a control gate of a non-volatile device—above the first dielectric layer, forming a second dielectric layer above the first polysilicon layer, forming a first spacer above the body region and adjacent said first polysilicon layer, forming a second oxide layer above a second portion of the body region that is not covered by the first spacer, forming a second polysilicon layer—that forms a guiding gate of the non-volatile device—above the second oxide layer, the first spacer and a portion of the second dielectric layer, forming a second spacer above the body region to define source and drain regions of the non-volatile device, and delivering n-type implants in the defined source and drain regions of the non-volatile device.

In some embodiments, the semiconductor substrate is a p-type substrate. In such embodiments, the first well is an n-well formed using a number of implant steps each using a different energy and doping concentration of phosphorous. Furthermore, in such embodiments, the second well is a p-well formed using a number of implant steps each using a different energy and doping concentration of boron. In some embodiments, the implant steps used to form the n-well and p-well are carried out using a single masking step.

In some embodiments, the first dielectric layer further includes an oxide layer and a nitride layer and the second dielectric layer is an oxide layer. Moreover, the thickness of the second oxide layer is greater than that of the first oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified transistor schematic diagram of a non-volatile DRAM, as known in the prior art.

FIG. 2 is a simplified transistor schematic diagram of a non-volatile SRAM, as known in the prior art.

FIG. 3 is a cross-sectional view of a non-volatile memory device, in accordance with one embodiment of the present invention.

FIG. 4 is a cross-sectional view of a semiconductor substrate in which an integrated circuit including the non-volatile memory device of FIG. 3 is formed.

FIG. 5 is a cross-sectional view of the semiconductor structure of FIG. 4 after a layer of pad oxide is formed thereon.

FIG. 6 is a cross-sectional view of the semiconductor structure of FIG. 5 after a layer of nitride is deposited on the pad oxide.

FIG. 7 is a cross-sectional view of the semiconductor structure of FIG. 6 after formation of trench isolation.

FIG. 8 is a cross-sectional view of the semiconductor structure of FIG. 7 after the trench isolations are filled with dielectric materials.

FIG. 9 is a cross-sectional view of the semiconductor structure of FIG. 8 after formation of an n-well and a p-well defining a body region in which the non-volatile device of FIG. 3 is formed.

FIG. 10 is a cross-sectional view of the semiconductor structure of FIG. 9 after a second n-well is formed adjacent the first n-well and p-well.

FIG. 11 is a cross-sectional view of the semiconductor structure of FIG. 10 after formation of various layers thereon.

FIG. 12A is a cross-sectional view of the semiconductor structure of FIG. 11 after a photo-resist mask has been formed to define the control gate of the non-volatile device, in accordance with a first embodiment of the present invention.

FIG. 12B is a cross-sectional view of the semiconductor structure of FIG. 11 after a photo-resist mask has been formed to define the control gate of the non-volatile device, in accordance with a second embodiment of the present invention.

FIG. 13A is a cross-sectional view of the semiconductor structure of FIG. 12A following etching steps and oxide spacer formation steps.

FIG. 13B is a cross-sectional view of the semiconductor structure of FIG. 13A following etching steps and oxide spacer formation steps.

FIG. 14A is a cross-sectional view of the semiconductor structure of FIG. 13A after a second-well, a third n-well and various gate oxide layers have been formed.

FIG. 14B is a cross-sectional view of the semiconductor structure of FIG. 13B after a second-well, a third n-well and various gate oxide layers have been formed.

FIG. 15A is a cross-sectional view of the semiconductor structure of FIG. 14A after a second poly layer has been deposited and photo-resist masks have been formed to define gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices.

FIG. 15B is a cross-sectional view of the semiconductor structure of FIG. 14B after a second poly layer has been deposited and photo-resist masks have been formed to define gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices.

FIG. 16A is a cross-sectional view of the semiconductor structure of FIG. 15A after various etching steps are carried out to form the gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices.

FIG. 16B is a cross-sectional view of the semiconductor structure of FIG. 15B after various etching steps are carried out to form the gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices.

FIG. 17A is a cross-sectional view of the semiconductor structure of FIG. 16A after a photo-resist mask has been formed to separate the guiding gates of the pair of non-volatile devices and to define their respective LDD regions.

FIG. 17B is a cross-sectional view of the semiconductor structure of FIG. 16B after a photo-resist mask has been formed to remove various dielectric layers from the exposed areas and to define LDD regions of the pair of non-volatile devices.

FIG. 18 is a cross-sectional view of the semiconductor structure of FIG. 17A or 17B after LDD implants.

FIG. 19 is a cross-sectional view of the semiconductor structure of FIG. 18 after formation of a second oxide spacer layer.

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FIG. 20 is a cross-sectional view of the semiconductor structure of FIG. 19 after formation of a salicide layer and source/drain implant steps.

FIG. 21 is a cross-sectional view of the semiconductor structure of FIG. 20 after layers of nitride and oxide have been deposited thereon.

FIG. 22 is a cross-sectional view of the semiconductor structure of FIG. 21 after formation of tungsten plugs and first metal layer.

FIG. 23 is a cross-sectional view of the semiconductor structure of FIG. 22 after formation of a second metal layer.

DETAILED DESCRIPTION OF THE INVENTION

According to the present invention, an improved non-volatile memory device and method is provided. Although the invention has been applied to a single integrated circuit device in a memory application, there can be other alternatives, variations, and modifications. For example, the invention can be applied to embedded memory applications, including those with logic or microcircuits, and the like.

FIG. 3 is a cross-sectional view of some of the regions of non-volatile memory device 200 (hereinafter alternatively referred to as device 200), in accordance with the present invention. Device 200 which is formed in, e.g., a p-type semiconductor substrate or a p-well formed in an n-type semiconductor substrate, includes, in part, a guiding gate 152a, a control gate 124, n-type source/drain regions 166 formed in p-well 114. Control gate 124, which is typically formed from polysilicon, is separated from p-type substrate or p-well layer 114 via oxide layer 118, nitride layer 120 and oxide layer 122. Guiding gate 152a, which is also typically formed from polysilicon, is separated from substrate 206 via layer 136. Layer 136 may be an oxide layer or oxinitride layer or any other dielectric layer. Guiding gate 152a partially extends over control gate 124 and is separated therefrom via oxide layer 126. A sequence of steps adapted to manufacture device 200 is described below. In the following, it is understood that similar elements or regions in the drawings are identified with similar reference numerals. Moreover, after various regions or elements in a drawing are identified with their respective reference numerals, the subsequent drawings may omit those reference numerals for simplification purposes.

FIG. 4 shows a semiconductor substrate 100 in which the non-volatile device 200 shown in FIG. 3 is formed. In the exemplary embodiment described above, substrate 100 is a p-type substrate. It is understood that in other embodiments, substrate 100 may be an n-type substrate. To form non-volatile device 200, a layer of pad oxide 102 having a thickness in the range of, e.g., 60–70 Å, is grown on substrate 100 using conventional thermal oxidation processes, as shown in FIG. 5. Next, as shown in FIG. 6, a layer of silicon-nitride 104 having a thickness in the range of, 1000 Å, is deposited on pad oxide layer 102. It is understood that the various layers and spacings shown in the figures are not drawn to scale. Next, using conventional masking and etching steps, shallow trenches 106 are formed in substrate 100, thereby forming structure 505 as shown in FIG. 7.

After shallow trenches 106 are formed, a layer of oxide having a thickness of, e.g., 150 Å, is grown over structure 505. This oxide is also grown in trenches 106. Next, a layer of TEOS having a thickness of, e.g., 5000–10,000 Å is deposited on the oxide. This TEOS layer is also deposited in trenches 106. Thereafter, using a planarization technique,

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such as chemical-mechanical polishing (CMP), the resulting structure is planarized. FIG. 8 shows the resulting structure 510 after the planarization process. As is seen from FIG. 8, as all the layers overlaying substrate 100, except for the oxide layer 108 and TEOS layer 110 formed in trenches 106, are removed.

Next, as shown in FIG. 9, using conventional photo-resist patterning and etching steps, n-well 112 and p-well 114 are formed. As seen from FIG. 9, n-well 112 is deeper than and formed before p-well 114. In some embodiments, a phosphorous implant with a concentration of $2.0e^{13}$ atoms/cm² and using an energy of 1.5 Mega-electron volts is used to form n-well 112. In such embodiments, five separate Boron implants are used to form p-well implant 114. The first boron implant made using a concentration of $2.0e^{13}$ atoms/cm² and an energy of 600 Kilo-electron volts. The second boron implant is made using a concentration of $1.0e^{13}$ atoms/cm² and an energy of 300 Kilo-electron volts. The third boron implant is made using a concentration of $4.0e^{13}$ atoms/cm² and an energy of 160 Kilo-electron volts. The fourth boron implant is made using a concentration of $6.0e^{13}$ atoms/cm² and an energy of 70 Kilo-electron volts. The fifth boron implant is made using a concentration of $1.0e^{13}$ atoms/cm² and an energy of 300 Kilo-electron volts. The above phosphorous and boron implants are performed using the same masking step.

Because, the phosphorous implant performed using a relatively high energy, relatively few phosphorous impurities may remain in p-well 114. Therefore, in accordance with the present invention, advantageously very few boron impurities in p-well 114 are neutralized (i.e., compensated) by the phosphorous impurities. After the above implants, a thermal anneal is performed at the temperature of, e.g., 1050° C. for a period of, e.g., 30 seconds. The resulting structure 515 is shown in FIG. 9.

Next, as shown in FIG. 10, a second n-well 116 is formed adjacent n-well 112 and p-well 114. N-well 116 that extends to the surface of substrate 100 has a depth that is substantially the same as the combined depth of n-well 112 and p-well 114. The resulting structure 520 is shown in FIG. 10. As is seen from FIG. 10, n-well 116 and deep n-well 112 are connected in substrate 100.

Next, as shown in FIG. 11, a layer of thermal oxide 118 having a thickness in the range of, e.g., 15–40 Å, is grown over structure 520. Thereafter, a layer of nitride 120 having a thickness in the range of, e.g., 40–120 Å, is formed over oxide layer 118. Next, a layer of CVD oxide 122 having a thickness in the range of, e.g., 40–70 Å, is deposited over nitride layer 120. Thereafter, during a densification step, the resulting structure is heated to a temperature of, e.g., 800° C. for a period of, e.g., 0.5 to 1 hour. After the densification step, a layer of polysilicon (alternatively referred to herein below as poly) 124 having a thickness in the range of, e.g., 2000–3000 Å is deposited over CVD oxide layer 122. Poly layer 124 may be doped in-situ or using other conventional doping techniques. Thereafter, a layer of nitride-oxide layer 126 having a combined thickness in the range of, e.g., 500–1500 Å is formed over poly layer 124. The thickness of oxide layer in the oxide-nitride layer 126 may be between, e.g., 100–200 Å. FIG. 11 shows structure 525 that is formed after the above growth and deposition steps are performed on structure 520.

Next, using standard photo-resist deposition, patterning and etching steps, photo-resists masks 128 are formed over oxide-nitride layer 126. In accordance with a first embodiment, photo-resists mask 128 includes two separate

pieces, as shown in FIG. 12A. In accordance with a second embodiment, photo-resists mask 128 includes one continuous piece, as shown in FIG. 12B. The resulting structures 530A and 530B are shown in FIGS. 12A and 12B. Mask 128 is subsequently used to define the control gates of the non-volatile devices formed in substrate 100. As described further below, in accordance with the first embodiment, two masking steps are used to form the control gate and one masking step is used to form the guiding gate of the non-volatile device. In accordance with the first embodiment, one masking step is used to form the control gate and two masking steps are used to form the guiding gate of the non-volatile device. Additional differences between the two embodiments are described below, and are shown in FIGS. 13–17.

Next, using conventional etching techniques, such as reactive ion etching, all the various layers grown or deposited on substrate 100, namely layers 118, 120, 122, 124 and 126 are removed from substantially all regions down to the surface of substrate 100 except for the regions positioned below masks 128. Thereafter, photo-resist masks 128 are also removed. Next, a layer of gate oxide 130 is thermally grown. In some embodiments, gate oxide layer 130 has a thickness in the range of, e.g., 100–200 Å. As is known to those skilled in the art, during this thermal oxidation, portions of polysilicon layer 124 are also oxidized, thereby causing the formation of rounded oxide regions 132, commonly referred to as spacers. Structure 535A of FIG. 13A shows the result of performing these steps on structure 530A, in accordance with the first embodiment. Structure 535B of FIG. 13B shows the result of performing these steps on structure 530B, in accordance with the first embodiment. It is understood that the drawings do not show some of the intermediate steps involved in forming structure 535A and 535B from structures 530A and 530B respectively.

Next, using conventional anisotropic etching techniques, oxide layer 130 overlaying substrate 100 is removed as a result of which spacers 132 are also partially etched. Next, using conventional masking and ion implantation step highly doped p-well region 140 is formed (see FIGS. 14A and 14B). In some embodiments, four separate boron implants are used to form p-well implant 140. The first boron implant is made using a concentration of $3.3e^{12}$ atoms/cm² and an energy of 20 Kilo-electron volts (Kev). The second boron implant is made using a concentration of $6.5e^{12}$ atoms/cm² and an energy of 70 Kev. The third boron implant is made using a concentration of $3.4e^{12}$ atoms/cm² and an energy of 180 Kev. The fourth boron implant is made using a concentration of $3.5e^{13}$ atoms/cm² and an energy of 500 Kilo-electron volts.

Next using conventional masking and ion implantation steps, highly doped n-well region 142 is formed (see FIGS. 14A and 14B). In some embodiments, four separate phosphorous implants are used to form n-well implant 142. The first phosphorous implant is made using a concentration of $5.7e^{12}$ atoms/cm² and an energy of 50 Kev. The second phosphorous implant is made using a concentration of $6.6e^{12}$ atoms/cm² and an energy of 150 Kev. The third phosphorous implant is made using a concentration of $5.0e^{12}$ atoms/cm² and an energy of 340 Kev. The fourth phosphorous implant is made using a concentration of $4.0e^{13}$ atoms/cm² and an energy of 825 Kilo-electron volts. After the above implants, a thermal anneal is performed at the temperature of, e.g., 1000° C. for a period of, e.g., 10 seconds.

Thereafter using several masking steps, three layers of oxide thickness each having a different thickness are thermally grown. In the surface regions identified with reference

numeral 134, the oxide layer has a thickness in the range of, e.g., 35–40 Å. The semiconductor substrate underlying oxide layer 134 is used to form core transistors having relatively high speed. In the region identified by reference numeral 136, the oxide layer has a thickness in the range of, e.g., 60–80 Å. The semiconductor substrate underlying oxide layer 136 and overlaying p-well 114 is used to form high-voltage non-volatile devices. In the region identified by reference numeral 138, the oxide layer has a thickness in the range of, e.g., 160–250 Å. The semiconductor substrate underlying oxide layer 138 is used to form high-voltage transistors, such as Input/Output transistors. The process of making multiple, e.g. 3, layers of oxide each with a different thickness is known to those skilled in the art and is not described herein. In some other embodiments, oxide layers 136 and 138 have the same thickness in the range of, e.g., 160–250 Å. Structure 540A of FIG. 14A shows the result of performing these steps on structure 535A of FIG. 13A, in accordance with the first embodiment. Structure 540B of FIG. 14B shows the result of performing these steps on structure 535B of FIG. 13B, in accordance with the second embodiment. It is understood that the drawings do not show some of the intermediate steps involved in forming structure 540A from structure 535A and some of the intermediate steps involved in forming structure 540B from structure 535B.

Next, as shown in FIGS. 15A and 15B, a layer of polysilicon 144 having a thickness in the range of, e.g., 2200–3200 Å, is deposited. Thereafter using standard photo-resist masking and patterning techniques, photo-resists masks 146 are formed over polysilicon layer 144. Structure 545A of FIG. 15A shows the result of performing these steps on structure 540A of FIG. 14A, in accordance with the first embodiment. Structure 545B of FIG. 15B shows the result of performing these steps on structure 540B of FIG. 14B, in accordance with the second embodiment.

Next, using conventional etching steps, polysilicon layer 144 and oxide layer 134, 136 and 138 are removed from all regions except those positioned below masks 146. Structure 550A of FIG. 16A shows the result of performing these steps on structure 545A of FIG. 15A, in accordance with the first embodiment. Structure 550B of FIG. 16B shows the result of performing these steps on structure 545B of FIG. 15B, in accordance with the second embodiment. Poly gate 148 is shown as overlaying gate oxide layer 134 formed above n-well 142. Poly gate 150 is shown as overlaying gate oxide layer 134 formed above p-well 140. Poly gate 154 is shown as overlaying gate oxide layer 138 formed above p-well 114. Poly gate 156 is shown as overlaying gate oxide layer 138 formed above n-well 116. Poly gates 148 and 150 respectively form the gates of low-voltage high-speed PMOS and NMOS transistors. Poly gates 154 and 156 respectively form the gates of high-voltage NMOS and PMOS transistors.

In accordance with the first embodiment 550A shown in FIG. 16A and as described further below, poly gate 152 is subjected to additional masking steps to form the guiding gates of a pair of non-volatile devices. Poly gate 152 of FIG. 16A is shown as fully overlaying gate oxide layers 136, 138 formed positioned below it. In accordance with the second embodiment shown in FIG. 16B, poly gates 152A and 152B respectively form the guiding gates of a pair of non-volatile devices and each is shown as overlaying, in part, gate oxide layer 136 formed below it.

Next, using known photo-resist deposit and patterning techniques, photo-resist masks 158 are formed. Structure 555A of FIG. 17A shows the result of performing these steps on structure 550A of FIG. 16A, in accordance with the first

embodiment. Structure **555B** of FIG. **17B** shows the result of performing these steps on structure **550B** of FIG. **16B**, in accordance with the second embodiment. Via **160** is formed in both structures.

In accordance with the first embodiment, using either wet etching or reactive ion etching polysilicon **152** exposed in via **160** is removed from structure **555A**. (see FIG. **18**). Following this etching, and as seen in FIG. **18**, two poly gates **152a** and **152b** remain, each forming the guiding gate of a different non-volatile device. Next, oxide spacers **132** and oxide layer **138** exposed in via **160** are also etched, thereby exposing the surface of p-well **114** in via **160**.

In accordance with the second embodiment, layers **118**, **120**, **122**, **124** and **126** disposed in via **160** are etched from structure **555B** using standard etching steps. (see FIG. **18**) The steps described below are common to both embodiments and thus no distinction in the drawings is made hereinafter.

Next, using several masking steps, low voltage p-type lightly doped (LDD) regions **162**, low-voltage n-type LDD regions **164**, intermediate voltage n-type LDD regions **166**, high voltage n-type LDD region **168**, and high voltage p-type LDD region **170** are formed. The resulting structure **560** is shown in FIG. **18**.

Next, as shown in FIG. **19**, using conventional processing steps, side-wall spacers **172** are formed. In some embodiments, each side-wall spacer **172** is made from oxide and each has a thickness in the range of, e.g., 500–1500 Å. Thereafter, several p⁺ and n⁺ masking step are performed to form p⁺ source/drain regions **174**, n⁺ source/drain regions **176**, n⁺ source/drain regions **178**, and p⁺ source/drain regions **180**. In some embodiments, the doping concentration of boron used to form p⁺ source/drain regions **174** is the same as that used to form p⁺ source/drain regions **180**. In some other embodiments, the doping concentration of boron used to form p⁺ source/drain regions **174** is different from that used to form p⁺ source/drain regions **180**. In some embodiments, the doping concentration of arsenic used to form n⁺ source/drain regions **176** is the same as that used to form n⁺ source/drain regions **178**. In some other embodiments, the doping concentration of arsenic used to form n⁺ source/drain regions **176** is different from that used to form n⁺ source/drain regions **178**. The resulting structure **565** is shown in FIG. **19**.

Next, salicide is deposited over structure **565**. Thereafter, a high-temperature anneal cycle is carried out. As is known to those skilled in the art, during the anneal cycle, salicide reacts with silicon and polysilicon, but not with silicon-nitride or silicon-oxide. In the resulting structure **570**, which is shown in FIG. **20**, salicided layers are identified with reference numeral **182**.

Next, a layer of nitride **184** is deposited over structure **570** and a layer of oxide **186** is deposited over nitride layer **184**, as shown in FIG. **21**.

Next, vias are formed in nitride layer **184** and oxide layer **186** to expose the underlying salicide layers. Thereafter, a barrier metal, such as titanium-nitride **188** is sputter-deposited partly filling the vias. Next, tungsten **190** is deposited over titanium-nitride layer to fill the remainder of the via. The deposited tungsten is commonly referred to as tungsten Plug. Next, using a CMP technique, the tungsten deposited structure is planarized. Next, a metal such as aluminum or copper is deposited and patterned over the planarized structure. The resulting structure **580** is shown in FIG. **22**. As is seen from FIG. **22**, each via has disposed therein a titanium-nitride layer **188** and tungsten layer **190**.

The deposited and patterned Al or Copper layers are identified with reference numeral **192**.

The description above is made with reference to a single metal layer. However, it is understood that additional metal layers may be formed over metal layers **192** in accordance with known multi-layer metal processing techniques. For example, FIG. **23** shows structure **580** after it is processed to include a second metal layer **194** that is separate from metal layer **192** via layers of dielectric materials.

What is claimed is:

1. A method of making an integrated circuit in a semiconductor substrate, the method comprising:

forming at least two trench isolation regions in the semiconductor substrate;

forming a first well between the two trench isolation regions;

forming a second well between the two trench isolation regions and above the first well to define a body region;

forming a first oxide layer above a first portion of the body region;

forming a first dielectric layer above, the first oxide layer;

forming a first polysilicon layer above said first dielectric layer, said first polysilicon layer forming a control gate of a non-volatile device;

forming a second dielectric layer above the first polysilicon layer;

forming a first spacer above the body region and adjacent said first polysilicon layer;

forming a second oxide layer above a second portion of the body region not covered by said first spacer;

forming a second polysilicon layer over the second oxide layer, the first spacer and a portion of the second dielectric layer; said second polysilicon layer forming a guiding gate of the non-volatile device;

forming a second spacer above the body region to define source and drain regions of the non-volatile device; and delivering n-type implants in the defined source and drain regions of the non-volatile device.

2. The method of claim 1 further comprising:

forming a layer of photo-resist after forming the second polysilicon layer and prior to delivering the n-type implants, wherein said photo-resist layer fully covers the second polysilicon layer and partly covers the second dielectric layer; and

thereafter removing the second dielectric layer disposed above the first poly layer and that is not covered by the photo-resist layer; and

thereafter removing the first polysilicon layer disposed below the removed second dielectric layer, and

thereafter removing the first dielectric layer disposed below the removed first polysilicon dielectric layer to expose the p-well surface.

3. The method of claim 2 further comprising:

performing LDD implants prior to delivering n-type implants in the defined source and drain regions of the non-volatile device, wherein a doping concentration of the LDD implant in one of the source and drain regions of the non-volatile device is greater than a doping concentration of the LDD implant in the other one of the source and drain regions of the non-volatile device.

4. The method of claim 3 wherein said first dielectric layer further includes an oxide layer and a nitride layer.

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5. The method of claim **4** wherein said second dielectric layer further includes an oxide layer and a nitride layer.

6. The method of claim **5** wherein said first well is an n-well and said second well is a p-well.

7. The method of claim **6** wherein said n-well is formed using at least one implant step.

8. The method of claim **7** wherein said p-well is formed using at least two implant steps each having associated therewith a different energy and doping concentration.

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9. The method of claim **8** wherein the at least two implant steps used to form the n-well and the at least two implant steps used to form the p-well region are performed using a same mask.

10. The method of claim **9** wherein said second oxide layer has a thickness greater than the thickness of the first oxide layer.

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